High Efficiency Analog and Digital Circuits for Wireless Applications Based on III-V HEMTs

Abstract

There has been an increasing demand for the design of high data rate transmitters and receivers for satellites, military remote sensing applications, phase array radar, and mobile applications. The radio frequency (RF) transceiver is being pushed to operate at higher frequencies and wider bandwidths, and with Orthogonal Frequency Division Modulation (OFDM) standards, including 5G application. These advanced modulations have very high Peak-to-Average Power Ratios (PAPRs) and variable envelope. The interest has increased to design circuits with GaN and GaAs for high power levels in the last decade. The RF front-end of the transceiver typically are designed in GaN to provide high transmitter power, and GaAs is used for the digital interface to save power consumption.

An enormous number of active radiating elements are used in radar systems to achieve the required precision of beamforming. Therefore, a huge number of control lines are required to control each element which is difficult to handle as the number of bits increases. In active electronically scanned phased array satellites, the amplitude and phase are controlled electrically, which is applicable by the MMIC core chip (CC) circuit which consists of RF and digital parts. One of the most important blocks in the digital part is the serial-to-parallel (S2P) circuit, which helps to reduce the number of control lines, thus reducing the occupied area, power consumption, and cost. However, the occupied area and power consumption increase by increasing the number of controlling bits, which is the most challenge in the design of SIPO. The main goal is to achieve low power consumption and small occupied area. A 18-bit serial-to-parallel converter is designed and implemented using 0.25 µm pHEMT GaAs WIN technology for an X-band core-chip. The S2P, designed from DC up to 50 MHz, shows good results. The power consumption is 43 mW with a supply voltage of -3.3 V. The differential structure with pull-up resistance is considered in the design of S2P to improve the power consumption. In addition, the drain and source transistors are shared to reduce the occupied area.

Concerning the high-frequency range RF part, the power amplifier (PA) is one of the most important blocks in the transmitter and receiver systems, since PA consumes a large part of the current of the whole system. On the other hand, advanced modulations are used in the new generation standards that have variable envelope and high PAPR, so PAs with high efficiency are required. The first part, a hybrid power amplifier with GaN CGH40010F Wolfspeed devices has been designed for 5G applications. After that, Doherty power amplifiers are developed and measured to improve efficiency at the back-off point for S-band frequency. In the DPA designs, the effect of frequency on the inverted impedance network (IIN) and also the effect of parasitic elements when the auxiliary transistor is OFF have been investigated in class-AB mode. To improve the bandwidth, the class-J operation mode is also considered, and the output matching network is designed directly and the IIN network is embedded in it. The results of both designs show over 43 dBm output power with efficiency at the back-off point and saturation over 44 % and 60 %, respectively, at frequency of 3.5 GHz.

Then, the transmitter and receiver for S-band frequency are developed, simulated, and implemented for satellite applications. The main goal of this implementation is to design and analyze the front end of the transceiver for CubeSats. Among the possible implementations, the first architecture considered is the classical approach based on up and down frequency conversions, for TX and RX, respectively, using a mixer and local oscillator to convert the baseband signal to S-band, together with a power amplifier to improve the output power. The required components available in the market are investigated and simulated in this design. In addition, each part is analyzed theoretically in detail. To validate the above concepts, a test board for the front-end part is designed and implemented. For the transmitter, the output power is 36 dBm while the drain efficiency is achieved around 50 %. Also, in the receiver, the output power is 22 dBm while the efficiency is higher than 50 %.