Memristor-Assisted Background Calibration for SAR ADCs: A Feasibility Study

Memristor-Assisted Background Calibration for SAR ADCs: A Feasibility Study

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***Abstract*—This paper proposes a memristor-assisted sign-based background calibration scheme for analog-to-digital converters (ADCs). The scheme was implemented and validated in a 12-bit asynchronous successive approximation register (SAR) ADC, which consists of a hybrid binary weighted/R-2R digital-to-analog converter (binary/R-2R DAC) and other peripheral circuits. This hybrid DAC, in which one redundancy bit is introduced, is built with a memristor and standard polysilicon resistors. The proposed calibration technique can detect the errors caused by DAC mismatches and correct them by adjusting the resistance of the memristor (memristance[1]) in a feedback loop. The implemented circuit takes the memristor's advantages such as small area and resistance switching property. The proposed scheme has been designed and simulated in a standard 180 nm CMOS process. Eventually, a monolithic CMOS/memristor chip will be fabricated with the CMOS part processed at a standard foundry and the memristors integrated through post-CMOS processing in house. Simulation results demonstrate the feasibility of exploiting memristors to improve the linearity of high-resolution SAR ADCs. The designed calibration scheme can effectively reduce the integral non-linearity (INL) and differential non-linearity (DNL) of the 12-bit SAR ADC.**

***Index Terms*—Memristor, Memristor-assisted calibration, Hybrid DAC, SAR ADC.**

I. Introduction

A memristor, which was first postulated by Leon Chua in 1971, is a two-terminal device that represents the relationship between electric charge and magnetic flux [1]. In 2008, the first physical memristor device was realised in Hewlett-Packard (HP) Laboratory, and it exhibits a resistance switching property correlating to amplitude, frequency, and polarity of applied voltages [2]. Since then, the memristor has become the focus of many studies. Over the last decade, as CMOS downscaling is approaching its physical limits, the memristor has been considered as one of the emerging devices beyond CMOS, and its potential has been proven in various applications such as non-volatile memories and in-memory computing, etc [3–8]. The capability of integrating the nanoscale memristors with the CMOS technology makes the memristor an ideal candidate in next-generation hybrid System-on-a-Chip (SoC) designs. The memristor's properties such as small feature size down to 2 nm [9], resistance tuning, and non-volatility provide breakthroughs and potential solutions for traditional analog and digital circuit designs [10].

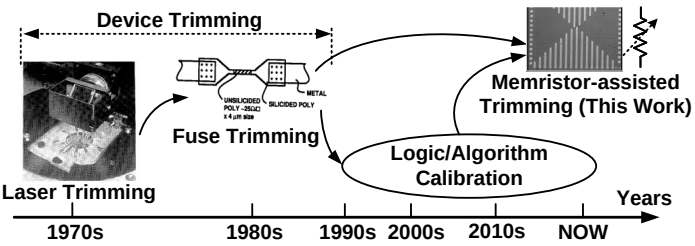

Fig. 1: Development of calibration techniques for data converters. The laser trimming is demonstrated in [16], and the fuse trimming is demonstrated in [17].

The performance of many CMOS circuits has benefited from advanced CMOS technology, and one example is the successive approximation (SAR) ADC. While SAR ADCs are energy efficient, their resolution is typically limited by element matching, which leads to mismatch and offset issues [11]. The mismatch issue can be mitigated by increasing the element size, but this will decrease the ADC's efficiency (i.e., chip area, power consumption, and latency). For instance, the area of the intrinsic DAC has to be scaled up four times for one extra effective bit to meet the matching requirements in capacitive SAR ADCs [12]. To deal with these limitations, various calibration techniques have been proposed to pursue higher resolution by trading off area, power, circuit complexity, and speed [11, 13–15].

Fig. 1 shows the development of existing calibration techniques over the past decades. Laser trimming and fuse trimming are the earliest calibration methods for data converters, and they both perform the calibration by changing the characteristics of the fundamental circuit elements (i.e., resistors).

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[1]Memristance is defined as the resistance of the memristor

However, these methods suffered from different drawbacks. Laser trimming requires a laser and thin-film process, which raises the complexity of fabrication and packaging. The laser also suffers from drifting issue [18]. As for fuse trimming, probe pads often limit the efficacy of calibration. Although there are techniques to overcome this problem [18], fuse trimming is still an irreversible operation and brings difficulties to ADC users. Furthermore, both trimming methods increase the cost of the ADC design. After the 1990s, most calibration methods are based on digital logic and algorithms. Besides existing calibration techniques, the memristor has the potential to be adopted as a trimming device for analog adjustments as well as a memory device that facilitates calibration logic and algorithms. Notably, memristors can be integrated into the CMOS back end of line, and thus monolithic chips can be developed [19], making the memristor-assisted trimming a promising solution for ADC calibration.

In this paper, we propose a memristor-assisted sign-based background calibration scheme for SAR ADCs. We implemented this new calibration technique in a 12-bit asynchronous SAR ADC and validated its effectiveness in improving linearity and area efficacy. The proposed SAR ADC contains a 13-bit hybrid binary/R-2R DAC (1-bit redundancy), in which the memristor-based trimming is introduced. The complete circuitry is designed and simulated in a standard 180 nm Bipolar-CMOS-DMOS (BCD) process. The memristor model used for circuit simulations was developed and validated from a physically fabricated memristor in [20]. Through this memristor-assisted background calibration scheme, the errors caused by element mismatches in the DAC are mitigated and the linearity of the SAR ADC has been effectively improved.

The paper is organized as follows: Section II introduces the proposed memristor-assisted sign-based background calibration scheme in a 12-bit SAR ADC and the model of the memristor. Section III presents the architecture of the complete ADC and the implementation of each block. Section IV shows the simulation results. Section V discusses the feasibility and limitation of applying this technique in future chip design, and Section VI concludes the paper.

II. Memristor-Assisted Sign-Based Background Calibration for the SAR ADC

A. The Concept of the Proposed Methodology

As a result of the nature of the SAR ADC, intrinsic element mismatches in the DAC are often the dominating factor that affects ADC performance such as integral non-linearity (INL), differential non-linearity (DNL), Spurious-Free Dynamic Range (SFDR), and Signal-to-Noise-and-Distortion Ratio (SNDR). To address the mismatch issue, different techniques have been proposed to calibrate the ADC. Fig. 2 (a) shows an example of the sign-based calibration scheme proposed in [11]. Unlike post-processing the output of the ADC in [15], this sign-based calibration can run in parallel with the normal ADC conversion and calibrate the output immediately when there is an error detected. This calibration scheme is implemented with a sign-error detection circuit, calibration registers, and a trimming circuit (i.e., correction

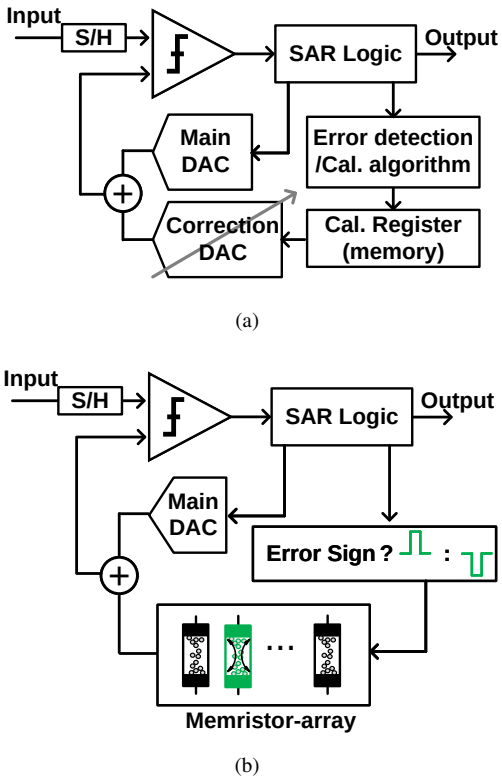


Fig. 2: (a) The sign-based calibration scheme proposed in [11]. (b) The concept of the proposed memristor-assisted calibration scheme.

DAC). Once the calibration is activated, with the assistance of the redundancy cycle, one sign error (i.e., "+" or "-" or "0") is generated by the detection circuit and stored in calibration registers. This sign error is then exploited to indicate the direction of the calibration and activate the correction DAC to trim the main DAC. The output of the main DAC can be trimmed to the desired reference level after some specific capacitors inside the correction DAC are activated or deactivated. The advantage of this sign-based calibration scheme is that it runs in the background, so normal ADC conversions are not interrupted during the calibration process. Compared to the digital calibration techniques such as detecting the full-bit output of the ADC in the digital domain [15], this sign-based calibration technique operates in the analog domain and achieved 5.5 fJ per conversion step in Walden figure-of-merit. This work is still competitive when compared to the recent state-of-the-art SAR ADC being designed in the same technology node with different calibration schemes such as [21]. As shown in Fig. 2, the aim of this work is to optimise further the sign-based SAR ADC calibration scheme by combining the calibration registers and the correction elements into one single block. This is enabled by using memristors which can be used as resisitve memory cells and resistive trimming elements at the same time thanks to its non-volatile resistive switching property. In a calibration process, the sign error works as a feedback signal which can determine the polarity of programming voltage pulses. The calibration can be easily conducted by applying positive or negative voltage pulses on the memristor according to the sign error. The memristance can thus be increased or

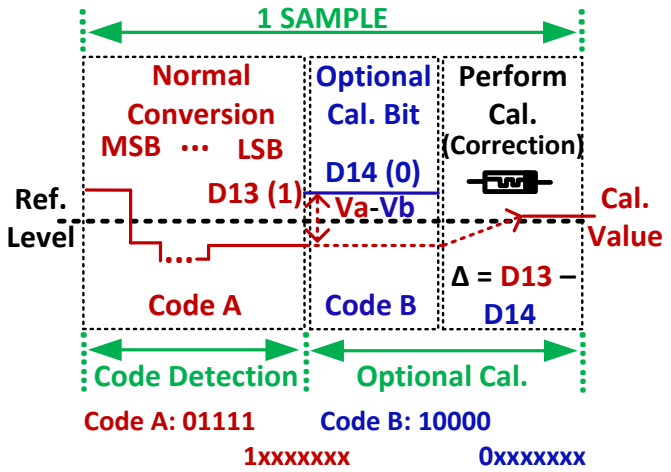


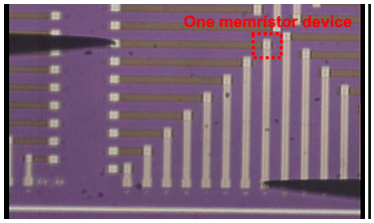
Fig. 3: An example of the logic flow of the memristor-assisted sign-based calibration scheme. 13-bit non-binary Code A and Code B stand for the same 12-bit code: "100000xxxxxxx". Thus, ideally, the equivalent analog value of Code A and B equal to each other.

decreased to make the DAC output reach the desired reference level. Compared to [11], non-volatility allows the memristor to store the calibration information and act as a trimming element at the same time, which can eliminate the excessive calibration registers (memories) and the correction DAC. In such a way, memristor-assisted calibration enhances the overall efficiency and further reduces the calibration latency and area occupation.

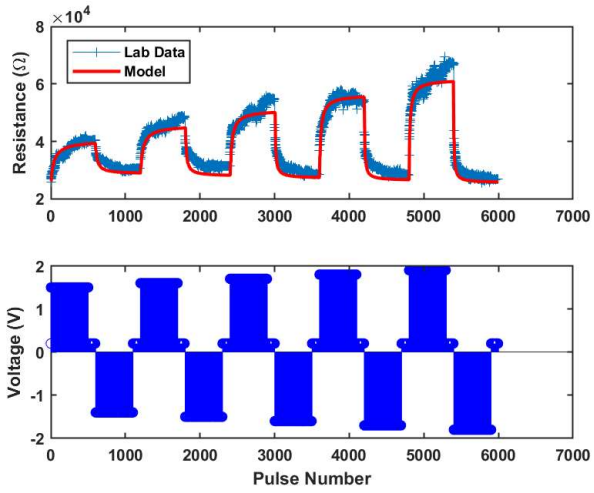
Fig. 3 shows an example of the logic flow of the proposed calibration scheme. The ADC first converts the input voltage in a 13-cycle normal conversion process, which includes 12 regular cycles and 1 redundant cycle. Thanks to redundancy, the same 12-bit code can be represented by two 13-bit non-binary codes (i.e., Code A and B in the figure). The DAC output of these two codes should be the same in ideal conditions. However, in reality, different DAC components (i.e., resistors in an RDAC, capacitors in an CDAC) suffer from different mismatches, and the equivalent analog values of the two codes are not the same because of the intrinsic mismatch have different effects on the two codes. The calibration is activated if Code A or B is detected after the 13^{th} conversion cycle. In the additional calibration (14^{th}) cycle, one more conversion is performed. As shown in the example in Fig. 3, because of the difference between two DAC outputs, the conversion result D14 is "0", which is different from the 13^{th} conversion result "1". This difference indicates a sign error (Δ). Based on this sign, in the following conversions, the memristance is adjusted to make the DAC output reach the desired reference level (i.e., correction), and the calibration is then finished. The calibrated DAC, which can provide more accurate D/A conversions, can benefit the subsequent A/D conversions and improve the output linearity of the ADC. More details of the working principle are described in Section III-A.

B. The Memristor and its Model

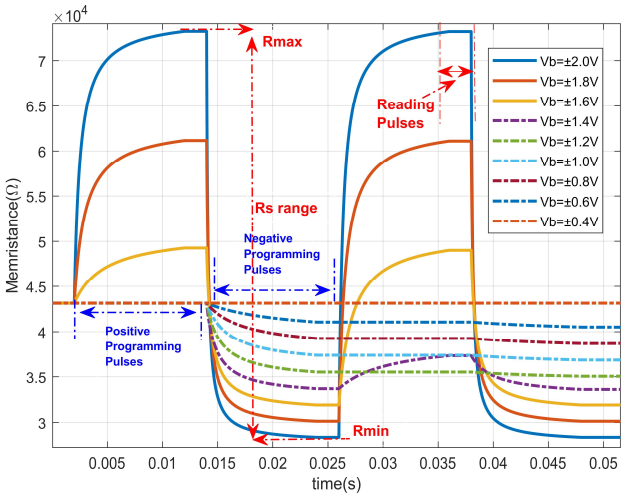
Fig. 4 (a) shows the micrograph of our in-house fabricated memristor. We performed a characterization process on a Pt/Al_2O_3/TiO_2/Pt multi-state memristor using a customized



(a)



(b)



(c)

Fig. 4: (a) Micrograph during the measurement of the selected memristive device. Every cross point is the active region of a single device. (b) The response of the in-house fabricated $Pt/Al_2O_3/TiO_2/Pt$ memristor (top) under the applied stimulus (bottom) and the result of the model fitting to the measurement data [22]. (c) A more detailed example of the simulation result based on the Verilog-A model proposed in [22]. The response is the result of applying positive programming pulses, negative programming pulses, and reading pulses, modulating the memristance from Rmin to Rmax.

probe station. A device response under stimulation of increasing amplitude pulse sequences is shown in Fig. 4 (b). A set of 500 programming pulses with different amplitude V_b from 1.5 V to 2 V were applied to the memristor. 100 reading pulses were applied between the two adjacent stimulus pulse trains. The memristance exhibits a gradual increase or decrease in

response to the applied voltage of different amplitude and polarity, indicating that device behaviour can be controlled for calibration by incrementally or decrementally programming to different resistance states.

The memristor model used in simulations has been introduced and verified in [20, 22]. The static characteristics of the model consist of a bi-directional hyperbolic sine, whilst the rate-of-change of memristance exhibits an exponential dependence on the applied voltage. In particular, the switching rate surface is generated to reveal the reaction of the memristor to current resistance and applied voltage. The static current-voltage (IV) characteristic is decided by the device's internal state variable, Resistive State (RS), and a hyperbolic sine function of the voltage applied on the device's terminal. The time derivative of the state variable $\frac{dR}{dt}$ is decided by the sign and amplitude of V_b and RS vaule (i.e., $R<r_p(v)$,$R\geq r_n(v)$ or $R>r_p(v)$,$R\leq r_n(v)$). In Eq. 1, $s(v)$ serves as the switching sensitivity function, controlling the intensity of RS change. $(r(V_b) - R)^2$ corresponds to the window function which features a simple quadratic fitting and is regulated by the maximum/minimum RS $r(v)$ described in a linear form. $s(v)$ and $r(v)$ are defined in [20].

$$\frac{dR}{dt}|_{V_b} = \begin{cases} s_p(V_b)(r_p(V_b) - R)^2 stp(r_p(V_b) - R) \\ s_n(V_b)(R - r_n(V_b))^2 stp(R - r_n(V_b)) \end{cases} \quad (1)$$

As shown in Fig. 4 (b) and (c), the model is fitted to the measurement data of the $Pt/Al_2O_3/TiO_2/Pt$ memristor and simulated with varied amplitude stimulation from $\pm 0.4\ V$ to $\pm 2.0\ V$. Every programming cycle contains 500 pulses and the pulse width is 10 μs. The simulated transient response demonstrates the same switching behaviour to the measurement results in Fig. 4 (b). Initialized from 43 kΩ $\pm$ 1 kΩ, the memristor can be written up to 74 kΩ $\pm$ 1 kΩ when applying positive voltage pulses, whereas negative voltage pulses can write the memristor down to 28 kΩ $\pm$ 1 kΩ. When the applied pulses have a maximum absolute voltage below $0.5\ V$, the device is prevented from switching and remains static. Thus, $0.5\ V$ is set as the threshold voltage in the design. It is worth mentioning that stimulus under $|1.4$ V$|$ only changes the memristance by a small value, which raises a trade-off between power consumption, speed of calibration, and the covered range of calibration. Low voltage stimulus can be applied to the memristor when a fine calibration is needed, the trade-off can be balanced not only rely on the memristor but also on the technology node and the variations brought by the fabrication. In this design, a 2 V pulse train is used to trim the memristor so that the effect of calibration is maximized, this will be presented with more details in Section IV. The Verilog-A model can be easily adopted within standard CMOS design flow in Cadence. The physically extracted parameters used for the simulations can be found in [20].

III. Implementation of the 12-bit SAR ADC with the Memristor-Assisted Background Sign-Based Calibration Scheme

A. SAR ADC Top-Level Architecture

Fig. 5 shows the proposed architecture of the ADC, which is a detailed block-level design developed from the scheme

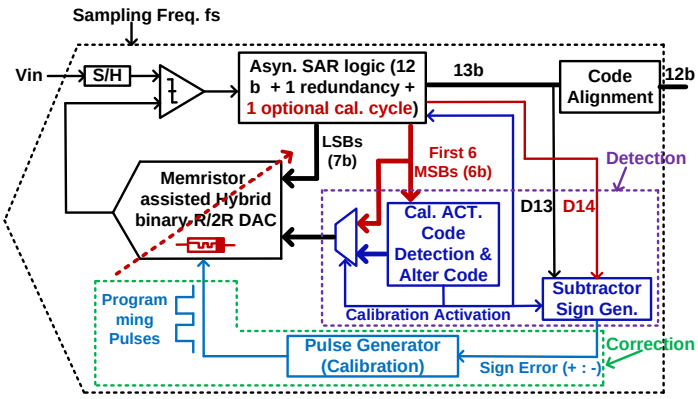


Fig. 5: Architecture of the 12-bit asynchronous SAR ADC, which contains a memristor-assisted calibration system for calibrating the DAC mismatches.

presented in Fig. 2 (b). The input voltage is sampled and held on a conventional S/H block. The SAR logic includes 12 regular conversion cycles, 1 redundancy cycle, and 1 calibration cycle. The SAR logic is based on an asynchronous architecture, which is similar to the one proposed in [23]. This asynchronous logic is exploited to ensure that the calibration cycle can be successfully activated when one of the calibration activation codes is detected. This is because, the internal clock signals are generated by an internally triggered asynchronous logic, so each conversion cycle can only be triggered by the preceding cycle. Thus, the 14^{th} calibration cycle can only be activated after the 13^{th} conversion cycle is finished and the "Calibration Activation" signal is activated. The "Cal. ACT. Code Detection & Alter Code" and "Subtractor Sign Gen" circuits detect the "calibration activation codes" in Fig. 6 and generate a feedback sign (i.e., detection). The "Pulse Generator" generates programming pulses based on the feedback sign to trim the memristor inside the DAC (i.e., correction).

In a complete conversion of one sample, the first 6 most significant bits (MSBs) are sent to a 6-bit multiplexer (MUX), which consists of six 2-to-1 MUXs and a calibration activation code detection circuit. When the 6 MSBs do not match any "calibration activation codes" in Fig. 6, the 6 MSBs will not activate the detection circuits shown in Fig. 6, thus the "Calibration Activation" signal keeps low, and the "Alter Code" circuit shown in Fig. 5 will not be activated. The MUX then sends the original 6 MSBs to the DAC. In the DAC, the MSBs and the least significant bits (LSBs) are recombined together into a 13-bit code. When the 6 MSBs match any "calibration activation codes" in Fig. 6, the 6 MSBs activate the detection circuits, and the detection circuits then turn the "Calibration Activation" signal on, which activates the additional calibration cycle and the "Alter Code" circuit. Before the additional cycle, the altered 6 MSBs are sent to the DAC by the MUX, so the recombined 13-bit code is updated to its relative form (i.e., Code A to B or Code B to A). In the additional cycle, the comparator performs one extra comparison and determines the 14^{th} compared result (D14). If the comparison result in the 13^{th} cycle (D13) equals D14, the pulse generator will not be turned on and the memristor will not be trimmed. If D13 is not equal to D14, a subtractor

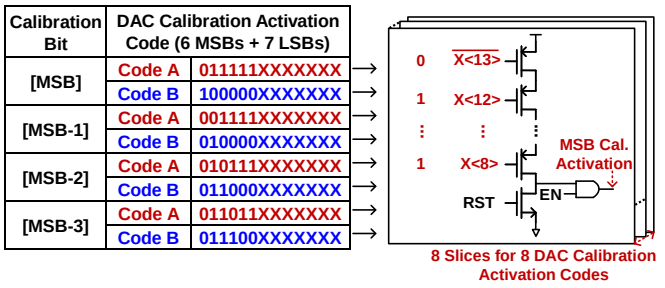


Fig. 6: Calibration activation codes for the DAC calibration and the implementation of the calibration activation code detection circuits. Similar to the code detection circuits used in [11], a set of dynamic CMOS detection circuits are designed to detect the code for calibration. "MSB - 1" represents the bit after the MSB, "MSB - 2" represents two bits after the MSB, etc. (e.g., if MSB is B_{12}, "MSB - 1" indicates B_{11}.)

logic will determine the sign of D13 minus D14 and generate a feedback signal. Next, the corresponding voltage pulses are generated to adjust the resistance of the memristor in the hybrid DAC. When the conversion is finished, the code alignment block converts the 13-bit non-binary code to a 12-bit binary code. This code alignment block is customized for the applied redundancy technique whose theory is first proposed in [24]. A detailed timing diagram that illustrates the above process is presented later in Section IV.

B. Implementation of the Detection & Code Alteration Circuit

Fig. 6 shows the calibration code detection logic. To avoid static power consumption, 8 specific codes can trigger the detection circuitry and turns on the "Calibration Activation" signal. Therefore, 8 slices of the detection circuit are implemented. Each detection circuit consists of 6 detecting transistors and 1 reset transistor. The 6 detecting transistors in each slice are customized to correspond to one of the 6-bit MSBs shown in Fig. 6. To avoid unnecessary power dissipation and ensure there is enough time to activate the optional calibration cycle, the enable signal turns high at the 11^{th} cycle in each conversion process. At the 11^{th} cycle, if the 6 MSBs fit in one of the 8 scenarios, the corresponding calibration signal is charged to logic high and the additional calibration cycle is activated. Using code "011111" as an example, the 6 MSBs "011111" are sent to the detection circuitry and compared to the 8 scenarios at the 11^{th} cycle. As 6 detecting transistors are all turned on, the "MSB Cal. Activation" signal is then charged to logic high, and the additional 14^{th} cycle is activated. In this work, to minimize the unexpected non-ideal factors and further investigate the performance of a single on-chip memristor, only the MSB calibration is validated and 2 slices in code detection are used. In the future, we plan to trim more MSBs, which may further improve the calibration performance, and thus the other 6 slices are also designed and implemented.

Fig. 7 shows the implementation of the code alteration circuit. The 6 MSBs are sent to a set of half adders and half subtractors at the same time, as shown in the top and bottom of Fig. 7. The last digit of the 6-bit MSBs determines whether the selection MUXs in the middle of Fig. 7 select the codes from either the half adders or the half subtractors. This algorithm

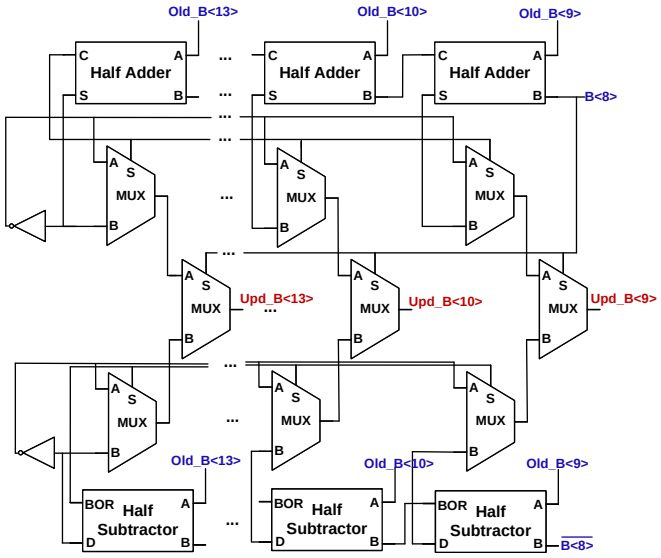


Fig. 7: The code alteration circuitry. Code A and Code B can be mutually altered by simply performing addition or subtraction in the digital domain.

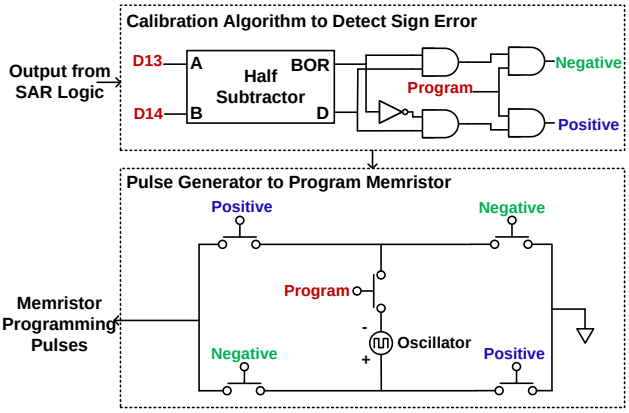


Fig. 8: The implementation of the sign generator and the pulse generator.

ensures that Code B can be generated if the input is Code A and vice versa. Still taking "011111" as an example. The last digit of this code is "1", and therefore it is categorized as Code A. When this code is sent to the code alteration circuitry, "011111" turns to "100000" by the half adders and "011110" by the half subtractors. Because the last digit of the input code is "1", the selection MUXs select "100000" as the output and thereby perform the code alteration. The same trick is applied to all 8 scenarios to ensure Code A and Code B can be altered between each other. The equivalent analog value of the altered code is compared with the reference level in the calibration cycle and generates the 14^{th} digit (D14). The D14 is then sent to the sign generator.

C. Implementation of Sign Generator and Pulse Generator

Fig. 8 shows the sign generator and the pulse generator. The sign generator is designed with a half subtractor and five logic gates. When the calibration is activated, D14 is generated and sent to the half subtractor. The subtractor subtracts D14 from D13. When D14 and D13 have different values, the logic gates

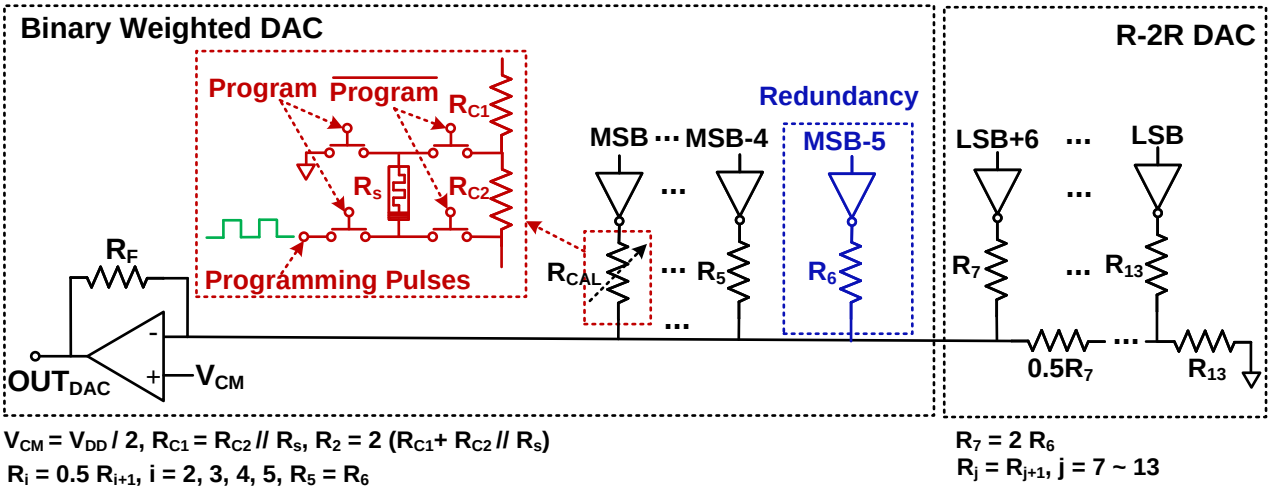


Fig. 9: The 13-bit hybrid binary/R-2R DAC of the proposed 12-bit SAR ADC. The first 6 bits (MSB $\sim$ MSB-5) of this R-DAC are in a binary weighted DAC architecture, while the rest of the 7 LSBs are designed to an R-2R ladder. The MSB-5 is the redundancy bit. In this design, only the MSB calibration is used to validate the calibration. The largest resistor (R_{13}) has a value of 336 kΩ and is in a size of 167.8375 $(\mu m)^2$. The switches are designed with standard MOS transistors in 180 nm process, and the on-resistance of each switch (R_{on}) is around 442 Ω.

determine whether a positive or a negative signal is sent to the pulse generator. In the sign generator, the "Program" signal is the "Calibration Activation" signal with certain delay, and the pulse generator is turned on only when the "Program" signal is high. When D13 and D14 have equal values, the pulse generator is not turned on and no pulses will be generated. Table I shows the truth table of the sign generator and pulse generator circuits. "x" indicates no pulse is generated, "-" indicates negative pulses, and "+" indicates positive pulses. Note that when "Positive" is high, it means that the value of the MSB is lower than it should be, and therefore negative pulses are generated to trim the memristance to a lower value, which will increase the value of the MSB.

TABLE I: Logic of the sign generator and pulse generator

D13	D14	Program	Positive	Negative	Pulses
0	0	0	0	0	x
1	0	0	0	0	x
0	1	0	0	0	x
1	1	0	0	0	x
0	0	1	0	0	x
1	0	1	1	0	-
0	1	1	0	1	+
1	1	1	0	0	x

The pulse generator is designed based on an H bridge. When "Program" and "Positive" signals are received, positive pulses are generated and sent to the DAC to trim the memristor. The same process is performed for negative signals. To meet our design needs, the amplitude, pulse number, and pulse width are set to fixed values. By doing this, we can set firm step sizes for the calibration (e.g., the DAC output can be adjusted by 0.2 LSB in each calibration). Then, if we increase the amplitude of the pulse without changing the number and inter-pulse time, the DAC output can be adjusted by a higher step size of 0.4 LSB and vice versa. The pulses are generated by an oscillator.

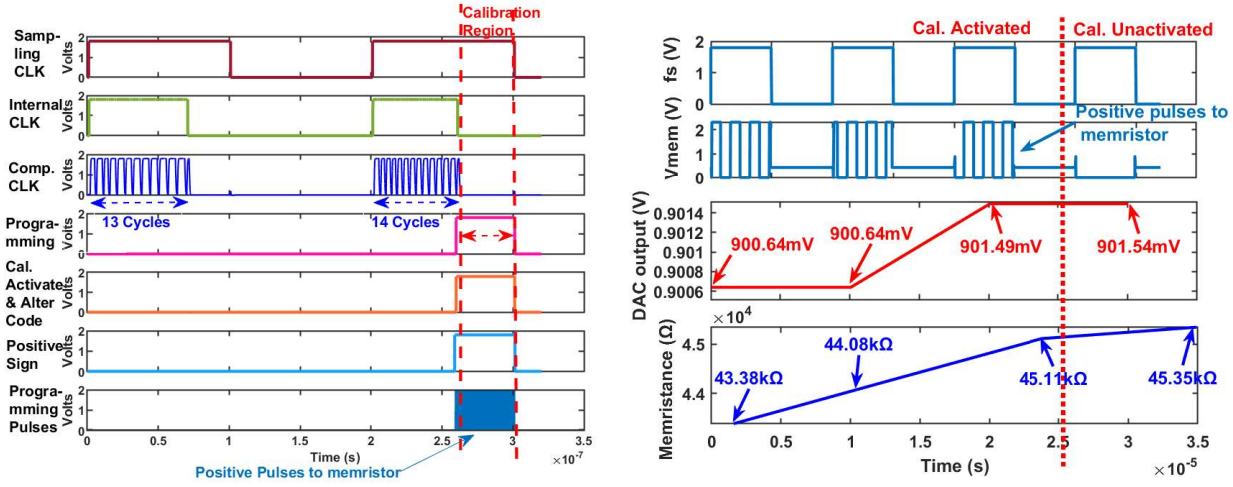
D. Hybrid Binary/R-2R DAC

In order to exploit the memristor as a trimming element in the DAC, a resistive DAC (R-DAC) is a straightforward design choice. Due to the use of the redundancy technique, a binary-weighted architecture needs to be applied to achieve the redundancy bit. However, assigning the resistors with binary weighted values leads to high power consumption and large area occupation. For example, in this design, the 12-bit SAR ADC requires a 13-bit DAC which includes 1-bit redundancy, and the DAC output needs to meet a non-binary relationship shown in Eq.2.

$$\begin{aligned} D_{out} = {} & 2048 \cdot B_{12} + 1024 \cdot B_{11} + 512 \cdot B_{10} + 256 \cdot B_9 \\ & +128 \cdot B_8 + 128 \cdot B_7(Redun.) + 64 \cdot B_6 + 32 \cdot B_5 + \\ & 16 \cdot B_4 + 8 \cdot B_3 + 4 \cdot B_2 + 2 \cdot B_1 + 1 \cdot B_0 \end{aligned} \quad (2)$$

B_7 is the redundant bit, and the resistor value for this bit is the same as the one assigned to B_8. If this R-DAC is fully in a binary weighted DAC architecture when the MSB resistor is 10.5 kΩ, the LSB resistor has to be 21.5 MΩ, and the total resistance is 43.165 MΩ. To reduce the overhead in power and area, we designed a hybrid binary/R-2R DAC for the proposed ADC.

As shown in Fig. 9, the 7-bit LSBs are designed in an R-2R ladder architecture and the unit resistance is set to 336 kΩ. Because R_7=2R_6, the Thévenin-equivalent resistance of the R-2R ladder can restore a binary weighted relationship along with the MSB resistors to make this hybrid design fully functional. The MSBs are designed in a binary-weighted DAC architecture. The MSB resistor R_{CAL} consists of a memristor labelled as R_S, and two resistors R_{C1} and R_{C2}. The R_{CAL} is formed by connecting the resistors R_{C1} and R_{C2}//R_S in series. The equivalent resistance of R_S is 10.5 kΩ, where R_{C1} and R_{C2}//R_S equal to 5.25 kΩ. The memristor has an initial value of 43 kΩ. By taking the on-resistance of the two switches into account (R_{on}≈442 Ω each), R_{C2} is calculated and equals to 5.96 kΩ.



(a) (b)

Fig. 10: (a) Timing diagram which illustrates the memristor-assisted background calibration logic. (b) One example in simulation shows the operation of the calibration. The calibration was performed at the end of the first two conversions. Four memristance values were read at the end of each conversion process.

The rest of the MSB resistors except R_6 are assigned with binary weighted resistance. For example, R_2 has a resistance of 21 kΩ, which is two times of the equivalent R_{CAL}. R_6 is designed to be the same as R_5 to work as a redundant bit. When combining the R-2R DAC with the binary-weighted DAC, R_7 has to be two times of R_6 to extend the binary relationship. An OTA is designed to establish a virtual ground to the binary-weighted DAC and the R-2R DAC, this ensures that resistors in the two DACs work separately and not causing any interaction. The relationships of the resistors are represented in the following equations.

$$R_2 = 2 \times (R_{C1} + R_{C2}//R_s) = 21\ k\Omega \tag{3}$$

$$R_i = 0.5R_{i+1},\ \ for\ i = 2, 3, 4, 5 \tag{4}$$

$$R_5 = R_6 = 168\ k\Omega \tag{5}$$

$$R_j = R_{j+1} = 2 \times R_6 = 336\ k\Omega,\ \ for\ j = 7 - 13 \tag{6}$$

The total resistance of our proposed hybrid DAC is 4.1895 MΩ, which saves more than 90% of area and power compared to a standard binary-weighted architecture.

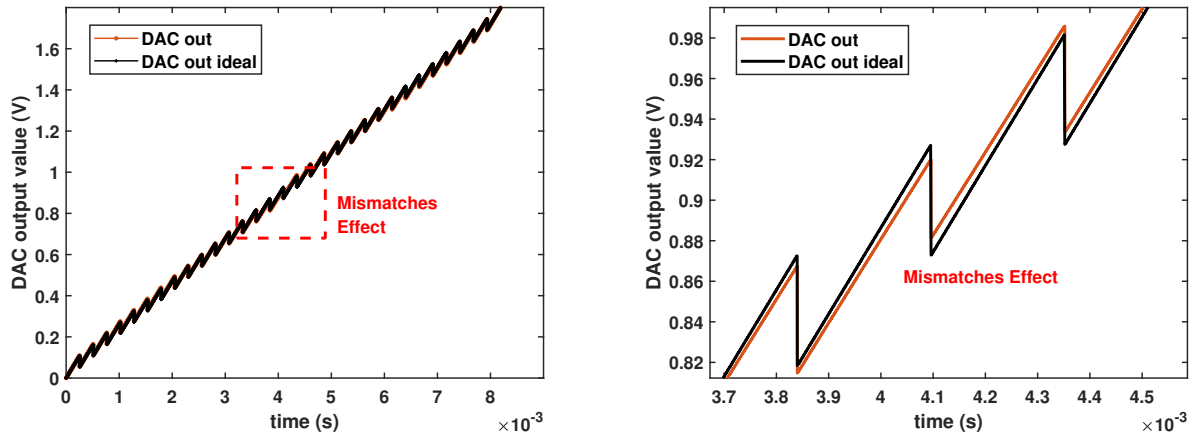
IV. Simulation Results of the SAR ADC

A. Calibration Logic

Fig. 10 shows an example of the simulated memristor-assisted background calibration timing diagram with the gradual change of the memristance and the DAC output. Fig. 10 (a) demonstrates two scenarios. In the first conversion process, there is no error detected by the detection circuitry, so 13 normal conversion cycles are performed. The asynchronous SAR logic outputs the result when the last comparison is finished. In the second conversion process, a "calibration activation code" is detected and the calibration cycle is activated. 14 cycles (13 normal conversion cycles + 1 calibration cycle) are performed. After the 14^{th} cycle, a positive sign is determined based on the sign error (Δ). The pulse generator then generates pulses with the corresponding polarity to program the memristor in the rest of the conversion period. Fig. 10 (b) shows one example of how the gradual change of memristance trims the DAC output. V_{mem} is the voltage across the memristor, and DAC output is the output value of the hybrid binary/R-2R DAC after each A/D conversion. The sampling frequency is 100 kS/s and the input of the ADC is set to a fixed DC voltage of 901.7 mV (code: 100000xxxxxxx or 011111xxxxxxx) to ensure the MSB calibration is activated in all four conversions. The exact pulse width and amplitude are 800 ns and 2.2 V respectively (2.2 V pulses can present the result more obviously than 2V pulses). As shown in the result, in the first three conversions, the DAC output is lower than the input value, and the "calibration activation code" is detected in both conversions. Based on the sign, positive programming pulses are generated to adjust the memristance by a specific resistance value. Then, in the next conversion, the DAC output reaches 901.54 mV, which is closer to the desired level (less than 1 LSB), and this indicates that the calibration performed in the previous three conversions effectively calibrate the DAC. The calibrated DAC assists the ADC to achieve more accurate results in the subsequent conversions, and thus improves the ADC output linearity.

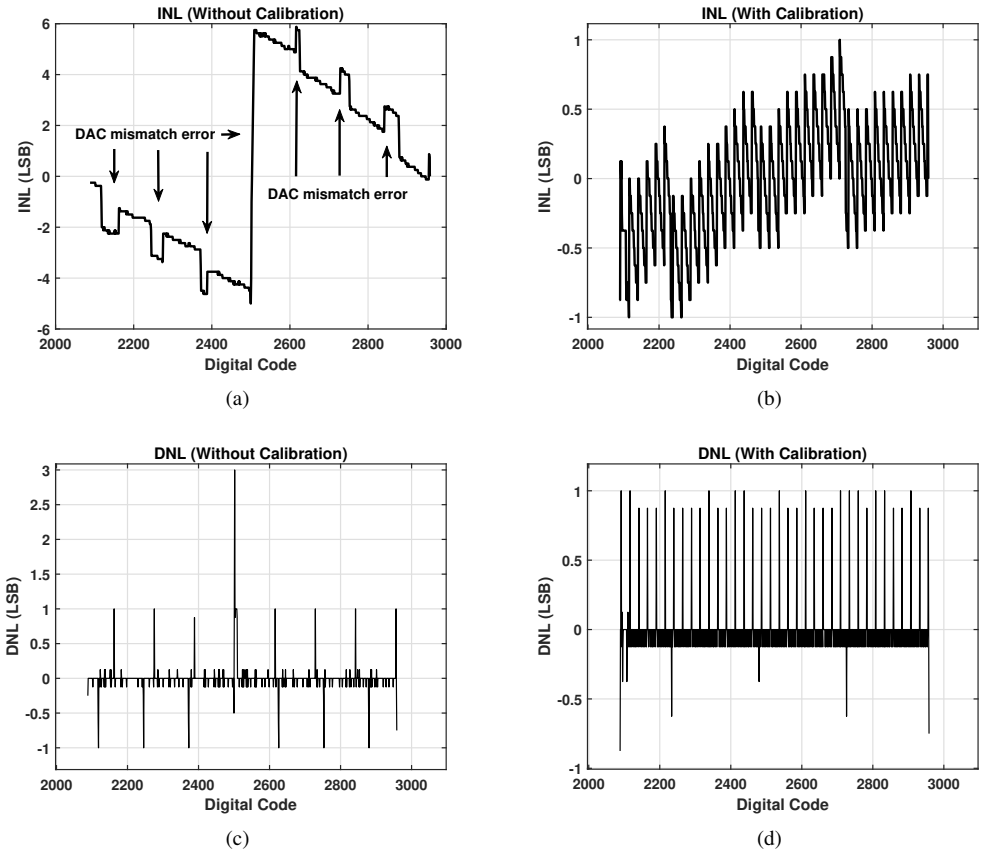
B. Functionality of the DAC

To ensure our proposed DAC works as expected, we examined its functionality separately by performing a full-scale sweep with device models for Monte Carlo simulation (i.e., from "0000000000000" to "1111111111111"). As shown in Fig. 11 (a), 8192 binary codes were input to two 13-bit non-binary DACs. One is our proposed hybrid resistive DAC, and the other one is an ideal DAC written in Verilog-A based on the functionality of our proposed DAC, which has no mismatch. Outputs of two DACs show continuous triangle-shaped steps, and these steps are expected because binary codes were used to test non-binary DACs. When the input approaches an equivalent analog value of 0.9 V, caused by the mismatches, the output of the proposed DAC starts to



(a) (b)

Fig. 11: (a) A Monte Carlo simulation result when 8192 binary codes (from "0000000000000" to "1111111111111") were input to our proposed 13-bit non-binary DAC. An ideal DAC output for comparison is labeled in red. The ideal output is generated by an Verilog-A code with the same functionality. (b) A zoom-in graph of the mismatch effects in (a). Only the mismatch effect was included in the Monte Carlo simulation. Simulation results include all parasitic effects from the layout.



(a) (b) (c) (d)

Fig. 12: (a) Simulated INL without the calibration. (b) Simulated INL with the calibration. (c) Simulated DNL without the calibration. (d) Simulated DNL with the calibration. The sampling rate is 100 kS/s. Transient noise was not added to ensure the non-linearities were only caused by the DAC mismatches. The amplitude and pulse width of programming pulses were set to 2 V and 500 ns respectively in the simulation. Simulation results include all parasitic effects from the layout.

deviate from the ideal output steps. Fig. 11 (b) shows a zoom-in graph of Fig. 11 (a), it is obvious that the intrinsic element mismatches of the DAC lead to the output non-linearity, which deteriorates the ADC performance. Despite the errors caused by the mismatches, our proposed DAC performs the correct D/A conversion, and the non-linearity caused by mismatches

can be calibrated by our proposed calibration scheme. Based on the proposed DAC architecture, when the memristance varies from 28 kΩ ± 1 kΩ to 74 kΩ ± 1 kΩ, the DAC output can be adjusted by a range from - 7.33 LSB to + 10.08 LSB. (N.B., the LSB here is the LSB for the 13-bit non-binary DAC, which is calculated by $\frac{Vref}{Din}$.)

C. Improvements in Linearity

To demonstrate the efficacy of the proposed calibration scheme, simulations were run to measure the INL and DNL before and after the calibration. The transient noise was disabled during the simulation and only the mismatch effect was included in the Monte Carlo simulation. This ensures the non-linearity of the ADC output can only be caused by intrinsic element mismatches. Please note that the statistical model of memristors is not yet available and therefore the Monte Carlo simulation presents the statistical variation of all the CMOS components in the circuits but not the memristors. However, the absolute precision of the memristors is not required in the proposed calibration scheme since their resistance values are adaptively programmed to null the error of DAC in a closed loop. As shown in Fig. 12, all simulations were run at 100 kS/s while a ramp signal with a step size of 0.125 LSB is applied at the input, which corresponds to 8 conversions at each step. We set the input range from 0.9 to 1.3 V because this is the range where the MSB calibration is activated. In this range, the 13-bit non-binary code "100000xxxxxxx" or "011111xxxxxxx" was detected and the effect of mismatches occurs alternatively because different resistors were activated for two different codes. A number of 7280 input codes, which indicate 910 (7280/8) 12-bit binary codes, were tested to verify the proposed scheme. The first 40 binary codes were omitted in the plots because the calibration was conducted during the first 320 conversions (40 binary codes x 8 =320). From Fig. 12 (a) and (b), it is apparent that the INL is effectively suppressed when the error caused by DAC mismatches is calibrated. Furthermore, as shown in Fig. 12 (c) and (d), the DNL hit within ±1 LSB with the aid of calibration. This indicates there are fewer missing codes after the calibration is performed. These results prove that the matching in DAC can be effectively improved with our proposed memristor-assisted calibration scheme.

D. Power Consumption

Fig. 13 shows the power consumption breakdown of the ADC at a sampling rate of 100 kS/s. The total power consumption is 183.93 μW, of which 89.54% is attributed to the conventional blocks in the SAR ADC (i.e., R-DAC, SAR logic, comparator, S/H, and clock). The code alignment circuit consumes 1.08% of the total power. The calibration circuitry (Cal. Logic + Programming memristance) account for only 9.23% of the total power. Overall, the digital blocks consume 12.27% of the total power consumption, which can be further reduced in a more advanced technology node than 180 nm process.

A total of 32768 (4096 x 8) codes were swept. During the simulation, the "calibration activation codes", which can be

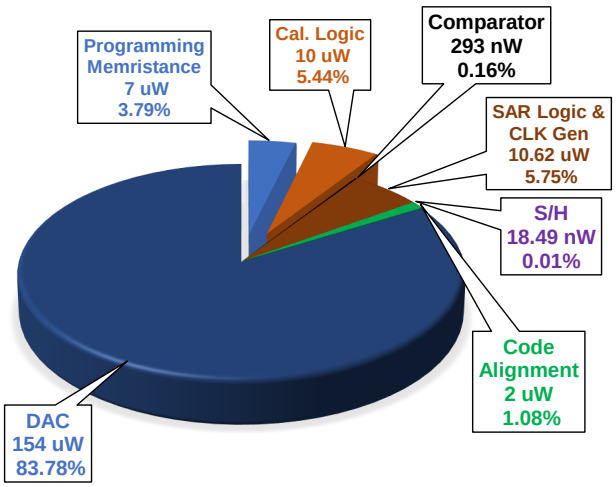


Fig. 13: Power consumption of each block in the ADC at 100 kS/s sampling rate. The total power consumption of the ADC is 183.93 μW. The values of power are based on simulation results. The simulation setting is the same as the one in Fig. 12. The simulation is performed in a standard 180 nm process.

either "100000xxxxxxx" or "011111xxxxxxx", were detected. Therefore, 2048 (1024 x 2) calibrations were activated, which means the calibrations were turned on in 6.25% (2048/32768) of the total simulation time. Because the calibration was not always on during the complete sweep, the power consumption of the calibration (Cal. Logic + Programming memristance) in 1 conversion is averaged over the full range and kept at a low value. It is worth noting that the memristor model in simulation cannot fully characterize the non-linear power consumption over time, and therefore we estimated the energy consumed during each voltage pulse when trimming the memristor based on the measurement data from the real memristors (the switching behaviour and I-V characteristics of the chosen memristor were measured in our lab and reported in [25]). For this design, we set the amplitude of the programming pulses to 2 V, due to the change of memristance being within a certain range, the instant worst-case current through the memristor is accounted for and equals to 74 μA, and thus the corresponding worst-case energy consumption within each trimming pulse is 148 pJ.

E. Layout

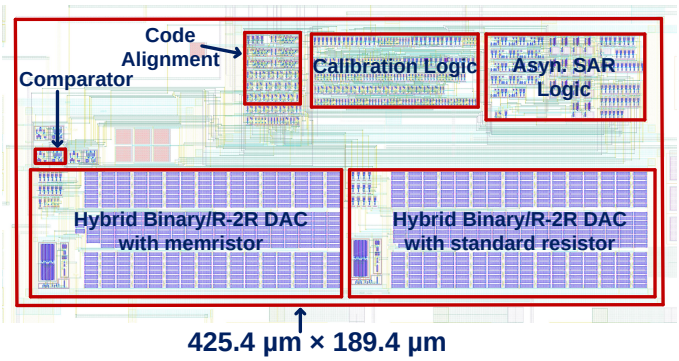


Fig. 14: Layout of the core chip.

Fig. 14 shows the layout of the core chip. The dimension of the core chip is 425.4 μm by 189.4 μm, and the total area occupation is 0.08 mm^2. The memristor will be laid on top of the MSB resistors in the DAC via Metal 5 and Metal 6. Therefore, the memristor itself does not occupy any area. It is worth mentioning that the DAC area is larger than it should have been. This is because we designed an off-chip option to connect the memristor since this is the first version of our test chip. Compared to the SAR ADC with sign-based calibration in [11], which adopted an area occupation of 0.0675 mm^2 in 40 nm technology node, our design has larger area occupation which is mostly due to the fact that the design is implemented in a much older 180 nm technology.

V. Discussion

We have demonstrated the feasibility of using the memristor to calibrate the intrinsic element mismatches in the DAC of the SAR ADC. The results shown in Section IV prove that the proposed scheme is a viable solution to improve the output linearity of a high-resolution SAR ADC. Since this is a feasibility study, we mainly focused on functionality verification and there are still limitations that need to be overcome before a memristor-assisted SAR ADC can be developed which outperforms the state of the art.

First of all, although the CMOS/Memristor integration technology is rapidly progressing, available memristor models today do not yet include process variation, mismatches, and stochastic switching behaviour. Accurately programming the memristance with voltage pulses is also critical because the memristors may experience device-to-device, cycle-to-cycle variations, and retention degeneration. The proposed scheme works based on a closed-loop mechanism which tackles to some extent the effects of these variations, but a more exhaustive study is only possible as more data becomes possible after these behaviours of memristors are characterized on a large scale (e.g. using the characterization platform developed in [26]). Another limitation of the memristor is that it needs a certain amount of time to be programmed; the proposed design can not be adopted to high-speed SAR ADCs at the moment (100 kS/s for this design). Yet, as mentioned in Section II-B, using a memristor in a coarse or fine trimming affects the speed and power consumption, the speed of the future SAR ADCs employing the memristor-assisted calibration can be increased and achieve better overall performance based on different applications.

In this study, we used the resistive DAC so that the element trimming using memristors is more straightforward. However, resistive DACs are typically not as energy-efficient as capacitive DACs (e.g., in this design, the proposed RDAC has a power consumption of 154 μW, which accounts for 83.78$\%$ of the total ADC power). Using memristors to calibrate capacitive DACs can be an interesting study topic in the next step, and a possible method is to use memristors to alter the DAC settling behaviour to effectively cancel the errors. Besides, as mentioned in Section III-B, we also plan to use a memristor array in the resistive DAC to trim more MSBs (i.e., MSB-1, MSB-2, etc.) instead of just the MSB. In such way, more errors caused by mismatch will be calibrated, and peripheral circuits can be reused to trim each memristor to reduce the circuit area and power consumption.

In the end, although the proposed SAR ADC still has limitations and is not yet competitive compared with the state-of-the-art ADCs, we believe the work is valuable to the memristor research community since this is the first work using memristor as a trimming element to calibrate a high-resolution SAR ADCs. With the results reported we would like to draw attentions of the ADC design community to an alternative calibration scheme enabled by the emerging memristor technology. We expect the performance will improve in the near future as the memristor technology is advancing rapidly.

VI. conclusion

This work presents a novel calibration scheme that exploits an in-house fabricated memristor to calibrate the intrinsic DAC mismatch of a 12-bit SAR ADC. To the best of the authors' knowledge, this is the first reported memristor-assisted calibration scheme for ADCs. The proposed scheme is designed based on the sign-based background calibration method along with the memristor that is used as both the calibration information register and the trimming element which is facilitated by using a hybrid binary/R-2R DAC architecture. The proposed scheme is validated in transistor-level simulations. While this is a feasibility study, we expect the proposed scheme will improve the SAR ADC performances further as memristor technology advances further.

Acknowledgments

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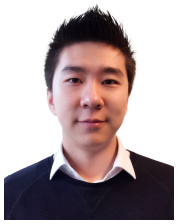

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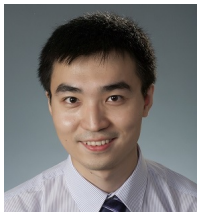

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