Dynamic Analysis, Stability and Design of Grid Forming Converters with PI-based Voltage Control in DC and 3-phase AC Microgrids

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***Abstract*—This paper analyzes the dynamic behavior of the voltage control loop based on proportional-integral regulators, commonly used for grid-forming converters in 3-phase AC and DC Microgrids and applications that involve a DC-link voltage control. The paper proposes a simple and accurate generalized analysis useful both for the system characterization and design. Two different control schemes, based on linear (Direct Voltage Control, DVC) and quadratic voltage feedback (Quadratic Voltage Control, QVC), are analytically studied, simulated and experimentally tested, demonstrating a superior performance of the QVC under the presence of constant power loads. The operation limits, the system stability and the disturbance rejection capability are analyzed considering the effect of control and plant parameters and the effect of the different types of disturbances and the operating point, taking into account the non-linearities of the system. The analysis is mainly focused on the effect of constant power loads given their negative impact on the system performance. The study provides a generic procedure for the analysis and design of proportional-integral voltage controllers, including the selection of the system capacitance for meeting specific dynamic specifications while considering system characteristics as the load level, the stability margins and the maximum voltage deviation under disturbances.**

***Index Terms*—Voltage control, Microgrids, Nonlinear systems, Power system dynamic stability, Constant Power Load**

I. Introduction

The increasing need for the integration of renewable energies and Distributed Generation (DG) in the grid have led to the concept of Microgrid (MG). Considering the high presence of electronic loads, DGs interfaced by Power Electronic Converters (PECs) and the significant penetration of renewable generation ruled under maximum power point tracking, grid control based on master-slave can simplify the MG design and operation [1]–[3]. In both cases, AC or DC, this approach requires a grid-forming converter controlling the voltage magnitude in DC MGs and voltage amplitude and frequency in AC MGs, usually using a feedback control based on Proportional-Integral (PI) regulators [4]–[6]. The high presence of tightly regulated Constant Power Loads (CPLs) contributes negatively to the low inertia and pose a challenge for grid-forming controller, affecting its dynamic control [7]. The dynamic and stability issues related to the non-linearity that CPLs introduce in voltage control schemes based on PI regulators, have been already addressed in the literature [2], [8]–[13] and is still a matter of concern [14]–[16]. Hardware (increasing capacitance or resistive loads) and control solutions (linear and boundary controllers or virtual impedance) have been proposed to reduce the effect of CPLs [17]–[20]. Nonetheless, the dynamics, stability limitations and selection of both the passive elements are still a challenging task and depends on the application.

The conventional implementation of PI-based grid-forming is based on the linear relationship between the voltage and the current at the capacitor [21]. Hereinafter this method will be referred as Direct Voltage Control (DVC). Despite its apparent simplicity, achieving good dynamic behavior is not straightforward, as already reported in the literature [22]. This is due to the non-linear behavior of the voltage reaction to both CPLs and Constant Impedance Loads (CILs) disturbances.

An alternative feedback control strategy has been proposed in the literature referred as fast-acting DC-link voltage controller or energy based controller, that here in after will be referred as quadratic voltage control (QVC) [22]–[25]. This controller uses the capacitor energy storage capability as an approach to linearize the relation between the voltage and the power at the capacitor plant using a quadratic voltage feedback. This controller has become widely used for the voltage control of the DC-links [26]–[28]. Nonetheless, its application can be generalized to any cascaded-based voltage control, such as grid-forming converters in both DC and 3-phase AC MGs. However, those techniques have not been further exploited for those applications and few examples are found on the analysis of the dynamic performance and tuning [22], [28]–[30]. In [29] the QVC approach is combined with a droop control in a DC MG. However, the performance under presence of CPLs is not evaluated and the tuning of the PI parameters is not deeply discussed. In [30] the QVC is applied in the interlinking converter of a hybrid MG operated as a DC grid-forming. Nonetheless, the study is not focus on the operation and benefits of this controller and, as in the previous study, its dynamic behavior and stability analysis under CPLs, as well as the discussion on the selection of the capacitance and the regulator parameters, are not provided. Although the QVC has been applied for DC regulation applications, to the authors knowledge, no records of this alternative are found for AC applications apart from [31]. Regarding the dynamic

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stiffness of grid-forming converters, in some cases the PI regulator might not be enough to ensure proper disturbance rejection and transient voltage quality, especially under CPLs. The literature has revealed that the effects of CPLs can be attenuated by increasing the system capacitance or the resistive loads and reducing the CPLs or the system inductance [7]. This can reduce the voltage oscillations and increase the stability margins. However, unlike the controller parameters, the modification of the system hardware is restricted. Alternatively, the dynamic performance can be enhanced through control methods as linear Proportional Derivative (PD) or boundary controllers [7], or by load decoupling, using measurements, observers or estimators [32], [33]. Methods adapted from the virtual inertia concept are also an appealing simple solution [34]–[36].

This paper analyzes the dynamic behavior of the voltage control loop used in grid-forming converters for 3-phase AC and DC applications, considering cascaded voltage-current control scheme. The aims of this paper are:

- Define small signal linearized and normalized equivalent models of DVC and QVC to fairly compare both approaches under different type of loads, focusing on CPLs. The superior performance of QVC under CPL is demonstrated.
- Define analytical solutions for determining the dependence of system damping, stability limits and disturbance rejection depending on the penetration of the different types of load.
- Evaluate the effect of capacitance, virtual capacitance, inner current control loop, damping and bandwidth in the disturbance rejection.
- Provide methods to define system damping depending on the load levels as well as procedures to select the capacitor value or the bandwidth depending on the maximum allowed transient voltage deviation and the maximum expected CPL step.

The proposed models and methods are evaluated both by simulations and experimentally.

This paper continues the study presented in [35]. The paper is organized as follows. Section II presents the system plant. Section III models the PI-based voltage controllers. Section IV analyzes the system behavior under disturbances and define the stability criteria. Section V discusses the effect of the capacitor. Section VI establishes the basics for a generalized analysis and design of the system based on its dynamic response. Section VII discusses the effect of the inner control loop. Section VIII presents the experimental results. Finally, section IX summarizes the conclusions.

II. Problem Definition and System Modeling

In most of the MG applications requiring a voltage regulation, the system plant to be controlled consists in a capacitor whose voltage derivative is proportional to its current. It is worth to point out that the following discussion assumes a DC system or an AC system modeled in the synchronous reference frame as done in [31]. An AC system in the *dq* reference frame can be considered as two independent DC

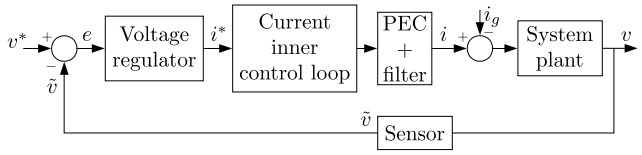

Fig. 1. Simplified diagram of the grid-forming control and system plant.

systems for each of the d and q axis. Thus, the modeling and analysis will consider a DC system, while the 3-phase AC model will consider the proposal in [31]. The control in this kind of applications is usually performed by a closed-loop cascaded controller consisting of an inner current/power control loop and an outer voltage control loop. Assuming the inner current/power control loop is fast enough, its dynamics can be neglected. In Fig. 1, the voltage control can be assumed as a voltage regulator, which input is the error, e, between the voltage reference, v^*, and the measured voltage, $\tilde{v}$, while the control action is the current, i, entering the system plant. Considering load disturbances, the system plant can be defined by (1), where C is the system plant total capacitance, $v(t)$ is the capacitor voltage, $i(t)$ is the control action of the voltage control loop, and $i_g(t)$ is the load disturbance.

$$\frac{dv(t)}{dt} = \frac{1}{C}(i(t) - i_g(t)) \tag{1}$$

Nevertheless, Constant Current Loads (CCLs) are not the only kind of loads found in power systems. More and more electrical appliances and industrial equipment behaves as CPLs, characterized by a tight control of load power, or as conventional CILs, presenting both of them a non-linear relation between power, voltage and current. Thus, the system in (1) must be reformulated as the non-linear system in (2), where i_L, P_L and g_L are the current, power and conductance disturbances associated to CCLs, CPLs, and CILs respectively.

$$\frac{dv(t)}{dt} = \frac{1}{C}\left(i(t) - \underbrace{\left(i_L(t) + \frac{P_L(t)}{v_{(t)}} + g_L(t)v(t)\right)}_{i_g(t)}\right) \tag{2}$$

Some assumptions are established regarding this expression: 1) Only pure resistive CIL are considered modeled as conductances, $g(t)$ in (2); 2) Generation is considered by negative signs in P_L and i_L; 3) The effect of line impedance is out of the scope of this paper and, thus, it is neglected in this analysis. Therefore, the system load seen by the grid-forming converter is considered as an aggregated current i_g.

Fig. 2 shows the single phase representation of the defined non-linear system. The behavior of the different loads existing in a MG are illustrated in Fig. 3 where I_n and V_n indicate the load nominal current and voltage and I_{max} and V_{max} are the load maximum point of operation. The non-linearities due to CPL and CIL will affect the voltage regulation design and performance. Moreover, unlike CILs, it is well known that CPLs are prone to compromise the system stability. In the literature, several attempts have been carried out for obtaining a linear approximation by defining a negative impedance [1],

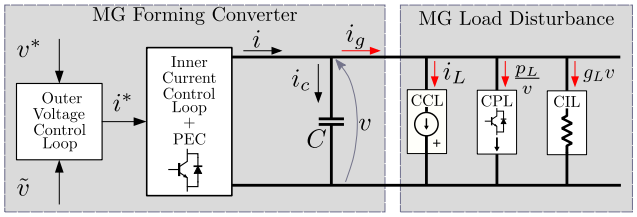

Fig. 2. Simplified diagram of the control, system plant and load disturbance for a generic DC or 3-phase AC grid-forming unit (considering dq reference frame complex form representation).

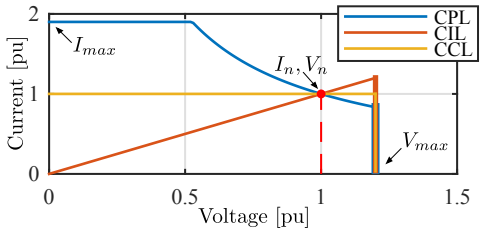

Fig. 3. Voltage-Current curves of the different types of loads in MGs.

[7], [10], [11]. In this paper, the effect of non-linear loads is approached by the linearization of the close loop system.

Before proceeding with the system analysis, it is worth to point out the assumptions and limitations of the analysis proposed in this paper: 1) as in any linearized model, the dynamic model accuracy is guaranteed only near the equilibrium point, 2) the scope of this study is only valid for low and negligible line impedance, 3) the feedback sensor effect is neglected, assuming its dynamic response is much faster and delay much lower than the voltage control loop time constant ($\tilde{v} = v$), 4) the inner current control loop (current controller, PEC topology, filter) is initially consider as ideal, assuming a bandwidth much higher than the one of voltage control ($i \approx i^*$). In order to establish the criteria to neglect the sensor effect and the inner current control loop, their effect is analyzed in Section III-D.

III. The Voltage Controller: PI-based Control Topologies and Modeling

The voltage controller models will be analyzed using linearized models. Two control schemes, shown in Fig. 4, are considered for the implementation of the outer voltage control loop in a grid-forming unit, the DVC and the QVC.

A. The Direct Voltage Controller (DVC)

The DVC control scheme is shown in Fig. 4a). A PI regulator in the standard form has been selected for the analysis, defined by (3), where i^* is the control action, v^* the voltage reference, v the actual voltage, and k_p and T_i are the PI proportional gain and integral time constant respectively. This controller is based on the linear relationship between the voltage and the current at the system plant capacitor.

$$i^*(t) = k_p(v^*(t) - v(t)) + k_p\frac{1}{T_i}\int (v^*(t) - v(t))dt \quad (3)$$

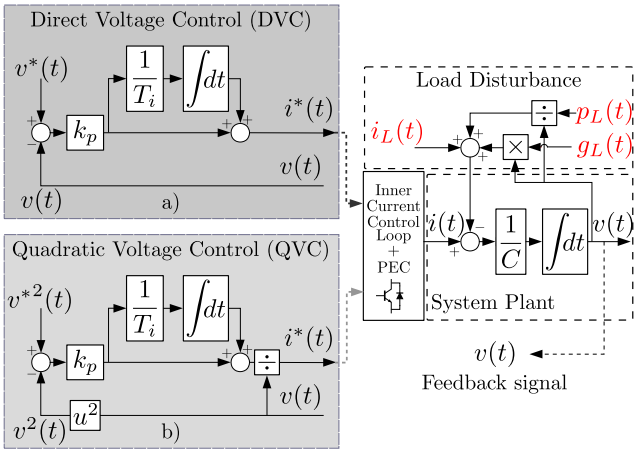

Fig. 4. PI-based alternatives for voltage control. a) DVC; b) QVC.

Considering an ideal inner control loop ($i = i^*$), the voltage closed-loop system when using DVC is defined by (4). This expression will be used as the starting point for the dynamic analysis of the DVC-based voltage control.

$$\frac{dv(t)}{dt}C = k_p\left(v^*(t) - v(t)\right) + k_p\frac{1}{T_i}\int\left(\left(v^*(t) - v(t)\right)dt\right) - i_L(t) - \frac{P_L(t)}{v(t)} - g_L(t)v(t) \quad (4)$$

Despite its apparent simplicity, achieving good dynamic behavior is not straightforward, as already reported in the literature [22]. This is due to the non-linear behavior of the voltage reaction to both CPLs and CILs disturbances as evidenced in (4). Nonetheless, if the disturbances are left apart, its reference tracking response is linear, defined by the Laplace domain transfer function (5).

$$\frac{V(s)}{V^*(s)} = \frac{k_p s + k_p\frac{1}{T_i}}{s^2C + sk_p + \frac{1}{T_i}k_p} \quad (5)$$

B. The Quadratic Voltage Controller (QVC)

An alternative to the DVC has been proposed in the literature referred as fast-acting DC-link voltage controller and energy based controller, in the context of applications for the DC-link control of DC/DC/AC and AC/DC/AC converters [22]–[25]. As a contribution of this paper, its generalization to any cascaded-based voltage control, such as grid-forming converters in both DC and 3-phase AC MGs applications is proposed. The control scheme is shown in Fig. 4b) and the regulator differential equation is given by (6). The closed-loop system using QVC is defined by (7). As in the case of DVC, that expression will be used as the starting point for the dynamic analysis of the QVC-based voltage control.

$$i^*(t) = \frac{k_p(v^{*2}(t) - v^2(t)) + k_p\frac{1}{T_i}\int (v^{*2}(t) - v^2(t))dt}{v(t)} \quad (6)$$

$$\frac{dv(t)}{dt}C = \frac{k_p\left(v^{*2}(t) - v^2(t)\right) + k_p\frac{1}{T_i}\int\left(\left(v^{*2}(t) - v^2(t)\right)dt\right)}{v(t)} - i_L(t) - \frac{P_L(t)}{v(t)} - g_L(t)v(t) \tag{7}$$

The control is based on the linear relation between the power flowing into the capacitor, and the instantaneous voltage squared. In [22], [24], its design is realized by exploiting the relation between voltage variations and the energy stored in the capacitor. However, the tuning method used in those papers is oriented to the regulation of the DC-link of an active front end (AFE) exposed to the steady state disturbances produced by AC grid unbalances. Here, a general approach based on disturbance rejection analysis is included, considering a meaningful comparison between DVC and QVC dynamic response.

One of the main advantages of QVC, concerning the disturbance rejection and stability analysis, is that the relation between $v^2(t)$ and $P_L(t)$ becomes linear (8), unlike in the case of DVC. This fact could simplify the delimitation of the stable region in case of considering only CPLs.

$$E(t) = \int P(t)dt = \frac{Cv^2(t)}{2} \xrightarrow[P(0)=v^2(0)=0]{\mathcal{L}} \frac{P(s)}{s} = \frac{CV^2(s)}{2} \tag{8}$$

However, the controlled variable is still $v(t)$ and considering CIL and CCL disturbances, being necessary the system linearization to perform a proper dynamic analysis.

Leaving the disturbances aside, unlike in the DVC, in the QVC the relation between v and v^* is non-linear, (6). The system defined in (7) has been linearized using the Taylor series approach. The linear approximation of the reference tracking transfer function is obtained as in (9), where V_0^* and V_0 are the voltage reference and the actual voltage at the equilibrium point, respectively. Assuming $V_0 \approx V_0^*$, the transfer function is approximated by (10).

$$\frac{V(s)}{V^*(s)} \approx \frac{s2k_pV_0^* + 2k_p\frac{1}{T_i}V_0^*}{s^2CV_0 + s2k_pV_0 + 2k_p\frac{1}{T_i}V_0} \tag{9}$$

$$\frac{V(s)}{V^*(s)} \approx \frac{s2k_p + 2k_p\frac{1}{T_i}}{s^2C + s2k_p + 2k_p\frac{1}{T_i}} \tag{10}$$

C. Establishing an Analytical Tuning Methodology

An analytical tuning methodology will be used to establish a parametric design of the regulator gains [2]. This will allow a proper an generalized comparison between the DVC and QVC, independent of the numeric value of the regulator gains. The close loop system can be simplified to a second order system with natural frequency ω_n and damping factor ζ. Equations (5) and (10), can be expressed as (11). Thus, the PI regulator gains for DVC and QVC are tuned according to (12) and (13) respectively. Fig. 5 shows an example of the reference tracking response, comparing the two methods when using $\omega_n = 2\pi 50$ and $\zeta = 0.7$ in both of them.

$$\frac{V(s)}{V^*(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{11}$$

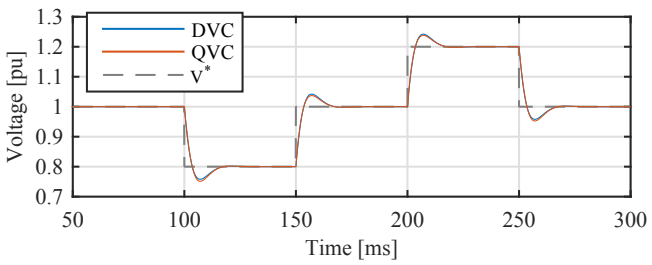

Fig. 5. Non-linear simulated reference tracking response. Comparison between DVC and QVC when using $\omega_n = 2\pi 50$ and $\zeta = 0.7$ in both methods.

$$\text{DVC} \rightarrow \quad k_p = 2\zeta\omega_n C \quad T_i = 2\zeta/\omega_n \tag{12}$$

$$\text{QVC} \rightarrow \quad k_p = \zeta\omega_n C \quad T_i = 2\zeta/\omega_n \tag{13}$$

D. Effect of the inner controller, delays and sensor

The inner current controller, PEC and sensor shown in Fig. 1 can condition the response given by the voltage controller. This section analyses the effect of those elements to determine the extent to which, considering them ideal, affects the voltage control loop. The linearized system in (11) becomes (14) where $G_i(s)$ and $G_{fb}(s)$ are the inner current control loop and the sensor transfer function respectively.

$$\frac{V(s)}{V^*(s)} = \frac{2\zeta\omega_n sG_i(s) + \omega_n^2 G_i(s)}{s^2 + 2\zeta\omega_n sG_i(s)G_{fb}(s) + \omega_n^2 G_i(s)G_{fb}(s)} \tag{14}$$

The inner current control can be modeled as a second order filter defined by (15). This transfer function considers a simplified model of the subsystem composed by the current controller, the power converter and the inductive coupling filter,

$$G_i(s) = \frac{I(s)}{I^*(s)} = \frac{\omega_{n_i}^2}{s^2 + 2\zeta_i\omega_{n_i}s + \omega_{n_i}^2}, \tag{15}$$

where ω_{n_i} and ζ_i are the current control loop natural frequency and damping factor respectively. Fig. 6 shows the frequency response for different ω_{n_i}/ω_n ratios both in open loop, (16), and closed loop, using $\omega_n = 2\pi 50$ and $\zeta = 1$ and $G_{fb} = 1$. Ratios equal and above 10 allow Gain Margins (GM) over 16 dB, Phase Margins (PM) above 60° and Delay Margins (DM) over 1.6 ms. In closed loop, the effect is shown above frequencies over ω_n, and the magnitude is close to ideal response for ratios above 5.

$$L(s) = \frac{2\zeta\omega_n + \frac{\omega_n^2}{s}}{s}G_i(s) \tag{16}$$

The sensor transfer function is modeled as pure delay and a 2^{nd} order Low Pass Filter (LPF) with $\zeta_s = 0.7$ as (17). When using digital controllers, the pure delay is usually associated to the sampling time and the LPF represent an anti-aliasing filter, neglecting the non-dominant poles of the voltage sensor in this kind of applications. Fig. 7 shows in a) the closed loop effect of different pure delays and in b) the effect when including the LPF with cutoff frequencies $\omega_{n_s} = 2\pi$ / $2\tau_d$ (2 times lower than the sampling frequency in case τ_d equals the sampling time). It is shown that the effect of the LPF is dominant but

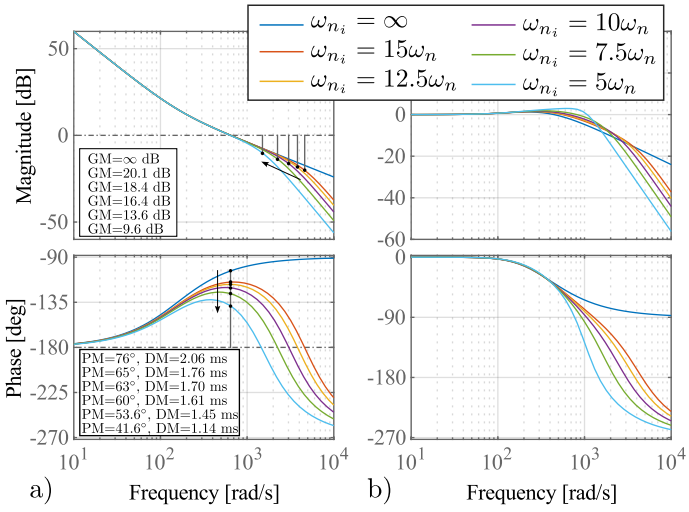

Fig. 6. Effect of the inner current control loop. a) Bode diagram of the open loop transfer function (16); b) Bode diagram of the transfer function (14) with ideal sensor($G_{fb} = 1$).

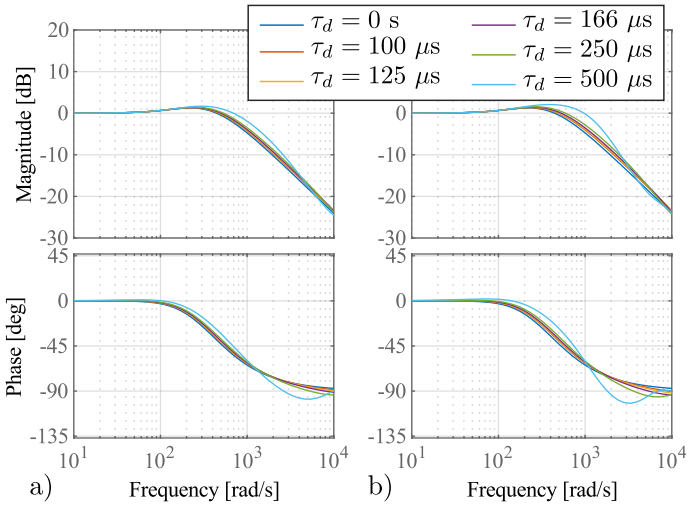

Fig. 7. Effect of the sensor delay and bandwidth with ideal inner control ($G_i = 1$). a) Bode diagram of the transfer function (14) and pure feedback delay ($G_{fb} = e^{-s\tau_d}$) ; b) Bode diagram of the transfer function (14) with LPF sensor and delay.

in any case G_{fb} is fairly negligible for delays below 500 μs ($\tau_d < 2\pi$ / $40\omega_n$) and $\omega_{n_s} > 20\omega_n$.

$$G_{fb}(s) = \underbrace{e^{-s\tau_d}}_{\text{delay}} \underbrace{\frac{\omega_{n_s}^2}{s^2 + 2\zeta_s\omega_{n_s}s + \omega_{n_s}^2}}_{\text{Anti-aliasing filter}} \tag{17}$$

Given the results, the sensor effect is neglected in the rest of the document while the current control effect will be further analyzed in Section VII.

IV. Closed Loop Disturbance Rejection Analysis

The main requirement of a grid-forming converter is a stiff voltage control under disturbances. As seen previously, the QVC presents a non-linear response for any case, while the DVC is linear only if CCL are taken into account. However, it is worth noting that the disturbance rejection of the system when using DVC becomes non-linear with CPLs or CILs. To analyze the system behavior under disturbances, the disturbance rejection transfer functions (load disturbance to output voltage) under different type of loads have been obtained by Taylor series linearization. The linearized transfer functions $\frac{\Delta V(s)}{\Delta P_L(s)}$, $\frac{\Delta V(s)}{\Delta I_L(s)}$ and $\frac{\Delta V(s)}{\Delta G_L(s)}$ in the Laplace domain are shown respectively in (18) for the DVC, and in (19) for the QVC. It is necessary to point out that an operation close to the equilibrium point is assumed, considering equal the voltage reference and the voltage at the equilibrium point ($V_0 = V_0^*$).

$$\overbrace{\begin{aligned}
\frac{\Delta V(s)}{\Delta P_L(s)} &\approx \frac{-sV_0}{s^2V_0^2C + s(k_pV_0^2 - P_{L0} + G_{L0}V_0^2) + \frac{1}{T_i}k_pV_0^2} \\
\frac{\Delta V(s)}{\Delta I_L(s)} &\approx \frac{-sV_0^2}{s^2V_0^2C + s(k_pV_0^2 - P_{L0} + G_{L0}V_0^2) + \frac{1}{T_i}k_pV_0^2} \\
\frac{\Delta V(s)}{\Delta G_L(s)} &\approx \frac{-sV_0^3}{s^2V_0^2C + s(k_pV_0^2 - P_{L0} + G_{L0}V_0^2) + \frac{1}{T_i}k_pV_0^2}
\end{aligned}}^{DVC} \tag{18}$$

$$\overbrace{\begin{aligned}
\frac{\Delta V(s)}{\Delta P_L(s)} &\approx \frac{-s}{s^2V_0C + s(2k_pV_0 + I_{L0} + 2G_{L0}V_0) + 2\frac{1}{T_i}k_pV_0} \\
\frac{\Delta V(s)}{\Delta I_L(s)} &\approx \frac{-sV_0}{s^2V_0C + s(2k_pV_0 + I_{L0} + 2G_{L0}V_0) + 2\frac{1}{T_i}k_pV_0} \\
\frac{\Delta V(s)}{\Delta G_L(s)} &\approx \frac{-sV_0^2}{s^2V_0C + s(2k_pV_0 + I_{L0} + 2G_{L0}V_0) + 2\frac{1}{T_i}k_pV_0}
\end{aligned}}^{QVC} \tag{19}$$

In these equations, the equilibrium point is defined by $x_0 = [V_0, P_{L0}, G_{L0}]$ for DVC and $x_0 = [V_0, I_{L0}, G_{L0}]$ for QVC. V_0 is the steady state voltage at the equilibrium point. P_{L0}, G_{L0} and I_{L0} are the load level at the equilibrium point in terms of power associated to CPLs, conductance given by CILs and current drawn by CCLs at the equilibrium point. This evince a clear dependence of the dynamic response on the load level at the equilibrium point, affecting the steady state consumption and generation to the system dynamic performance, that can lead to an unexpected behavior. As CPLs represent the most critical type of loads at the present time, special attention will be given to the CPL disturbance rejection transfer functions. The following analysis will mainly focus on the first expressions in (18) and (19).

A. Normalization and validation of the CPL disturbance rejection transfer function

Using (12) and (13) in (18) and (19), they can be expressed in terms of ω_n and ζ as (20) and (21) for DVC and QVC respectively, leading to similar expressions.

$$\frac{\Delta V(s)}{\Delta P_L(s)} \approx \frac{-1}{V_0 C} \frac{s}{s^2 + s(2\omega_n\zeta - \frac{P_{L0}}{V_0^2 C} + \frac{G_{L0}}{C}) + \omega_n^2} \quad (20)$$

$$\frac{\Delta V(s)}{\Delta P_L(s)} \approx \frac{-1}{V_0 C} \frac{s}{s^2 + s(2\omega_n\zeta + \frac{I_{L0}}{V_0 C} + \frac{2G_{L0}}{C}) + \omega_n^2} \quad (21)$$

By defining factors for representing the terms related to load level at the equilibrium point, a general expression valid for both DVC and QVC is formulated as (22).

$$\frac{\Delta V(s)}{\Delta P_L(s)} \approx -K \frac{s}{s^2 + s(2\omega_n\zeta + \alpha_0 + \beta_0) + \omega_n^2} \quad (22)$$

Where the close loop gain can be defined as $K = \frac{1}{V_0 C}$, while α_0 and β_0 are normalized factors that represents the effect of the load level, being defined by the expressions in Table I for the different controllers. From (22), it is expected an identical response in absolute value for systems with different V_n or C as far as the product $V_0 C$ remains constant.

TABLE I
DEFINITION OF α_0 AND β_0

	α_0	β_0		α_0	β_0
DVC	$\frac{-P_{L0}}{V_0^2 C}$	$\frac{G_{L0}}{C}$	QVC	$\frac{I_{L0}}{V_0 C}$	$\frac{2G_{L0}}{C}$

Furthermore, (22) can be normalized to per-unit (p.u.) by modifying the variable K as shown in K_{pu} (23), leading to the full normalize expression in (24), where V_n and P_n are the converter nominal voltage and power respectively.

$$K_{pu} = \frac{P_n}{V_n} \frac{1}{V_0 C} \rightarrow V_0 = V_n \rightarrow K_{pu} = \frac{P_n}{V_0^2 C} \quad (23)$$

$$\frac{\Delta V_{pu}(s)}{\Delta P_{Lpu}(s)} \approx -K_{pu} \frac{s}{s^2 + s(2\omega_n\zeta + \alpha_0 + \beta_0) + \omega_n^2} \quad (24)$$

where $\Delta V_{pu} = \frac{\Delta V}{V_n}$ and $\Delta P_{Lpu} = \frac{\Delta P_L}{P_n}$. From (24), it is expected an identical response in p.u. for systems with different V_n or C as far as the term $V_0^2 C$ remains constant.

To verify the linearized models, the response of $\frac{\Delta V(s)}{\Delta P_L(s)}$ and $\frac{\Delta V_{pu}(s)}{\Delta P_{Lpu}(s)}$ is compared in Figs. 8 and 9 with the simulation of the non-linear system obtained in Matlab/Simulink®, for DVC and QVC respectively. The results have been obtained for 2 example scenarios with different V_n and C, maintaining the term $V_0^2 C$ constant. The parameters are listed in Table II.

The error between the actual response and the linear approximation validates the linear models near the equilibrium point. However, in the case of DVC, when the load level P_{L0} is not considered, the linear model considerably deviates from the actual response as the system deviates from the equilibrium point. It is also clear, how the p.u. response remains the same for the two scenarios, validating the equations (22) and (24).

TABLE II
ANALYTICAL AND SIMULATION PARAMETERS

Parameter	Scenario 1	Scenario 2
Nominal Voltage V_n	325 V	650 V
Capacitor C	40μF	10μF
Nominal Active Power P_n	50kW	50kW
ω_n	2π50 rad/s	2π50 rad/s
ζ	1	1

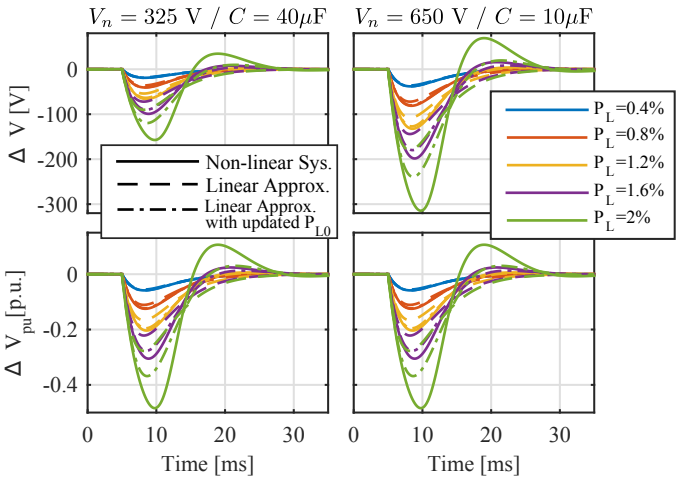

Fig. 8. DVC: Non-linear simulated response compared with the linear approximation of $\frac{\Delta V(s)}{\Delta P_L(s)}$ under increasing active power steps. Top, absolute value. Bottom, pu deviation.

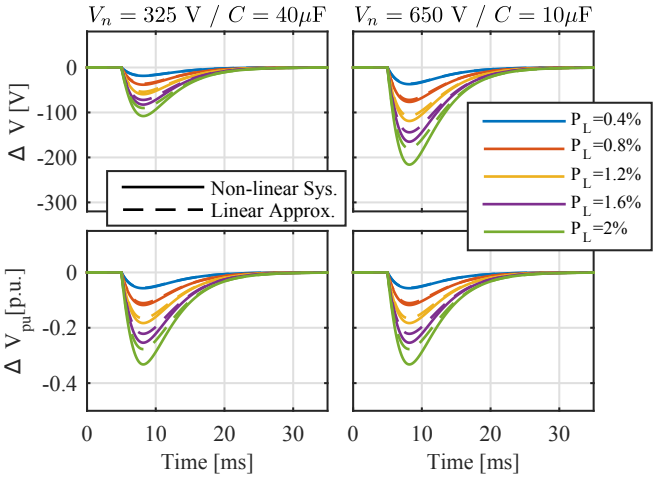

Fig. 9. QVC: Non-linear simulated response compared with the linear approximation of $\frac{\Delta V(s)}{\Delta P_L(s)}$ under increasing active power steps. Top, absolute value. Bottom, p.u. deviation.

B. Effect of the Load Levels in the System Stability

To analyze the effect of the load level at the equilibrium point, the system root-contour for the factors associated to the load level at the equilibrium point, α_0 and β_0, have been obtained for studying the stability limitations imposed by the load level. The root-contour expression can be generalized into a single equation for DVC and QVC by using the terms α_0 and β_0 defined in Table I. The resulting equation is (25).

$$1 + (\alpha_0 + \beta_0) G(s) H(s) \approx 1 + (\alpha_0 + \beta_0) \frac{s}{s^2 + s2\omega_n\zeta + \omega_n^2} \quad (25)$$

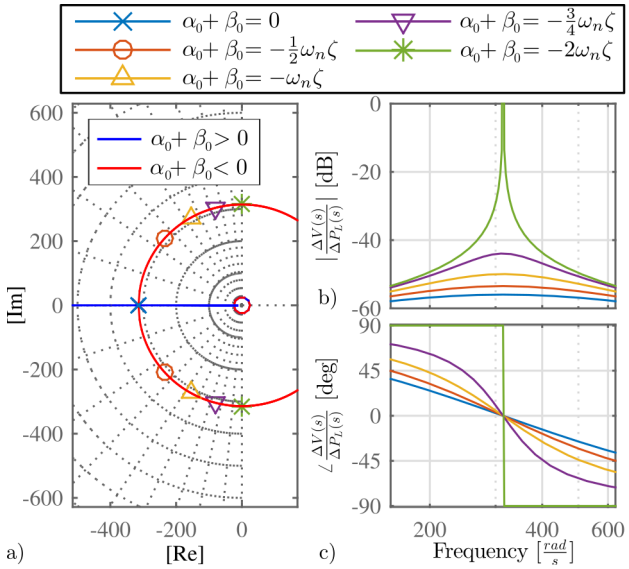

Fig. 10. System response depending on the load level terms α_0 and β_0. a) System root-contour for the gain $(\alpha_0+\beta_0)$ valid for DVC and QVC. b) and c) Bode diagram of the closed loop disturbance rejection transfer function for different values of $\alpha_0+\beta_0$.

This expression leads to the theoretical stability condition in (26), being the system stable whereas the condition is met.

$$\alpha_0+\beta_0 \geq -2\omega_n\zeta \tag{26}$$

Fig. 10 shows the system root-contour for the $(\alpha_0+\beta_0)$ term and the Bode diagram of the closed loop disturbance rejection in (22) ($\frac{\Delta V}{\Delta P_L}$) with $K=1$ and $\omega_n = 2\pi 50$rad/s. From Fig. 10, it is clear how the system damping is increased as $\alpha_0+\beta_0$ increases, while it tends to instability as $\alpha_0+\beta_0$ decreases, reaching the expected stability limit. In the DVC topology, α_0 will present negative sign under CPL (i.e. if P_{L0} is positive). As commented before, in case $\beta_0(\frac{G_{L0}}{C})$ is not high enough to cancel the effect of $\alpha_0(\frac{-P_{L0}}{V_0^2C})$, the system poles will move to the right as P_{L0} increases. For the QVC approach, P_{L0} term does not contribute to the system instability, which is one of the main advantages of this method over the widely used DVC. It is worth to point out that such an advantage has not been reported yet in the literature. Nonetheless, a dependency on CCLs appears in the QVC, represented by the load level I_{L0} (α_0=$\frac{I_{L0}}{V_0C}$)). Although positive load currents, $I_{L0}\geq 0$, does not present stability problems, a potential issue appears when $I_{L0}<0$, i.e. when constant current generation (CCG) is considered. G_{L0} appears in both methods and has a positive impact in the system damping for both DVC and QVC. However, if $G_{L0}<0$, i.e., when some equipment in the grid behaves as a negative resistor, like a generator operating in voltage/current droop mode, the system response can be also worsen until instability. An example of the stability limits for the scenario 1 defined in Table II is summarized in Table III.

For the same system, the time domain responses of DVC and QVC for a 2% CPL step (1kW) are shown in Fig. 11 for different load levels. It is clear how the system tends to oscillate as the conditions in Table III are approached.

TABLE III
EXAMPLE OF STABILITY LIMITS FOR THE SYSTEM DEFINED IN TABLE II

	Load Level Stability Limits		
	P_{L0} (if $G_{L0}=0$)	I_{L0} (if $G_{L0}=0$)	G_{L0} (if $P_{L0}=0$ or $I_{L0}=0$)
DVC	2.66 kW	$\pm\infty$	$-25\text{m}\Omega^{-1}$
QVC	$\pm\infty$	-8.175 A	$-12.5\text{m}\Omega^{-1}$

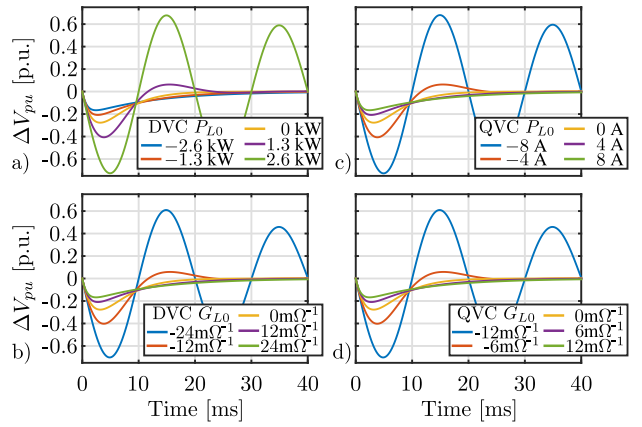

Fig. 11. Step response under a CPL step disturbance of 2%(1kW). a) Influence of P_{L0} in DVC; b) Influence of I_{L0} in QVC; c) Influence of G_{L0} in DVC; d) Influence of G_{L0} in QVC.

Conversely, when the load levels move away from the stability limit, the system damping is improved.

The effect of P_{L0} in the time domain response is illustrated in Fig. 12, where the behavior of DVC and QVC methods are compared under CPL increasing steps, from $P_L(t)=0$ to $P_L(t)=2.6$ kW (near the stability limit). As expected, unlike in the QVC, for the same load step, the response in the DVC method is altered for the worse at higher load levels.

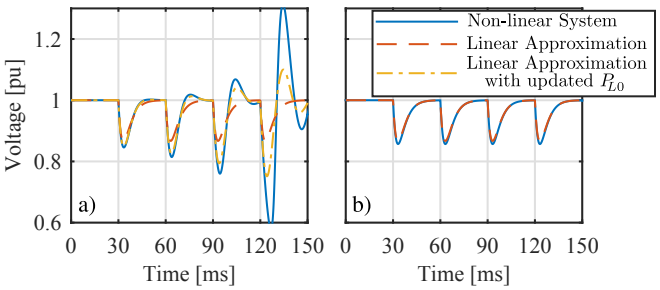

Fig. 12. Disturbance response under increasing CPL. Load is increased by steps of 480W (9.6%) every 30ms. Dashed lines show the linear approximations. a) DVC. b) QVC. Results using the data in Table II.

C. Voltage Collapse

The voltage level also represents a potential cause of instability as it deviates from the equilibrium point. The voltage collapse for both controllers is represented in Fig. 13 for a step CPL disturbance. As it is shown, the QVC is not only independent of the CPL load level at the equilibrium point, P_{L0}, but also withstands higher CPL step disturbances before it collapses. This effect will be further explored in section VI-A.

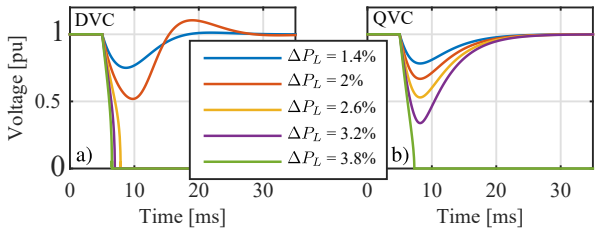

Fig. 13. Voltage collapse under CPL steps. a) DVC performance for an initial $P_{L0} = 0$; b) QVC performance. Results using the data in Table II.

V. Effect of System Capacitor and the Use of Virtual Capacitance

The capacitor and controller bandwidth take an important role in the system behavior. While the bandwidth is limited by the inner control loop, the size of the capacitor depends on the application. In DC voltage control applications, such as those found in DC-links, the capacitor is usually sized according to the expected oscillations caused by stationary power fluctuations, which in some cases leads to oversizing [24], [37]. Regarding AC grid-forming converters, the capacitor is often determined by the filtering requirements of switching frequency harmonics, leading to small capacitor values.

Increasing the capacitor size while maintaining ω_n and ζ, will lead to an improved disturbance rejection without compromising the system stability. Fig. 14 shows the dynamic stiffness in the frequency domain and the time domain for 1kW step response of the disturbance rejection transfer function $\frac{\Delta V(s)}{\Delta P_L(s)}$ for different capacitor values using DVC and QVC. It is worth noting that the QVC and DVC performance is the same if $P_{L0} = 0W$.

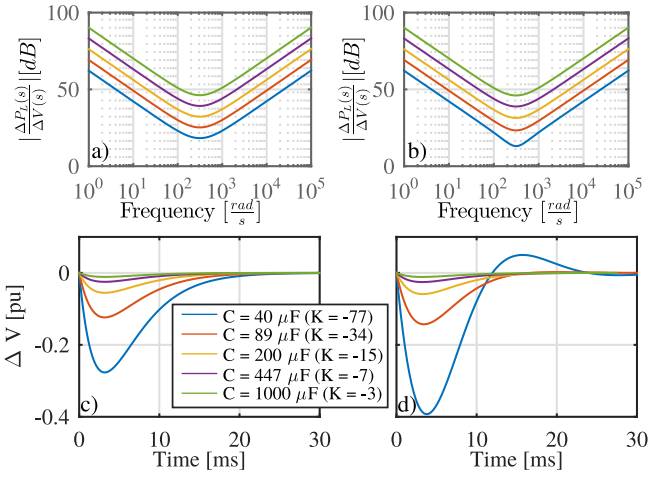

Fig. 14. Evaluation of the capacitor size effect in the disturbance rejection capabilities. a) DVC and QVC dynamic stiffness, $\frac{\Delta P_L(s)}{\Delta V(s)}$, for different capacitor values and $P_{L0} = 0$W; b) DVC dynamic stiffness when $P_{L0} = 1.2$k; c) DVC and QVC step response of the transfer function $\frac{\Delta V(s)}{\Delta P_L(s)}$ for $P_{L0} = 0$W; d) DVC step response of the transfer function $\frac{\Delta V(s)}{\Delta P_L(s)}$ for $P_{L0} = 1.2$kW.

As expected, the disturbance rejection is improved as the capacitor increases. The size of the capacitor has a direct influence on the maximum disturbance the system can withstand,

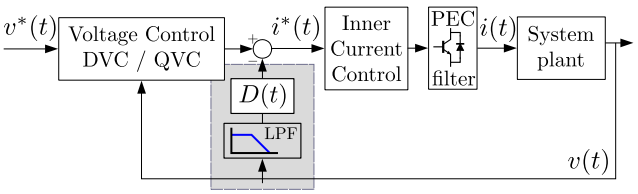

Fig. 15. Modified voltage control scheme using virtual capacitance C_v.

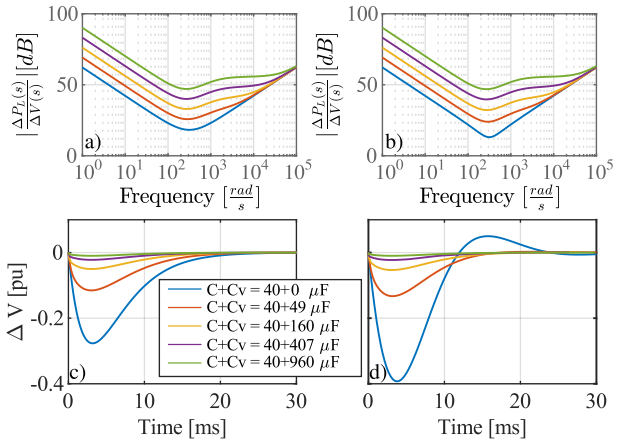

Fig. 16. Effect of the virtual capacitor LPF in the the disturbance rejection response. LPF BW of 200 Hz. For a),b),c) and d) refer to caption of Fig. 14.

presenting the QVC a better performance, specially noticeable under low capacitance.

Techniques for voltage control disturbance rejection enhancement have been proposed in the past, mainly based on load decoupling through measurements, observers or estimators [32]. A simpler alternative, presented before in the literature [34]–[36], is shown in Fig. 15, where $D(t) = C_v \frac{d}{dt}$. Using a pseudo-derivative feedback control, it is possible to add a virtual capacitance C_v which ideally will be added to the passive capacitance C, improving the disturbance rejection. Assuming an ideal derivative and ideal sensors, the transfer functions for DVC and QVC, can be modified by substituting the parameter C by $C+C_v$. In addition, the virtual capacitance does not only allow to improve the dynamic stiffness but can also be used to emulate low capacitance systems by applying a negative value, i.e. $C_v < 0$. Nonetheless, it is necessary to consider that the real implementation of the virtual capacitance is limited by the associated LPF. This should be set as high as possible, usually limited by the noise present in the feedback signal, but lower than the current control loop. Fig. 16 shows the non ideal response for a bandwidth of 200 Hz, affecting to the disturbance rejection at frequencies above that, but performing as ideal for frequencies below.

VI. Effect of the Nominal Operating Point and Bandwidth: Dynamic Analysis and Design

Besides the stability limits, one of the most important characteristics considered for the design and analysis is the maximum voltage deviation under CPL steps. In this section, an analytical expression that allows to determine that deviation is proposed.

A. Dynamic Analysis of maximum voltage deviation and maximum power step

To normalize the effect of the capacitance, the nominal voltage and the nominal active power on the system response, to make this study applicable to any scenario, the parameter K_{pu} was defined previously in (23), being dependent on these three parameters. If we define a new damping factor ζ' as (27), the analytical linearized response becomes a function of three factors: K_{pu}, ω_n and ζ'. Moreover, the stability condition will be now dependent on ζ', being the system stable as far as $\zeta' \geq 0$.

$$\zeta' = \zeta + \frac{\alpha_0 + \beta_0}{2\omega_n} \tag{27}$$

Thus, the maximum voltage deviation $\Delta V_{\substack{pu \\ max}}$ can be obtained with (28), where t_m is defined by (29).

$$\frac{\Delta V_{\substack{pu \\ max}}}{\Delta P_{Lpu}} = \begin{cases} \frac{K_{pu} e^{\left(-t_m \omega_n \zeta'\right)} \sin\left(t_m \omega_n \sqrt{1-\zeta'^2}\right)}{\omega_n \sqrt{1-\zeta'^2}} & if\ 0 \leq \zeta' < 1 \\ K_{pu} t_m \frac{e^{-t_m \omega_n}}{\omega_n} & if\ \zeta' = 1 \\ \frac{K_{pu} e^{\left(-t_m \omega_n \zeta'\right)} \sinh\left(t_m \omega_n \sqrt{\zeta'^2-1}\right)}{\omega_n \sqrt{\zeta'^2-1}} & if\ \zeta' > 1 \end{cases} \tag{28}$$

$$t_m = \begin{cases} \tan^{-1}\left(\frac{2\zeta'\sqrt{1-\zeta'^2}}{2\zeta'^2-1}\right) \frac{1}{2\omega_n \sqrt{1-\zeta'^2}} & if\ 0 \leq \zeta' < 1 \\ \frac{1}{\omega_n} & if\ \zeta' = 1 \\ \frac{\log\left(\frac{1}{\zeta' - \sqrt{\zeta'^2-1}}\right)}{\omega_n \sqrt{\zeta'^2-1}} & if\ \zeta' > 1 \end{cases} \tag{29}$$

To evaluate the effect of K_{pu} and ω_n considering the non-linearities, a non-linear simulation of the systems described by (4) and (7) has been conducted as an example using Matlab/Simulink® and ode45 solver. $\zeta = 1$ and $P_{L0} = I_{L0=}G_{L0} = 0$ are considered in the equilibrium point. Fig. 17 shows the maximum voltage deviation under a CPL step as a function of K_{pu}, and the power step disturbance, ΔP_{Lpu}. The results are shown for DCV and QVC for two different bandwidths, ω_n. $\Delta V_{pu} = 1$ represents the system voltage collapse or instability. It is worth to point out that the QVC extends the region of operation, allowing a better disturbance rejection and avoiding voltage collapse with higher K_{pu} values compared with the DVC method. The solid black line represents the analytical results for a $\Delta V_{pu} = 0.5$ pu, being in close agreement with the non-linear simulation results.

The voltage control bandwidth plays also an important role in the maximum voltage deviation. As an example of its effect, Fig. 18 shows the maximum CPL step, $\Delta P_{L_p u}$ that leads to a maximum voltage deviation of $\Delta V_{\substack{pu \\ max}} = 0.65$ pu. This maximum $\Delta P_{L_p u}$ is shown as a function of K_{pu}, and the controller bandwidth, ω_n. $\Delta P_{Lpu} = 1$ indicates that the system can withstand a CPL step of a power equal to the

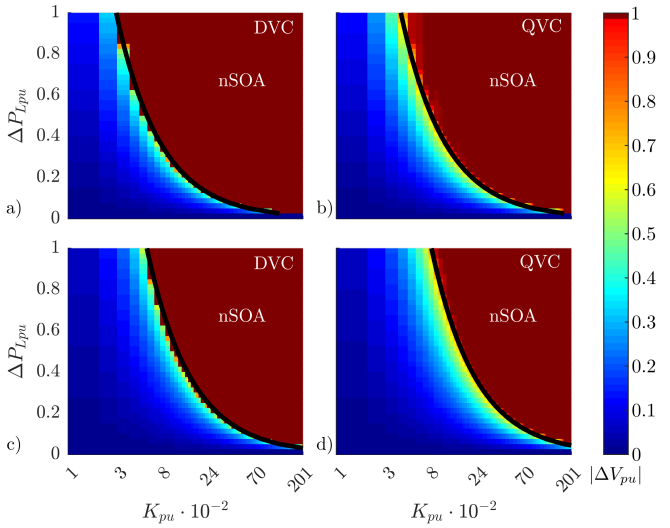

Fig. 17. Maximum voltage deviation depending on the CPL step disturbance and the K_{pu} value. Simulation results. a) DVC, ω_n=2π50 rad/s. b) QVC, ω_n=2π50 rad/s. c) DVC, ω_n=2π100 rad/s. d) QVC, ω_n=2π100 rad/s. Dark red (ΔV_{pu}=1) is considered as the non-Safe Operating Area (nSOA).

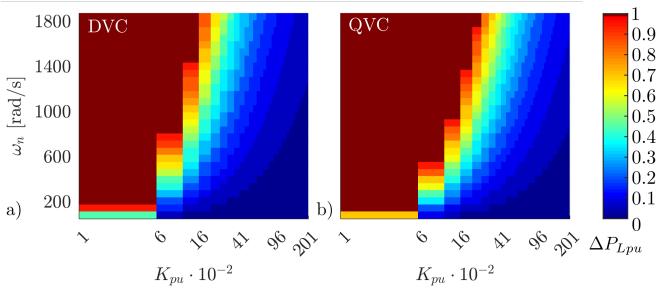

Fig. 18. Maximum CPL step disturbance for a maximum voltage deviation of 0.65 p.u., depending on the K_{pu} value and the voltage control bandwidth, ω_n, for $\zeta = 1$ and $\alpha_0 + \beta_0 = 0$. a) DVC. b) QVC. Non-linear simulation.

rated while keeping the voltage $\Delta V_{\substack{pu \\ max}} \leq 0.65$ pu. The value of 0.65 pu has been used as an example, but this analysis can be perform for any value of $\Delta V_{\substack{pu \\ max}}$.

B. System design based on maximum voltage deviation

The expressions derived in the previous sections can result as an useful and easy tool for the design and selection of the system parameters as well as its characterization. Both the analytical expressions and the simulation of the non-linear system, allows to select the value of K_{pu} or ω_n to comply with a determined dynamic response, keeping the stability, under CPL steps. It also offers the possibility for predicting the system behavior. When looking for the system design, as K_{pu} depends on 3 parameters, its selection allows to determine the value of one parameter fixing the other 2. Thus, given a ω_n, for a determined nominal voltage, V_n and nominal power, P_n, the size of the capacitor, C, can be obtained for a desired response. Similarly, given C, V_n and P_n, ω_n can be inferred. Two alternative procedures are proposed in Fig 19.

Table IV shows an example of design to select the capacitance given the system parameters (ω_n, ζ, V_n, P_n) and

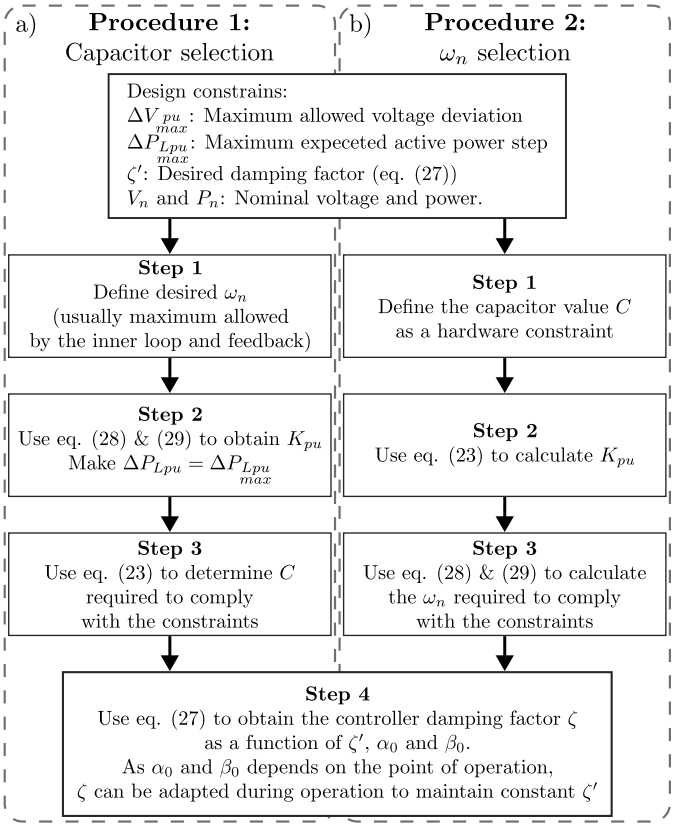

Fig. 19. Proposed design procedures. a) Capacitor selection. b) ω_n selection.

TABLE IV
EXAMPLE OF SYSTEM DESIGN USING THE PROPOSED METHODOLOGY

Design constrains and System Parameters					
ΔP_{Lpu}^{max}	ΔV_{max}^{pu}	$\omega_n[\frac{rad}{s}]$	ζ	V_n[V]	P_n[kW]
0.1	0.4	$2\pi 50$	1	325	50
Result					
$K_{pu}[s^{-1}]$			$C[\mu F]$		
3416			**138**		

the maximum voltage deviation (ΔV_{max}^{pu}) for a determined maximum CPL step (ΔP_{Lpu}^{max}) using QVC.

Regarding the selection of ω_n and ζ, it will depend on the characteristics of the inner control loop and the expected load level in the equilibrium point respectively. In the case of ω_n, it can be selected as high as possible, maintaining a high ratio between the outer and inner control loop bandwidth (usually > 10 in cascaded control systems). Appart from this limitation, in case of LC or LCL filters, the resonance frequency has to be damped and kept out of the current control bandwidth, imposing a superior limit for the overall system bandwidth [38]. The damping factor ζ can be selected depending on the expected α_0 and β_0. As those terms will vary depending on the load profile, it becomes interesting to adapt the value of ζ based on the load levels P_{L0}, I_{L0} and G_{L0}.

VII. EFFECT OF THE INNER CURRENT CONTROL LOOP

In the analysis carried out in the previous sections, the inner control loop has been considered as an ideal system with unitary gain and infinite bandwidth. This simplification assumes the decoupling between the outer and inner control loops if the ratio between their bandwidths is high enough. However, in a real implementation, the selection of such a ratio might not be trivial. Although the design and structure of the inner control loop is out of the scope of this paper, this section analyses the role of the inner control in the application under study. The inner current control is modeled as the second order low pass filter defined before in (15).

TABLE V
DEFINITION OF α_1, β_1, α_2 AND β_2

	α_1	β_1	α_2	β_2
DVC	$\frac{-P_{L0}2\zeta_i}{V_0^2 C\omega_{n_i}}$	$\frac{G_{L0}2\zeta_i}{C\omega_{n_i}}$	$\frac{-P_{L0}}{V_0^2 C\omega_{n_i}^2}$	$\frac{G_{L0}}{C\omega_{n_i}^2}$
QVC	$\frac{-P_{L0}2\zeta_i}{V_0^2 C\omega_{n_i}}$	$\frac{G_{L0}2\zeta_i}{C\omega_{n_i}}$	$\frac{-P_{L0}}{V_0^2 C\omega_{n_i}^2}$	$\frac{G_{L0}}{C\omega_{n_i}^2}$

Including this subsystem in the models defined in Sections III and IV and applying linearization, the expression in (24) is modified, obtaining the 4^{th} order transfer function in (30), where $a_0 - a_4$ are defined in (31).

$$\frac{\Delta V_{pu}(s)}{\Delta P_{Lpu}(s)} \approx -K_{pu}\frac{s^3\frac{1}{\omega_{n_i}} s^2\frac{2\zeta i}{\omega_{n_i}} + s}{s^4 a_0 + s^3 a_1 + s^2 a_2 + s a_3 + a_4} \quad (30)$$

$$a_0 = \frac{1}{\omega_{n_i}^2}; \qquad a_1 = \frac{2\zeta_i}{\omega_{n_i}} + \alpha_2 + \beta_2;$$
$$a_2 = 1 + \alpha_1 + \beta_1; \quad a_3 = 2\omega_n\zeta + \alpha_0 + \beta_0; \quad a_4 = \omega_n^2 \quad (31)$$

The inner control loop gives rise to the definition of 4 new terms related with the load level, ω_{n_i} and ζ_i. The terms α_1, β_1, α_2 and β_2 are defined in Table V.

As shown, considering $\omega_{n_i} = \infty$, (30) turns to be equal to (24). However, the consideration of finite inner control loop bandwidth reveals new dependencies in the load level. It is worth to point out that a dependency on P_{L0} appears now in the QVC, which effect depends on the inner loop bandwidth. The larger is ω_{n_i}, the smaller the effect of P_{L0}. To analyze the effect of ω_{n_i} and P_{L0} when considering non-ideal inner loop, the system has been evaluated in two cases: 1) using different ratios between ω_{n_i} and ω_n blue($\frac{\omega_{n_i}}{\omega_n}$) for a fixed value of P_{L0} and 2) using different values of P_{L0} for a fixed $\frac{\omega_{n_i}}{\omega_n}$ ratio. Fig. 20 shows the frequency response of (30) for both DVC (left) and QVC (right), using the parameters of scenario 1 in Table II and $\zeta_i = 0.707$.

In the upper part of Fig. 20, $P_{L0} = 4\%$ and different ratios of $\frac{\omega_{n_i}}{\omega_n}$ are analyzed. ω_{n_i} affects mainly at high frequencies, reducing the disturbance rejection as ω_{n_i} decreases. Nonetheless, the response is always similar for all the cases (≤ 1 dB) at least for frequencies below the voltage loop natural frequency ω_n. Nonetheless, an underdamped response is observed for all the cases in DVC and for QVC with low ω_{n_i}. It is worth pointing out that the disturbance rejection for the DVC is worse than for the QVC in any of the cases. The lower part of Fig. 20 shows the response using a $\frac{\omega_{n_i}}{\omega_n}$ ratio of 10, common in cascaded controllers, and increasing P_{L0}. As expected, the effect of P_{L0} in the DVC remains as in the previous analysis, ensuring a

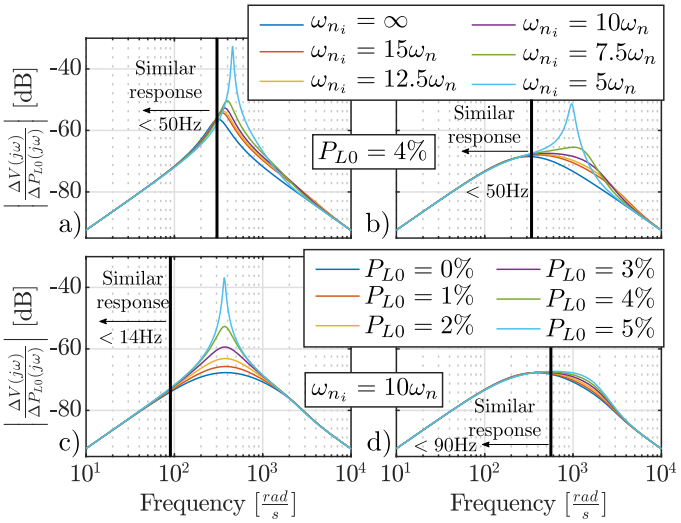

Fig. 20. Bode magnitude plot of the transfer function (30). a) DVC fixed $P_{L0} = 4\%$; b) QVC fixed $P_{L0} = 4\%$; c) DVC fixed $\omega_{n_i} = 10\omega_n$; d) QVC fixed $\omega_{n_i} = 10\omega_n$.

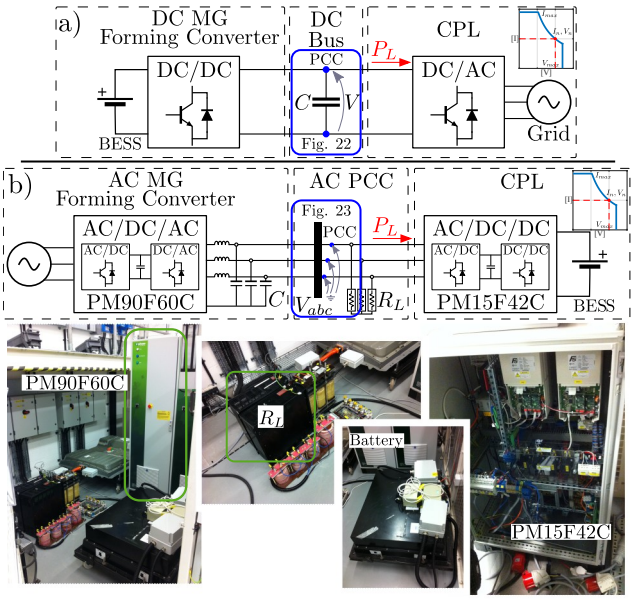

Fig. 21. Experimental setup. a) DC MG (PM15F42C); b) AC MG (PM90F60C & PM15F42C). The blue boxes locate the measurement points at point of common coupling (PCC).

similar response only below 14 Hz for the analyzed cases. On the other hand, although P_{L0} affects the response in the QVC when considering a finite ω_{n_i}, the effect is reduced and present only at high frequencies above the voltage control bandwidth. Some conclusions can be drawn, 1) increasing the inner control bandwidth can drastically reduce the effect of P_{L0} in the QVC but not in the DVC, 2) ω_{n_i} affects at frequencies higher than ω_n as soon as the system is stable, 3) the effect of P_{L0} is acceptable in the QVC for $\omega_{n_i} \geq 10$, and 4) the effect of P_{L0} in the DVC might be more critical than the ratio $\frac{\omega_{n_i}}{\omega_n}$.

VIII. Experimental Results

The control models presented in this paper have been tested experimentally under 2 different scenarios, covering the application of voltage control in both DC and AC grids. The experimental results have been obtained using the Triphase power modules PM15F42C and PM90F60C. The experimental parameters are included in Table VI.

TABLE VI
System Parameters Used for Voltage Control Analysis

Device Information	PM15F42C	PM90F60C
Topology	back to back 2-level 3-ph IGBT inverter	
Controller	FPGA + Monitoring PC	
Rated Power	11 kW	90 kW
AC Filter Inductance L	800 μH	500 μH
Switching frequency f_{sw}	8 kHz	16 kHz
Sampling time T_s	125 μs	62.5 μs
System Parameters	DC MG Fig. 21a)	AC MG Fig. 21b)
Voltage reference V^*	680 V_{DC}	230 $V_{AC_{rms}}$
Nominal Frequency	DC	50 Hz
Nominal Active Power P_n	11 kW	90 kW
Capacitor C	1000 μF	40 μF
Current control (PI) ω_{n_i}/ζ_i	2π500 rad/s / 0.7	2π500 rad/s / 0.7
Voltage control (PI) ω_n/ζ	2π6 rad/s / 0.7	2π50 rad/s / 1

Fig. 21 illustrates the simplified scheme of the experimental setups. For the DC voltage control, an inverter coupled to the DC/DC converter of a battery energy storage system (BESS) has been used (PM15F42C). The DC-link voltage is controlled by a DC/DC forming converter fed by the battery, while a DC/AC 3-phase grid tied converter operates as a DC CPL. To test the AC voltage control, the PM90F60C 3-ph converter has been used as the AC grid-forming converter while the D-Statcom with BESS (PM15F42C) plays the role of an AC CPL. An additional 56 Ω resistive load, R_L, has been included in the MG ($G_L = \frac{1.5}{56}$ considering 3-phase system). The AC control has been implemented in the *dq* synchronous reference frame applying the QVC and DVC to both d and q axis [31].

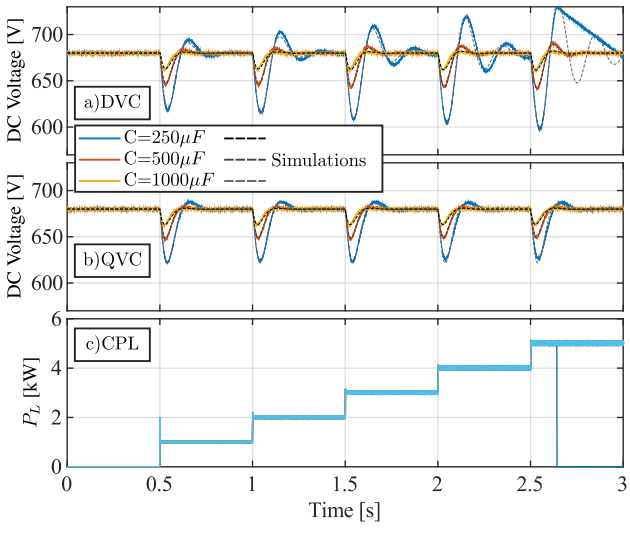

Fig. 22. DC setup experimental results. DC grid forming converter performance for different capacitor values. a) DVC and b) QVC are compared under multistep P_L, from 0 to 5kW. Dashed lines show average model simulations.

Fig. 22 shows the response of both DVC and QVC under increasing CPL steps for several capacitor values in the DC

MG setup. Due to the experimental setup limitations, the capacitor has been resized using virtual capacitance (Fig. 15), being the physical capacitor value 1000 μF. To better illustrate the effect, the voltage regulator bandwidth has been set to 6Hz.

Fig. 23 shows the performance comparison between DVC and QVC in the AC 3-ph MG with an increasing CPL. The instantaneous voltage magnitude is represented. As expected from simulations, the DVC dependency on the load level makes its response to be worsen with increased CPL level (P_{L0}). It is worth noting that the local resistive load provides an improved damping, allowing to move the stability limit from $P_{L0} \simeq 2.66$ kW (see Table III) to $P_{L0} \simeq 5.5$ kW.

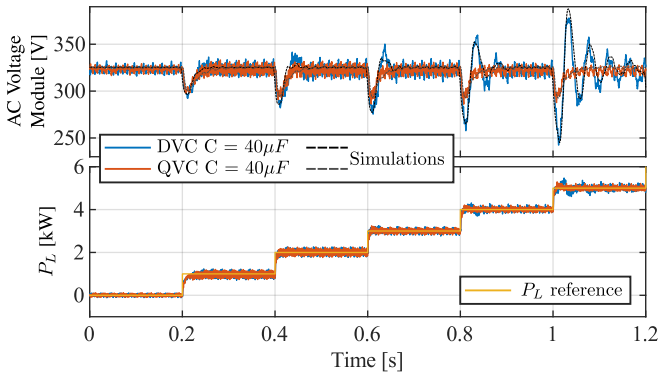

Fig. 23. AC setup experimental results. AC grid forming converter performance. DVC and QVC are compared under multistep P_L, from 0 to 5kW. Dashed lines show average model simulation results under same load profile.

To demonstrate the use of virtual capacitance applied to the AC setup, the performance under different virtual capacitance values is shown in Fig. 24 comparing the step response of DVC and QVC. The improved response of the QVC with respect to the DVC should be highlighted, specially when low capacitance values are used. A cut-off frequency of 200Hz has been used for the Virtual Capacitance LPF selected experimentally, pursuing the maximum possible bandwidth without being affected by feedback noise.

To demonstrate the viability of the response prediction proposed in Section VI, the experimental data in Figs. 22 and 23 have been compared with the expected response obtained analytically with the expressions (28) and (29). The results are shown in Fig. 25, exhibiting a close match between the experiments and the predicted ΔV_{pu}.

IX. Conclusions

The paper has proposed a simple but effective methodology for the analysis of cascaded voltage control in grid-forming units feeding different type of loads, with a special concern about CPLs. The study has focused in the analysis of two PI-based control methods, DVC and QVC, that have been compared outlining their benefits and drawbacks, summarized in Table VII. The QVC has proved to enhance the dynamic behavior under CPL disturbances. As demonstrated, the proposed generalized method can be applied to converter having different rated values, thus having the potential of becoming a design tool. It is worth noting that the methodology leaves up

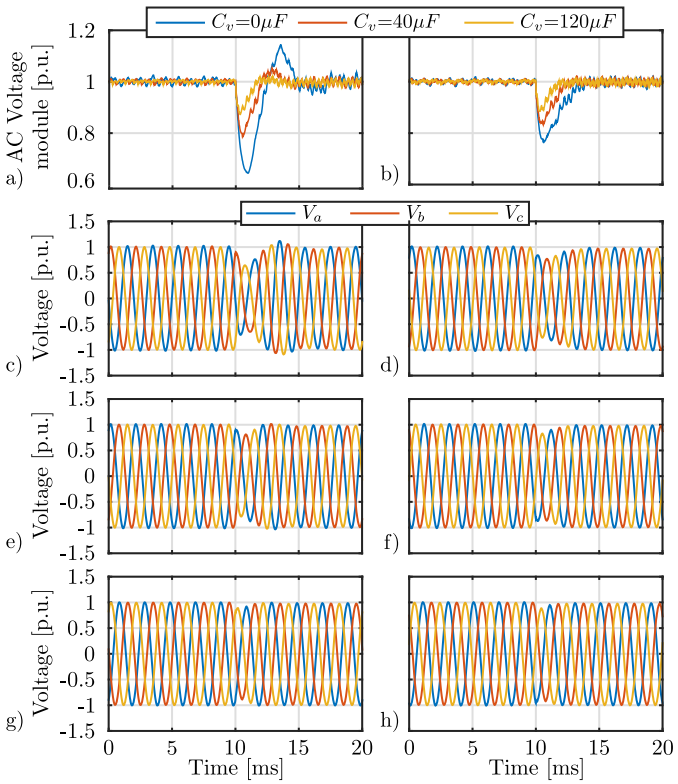

Fig. 24. AC setup experimental results (voltage at PCC). DVC and QVC responses using different values of virtual capacitance. Step of $P_L = 2.5$ kW at $t = 0.1$ s. a) DVC voltage magnitude comparison; b) QVC voltage magnitude comparison; c), e) and g) DVC phase voltages for $C_v = 0$ μF, $C_v = 40$ μF and $C_v = 120$ μF; d), f) and h) QVC phase voltages for $C_v = 0$ μF, $C_v = 40$ μF and $C_v = 120$ μF.

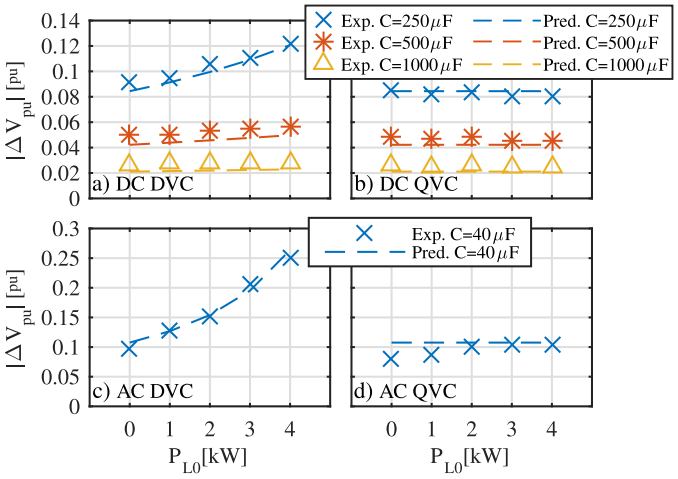

Fig. 25. Comparison between the experimental results and the analytical prediction of ΔV_{pu} for different values of P_{L0}. Dashed lines represent the predicted response. a)DC setup using DVC; b)DC setup using QVC; c)AC setup using DVC; d)AC setup using QVC.

to the designed the selection of parameters which are application dependant such as the load level in the equilibrium point, the stability margins and the maximum voltage deviation under CPL disturbances. The ideas presented during the theoretical discussion allow for building a methodology for the voltage control loop design or the selection of the capacitor value

TABLE VII
COMPARATIVE SUMMARY OF DVC AND QVC PERFORMANCE

Characteristic	Method	Indicators
Equilibrium point not affected by P_{L0} (CPL)	QVC	eq. (18), (19)
Equilibrium point not affected by I_{L0} (CCL)	DVC	eq. (18), (19)
Linear behaviour approximation under CPLs	QVC	Fig. 8 & 9
Stability limits not affected by P_{L0} (CPLs)	QVC	Fig. 10
Stability limits not affected by I_{L0} (CCLs)	DVC	Fig. 10
Stability limits affected by G_{L0}	both	Fig. 10
Better disturbance rejection under CPLs	QVC	Fig. 10,12,22,23
Better performance for low capacitance	QVC	Fig. 14 & 16
Higher stable region of operation under CPLs	QVC	Fig. 13,18,17
Better performance under low inner bandwidth	QVC	Fig. 20

considering the dynamic performance. Additionally, the use of the virtual capacitance as a tool for response enhancement, and as a tool to experimentally forecast the effect of resizing the capacitance in existing systems, has been evaluated. The ideas and proposals in the paper has been validated and illustrated through Matlab simulations and experimental results in an experimental rig integrated by Triphase equipment, matching the expected operation predicted by the analytical analysis.

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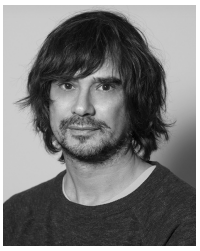

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