POWER FLOW STUDIES OF HVDC GRIDS WITH DC POWER FLOW CONTROLLERS

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ABSTRACT

High-Voltage Direct Current (HVDC) transmission, especially based on voltage source converters (VSCs), have attracted significant research interests due to renewable energy sources integration in power grids, notably offshore wind farms. Despite recent research contributions in the literature on HVDC systems, a number of challenges remain unsolved, such as lack of a comprehensive study regarding power-electronics-based devices in HVDC systems, suitable modelling approaches for sophisticated DC power flow controllers, power loss modeling of DC power flow controllers, powerful and practical DC power flow solvers, and the highly-meshed test structure of HVDC grids for power flow.

To address these research gaps, in this thesis, a comprehensive literature review has been conducted on power electronics devices in HVDC systems in Chapter 2. These devices are divided into three categories in the review: 1) power converters; 2) DC/DC converters; and 3) DC power flow controllers (DCPFCs). As an emerging power electronics device being introduced less than a decade ago, DCPFCs are the main focus of this thesis.

A novel unified Newton-Raphson (NR)-based DC power flow solver (DCPFS) is presented in Chapter 3 to solve the DC power flow problem in multi-terminal HVDC (MT-HVDC) grids by employing a novel DCPFC, the multi-port interline DC power flow controller (MIDCPFC). The proposed DCPFS modifies physical and control state variables of the whole system (MIDCPFC and the MT-HVDC grid) simultaneously to control power flow in HVDC lines, especially overloaded lines. The static model and the power injection model of the MIDCPFC are obtained and their equations are embedded within the designed DCPFS. The absence of the fictitious bus preserves the original conductance matrix of the system and its symmetry, and thus, the original system's Jacobin matrix only needs minor modifications in the developed unified NR-based DCPFS. Additionally, the proposed DCPFS is straightforward for implementation since the voltage of the intermediate capacitor of MIDCPFC is treated as an independent variable, as a result, there is no need to use external processes to control its value. The shunt conductance of HVDC lines is also considered. The comprehensive models have been proposed to model power losses of MIDCPFC and VSCs for the first time. Finally, a new modified 15-bus MT-HVDC grid is proposed and implemented for verification purposes. The obtained results verify the accuracy and efficacy of the proposed concepts, models, and formulations of this study.

A novel sequential NR-based DCPFS is proposed in Chapter 4 to solve the DC power flow problem in MT-HVDC grids by employing MIDCPFC and decoupling the power flow equations of the MIDCPFC and the MT-HVDC grid. In the proposed sequential NR-based DCPFS, there is no trace of fictitious buses, the original conductance matrix of the system and its symmetry are preserved, and the shunt conductance of HVDC lines is considered for precise modeling. The structure of the proposed DCPFS is sequential, which decouples the MIDCPFC and grid related power flow equations. A prominent feature of the DCPFS is that it fully preserves the system's original Jacobin matrix and does not require any modification to that matrix, which reduces the computational burden. In addition, power losses of the MIDCPFC and VSCs are embedded in DC power flow equations. The proposed sequential NR-based DCPFS is straightforward to implement as the voltage of the MIDCPFC is treated as an independent variable, and consequently, no external process is needed to control it. Various scenarios are tested on a modified 15-bus MT-HVDC grid to verify the proposed sequential NR-based DCPFS. The accuracy and efficacy of the proposed approach is validated through these case studies.

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DEDICATION

I dedicate my thesis to my family and my friends. A special feeling of gratitude to my loving parents, Nosratollah Abbasipour (my father) and Parivash Tadbiri (my mother). Without their endless love and encouragement, I would never have been able to complete my graduate studies. This thesis is also dedicated to my wonderful brother, Ali, who was there for me throughout this process and gave me lots of support. I love you all and I appreciate everything that you have done for me. I would like to dedicate my thesis to my lovely fiancée, Negar Afshari, who supported me from a long distance during the hardships of my studies. My lovely Negar, I love you so much.

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1.1. Abbreviation

AC	Alternating Current
CDCPFC	Cascaded DC Power Flow Controller
DC	Direct Current
DCOPF	DC Optimal Power Flow
DCPF	DC Power Flow
DCPFCs	DC Power Flow Controllers
DCPFEs	DC Power Flow Equations
DCPFP	DC Power Flow Problem
DCPFS	DC Power Flow Solver
FACTS	Flexible AC Transmission Systems
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IDCPFC	Interline DC Power Flow Controller
IPFC	Interline Power Flow Controller
ISOP	Input-Series Output-Parallel
LCCs	Line-commutated Current-sourced Converters
MIDCPFC	Multi-port Interline DC Power Flow Controller
MT-HVDC	Multi-Terminal HVDC
NR	Newton-Raphson
OPF	Optimal Power Flow

PF	Power Flow
RESs	Renewable Energy Sources
SDCPFC	Series DC Power Flow Controller
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
UPFC	Unified Power Flow Controller
VSCs	Voltage Source Converters
WPPs	Wind Power Plants

1.2. The History of DC Electricity

The history of DC systems can be dated back to 1882, when Thomas Edison founded the first Direct Current (DC) distribution system in New York City, USA [1]. The DC power transmission system developed by Thomas Edison had the performance issue, incapable of transmitting electrical energy over long distances due to high losses.

In 1886, George Westinghouse used an alternating current (AC) system to transmit electrical energy over a long distance. In this system, transformers were used to increase and decrease the voltage. The use of transformers made it easier to transmit electricity to remote areas. Therefore, this AC system became Edison's biggest competition, not just technically but also economically.

The end of the 19th century was the era of the war between Thomas Edison’s DC system and George Westinghouse’s AC systems. Eventually, the war ended in favor of George Westinghouse’s AC system, and the AC system became the dominant electric power transmission system [2]. There were several advantages to choose an AC system over a DC system at that time because: 1) a AC system was able to transmit electrical energy to remote areas due to adjustable voltage levels; and 2) most loads were AC lamps.

However, DC power are still in use today, such as in telecommunications, hybrid ships and cars, aircraft, electrical traction systems, and high voltage DC transmissions.

1.3. High-Voltage Direct Current Transmission Lines

It was in 1954 that a DC system was reinstated through an industrial project carried out by ABB to provide a High-Voltage Direct Current (HVDC) connection between Gotland and Sweden. Through a 98 km line at 100 kV, 20 MW of electricity was transmitted using HVDC lines in this project [3]. Due to advancement of technology over the years, including significant advances in power electronics and design and manufacturing of DC cables, HVDC lines become a more economical and cost-effective way to transmit electrical power than HVAC systems for long distance transmission.

A HVAC system is less expensive than a HVDC system for underground and submarine applications, and is generally a better choice for short distances under 40 kilometers. However, the HVDC system requires less cable volume than a similar HVAC system, so costs of the cable and its installation are reduced. Other benefits include lower maintenance costs, lower fault rates, simpler towers, shorter cables, asynchronous network connections, no line charging current, fewer cable losses, higher capacity, and a lower environmental impact. When coupled with AC systems, HVDC systems offer significant technical advantages as summarized as follows [4, 5]:

- Line losses in HVDC are lower than that in HVAC.
- HVDC lines enable instantaneous control of the transmitted power, so can be used to control the frequency of AC grids.
- Through a HVDC system, active and reactive power can be controlled independently, and thus, both DC and AC voltages of the converter can be controlled.
- The HVDC system does not increase the short circuit level of AC grids.

1.4. Renewable Energy Sources

With increasing integration of renewable energy sources (such as wind and solar power), a transmission grid is required to link these resources and share their energy effectively. According to geographical locations that utilize these resources, the DC system is the most appropriate method for establishing a connection between them [6].

As an example, we consider wind power plants (WPPs) in HVDC transmission applications. In general, WPPs can be categorized into two major subgroups: offshore and onshore. Compared to

their onshore counterparts, offshore WPPs have a number of significant advantages, including higher and more stable wind speed, and thus, producing higher wind energy. However, due to the fluctuation in wind speed, to ensure reliable, safe and secure transmission of electricity generated by WPPs, WPPs are usually utilized in conjunction with other energy sources, such as the main AC grid, and solar power plants, etc. Using HVDC lines is a viable solution to transmit offshore wind power to load centers. Figure 1.1 illustrates how WPPs are connected to the main grid [6], HVDC lines are shown in green, and HVAC lines are shown in red. In this figure, there are three offshore WPPs (nodes 43-45) connected through HVDC lines to one another and to the main AC onshore grid.

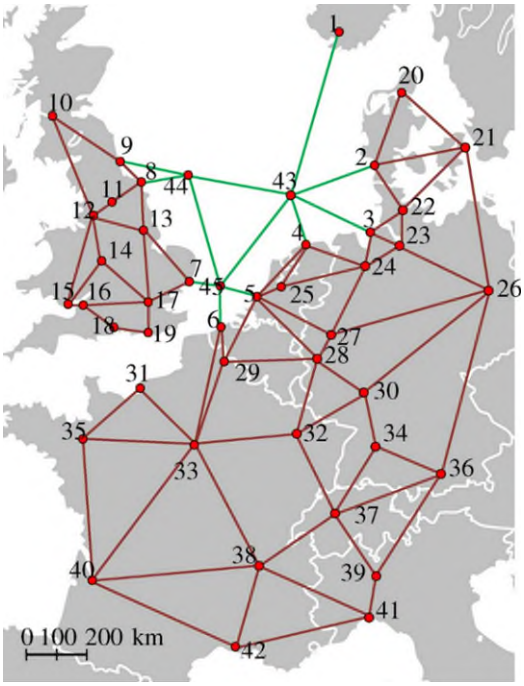

Figure 1.1. Offshore wind power plants connection to the main AC grid [6].

1.5. Multi-Terminal HVDC Grids

A multi-terminal HVDC (MT-HVDC) grid is composed of three or more converter stations that are connected by ground cables or overhead DC cables. During the 1980s, HVDC technology was developed fundamentally based on Line Commutated Converters (LCCs), and the first large MT-HVDC grid was formed in the 1990s. This MT-HVDC grid was the result of expansion of a two-bus HVDC grid to a larger five-bus grid utilized by ABB in 1990 in Quebec, Canada with a capacity of 2000 MW and a rated voltage of 450 kV [7].

There are generally two types of technologies used in HVDC transmission: LCC technology using thyristors and Voltage Source Converter (VSC) technology using insulated-gate bipolar transistors (IGBTs). Configurations of LCC and VSC technologies are illustrated in Figures 1.2, and 1.3, respectively [8].

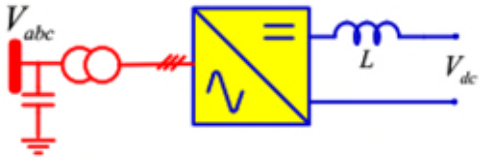

Figure 1.2. The configuration of LCC [1].

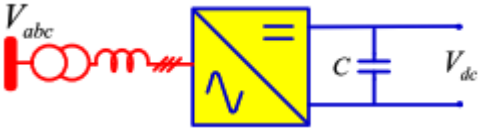

Figure 1.3. The configuration of VSC [1].

With LCC-based HVDC transmission systems, significant effort has been made to increase their connectivity to form a MT-HVDC grid. However, only two-bus systems were used with LCC technology, and a grid with more than two terminals was never built. This is mainly due to difficulty of controlling LCC-based HVDC converters when the number of terminals expands. A fast telecommunication system is also essential to synchronize power flow of converters, detect faults, and restart the system after shutdown. Other limitations of LCC technology include not possible to change power direction without using mechanical keys in such systems, and converters occupying large space, which prevent the creation of a MT-HVDC grid. Following the advancement of VSC technology, MT-HVDC grids were built using VSC technology. Compared to LCC technology, the VSC technology offers lower volume, better reliability, better controllability, no need for a robust grid, independent active and reactive power control, fast-changing power flow direction capability, island operating capability, and power systems stabilization. The following is a summary of comparison between LCC and VSC technologies [1]:

- LCC technology has less power losses (1-2 %) than VSC technology (2-3 %).

- LCC technology operates at AC line frequency (60 or 50 Hz), while VSC HVDC technology operates at the switching frequency (at the kHz level). Therefore, the volume of the filter used in VSC technology is lower than that used in LCC technology.
- LCC converters require reactive power proportional to their firing angle, and thus, it is necessary to use a capacitor bank, Static Var Compensator (SVC), or Static Synchronous Compensator (STATCOM) to supply reactive power. On the other hand, VSC converters are capable of operating in all four quadrants and controlling both active and reactive power. Therefore, VSC technology can enhance the power quality of the grid.
- VSC converters are a better option for forming MT-HVDC grids than LCC converters due to less coordination required.
- LCC technology has a better ability to control DC faults than VSC technology.
- VSC technology requires more sophisticated control structures and other physical circuits than LCC technology.
- LCC technology has a higher rated power than VSC technology. Therefore, LCC technology is a better way of transmitting high power.
- LCC technology requires larger offshore/onshore converter stations than VSC technology. In addition, offshore stations using LCC technology require more maintenance services than those using VSCs.

Due to increasing interests using HVDC lines for renewable energy transmission, such as offshore WPPs, forming MT-HVDC grids is a promising solution. MT-HVDC grids offer several benefits, including creation of DC super grids, linking electricity markets of different countries, power balancing, asynchronous interconnection of various grids, congestion management, providing suitable infrastructure for construction of submarine storage, and providing power supply for equipment required in gas and oil rigs [9-11].

Currently, there are several practical MT-HVDC grids in operation in real life. In Canada, the Hydro-Québec–New England multi-terminal HVDC system project was completed in two phases. Phase one was completed in October 1986, and involved commissioning of two terminals that connected Des Cantons station (located near Sheerbrooke, Québec) to Comerford station (near Monroe, New Hampshire). This phase consisted of a 172 km long line that operated at a bipolar direct voltage of ±450 kV, and had a power transmission capacity of 690 MW for each station. In

phase two, three more converter stations were added to the system. The Radisson converter station (2250 MW) in Québec and the Sandy Pond converter station (2000 MW) in Boston were commissioned in 1990, and the Nicolet converter station (2138 MW) near Montreal was commissioned in 1992. Although Comerford and Des Cantons converter stations were originally intended to be incorporated into this multi-terminal system, the owners ultimately chose not to do so due to the performance concerns. As a result, commercial integration of the two converter stations was suspended [1, 7].

In China, the purpose of Zhang-Bei project was to create a DC grid system that could provide Beijing with a reliable source of electricity from various renewable sources, such as solar, wind and hydro power. The first phase of the project included building four converter stations, with three for sending power (1500MW/±500kV each) and one for receiving power (3000MW/±500kV). This project was completed in 2018 and is considered the largest DC grid project in the world. In the second phase, two more terminals were planned to be built with commissioning in 2021 [7, 11].

Depending on how HVDC lines are connected, MT-HVDC grids can be divided into three major groups: Radial Grids, Ring Grids, and Meshed Grids. Each type of MT-HVDC grids has its own unique advantages and disadvantages. Designing and utilizing lightly and densely meshed MT-HVDC grids will play an increasing important role in integration of renewable energy sources in tomorrow's power grids.

1.6. Challenges of MT-HVDC Grids

Extensive studies have been conducted on HVDC networks and their connection between offshore WPPs and the main AC grid [9, 12-26]. Valuable experience of AC networks can be used to identify challenges of MT-HVDC grids [27]. MT-HVDC grids face significant challenges, which can be summarized as follows [1, 9, 28]:

- System Integration
- Power Flow (PF) Control
- Dynamic Behavior
- Stability
- Protection

- Economic Issues
- Multiple Manufactures

Among these challenges, PF control in HVDC lines is one major challenge, as failure to do so can seriously endanger the system's stability and reliability. This thesis aims to fill in this research gap and tackle this PF control challenge.

1.7. Literature Review

In this section, a literature review is conducted. The first part covers recently proposed devices, DC Power Flow Controllers (DCPFCs), in controlling PF in HVDC systems. The second part covers PF studies, particularly in the presence of DCPFCs.

1.7.1. DC Power Flow Controllers in HVDC Systems

In a meshed MT-HVDC grid, PF control is challenging. DC PF is dependent on the voltage difference between two DC-ends and the resistance of DC lines, so power can pass through different available lines, which may cause either overload or underload conditions. AC systems faced the similar PF challenge, a number of methods were proposed to address it, and one method involved employing flexible AC transmission system (FACTS). During the past decades, various FACTS devices have been proposed, from simple structures, such as SVC and STATCOM, to more complex structures, such as Static Synchronous Series Compensator (SSSC), Interline Power Flow Controller (IPFC), and Unified Power Flow Controller (UPFC).

Inspired by the concept of FACTS in AC grids, a similar concept, namely the Flexible DC Transmission System [29, 30], arose, which led to power electronics-based devices, DCPFCs. DCPFCs are basically DC/DC converters, which are used to facilitate power flow in HVDC systems and resolve the mentioned PF challenge.

DCPFCs can be generally categorized into three major groups: 1) Series DC power flow controllers (SDCPFCs), 2) Cascaded DC power flow controllers (CDCPFCs), and 3) Interline DC power flow controllers (IDCPFCs).

SDCPFCs are connected to a HVDC line in series. They can be DC/DC converters or resistive-based devices. In [30, 31], two resistive-based devices have been introduced for PF control

purposes. Their principal operation is based on entering constant or variable resistance in HVDC lines in series to reduce or control the current flowing through them. These topologies are based on mechanical or semiconductor-based switches and easy to implement. In [22, 32, 33], two DC/DC converters have been developed as DCPFCs. In [33], the proposed topology is based on a single H-bridge, which is connected to the AC side via a two-level VSC. In [22], the proposed topology is based on two parts. The first part is comprised of a series of half bridges, which are connected to the second part by transformers; while the second part is a combination of full bridges that convert outputs of intermediate transformers and inject a suitable DC voltage source into the HVDC line. The topology in [22] is based on DC connection rather than AC connection, which has been used in [33].

A CDCPFC is installed in series with a HVDC line. However, the operation principal of CDCPFCs is completely different from that of SDCPFCs. The CDCPFC is a DC transformer that creates a fictitious bus with a proper voltage level to control the flowing current, and it is based on converting DC voltage with respect to a specified transfer ratio. In [34], a CDCPFC topology and its related control structure are proposed based on a DC/DC converter.

IDCPFCs are the DC version of IPFC devices in AC systems. Their responsibility is to control PF in several HVDC lines. Various topologies consisting of DC/DC converters, transformers, and power electronic elements have been proposed based on concepts of bidirectional/unidirectional, grid-connected, non-grid-connected, master-slave, and independent control and operation. In [35, 36], two similar non-grid connected IDCPFC topologies based on half bridges and master-slave control are proposed. The topology in [36] is unidirectional, and the topology in [35] is bidirectional. In [37, 38], a novel IDCPFC topology is proposed, which is modular and can be extended to control numerous HVDC lines. In [39], an improved IDCPFC is proposed based on bidirectional operation and independent control of the current of HVDC lines. It is based on half bridges and Input-Series Output-Parallel (ISOP) DC/DC converters, and capable of controlling currents of several HVDC lines independently.

1.7.2. Power Flow Studies in HVDC Systems

Evolving point-to-point HVDC transmission systems to mesh MT-HVDC grids provides significant advantages for effective integration of renewable energy sources in terms of flexibility

and reliability. However, one significant challenge of MT-HVDC grids compared to point-to-point HVDC transmission systems is to achieve a proper operating point, which ensures appropriate power flow within the grids. Therefore, DC power flow (DCPF) studies have been conducted for MT-HVDC grids. These studies include: 1) DC Power Flow, and 2) DC Optimal Power Flow (DCOPF), which are mostly done using DC droop control and DCPFC concepts.

DCPF studies involve solving the PF problem to derive a proper operating point, i.e., the voltage of HVDC buses. This can be accomplished by employing appropriate droop control settings and DCPFCs, especially in contingencies. In [40-44], various methods based on a droop control scheme have been proposed to control power sharing and regulate HVDC bus voltages close to their nominal values in MT-HVDC grids. In [45], DC Power Flow Equations (DCPFEs) for SDCPFC are proposed. In the proposed modeling, the inserted dependent voltage of SDCPFC is modeled as a ratio of the voltage of the connected bus, and the proposed algorithm is based on the Newton-Raphson (NR) method. However, the process of adding the static model (SM) of the SDCPFC to general DCPFEs of the system is vague. In [46], DCPFEs of a SDCPFC compensated three-terminal HVDC grid are derived. The proposed DCPFEs are based on a non-conventional approach, which relates the voltage and current of buses and lines to the resistance of lines. Noted, only series resistances are considered in [46]. In conventional approaches, DCPFEs are based on power and voltage of buses. In [47], an IDCPFC is used to solve a DC Power Flow Problem (DCPFP) by deriving DCPFEs based on the relation of the voltage of buses and the current (non-conventional approach), but a specific algorithm was not proposed. In [39], the basic power flow characteristics of an IDCPFC compensated MT-HVDC grid are provided, and the main DCPFEs are derived; the droop control approach is used to ensure stable power flow in the system, but the process of solving DCPFEs is not proposed. In [34], the DCPFP of a CDCPFC compensated MT-HVDC grid is examined; the CDCPFC is modeled as a voltage ratio in the derived DCPFEs. The related Jacobin matrix are derived such that the DCPFC-related equations are decoupled. The proposed structure is based on the NR method. In [48], the DCPFP of MT-HVDC grids in the presence of IDCPFC is solved, an algorithm based on the NR concept is proposed, and the DCPFEs are derived correctly by modeling IDCPFCs as series voltage sources. However, the proposed algorithm does not provide any process to meet the system's constraints, and the shunt admittance of lines has not been considered to reach more precise results. In [49], DCPF and DCOPF problems of a three-terminal HVDC grid are examined in the presence of various structures of SDCPFCs

and IDCPFC, and only general approaches based on the NR concept are discussed. In [22], the DCPFEs of a SDCPFC compensated HVDC grid are derived and solved based on the NR concept. In [50], a PF study is conducted on a DC distribution grid considering a SDCPFC, droop control approach is also considered to model power converters, and the approach is based on the NR concept. However, power losses from power converters or DCPFCs are not considered in [50]. In [51], DCPFEs of a simple HVDC grid in the presence of an IDCPFC are derived based on the mathematical relation of the voltage of buses, current and conductance of the system, which is an unconventional approach to solving PF problems. In [52, 53], PF studies were carried out by considering IDCPFC in MT-HVDC grids. The related PF problem has been solved by employing well-accepted and widely-used NR method by integrating the average model of the IDCPFC in PF equations. Also, general limitations of MT-HVDC grids are considered in solving PF problems by proposing a comprehensive hierarchical solution procedure [53]. In [54, 55], a new method for solving DCPFPs using IDCPFCs is proposed, which reduces the computational burden of the previous method in [52, 53] by treating the voltage of the capacitor of the IDCPFC as an independent variable. However, the proposed structures in [52-55] do not consider power losses of VSCs and IDCPFCs, and the IDCPFC is only capable of controlling one HVDC line actively, which is not practical in highly-meshed future MT-HVDC grids.

A DCOPF study examines PF problems by incorporating a variety of constraints and objective functions to find an optimal operating point at which the operating cost and losses are at their lowest. In HVDC transmission systems, this can be accomplished with a droop control scheme and DCPFCs. In [17, 56-58], droop control-based methods are proposed to achieve optimal power flow in MT-HVDC grids, where various constraints, such as limitations of voltages and currents in MT-HVDC grids, and various objective functions, such as losses and costs minimization, are considered. The principle of droop control-based optimal power flow lies in two hierarchical layers, the first layer is dedicated to solving OPF problem, and the second layer is responsible to derive suitable droop control settings based on results of the first layer. In [23], the DCOPF of a SDCPFC compensated MT-HVDC grid is studied. The main DCPFEs are derived based on the droop control approach applied to some DC buses. However, the reflection of the DCPFC model in the derived DCPFEs is not clear as its effects have been decoupled from the rest of the DC system. In [48, 49, 59], the effect of DCPFCs on reducing operating losses and costs of MT-HVDC grids is investigated on the basis of solving the hybrid AC/DC optimal power flow problem, and

DCPFEs are derived. In [60], the effect of a SDCPFC on OPF of an hybrid AC/DC grid is examined with a simple model of SDCPFC as a series voltage source, where the generic DCPFEs of a flexible MT-HVDC grid are derived, and the derived DCPFEs are used to solve the DCOPF problem. In [61], the effect of SDCPFCs and IDCPFCs on power losses of HVDC grids is examined, and DCPFEs of HVDC grids with SDCPFCs and IDCPFCs are derived. However, DCPFEs are solved through non-numeric methods, and the process of solving them is not discussed in the paper. In [59], the OPF problem of a hybrid AC/DC mesh grid in the presence of a unidirectional IDCPFC is examined, DCPFEs of the system are derived by utilizing the average model of the IDCPFC. In [62], a probabilistic OPF study is conducted in a hybrid AC/DC system with an IDCPFC, and DCPFEs of the DC system with the IDCPFC are derived by modeling the IDCPFC as a series voltage source. In [63], an OPF study is conducted in a hybrid AC/DC system with an IDCPFC, and a NR-based algorithm is proposed to derive the DCPFEs. However, the proposed algorithm does not take into account the system's constraints and shunt admittances.

1.8. Problem Statement

Various power electronics-based devices are used in HVDC systems, including emerging DCPFCs, and they play an increasing important role in proper operations of HVDC transmission. However, based on the above literature review, there are many challenges remain to be solved for PF studies in HVDC systems with DCPFCs.

In existing papers in the literature on DCPFCs to solve DCPFPs, there are three main issues:

1) The devices used are very simple, and cannot handle more complex and highly meshed HVDC system configurations. In the near future, the creation of highly meshed HVDC grids is inevitable due to integration of renewable energy sources, novel and more sophisticated DCPFCs need to be developed.
2) Most studies have been conducted on very simple test grids, simple test grids lead to simple and few numbers of DCPFEs, and the process of solving DCPFEs, especially in the presence of DCPFCs, is not clearly demonstrated.
3) DCPFCs are assumed to be lossless, and loss equations of VSCs in HVDC systems are also rarely considered, leading to unrealistic results.
4) Lack of effective DC power flow solvers (DCPFCs) to solve DCPFPs.

1.9. Thesis Objectives and Structure

To fill in research gaps and solve challenges in emerging DCPFC technology for PF studies in HVDC systems, in this thesis, the following objectives are determined:

1) Perform a comprehensive literature review on power-electronics-based devices facilitating power transmission and power flow in HVDC systems, including emerging DCPFCs.
2) Employ one of the most sophisticated and recently-proposed DCPFCs, the multi-port IDCPFC, to solve DCPFPs.
3) Derive the basic and comprehensive static models, and power injection model (PIM) of MIDCPFC for the first time.
4) Drive loss equations of MIDCPFC and consider loss equations of VSCs and MIDCPFC simultaneously for the first time.
5) Propose two novel NR-based DC power flow solvers (DCPFSs), one is based on unified concept, and another is based on sequential concept.
6) Model power losses of MIDCPFC and VSCs in a comprehensive and conventional style, and embed their equations in the proposed DCPFSs.
7) Propose solution procedures considering practical constraints of MIDCPFC and MT-HVDC grids for solving DCPFPs.
8) Create a new highly meshed 15-bus MT-HVDC grid with 17 HVDC lines to verify the accuracy of the proposed models, DCPFS, derived equations, and proposed/employed concepts.

The thesis includes five chapters:

1) Chapter one introduces HVDC technology, and conducts literature review regarding main technology challenges, particularly on PF studies in HVDC systems with DCPFCs.
2) Chapter two provides a comprehensive literature review on power electronics-based devices in HVDC systems, including emerging DCPFCs.
3) Chapter three proposes a novel unified NR-based DCPFS to solve the DCPFP in MT-HVDC grids by using a novel DCPFC, i.e., MIDCPFC. In this chapter, the SM and PIM of the MIDCPFC are obtained and their equations are embedded within the designed DCPFS without using any fictitious bus, and thus, the original conductance matrix of the

system and its symmetry are preserved, and only minor modifications to the original system's Jacobin matrix are required. The voltage of the intermediate capacitor of MIDCPFC is treated as an independent variable, so controlling its value using the external process is not needed, which makes the proposed DCPFS easy to implement. The comprehensive power loss models have been proposed for MIDCPFC and VSCs for the first time. A solution procedure is proposed to explain step-by-step processes of solving DCPFP of the MT-HVDC grid through the proposed DCPFS. Finally, a new modified 15-bus MT-HVDC grid is proposed and implemented for verification purposes.

4) Chapter four presents a novel sequential NR-based DCPFS by using MIDCPFC and decoupling power flow equations of the MIDCPFC and the MT-HVDC grid. In the proposed sequential NR-based DCPFS, fictitious buses are not used, the original conductance matrix of the system and its symmetry are preserved, and the shunt conductance of HVDC lines is considered for precise modeling. The sequential structure of the proposed DCPFS enables decoupling the MIDCPFC and grid related power flow equations. The system's original Jacobin matrix does not require any modification in the proposed approach. Power losses of the MIDCPFC and VSCs are embedded in DC power flow equations. The proposed sequential NR-based DCPFS is straightforward to implement as the voltage of the MIDCPFC is treated as an independent variable, so no external process is needed to control it. A solution procedure including step-by-step processes of solving DCPFP is proposed. Finally, various scenarios are tested on a modified 15-bus MT-HVDC grid to verify the performance of the proposed sequential NR-based DCPFS.
5) Chapter five provides conclusions and future works.

Note: Chapter two is a book chapter, which has been published in a book entitled “Smart and Power Grid Systems – Design Challenges and Paradigms” by River Publishers in 2022. Chapter three is a journal paper, which has been accepted for publication in IEEE Transactions on Industry Applications on March 13, 2023.

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PERMISSION TO REPRODUCE

Chapter two of the current thesis has already been published in a book entitled “Smart and Power Grid Systems – Design Challenges and Paradigms” by River Publisher in 2022. The related reference to the book chapter is provided as follows:

> M. Abbasipour, X. Liang, and M. Mitolo, “Power Electronics in HVDC Transmission Systems,” in Smart and Power Grid Systems – Design Challenges and Paradigms, River Publishers, 2022.

2. Power Electronics in HVDC Transmission Systems

2.1. Abbreviation

AAMMCs	Alternative Arm Modular Multi-Level Converter
AC	Alternating Current
B2B	Back-To-Back
CDCPFC	Cascaded DC Power Flow Controller
CS	Current Source
CSC	Current Source Converters
CTB	Controlled Transition Bridge
DAB	Dual Active Bridge
DAB-AAMMC	Dual Active Bridge-Alternative Arm Modular Multi-Level Converter
DC	Direct Current
DCCFCs	DC Current Flow Controllers
DCPFCs	DC Power Flow Controllers
EMI	Electromagnetic Interference
FACTS	Flexible AC Transmission Systems
FC	Flying Capacitor
HCTC	Hybrid Cascaded Tow-Level Converters
HCVSCs	Hybrid Current & Voltage Source Converters
HCVSCs	Hybrid Current and Voltage Source Converters
HV	High Voltage
HVDC	High Voltage Direct Current
IDCPFC	Interline DC Power Flow Controller

IPFC	Interline Power Flow Controller
IPOP	Input-Parallel Output-Parallel
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
MCSCs	Modular Current Source Converters
MF	Medium Frequency
MMCs	Modular Multi-Level Converters
MMCSCs	Modular Multi-Level Current Source Converters
MT-HVDC	Multi-Terminal HVDC
NPC	Neutral Point Clamped
P2P	Point-To-Point
PWM	Pulse Width Modulation
RB	Reverse Blocking
RC	Reverse Conducting
RESs	Renewable Energy Sources
R-type	Resistance-Type
SDCPFC	Series DC Power Flow Controller
SHE	Selective Harmonic Elimination
SMs	Sub-Modules
SPPs	Solar Power Plants
SWRT	Single-Wire Earth Return
TAC	Transition Arm Converter
THD	Total Harmonic Distortion
VS	Voltage Source

VSC	Voltage Source Converters
V-type	Voltage-Type
WPPs	Wind Power Plants
ZVS	Zero-Voltage Switching

2.2. Introduction

Direct Current (DC) technology was firstly introduced for power transmission and electrification in the late 1880s and early 1890s by the Thomas Edison's company. Meanwhile, the George Westinghouse's company proposed the Alternating Current (AC) technology. The competition between the technologies was later known as the War of the Currents. Eventually, Westinghouse's AC technology became dominant for the electrification [1]. Advantages of DC and High Voltage Direct Current (HVDC) systems over the AC transmission on certain applications, such as bulk power transmission, asynchronous connection and marine power transmission, attracted attention again in the 1930s. The first commercialized HVDC transmission systems were constructed in the Soviet Union and Sweden in 1951 and 1954, respectively. Since then, several HVDC transmission systems have been installed [2]. Since 2008, many countries have changed their energy policies due to the rapid growth of electricity demand and environmental concerns related to fossil fuel-based power generation. Renewable energy sources (RESs) play nowadays an increasing role in modern power systems. HVDC transmission has gained significant interest in the arena of renewable energy integration [3, 4].

Power electronic converters and inverters are important in HVDC transmission systems. Considerable developments in the design of novel and sophisticated high-voltage and high-power switches have enabled the advancement of power electronics converters and inverters in HVDC applications.

In this chapter, we focus on existing power electronics converters and inverters for HVDC transmission systems. In Section two, HVDC transmission systems are examined. In Sections three through five, power converters, DC/DC converters and DC power flow controllers in HVDC transmission systems are analyzed. A summary is presented in Section six.

2.3. HVDC Transmission Systems

We will start by introducing existing HVDC transmission systems, their configurations, and the importance of power electronics converters.

2.3.1. Brief Overview on HVDC Transmission Technologies

The operation of HVDC transmission systems requires the conversion of AC power to DC power and vice versa. Typically, rectifiers perform the conversion of AC to DC power at generation stations, or at wind power plants (WPPs), solar power plants (SPPs), and hydropower plants. Inverters are used at consumption stations or receiving ends, to convert from DC back to AC. HVDC converting stations can provide both rectification and inversion, enabling bidirectional power flow. Similar to the AC transmission technology, HVDC stations include switchgears, converters, and transformers, which facilitate the AC/DC and DC/AC power conversion and transmission.

Power electronics converters in HVDC transmission systems perform power conversion, harmonic reduction, voltage regulation, fault protection, and reliability enhancement. HVDC transmission technologies include two types of converters: Current Source Converters (CSC) and Voltage Source Converters (VSC).

HVDC transmission systems can also be classified into three major groups: a) Back-to-Back HVDC Transmission Systems; b) Point-to-Point HVDC Transmission Systems; and c) Multi-Terminal HVDC Transmission Systems [3].

2.3.1.1. Back-to-Back HVDC Transmission

In the Back-to-Back (B2B) configuration, no transmission medium (or short of transmission medium) is present between transmitting and receiving ends of a HVDC system (Figure 2.1). B2B systems are primarily used to provide an asynchronous connection between two AC networks with different operating frequencies. An example of B2B connection is the power exchange and energy trade between the U.S. (60 Hz operating frequency) and Mexico (50 Hz operating frequency) [5]. Both CSC-HVDC and VSC-HVDC technologies can be used to provide asynchronous connections.

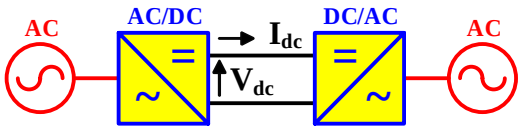


Figure 2.1. The schematic diagram of the Back-to-Back HVDC transmission systems [5].

2.3.1.2. Point-to-Point HVDC Transmission

In the Point-to-Point (P2P) configuration, a transmission medium between transmitting and receiving ends exists (Figure 2.2). HVDC transmission can transfer bulk power to remote load centers. Remarkable examples are the submarine HVDC transmission system in Gotland, Sweden, and the overhead-line HVDC transmission system in Manitoba, Canada.

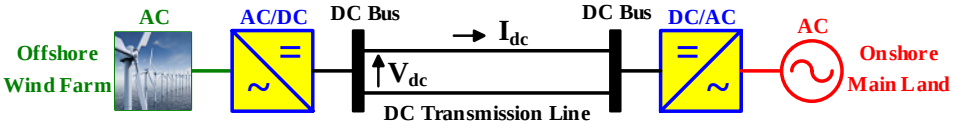


Figure 2.2. The schematic diagram of the Point-to-Point HVDC transmission systems [3].

Most P2P systems are built based on the CSC-HVDC technology, which is more mature than the VSC-HVDC in ultra-bulk power transmission. However, the rapid development of the VSC-HVDC technology may soon allow P2P systems to be built based on both systems [6-8].

2.3.1.3. Multi-Terminal HVDC Grids

Generally, a HVDC grid is composed of at least three HVDC stations (i.e., a three-terminal HVDC grid) (Figure 2.3(a)). Multi-Terminal HVDC (MT-HVDC) grids have been developed with multiple HVDC terminals and lines. MT-HVDC grids offer many advantages, such as the efficient transfer of bulk power across long distances (i.e., mainland overhead lines) and short distances (i.e., marine cables), the connection of various types of RESs, which improves the capability of RESs of meeting the power demand and with lower losses.

An eight-terminal MT-HVDC grid is shown in Figure 2.3(b) [9, 10]. Generally, MT-HVDC grids are classified into three types: a) Radial MT-HVDC grids; b) Ring MT-HVDC grids; and c) Meshed MT-HVDC grids.

Radial MT-HVDC grids are very similar to their AC counterpart, resembling a star configuration with no loops. Radial MT-HVDC grids are relatively simple, and require a low initial investment. HVDC converters are connected to only one HVDC line/cable and only one HVDC line/cable connects the generation HVDC station to a specific mainland HVDC station. Drawbacks of this configuration include a low reliability, since a DC fault can put the HVDC station offline. The schematic diagram of a Radial MT-HVDC grid is shown in Figure 2.4(a).

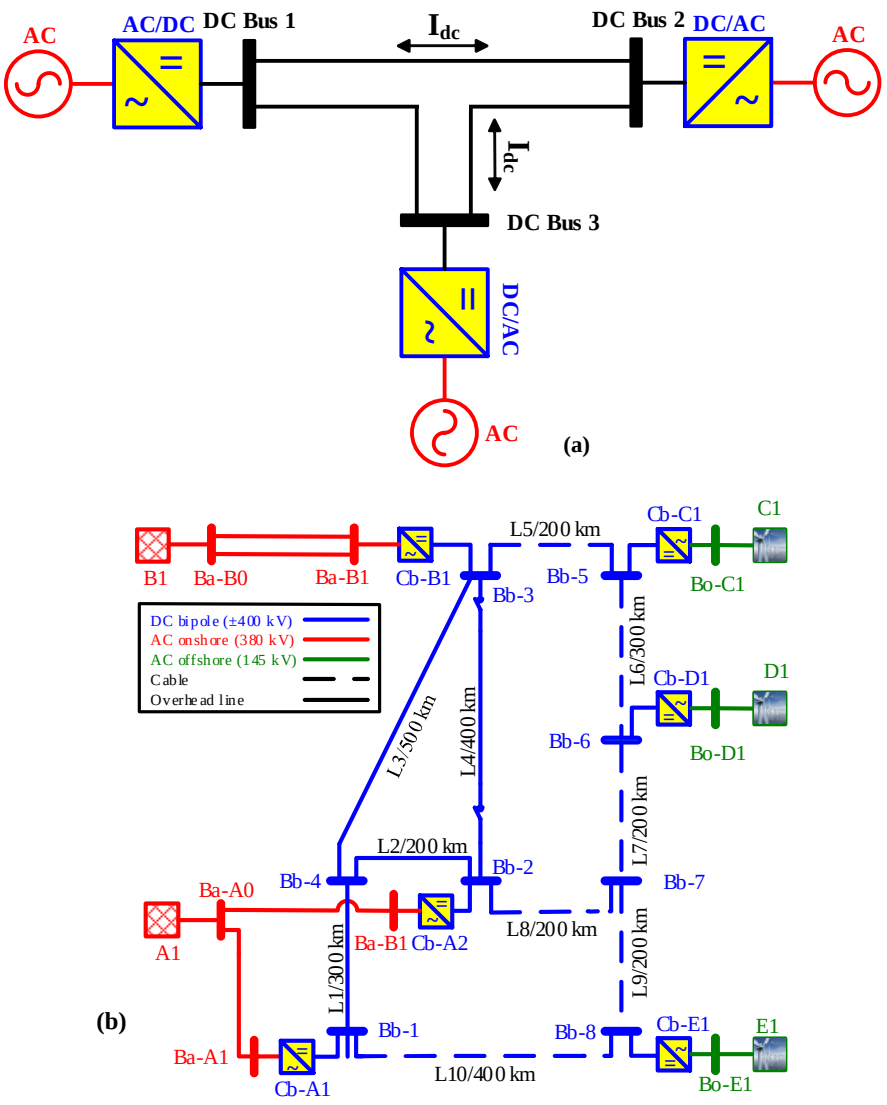


Figure 2.3. Two MT-HVDC grids: a) three-terminal b) eight-terminal [9, 11].

MT-HVDC grids in a Ring configuration also have a simple structure and are similar to their AC counterpart. They resemble a ring with one large loop. In this configuration, all HVDC stations

are connected to two HVDC lines/cables. A DC fault cannot entirely interrupt a HVDC station because of the redundancy offered by the second HVDC line/cable. Thus, the reliability of this configuration is higher than that of the Radial MT-HVDC grid. The schematic diagram of a Ring MT-HVDC grid is shown in Figure 2.4(b).

Meshed MT-HVDC grids are the most complex configuration and are very similar to their AC counterpart. This configuration is a combination of Ring and Radial MT-HVDC grids, with at least one loop, and requires more investment than the other cases. In this arrangement, all HVDC stations are connected to two or more HVDC lines/cables. A DC fault cannot disconnect the HVDC station thanks to the multiple HVDC lines/cables, thus the reliability of this configuration is higher than that of Radial or Ring MT-HVDC grids.

Generally, meshed MT-HVDC grids can be Lightly-Meshed and Densely-Meshed. Lightly-Meshed MT-HVDC grids are simpler, with fewer HVDC lines/cables in their structure, whereas Densely-Meshed MT-HVDC grids feature numerous HVDC lines/cables with several loops in their structure. Densely-Meshed MT-HVDC grids have the highest reliability among all existing MT-HVDC transmission systems. The schematic diagrams of the Lightly- and Densely-Meshed MT-HVDC grids are shown in Figure 2.4(c)-(d).

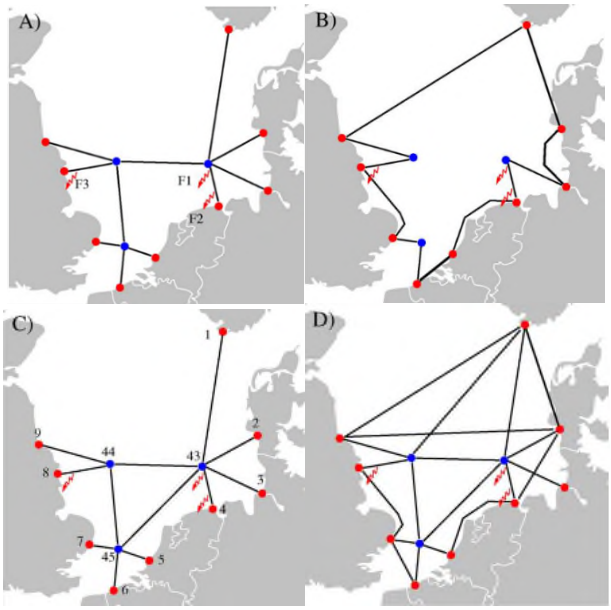


Figure 2.4. The schematic diagram of the MT-HVDC grids: a) Radial MT-HVDC grid; b) Ring MT-HVDC grid; c) Lightly-Meshed MT-HVDC grid; and d) Densely-Meshed MT-HVDC grid [10].

2.3.2. HVDC Configurations

Among various types of HVDC transmission systems, Meshed MT-HVDC grids are expected to play an essential role in tomorrow's power systems. It is anticipated that future Meshed MT-HVDC grids will be based on VSC-HVDC technology, as they can transport power at a constant voltage.

Generally, HVDC transmission systems can be categorized into four major groups based on their electrical circuits and number of poles: a) Monopolar; b) Bipolar; c) Homopolar; and d) Hybrid [12-15].

2.3.2.1. Monopolar

The electrical circuit of a Monopolar HVDC configuration is completed through one or two metallic conductor(s). Generally, Monopolar HVDC configurations can be separated into two subgroups based on the voltage's symmetry and its polarity: a) Asymmetric Monopolar; and b) Symmetric Monopolar [12, 13].

In the Asymmetric Monopolar configuration, one metallic path operates at the system's nominal voltage ($+U_n$), and the return path operates at zero volts (or very low voltage). The term *Monopolar* indicates that one converter is present at each HVDC terminal, and it operates at the system's rated voltage. The term *Asymmetric* indicates that one path operates at the nominal voltage, whereas the operating voltage of the return path is zero: there is no symmetry between the two voltages. In *symmetric* configurations, the voltages of the electrical paths are the same but with opposite polarity.

The operating polarity of the conductor can be either positive or negative; however, it is preferred to assign the negative polarity ($-U_n$) to the conductor to prevent the *Corona* effect. We can have two configurations for the Asymmetric Monopolar arrangement: a) Asymmetric Monopolar configuration with the Earth Return Path; and b) Asymmetric Monopolar configuration with Metallic Return Path [12, 13].

The asymmetric Monopolar configuration with the Earth Return Path is also known as the Monopolar Single-Wire Earth Return (SWER), where just one conductor is used at the system rated voltage ($+U_n$ or $-U_n$), and the return path is the actual earth. Two ground electrodes are

installed at the HVDC station to drive the operating current into the earth. Because the power can only flow in one direction, one HVDC station is the rectifier, and the other one is the inverter. A capacitor is used in both HVDC terminals to maintain the voltage at the desired value. The schematic diagram of the Monopolar SWER configuration is shown in Figure 2.5 [12, 13].

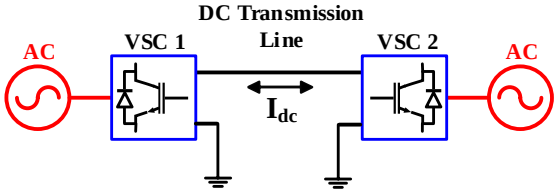


Figure 2.5. The schematic diagram of the Monopolar SWRT Configuration [12, 13].

Asymmetric Monopolar configuration with a Metallic Return Path is concisely named "Asymmetric Monopolar", and unlike the SWER, two metallic conductors are employed. One conductor is used at the system rated voltage ($+U_n$ or $-U_n$), and the other is used as the return path at zero voltage (or close to zero voltage) to complete the circuit. Thanks to the metallic return path, the Asymmetric Monopolar configuration can be used for bidirectional power flow. The schematic diagram of the Asymmetric Monopolar configuration is shown in Figure 2.6(a) [12, 13].

In the Symmetric Monopolar configuration, two conductors operate at half of the system's rated voltage with different polarities ($\pm U_n/2$). The term *Symmetric* indicates that the voltages of the two paths have the same magnitude but opposite polarities. The capacitance is divided into two parts with its midpoint grounded. The schematic diagram of the Symmetric Monopolar configuration is shown in Figure 2.6(b) [12, 13].

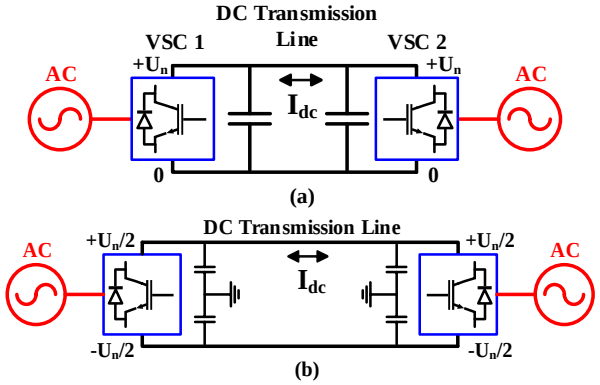


Figure 2.6. The schematic diagram of (a) Asymmetric Monopolar configuration (b) Symmetric Monopolar configuration [12, 13].

2.3.2.2. Bipolar

The Bipolar HVDC transmission is the most popular configuration, which generally employs two conductors to complete the circuit. The term bipolar indicates the presence of two converters in each HVDC terminal. This configuration is basically symmetric, as conductors and converters operate at half of the system rated voltage with opposite polarities ($\pm U_n/2$). Bidirectional power flow is possible due to the two conductors. The schematic diagram of the Bipolar HVDC configuration is shown in Figure 2.7 [12, 13].

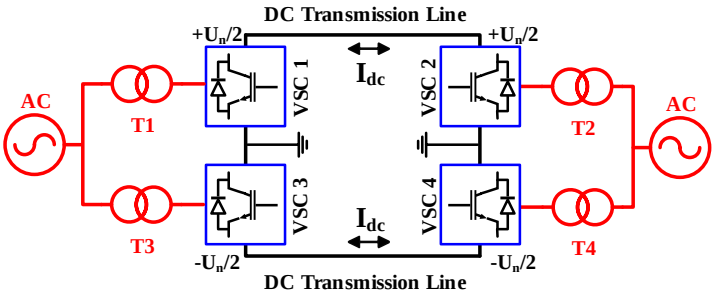


Figure 2.7. Schematic diagram of the Bipolar HVDC configuration [12, 13].

As shown in Figure 2.8, the midpoint between the two converters may be grounded. Therefore, a Bipolar HVDC configuration has the unique capability of being able to operate in the Monopolar SWER mode if one of the converters at HVDC terminals has issues. Power transmission can still be assured at half of its capacity, which is a significant feature.

Several Bipolar configurations are proposed in the literature and two are shown in Figure 2.8 [14].

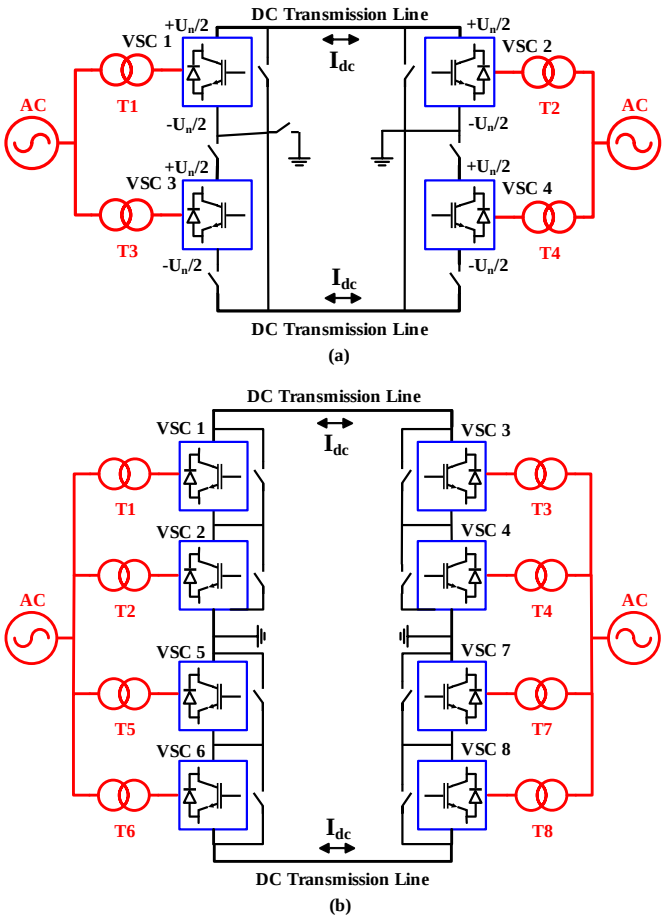


Figure 2.8. Two improved Bipolar HVDC configurations: a) Bipolar configuration with Metallic Return Path b) Bipolar configuration with Series-Connected Converters [14].

The Bipolar configuration with Metallic Return Path in Figure 2.8(a) can operate in the Asymmetric Monopolar configuration during contingencies, such as a fault at each converter, or temporary outages for the converter maintenance. The difference between monopolar operations and the basic Bipolar configuration is the metallic return path, which provides advantages similar to the Asymmetric Monopolar configuration. The Bipolar configuration with Series-Connected Converters of Figure 2.8(b) is another improved arrangement, where each converter can be bypassed during maintenance, without disrupting operations, thanks to the bipolar or monopolar SWER configurations [12-14].

2.3.2.3. Homopolar

The Homopolar HVDC configuration features two conductors with the same voltage magnitude and polarity, and employs the earth as the return path. In this configuration, the conductors'

polarity can be negative or positive ($+U_n$ or $-U_n$), but the negative polarity is preferred as it reduces Corona effects. These features are the main differences between Homopolar and Bipolar HVDC configurations. Since the earth return path is used, the Homopolar HVDC solution can only transfer power unidirectionally. Although this configuration is very similar to the arrangement of the Bipolar, it has similar performance to the Monopolar SWER configuration, as if two Monopolar SWER configurations were merged to create a Homopolar configuration. The schematic diagram of the Homopolar HVDC configuration is shown in Figure 2.9 [15].

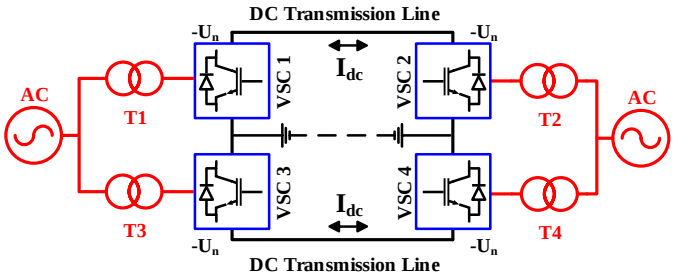
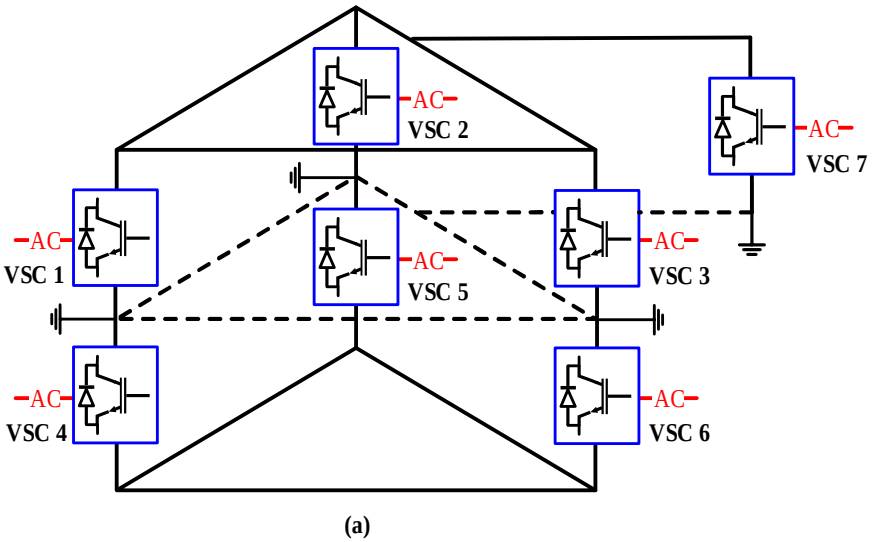


Figure 2.9. Schematic diagram of the Homopolar HVDC configuration [15].

2.3.2.4. Hybrid

The hybrid HVDC configuration is the combination of HVDC configurations. Monopolar, Bipolar, and Homopolar HVDC configurations can be combined to satisfy requirements of HVDC systems. Schematic diagrams of Hybrid HVDC configurations are shown in Figure 2.10 [13].



(a)

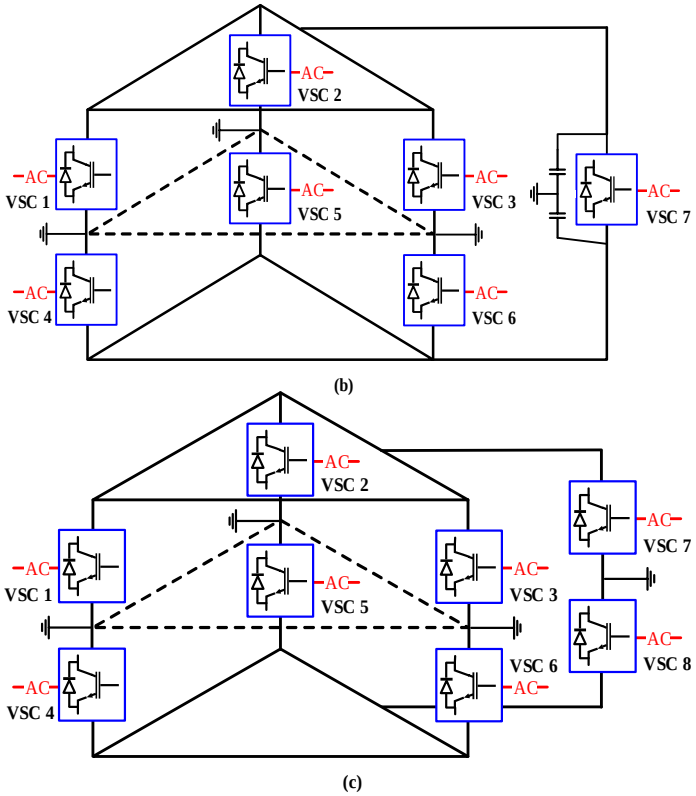


Figure 2.10. Schematic diagrams of Hybrid HVDC configurations: a) Bipolar HVDC with Monopolar SWER; b) Homopolar HVDC with Symmetric Monopolar; and c) Homopolar HVDC with Bipolar HVDC [13].

2.3.3. Power Electronics Converters in HVDC Transmission Systems

HVDC transmission systems include various components, such as DC cables, power conversion units, filters, DC circuit breakers, and control systems, where power electronics converters play a critical role. Recently, HVDC transmission systems received a renewed interest due to renewable energy integration, and thus, experienced rapid developments. New technologies, such as VSC-HVDC, and MT-HVDC grids, and new HVDC configurations, such as Bipolar and Hybrid HVDC, became available. Current research on HVDC transmission includes protection, power flow, harmonics, control, and reliability. Rapid developments in semiconductor materials and switches enable the advancement of new power electronic converters with novel and unique features.

This chapter reviews existing power electronics converters in HVDC transmission systems [16]. Generally, power electronics converters in HVDC transmission systems can be classified into three

major groups based on their structure and duties: a) Power Converters; b) DC/DC Converters; and c) DC Power Flow Controllers.

2.4. Power Converters

The primary duty and purpose of power converters are to convert power from AC to DC and vice versa. Studies have been conducted to develop novel topologies of power converters and improve the performance of existing power converters in HVDC transmission systems. We will first introduce existing AC/DC power converters [12, 17-23].

All AC/DC power converters are generally categorized into three major groups: a) Voltage Source Converters (VSCs); b) Current Source Converters (CSCs); and c) Hybrid Current & Voltage Source Converters (HCVSCs). Each type of these AC/DC power converters can be divided into other subgroups based on their structure (Figure 2.11) [12, 17-23].

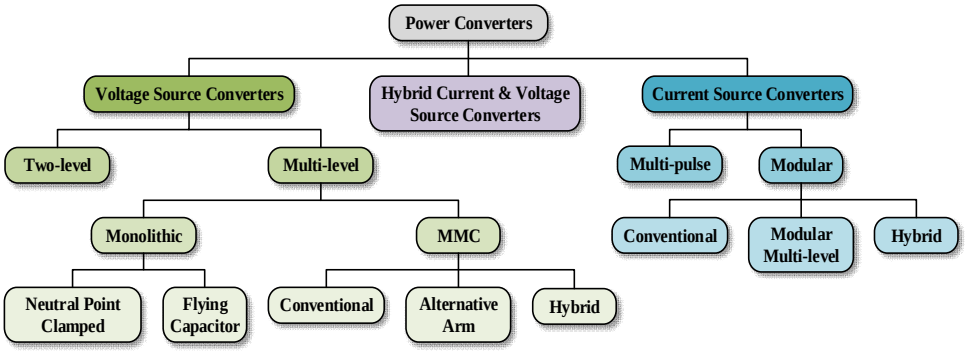


Figure 2.11. General categorization of AC/DC power converters.

2.4.1. Voltage Source Converters

VSCs are AC/DC power converters that maintain their output voltage at a predetermined value, regardless of the magnitude and direction of the current flowing through them. VSCs can be controlled to perform as rectifiers or inverters by controlling the magnitude and phase angle of the AC output voltage (when they are connected to an active DC system). Such control is realized by leading or lagging power reactive generation/consumption in the system. Power reversal can be realized by switches that have the bidirectional current-conducting capability (also known as Reverse Conducting (RC)). The direction of I_{dc} in the system is controlled while V_{dc} is fixed at a

constant polarity. A VSC can be connected to AC systems through a coupling reactance. The general schematic diagram of a back-to-back VSC is shown in Figure 2.12 [19].

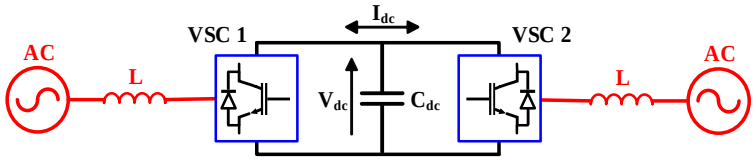


Figure 2.12. The general schematic diagram of a back-to-back VSC [19].

2.4.1.1. Two-level VSCs

The two-level VSCs are the first generation of AC/DC power converters in HVDC transmission systems. This topology has been firstly commercialized by ABB and is known as the "*HVDC Light.*" The schematic diagram and output voltage of a two-level VSC are shown in Figure 2.13 [24].

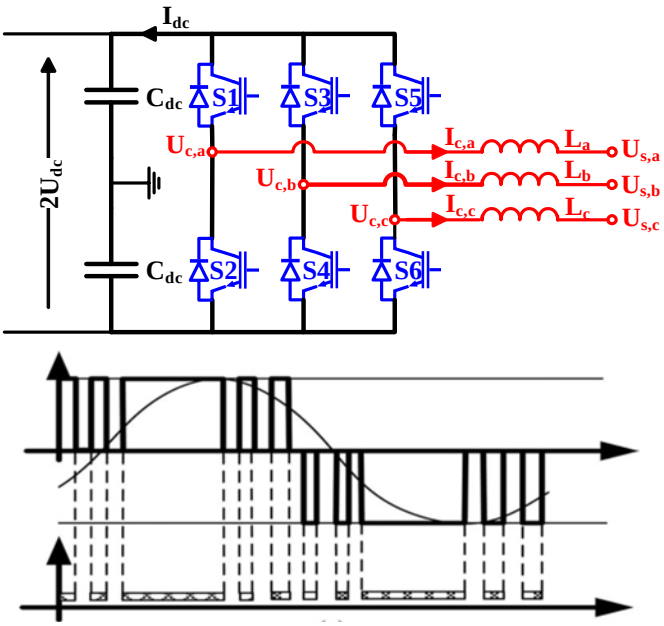


Figure 2.13. Three-phase two-level VSC [19].

This topology is called two-level because it provides two output voltage levels ($+U_{dc}$ and $-U_{dc}$). Only one dc voltage is present, and it is used to generate the reference AC waveform. To generate a suitable AC waveform at the output of the VSC in the inverting mode, the Pulse Width Modulation (PWM) scheme is employed. IGBT switches are commonly used in this topology;

however, their inherent low power losses (about 3% of the total power) is still considered very high. The total harmonic distortion (THD) is also very high, and thus, filters are required. Generally, this topology was exploited in early HVDC transmission systems, and currently is no longer employed [12].

2.4.1.2. Multi-level Converters

Multi-level Converters are the advanced generation of AC/DC power converters in HVDC transmission systems. The output waveform of a multi-level converter is shown in Figure 2.14.

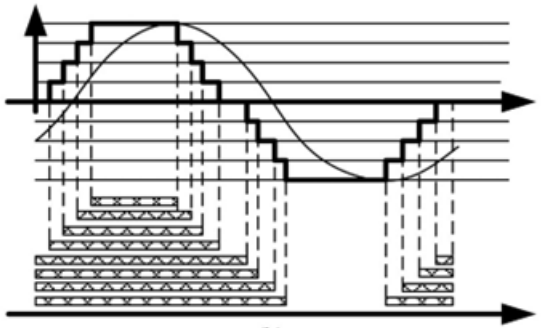


Figure 2.14. Output waveform of a multi-level converter [19].

Multi-level converters produce output voltage waveforms with different voltage levels. As shown in Figure 2.14, multi-level converters have the output waveform very similar to a “staircase”, which is much closer to the sinusoidal AC waveform, when compared to the output of two-level VSCs. Suitable switching schemes can be used to reduce the output THD by eliminating or reducing low-frequency harmonics. This topology requires much smaller filters, which is the significant advantage of multi-level converters over the two-level configuration. Also, the voltage stress (*dv/dt*) is considerably lower than that of two-level VSCs, which significantly reduces the electromagnetic interference in converters. Furthermore, multi-level converters’ switching can be conducted at a lower frequency. Lower switching frequency and voltage stress level are two remarkable factors, which result in a significant reduction in switching power loss. However, multi-level converters have one major drawback: the total energy stored in passive components is significantly higher than that in two-level VSCs for the same rated power. In general, multi-level converters are superior to their two-level counterparts in terms of power quality [12, 17, 19, 20, 23].

Multi-level converters are generally categorized into two major subgroups based on the modularity or solidarity of their structure: a) Monolithic Multi-level Converters; and b) Modular Multi-level Converters (MMCs) [19].

2.4.1.2.1. Monolithic Multi-level Converters

Monolithic Multi-level Converters have no modular or extendible features. Many series-connected switches are employed to withstand the high operating voltage of HVDC transmission systems. Two well-known topologies are present in the monolithic multi-level converter's family: Neutral Point Clamped (NPC) Multi-level Converters and Flying Capacitor (FC) Multi-level Converters [12, 17].

2.4.1.2.1.1. Neutral Point Clamped Multi-Level Converter

NPC Multi-level Converters are also known as Diode Clamped Multi-level Converters. The schematic diagram of the NPC three-level converters is shown in Figure 2.15.

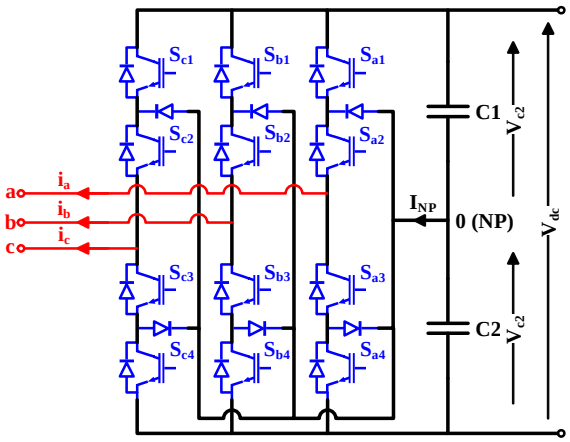


Figure 2.15. Schematic diagram of the NPC three-level converters [12, 17].

NPC multi-level converters generate a multi-level output voltage. The output voltage of an NPC three-level converter may have three magnitudes: $+V_{dc}/2$, *0*, and $-V_{dc}/2$. NPC multi-level converters can be optimally utilized because only a few capacitors are needed with a single DC source. However, maintaining the neutral point voltage at half, or full, voltage of the DC input source may be a challenge. The main advantages and disadvantages of this topology are summarized below [12, 17].

Advantages:

- Only one isolated DC source is required.
- Small harmonic filters may be used to eliminate undesired harmonics.
- Reactive power regulation can be achieved.

Disadvantages:

- More diodes are needed to reach more voltage levels.
- Some switching patterns cannot maintain the capacitor voltage at the desired value, which limits the choice of patterns.
- Additional complex control schemes are needed to balance neutral point voltage in topologies with more than three voltage levels.
- Complex active power control of individual NPC converters is needed due to improper balancing of the capacitor.
- Decreased performance may occur in redundancy applications of HVDC systems.

2.4.1.2.1.2. Flying Capacitor Multi-Level Converter

FC Multi-level Converters are also known as Capacitor Clamped Multi-level Converters. The schematic diagram of this converter is shown in Figure 2.16. This topology is very similar to the NPC multi-level converter, the only difference is that capacitors are clamped at the midpoint of switches to share the voltage. A three-level FC converter can produce a three-level voltage: $+V_{dc}/2$, 0, and $-V_{dc}/2$. The main advantages and disadvantages of this topology are summarized below [12, 17].

Advantages:

- A single DC source is required.
- Active power and reactive power regulation can be achieved.
- No filters are needed for harmonic reduction.
- The THD level is low in high-level FC multi-level converters.

Disadvantages:

- More capacitors are needed to reach more voltage levels, which makes the system bulky.
- More complex control schemes are required for high-level FC multi-level converters.

- Switching losses are high because of the high frequency operations.

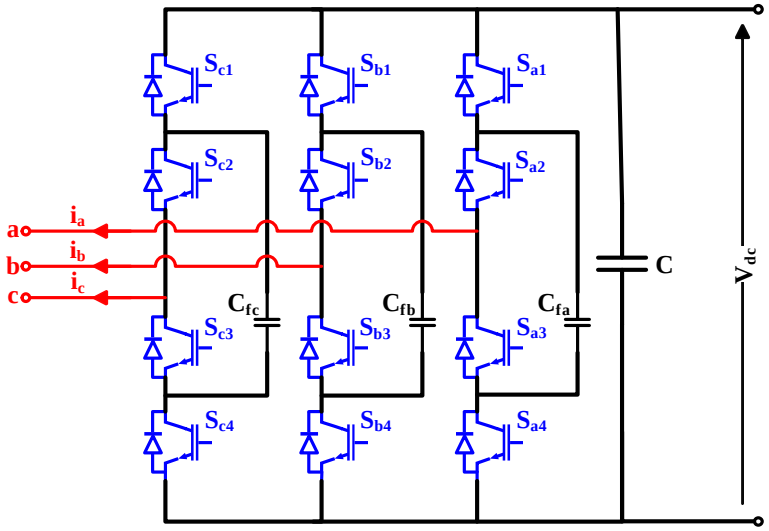


Figure 2.16. Schematic diagram of the FC three-level converters [12, 17].

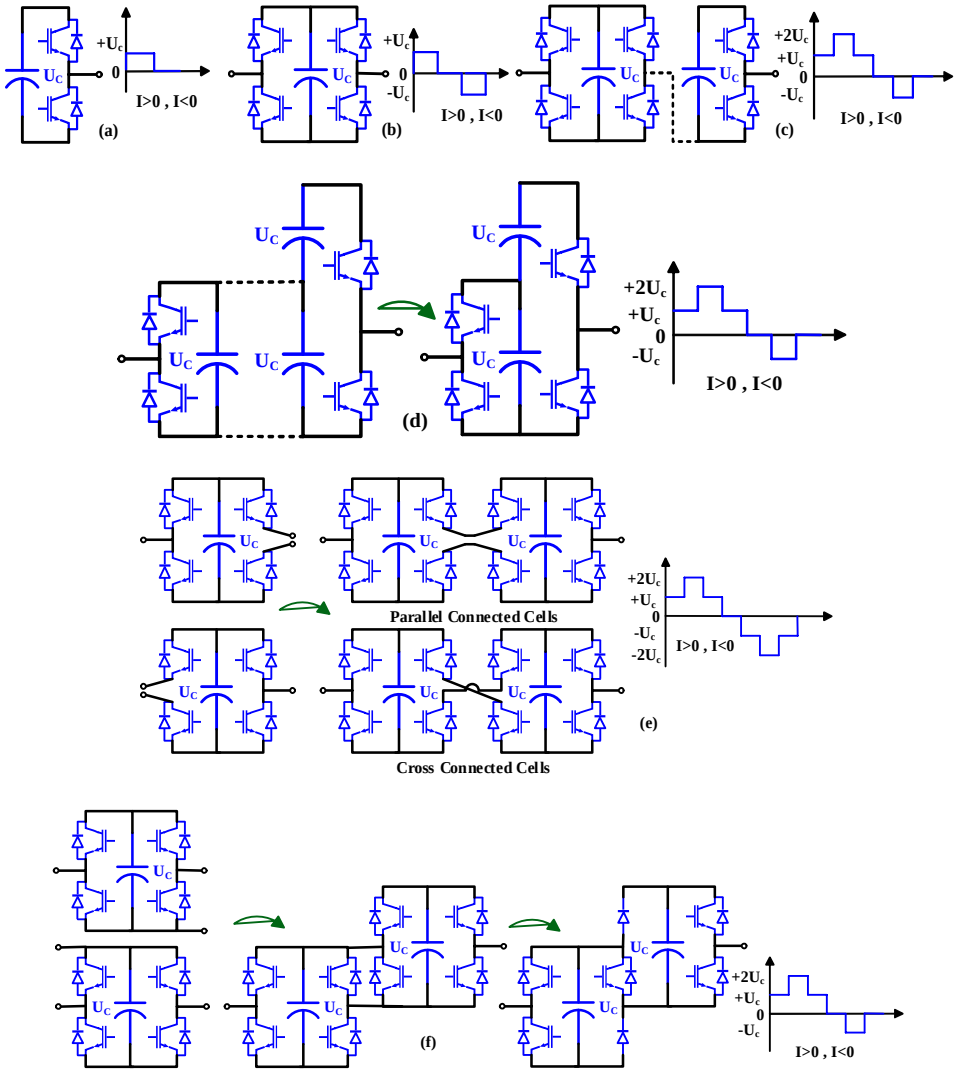
2.4.1.2.2. Modular Multi-level Converters

Monolithic multi-level converters have no modularity features, which complicates their maintenance. Their structure also poses limitations for their use in high-voltage and high-power applications, especially in HVDC transmission systems. In this regard, to improve the performance of the monolithic multi-level converters, the concept of *modularity* has been proposed. Modularity indicates the combination of several subsystems to form a larger system, which, in power converters, is realized through the cascaded connection (the *chain-links*) of several small converter cells. The chain-links of converter cells allow high-voltage and high-power applications of monolithic multi-level converters, with high-quality output waveforms. In this configuration, converter cells and building blocks/sub-modules (SMs) are connected together, forming the intermediate stage of integrated passive elements and power-switching devices. To increase voltage-withstanding and current-conducting capabilities, the sub-modules are connected in series and in parallel.

Monolithic multi-level converters can also be used in Modular Multi-level Converters as: a) chain links of power electronic sub-modules; and b) the combination of sub-modules and monolithic multi-level converters [19, 20].

2.4.1.2.2.1. Power Electronics Voltage Source Sub Modules

Power electronics building blocks are the fundamental bricks of MMCs. The sub-module of an MMC are DC/DC or DC/AC converters, which can be connected in parallel (to increase the current-conducting capability) or in series (to increase the voltage-withstanding capability). The combined series and parallel connections can be used to meet the required specifications in various applications. The popular sub-modules of MMCs, and their related output voltage waveform, are summarized in Figure 2.17. The important features of each sub-module are explained below [19, 20].



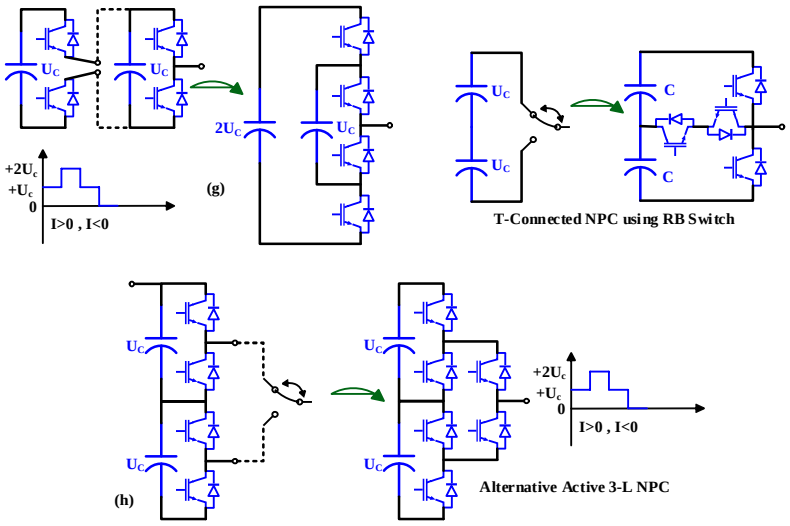


Figure 2.17. Sub-modules of MMCs: a) Half-Bridge; b) Full-Bridge; c) Mixed; d) Asymmetrical; e) Cross-Connected & Parallel; f) Clamped; g) FC-Type; and h) NPC-Type [19].

a) Half-Bridge sub-module: It is the simplest and fundamental sub-module, capable of providing bidirectional current flow and unidirectional voltage blocking. It generates a unipolar output voltage by chopping the DC link voltage. Its output voltage waveform allows the operation in two quadrants by generating a two-level output voltage (U_c and 0) (Figure 2.17(a)) [19].

b) Full-Bridge sub-module: It is implemented by connecting two half-bridges in parallel and operates in four quadrants by generating both positive and negative dc output voltages ($+U_c$, 0, and $-U_c$) (Figure 2.17(b)). Because of the two half-bridges, the number of switches of this sub-module is twice than that of half-bridge sub-modules, but it enables bidirectional current flow [19].

c) Mixed sub-module: It is implemented by connecting the half-bridge and the full-bridge sub-modules. This configuration can offer both bipolar and unipolar benefits. This sub-module produces asymmetric four-level output voltages ($+2U_c$, $+U_c$, 0, and $-U_c$) (Figure 2.17(c)) [19].

d) Asymmetrical Double sub-module: it consists of two half-bridges, similar to the mixed sub-module, and generates asymmetric four-level dc output voltages ($+2U_c$, $+U_c$, 0, and

$-U_c$) (Figure 2.17(d)). This is another alternative for asymmetric four-level sub-modules [19].

e) **Cross-Connected & Parallel sub-modules:** These two building blocks are very similar and obtained by connecting two full-bridges. With a similar performance, they both generate a symmetric bipolar five-level DC output voltage ($+2U_c$, $+U_c$, 0, $-U_c$, and $-2U_c$) (Figure 2.17(e)). There is a structural difference between these two sub-modules: in the cross-connected sub-module, it is possible to generate more voltage levels by cross-connecting more intermediate capacitors; in the parallel sub-module, the parallel connection of the capacitors helps the sub-module reduce voltage ripples in capacitors [19].

f) **Clamped sub-module:** this sub-module consists of two full-bridges, and generates an asymmetric four-level output voltage ($+2U_c$, $+U_c$, 0, and $-U_c$), (Figure 2.17(f)). By employing suitable switching schemes, capacitors can be connected in series or parallel. A precise design and control schemes are required when this sub-module operates in the full-bridge mode, because of the danger of the parallel connection of capacitors with two different voltages. One way to avoid this issue is to replace active switches with diodes (Figure 2.17(f)), but this approach limits the full-bridge mode to a three-quadrant operation [19].

g) **FC-Type sub-module:** This sub-module is based on connecting half-bridges in a nested configuration and generates an asymmetric three-level output DC voltage ($+2U_c$, $+U_c$, and 0) (Figure 2.17(g)). With a three-level voltage, its intermediate capacitor's voltage is half of the DC voltage [19].

h) **NPC-Type sub-module:** This sub-module can be obtained with two different approaches: 1) connecting two half-bridges in series; and 2) connecting switches in a *T-shape*, where the midpoint of the switch package must block both polarities, ("T-connected NPC sub-module"). This sub-module generates an asymmetric three-level output DC voltage ($+2U_c$, $+U_c$, and 0) (Figure 2.17(h)). The switches of the first NPC sub-module block the same voltages, since one of the capacitors is present in each switching process; the upper and lower arm's switches in the T-connection NPC sub-module block the double DC link voltage, as both capacitors are present in the switching process [19].

A comparison among various sub-modules is provided in Table 2.1 in terms of the output voltage levels, voltage blocking level, number of switches, and the complexity level of control and design.

It is usually preferred to design a sub-module following specific technical features, such as high voltage blocking, symmetrical voltage levels, bipolar operation, and the least cost. Other factors, including cell mechanical design, protection schemes (for internal faults), and the control complexity, should also be considered. There is always a trade-off between the cell complexity and its functionality/reliability for an optimal sub-module design [19].

Table 2.1. The comparison of various voltage source sub-modules [19].

Characteristics \ Sub-module Type	a	b	c	d	e	f	g	h
Output Voltage Levels	*2*	*3*	*4*	*4*	*5*	*4*	*3*	*3*
Voltage Blocking Level	*Uc*	*Uc*	*2Uc*	*2Uc*	*2Uc*	*2Uc*	*2Uc*	*2Uc*
No. of Switches (Normalized by Uc)	*2*	*4*	*6*	*6*	*8*	*7*	*4*	*6*
Max no. Switches (for conducting)	*1*	*2*	*3*	*3*	*4*	*3*	*2*	*2*
Bipolar Output Voltage	*No*	*Yes*	*Yes*	*Yes*	*Yes*	*Yes*	*No*	*No*
Design Complexity Level	*Low*	*Low*	*Low*	*High*	*High*	*High*	*High*	*High*
Control Complexity Level	*Low*	*Low*	*Low*	*High*	*Low*	*Low*	*High*	*High*

2.4.1.2.2.2. Conventional MMCs

MMCs are composed of various sub-modules, and the general structure based on chain-links is shown in Figures 3.8 and 3.9; it can be seen that the main structure of MMCs is similar to that of a two-level VSC. There is, however, a remarkable difference: the conventional RC devices in each arm of two-level VSCs are replaced by the chain-links of sub-modules. Thus, the energy storage is distributed in the MMCs' arms [12, 17, 19].

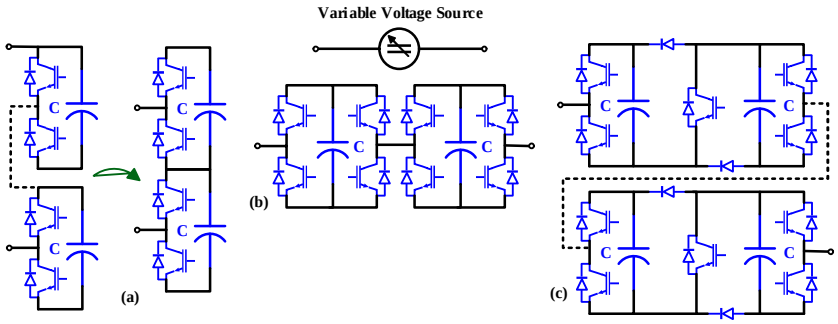


Figure 2.18. The general structure of MMCs [12, 17, 19].

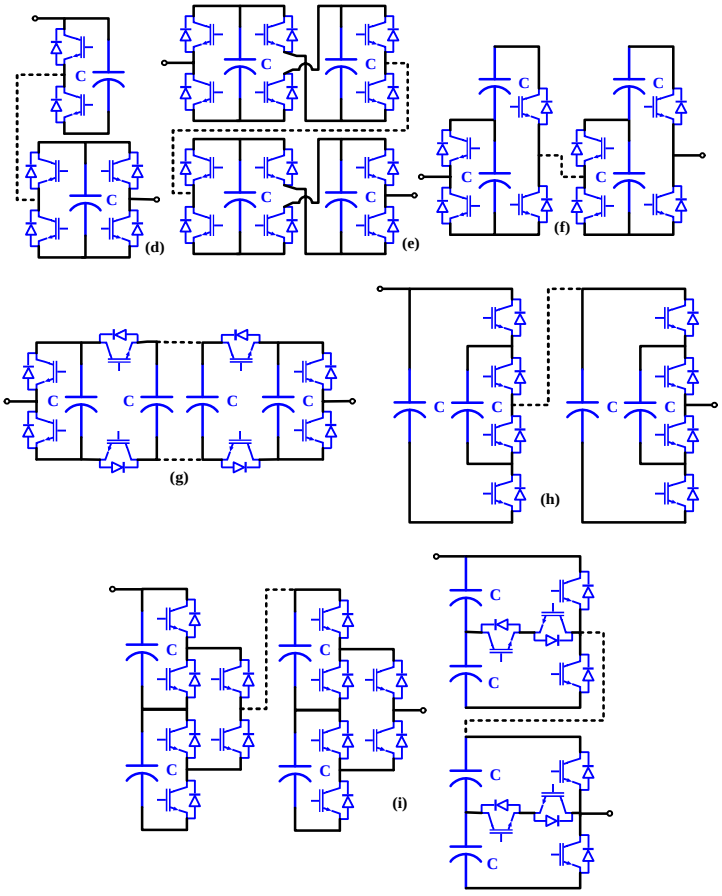


Figure 2.19. Chain-links of power electronics sub-modules: a) Chain-links of Half-Bridges; b) Chain-links of Full-Bridges; c) Chain-links of Double Clamped; d) Chain-links of Mixed; e) Chain-links of Cross-Connected; f) Chain-links of Asymmetrical; g) Chain-links of Stacked FC-Type; h) Chain-links of Series FC-Type; and i) Chain-links of NPC-Type [19].

Advantages:

- A superior performance.
- The dv/dt challenge is eliminated by multilevel steps on the AC side, and consequently, the transformer insulation requirement in high-voltage applications is minimized.
- Fault blocking capability, which suppresses fault currents.
- Low distortion for medium voltage motor drives.
- A compatible structure with economical IGBT switches, with cost reductions.
- The required switching frequency is reduced considerably, because of the high number of sub-modules in each converter's arm.

- Harmonics are reduced significantly, and the filter can be reduced in size or eliminated.

Disadvantages:

- A complex control scheme is required for high level converters.

Most MMCs are based on half-bridge and full-bridge sub-modules. Figure 2.20(a)-(b) shows MMCs based on half-bridge and full-bridge, respectively. Figure 2.20(c) shows the comparison of output currents and voltages between a two-level VSC and a MMC [12, 19].

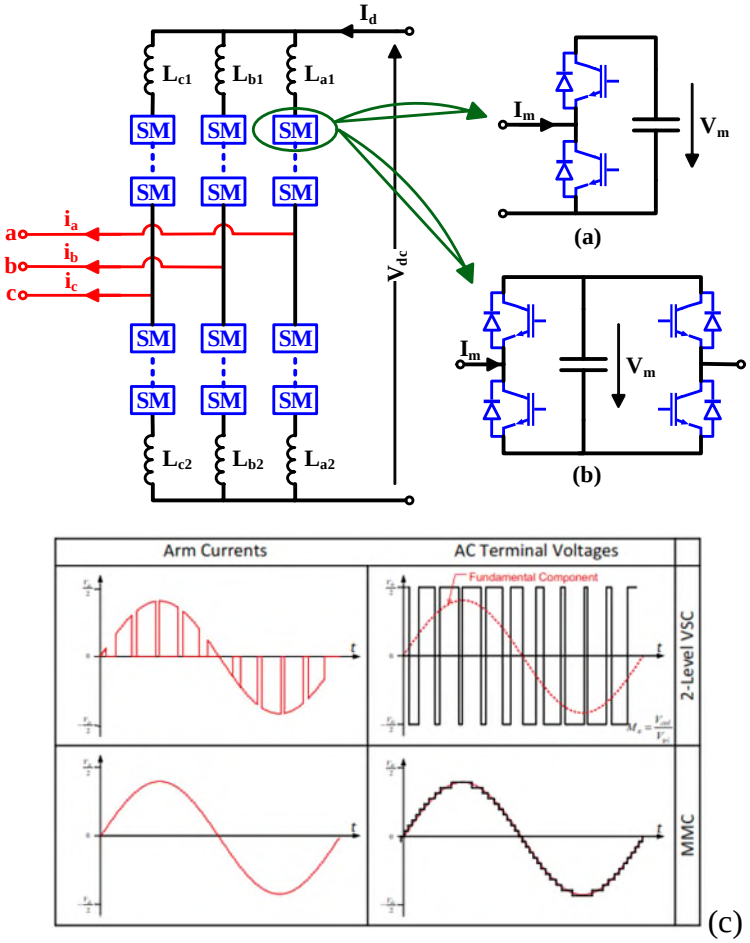


Figure 2.20. Schematic diagram of a complete three-phase MMC based on: a) Half-Bridge sub-modules; b) Full-Bridge sub-modules; and c) Comparison between a two-level VSC and a MMC [12, 19].

Due to the high-power quality at the output, MMCs are considered a promising power converter technology for HVDC transmission systems, considering the potential development of semiconductors and power electronics. However, MMCs have some issues in high and medium

power applications. One critical challenge is the current circulation in their circuitry caused by energy differences in the converter's arms. Protection against internal and external faults is another challenge. Solving these issues is an important research goal [12, 17, 19, 20].

2.4.1.2.2.3. Alternative Arm Modular Multi-Level Converters

The Alternative Arm Modular Multi-level Converter (AAMMCs) is another variant of MMCs, and is designed by changing the sub-module structure or chain-link configuration; its general structure is shown in Figure 2.21 [17, 19].

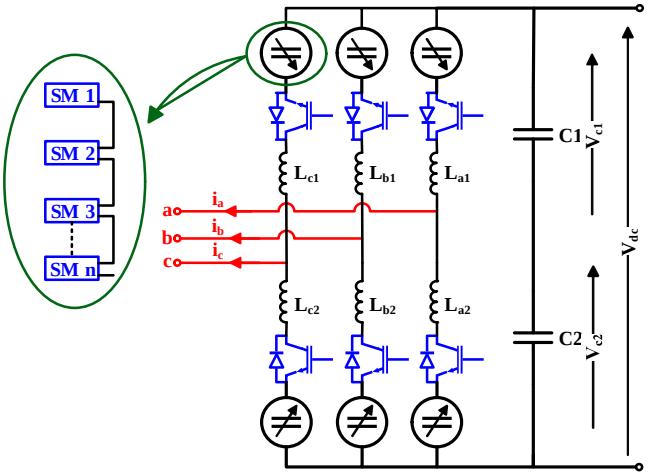


Figure 2.21. The general structure of AAMMCs [17, 19].

The alternative chain-link configuration in AAMMCs provides several interesting features. The capacitors in sub-modules can be used in either polarity in the chain-link configurations of Figure 2.19(b)-(g). This unique feature provides a fault blocking capability for AAMMCs in the case of a short-circuit fault between positive and negative DC terminals. This characteristic offers extra controllability in VSCs in the case of a temporary fault along overhead lines. Bipolar chain-link provides a decoupling between AC and DC voltages, which allows VSCs to be utilized in either polarity, similar to LCC-HVDC systems; thus, they can be employed to connect CSC-HVDC and VSC-HVDC technologies to create a Hybrid-HVDC system [19].

However, these prominent features come with issues, such as a high number of power electronics devices and high-power losses, compared to unipolar configurations. The design of AAMMCs must also consider extra protection, measurement, and cooling equipment for the bipolar sub-modules. The main advantages and disadvantages of AAMMCs are summarized below [17].

Advantages:

- A modular and scalable structure.
- A DC fault capability and management that can omit the need for large AC/DC breakers.
- The need for large AC filters is eliminated, and consequently, the converter size is reduced.
- A sinusoidal AC waveform at the output terminal with negligible harmonic contents or harmonic-free.

Disadvantages:

- A complex control scheme is required for high level converters.
- A higher number of power electronics components than that of other MMC topologies.

2.4.1.2.2.4. Hybrid MMCs

Hybrid MMCs of different topologies are designed by combining chain-link sub-modules and monolithic MMCs, and thus, have advantages and disadvantages of both chain-link sub-modules and monolithic MMCs. The low number of power electronics elements, high level of modularity, and high-power quality are the major advantages of Hybrid MMCs. High-voltage stress and the series connection of devices are major disadvantages. Generally, hybrid MMCs can be designed in two ways: a) Hybrid MMCs with Monolithic Director Switches; and b) Hybrid MMCs with H-bridge Director Switches. The series-connected devices (also known as *director switches*) are responsible for generating output waveforms [19, 20].

Hybrid MMCs with Monolithic Director Switches are designed to connect series-connected chain-link sub-modules to different points (i.e., converter leg, AC side, or DC midpoint) of monolithic two-level converters. The primary purpose of using chain-link sub-modules at the DC or AC side of monolithic MMCs is to mitigate harmonics of the square-shaped output waveforms generated by director switches (monolithic converters). Switching is basically performed according to the *zero-voltage switching* (ZVS) approach, to minimize switching losses and voltage stress. The chain-link sub-modules can generate bipolar multi-level voltage waveforms and produce a near-sinusoidal waveform at the output terminals. Thus, just bipolar chain-link sub-modules can be used (Figure 2.19(b)-(g)). The higher number of sub-modules in chain-links leads to a higher quality of the output voltage. Various topologies of such hybrid MMCs are shown in Figure 2.22 [19].

This type of Hybrid MMCs is expected to reduce the number of sub-modules and power electronics components, as the DC voltage is shared between director switches and chain-link sub-modules. However, the ZVS approach introduces a specific relationship between AC and DC voltages, which is based on maintaining power balance (zero average power) in chain-link sub-modules. This AC and DC voltage correlation affects active and reactive power controls. One way to facilitate the decoupling of AC and DC voltages is to use three-level monolithic FC- and NPC-type director switches. However, this scheme may increase the complexity of the design and the control. Suitable schemes will have to be introduced, which makes this issue an interesting research topic [19].

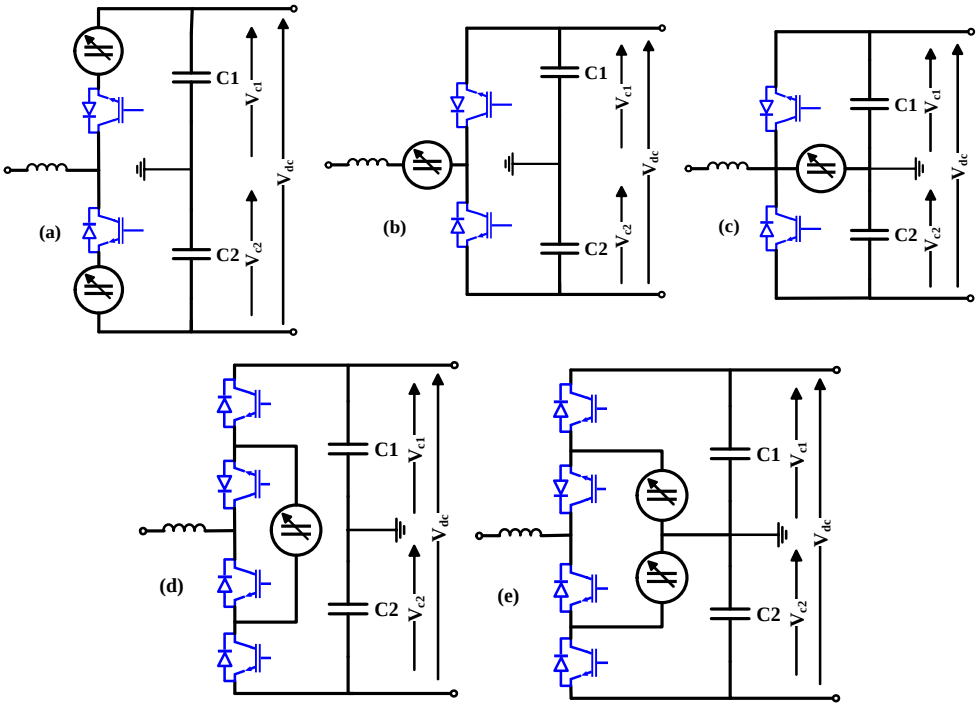


Figure 2.22. Hybrid MMCs with Monolithic Director Switches: a) Hybrid MMC with arm chain-link sub-modules; b) Hybrid two-level with AC-bus chain-link sub-modules; c) Hybrid two-level with midpoint chain-link sub-modules; d) Hybrid three-level FC with midpoint chain-link sub-modules; and e) Hybrid three-level NPC with arm chain-link sub-modules [19].

Hybrid MMCs with H-bridge Director Switches are designed by combining H-bridge or a three-phase monolithic converter with chain-link sub-modules. Its operation principle consists of generating a bipolar multi-level waveform by synthesizing a rectified half-wave multi-level voltage (generated by chain-link sub-modules), and by the polarity adjustment through director

switches (H-bridge or three-phase monolithic converters). The chain-link sub-modules are connected to H-bridge or three-phase monolithic converters in parallel. Also, their switching is performed under the ZVS approach to minimize switching losses and voltage stresses.

The various topologies of this type of Hybrid MMCs are shown in Figure 2.23 [19].

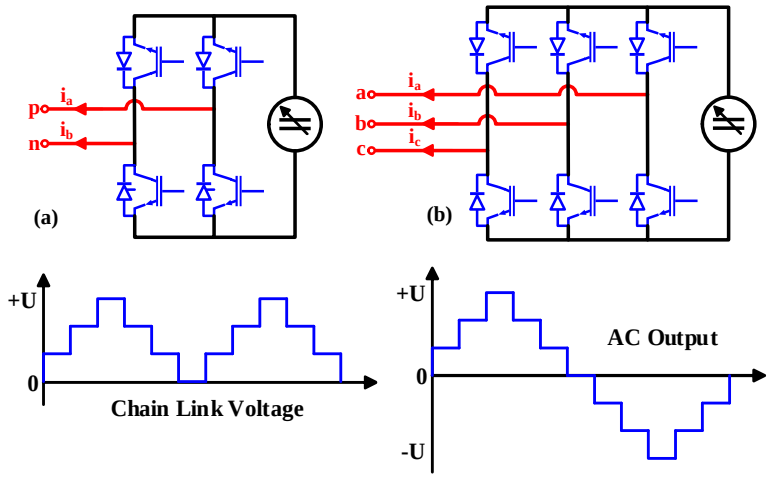


Figure 2.23. Hybrid MMCs with H-bridge Director Switches: a) H-bridge Hybrid MMC with parallel chain-link sub-modules; b) Three-phase Hybrid MMC with parallel chain-link sub-modules [19].

2.4.2. Current Source Converters

CSCs are AC/DC power converters that maintain their output current in their predetermined value, regardless of the polarity and magnitude of the voltage at the poles. CSCs are controlled to act as rectifier or inverter by controlling the magnitude and phase angle of the AC output current. The performance of CSCs relies on large inductors at the DC side. Unlike VSCs, the power reversal is achieved by reversing the voltage polarity in CSCs, and the current can flow in one direction only. Power reversal is realized through existing switches with bidirectional voltage blocking capability (also known as Reverse Blocking (RB)). The polarity of DC link voltage V_{dc} is controlled, but the DC link current I_{dc} is controlled in a fixed direction. Because the AC system has a considerable inductance in its structure, a shunt intermediary capacitor is used at the AC side of the converter. The general schematic diagram of a back-to-back CSC is shown in Figure 2.24. Relevant CSCs, present in Figure 2.11, are examined as follows [19].

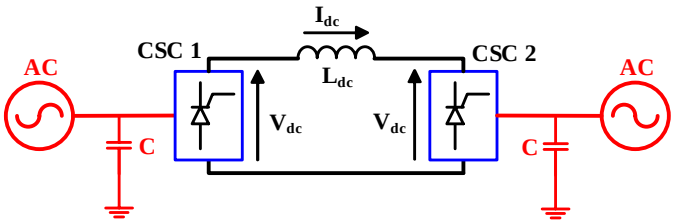


Figure 2.24. General schematic diagram of a back-to-back CSC [19].

2.4.2.1. Multi-pulse CSCs

Multi-pulse CSCs are the first generation and simplest current source AC/DC for power converters in HVDC transmission systems. Mercury-arc valves were firstly used until they became obsolete, then thyristors were used in multi-pulse CSCs as rectifiers/inverters. Basically, six thyristor switches must be used to form the simplest CSC. Other multi-pulse CSCs must be made by using a proper number of thyristor switches, in multiples of six. Accordingly, various topologies, such as 6-, 12-, 18-, and 24-pulse CSCs have been proposed, with 6- and 12-pulse CSCs being the prominent types. The schematic diagrams of 6- and 12-pulse CSCs are shown in Figure 2.25. These topologies are known as multi-pulse because they chop the voltage based on the number of thyristors being used. As shown in Figure 2.25(a), a 6-pulse CSC chops the input voltage into six periods based on the order of switching. The 6-pulse CSC is also known as Graetz bridge, named after Leo Graetz, who firstly proposed a similar structure in the 1890s [12].

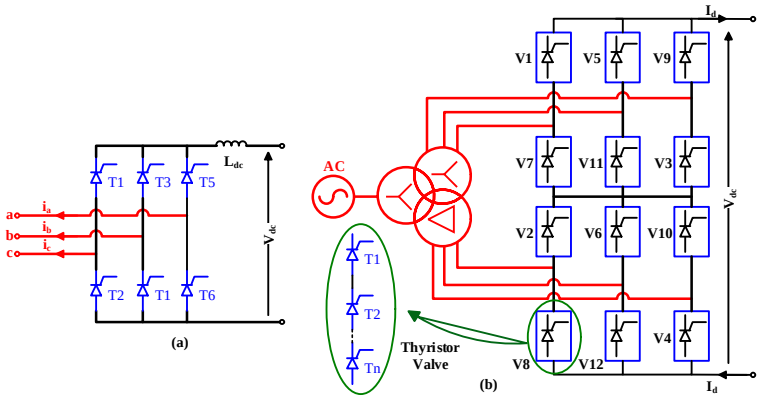


Figure 2.25. Schematic diagram of CSCs: a) Three-phase 6-pulse; and b) Three-phase 12-pulse [12].

Thyristors can withstand voltages in either polarity when they are turned off and keep this condition until they receive a current signal to their gate. They are then turned on and keep this

condition until the current flowing through them drops to zero, or an external circuit imposes a negative voltage at their terminals. These topologies cannot control the voltage at the AC side because it is not possible to turn off thyristors without interfering with the AC voltage, when external circuits are not used. The switching approach is based on firing thyristors, at a suitable angle and forward condition, to conduct the current; the thyristors are then turned off when the current flowing through them drops to zero. In these topologies, it is possible to control the DC side voltage by controlling the DC links at both ends of the HVDC transmission systems. The DC side current is kept at its predetermined value by using large inductors and the appropriate switching approach; the current direction cannot be reversed due to the presence of thyristors, but the power and polarity of the DC side voltage can [12].

2.4.2.2. Modular Current Source Converters

Similar to VSCs, Modular Current Source Converters (MCSCs) can be derived considering the existing duality concept between the VSC and the CSC (i.e., most MCSCs can be designed based on the duality principle in circuit topologies of VSCs). However, the VSC must have a dual topology to be used under the current source approach. The majority of sub-modules and single-phase structures have a dual circuit, but this is not necessarily true for all other three-phase topologies [19].

Multi-pulse CSCs lack in modularity, like the case of monolithic multi-level VSCs, which makes their maintenance difficult. The definition of modularity in the current source approach is the same as the previous definition for the voltage source concept; other concepts, such as chain-link, building blocks, or sub-modules, are also similar. MCSCs consist of chain-links of sub-modules, which can be connected in series or parallel, like in the case of modular VSCs. MCSCs can be designed via a) chain links of power electronics sub-modules, and b) combination of sub-modules and monolithic CSCs.

2.4.2.2.1. Power Electronics Current Source Sub Modules

Power electronics current source sub-modules are the fundamental building blocks of any MCSCs. The sub-module of an MCSC is a DC/DC or DC/AC converter, which can be connected in parallel (to increase the current-conducting capability) or in series (to increase the voltage-withstanding capability). The combined series and parallel connections can be used to meet the specifications

of a variety of applications. The popular sub-modules of MCSCs, and their output current waveforms, are shown in Figure 2.26. The features of each sub-module are explained as follows [19].

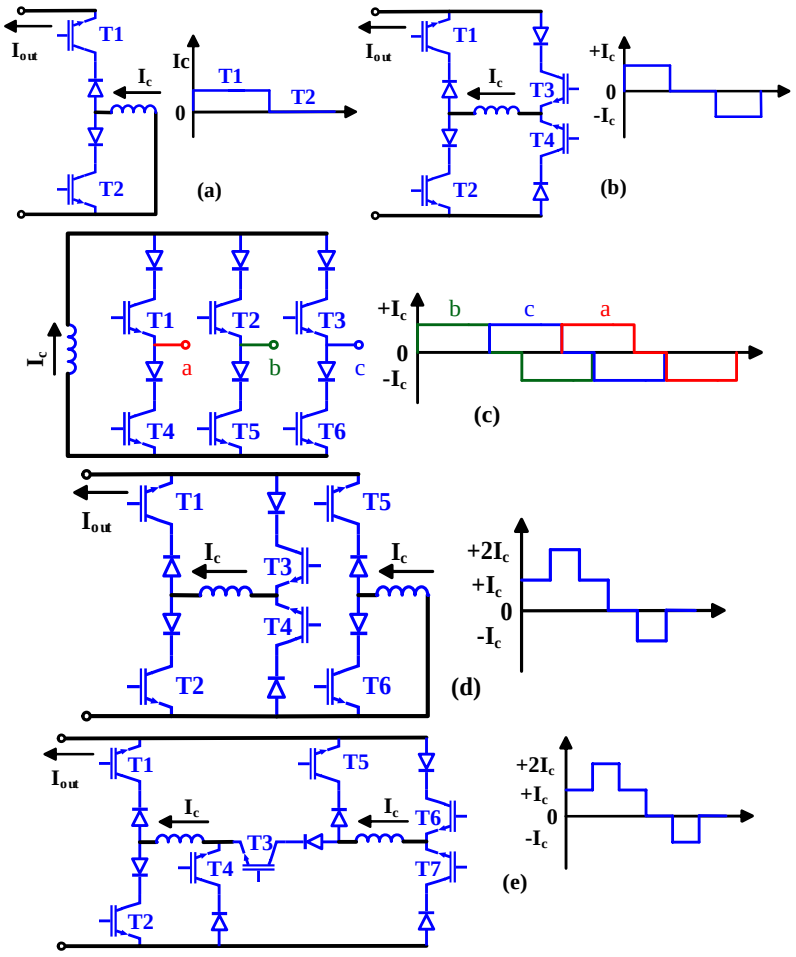


Figure 2.26. Sub-modules of MCSCs: a) Half-Bridge; b) Full-Bridge; c) Three-phase; d) Mixed; and e) Clamped [19].

a) Half-Bridge sub-module: It is the simplest and fundamental sub-module, and has a dual half-bridge sub-module (Figure 2.17(a)). In this sub-module, the switches must be able to block voltage in any polarity and conduct current in one or in two directions (bidirectional). Since the duality concept can be applied, the output current of this current source sub-module is similar to the output voltage of its voltage source sub-module counterpart. The Half-Bridge sub-module generates a unidirectional output current, which operates in two quadrants by generating a two-level output current (I_c and *0*) (Figure 2.26(a)) [19].

b) Full-Bridge sub-module: It is designed by connecting two half-bridges in parallel (Figure 2.17(b)). This sub-module can conduct current in bidirectional paths and can block the voltage of either polarity. It operates in four quadrants and generates three-level output currents ($+I_c$, 0, and $-I_c$) Figure 2.26(b) [19].

c) Three-phase sub-module: This sub-module generates a symmetrical three-level output DC current ($+I_c$, 0, and $-I_c$) (Figure 2.26(c)) [19].

d) Mixed sub-module: This sub-module is designed by connecting half-bridge and full-bridge sub-modules. The output current waveform is an asymmetric four-level current ($+2I_c$, $+I_c$, 0, and $-I_c$) (Figure 3.16(d)) [19].

e) Clamped sub-module: It consists of two full-bridge sub-modules, and its simplified version is shown in Figure 2.26(e). This sub-module is equivalent to two parallel-connected half-bridge sub-modules under a specific switching (T3 off, T4 and T5 on). It is equivalent to a full-bridge sub-module with two series-connected inductors for a different specific switching (T3 on, T4 and T5 off). The presence of two series-connected inductors limits the *di/dt*, providing an interesting feature in the full-bridge mode of operation. Precise design and control schemes are required to prevent possible connection of the two inductors with different currents. This sub-module generates an asymmetrical four-level output current ($+2I_c$, $+I_c$, 0, and $-I_c$) (Figure 2.26(e)) [19].

A comparison among various current source sub-modules, in terms of output current levels, maximum output current, number of switches, and complexity of control and design, is shown in Table 2.2.

Table 2.2. The comparison of various current source sub-modules [19].

Characteristics \ Sub-module Type	a	b	c	d	e
Output Current Levels	*2*	*3*	*3*	*4*	*4*
Max. Output Current	*Ic*	*Ic*	*Ic*	*2Ic*	*2Ic*
No. of RB Switches	*2*	*4*	*6*	*6*	*7*
No. of Switches (for Conducting)	*1*	*2*	*2*	*3*	*4*
Bidirectional Output Current	*No*	*Yes*	*Yes*	*Yes*	*Yes*
Design Complexity Level	*Low*	*Low*	*Low*	*Low*	*High*
Control Complexity Level	*Low*	*Low*	*High*	*Low*	*Low*

2.4.2.2.2. Conventional MCSCs

Conventional MCSCs consist of parallel-connected full-bridge and three-phase current source sub-modules. The reason for the parallel connection is because of the nature of the CSCs. The schematic diagram of the conventional MCSCs is shown in Figure 2.27 [19].

The DC side of each current source cell is connected through inductors and is opened to minimize circulating currents between current source cells. It is possible to switch each current source at the fundamental frequency, providing that a sufficient number of sub-modules are used in the structure. Each valve should be able to withstand a full AC line-to-line voltage. For high-voltage applications, a large number of sub-modules should be connected in series [19].

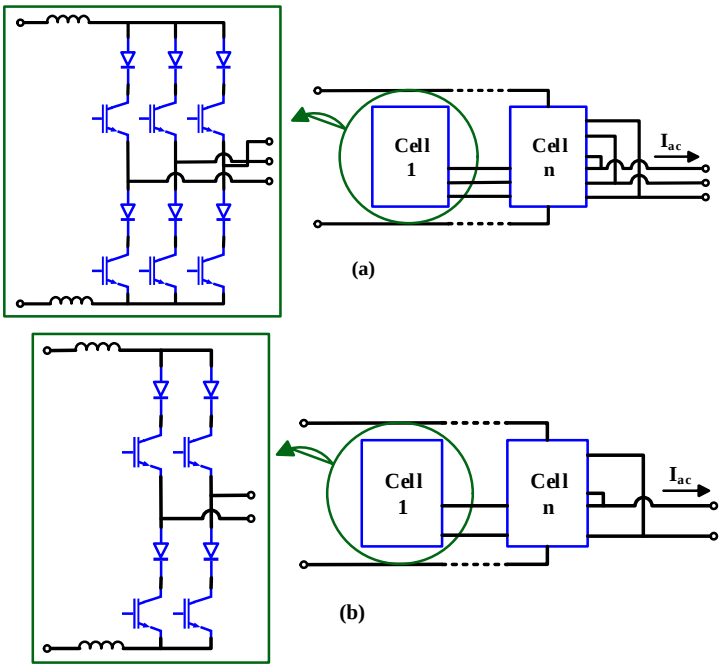


Figure 2.27. Schematic diagram of the conventional MCSCs: a) Three-phase MCSC; and b) Single-phase MCSC [19].

2.4.2.2.3. Modular Multi-level Current Source Converters

Modular Multi-level Current Source Converters (MMCSCs) can be designed by applying the duality concept. The current source arm and single-phase MMCSC can be obtained from their voltage source counterparts. The schematic diagrams of the current source (CS) arm and single-phase MMCSC are shown in Figure 2.28 [19].

In single-phase MMCSCs, the arms are complementary, i.e., the sum of currents flowing through "CS Arm 1" and "CS Arm 3" is constant and are both equal to I_{dc}. The AC output current of this topology is equal to the current difference of "CS Arm 1" and "CS Arm 2." In the case of half-bridge sub-modules, the CS arm must be operated under unidirectional condition, and consequently, the CS arm voltage must be bipolar to realize zero average power.

The duality concept cannot be applied for three-phase MMCSCs, because their voltage source counterpart is not planar. To eliminate this problem, the higher-level circuit topology of the voltage source counterpart can be copied. The schematic diagram of a three-phase MMCSC is shown in Figure 2.29 [19].

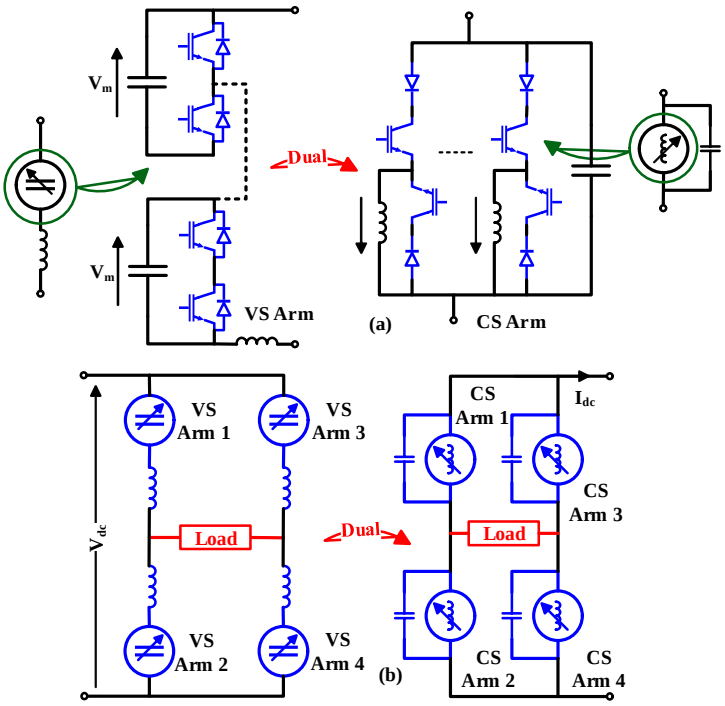


Figure 2.28. The schematic diagram of the MMCSCs: a) CS arm; b) Single-phase MMCSC [19].

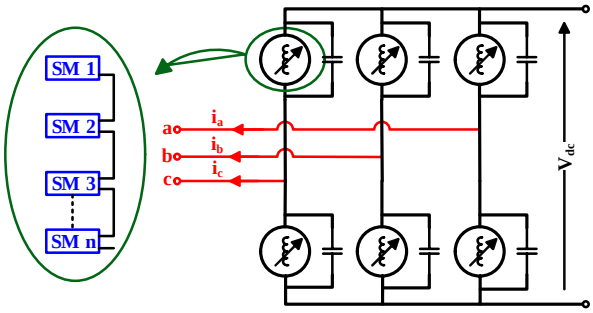


Figure 2.29. The schematic diagram of a three-phase MMCSC [19].

2.4.2.2.4. Hybrid MCSCs

Hybrid MCSCs are designed by combining CS arms and monolithic CSCs. In this configuration, the CS arm is used as a current shaper to modify the output current of monolithic CSCs. Two hybrid MCSCs are shown in Figure 2.30, where the current shaper can only synthesize quadrature and/or harmonic currents, to preserve zero average power in the topology [19].

An alternative design may use CS arms as current shapers at the DC side. The schematic diagrams of two new hybrid MCSCs based on monolithic full-bridge current source sub-module are shown in Figure 2.31. In series-connected CS arm hybrid MCSCs, the CS arm is responsible for synthesizing the rectified current, and the monolithic full-bridge SM CSC is used to invert the rectified current into a sinusoidal AC current. In series-connected CS arm hybrid MCSCs, the CS arm has a different role, including synthesizing the current difference between a rectified current and the phase DC current [19].

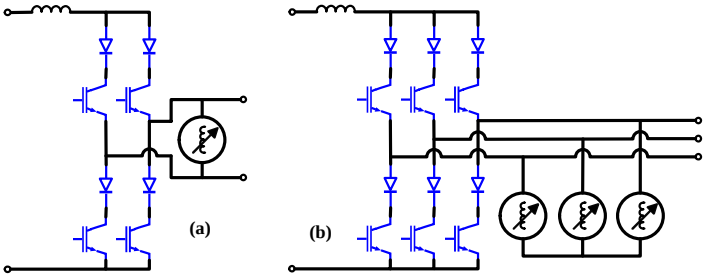


Figure 2.30. Schematic diagrams of two Hybrid MCSCs: a) Single-phase; b) Three-phase [19].

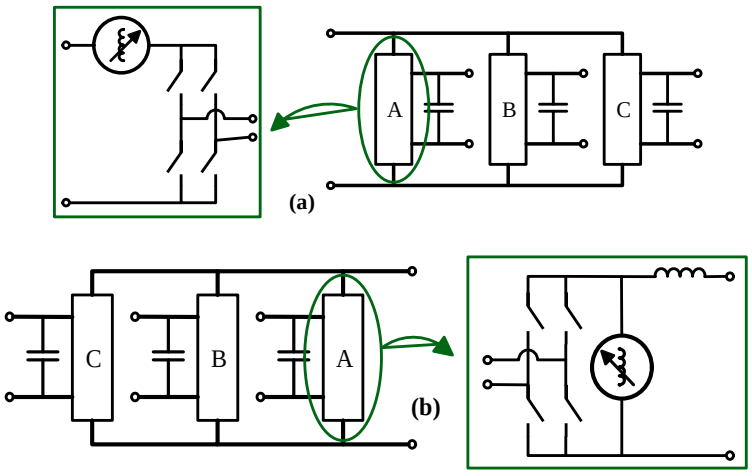


Figure 2.31. Schematic diagrams of two new hybrid MCSCs: a) Series-connected CS arm; b) Parallel-connected CS arm [19].

2.4.3. Hybrid Current and Voltage Source Converters

Hybrid Current and Voltage Source Converters (HCVSCs) combine both current source and voltage source (VS) concepts. Basically, the CS/VS arm can be connected to a VSC/CSC. The general schematic diagram of an HCVSC and its output waveforms are shown in Figure 2.32.

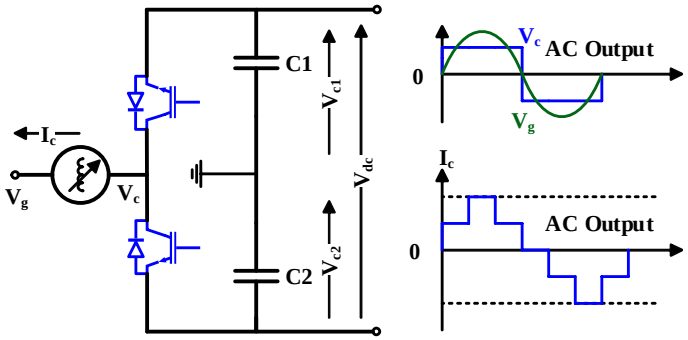


Figure 2.32. The schematic diagram of an HCVSC and its output waveforms [19].

In this configuration, the CS arm is used to synthesize the desired fundamental current, and the two-level VSC is used to maintain a zero average power. To do so, the two-level VSC is responsible for implementing a zero/90° phase displacement between the CS arm's voltage and its current.

HCVSCs can also be constructed by using hybrid CS-VS arms consisting of hybrid CS-VS sub-modules. The schematic diagram of hybrid CS-VS arms and SMs are shown in Figure 2.33. In this topology, the role of the inductor is to synthesize the desired current waveform, and the role of the capacitor is to modify the voltage of CS arms. More studies should be performed on HCVSCs [19].

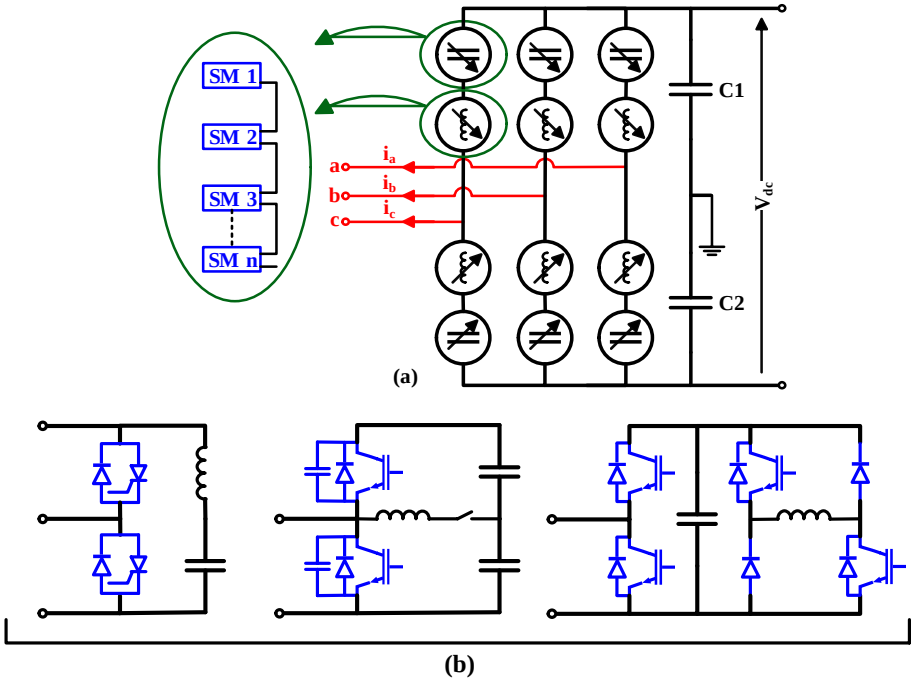


Figure 2.33. Schematic diagram of (a) Hybrid CS-VS arms; (b) Hybrid CS-VS SMs [19].

2.5. DC/DC Converters

DC/DC converters, also known as DC Transformers, provide DC voltage matching. Besides this primary purpose, they can also be used to subdivide large MT-HVDC grids into several smaller protection zones, for DC voltage regulation, fault isolation, and to connect bipolar/monopolar configurations. CSC/VSC technologies have been considered for DC/DC converters. DC/DC converters play a pivotal role in HVDC transmission systems, especially large-meshed MT-HVDC grids. In this regard, various studies are conducted to develop novel practical topologies and improve the performance of existing DC/DC converters in HVDC transmission systems [25-29].

Generally, DC/DC power converters can be designed by considering two major approaches: a) Isolated DC/DC converters; and b) Non-Isolated DC/DC converters. In the Isolated approach, an AC link exists in the heart of DC/DC converters, unlike the case of the Non-Isolated converters, where the AC link is not employed. Each of these two configurations can be divided into subgroups based on their structures. The general categorization of DC/DC converters is shown in Figure 2.34 [25-29].

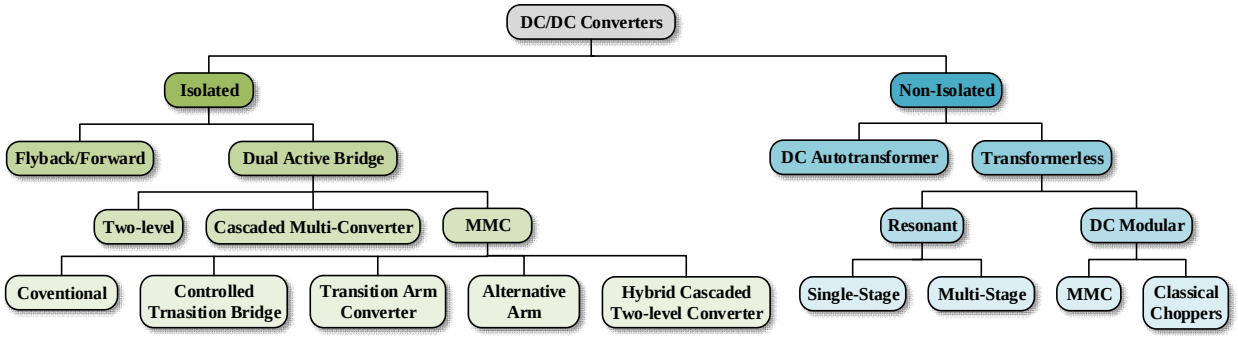


Figure 2.34. General categorization of the DC/DC converters.

2.5.1. Isolated DC/DC Converters

Isolated DC/DC converters belong to a large family, and their performance is based on the DC/AC/DC conversion. To design DC/DC converters, different AC/DC structures and topologies can be used. In isolated DC/DC converters, the galvanic separation is done deliberately by means of an intermediate AC link. A conventional AC transformer or coupled inductors allows the DC fault blocking capability, because the DC fault is a controllable AC overcurrent at the healthy side of the converter. The isolation feature is used to enable different grounding schemes in HVDC transmission systems. Although grounding schemes can be implemented by other means, isolation schemes offer design simplicity and safety assessment [27].

2.5.1.1. Flyback/Forward-based

Generally, the most promising DC/DC converters for HVDC applications are developed under the front-to-front dual active bridge (DAB) concept. Other DC/DC converters that cannot be categorized into the DAB group are based on flyback/forward concepts. In some topologies of this group, a central coupled inductor and MMC-sub-modules are utilized for high-voltage purposes. Other modular structures based on coupled inductors have also been proposed, which are used for high step-up voltage ratios. High insulation requirements in coupled inductors-based DC/DC converters are a considerable challenge, and the high current requirement is a challenge in centralized inductor topologies. These issues have limited flyback/forward-based DC/DC converters in low-power applications. The schematic diagrams of the flyback/forward-based DC/DC converters are shown in Figure 2.35 [27].

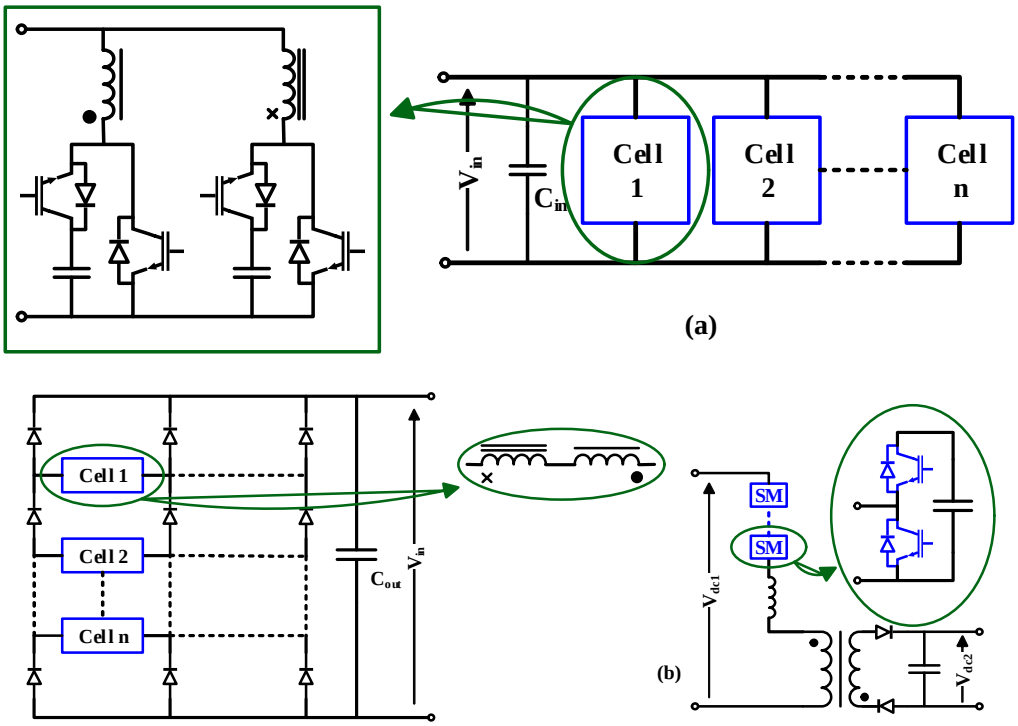


Figure 2.35. Schematic diagram of the flyback/forward-based DC/DC converters: a) Modular topology; and b) Centralized coupled inductor topology [27].

2.5.1.2. Dual Active Bridge (DAB)

Since most DC/DC converters are based on the DAB concept, we herein focus on the most important three subgroups in DAB DC/DC converters, as shown in Figure 2.34.

2.5.1.2.1. Two-level DAB

Two-level DAB DC/DC converters can be built with two two-level VSCs, with series-connected IGBTs connected via an AC transformer. The schematic diagram of the two-level DAB DC/DC converter is shown in Figure 2.36.

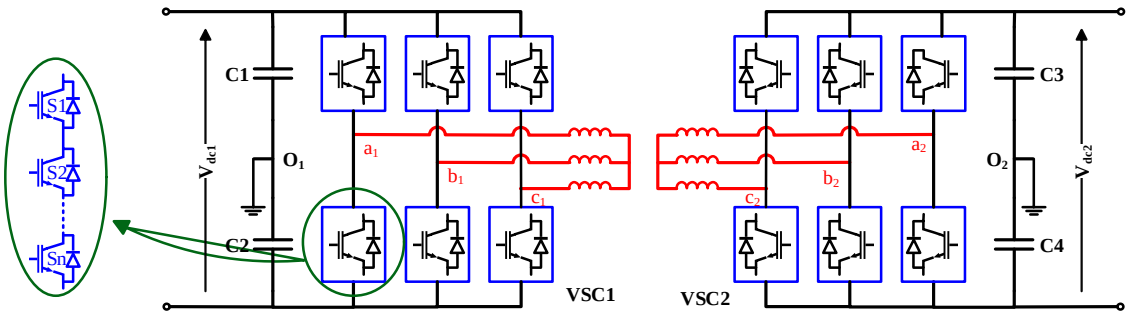


Figure 2.36. Schematic diagram of the two-level DAB DC/DC converter [27, 28].

The operation of this configuration relies on the phase shift modulation at a fixed duty cycle. Typically, this topology operates in the square wave mode at the fundamental frequency, and each arm is used to conduct 180°. Various modulation schemes, such as PWM, may be used in this topology. Selective Harmonic Elimination (SHE) schemes are also employed to eliminate undesired harmonics. The two-level DAB DC/DC converter can be used for power flow control between two VSCs (i.e., VSC1 and VSC2). However, the main issue of this topology is its high *dv/dt* (which limits its application to low power, and voltages up to ±200 kV), insulation issues, electromagnetic interference (EMI), unbalanced static and dynamic voltage sharing on transistor valves, and high switching losses. These issues make this topology not efficient for HV applications [27, 28].

2.5.1.2.2. Cascaded DAB Multi-level Converter

Cascaded DAB Multi-Converter topologies can be designed by using the series/parallel connection of several small DAB converters, which operate as elementary cells. In this topology, there are no series-connected switches since just a portion of the rated voltage should be withstood by small DAB converters. DAB converters can be connected in series or parallel at both input and output terminals, leading to four configurations: 1) Input-Series Output-Series (ISOS); 2) Input-Parallel Output-Series (IPOS); 3) Input-Series Output-Parallel (ISOP); and 4) Input-Parallel Output-Parallel (IPOP). The schematic diagrams of the fourfold cascaded DAB multi-converter as DC/DC converters are shown in Figure 2.37 [27, 28].

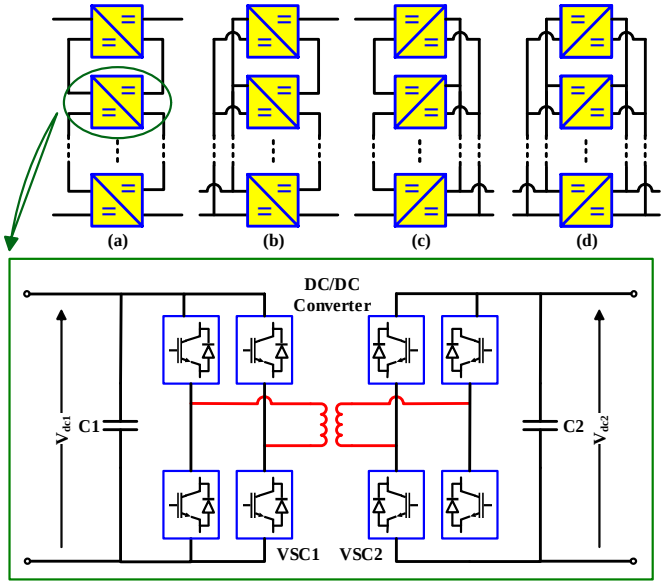


Figure 2.37. Schematic diagrams of the fourfold cascaded DAB multi-converter as the DC/DC converters: a) ISOS; b) IPOS; c) ISOP; and d) IPOP [27].

Generally, the parallel connection is used to increase the current capability, and the series connection is used to increase the voltage capability. Therefore, these fourfold configurations of cascaded DAB multi-converters can be used to meet requirements of HVDC applications. Each DAB converter operates under the conventional standards of DAB converters but with an additional limitation: a balanced distribution of voltages and currents in the cells. It is possible to use this topology in medium frequency (MF, tens of kHz), leading to a considerable reduction in the size and weight of passive elements and the transformer. Soft switching can reduce switching losses, provided that this configuration is properly sized.

The prominent features of this family of DC/DC converters are their scalability and modularity, which allow different operating voltages and power levels. Other variations of this topology (especially IPOS) can be used for high transformation ratio applications. Despite advantages, the main challenge of this family is the high insulation level requirement of the transformer, which limits its application to medium voltage [27].

2.5.1.2.3. DAB-MMC

DAB-MMC is considered an appropriate topology for DC/DC converters for HV topologies. DAB-MMC is designed by connecting two MMCs via a MF transformer, where the AC link uses

the front-to-front concept. The main reason to use the MF AC link is its capability to provide a compact transformer design and reduce the size of passive elements, including cell capacitance and arm inductance. The AC voltage is achieved by sub-modules used in the heart of MMCs. They employ sub-modules that can be of any type, but half-bridge and full-bridge are the most well-known types in this family. Half-bridge can provide unipolar voltages, and full-bridge can generate bipolar voltages at their terminals. The full-bridge converter is the preferred sub-module for DAB-MMC [27, 28].

2.5.1.2.3.1. Conventional DAB-MMC

Conventional DAB-MMCs are DC/DC converters in which conventional MMCs, such as those used as power converters in VSC-HVDC transmission systems, are employed. The MMCs in this family rely on half-bridge and full-bridge sub-modules. The schematic diagram of the conventional DAB-MMC is shown in Figure 2.38 [27, 28].

Various modulation schemes/modes can be used for this topology, but there are two important modes of operation: a) full multi-level modulation with sinusoidal voltages; and b) quasi-two-level mode with trapezoidal voltages. In the first mode of operation, the MMCs use the same modulation employed in power converters, and the distributed cell capacitors are controlled in an appropriate way; this guarantees the complementary operation of the upper and lower arms. The control of the power flow between AC and DC can be accomplished without undesired inrush currents at the DC side. To limit inrush currents caused by existing mismatch between the common-mode voltage and the input DC voltage, the arm inductor is used. In this mode, MMC is used like a VSC, because its upper and lower arms are used simultaneously. AC and DC currents circulates in all arms, whereas the AC current is responsible for transferring active power from the AC side to the converter; the DC current is used to transfer power from the DC/DC converter to the DC side. The major advantages and disadvantages of this mode are summarized as follows [27, 28]:

- Low switching losses compared to its two-level counterpart.
- Low voltage stress (*dv/dt*) compared to its two-level counterpart.
- The full modulation index for AC voltage control is available during DC fault and black start.

- Lower power density is caused by a not full exploitation of the active power due to low-order harmonics.

The second mode of operation was firstly used for diode clamped multi-level inverters, and later was used for MMCs. This mode uses MMCs as a two-level converter, and cell capacitors are used as a clamping package to facilitate the voltage transition at the output terminals. The fundamental current is allowed to flow through MMC cell capacitors during the voltage transition. The required energy storage capacity of cell capacitances, therefore, decreases. In this mode, upper and lower cell capacitors are bypassed when the output voltage is equal to $-V_{dc}/2$ or $+V_{dc}/2$. This feature leads to negligible voltage mismatches among the DC link voltage and the voltage of cell capacitors, and thus, a small inductor is enough to suppress and limit circulating currents. These features make this mode of operation of conventional DAB-MMC a suitable and promising DC/DC converter for MT-HVDC grids [27, 28].

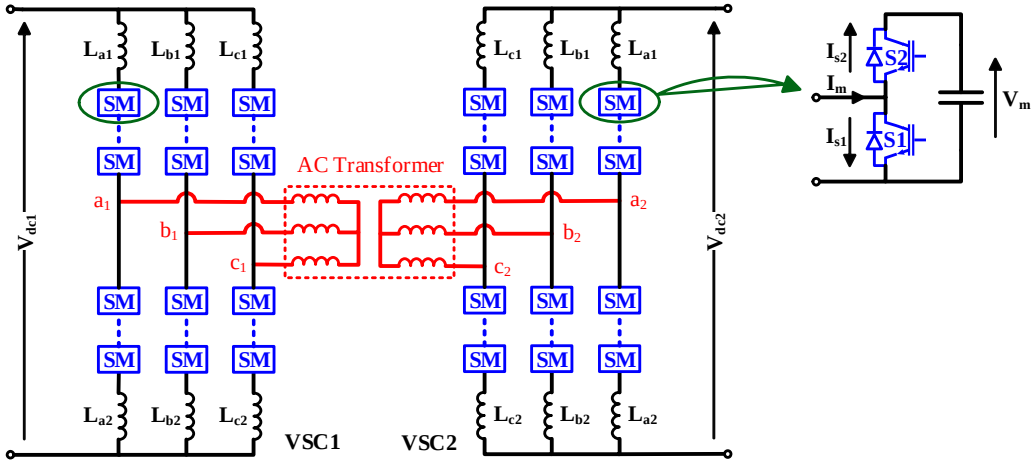


Figure 2.38. Schematic diagram of the conventional DAB-MMC as the DC/DC converter [27, 28].

2.5.1.2.3.2. DAB-MMC based on Controlled Transition Bridge

DAB-MMC using Controlled Transition Bridge (CTB) is a three-phase controlled MMC consisting of full-bridge sub-modules. The schematic diagram of this converter is shown in Figure 2.39 [28].

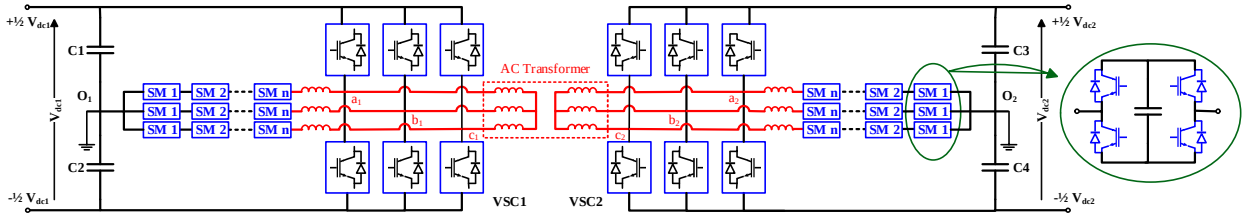


Figure 2.39. Schematic diagram of the DAB-MMC based on CTB [28].

The converter in Figure 2.39 consists of N_1 full-bridge sub-modules in each arm that can generate $2N+1$ voltage levels. The operation of this topology (its main two-level bridge) at the fundamental frequency generates negligible switching losses. The related chain-link withstands just half the voltage ($V_{dc}/2$) of the DC link, and the voltage of each cell capacitor is ($V_{dc}/2)/N$. $2N$ switches cooperate in each arm for current conduction, in a similar fashion as the conventional two-level bridge. Since full-bridge sub-modules are utilized in this topology, the on-state loss is lower than that with half-bridge sub-modules. The performance of the chain-links and the two-level bridge is complementary, and the chain-links provide a suitable transition between positive and negative DC terminals [28].

This topology can be used as a power converter and DC/DC converter. In power converter applications, various modulation schemes can be implemented; while in DC/DC converter applications, the quasi-two-level operation is preferred, because size and weight of the converter are highly important. This quasi-two-level operation mode provides several advantages, such as low semiconductor losses, scalability, modularity, and low *dv/dt*. The main disadvantage of this topology is the discharging of the DC capacitor, which can lead to the high current stress in the event of DC faults. This is not a severe challenge because the intermediary AC link is weak [28].

2.5.1.2.3.3. DAB-MMC based on Transition Arm Converter

DAB-MMC based on Transition Arm Converter (TAC) is basically an MMC in which the typical half-bridge sub-modules are replaced with high voltage (HV) series-connected sub-modules made of IGBTs. The schematic diagram of this topology is shown in Figure 2.40 [28].

This topology features a lower number of semiconductor devices for the DC/DC conversion in MT-HVDC grids. The upper arm is employed as the control and provides a suitable step-level transition between the positive and negative DC terminals during AC conversion; the lower arm

switches are turned on only when the negative DC voltage ($-V_{dc}/2$) must be converted at the AC link. Based on its operation, a common-mode current flows in both arms. Also, the voltage stress (dv/dt) across the switches occurs gradually. This characteristic leads to the elimination of snubber circuits. In addition, the quasi-two-level operation mode can be applied, which makes this topology a promising DC/DC converter [28].

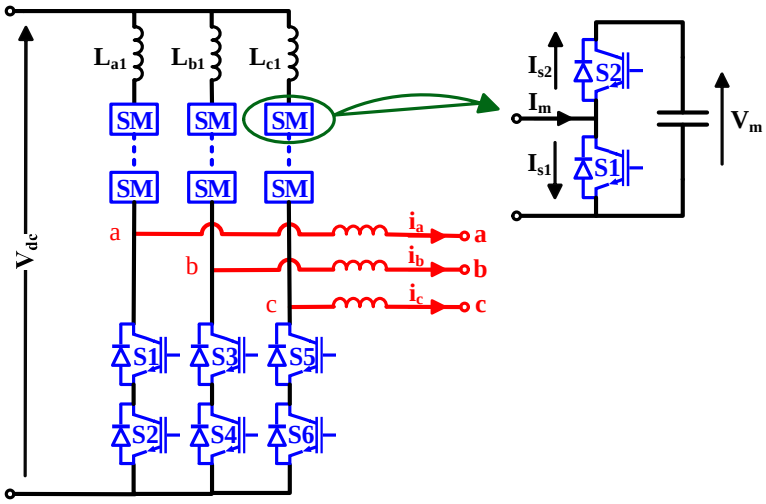


Figure 2.40. The schematic diagram of the DAB-MMC based on TAC [28].

2.5.1.2.3.4. DAB-Alternative Arm MMC

DAB-Alternative Arm MMC (DAB-AAMMC) is designed by using full-bridge sub-module-based MMC, but with two major differences: 1) the number of the full-bridge sub-modules is reduced compared to typical MMCs; and 2) the basic operation of MMCs is modified such that each DAB-AAMMC arm is utilized for 180°, while the director switch ensures full DC link voltage blocking. The schematic diagram of the DAB-AAMMC is shown in Figure 2.41.

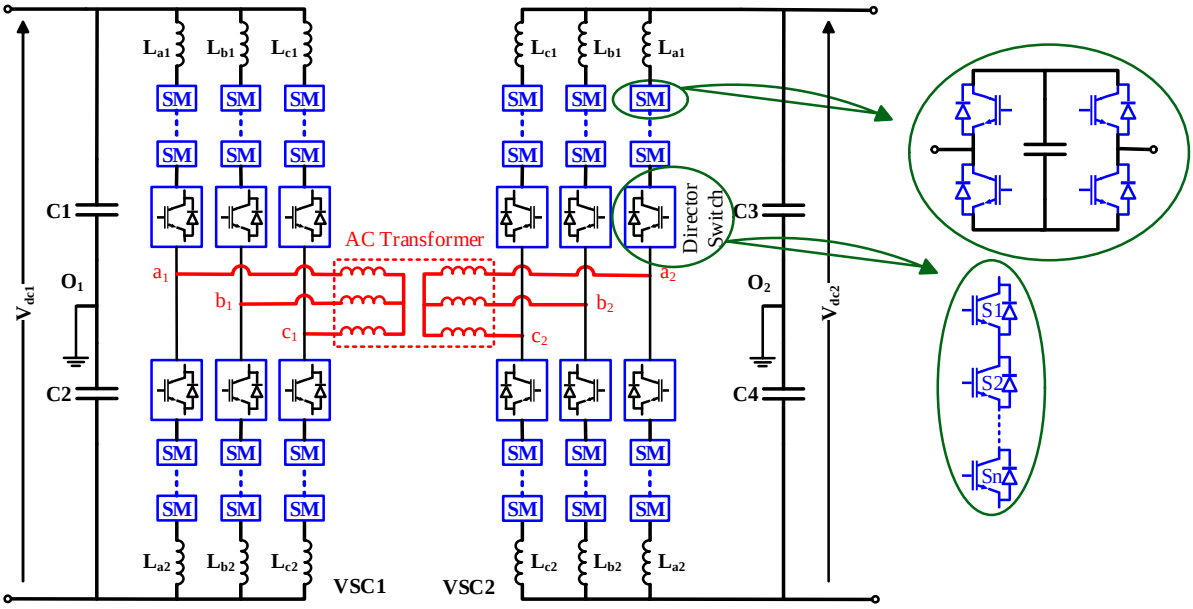


Figure 2.41. Schematic diagram of the DAB-AAMMC [27, 28].

In this topology, a deliberate short time overlap is considered for both upper and lower arms to provide a smooth current commutation for a fault blocking capability. The switch losses are reduced compared to those of a typical full-bridge sub-module-based MMCs and DAB-MMC based on hybrid cascaded two-level converters.

Similar to conventional MMCs, the quasi-two-level operation mode is applicable for this topology. This operation mode can reduce the cell capacitor's size and arm inductors. This operation mode of DAB-AAMMC makes it a suitable choice for HV DC/DC conversion applications. However, this topology has a low efficiency if compared to that of the half-bridge sub-module-based MMC operated in quasi-two-level mode. In addition, the concentrated DC link capacitor can increase the transient peak of DC fault currents [27, 28].

2.5.1.2.3.5. DAB-MMC based on Hybrid Cascaded Two-level Converter

DAB-MMC based on Hybrid Cascaded Tow-level Converters (HCTC) is a DC/DC converter with a similar structure to DAB-MMC based on CTB. The schematic diagram of the DAB-MMC based on HCTC is shown in Figure 2.42.

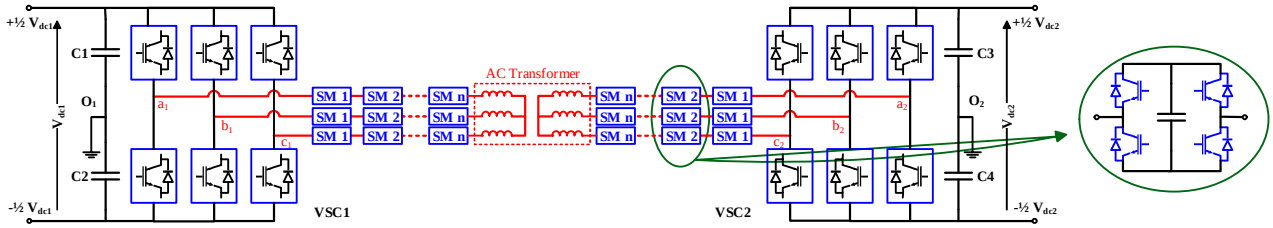


Figure 2.42. Schematic diagram of the DAB-MMC based on HCTC [27, 28].

This topology has a significant advantage over its CTB counterpart, which is the reverse fault blocking capability, with the same number of sub-modules and capacitor cells. However, there are some disadvantages that make this topology inadequate for HV DC/DC conversion applications. In its structure, more switches (*4N*) are used compared to the CTB counterpart (*2N*), because full-bridge sub-modules are used. Therefore, this topology has more power losses, even in quasi-two-level operation mode. Similar to CTB and AAMMC counterparts, its DC link capacitor can increase the current stress during DC side faults [27, 28].

2.5.2. Non-Isolated DC/DC Converters

Non-Isolated converters are another family of DC/DC converters, which is larger than the Isolated counterpart. This family can be classified into two major subgroups based on the presence/absence of the transformer: 1) DC Autotransformer; and 2) Transformerless DC/DC converters [27].

2.5.2.1. DC Autotransformer

DC (or HVDC) Autotransformer consists of two HV DC/AC converters based on DC/AC/DC conversion, and their performance is similar to that of its Isolated counterpart. The schematic diagram of the DC Autotransformer is shown in Figure 2.43, where DC and AC sides of two DC/AC converters are connected in series. The DC side is connected directly, but the AC side is connected via an AC transformer. This topology is different from the DAB family previously discussed because a portion of the power is conducted through the AC link, which leads to lower power losses and transformer rating. Series connections lead to a reduction in voltage ratings of each DC/AC converter. They are compatible with VSCs (such as two-level, three-level, and MMCs), HCVSCs, or VSC-based diode rectifiers. However, this family is more suitable for low or medium transformation ratios [27].

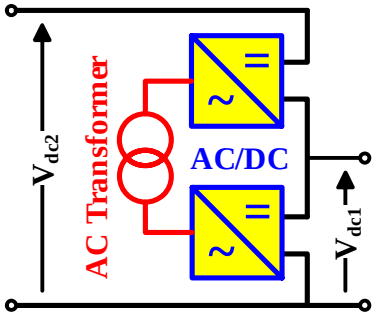


Figure 2.43. Schematic diagram of the DC Autotransformer [27].

2.5.2.2. Transformerless

Transformerless DC/DC converters do not have transformers in their structure, and they will be discussed below.

2.5.2.2.1. Resonant DC/DC Converters

Resonant DC/DC converters are made of LC tanks. Their performance is based on the resonance of inductances and capacitances as a practical means for stepping up the DC voltage, while preserving the soft-switching scheme. The schematic diagram of the resonant DC/DC converters is shown in Figure 2.44.

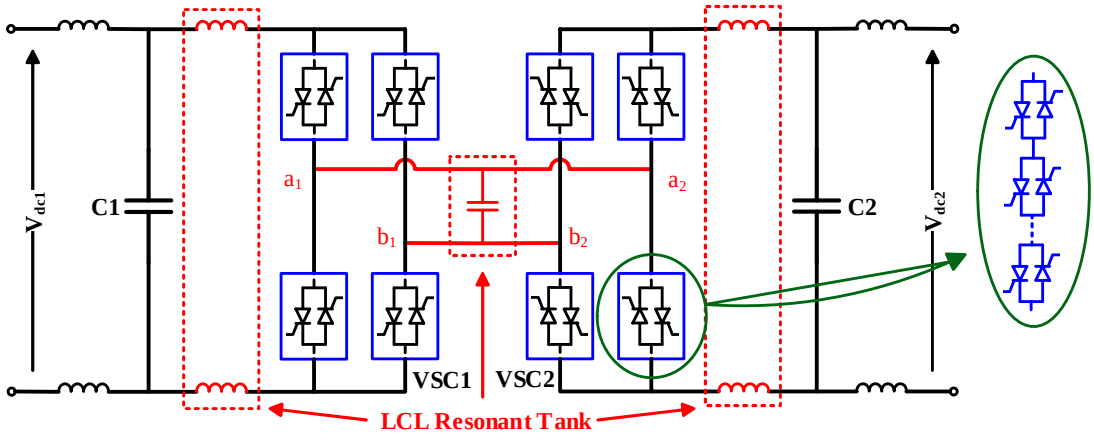


Figure 2.44. Schematic diagram of the resonant DC/DC converters [27].

This family has been initially proposed as a multi-functional unit to be used in MT-HVDC grids, capable of bidirectional power flow and limiting DC faults to a predefined section of the HVDC system. It can be implemented as two different subgroups based on the number of LC tanks used

in their structure: 1) Single-stage resonant DC/DC converters; and 2) Multiple-stage resonant DC/DC converters [27].

2.5.2.2.1.1. Single-Stage Resonant DC/DC Converters

Single-Stage Resonant DC/DC converters operate under the DC/AC/DC approach but without isolation, i.e., there is no AC transformers in their structure. The schematic diagram of this topology is the same as that shown in Figure 2.44, where power electronics bridges have been connected to the AC side through the resonant tank. Various resonant tanks, such as LCL and LC parallel tank with voltage doubler, can be used. However, this topology is suitable for low and medium power range with medium voltage ratios because of the high electrical stress on passive elements and the needs for high voltage/current rating resonant elements [27].

2.5.2.2.1.2. Multi-Stage Resonant DC/DC Converters

Multi-Stage Resonant DC/DC converter is the most advanced topology in the resonant family. In this topology, the full-rated central resonance tank is divided into several smaller and low-rated resonant circuits. The schematic diagram of the multi-stage resonant DC/DC converter is shown in Figure 2.45. This structure leads to a low-complexity design, and increases its modularity compared to that of its single-stage counterpart. However, it is not a pure modular topology because its structure has an inherent issue, which is the uneven distribution of currents/voltages on switches. In this topology, each resonant tank is used sequentially, and the power is transferred tank by tank to deliver the full power to the HV terminals. The reverse process is done similarly for step-down operations. This topology is suitable for high transformation ratios without considerable electrical stress on the resonant elements, unlike its single-stage counterpart [27].

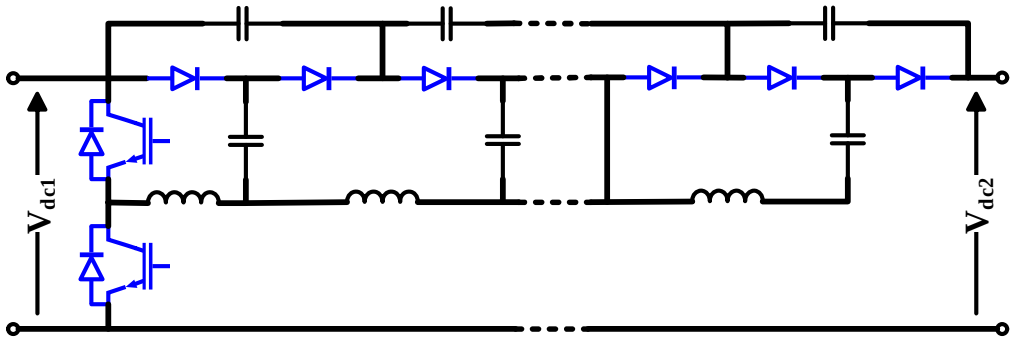


Figure 2.45. Schematic diagram of the Multi-stage resonant DC/DC converter [27].

2.5.2.2.2. DC Modular DC/DC Converters

DC Modular DC/DC converters employ the modular approach of MMCs to make the DC/DC conversion. To do so, two basic approaches are adopted: a) DC-MMC and b) Classical Choppers. Each of these approaches is herein examined [27].

2.5.2.2.2.1. DC Modular Multi-level Converters

DC Modular Multi-level Converters (DC-MMCs) are very similar to MMC power converters because they employ chain-links of MMC's sub-modules to generate voltages and currents at the desired frequencies. The schematic diagram of the DC-MMCs is shown in Figure 2.46.

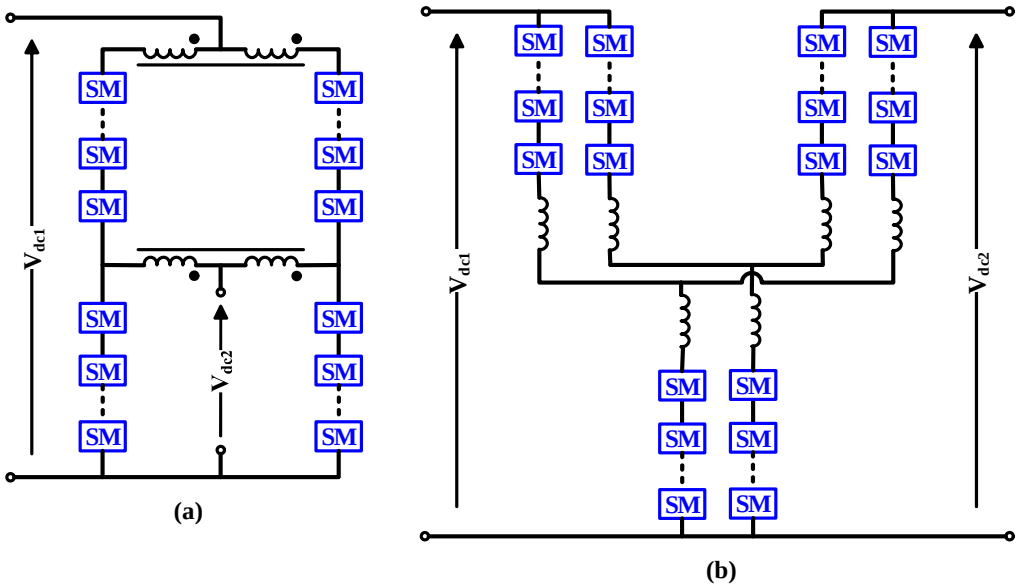


Figure 2.46. Schematic diagram of the DC-MMCs: a) equipped with filter; and b) equipped with control scheme [27].

This topology relies on the simultaneous generation of DC and AC waveforms to realize the power transmission. AC waveforms are used to ensure the energy balance in sub-modules, whereas DC waveforms are used to transfer power between DC terminals. However, issues arise due to the combination of AC and DC waveforms at the output DC terminal. To prevent such issues, a passive filter or a proper control scheme, can be used (Figure 2.46(a)-(b)). This family adopts the hard-switching scheme, and power losses of switches are high; this issue has been partially compensated by low-frequency switching. Increasing the operating frequency can decrease the required filter size, but switching losses will increase; thus, a trade-off is present between the filter size and power

losses. This family of DC/DC converters holds inherent advantages of MMCs (i.e., high reliability, modularity, and scalability) and is suitable for high power and voltage applications. However, there are some challenges, such as the required filter and AC circulating currents, which limit its application in low/medium power/voltage applications [27].

2.5.2.2.2.2. Classical Choppers

Classical Choppers belong to another family of DC modular DC/DC converters, and their operating principle relies on replacing some of the basic converter's switches with MMC's sub-modules, which extends the control capability. There are two topologies in this family based on the employed energy storage system: a) Capacitive Accumulation Choppers; and b) Inductive Accumulation Choppers. The schematic diagrams of both types of Choppers are shown in Figure 2.47.

The principle of Capacitive Accumulation Choppers is the adoption of MMC sub-modules as variable capacitors for energy storage purposes; existing capacitors are charged and discharged by switching the related chain-link of sub-modules, which are connected between DC terminals. Also, a dead time in the switching pattern is required to make this principle feasible considering DC voltage levels. The main switches operate under the soft-switching approach, but sub-modules are switched under the hard-switching approach. The schematic diagram of Capacitive Accumulated Choppers is shown in Figure 2.47(a).

Inductive Accumulation Choppers adopt a central inductor for energy storage, which is charged and discharged by switching the related chain-link of sub-modules. In this topology, a stair-case transition is performed between charging and discharging modes by using interleaved sub-modules, operating in either the resonance mode or resonance discontinuous-connection mode. As opposed to their capacitive counterpart, sub-modules can be operated using the soft-switching approach but with the cost of high conduction losses due to AC circulating currents. Therefore, a compromise should be achieved to reach an optimal operation point. Inductive Accumulation Choppers are suitable for applications that require high transformation ratios at low power, but a large-size central inductor should be employed. The sub-modules are switched following the hard-switching approach. The schematic diagram of the Inductive Accumulated Choppers is shown in Figure 2.47(b) [27].

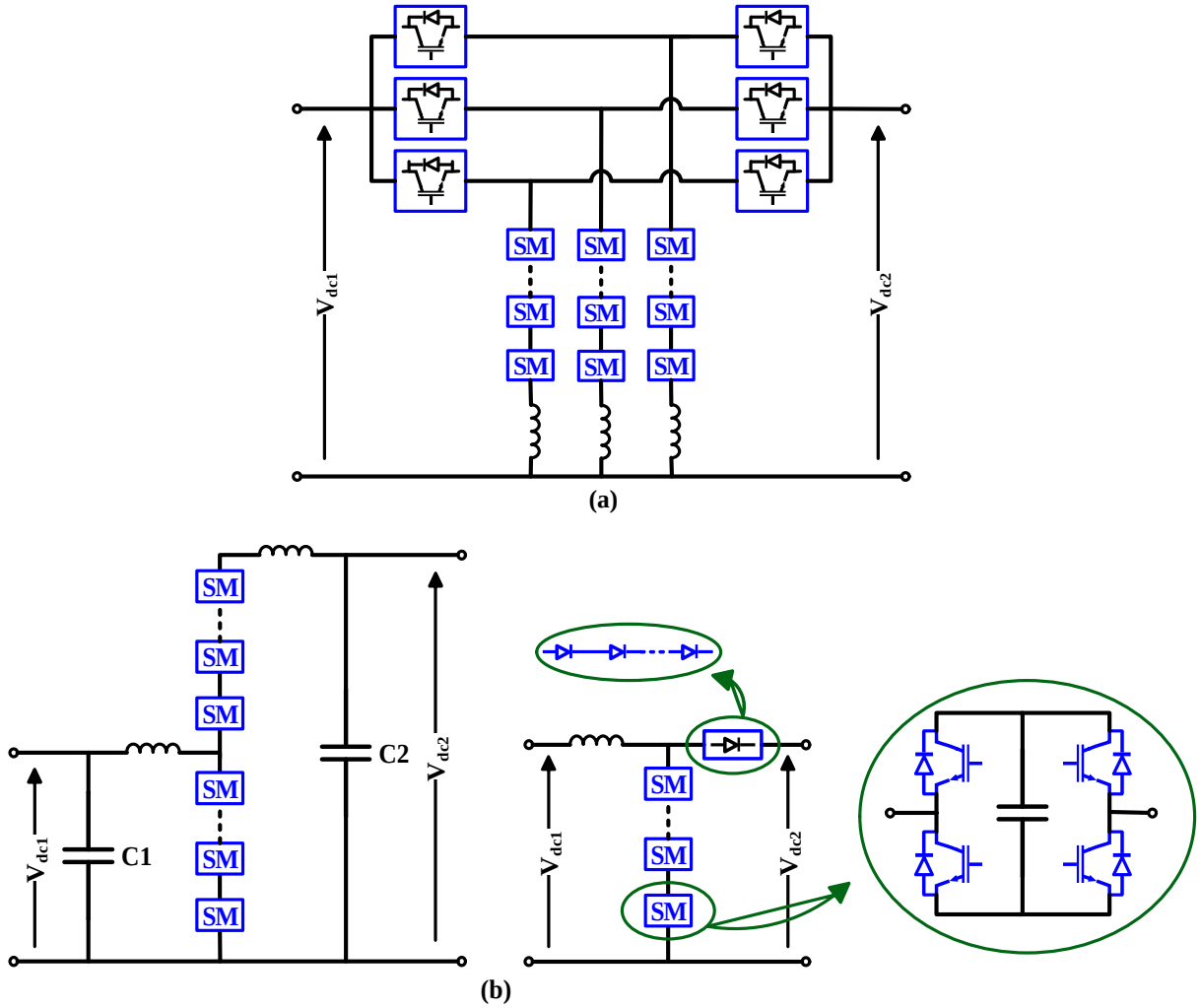


Figure 2.47. Schematic diagram of both types of Choppers: a) Capacitive Accumulated Choppers; and b) Inductive Accumulation Choppers [27].

2.6. DC Power Flow Controllers

DC Power Flow Controllers (DCPFCs), also known as DC Current Flow Controllers (DCCFCs), are power electronic devices primarily used for power flow control in HVDC transmission systems. Besides this purpose, they also perform fault blocking/limiting and protection functions. Therefore, DC-PFCs play a critical role in HVDC transmission systems. The importance of DC-PFCs becomes significant in the case of meshed MT-HVDC grids, because power can flow in different paths. Employing suitable devices (similar to Flexible AC Transmission Systems (FACTS) in AC systems) is essential for the power flow control and for compensating purposes. Various studies have been conducted to propose and develop novel and effective topologies for DCPFCs [30-35].

First, we briefly introduce the principle of power flow in DC transmission systems, for which, as opposed to AC systems, the capacitance and the inductance of transmission lines are not present in steady-state studies. The only parameter of DC transmission lines is their series and parallel resistances. According to the inherent feature of DC systems, there are no phasor angle and frequency in the voltage or current at DC terminals. Therefore, power flow of a DC line depends only on the voltage difference between DC sending terminals and DC receiving ends, and the line's series resistance. It is worth mentioning that line's parallel resistance has a negligible impact on the power flow of a DC line. Therefore, power flow of a DC line can only be controlled by changing the series resistance of a DC line or the voltage difference at the two DC ends. Various DCPFCs have been proposed, which can be categorized into three major groups: 1) Series DCPFC (SDCPFC); 2) Cascaded DCPFC (CDCPFC); and 3) Interline DCPFC (IDCPFC) [36-39].

DCPFCs can also be divided into two major groups based on the power electronics components used in their main structure: 1) Resistance-type (R-type); and 2) Voltage-type (V-type). DCPFCs are discussed in detail below. The general classification of DCPFCs is shown in Figure 2.48 [35-46].

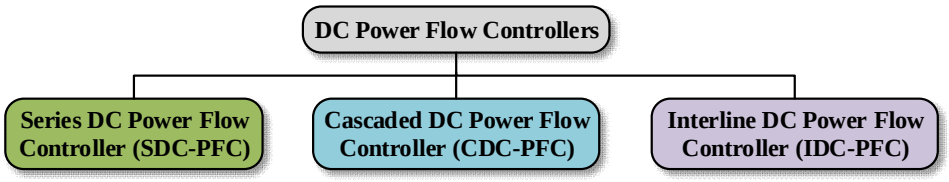


Figure 2.48. General classification of the DCPFCs.

2.6.1. Series DC Power Flow Controllers

SDCPFCs are power electronics devices installed in series in DC lines to control the current flow. These devices can be R-type or V-type. The R-type SDCPFCs "inject" resistance in a continuous or discrete mode. In the discrete mode, mechanical switches are used to inject or bypass one or several resistances. By using semiconductor switches, a specific amount of resistance can be injected in the DC lines ranging between *zero* (bypassed resistance condition) and R_{max} (the entire amount of resistance). However, this approach can only increase the total resistance of a DC line, and consequently, its current flow can only be decreased. Although the principle, implementation, and control of this type of SDCPFCs are straightforward, the R-type SDCPFCs are not an attractive

solution for HVDC transmission systems, due to their significant inherent power losses. The schematic diagram of the R-type SDCPFCs is shown in Figure 2.49 [42].

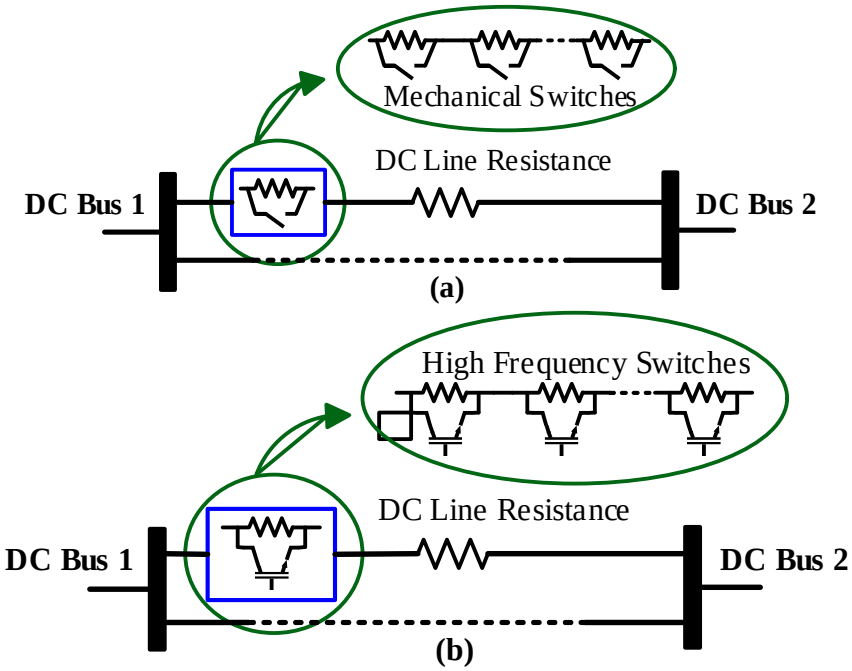


Figure 2.49. Schematic diagram of the R-type SDCPFCs: a) Discrete R-type SDCPFC; b) Variable R-type SDCPFC [42].

The V-type SDCPFCs use power electronic converters to inject a series of DC voltages into DC lines, and the voltage difference between the two DC ends will be accordingly changed. Using this method, the current flow can be increased and decreased. The principle is the use of an internal connection with the main system or an external connection with another energy source to inject a series of voltages into DC lines. The schematic diagram of V-type SDCPFC is shown in Figure 2.50 [43].

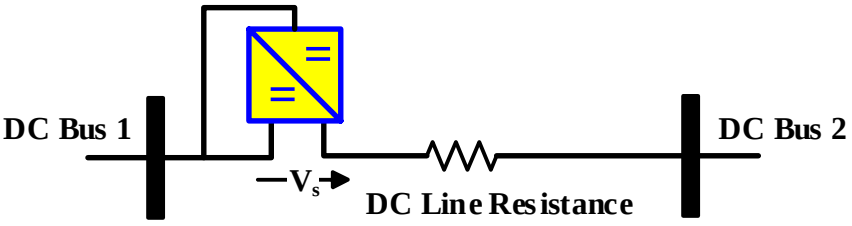


Figure 2.50. Schematic diagram of the V-type SDCPFC [43].

2.6.2. Cascaded DC Power Flow Controllers

CDCPFCs are power electronics and V-type DCPFC devices, whose purpose is the power flow control in a DC line (similar to SDC-PFCs). CDCPFCs are connected in series, their operation principle relies on changing the DC voltage with a suitable ratio, and their performance is similar to a DC transformer. DC/DC converters can be considered as CDCPFC because of DC/DC converters' capability to control power flow of DC lines. However, the applications of DC/DC converters are slightly different from CDCPFC. DC/DC converters are used for an entire HVDC station, and their size and power capacity are very large; while the CDCPFC concept has been proposed for just one HVDC line, and their size and power capacity are smaller than that of DC/DC converters. DC/DC converters can be redesigned to be used in HVDC lines. In real life, a CDCPFC has not yet been realized, but its conceptual structure has been proposed in [45], as shown in Figure 2.51.

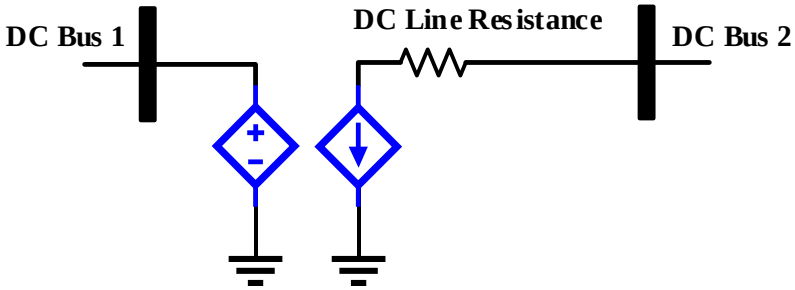


Figure 2.51. Conceptual structure of the CDCPFC [45].

2.6.3. Interline DC Power Flow Controllers

IDCPFCs are the most sophisticated family among the DCPFCs. The primary purpose of this family is to simultaneously control power flow in two or more DC lines. The principle of operation consists of power exchanges between two or more adjacent HVDC lines through an energy hub; passive elements, such as capacitances or inductances, are used to store extra power/energy from one line, which is then injected into one (or more) adjacent line(s). In this way, the current flow of the desired DC line will be controlled. Different IDCPFCs topologies and structures have been proposed and are under development. A leading and practical configuration has been proposed in [32]. This topology is based on merging and simplifying two simple H-bridges. The schematic diagram of an IDCPFC is shown in Figure 2.52.

The operation of this topology is similar to its AC counterpart, Interline Power Flow Controller (IPFC). In IPFC, power compensation and power flow control are achieved using the master-slave concept, and the parameters of the main line (i.e., the master line) are independently/actively controlled, while one parameter of another line (i.e., the slave line) is indirectly/passively controlled to meet the power balance criteria of the device. According to this operating philosophy, in IDCPFC, the power of the master line is actively controlled, and the power of the slave line is passively controlled to provide equilibrium in power transmission of the device. Other features, such as fault blocking/limiting, composite operation, and protection capabilities, can also be added. Various topologies are under development in this active and promising research area [32, 36-39].

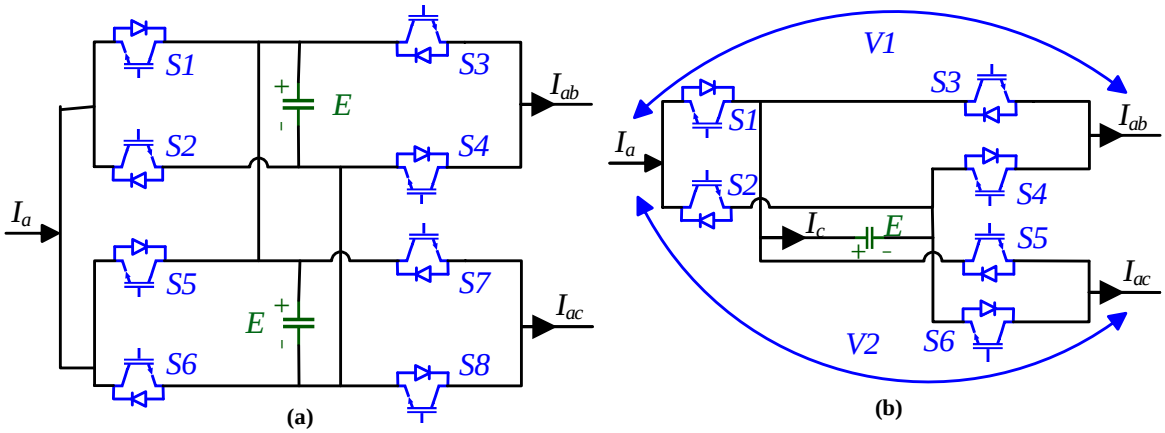


Figure 2.52. Schematic diagram of an IDCPFC: a) Original Structure b) Simplified Structure [32].

2.7. Conclusion

HVDC transmission systems are the promising technology serving as the backbone of tomorrow's power grids. Back-to-Back, Point-to-Point, and Multi-Terminal HVDC (MT-HVDC) grids have been herein discussed. Various configurations such as Monopolar, Bipolar, Homopolar, and Hybrid have been analyzed based on the principle of AC to DC power conversion and vice versa. These systems are generally based on power electronics converters and inverters. In this chapter, existing power electronics converters and inverters in HVDC transmission systems have been introduced.

Generally, power electronics converters can be classified into three major groups: a) Power Converters; b) DC/DC Converters; and c) DC Power Flow Controllers.

Power converters are primarily used to convert AC to DC power and vice versa. AC/DC power converters are implemented as electrical energy sources, according to the network theory definition of Voltage Source and Current Source, and all power converters can be categorized into three major groups: a) Voltage Source Converters (VSCs); b) Current Source Converters (CSCs); and c) Hybrid Current and Voltage Source Converters (HCVSCs). VSCs and its Modular Multi-level Converter (MMC) family will play an essential role in tomorrow's HVDC transmission systems because of their superior performance.

DC/DC converters, or DC Transformers, are power electronics devices with the duty of providing DC voltage matching. They can divide large MT-HVDC grids into several smaller protection zones, and realize DC voltage regulation, fault isolation, and connection of Bipolar/Monopolar configurations and CSC/VSC technologies. DC/DC power converters can be categorized into two major concepts: a) Isolated; and b) Non-Isolated. In the Isolated configuration, an AC link exists in the heart of the DC/DC converters, whereas the AC link is not present in the Non-Isolated configuration. Isolated DC/DC converters, mainly the Dual Active Bridge (DAB) family for HVDC transmission systems, are superior topologies compared to others.

DC Power Flow Controllers (DCPFCs) or DC Current Flow Controllers (DCCFCs) are power electronics devices for power flow control in HVDC transmission systems, especially in meshed MT-HVDC grids. Their operation principles have been inspired by Flexible AC Transmission Systems (FACTS) in AC systems. According to the inherent feature of DC systems, the power flow of a DC line depends only on the voltage difference between the DC terminals and the line's series resistance. Therefore, the principle of DCPFCs is to control or change the series resistance of a DC line or the voltage difference between the two DC ends. DCPFCs can be categorized into three major groups: a) Series DCPFC (SDCPFC); b) Cascaded DCPFC (CDCPFC); and c) Interline DCPFC (IDCPFC). They can also be categorized into Resistance-type (R-type) or Voltage-type (V-type). IDCPFCs possess superior performance compared to other DCPFCs, which is crucial for the tomorrow's HVDC transmission systems.

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3. Power Flow Study of MT-HVDC Grid Compensated by Multiport Interline DC Power Flow Controller

3.1. Abbreviation

CDCPFC	Cascaded DC power flow controller
CPB	Constant power bus
DCB	Droop controlled bus
DCPFC	DC power flow controller
DCPFE	DC power flow equation
DCPFP	DC power flow problem
DCPFS	DC power flow solver
FACTS	Flexible AC transmission system
IDCPFC	Interline DC power flow controller
KVL	Kirchhoff's voltage law
MIDCPFC	Multiport interline DC power flow controller
MT-HVDC	Multi-terminal HVDC
NR	Newton-Raphson
OffWF	Offshore wind farm
PF	Power flow
PIM	Power injection model
SDCPFC	Series DC power flow controller
SM	Static model
SP	Solution procedure
VSC	Voltage source converter

3.2. Introduction

MT-HVDC grids based on VSC technology are essential for transmitting power of renewable energy sources, especially offshore wind farms (OffWFs) [1-4]. However, development and expansion of these grids face significant challenges, such as restricted power flow (PF)

controllability, power flow through different paths (and consequently, loop flow), and under-utilization or overload of HVDC lines (especially in contingencies), which may cause diminished static security of MT-HVDC grids [5]. To overcome these challenges, practical devices known as DC power flow controllers (DCPFCs), inspired by the success of Flexible AC transmission system (FACTS) in AC systems, have been proposed in MT-HVDC grids [6, 7].

Series DC power flow controller (SDCPFC), Cascaded DC power flow controller (CDCPFC), and Interline DC power flow controller (IDCPFC) are three major groups of DCPFCs, which are categorized by their compensation approach. CDCPFCs are notable devices due to their advantages in the fault blocking capability and excellent control on PF of HVDC lines. SDCPFCs and IDCPFCs are prominent devices as a few numbers of semiconductor devices/switches are used in their structure, and thus, they are economical and can operate under a partial amount of the rated voltage in the system [5, 6, 8].

Generally, IDCPFCs are a pioneer family of DCPFCs, they are installed between HVDC lines (typically two lines) and transfer power from one line to another. To date, most studies have focused on proposing and developing novel structures for IDCPFCs. In [9-12], various topologies of IDCPFCs are proposed based on the master-slave concept, where PF of one HVDC line is controlled independently (actively), and PF of another line is controlled dependently (passively). Master-slave is used to meet the power-balance concept of IDCPFCs. Hence, one degree of freedom is added to the system in these topologies. A novel IDCPFC based on the master-slave concept, known as multiport interline DC power flow controller (MIDCPFC), is proposed in [13]; this controller can be installed among three HVDC lines, and can control two HVDC lines independently, and subsequently, adding two degrees of freedom to the system. PF studies of a typical IDCPFC are proposed in [14-17]. In [14, 15], two approaches, as a DC power flow solver (DCPFS), based on widely accepted Newton-Raphson (NR) method are proposed to solve the DC power flow problem (DCPFP) by deriving a static model (SM), and subsequently, a power injection model (PIM) of the considered IDCPFC. In [16, 17], two comprehensive solution procedures are proposed to solve DCPFPs considering technical constraints of the whole system and the employed IDCPFC. In [1], a DCPFS is proposed to solve DCPFPs of MT-HVDC grids in presence of MIDCPFCs considering losses of power converters and DCPFCs. However, it is not straightforward to implement the proposed DCPFS as an external process is needed to control the

voltage of the MIDCPFC's capacitor within its limits, which leads to a complicated Jacobin matrix, and thus, the higher computational burden. Also, the proposed model of the loss of MIDCPFCs is not simple, which increases the complexity of the DCPFS.

Despite a few reported studies on practical structures of IDCPFCs and their PF studies, a proper method (including an easy-to-use and effective DCPFS and suitable models for losses of MIDCPFC and VSCs) is lacking for solving the DCPFP of a highly meshed MT-HVDC grid with MIDCPFCs.

To fill in this research gap, in this chapter, a novel NR-based DCPFS is proposed by employing a novel MIDCPFC to solve the DCPFP. There are five main contributions in this chapter:

I. The SMs and PIM of the MIDCPFC are derived, and degrees of freedom related to the employed MIDCPFC are embedded in the proposed DCPFS to realize the predetermined PF objective(s).
II. A novel NR-based DCPFS is proposed. Since there are no fictitious buses in this proposed DCPFS, only a few modifications are needed in the original Jacobin matrix of the system and the original conductance matrix of the system, and its symmetry are preserved. Furthermore, this proposed DCPFS is very straightforward to use as an external process is not needed to control the voltage of MIDCPFC's capacitor.
III. Power losses of the MIDCPFC and VSCs are modeled in a comprehensive and conventional style, and their equations are embedded in the proposed DCPFS.
IV. A comprehensive solution procedure (SP) considering practical constraints of the MIDCPFC and MT-HVDC grid is proposed for solving the DCPFP.
V. A new highly meshed 15-bus MT-HVDC grid composed of 17 HVDC lines is created in this chapter to verify the accuracy of the proposed models and DCPFS, the derived equations, and the proposed/employed concepts.

The chapter is arranged as follows: In Section 3.3, MIDCPFC modeling is presented. DC power flow equations (DCPFEs) of the flexible MT-HVDC grid is derived in Section 3.4. In Section 3.5, a comprehensive solution procedure is proposed. Numerical results are presented in Section 3.6. Finally, the conclusion is drawn in Section 3.7.

3.3. MIDCPFC Modeling

This section is dedicated to developing the SMs (both basic and comprehensive types) and the PIM of the MIDCPFC. The MIDCPFC is connected among three HVDC lines to exchange/regulate/control power from two HVDC lines (master lines) to the third line (slave line).

3.3.1. Basic SM of the MIDCPFC

A MIDCPFC is basically a DC/DC converter as shown in Figure 3.1(a). It is composed of an H-bridge as its energy-hub and bidirectional IGBT switches to enable its bidirectional power flow capability. Without loss of generality, the current directions shown in Figure 3.1(a) are considered to develop the MIDCPFC's SM based on the average modeling method. Accordingly, DT4, DT1, DS1, DS2, DS3, S4, S5, S6, T2, T3, Q1, Q2, and Q3 are the semiconductor elements that conduct currents through the MIDCPFC.

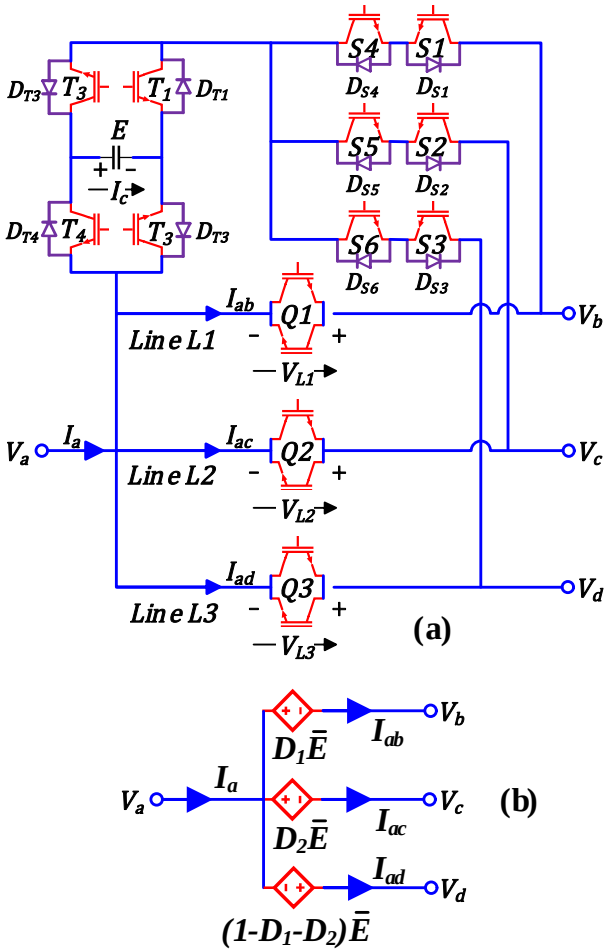

Figure 3.1. The schematic diagram of the MIDCPFC (a) and its basic SM (b).

To perform the average modeling, the steady-state value of the intermediate capacitor's current is considered to be zero ($I_c = 0$) to ensure a constant value of the intermediate capacitor's voltage (E). Also, unequal steady-state values of compensating voltages (V_{L1}, V_{L2}, and V_{L3}) are the essential condition for exchanging power/current between master and slave lines. The MIDCPFC's duty cycles (D_1 and D_2) are computed in (3.1), and the compensating voltages are computed in (3.2) by conducting the average modeling under suitable status (on/off) of semiconductor elements.

$$D_1 I_{ab} + D_2 I_{ac} - (1 - D_1 - D_2) I_{ad} = 0 \tag{3.1}$$

$$\overline{V_{L1}} = -D_1 \overline{E}, \quad \overline{V_{L2}} = -D_2 \overline{E}, \quad \overline{V_{L3}} = (1 - D_1 - D_2) \overline{E} \tag{3.2}$$

Where, I_{ab}, I_{ac}, and I_{ad} are currents of lines L1, L2, and L3, respectively.

The MIDCPFC's SM is shown in Figure 3.1(b), which is composed of three controllable and coordinated voltage sources and a function of control (independent) and physical (dependent) variables of the MIDCPFC ($D_1 \& D_2$ and $\overline{E}$, respectively). The developed SM, its procedure and conclusions of this subsection are applicable and authentic to other current directions of the MIDCPFC. A detailed process of developing SM can be found in [12].

3.3.2. Comprehensive SM of the MIDCPFC

According to the employed topology, two lines are master lines with the duty cycles of D_1 and D_2, and one line is the slave line with the duty cycle of ($1 - D_1 - D_2$). There is a significant difference between duty cycles of the two master lines: D_1 can be any value between zero and one, but D_2 can only be between zero and ($1 - D_1$). Therefore, D_1 is an independent freedom degree and D_2 is a semi-independent freedom degree. Accordingly, there are six states to select independent and semi-independent master lines. Since a master line can be connected to the MIDCPFC's intermediate capacitor through its both ends (positive/negative sides) to control (decrease/increase) currents, there are two states to control a master line's current. Therefore, there are a total of twelve states based on choosing master lines and the objective of the MIDCPFC in increasing/decreasing the

master line's currents. The developed SM of the MIDCPFC (considering the current directions) can be extended, as shown in Figure 3.2 and Table 3.1, in which k_{ab} , k_{ac}, and k_{ad} are duty cycles of voltage sources in the particular lines, and can be any parameter, D_1, D_2, or $(1-D_1-D_2)$.

The proposed comprehensive SM has a multi-role capability for the MIDCPFC as independent and semi-independent master lines can be chosen arbitrarily. In this study, the first state in Table 3.1 is considered for further analysis, but the whole concept can be applied to other states.

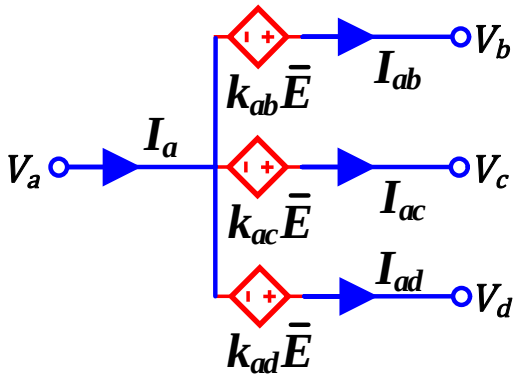

Figure 3.2. The comprehensive SM of the MIDCPFC.

Table 3.1. States of the comprehensive SM of the MIDCPFC

State	k_{ab}	k_{ac}	k_{ad}	$I_{ab}/I_{ac}/I_{ad}$
1	$-D_1$	$-D_2$	$(1-D_1-D_2)$	↓/↓/↑
2	D_1	D_2	$-(1-D_1-D_2)$	↑/↑/↓
3	$-D_2$	$-D_1$	$(1-D_1-D_2)$	↓/↓/↑
4	D_2	D_1	$-(1-D_1-D_2)$	↑/↑/↓
5	$-D_1$	$(1-D_1-D_2)$	$-D_2$	↓/↑/↓
6	D_1	$-(1-D_1-D_2)$	D_2	↑/↓/↑
7	$-D_2$	$(1-D_1-D_2)$	$-D_1$	↓/↑/↓
8	D_2	$-(1-D_1-D_2)$	D_1	↑/↓/↑
9	$(1-D_1-D_2)$	$-D_1$	$-D_2$	↑/↓/↓
10	$-(1-D_1-D_2)$	D_1	D_2	↓/↑/↑
11	$(1-D_1-D_2)$	$-D_2$	$-D_1$	↑/↓/↓
12	$-(1-D_1-D_2)$	D_2	D_1	↓/↑/↑

3.3.3. PIM of the MIDCPFC

The process of deriving the PIM for the MIDCPFC begins by embedding its SM in HVDC lines and deriving DCPFEs. We use the lumped π-model of HVDC lines including their parallel branches to derive precise DCPFEs [18]. Inductive/capacitive elements are neglected as the focus of this study is on the static analysis. The MIDCPFC compensated (*flexible*) HVDC lines are shown in Figure 3.3(a) and their DCPFEs are derived in (3.3)-(3.8) by employing KVL.

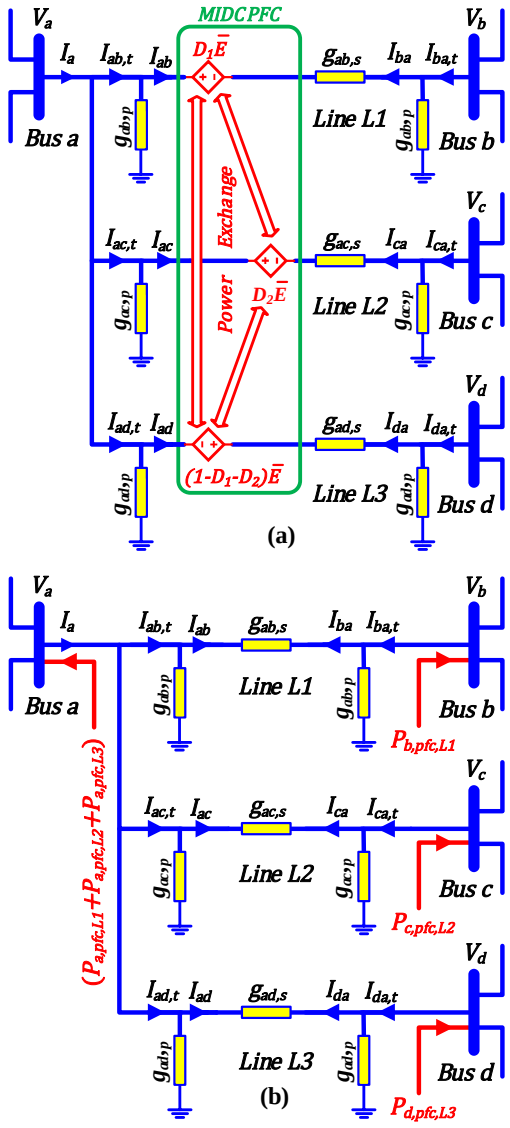

Figure 3.3. The PIM of the MIDCPFC.

$$P_{ab,t} = V_a I_{ab,t} = (g_{ab,p} + g_{ab,s})V_a^2 - V_a g_{ab,s} V_b - \underbrace{V_a g_{ab,s} D_1 \overline{E}}_{P_{a,pfc,L1}} \tag{3.3}$$

$$P_{ba,t} = V_b I_{ba,t} = (g_{ab,p} + g_{ab,s})V_b^2 - V_b g_{ab,s} V_a - \underbrace{(-V_b g_{ab,s} D_1 \overline{E})}_{P_{b,pfc,L1}} \tag{3.4}$$

$$P_{ac,t} = V_a I_{ac,t} = (g_{ac,p} + g_{ac,s})V_a^2 - V_a g_{ac,s} V_c - \underbrace{V_a g_{ac,s} D_2 \overline{E}}_{P_{a,pfc,L2}} \tag{3.5}$$

$$P_{ca,t} = V_c I_{ca,t} = (g_{ac,p} + g_{ac,s})V_c^2 - V_c g_{ac,s} V_a - \underbrace{(-V_c g_{ac,s} D_2 \overline{E})}_{P_{c,pfc,L2}} \tag{3.6}$$

$$P_{ad,t} = V_a I_{ad,t} = (g_{ad,p} + g_{ad,s})V_a^2 - V_a g_{ad,s} V_d - \underbrace{(-V_a g_{ad,s}(1 - D_1 - D_2)\overline{E})}_{P_{a,pfc,L3}} \tag{3.7}$$

$$P_{da,t} = V_d I_{da,t} = (g_{ad,p} + g_{ad,s})V_d^2 - V_d g_{ad,s} V_a - \underbrace{(V_d g_{ad,s}(1 - D_1 - D_2)\overline{E})}_{P_{d,pfc,L3}} \tag{3.8}$$

Where g , V , and I represent conductances, voltages, and currents, respectively. By deriving DCPFEs related to the MIDCPFC ($P_{a,pfc,L1}$, $P_{a,pfc,L2}$, $P_{a,pfc,L3}$, $P_{b,pfc,L1}$, $P_{c,pfc,L2}$, $P_{d,pfc,L3}$) and omitting the MIDCPFC's schematic from HVDC lines, the PIM of the MIDCPFC is obtained without using any fictitious buses as shown in Fig. 3(b). The derived DCPFEs of the MIDCPFC are represented as extra fictitious injected power, which are the core of the PIM of the MIDCPFC. At particular values of the MIDCPFC's duty cycles (D_{1null} and D_{2null}), $\overline{E}$ is equal to zero, so the fictitious power is zero, and the MIDCPFC is in null operation state.

3.4. DC Power Flow Equations of Flexible MT-HVDC Grids

This section is dedicated to deriving DCPFEs of the MIDCPFC compensated (flexible) MT-HVDC grids by considering power losses of VSCs and the MIDCPFC in the system, and proposing a novel DCPFS to solve the DCPFP. The power loss equations of the MIDCPFC and VSCs are derived in Subsection A; DCPFEs of HVDC buses are provided in Subsection B; and a novel DCPFS is proposed in Subsection C, the MIDCPFC and power losses of the system are considered in this solver.

3.4.1. Power Loss Equations of the MIDCPFC and VSCs

The power loss equation of the MIDCPFC is derived by employing the active power-balance concept. Accordingly, $\overline{E}$ is derived in terms of the voltage of the buses connected to the MIDCPFC

(V_a, V_b, V_c, and V_d). The power loss of the MIDCPFC is modeled as a function of the intermediate capacitor voltage and current ($\overline{E}$ and I_c). Therefore, the power loss of the MIDCPFC (and its power-balance equation) can be expressed in (3.9).

$$\begin{aligned} &P_{loss,PFC} = (D_1 I_{ab} + D_2 I_{ac} - (1 - D_1 - D_2) I_{ad})\overline{E} = \alpha \\ &+\beta[|D_1 I_{ab}| + |D_2 I_{ac}| + |(1 - D_1 - D_2) I_{ad}|] + \gamma[(D_1 I_{ab})^2 + (D_2 I_{ac})^2 + ((1 - D_1 - D_2) I_{ad})^2] \\ &I_{ab} = (V_a - D_1 \overline{E} - V_b) g_{ab,s},\ I_{ac} = (V_a - D_2 \overline{E} - V_c) g_{ab,s},\quad I_{ad} = (V_a + (1 - D_1 - D_2)\overline{E} - V_d) g_{ad,s} \end{aligned} \tag{3.9}$$

Where the first two terms on the left side of (3.9) are related to the stored power in the energy-hub (the intermediate capacitor) of the MIDCPFC, and the third term is the power extracted from the energy-hub. α is the no-load loss. β and γ are linear and quadratic dependency of the MIDCPFC's loss on the current flowing through the MIDCPFC, respectively.

The general power of the MIDCPFC is computed in (3.10).

$$\begin{aligned} &P_{dev} = (D_1 I_{ab} + D_2 I_{ac} - (1 - D_1 - D_2) I_{ad})\overline{E} - [\alpha + \beta[|D_1 I_{ab}| + |D_2 I_{ac}| + |(1 - D_1 - D_2) I_{ad}|] \\ &+\gamma[(D_1 I_{ab})^2 + (D_2 I_{ac})^2 + ((1 - D_1 - D_2) I_{ad})^2]] \end{aligned} \tag{3.10}$$

The power loss of VSCs can be modeled in (3.11).

$$P_{loss,VSC} = a + b|I_{th}| + cI_{th}^2 \tag{3.11}$$

Where a represents no-load converter losses. b and c are two constant coefficients representing linear and quadratic dependency of the VSC's loss on the current flowing through the VSC in injecting/absorbing states, respectively. I_{th} is the sum of currents of all lines connected to the VSC in the power-absorbing state. I_{th} can also be computed by (3.12) in the power-injecting state [19].

$$I_{th} = \frac{P_{Injection}}{pf\sqrt{3}V_{ac}} \tag{3.12}$$

Where $P_{Injection}$ is the injected power from the generation unit (e.g. OffWF) to the VSC. pf and V_{ac} are the power factor and AC voltage of the generation unit, respectively.

3.4.2. DCPFEs of DC Buses

DCPFEs of a non-compensated MT-HVDC grid can be found in [14-17]. Therefore, in this subsection, we only derive DCPFEs for flexible MT-HVDC grids.

In this chapter, a generic N-bus flexible MT-HVDC grid is considered, in which some buses are constant power buses (CPBs), and some buses are droop-controlled buses (DCBs) operating under the droop control philosophy for distributed DC voltage control [20].

The DCPFE of CPBs considering the VSC power loss is derived in (3.13).

$$P_i = P_{Gi} - P_{Li} = V_i I_i = V_i \sum_{j=1}^{N} (G_{ij} V_j) + P_{loss,i}\ ,\ i, j = 1, ..., N \tag{3.13}$$

Where P_i , I_i , P_{Li}, P_{Gi}, $P_{loss,i}$, and V_i represent the net power and current injected to bus i , the power of the load and generating units, the power loss of the VSC, and the voltage of bus i , respectively. Also, $\boldsymbol{G}$ symbolizes the system's conductance matrix in (3.14), in which $g_{ij,s}$ and $g_{ij,p}$ represent series and parallel conductances of HVDC lines, respectively.

$$\boldsymbol{G} = [G_{ij}],\ G_{ij} = -g_{ij,s}\ ,\ G_{ii} = \sum_{j=1}^{N} (g_{ij,s} + g_{ij,p}),\ i, j = 1, ..., N \tag{3.14}$$

The DCPFE of DCBs considering the VSC power loss is derived in (3.15).

$$P_i = V_i I_i = -k_{d,i}(V_i - V_i^*) = V_i \sum_{j=1}^{N} (G_{ij} V_j) + P_{loss,i}\ ,\ i, j = 1, ..., N \tag{3.15}$$

Where V_i^* and $k_{d,i}$ are the droop voltage reference and the droop gain, respectively.

3.4.3. The proposed DCPFS

The general equations of a DCPFS (without integrating the DCPFCs) are presented in [14-17]. Therefore, we only focus on the proposed novel NR-based DCPFS. Its structure is made by three matrices: the variable vector ($\boldsymbol{VarV}$), the mismatch vector ($\boldsymbol{MV}$), and the related Jacobin matrix ($\boldsymbol{J}$). The general process of solving a DCPFP employing NR-based methods is provided as follows:

$$\boldsymbol{VarV} = [V_1\ ...\ V_N\ \ D_1\ \ D_2\ \ E]^T \tag{3.16}$$

$$\boldsymbol{ParV} = [P_1\ ...\ P_N\ REF_1\ \ REF_2\ \ P_{dev}]^T \tag{3.17}$$

$$\boldsymbol{MV} = [\Delta P_1\ ...\ \Delta P_N\ \ \Delta REF_1\ \ \Delta REF_2\ \ \Delta P_{dev}]^T \tag{3.18}$$

$$\Delta P_i = P_i^* - P_i\ ,\ i = 1, ..., N\ ,\ \Delta REF_n = REF_n^* - REF_n\ ,\ n = 1, 2,\quad \Delta P_{dev} = P_{dev}^* - P_{dev} \tag{3.19}$$

$$[\boldsymbol{J}].[\Delta \boldsymbol{VarV}] = [\boldsymbol{MV}] \tag{3.20}$$

$$[\Delta \boldsymbol{VarV}]^k = ([\boldsymbol{J}]^k)^{-1}.[\boldsymbol{MV}]^k \tag{3.21}$$

$$[\boldsymbol{VarV}]^{k+1} = [\boldsymbol{VarV}]^k + [\Delta \boldsymbol{VarV}]^k \tag{3.22}$$

Where REF and REF^* are parameters that must be controlled in the system (e.g., the power flowing through a HVDC line) and their predetermined values, respectively. P_i^* is the reference/predetermined value of the power of bus i. k is the iteration number. The predetermined value of DCBs is equal to $k_{d,i}V_i^*$.

In a generic non-compensated MT-HVDC grid, $\boldsymbol{VarV}$ is the bus voltage, and $\boldsymbol{MV}$ is the difference between the calculated power of buses/parameters (parameters of the system, $\boldsymbol{ParV}$) and their predetermined values. However, in flexible MT-HVDC grids, variables/parameters of the MIDCPFC are added to $\boldsymbol{VarV}$, $\boldsymbol{ParV}$ and $\boldsymbol{MV}$, the $\boldsymbol{J}$ matrix is thus modified. In this study, N_p buses are CPBs, N_d buses are DCBs ($N = N_d + N_p$), and it is assumed that buses a, b, c, and d are connected to the MIDCPFC (that can be any combination of CPBs and/or DCBs). Without loss of generality, they are assumed to be CPBs. Accordingly, the following numbering order of the buses is considered to facilitate deriving the $\boldsymbol{J}$ matrix.

$$1<...<N_d<f<...<m<a<b<c<d, \quad f = N_d + 1,\ m = N_d + N_p - 4,\ d = N \tag{3.23}$$

The triple constituent matrices of the proposed DCPFS are expressed as follows:

$$[\boldsymbol{J}]=$$

	1 … … N_d	f …	m	a b c d	N+1	N+2	N+3
1 … N_d							
f … m	H			K	L		
a b c d				M	O	Q	A
N+1				R	S		T
N+2	U			W	Y		Z
N+3				B	C		F

(3.24)

$$[\Delta \boldsymbol{VarV}]=[\underbrace{\Delta V_1..\Delta V_{N_d}}_{N_d\ buses}\underbrace{\Delta V_f..\Delta V_m \Delta V_a \Delta V_b \Delta V_c \Delta V_d}_{N_p\ buses}\underbrace{\Delta D_1 \Delta D_2 \Delta E}_{added\ \text{var.}}] \tag{3.25}$$

$$[\boldsymbol{MV}]=[\underbrace{\Delta P_1..\Delta P_{N_d}}_{N_d\ buses}\underbrace{\Delta P_f..\Delta P_m \Delta P_a \Delta P_b \Delta P_c \Delta P_d}_{N_p\ buses}\underbrace{\Delta REF_1 \Delta REF_2 \Delta P_{dev}}_{added\ \text{var.}}] \tag{3.26}$$

Equations (3.24)-(3.26) are the core of the proposed DCPFS. The original system's variable matrix is extended by embedding three MIDCPFC's variables/degrees of freedom (D_1, D_2, and E) placed at the end of $\boldsymbol{VarV}$. Also, the parameters REF_1, REF_2, and P_{dev} are the added control objectives that have been added to the original vector. The parameter E is inherently a dependent variable and the function of V_a, V_b, V_c, V_d, D_1 and D_2[1], but it can be sensed/treated as an independent variable as long as P_{dev} is satisfied/reached. This feature adds one extra freedom degree (i.e., E) to the system, i.e., the proposed DCPFS is able to treat/control the variable E as an independent variable/freedom degree while respecting its inherent feature. REF can be any arbitrary system's parameter (current/power of any HVDC line) to be controlled. Flexibility in choosing REF provides a multi-control objective feature for the proposed DCPFS. Since the main purpose of employing the

MIDCPFC is to control power/current flowing through particular (master) HVDC lines, the following parameters can be chosen as REF_1 and REF_2:

- *The transferred power to the energy-hub of the MIDCPFC:*

$$P_{PFCm}=\begin{cases} D_1\overline{E}I_{ab}=D_1\overline{E}(V_a-D_1\overline{E}-V_b)g_{ab,s}, \ Line \ \ L1 \\ D_2\overline{E}I_{ac}=D_2\overline{E}(V_a-D_2\overline{E}-V_c)g_{ac,s}, \ Line \ \ L2 \end{cases} \tag{3.27}$$

- *The power flowing through the master HVDC lines:*

$$P_{L1}=V_aI_{ab}=V_a(V_b+D_1\overline{E}-V_a)G_{ab}, \ Line \ \ L1 \tag{3.28}$$

$$P_{L2}=V_aI_{ac}=V_a(V_c+D_2\overline{E}-V_a)G_{ac}, \ Line \ \ L2 \tag{3.29}$$

- *The current flowing through the master HVDC lines:*

$$I_{L1}=I_{ab}=(V_b+D_1\overline{E}-V_a)G_{ab}, \ Line \ \ L1 \tag{3.30}$$

$$I_{L2}=I_{ac}=(V_c+D_2\overline{E}-V_a)G_{ac}, \ Line \ \ L2 \tag{3.31}$$

Lines L1 and L2 are the master lines with independent duty cycles of the MIDCPFC, D_1 and D_2. Line L3 is the slave line with a dependent duty cycle of the MIDCPFC, $(1-D_1-D_2)$. The power flowing through the master lines is the control objective parameter in this chapter.

Accordingly, the $\boldsymbol{J}$ matrix can be computed by (3.32)-(3.86):

$$H_{ij}=\frac{-\partial ParV_i}{\partial VarV_j}=\begin{cases} -G_{ij}V_i+X_1 & ,1\le i\le d \ ,1\le j\le m \ ,i\ne j \\ -\sum_{j=f,j\ne i}^{m}(G_{ij}V_j)-2G_{ij}V_i+X_1 & ,f\le i=j\le m \\ -\sum_{j=1,j\ne i}^{N_d}(G_{ij}V_j)-2G_{ij}V_i-k_{d,i}+X_1 & ,1\le i=j\le N_d \end{cases} \tag{3.32}$$

$$K_{ij}=\frac{-\partial ParV_i}{\partial VarV_j}=-G_{ij}V_i+X_1 \ \ ,1\le i\le m \ ,a\le j\le d \tag{3.33}$$

$$L_{ij}=\frac{-\partial ParV_i}{\partial VarV_j}=0, \ 1\le i\le m \ \ ,(N+1)\le j\le(N+2) \tag{3.34}$$

$$M_{aa} = \frac{-\partial ParV_a}{\partial VarV_a} = \frac{-\partial P_a}{\partial V_a}$$
$$= -\sum_{j=1,\, j\neq a}^{d=N} \left(G_{aj}V_j\right) - 2G_{aa}V_a - G_{ab}ED_1 - G_{ac}ED_2 + G_{ad}E(1-D_1-D_2) + X_1 \quad (3.35)$$

$$M_{ab} = \frac{-\partial ParV_a}{\partial VarV_b} = \frac{-\partial P_a}{\partial V_b} = -G_{ab}V_a + X_1 \quad (3.36)$$

$$M_{ac} = \frac{-\partial ParV_a}{\partial VarV_c} = \frac{-\partial P_a}{\partial V_c} = -G_{ac}V_a + X_1 \quad (3.37)$$

$$M_{ad} = \frac{-\partial ParV_a}{\partial VarV_d} = \frac{-\partial P_a}{\partial V_d} = -G_{ad}V_a + X_1 \quad (3.38)$$

$$M_{ba} = \frac{-\partial ParV_b}{\partial VarV_a} = \frac{-\partial P_b}{\partial V_a} = -G_{ab}V_b + X_1 \quad (3.39)$$

$$M_{bb} = \frac{-\partial ParV_b}{\partial VarV_b} = \frac{-\partial P_b}{\partial V_b} = -\sum_{j=1,\, j\neq b}^{d=N} \left(G_{bj}V_j\right) - 2G_{bb}V_b + G_{ab}ED_1 + X_1 \quad (3.40)$$

$$M_{bc} = \frac{-\partial ParV_b}{\partial VarV_c} = \frac{-\partial P_b}{\partial V_c} = -G_{bc}V_b + X_1 \quad (3.41)$$

$$M_{bd} = \frac{-\partial ParV_b}{\partial VarV_d} = \frac{-\partial P_b}{\partial V_d} = -G_{bd}V_b + X_1 \quad (3.42)$$

$$M_{ca} = \frac{-\partial ParV_c}{\partial VarV_a} = \frac{-\partial P_c}{\partial V_a} = -G_{ac}V_c + X_1 \quad (3.43)$$

$$M_{cb} = \frac{-\partial ParV_c}{\partial VarV_b} = \frac{-\partial P_c}{\partial V_b} = -G_{bc}V_c + X_1 \quad (3.44)$$

$$M_{cc} = \frac{-\partial ParV_c}{\partial VarV_c} = \frac{-\partial P_c}{\partial V_c} = -\sum_{j=1,\, j\neq c}^{d=N} \left(G_{cj}V_j\right) - 2G_{cc}V_c + G_{ac}ED_2 + X_1 \quad (3.45)$$

$$M_{cd} = \frac{-\partial ParV_c}{\partial VarV_d} = \frac{-\partial P_c}{\partial V_d} = -G_{cd}V_c + X_1 \quad (3.46)$$

$$M_{da} = \frac{-\partial ParV_d}{\partial VarV_a} = \frac{-\partial P_d}{\partial V_a} = -G_{ad}V_d + X_1 \quad (3.47)$$

$$M_{db} = \frac{-\partial ParV_d}{\partial VarV_b} = \frac{-\partial P_d}{\partial V_b} = -G_{bd}V_d + X_1 \quad (3.48)$$

$$M_{dc} = \frac{-\partial ParV_d}{\partial VarV_c} = \frac{-\partial P_d}{\partial V_c} = -G_{cd}V_d + X_1 \quad (3.49)$$

$$M_{dd} = \frac{-\partial ParV_d}{\partial VarV_d} = \frac{-\partial P_d}{\partial V_d} = -\sum_{j=1,\, j\neq b}^{d=N} \left(G_{dj}V_j\right) - 2G_{dd}V_d + G_{ad}E(1-D_1-D_2) + X_1 \tag{3.50}$$

$$O_{a(N+1)} = \frac{-\partial ParV_a}{\partial VarV_{N+1}} = \frac{-\partial P_a}{\partial D_1} = -(G_{ab}+G_{ad})EVa + X_1 \tag{3.51}$$

$$O_{b(N+1)} = \frac{-\partial ParV_b}{\partial VarV_{N+1}} = \frac{-\partial P_b}{\partial D_1} = G_{ab}EV_b + X_1 \tag{3.52}$$

$$O_{c(N+1)} = \frac{-\partial ParV_c}{\partial VarV_{N+1}} = \frac{-\partial P_c}{\partial D_1} = 0 \tag{3.53}$$

$$O_{d(N+1)} = \frac{-\partial ParV_d}{\partial VarV_{N+1}} = \frac{-\partial P_d}{\partial D_1} = G_{ad}EV_d + X_1 \tag{3.54}$$

$$Q_{a(N+2)} = \frac{-\partial ParV_a}{\partial VarV_{N+2}} = \frac{-\partial P_a}{\partial D_2} = -(G_{ac}+G_{ad})EV_a + X_1 \tag{3.55}$$

$$Q_{b(N+2)} = \frac{-\partial ParV_b}{\partial VarV_{N+2}} = \frac{-\partial P_b}{\partial D_2} = 0 \tag{3.56}$$

$$Q_{c(N+2)} = \frac{-\partial ParV_c}{\partial VarV_{N+2}} = \frac{-\partial P_c}{\partial D_2} = G_{ac}EV_c + X_1 \tag{3.57}$$

$$Q_{d(N+2)} = \frac{-\partial ParV_d}{\partial VarV_{N+2}} = \frac{-\partial P_d}{\partial D_2} = G_{ad}EV_d + X_1 \tag{3.58}$$

$$A_{a(N+3)} = \frac{-\partial ParV_a}{\partial VarV_{N+3}} = \frac{-\partial P_a}{\partial E} = -[D_1G_{ab} + D_2G_{ac} - (1-D_1-D_2)G_{ad}]V_a + X_1 \tag{3.59}$$

$$A_{b(N+3)} = \frac{-\partial ParV_b}{\partial VarV_{N+3}} = \frac{-\partial P_b}{\partial E} = D_1G_{ab}V_b + X_1 \tag{3.60}$$

$$A_{c(N+3)} = \frac{-\partial ParV_c}{\partial VarV_{N+3}} = \frac{-\partial P_c}{\partial E} = D_2G_{ac}V_c + X_1 \tag{3.61}$$

$$A_{d(N+3)} = \frac{-\partial ParV_d}{\partial VarV_{N+3}} = \frac{-\partial P_d}{\partial E} = (1-D_1-D_2)G_{ad}V_d + X_1 \tag{3.62}$$

$$U_{ij} = \frac{-\partial ParV_i}{\partial VarV_j} = 0, \;\; (N+1) \le i \le (N+2) \;\; ,1 \le j \le m \tag{3.63}$$

$$R_{(N+1)a} = \frac{-\partial ParV_{N+1}}{\partial VarV_a} = \frac{-\partial REF_1}{\partial V_a} = -G_{ab}(V_b + D_1E - 2V_a) \tag{3.64}$$

$$R_{(N+1)b} = \frac{-\partial ParV_{N+1}}{\partial VarV_b} = \frac{-\partial REF_1}{\partial V_b} = -G_{ab}V_a \tag{3.65}$$

$$R_{(N+1)c} = \frac{-\partial ParV_{N+1}}{\partial VarV_c} = \frac{-\partial REF_1}{\partial V_c} = 0 \tag{3.66}$$

$$R_{(N+1)d} = \frac{-\partial ParV_{N+1}}{\partial VarV_d} = \frac{-\partial REF_1}{\partial V_d} = 0 \tag{3.67}$$

$$W_{(N+2)a} = \frac{-\partial ParV_{N+2}}{\partial VarV_a} = \frac{-\partial REF_2}{\partial V_a} = -G_{ac}(V_c + D_2E - 2V_a) \tag{3.68}$$

$$W_{(N+2)b} = \frac{-\partial ParV_{N+2}}{\partial VarV_b} = \frac{-\partial REF_2}{\partial V_b} = 0 \tag{3.69}$$

$$W_{(N+2)c} = \frac{-\partial ParV_{N+2}}{\partial VarV_c} = \frac{-\partial REF_2}{\partial V_c} = -G_{ac}V_a \tag{3.70}$$

$$W_{(N+2)d} = \frac{-\partial ParV_{N+2}}{\partial VarV_d} = \frac{-\partial REF_2}{\partial V_d} = 0 \tag{3.71}$$

$$\begin{aligned} B_{(N+3)a} &= \frac{-\partial ParV_{N+3}}{\partial VarV_a} = \frac{-\partial P_{dev}}{\partial V_a} = (D_1G_{ab} + D_2G_{ac} - (1-D_1-D_2)G_{ad})E \\ &-\beta[D_1G_{ab}\,\mathrm{sgn}(D_1G_{ab}(V_b + D_1E - V_a)) + D_2G_{ac}\,\mathrm{sgn}(D_2G_{ac}(V_c + D_2E - V_a)) \\ &-(1-D_1-D_2)G_{ad}\,\mathrm{sgn}((D_1+D_2-1)G_{ad}(V_d - (1-D_1-D_2)E - Va))] \\ &-\gamma[2D_1^2G_{ab}^2(V_b + D_1E - V_a) + 2D_2^2G_{ac}^2(V_c + D_2E - V_a) \\ &+2(1-D_1-D_2)^2G_{ad}^2(V_d - (1-D_1-D_2)E - V_a)] \end{aligned} \tag{3.72}$$

$$\begin{aligned} B_{(N+3)b} &= \frac{-\partial ParV_{N+3}}{\partial VarV_b} = \frac{-\partial P_{dev}}{\partial V_b} \\ &= -D_1G_{ab}E + \beta D_1G_{ab}\,\mathrm{sgn}(D_1G_{ab}(V_b + D_1E - V_a)) + 2\gamma D_1^2G_{ab}^2(V_b + D_1E - V_a) \end{aligned} \tag{3.73}$$

$$\begin{aligned} B_{(N+3)c} &= \frac{-\partial ParV_{N+3}}{\partial VarV_c} = \frac{-\partial P_{dev}}{\partial V_c} \\ &= -D_2G_{ac}E + \beta D_2G_{ac}\,\mathrm{sgn}(D_2G_{ac}(V_c + D_2E - V_a)) + 2\gamma D_2^2G_{ac}^2(V_c + D_2E - V_a) \end{aligned} \tag{3.74}$$

$$\begin{aligned} B_{(N+3)d} &= \frac{-\partial ParV_{N+3}}{\partial VarV_d} = \frac{-\partial P_{dev}}{\partial V_d} = (1-D_1-D_2)G_{ad}E \\ &+\beta(1-D_1-D_2)G_{ad}\,\mathrm{sgn}((D_1+D_2-1)G_{ad}(V_d - (1-D_1-D_2)E - V_a)) \\ &+2\gamma(1-D_1-D_2)^2G_{ad}^2(V_d - (1-D_1-D_2)E - V_a) \end{aligned} \tag{3.75}$$

$$S_{(N+1)(N+1)} = \frac{-\partial ParV_{N+1}}{\partial VarV_{N+1}} = \frac{-\partial REF_1}{\partial D_1} = -G_{ab}V_aE \tag{3.76}$$

$$S_{(N+1)(N+2)} = \frac{-\partial ParV_{N+1}}{\partial VarV_{N+2}} = \frac{-\partial REF_1}{\partial D_2} = 0 \tag{3.77}$$

$$Y_{(N+2)(N+1)} = \frac{-\partial ParV_{N+2}}{\partial VarV_{N+1}} = \frac{-\partial REF_2}{\partial D_1} = 0 \tag{3.78}$$

$$Y_{(N+2)(N+2)} = \frac{-\partial ParV_{N+2}}{\partial VarV_{N+2}} = \frac{-\partial REF_2}{\partial D_2} = -G_{ac}V_aE \tag{3.79}$$

$$C_{(N+3)(N+1)} = \frac{-\partial ParV_{N+3}}{\partial VarV_{N+1}} = \frac{-\partial P_{dev}}{\partial D_1} = -E(G_{ad}X_2 + G_{ab}X_3 + D_1G_{ab}E + X_4)$$
$$+\beta[(G_{ad}X_2 + X_4)\,\mathrm{sgn}(G_{ad}X_2(D_1 + D_2 - 1)) + (G_{ab}X_3 + D_1G_{ab}E)\,\mathrm{sgn}(D_1G_{ab}X_3)] \quad (3.80)$$
$$+2\gamma[G_{ab}^2(D_1X_3^2 + D_1^2EX_3) + G_{ad}^2((D_1 + D_2 - 1)X_2^2 + (D_1 + D_2 - 1)^2EX_2)]$$

$$C_{(N+3)(N+2)} = \frac{-\partial ParV_{N+3}}{\partial VarV_{N+2}} = \frac{-\partial P_{dev}}{\partial D_2} = -E(G_{ad}X_2 + G_{ac}X_3 + D_2G_{ac}E + X_4)$$
$$+\beta[(G_{ad}X_2 + X_4)\,\mathrm{sgn}(G_{ad}X_2(D_1 + D_2 - 1)) + (G_{ac}X_3 + D_2G_{ac}E)\,\mathrm{sgn}(D_2G_{ac}X_3)] \quad (3.81)$$
$$+2\gamma[G_{ac}^2(D_2X_3^2 + D_2^2EX_3) + G_{ad}^2((D_1 + D_2 - 1)X_2^2 + (D_1 + D_2 - 1)^2EX_2)]$$

$$T = \frac{-\partial ParV_{N+1}}{\partial VarV_{N+3}} = \frac{-\partial REF_1}{\partial E} = -D_1G_{ab}V_a \quad (3.82)$$

$$Z = \frac{-\partial ParV_{N+2}}{\partial VarV_{N+3}} = \frac{-\partial REF_2}{\partial E} = -D_2G_{ac}V_a \quad (3.83)$$

$$F = \frac{-\partial ParV_{N+3}}{\partial VarV_{N+3}} = \frac{-\partial P_{dev}}{\partial E} = -E(D_1^2G_{ab} + D_2^2G_{ac} + G_{ad}X_6) - D_1G_{ab}X_5 - D_2G_{ac}X_3 - X_7$$
$$+\beta[D_1^2G_{ab}\,\mathrm{sgn}(D_1G_{ab}X_5) + D_2^2G_{ac}\,\mathrm{sgn}(D_2G_{ac}X_3) + G_{ad}\,\mathrm{sgn}(X_7)X_6] \quad (3.84)$$
$$+2\gamma[D_1^3G_{ab}^2X_5 + D_2^3G_{ac}^2X_3 - (1 - D_1 - D_2)^3G_{ad}^2X_2]$$

$$X_1 = \frac{-\partial P_{loss,i}}{\partial VarV_j} = \begin{cases} 0, & \textit{Inj. state} \quad 1 \le i \le d, \\ \dfrac{-\partial(a_i + b_i\left|I_{th,i}\right| + c_iI_{th,i}^2)}{\partial VarV_j}, & \textit{Abs. state} \quad 1 \le j \le (N+2) \end{cases} \quad (3.85)$$

$$X_2 = [V_d - (1 - D_1 - D_2)E - V_a], \quad X_3 = (V_c + D_2E - V_a)$$
$$X_4 = -(1 - D_1 - D_2)G_{ad}E, \quad X_5 = (V_b + D_1E - V_a) \quad (3.86)$$
$$X_6 = (1 - D_1 - D_2)^2, \quad X_7 = -(1 - D_1 - D_2)G_{ad}X_2$$

The term $-k_{d,i}$ ($i = a, b, c,$ and d) is added to the diagonal arrays of the $\boldsymbol{M}$ block in case of connecting the MIDCPFC to the DCB(s).

3.5. The Solution Procedure

In this section, an 11-step SP is designed and proposed as shown in Figure 3.4 to solve DCPFPs in flexible MT-HVDC grids.

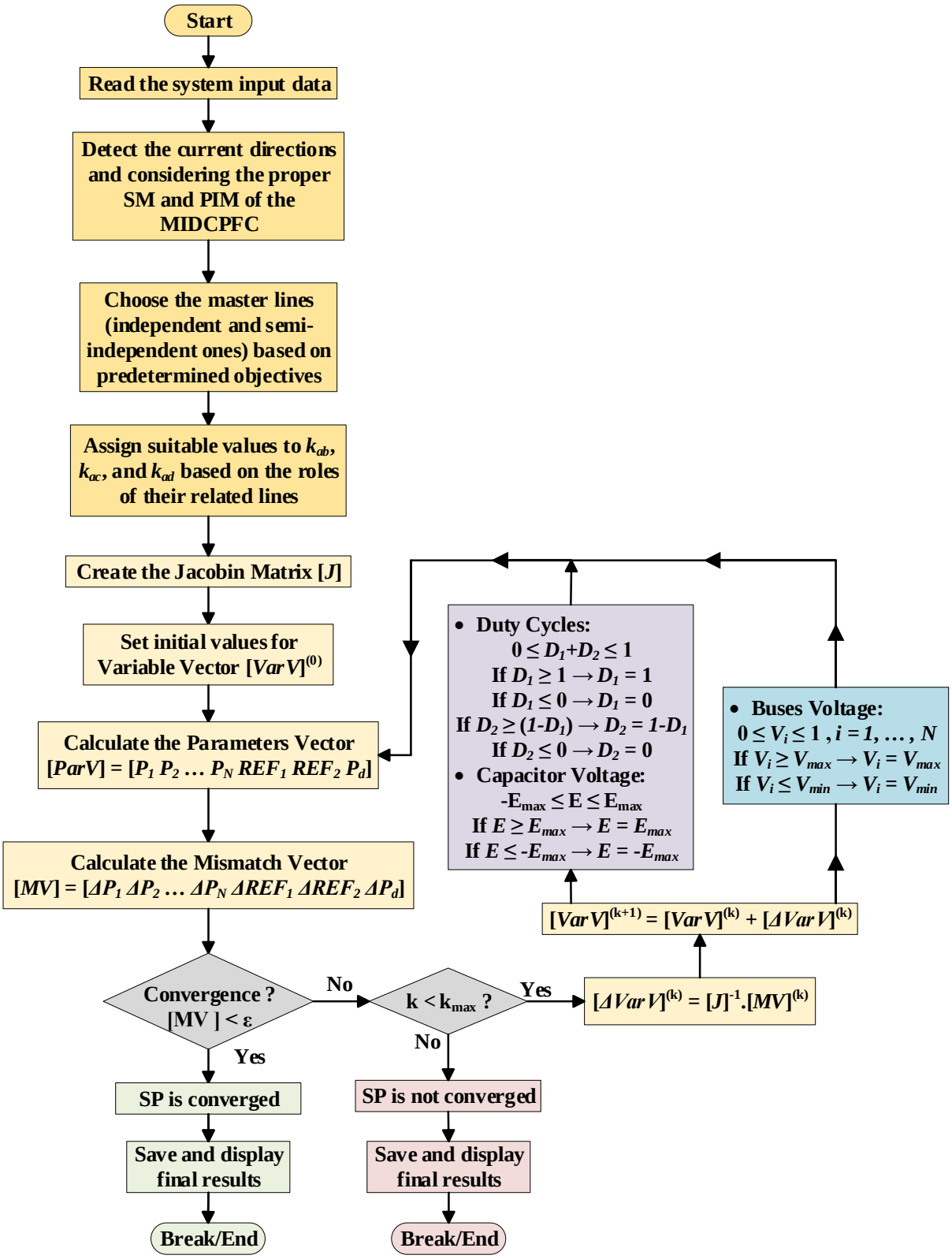

Figure 3.4. The proposed solution procedure.

The 11 steps are explained as follows:

- *Step 1*: Read the general data of the system and create its conductance matrix.
- *Step 2*: Detect the direction of currents flowing through the MIDCPFC and choose the suitable SM and PIM of the MIDCPFC according to the direction of currents.
- *Step 3*: Choose the master (independent and semi-independent) lines according to the predetermined objectives for the MIDCPFC.
- *Step 4*: Assign suitable values to k_{ab}, k_{ac}, and k_{ad} based on the role of their lines.
- *Step 5*: Create the $\boldsymbol{J}$ matrix considering the assigned variables and derived DCPFEs.
- *Step 6*: Set proper initial values for the $\boldsymbol{VarV}$ vector.
- *Step 7*: Calculate the $\boldsymbol{ParV}$ vector.
- *Step 8*: Calculate the $\boldsymbol{MV}$ vector.
- *Step 9*: Check the convergence condition considering the convergence tolerance (ε). If the convergence is not met, the iteration number (k) will be checked. If k is less than k_{max} (the maximum iteration number), $\boldsymbol{VarV}$ will be updated using (3.20)-(3.22).
- *Step 10*: Check new/updated values of $\boldsymbol{VarV}$ considering the type of variable. The bus voltage will be checked against the specific limits to be in an acceptable range ($V_{min} < V_i < V_{max}$). If the limits are violated, the bus voltage will be set to its extremum value. Also, the MIDCPFC constraints associated with the two duty cycles (D_1 and D_2) and the capacitor voltage ($\overline{E}$) will be checked against their limits. The independent duty cycle D_1 is free to be $0 < D_1 < 1$, and the semi-independent duty cycle D_2 must be between $0 < D_2 < (1 - D_1)$. The capacitor voltage must be in its acceptable range, $-E_{max} < E < E_{max}$. If these limits are violated, these parameters would be set to their extremum values. Then, the SP will be repeated from Step 7.
- *Step 11*: Display the final DC PF results.

3.6. Numerical Results

In this section, the following aspects are verified: the accuracy of the derived SMs and PIM of the MIDCPFC; the performance of the proposed NR-based DCPFS; the accuracy of the extracted

DCPFEs considering power loss equations of VSCs and the MIDCPFC; and the PF control capability of the MIDCPFC. A new meshed 15-bus MT-HVDC grid is created in this chapter to validate the proposed concepts. The simulation is conducted in MATLAB/Simulink environment.

3.6.1. A New 15-bus Flexible MT-HVDC Grid

The new 15-bus MT-HVDC grid as shown in Figure 3.5 is a symmetric monopolar network composed of 17 HVDC lines, 15 VSCs, and six OffWFs. It is created in this chapter and inspired by [21, 22]. In this grid, three DCBs (Bm-2, Bm-3, and Bm-14) are considered, which are connected to onshore VSC stations (Cm-B2, Cm-B3, and Cm-B14), and the remaining buses are CPBs. Six CPBs (Bm-5, Bm-6, Bm-7, Bm-8, Bm-10, and Bm-13) are connected to OffWFs, five CPBs (Bm-1, Bm-4, Bm-9, Bm-12, and Bm-15) are connected to the onshore side, and one CPB (Bm-11) is an intermediate bus whose net power is equal to zero. The MIDCPFC is connected in bus Bm-6 among lines L3, L5, and L8, where L3 and L5 are the master lines and L8 is the slave line. All parameters of this test grid are provided in Table 3.2.

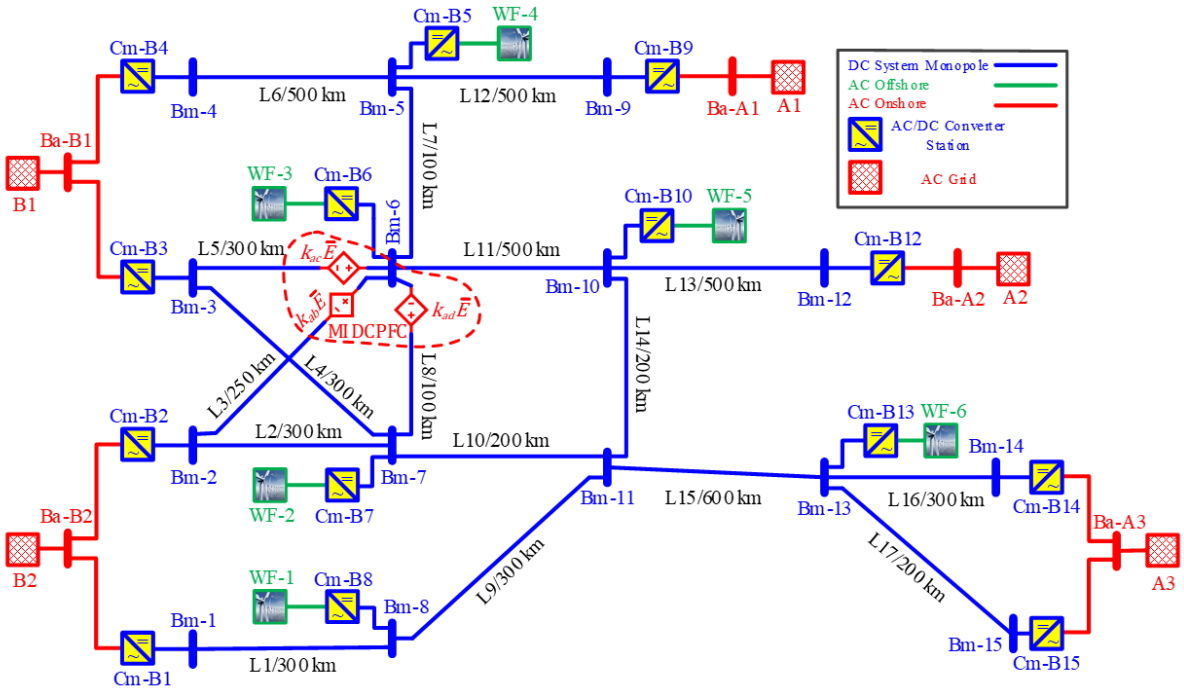

Figure 3.5. The created 15-bus MT-HVDC grid.

Table 3.2. Parameters and technical constraints of the created flexible 15-bus MT-HVDC test grid

Parameters	Values	Parameters	Values
$P_{b,DC}$	4000 (MW)	V_{min}	0.9500 (pu)
$V_{b,DC}$	800 (kV)	V_{max}	1.0500 (pu)
G_{Line}	0.48 (μs/km)	Duty Cycles	$0 \leq D_{1,2} \leq 1$
R_{Line}	0.006 (Ω/km)	α	0.001
OffWF Power Factor	0.95	β	0.006
		γ	0.008
$V_{b,ac}$	400 (kV)	a	0.007
$K_{d2,3,14}$	57.58 (pu)	b	0.0036
$V^{*}_{d2,3,14}$	0.9500 (pu)	c	0.0002
ε (Convergence Tolerance)	10^{-12}	k (Maximum Iteration)	50

3.6.2. DC PF Results

To have a proper examination of the proposed concepts in this chapter, the following four scenarios are designed:

- **Scenario A:** Performing PF on the non-compensated state of the MT-HVDC test grid under normal conditions.
- **Scenario B:** Performing PF on the non-compensated state of the MT-HVDC test grid under contingency (inability of Bm-4 in consuming power).
- **Scenario C:** Performing PF on the compensated state of the MT-HVDC test grid considering L3 as the independent and L5 as the semi-independent master lines.
- **Scenario D:** Performing PF on the compensated state of the MT-HVDC test grid considering L5 as the independent and L3 as the semi-independent master lines.

The PF results of all scenarios in per-unit (base values can be found in Table 3.2) are presented in Table 3.3.

Table 3.3. DC PF results obtained by the proposed method for all four scenarios

Case study		**Scenario A**		**Scenario B**		**Scenario C**		**Scenario D**	
Bus	Type	V	P	V	P	V	P	V	P
1	CPB	0.9994	-0.7000	1.0102	-0.7000	1.0146	-0.7000	1.0146	-0.7000
2	DCB	0.9849	-2.0103	0.9933	-2.4955	0.9928	-2.4660	0.9928	-2.4660
3	DCB	0.9836	-1.9345	0.9916	-2.3974	0.9909	-2.3534	0.9909	-2.3534
4	CPB	0.9677	-1.1000	1.0333	0.0000	1.0358	0.0000	1.0358	0.0000
5	CPB	1.0109	1.5000	1.0337	1.5000	1.0362	1.5000	1.0362	1.5000
6	CPB	1.0064	1.5000	1.0210	1.5000	1.0235	1.5000	1.0235	1.5000
7	CPB	1.0054	1.5000	1.0171	1.5000	1.0229	1.5000	1.0229	1.5000
8	CPB	1.0154	1.0000	1.0261	1.0000	1.0304	1.0000	1.0304	1.0000
9	CPB	1.0214	0.3000	1.0440	0.3000	1.0465	0.3000	1.0465	0.3000
10	CPB	1.0154	1.5000	1.0272	1.5000	1.0310	1.5000	1.0310	1.5000
11	CPB	1.0096	0.0000	1.0204	0.0000	1.0247	0.0000	1.0247	0.0000
12	CPB	0.9844	-0.8000	0.9966	-0.8000	1.0005	-0.8000	1.0005	-0.8000
13	CPB	0.9937	1.5000	0.9987	1.5000	1.0007	1.5000	1.0007	1.5000
14	DCB	0.9686	-1.0687	0.9707	-1.1918	0.9716	-1.2420	0.9716	-1.2420
15	CPB	0.9829	-0.7000	0.9879	-0.7000	0.9899	-0.7000	0.9899	-0.7000
	D_1	---		---		0.31504		0.38631	
DCPFC:	D_2	---		---		0.38631		0.31504	
	E	---		---		0.02683		0.02768	
Iteration:		5		5		10		10	
Inj.[a] Power		8.8000		8.8000		8.8000		8.8000	
Abs.[b] Power		8.3135(94.47%)		8.2848(94.15%)		8.2614(93.88%)		8.2614(93.88%)	
VSCs Loss		0.1734 (1.97%)		0.1737 (1.97%)		0.1735 (1.97 %)		0.1735 (1.97 %)	
DCPFC Loss		---		---		0.0108 (0.12%)		0.0108 (0.12%)	
Lines Loss		0.3130 (3.56%)		0.3415 (3.88%)		0.3543 (4.03%)		0.3543 (4.03%)	
Line	M.P.[c]	P	Status	P	Status	P	Status	P	Status
L1	±0.8000	0.7258	---	0.7256	---	0.7255	---	0.7255	---
L2	±1.5000	0.9198	---	1.0777	---	1.3678	---	1.3678	---
L3	±1.2000	1.1577	---	**1.5098**	**O.L.[d]**	**1.2000**	---	**1.2000**	---
L4	±1.5000	0.9786	---	1.1547	---	1.4568	---	1.4568	---
L5	±1.2000	1.0243	---	**1.3362**	**O.L.**	**1.0000**	---	**1.0000**	---
L6	±1.2000	1.1687	---	**0.0152**	**Con.[e]**	0.0153	Con.	0.0153	Con.
L7	±1.8000	0.5978	---	1.7511	---	1.7510	---	1.7510	---
L8	±1.5000	0.1350	---	0.5319	---	1.2148	---	1.2148	---
L9	±0.8000	0.2626	---	0.2628	---	0.2628	---	0.2628	---
L10	±0.8000	0.2836	---	0.2223	---	0.1299	---	0.1299	---
L11	±0.8000	0.2476	---	0.1733	---	0.2106	---	0.2106	---
L12	±0.8000	0.2917	---	0.2917	---	0.2917	---	0.2917	---
L13	±1.0000	0.8434	---	0.8429	---	0.8428	---	0.8428	---
L14	±0.8000	0.3948	---	0.4696	---	0.4323	---	0.4323	---
L15	±0.8000	0.3622	---	0.4974	---	0.5531	---	0.5531	---
L16	±1.5000	1.1125	---	1.2428	---	1.2961	---	1.2961	---
L17	±0.8000	0.7206	---	0.7205	---	0.7205	---	0.7205	---

[a] Injected [b] Absorbed [c] Maximum Power [d] Overload [e] Contingency

In Scenario A, the MT-HVDC test grid is operated in a non-compensated state under normal condition. Due to proper system references, the power transmission from the generating units (OffWFs) to the consuming units (onshore VSC stations) is achieved with all system criteria/constraints (line current and bus voltage limits) being met. Therefore, the system does not need any DCPFC, especially the MIDCPFC.

In Scenario B, the inability of VSC Cm-B4 in absorbing power leads to an overloading condition on HVDC lines, L3 and L5, forcing the whole system to change the power direction from HVDC line L6 to line L7. Therefore, the injected power at buses, Bm-5 and Bm-9, are absorbed by bus Bm-6, the extra absorbed power is then transmitted through HVDC lines, L3, L5, and L7. However, the added extra power to HVDC lines L3 and L5 exceed their limits, so an overloading condition occurs.

In Scenario C, employing the MIDCPFC has completely resolved the overloading condition of HVDC lines L3 and L5 by inserting compensating voltage sources with proper values, and thus, exchanging power from the master lines (L3 and L5) to the slave line (L8). The MIDCPFC diverts a part of the overloading power of particular (master) lines to the adjacent (slave) line without changes in power generation (especially by OffWFs) or power curtailment in other consuming units.

In Scenario D, the roles of L3 and L5 are exchanged with L3 as a semi-independent line and L5 as an independent line. The obtained results are exactly the same as those in Scenario C, which proves the accuracy of the proposed comprehensive SM, and the ability and flexibility of the proposed DCPFS and solution procedure in solving a DCPFP when the role of the compensated lines and their duty cycles are changed.

The PF results of Table 3.3 reveal the effective application of the MIDCPFC and its superior PF control capability in controlling PF of the particular (master) HVDC lines simultaneously, and providing a decent operating point for the whole grid with practical constraints. The PF results also reveal that the proposed DCPFS possesses the superior convergence property as it has converged in 10 iterations and less. This proves that all derived DCPFEs and power loss equations are correct and embedded properly in the whole system’s DCPFEs and the proposed DCPFS.

Furthermore, the results prove that the proposed DCPFS is an effective and practical solver to solve DCPFPs of highly meshed flexible MT-HVDC grids.

3.7. Conclusion

In this chapter, a novel Newton-Raphson-based DCPFS is proposed to solve the DCPFP in highly meshed MT-HVDC grids compensated by a MIDCPFC. The SMs and PIM of the MIDCPFC are proposed to tackle shortcomings in the literature. For precise modeling, power loss of the MIDCPFC is modeled/formulated for the first time. The proposed power loss model can be used for other voltage-source-based DCPFCs. A new highly meshed 15-bus MT-HVDC test grid is created for validation, and four scenarios are tested. The results prove accuracy of the proposed SMs and PIM of the MIDCPFC, the effective embedding of the derived models in general DCPFEs of the system, and the proper performance of the proposed NR-based DCPFS.

3.8. References

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4. A Sequential Algorithm to Solve Power Flow in MT-HVDC Grids Compensated by Multiport Interline DC Power Flow Controllers

4.1. Abbreviation

CDCPFC	Cascaded DC power flow controller
CPB	Constant power bus
DCB	Droop controlled bus
DCOPF	DC optimal power flow
DCPF	DC power flow
DCPFC	DC power flow controller
DCPFE	DC power flow equation
DCPFP	DC power flow problem
DCPFS	DC power flow solver
FACTS	Flexible AC transmission system
IDCPFC	Interline DC power flow controller
KVL	Kirchhoff's voltage law
MIDCPFC	Multiport interline DC power flow controller
MT-HVDC	Multi-terminal HVDC
NR	Newton-Raphson
OffWF	Offshore wind farm
PF	Power flow
PIM	Power injection model
SDCPFC	Series DC power flow controller
SM	Static model
SP	Solution procedure
VSC	Voltage source converter

4.2. Introduction

Over/under-utilization of HVDC lines may occur in highly meshed VSC-based MT-HVDC grids due to various factors, such as maintenance, outages and other contingencies [1, 2]. To improve static security of the entire system, integrating DCPFCs into MT-HVDC grids is an effective solution [3, 4]. Multiple IDCPFCs may be installed and selectively operated to enhance static security [5, 6]. Although this proposed concept has several benefits, it poses challenges when using standard unified algorithms due to frequent changes in variables, DCPFEs, and the Jacobin matrix of a MT-HVDC system.

Refs [7, 8] discussed issues related to DCOPF and DCPF in MT-HVDC grids, and considered integrating DCPFCs a solution to improve control flexibility, PF optimization and static security. IDCPFCs [5, 9-12] have gained more attentions as they use fewer semiconductors, are more reliable and economical. In IDCPFCs, the voltage stress on components, such as IGBTs, is limited to a small fraction of the rated system voltage, and isolation transformers are not usually needed. More research on DCPF studies with IDCPFCs is reported in the literature than with other DCPFCs. A new DCPFC, known as “the multiport interline DC power flow controller (MIDCPFC)”, has been created, which can control more than two HVDC lines simultaneously and independently/semi-independently.

Recently, DCPFCs have been integrated into DCOPF and DCPF problems, and a coordination philosophy has been established between static control of DC/AC converters and DCPFCs [13, 14]. Two unified algorithms are proposed in [15-19] to integrate an IDCPFC with the DCPFP. In [15-19], the impact of insertion of a single IDCPFC has been modeled using the NR-based DCPF algorithm by employing its PIM and artificially injected power. However, the presence of the IDCPFC and the adoption of unified algorithms have resulted in alterations to the Jacobian matrix of a HVDC grid. Consequently, DCPFEs of the system are affected in three major ways, which are elaborated as follows:

- Adding nonlinear terms in the net injected power to buses of the system due to PF models for IDCPFCs. These nonlinear terms are functions of duty cycles of IDCPFCs and voltages of the buses, to which lines are connected.

- Adding a new equation governing control objectives of IDCPFCs (e.g., regulation of the current and power of master HVDC lines).
- Introducing a new PF variable, i.e., duty cycle of IDCPFC.

The complexity of a system will increase if its limits are enforced with a constrained DCPFP. As control objectives of IDCPFCs might change frequently to constrain system variables within their feasible ranges, the Jacobin matrix will be altered. Consequently, the implementation complexity of the unified DCPF algorithm would increase.

There will be further complexity and computational burden if several DCPF models exist and operate selectively because each DCPFC introduces new nonlinear PF models, new control objectives, variables, and constraints to the DCPFP [5, 6]. The root cause of these technical challenges is the adoption of unified algorithms (rather than sequential algorithms), which solve the system equations simultaneously without ensuring appropriate decoupling between equations of DCPFCs and rest of the MT-HVDC grid.

According to previous studies, sequential algorithms have been employed to solve the AC/DC problem or AC PF problem with FACTSs [20, 21]. Contrary to unified algorithms [21], sequential algorithms do not change the Jacobin matrices, equations, or variables for both AC and DC systems, and do not require calculating a combined AC/DC or AC/FACTS Jacobin matrix [22]. Therefore, sequential algorithms facilitate the integration of DC or FACTS components into existing AC power flow scripts/software. In [23], a relaxation method has been proposed to develop a DCOPF problem that is convex, computationally efficient and suits the quadratic programming approach. A sequential penalization method is introduced to the relaxed AC/DC optimal power flow problem to enforce technical constraints associated with the interlinked DC/AC VSC located between AC and DC microgrids, and develop a security-constrained AC/DC optimal power flow problem. However, to the best of the author's knowledge, sequential algorithms have not been used to solve the PF problem of DCPFCs within a VSC-HVDC grid. To address this research gap, in this paper, a sequential algorithm is proposed to address the DCPFP of VSC-HVDC grids compensated by one DCPFC. The DCPFC under consideration is the recently proposed MIDCPFC, a sophisticated device in the IDCPFC family.

This chapter aims to develop an accurate, easy-to-implement sequential DCPF algorithm for MT-HVDC grids with the MIDCPFC. The main contribution is to decouple equations governing the MT-HVDC grid and equations for the MIDCPFC, and solve them sequentially. In the proposed sequential DCPF algorithm, DCPFEs of the uncompensated MT-HVDC grid will be solved using the NR method in the first sequence, where the MIDCPFC is modeled using constant PIMs in the mismatch vector. Therefore, the original system's equations, symmetric conductance matrix, variables vector, and Jacobin matrix will favorably remain intact. Computed/updated variables, which are voltages of the system, will be transferred to the second sequence, where physical/control equations of the MIDCPFC will be solved to compute the variables, which are the duty cycle and voltage of their intermediary capacitor, and update the value of PIMs. The sequential DCPF algorithm will iterate through the first and second sequences until meeting the pre-defined convergence criteria to achieve control objectives of the MIDCPFC. The proposed sequential algorithm can be implemented easily by extending DCPF scripts of the uncompensated MT-HVDC grid.

4.3. MIDCPFC Modeling

The MIDCPFC used in Chapter 3 is also used here. Hence, all the obtained results for its modeling are valid, and will be used in this paper.

A circuit schematic of the MIDCPFC used in this study is illustrated in Figure 3.1, and its basic SM are derived using (3.1)-(3.2) in Section 3.3.1. Based on the basic SM, a comprehensive SM of the MIDCPFC has been proposed in Section 3.3.2, which includes its general schematic (Figure 3.2) and different conducting states (Table 3.1). The results in Section 3.3.2 are used here. The process of extracting PIM of the MIDCPFC is mentioned in Section 3.3.3, which is valid here. For the ease of study, the schematic and equations of the PIM for MIDCPFCs are provided in Figure 4.1 and (4.1)-(4.6), respectively.

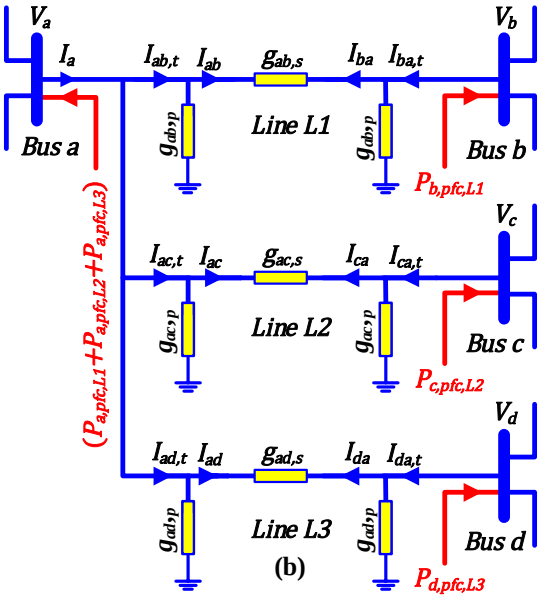

Figure 4.1. The PIM for the MIDCPFC.

$$P_{ab,t} = V_a I_{ab,t} = (g_{ab,p} + g_{ab,s})V_a^2 - V_a g_{ab,s} V_b - \underbrace{V_a g_{ab,s} D_1 \overline{E}}_{P_{a,pfc,L1}} \tag{4.1}$$

$$P_{ba,t} = V_b I_{ba,t} = (g_{ab,p} + g_{ab,s})V_b^2 - V_b g_{ab,s} V_a - \underbrace{(-V_b g_{ab,s} D_1 \overline{E})}_{P_{b,pfc,L1}} \tag{4.2}$$

$$P_{ac,t} = V_a I_{ac,t} = (g_{ac,p} + g_{ac,s})V_a^2 - V_a g_{ac,s} V_c - \underbrace{V_a g_{ac,s} D_2 \overline{E}}_{P_{a,pfc,L2}} \tag{4.3}$$

$$P_{ca,t} = V_c I_{ca,t} = (g_{ac,p} + g_{ac,s})V_c^2 - V_c g_{ac,s} V_a - \underbrace{(-V_c g_{ac,s} D_2 \overline{E})}_{P_{c,pfc,L2}} \tag{4.4}$$

$$P_{ad,t} = V_a I_{ad,t} = (g_{ad,p} + g_{ad,s})V_a^2 - V_a g_{ad,s} V_d - \underbrace{(-V_a g_{ad,s}(1 - D_1 - D_2)\overline{E})}_{P_{a,pfc,L3}} \tag{4.5}$$

$$P_{da,t} = V_d I_{da,t} = (g_{ad,p} + g_{ad,s})V_d^2 - V_d g_{ad,s} V_a - \underbrace{(V_d g_{ad,s}(1 - D_1 - D_2)\overline{E})}_{P_{d,pfc,L3}} \tag{4.6}$$

Where g , V , and I represent conductances, voltages, and currents, respectively. Also, $P_{a,pfc,L1}$, $P_{a,pfc,L2}$, $P_{a,pfc,L3}$, $P_{b,pfc,L1}$, $P_{c,pfc,L2}$, $P_{d,pfc,L3}$ are DCPFEs related to the MIDCPFC.

4.4. DC Power Flow Equations of Flexible MT-HVDC Grids

In this section, DCPFEs are derived for the MIDCPFC compensated (flexible) MT-HVDC grids by considering power losses of VSCs and the MIDCPFC in the system, and a novel sequential DCPFS is proposed to solve the DCPFP.

4.4.1. Power Loss Equations of the MIDCPFC and VSCs

The novel sequential DCPFS begins with deriving power loss equations of the MIDCPFC and VSCs, as derived in Section 3.4.1. For the ease of study, the MIDCPFC and VSCs loss equations are given as (4.7) and (4.9), respectively.

$$\begin{aligned} &P_{loss,PFC} = (D_1 I_{ab} + D_2 I_{ac} - (1 - D_1 - D_2) I_{ad})\overline{E} = \alpha + \beta[|D_1 I_{ab}| + |D_2 I_{ac}| + |(1 - D_1 - D_2) I_{ad}|] \\ &+\gamma[(D_1 I_{ab})^2 + (D_2 I_{ac})^2 + ((1 - D_1 - D_2) I_{ad})^2] \\ &I_{ab} = (V_a - D_1 \overline{E} - V_b) g_{ab,s},\ I_{ac} = (V_a - D_2 \overline{E} - V_c)\, g_{ab,s},\quad I_{ad} = (V_a + (1 - D_1 - D_2)\overline{E} - V_d) g_{ad,s} \end{aligned} \tag{4.7}$$

Where V_a, V_b, V_c, and V_d are voltages of the buses connected to the MIDCPFC. $\overline{E}$ is the intermediate capacitor voltage. α is the no-load loss. β and γ are linear and quadratic dependency of the loss of the MIDCPFC due to the current flowing through it, respectively.

The general power of the MIDCPFC is computed in (4.8).

$$\begin{aligned} &P_{dev} = (D_1 I_{ab} + D_2 I_{ac} - (1 - D_1 - D_2) I_{ad})\overline{E} - [\alpha + \beta[|D_1 I_{ab}| + |D_2 I_{ac}| + |(1 - D_1 - D_2) I_{ad}|] \\ &+\gamma[(D_1 I_{ab})^2 + (D_2 I_{ac})^2 + ((1 - D_1 - D_2) I_{ad})^2]] \end{aligned} \tag{4.8}$$

The power losses of VSCs can be modeled in (4.9).

$$P_{loss,VSC} = a + b|I_{th}| + cI_{th}^2 \tag{4.9}$$

Where a represents no-load converter losses. b and c are two constant coefficients representing linear and quadratic dependency of the loss of the VSC due to the current flowing through it in injecting/absorbing states, respectively. I_{th} is the sum of currents of all lines connected to the VSC in the power-absorbing state. I_{th} can also be computed by (4.10) in the power-injecting state [24].

$$I_{th} = \frac{P_{Injection}}{pf\sqrt{3}V_{ac}} \tag{4.10}$$

Where $P_{Injection}$ is the injected power from the generation unit (e.g. offshore WPPs) to the VSC. pf and V_{ac} are the power factor and AC voltage of the generation unit, respectively.

4.4.2. DCPFEs of DC Buses

DCPFEs of DC Buses are examined in Section 3.4.2. For the ease of study, they are given in this section as (4.11)-(4.13) with the same assumptions. The DCPFE of CPBs considering the VSC's power losses is derived in (4.11).

$$P_i = P_{Gi} - P_{Li} = V_i I_i = V_i \sum_{j=1}^{N} (G_{ij} V_j) + P_{loss,i},\ i, j = 1, ..., N \tag{4.11}$$

Where P_i, I_i, $P_{Li}, P_G, P_{loss,i}$, and V_i are the net power, the current injected to bus i, the power of the load, the power of generating unit, the power loss of the VSC, and the voltage of bus i, respectively. $\boldsymbol{G}$ symbolizes the system's conductance matrix in (4.12), in which $g_{ij,s}$ and $g_{ij,p}$ are series and parallel conductances of HVDC lines, respectively.

$$\boldsymbol{G} = [G_{ij}],\ G_{ij} = -g_{ij,s},\ G_{ii} = \sum_{j=1}^{N} (g_{ij,s} + g_{ij,p}),\ i, j = 1, ..., N \tag{4.12}$$

The DCPFE of DCBs considering the VSC's power losses is derived in (4.13).

$$P_i = V_i I_i = -k_{d,i}(V_i - V_i^*) = V_i \sum_{j=1}^{N} (G_{ij} V_j) + P_{loss,i},\ i, j = 1, ..., N \tag{4.13}$$

Where V_i^* and $k_{d,i}$ are the droop voltage reference and the droop gain, respectively.

4.4.3. The Proposed Sequential DCPFS

The proposed DCPFS is a sequential-based algorithm, which is comprised of two main sections: 1) Sequence One - Grid Sequence 2) Sequence Two - DCPFC Sequence. The proposed sequential DCPFS can decouple equations of the DCPFC and equations of the grid to keep the grid's Jacobin matrix intact without requiring any modifications.

The present of DCPFCs and their off and on status can impose various modifications in the grid's Jacobin matrix, leading to complicated equations. As mentioned in Section 4.3, variables of the MIDCPFC exist in DCPFEs. Hence, at the first glance, it seems that decoupling the grid variables

from the MIDCPFC variables is not possible, but there is a solution to this challenge. The solution is inspired from the same studies on decoupling FACTS devices in AC grids and AC/DC systems, where the terms related to FACTS devices or DC systems are treated as constant values, so PF equations of AC grids can be decoupled from other variables. The same process can be applied here to decouple variables of the MT-HVDC grid and the MIDCPFC with the MIDCPFC-related terms treated as constant values. The whole process of solving DCPFEs will be explained in the following sections. The two sequences are based on the NR concept, and their equations are solved through an iterative procedure.

4.4.3.1. Sequence One - Grid Sequence

The grid sequence is designed to solve DCPFEs related solely to the grid variables, voltages of the buses. Therefore, only grid variables are used in this sequence, while all variables from both the grid and MIDCPF are used in the unified algorithm in Chapter 3. The general process of solving DCPFEs in the grid sequence is given by (4.14)-(4.26). Similar to the structure proposed in Chapter 3, its structure is made by three matrices: the variable vector ($\boldsymbol{VarV}_g$), the mismatch vector ($\boldsymbol{MV}_g$), and the Jacobin matrix ($\boldsymbol{J}_g$).

$$\boldsymbol{VarV_g} = [V_1 \ ... \ V_N]^T \tag{4.14}$$

$$\boldsymbol{ParV_g} = [P_1 \ ... \ P_N]^T \tag{4.15}$$

$$\boldsymbol{MV_g} = [\Delta P_1 \ ... \ \Delta P_N]^T \tag{4.16}$$

$$\Delta P_i = P_i^* - P_i, \ i = 1, ..., N \tag{4.17}$$

$$[\boldsymbol{J_g}].[\Delta \boldsymbol{VarV_g}] = [\boldsymbol{MV_g}] \tag{4.18}$$

$$[\Delta \boldsymbol{VarV_g}]^k = ([\boldsymbol{J_g}]^k)^{-1}.[\boldsymbol{MV_g}]^k \tag{4.19}$$

$$[\boldsymbol{VarV_g}]^{k+1} = [\boldsymbol{VarV_g}]^k + [\Delta \boldsymbol{VarV_g}]^k \tag{4.20}$$

Where P_i^* is the reference/predetermined value of the power of bus i. k is the iteration number. The predetermined value of DCBs is equal to $k_{d,i}V_i^*$.

Similar to Chapter 3, N_p buses are CPBs, N_d buses are DCBs ($N = N_d + N_p$), and it is assumed that buses a, b, c, and d are connected to the MIDCPFC that can be any combination of CPBs

and/or DCBs. Without loss of generality, they are assumed to be CPBs. Accordingly, the following numbering order of the buses is considered to facilitate deriving the $\boldsymbol{J}_g$ matrix.

$$1<...<N_d<f<...<m<a<b<c<d,\ f=N_d+1,\ m=N_d+N_p-4,\ d=N \tag{4.21}$$

The triple constituent matrices of the grid sequence are expressed as follows:

$$\left[\boldsymbol{J}_g\right]= \begin{array}{c} \\ 1 \\ \vdots \\ \vdots \\ N_d \\ f \\ \vdots \\ m \\ \\ a \\ b \\ c \\ d \end{array} \begin{array}{c} \begin{array}{cccccccccc} 1 & \cdots & \cdots & N_d & f & \cdots & m & a & b & c & d \end{array} \\ \left[\begin{array}{cccccccccc} & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & H & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \\ & & & & & & & & & & \end{array}\right] \end{array} \tag{4.22}$$

$$[\Delta \boldsymbol{VarV}_g]=[\underbrace{\Delta V_1..\Delta V_{N_d}}_{N_d\ buses}\underbrace{\Delta V_f..\Delta V_m\Delta V_a\Delta V_b\Delta V_c\Delta V_d}_{N_p\ buses}\ ] \tag{4.23}$$

$$[\boldsymbol{MV}_g]=[\underbrace{\Delta P_1..\Delta P_{N_d}}_{N_d\ buses}\underbrace{\Delta P_f..\Delta P_m\Delta P_a\Delta P_b\Delta P_c\Delta P_d}_{N_p\ buses}\ ] \tag{4.24}$$

Accordingly, the $\boldsymbol{J}_g$ matrix can be computed by (4.25) and (4.26):

$$H_{ij}=\frac{-\partial ParV_{g\,i}}{\partial VarV_{g\,j}}=\begin{cases} -G_{ij}V_i+X_1 & ,1\le i\le d\ ,1\le j\le d\ ,i\ne j \\ -\sum_{j=f,\,j\ne i}^{m}(G_{ij}V_j)-2G_{ij}V_i+X_1 & ,f\le i=j\le d \\ -\sum_{j=1,\,j\ne i}^{N_d}(G_{ij}V_j)-2G_{ij}V_i-k_{d,i}+X_1 & ,1\le i=j\le N_d \end{cases} \tag{4.25}$$

$$X_1=\frac{-\partial P_{loss,i}}{\partial VarV_{g\,j}}=\begin{cases} 0 \quad , \textit{Inj. state} & 1\le i\le d, \\ \dfrac{-\partial(a_i+b_i\left|I_{th,i}\right|+c_i I_{th,i}^2)}{\partial VarV_{g\,j}}, \textit{Abs. state} & 1\le j\le d \end{cases} \tag{4.26}$$

4.4.3.2. Sequence Two - DCPFC Sequence

The DCPFC sequence is designed to solve DCPFEs related solely to variables of the DCPFC, the voltage of the intermediate capacitor and the duty cycle. In this study, only variables of the MIDCPFC exist in this sequence, while all variables for both grid and MIDCPFC are used in the unified algorithm in Chapter 3. The general process of solving DCPFEs of the DCPFC sequence is given by (4.27)-(4.51). Its structure is made by three matrices: the variable vector ($\boldsymbol{VarV}_{pfc}$), the mismatch vector ($\boldsymbol{MV}_{pfc}$), and the Jacobin matrix ($\boldsymbol{J}_{pfc}$).

$$\boldsymbol{VarV}_{pfc}=[D_1\ \ D_2\ \ E]^T \tag{4.27}$$

$$\boldsymbol{ParV}_{pfc}=[REF_1\ \ REF_2\ \ P_{dev}]^T \tag{4.28}$$

$$\boldsymbol{MV}_{pfc}=[\Delta REF_1\ \ \Delta REF_2\ \ \Delta P_{dev}]^T \tag{4.29}$$

$$\Delta REF_n=REF_n^*-REF_n,\ n=1,2,\quad \Delta P_{dev}=P_{dev}^*-P_{dev} \tag{4.30}$$

$$[\boldsymbol{J}_{pfc}].[\Delta\boldsymbol{VarV}_{pfc}]=[\boldsymbol{MV}_{pfc}] \tag{4.31}$$

$$[\Delta\boldsymbol{VarV}_{pfc}]^k=([\boldsymbol{J}_{pfc}]^k)^{-1}.[\boldsymbol{MV}_{pfc}]^k \tag{4.32}$$

$$[\boldsymbol{VarV}_{pfc}]^{k+1}=[\boldsymbol{VarV}_{pfc}]^k+[\Delta\boldsymbol{VarV}_{pfc}]^k \tag{4.33}$$

Where REF and REF^* are parameters that must be controlled in the system, e.g., the power flowing through a HVDC line, and their predetermined values, respectively. k is the iteration number.

Three MIDCPFC's variables (degree of freedom), D_1, D_2, and E, are placed at the end of $\boldsymbol{VarV}_{pfc}$. Also, the parameters REF_1, REF_2, and P_{dev} are the added control objectives in $\boldsymbol{MV}_{pfc}$. The parameter E is inherently a dependent variable and is the function of V_a, V_b, V_c, V_d, D_1 and D_2 [25], but it can be treated as an independent variable as long as P_{dev} is satisfied. Therefore, the system can enjoy one extra freedom degree, E. REF can be any arbitrary system's parameter, such as

the current or the power of any HVDC line, to be controlled, which provides a multi-control objective feature for the proposed sequential DCPFS. The following parameters can be chosen as REF_1 and REF_2:

- *The transferred power to the energy-hub of the MIDCPFC:*

$$P_{PFCm}=\begin{cases} D_1\overline{E}I_{ab}=D_1\overline{E}(V_a-D_1\overline{E}-V_b)g_{ab,s}, \ \ Line \ \ L1 \\ D_2\overline{E}I_{ac}=D_2\overline{E}(V_a-D_2\overline{E}-V_c)g_{ac,s}, \ \ Line \ \ L2 \end{cases} \tag{4.34}$$

- *The power flowing through the master HVDC lines:*

$$P_{L1}=V_aI_{ab}=V_a(V_b+D_1\overline{E}-V_a)G_{ab}, \ \ Line \ \ L1 \tag{4.35}$$

$$P_{L2}=V_aI_{ac}=V_a(V_c+D_2\overline{E}-V_a)G_{ac}, \ \ Line \ \ L2 \tag{4.36}$$

- *The current flowing through the master HVDC lines:*

$$I_{L1}=I_{ab}=(V_b+D_1\overline{E}-V_a)G_{ab}, \ \ Line \ \ L1 \tag{4.37}$$

$$I_{L2}=I_{ac}=(V_c+D_2\overline{E}-V_a)G_{ac}, \ \ Line \ \ L2 \tag{4.38}$$

Lines L_1 and L_2 are the master lines with independent duty cycles of the MIDCPFC, D_1 and D_2. Line L_3 is the slave line with a dependent duty cycle of the MIDCPFC, $(1-D_1-D_2)$. The power flowing through the master lines is the control objective parameter.

The triple constituent matrices of the DCPFC sequence are expressed as follows:

$$\left[\boldsymbol{J}_{pfc}\right]= \begin{array}{c} \\ 1 \\ 2 \\ 3 \end{array} \begin{array}{c} \begin{array}{ccc} 1 & 2 & 3 \end{array} \\ \begin{bmatrix} & & \\ & S & \\ & & \end{bmatrix} \end{array} \tag{4.39}$$

$$[\Delta \boldsymbol{Var V}_{pfc}]=[\underbrace{\Delta D_1 \Delta D_2}_{added} \underbrace{\Delta E}_{\text{var.}}] \tag{4.40}$$

$$[\boldsymbol{MV}_{pfc}]=[\underbrace{\Delta REF_1 \Delta REF_2}_{added} \underbrace{\Delta P_{dev}}_{\text{var.}}] \tag{4.41}$$

Accordingly, the $\boldsymbol{J}_{pfc}$ matrix can be computed by (4.42)-(4.51):

$$S_{11} = \frac{-\partial ParV_{pfc1}}{\partial VarV_{pfc1}} = \frac{-\partial REF_1}{\partial D_1} = -G_{ab}V_a E \tag{4.42}$$

$$S_{12} = \frac{-\partial ParV_{pfc1}}{\partial VarV_{pfc2}} = \frac{-\partial REF_1}{\partial D_2} = 0 \tag{4.43}$$

$$S_{21} = \frac{-\partial ParV_{pfc2}}{\partial VarV_{pfc1}} = \frac{-\partial REF_2}{\partial D_1} = 0 \tag{4.44}$$

$$S_{22} = \frac{-\partial ParV_{pfc2}}{\partial VarV_{pfc2}} = \frac{-\partial REF_2}{\partial D_2} = -G_{ac}V_a E \tag{4.45}$$

$$\begin{aligned} S_{31} &= \frac{-\partial ParV_{pfc3}}{\partial VarV_{pfc1}} = \frac{-\partial P_{dev}}{\partial D_1} = -E(G_{ad}X_2 + G_{ab}X_3 + D_1 G_{ab}E + X_4) \\ &+\beta[(G_{ad}X_2 + X_4)\,\mathrm{sgn}(G_{ad}X_2(D_1 + D_2 - 1)) + (G_{ab}X_3 + D_1 G_{ab}E)\,\mathrm{sgn}(D_1 G_{ab}X_3)] \\ &+2\gamma[G_{ab}^2(D_1 X_3^2 + D_1^2 E X_3) + G_{ad}^2((D_1 + D_2 - 1)X_2^2 + (D_1 + D_2 - 1)^2 E X_2)] \end{aligned} \tag{4.46}$$

$$\begin{aligned} S_{32} &= \frac{-\partial ParV_{pfc3}}{\partial VarV_{pfc2}} = \frac{-\partial P_{dev}}{\partial D_2} = -E(G_{ad}X_2 + G_{ac}X_3 + D_2 G_{ac}E + X_4) \\ &+\beta[(G_{ad}X_2 + X_4)\,\mathrm{sgn}(G_{ad}X_2(D_1 + D_2 - 1)) + (G_{ac}X_3 + D_2 G_{ac}E)\,\mathrm{sgn}(D_2 G_{ac}X_3)] \\ &+2\gamma[G_{ac}^2(D_2 X_3^2 + D_2^2 E X_3) + G_{ad}^2((D_1 + D_2 - 1)X_2^2 + (D_1 + D_2 - 1)^2 E X_2)] \end{aligned} \tag{4.47}$$

$$S_{13} = \frac{-\partial ParV_{pfc1}}{\partial VarV_{pfc3}} = \frac{-\partial REF_1}{\partial E} = -D_1 G_{ab}V_a \tag{4.48}$$

$$S_{23} = \frac{-\partial ParV_{pfc2}}{\partial VarV_{pfc3}} = \frac{-\partial REF_2}{\partial E} = -D_2 G_{ac}V_a \tag{4.49}$$

$$\begin{aligned} S_{33} &= \frac{-\partial ParV_{pfc3}}{\partial VarV_{pfc3}} = \frac{-\partial P_{dev}}{\partial E} = -E(D_1^2 G_{ab} + D_2^2 G_{ac} + G_{ad}X_6) - D_1 G_{ab}X_5 - D_2 G_{ac}X_3 - X_7 \\ &+\beta[D_1^2 G_{ab}\,\mathrm{sgn}(D_1 G_{ab}X_5) + D_2^2 G_{ac}\,\mathrm{sgn}(D_2 G_{ac}X_3) + G_{ad}\,\mathrm{sgn}(X_7)X_6] \\ &+2\gamma[D_1^3 G_{ab}^2 X_5 + D_2^3 G_{ac}^2 X_3 - (1 - D_1 - D_2)^3 G_{ad}^2 X_2] \end{aligned} \tag{4.50}$$

$$\begin{aligned} &X_2 = [V_d - (1 - D_1 - D_2)E - V_a], \quad X_3 = (V_c + D_2 E - V_a), \quad X_4 = -(1 - D_1 - D_2)G_{ad}E \\ &X_5 = (V_b + D_1 E - V_a), \quad X_6 = (1 - D_1 - D_2)^2, \quad X_7 = -(1 - D_1 - D_2)G_{ad}X_2 \end{aligned} \tag{4.51}$$

Compared to equations (3.16)-(3.86) in Chapter 3, (4.14)-(4.51) are more straightforward with fewer equations for the sequential DCPFS, and the original Jacobin matrix of the system (J_g) is kept intact.

4.5. The Solution Procedure (SP)

In this section, a SP is designed and proposed to solve DCPFPs in flexible MT-HVDC grids. The process of solving a DCPFP is based on solving DCPFEs in each sequence, and the output of each sequence is used as the input for the other sequence. The MIDCPFC-related terms, $P_{a,pfc,L1}$, $P_{a,pfc,L2}$, $P_{a,pfc,L3}$, $P_{b,pfc,L1}$, $P_{c,pfc,L2}$, $P_{d,pfc,L3}$ in (4.1)-(4.6), are treated as constant values, and they are known as "MIDCPFC constant values." In the grid sequence, inputs are the MIDCPFC constant values and initial values for the grid variables; and its outputs are the grid variables, i.e., the voltage of buses which are obtained after convergence in the grid sequence. In the DCPFC sequence, the inputs are the outputs of the grid sequence (i.e., the voltage of buses) and initial values of the MIDCPFC variables, D_1, D_2, and $\overline{E}$, and its outputs are the MIDCPFC variables, i.e., the duty cycles and voltage of intermediate capacitor which are obtained after convergence in the DCPFC sequence. The outputs of the DCPFC sequence are used as the primary input to update the MIDCPFC constant values in the grid sequence. In this way, an iterative sequential method is formed to solve the DCPFP in flexible MT-HVDC grids. Based on the mentioned concepts, a SP is proposed in Figure 4.2.

The steps of the proposed SP are explained as follows:

- *Step 1*: Read the general data of the system and create its conductance matrix.
- *Step 2*: Detect the direction of currents flowing through the MIDCPFC and choose the suitable SM and PIM of the MIDCPFC according to the direction of currents.
- *Step 3*: Choose the master (independent and semi-independent) lines according to the predetermined objectives for the MIDCPFC.
- *Step 4*: Assign suitable variables to k_{db}, k_{ac}, and k_{ad} based on the role of their lines.
- *Step 5*: Create the $\boldsymbol{J}$ matrices for both grid and DCPFC sequences considering the assigned variables and derived DCPFEs.
- *Step 6*: The grid sequence begins in Step 6 by setting initial values for the $\boldsymbol{VarV}_g$ vector.
- *Step 7*: The MIDCPFC converted results of Step 18 are used to update the MIDCPFC constant values (note: initial values are assumed for MIDCPFC variables at the beginning to start the algorithm).
- *Step 8*: Calculate the $\boldsymbol{ParV}_g$ vector.

- *Step 9*: Calculate the $\boldsymbol{MV}_g$ vector.
- *Step 10*: Check the convergence condition considering the convergence tolerance (ε). If the convergence condition is not met, the iteration number (k_g) will be checked. If k_g is less than $k_{\max}$ (the maximum iteration number), $\boldsymbol{VarV}_g$ will be updated using (4.18)-(4.20).
- *Step 11*: Check the new/updated values of $\boldsymbol{VarV}_g$. The bus voltage will be checked against the specific limits to be in an acceptable range ($V_{\min} < V_i < V_{\max}$). If the limits are violated, the bus voltage will be set to its extremum value. Then, the MIDCPFC constants are updated considering the updated bus voltages, and the SP will be repeated from Step 8.
- *Step 12*: The converged results will be sent to the next step after sufficient iterations.
- *Step 13*: The DCPFC sequence begins by setting initial values for the $\boldsymbol{VarV}_{pfc}$ vector. The obtained converged results of the grid sequence are used in the DCPFC sequence.
- *Step 14*: Calculate the $\boldsymbol{ParV}_{pfc}$ vector.
- *Step 15*: Calculate the $\boldsymbol{MV}_{pfc}$ vector.
- *Step 16*: Check the convergence condition considering the convergence tolerance (ε). If the convergence condition is not met, the iteration number (k_p) will be checked. If k_p is less than $k_{\max}$ (the maximum iteration number), $\boldsymbol{VarV}_{pfc}$ will be updated using (4.31)-(4.33).
- *Step 17*: Check the new/updated values of $\boldsymbol{VarV}_{pfc}$. The MIDCPFC constraints associated with the two duty cycles (D_1 and D_2) and the capacitor voltage ($\overline{E}$) will be checked against their limits. The independent duty cycle D_1 is free to be $0 < D_1 < 1$, and the semi-independent duty cycle D_2 must be between $0 < D_2 < (1 - D_1)$. The capacitor voltage must be in its acceptable range, $-E_{\max} < E < E_{\max}$. If these limits are violated, these parameters would be set to their extremum values. Then, the SP will be repeated from Step 13.

Step 18: The converged results will be saved. If both values of k_g and k_p are equal to one, the final results will be saved and displayed as it means the obtained/updated grid and MIDCPFC variables can meet the predetermined objectives. That is to say, the DCPFP is solved. Otherwise, the converged results of the DCPFC sequence are sent to the grid

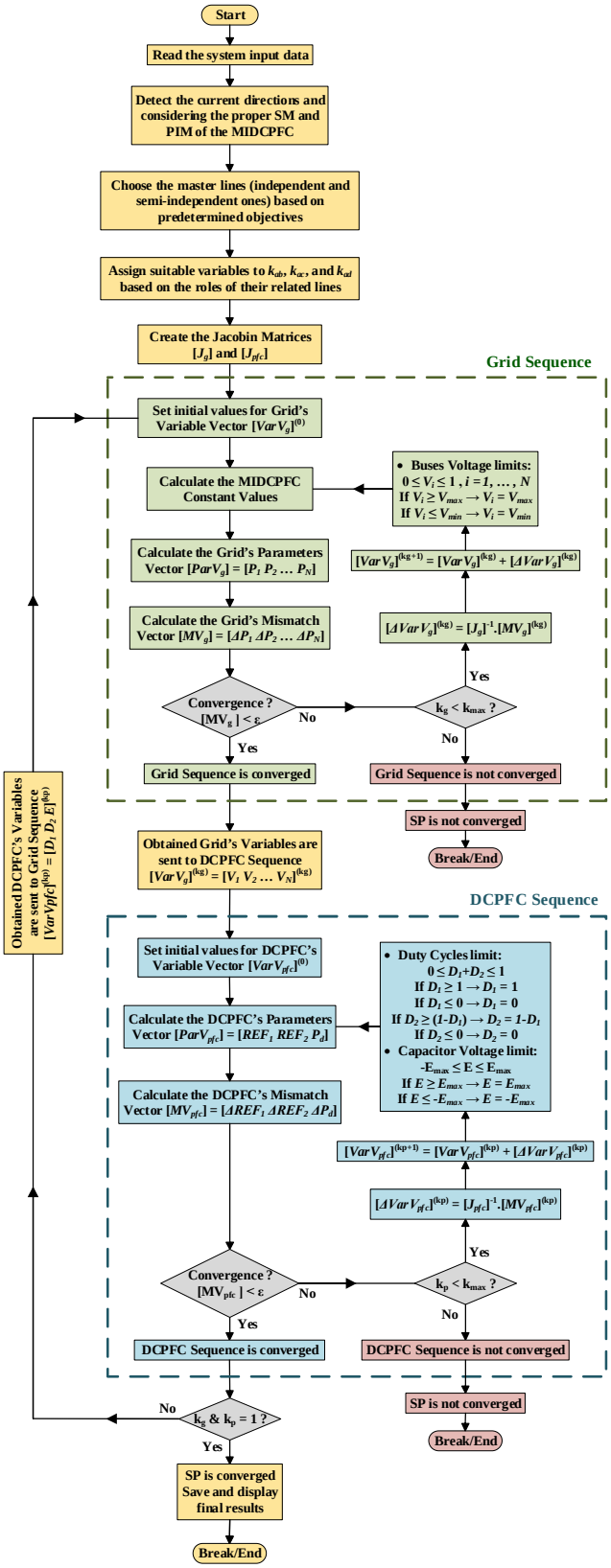

Figure 4.2. The proposed solution procedure.

- sequence (Step 6) to start a new iteration. At this time, the obtained results for grid variables are used as initial values to begin the grid sequence. In this way, the system can converge efficiently.
- *Step 19***:** Display the final DC PF results.

4.6. Numerical Results

In this section, three aspects are examined: the performance of the proposed NR-based sequential DCPFS; the accuracy of the extracted DCPFEs; and the capability of the MIDCPFC to control PF. The proposed concepts are validated using a new meshed 15-bus MT-HVDC grid developed in this thesis. The simulation and programming are carried out in the MATLAB/Simulink environment.

4.6.1. The Flexible MT-HVDC Grid

In this chapter, the15-bus MT-HVDC grid with specifications and features of the grid the same as Chapter 3 is used as shown in Figure 4.3. All parameters of this test grid are given in Table 4.1.

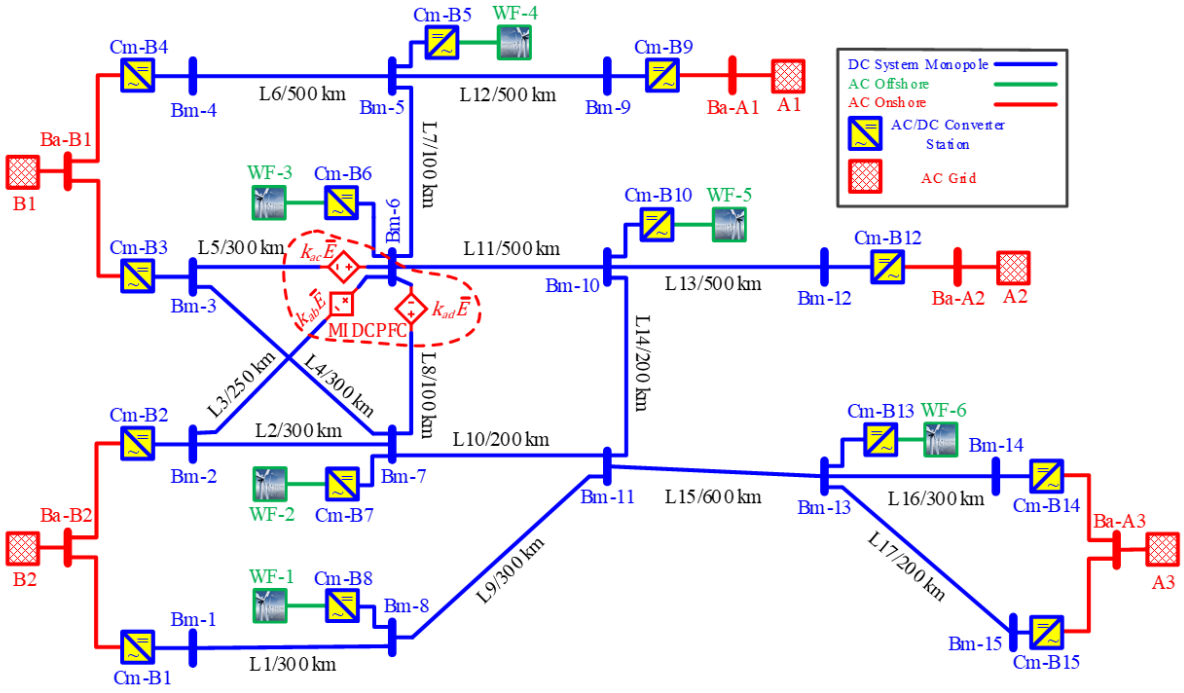

Figure 4.3. The created 15-bus MT-HVDC grid.

Table 4.1. Parameters and technical constraints of the flexible 15-bus MT-HVDC test grid

Parameters	Values	Parameters	Values
$P_{b,DC}$	4000 (MW)	V_{min}	0.9500 (pu)
$V_{b,DC}$	800 (kV)	V_{max}	1.0500 (pu)
G_{Line}	0.48 (μs/km)	Duty Cycles	$0 \leq D_{1,2} \leq 1$
R_{Line}	0.006 (Ω/km)	α	0.001
OffWF Power Factor	0.95	β	0.006
		γ	0.008
$V_{b,ac}$	400 (kV)	a	0.007
$K_{d2,3,14}$	57.58 (pu)	b	0.0036
$V^{*}_{d2,3,14}$	0.9500 (pu)	c	0.0002
ε (Convergence Tolerance)	10^{-6}	k_g (Grid Sequence Iteration)	$k_{max} = 50$
k_p (DCPFC Sequence Iteration)	$k_{max} = 50$	$k_c = k_g + k_p$	$k_{max} = 100$
k_t (Algorithm Iteration)	$k_{max} = 50$		

4.6.2. DC PF Results

Four scenarios are considered to examine the proposed concepts in this chapter:

- **Scenario A:** Performing PF on the non-compensated state of the MT-HVDC test grid under normal conditions.
- **Scenario B:** Performing PF on the non-compensated state of the MT-HVDC test grid under contingency (inability of Bm-4 in consuming power).
- **Scenario C:** Performing PF on the compensated state of the MT-HVDC test grid considering L3 as the independent and L5 as the semi-independent master lines.
- **Scenario D:** Performing PF on the compensated state of the MT-HVDC test grid considering L5 as the independent and L3 as the semi-independent master lines.

The PF results of all scenarios in per-unit (base values can be found in Table 4.1) are presented in Table 4.2.

Table 4.2. DC PF results obtained by the proposed method

Case study		**Scenario A**		**Scenario B**		**Scenario C**		**Scenario D**	
Bus	Type	V	P	V	P	V	P	V	P
1	CPB	0.9994	-0.7000	1.0102	-0.7000	1.0146	-0.7000	1.0146	-0.7000
2	DCB	0.9849	-2.0103	0.9933	-2.4955	0.9928	-2.4660	0.9928	-2.4660
3	DCB	0.9836	-1.9345	0.9916	-2.3974	0.9909	-2.3534	0.9909	-2.3534
4	CPB	0.9677	-1.1000	1.0333	0.0000	1.0358	0.0000	1.0358	0.0000
5	CPB	1.0109	1.5000	1.0337	1.5000	1.0362	1.5000	1.0362	1.5000
6	CPB	1.0064	1.5000	1.0210	1.5000	1.0235	1.5000	1.0235	1.5000
7	CPB	1.0054	1.5000	1.0171	1.5000	1.0229	1.5000	1.0229	1.5000
8	CPB	1.0154	1.0000	1.0261	1.0000	1.0304	1.0000	1.0304	1.0000
9	CPB	1.0214	0.3000	1.0440	0.3000	1.0465	0.3000	1.0465	0.3000
10	CPB	1.0154	1.5000	1.0272	1.5000	1.0310	1.5000	1.0310	1.5000
11	CPB	1.0096	0.0000	1.0204	0.0000	1.0247	0.0000	1.0247	0.0000
12	CPB	0.9844	-0.8000	0.9966	-0.8000	1.0005	-0.8000	1.0005	-0.8000
13	CPB	0.9937	1.5000	0.9987	1.5000	1.0007	1.5000	1.0007	1.5000
14	DCB	0.9686	-1.0687	0.9707	-1.1918	0.9716	-1.2420	0.9716	-1.2420
15	CPB	0.9829	-0.7000	0.9879	-0.7000	0.9899	-0.7000	0.9899	-0.7000
DCPFC:	D_1	---		---		0.31504		0.38631	
	D_2	---		---		0.38631		0.31504	
	E	---		---		0.02683		0.02768	
Iteration:	k_g	5		5		27		27	
	k_p	---		---		32		32	
	k_c	---		---		59		59	
	k_t	---		---		11		11	
Inj.[a] Power		8.8000		8.8000		8.8000		8.8000	
Abs.[b] Power		8.3135(94.47%)		8.2848(94.15%)		8.2614(93.88%)		8.2614(93.88%)	
VSCs Loss		0.1734 (1.97%)		0.1737 (1.97%)		0.1735 (1.97 %)		0.1735 (1.97 %)	
DCPFC Loss		---		---		0.0108 (0.12%)		0.0108 (0.12%)	
Lines Loss		0.3130 (3.56%)		0.3415 (3.88%)		0.3543 (4.03%)		0.3543 (4.03%)	
Line	M.P.[c]	P	Status	P	Status	P	Status	P	Status
L1	±0.8000	0.7258	---	0.7256	---	0.7255	---	0.7255	---
L2	±1.5000	0.9198	---	1.0777	---	1.3678	---	1.3678	---
L3	±1.2000	1.1577	---	**1.5098**	**O.L.[d]**	**1.2000**	---	**1.2000**	---
L4	±1.5000	0.9786	---	1.1547	---	1.4568	---	1.4568	---
L5	±1.2000	1.0243	---	**1.3362**	**O.L.**	**1.0000**	---	**1.0000**	---
L6	±1.2000	1.1687	---	**0.0152**	**Con.[e]**	0.0153	Con.	0.0153	Con.
L7	±1.8000	0.5978	---	1.7511	---	1.7510	---	1.7510	---
L8	±1.5000	0.1350	---	0.5319	---	1.2148	---	1.2148	---
L9	±0.8000	0.2626	---	0.2628	---	0.2628	---	0.2628	---
L10	±0.8000	0.2836	---	0.2223	---	0.1299	---	0.1299	---
L11	±0.8000	0.2476	---	0.1733	---	0.2106	---	0.2106	---
L12	±0.8000	0.2917	---	0.2917	---	0.2917	---	0.2917	---
L13	±1.0000	0.8434	---	0.8429	---	0.8428	---	0.8428	---
L14	±0.8000	0.3948	---	0.4696	---	0.4323	---	0.4323	---
L15	±0.8000	0.3622	---	0.4974	---	0.5531	---	0.5531	---
L16	±1.5000	1.1125	---	1.2428	---	1.2961	---	1.2961	---
L17	±0.8000	0.7206	---	0.7205	---	0.7205	---	0.7205	---

[a] Injected [b] Absorbed [c] Maximum Power [d] Overload [e] Contingency

In Scenario A, the generated power from OFFWFs is transmitted to the consuming units (onshore VSC stations). The system references in this scenario are sufficient to comply with all the system constraints (line current and bus voltage limits), and therefore, no DCPFCs/MIDCPFCs are required.

Scenario B shows an overloading condition because VSC Cm-B4 is unable to absorb power. There was an overloading condition on the HVDC lines, L3 and L5 forcing the whole system to change power direction from line L6 to line L7. Consequently, the injected power at buses Bm-5 and Bm-9 must be absorbed at bus Bm-6 and the extra absorbed power is then transmitted through HVDC lines, L3, L5, and L7. However, the additional power added to HVDC lines L3 and L5 exceeds their limits, so an overloading condition occurs.

In Scenario C, employing the MIDCPFC shows its efficacy as it has completely resolved the overloading condition of HVDC lines L3 and L5 by inserting compensating voltage sources, and consequently, facilitating power exchange from the master lines (L3 and L5) to the slave line (L8). In other words, MIDCPFC acts as a power diverter to change the path of overloading power of particular (master) lines to the adjacent (slave) line. Power generation (especially by OffWFs) or power curtailment in other consuming units remains no change.

The roles of L3 and L5 are reversed in Scenario D, as L3 is considered as a semi-independent line while L5 is considered as an independent line. The obtained results are exactly the same as those in Scenario C, which proves the accuracy of the proposed comprehensive SM, the ability and flexibility of the proposed sequential DCPFS in solving a DCPFP when the role of the compensated lines and their duty cycles have been changed.

The PF results of Table 4.2 reveal the following aspects:

- The effectiveness of the MIDCPFC and its superior PF control capabilities in HVDC lines while meeting practical constraints.
- The sequential DCPFS model preserves the original Jacobin matrix and exhibits superior convergence properties.
- The accuracy of the derived DCPFEs and power loss equations, and their correct embedding into the sequential DCPFS.

- The sequential DCPFS has demonstrated a superior performance in solving highly meshed flexible MT-HVDC grids.

4.7. Conclusion

In this chapter, a novel Newton-Raphson-based sequential DCPFS is proposed to solve the DCPFP in highly meshed MT-HVDC grids compensated by a MIDCPFC. The main objective is to overcome shortcomings of the available literature by proposing a DCPFS without modifying the original Jacobin matrix of the system. To provide precise modeling, the power loss of the MIDCPFC is formulated at the core of DCPFEs. This proposed power loss modelling approach can also be used for other voltage-source-based DCPFCs. A highly mesh 15-bus MT-HVDC test grid is used for validation with four scenarios being tested. The obtained results demonstrate a significant reduction in the complexity of the original Jacobin matrix of the system. The performance of the proposed NR-based sequential DCPFS has been validated, and the original Jacobin matrix of the system is kept intact, which facilitates integration of DCPFCs as their on/off status may cause significant modifications in the original Jacobin matrix of the system under the unified approach. The proposed sequential DCPFS successfully decouples the DCPFC equations from DCPFEs of the main MT-HVDC grid. The proposed methods in this paper can be used to develop the future power flow software for solving DCPFPs in HVDC grids.

4.8. References

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5. Conclusion and Future Work

5.1. Conclusion

HVDC Transmission is a promising technology for tomorrow's power grids with increasing penetration of renewable energy sources, such as offshore wind farms. Despite decades of research, several challenging aspects remain unsolved in power flow studies of HVDC systems.

Various power electronic devices play a critical role in HVDC transmission, including the emerging power electronic device, DC power flow controllers. To introduce these power electronic devices, especially DCPFCs, in HVDC systems, a comprehensive literature review is conducted in Chapter 2 of this thesis.

Considering DCPFCs in power flow studies of HVDC grids, two novel DC power flow solvers are proposed in Chapters 3 and 4 in this thesis.

In Chapter 3, to overcome lack of a comprehensive power flow study of HVDC systems in the presence of DCPFCs, a novel unified Newton-Raphson-based DCPFS is proposed to solve the DC power flow problems in highly meshed MT-HVDC grids compensated by multi-port IDCPFCs. The static models (SMs) and power injection model (PIM) of MIDCPFCs are proposed to tackle shortcomings in the literature. For precise modeling, for the first time, power losses of the MIDCPFC is formulated, and power losses of the MIDCPFC and VSCs in HVDC grids are considered simultaneously. A new highly meshed 15-bus MT-HVDC test grid is created to validate the proposed DCPFS through case studies. The results prove the accuracy of the proposed SMs and PIM of the MIDCPFC, their effective embedding in DC power flow equations of the system, and good performance of the proposed unified DCPFS.

In Chapter 4, a novel sequential Newton-Raphson-based DCPFS is proposed to solve DC power flow problems in highly meshed MT-HVDC grids compensated by MIDCPFC. In Chapter 3, the original Jacobin matrix of the HVDC system faces some minor modifications due to the presence of MIDCPFCs. It works well when only one DCPFC is used in the system at the on-state, but when several DCPFCs or one DCPFC with several on- and off-states are used during operation, it may

cause high computational burden as the original Jacobin matrix of the system must be changed several times. To improve this situation, the sequential Newton-Raphson-based DCPFS is proposed in Chapter 4 to avoid modifying the original Jacobin matrix of the system. Power losses of the MIDCPFC is modeled in DCPFEs, and power loss equations of the MIDCPFC and VSCs are considered simultaneously. The proposed sequential DCPFS is validated by the highly meshed 15-bus MT-HVDC test grid through case studies. The results show a significant reduction in complexity of equations for the system's original Jacobin matrix, and the original Jacobin matrix is intact, which facilitates integration of DCPFCs in HVDC grids. The results also prove the accuracy of the proposed models of the MIDCPFC and the derived DCPFEs of the system, and good performance of the proposed sequential DCPFS, which enables decoupling equations of DCPFCs and DCPFEs of the main MT-HVDC grid.

The two proposed unified and sequential DCPFSs can be used to develop the future power flow software for solving DCPFPs of HVDC grids.

5.2. Future Work

The following are proposed future work to improve the performance of DCPFCs to facilitate power transmission through MT-HVDC grids:

1. Novel power electronics structures for DCPFCs with independent capability of controlling PF in numerous HVDC lines.
2. Comprehensive schemes handling simultaneous operation of several DCPFCs in a MT-HVDC grid.
3. Novel DCPFSs for power flow problems of hybrid AC/DC systems.
4. Protection schemes for DCPFCs to isolate faults of HVDC lines in MT-HVDC grids.
5. Dynamic interactions of installed DCPFCs and power converters, such as VSCs or CSCs, in MT-HVDC grids.

Publications

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Submitted Referred Paper:

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