Resonant DC Link Converters and Their Use in Rail Traction Applications

by

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Contents

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Abstract

Conventional 'hard switching' converters suffer from significant switching loss due to the simultaneous imposition of high values of current and voltage on the devices during commutation. Resonant converters offer a solution to this problem. A review of resonant circuit topologies is presented, which includes a summary of the interference problems which may occur when using power converters in the rail traction environment. Particular attention is given to the Resonant DC Link Inverter (RDCLI) which shows a great deal of promise using currently available devices.

The frequency domain simulation of RDCLIs is discussed as a means of rapidly evaluating circuit behaviour, especially in relation to modulation strategies. A novel modulation strategy is proposed for Resonant DC Link Inverters, based on a procedure known as Simulated Annealing which allows complex harmonic manipulations such as harmonic minimisation, to be performed. This is despite the fact that RDCLIs are constrained to use Discrete Pulse Modulation whereby switch commutations are restricted to specific moments in time. The modulation algorithms were verified by use of a low-power test rig and the results obtained are compared against theoretical values. Details of the hardware implementation are also included.

A single-phase pulse-converter input stage is described which may be incorporated into the Resonant DC Link Inverter topology. This input stage also benefits from soft-switching and allows four-quadrant operation at any desired power factor. A modulation scheme based on Simulated Annealing is proposed for the pulse-converter, to achieve harmonic control whilst also synchronising with the supply waveform. Practical results are presented and compared with those obtained by simulation and calculation.

Finally the design of Resonant DC Link Converters is discussed and recommendations made for the choice of resonant components based on the minimisation of overall losses. Comparisons are

made between hard-switching and soft-switching converters in terms of loss and harmonic performance, in an attempt to quantify the benefits which may be obtained by the application of soft-switching.

Chapter 1

Introduction

Switching Losses are a major constraint on the performance of power converters. They are a dominant feature in 'hard-switching' converters due to the trajectories taken by voltage and current waveforms during device commutation. This places restrictions on the upper operating frequency which as a consequence, limits the power density (kW/kg) and the capabilities for harmonic control of the output spectrum. In addition, hard-switching exacerbates effects such as the generation of Electromagnetic Interference. To cure these problems it is apparent that the energy loss due to switching should be reduced to very low values. This may be achieved by introducing current or voltage zeros at the instant of device commutation. Resonant Converters are a family of converters capable of operating in this mode and form the subject of this thesis.

The problems associated with converter size and weight are made more acute when operating in the rail traction environment due to the considerable pressure to reduce the overall weight of rail vehicles, whilst maximising the space available for passengers. Additionally, the equipment must not interfere with the railway signalling and communication systems. A major application for power converters on rail vehicles is for auxiliary supplies where they perform an important function, supplying power to systems essential for passenger comfort, safety, and normal train operation. The increasing expectations of passengers and desire of rail operators to improve customer facilities, demand higher equipment specification levels with attendant increases in power supply requirements. As a consequence, there is a need to increase the rating of auxiliary converters, yet this counters the aspirations for reduced size and weight. Thus a compromise must be reached but the situation may be improved by the application of Resonant Converters.

The aim of the work described in this thesis was to investigate Resonant Converters, with a particular emphasis on their application in the rail traction environment in order to address the

issues outlined above. The thesis begins by examining switching loss in more detail, and reviews the various resonant converter families which may be used to reduce losses. The design and application of resonant converters are discussed both in general terms and with reference to railway applications. Novel modulation and control strategies are introduced, which allow harmonic manipulation of the spectra of the waveforms generated by resonant converters which are constrained to use Discrete Pulse Modulation. It is shown how minimisation of specific harmonics or groups of harmonics is possible, which is of relevance to rail traction applications where signalling frequency avoidance may be required, or steps may need to be taken to prevent interference with communication systems. A common configuration for converters on AC-supplied rail vehicles is single-phase to three-phase. A 'soft-switching' topology is described, and its harmonic control characteristics assessed. Finally, comparisons are made between hard-switching and resonant converters to enable an evaluation of the benefits and disadvantages of each technique.

Chapter 2

Background to Switching Loss, Resonant Converters, and Signalling Compatibility

2.1 A Review of Hard Switching Converters

Many of the popular power converter topologies employ *hard switching* techniques. This means that during switching the power components experience high values of voltage and current simultaneously. As a result of this, significant quantities of power are dissipated in the devices during each switching event. For a given heatsinking capability this places a restriction on the maximum switching frequency achievable. This is a particular problem when attempting to reduce the size and weight of a converter by increasing the switching frequency since there follows a linear increase in switching losses. The increase in losses detracts from the advantages gained from increasing the switching frequency.

Figure 2.1 shows in more detail the cause of switching loss when driving an inductive load. Consider one leg of a DC-AC converter as shown in Figure 2.1(a). Suppose that switch S2 is initially closed and switch S1 is open. Thus S2 conducts the whole of I_0. When the control signal to S2 changes to the off condition the voltage across the power device begins to rise as it changes to the off-state. The inductance of the load maintains I_0 virtually constant. When the voltage across S2 reaches the rail voltage (plus a small overshoot due to stray inductance) the current begins to commutate from S2 to D1. Figure 2.1(b) shows the changes in voltage and current applied to S2, and the resulting switching power loss. A similar process occurs during turn-on, but in this case it is the current which overshoots rather than the voltage. This is due to the reverse recovery current of the diode.

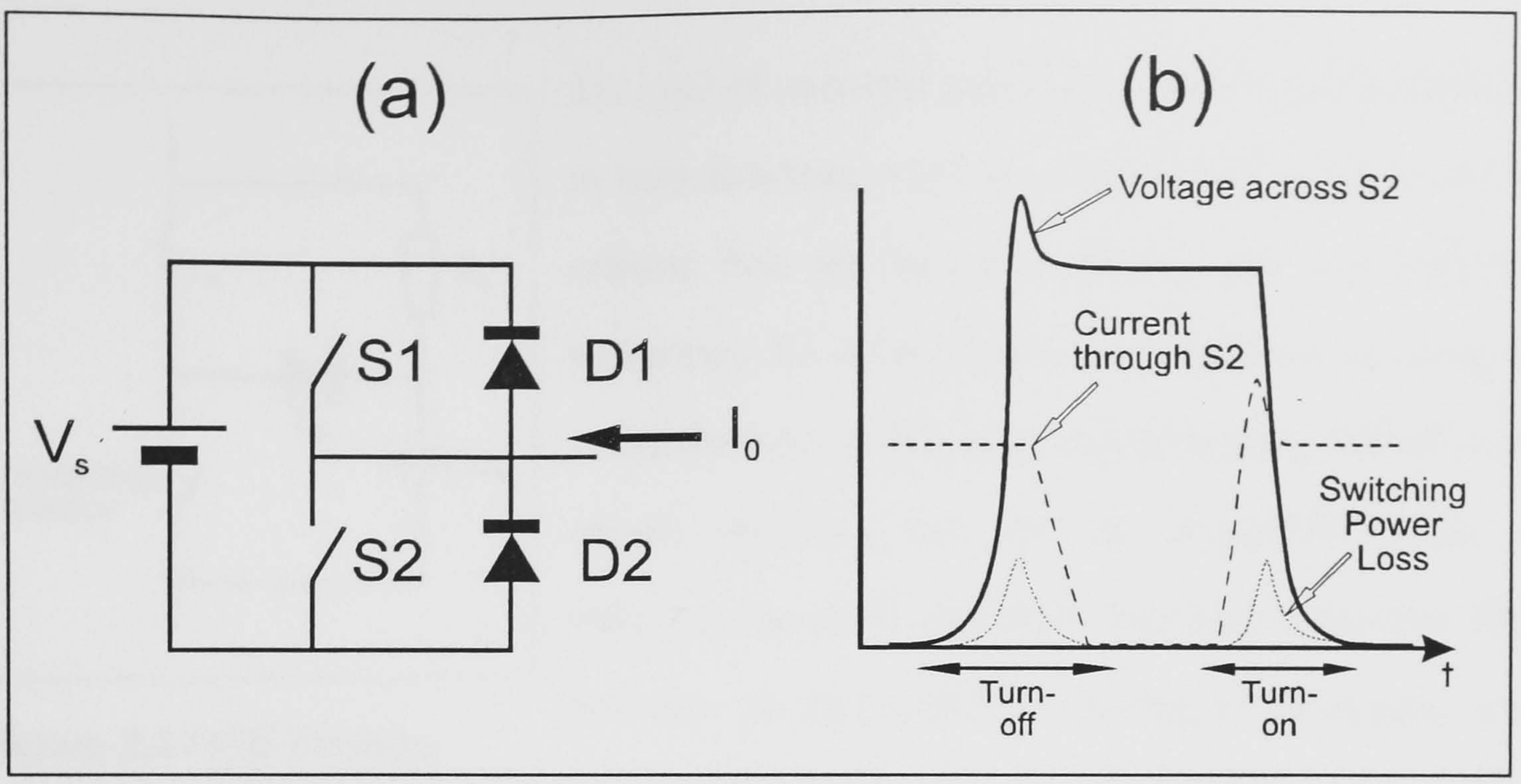

Figure 2.1 Voltage and Current Transitions Leading to Switching Power Loss

The limit imposed on switching frequency, and the manner in which switching takes place has many implications for the operation of such converters, which may be summarised as follows [1,2]:

- The low switching frequency results in high harmonic distortion of the output waveforms
- Harmonic distortion of the output also appears on the input side of the converter, and hence in the supply network
- The mode of switching causes high values of *di/dt* and *dv/dt* which can cause serious problems of Electromagnetic Interference (EMI).
- High values of *dv/dt* cause capacitively coupled currents to flow in machine windings leading to increased motor heating.
- The rapidly changing voltages and currents increase device stress which can adversely affect reliability.
- Due to the restricted frequency of operation, transformers and reactive components used in filters must be large.
- The switching frequency may be limited to a value within the audible range. The noise subsequently produced may be unacceptable in some applications.
- The bandwidth of the converter as a whole is limited by the switching frequency which can complicate control loops.

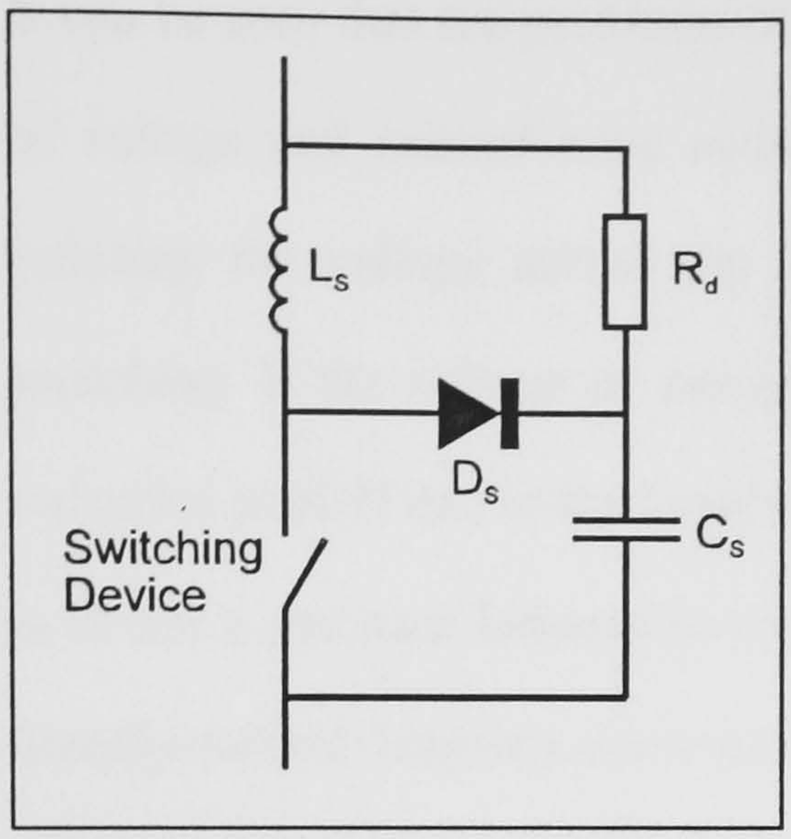

Figure 2.2 RCD Snubber

The goal of increased switching frequency can be achieved in hard-switching converters if the switching losses can be reduced. This may be done in several ways. One method is to increase the speed of *device* commutation by using an inherently faster device, or by modifying the gate/base driver circuit. However, this has the undesirable effect of increasing the *dv/dt* and *di/dt*. This may exacerbate EMI problems. Another method of reducing switching losses is to divert current away from the device and into a *snubber* circuit during the switching period. One of the most popular snubber configurations is shown in Figure 2.2. During device turn-off, the diode D_S and capacitor C_S delay the rate of rise of voltage across the device. During turn-on, L_S delays the rate of rise of current through the device. Capacitor C_S then discharges through the device via R_D. The problem with this circuit is that it dissipates energy. As a consequence the overall efficiency of the converter does not change significantly. *Lossless* snubber topologies exist, [3] an example of which is shown in Figure 2.3 (S1 and S2 are the power devices). These circuits return the switching energy to the supply or to the load using (ideally) non-dissipative components which improves the converter efficiency. However the circuits are often quite complex and can significantly add to the overall component count since they must be repeated for each switching device.

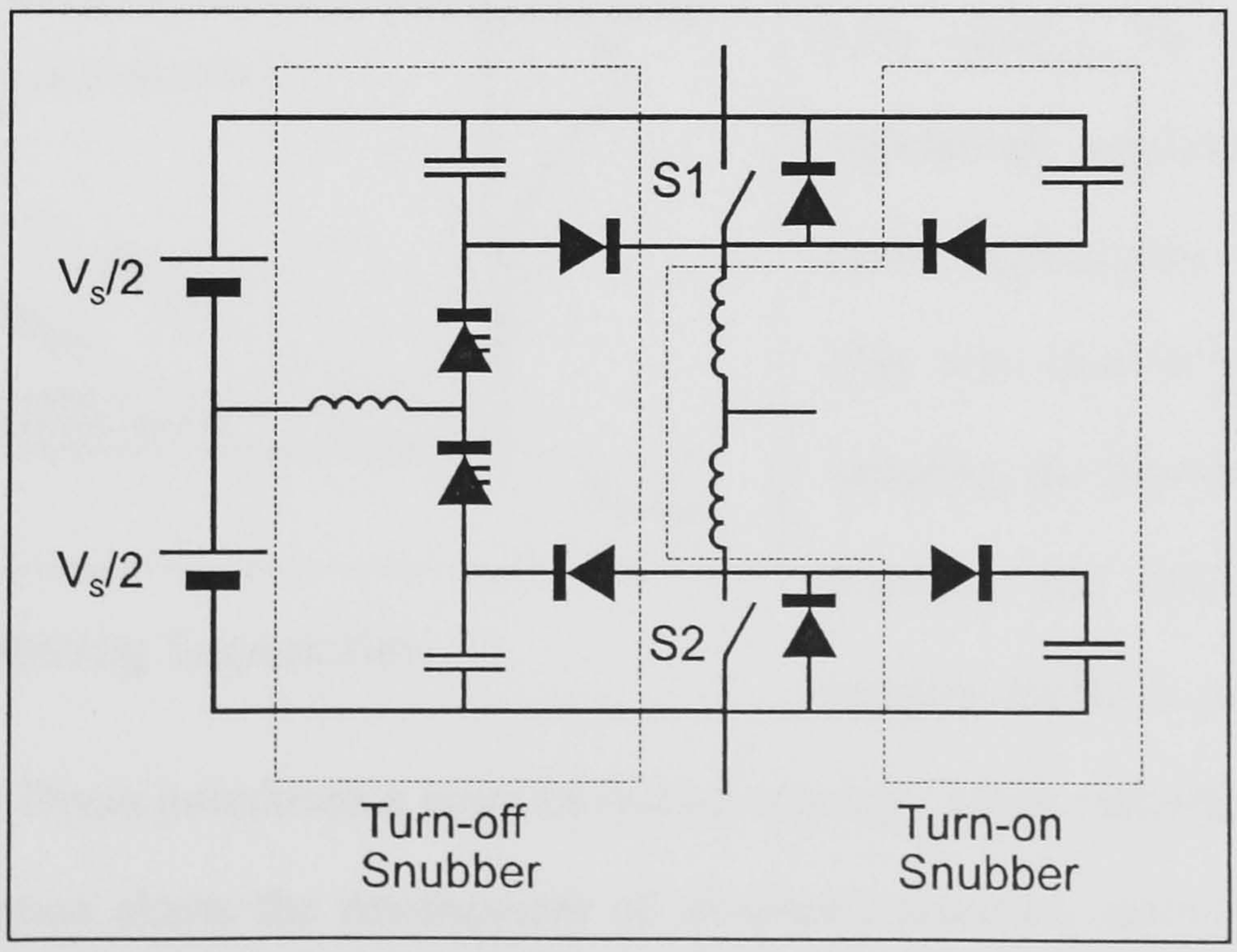

Figure 2.3 Lossless Inverter Snubber Circuit

It can be seen that the problems of switching loss could be alleviated if simultaneous application of voltage and current were avoided during switch commutation. This could be achieved by reducing the voltage across the switch, or the current through it, to zero at the instant of switching. If the voltage or current was reduced in a controlled manner there would also be a reduction in EMI due to the lower *dv/dt* and *di/dt* values. A convenient way of accomplishing this is to use a resonant Inductance-Capacitance (L-C) circuit. This has led to a class of converters broadly termed 'resonant converters'. The use of L-C components in converters is not limited to the task of reducing switching losses; they may perform other functions such as switch commutation.

The behaviour of switches during commutation may be described in terms of switching trajectories, i.e. the locus which is formed by a plot of current against voltage. The area under this locus gives an indication of the likely switching loss, though the time to traverse the loop is a vital additional factor in determining the actual loss. Figure 2.4 shows the switching trajectories for various types of converter switching arrangements. It can be seen how snubbers modify the trajectory to reduce losses in hard switching types. The small area under the switching locus of the resonant converter is characteristic of the low losses associated with this topology.

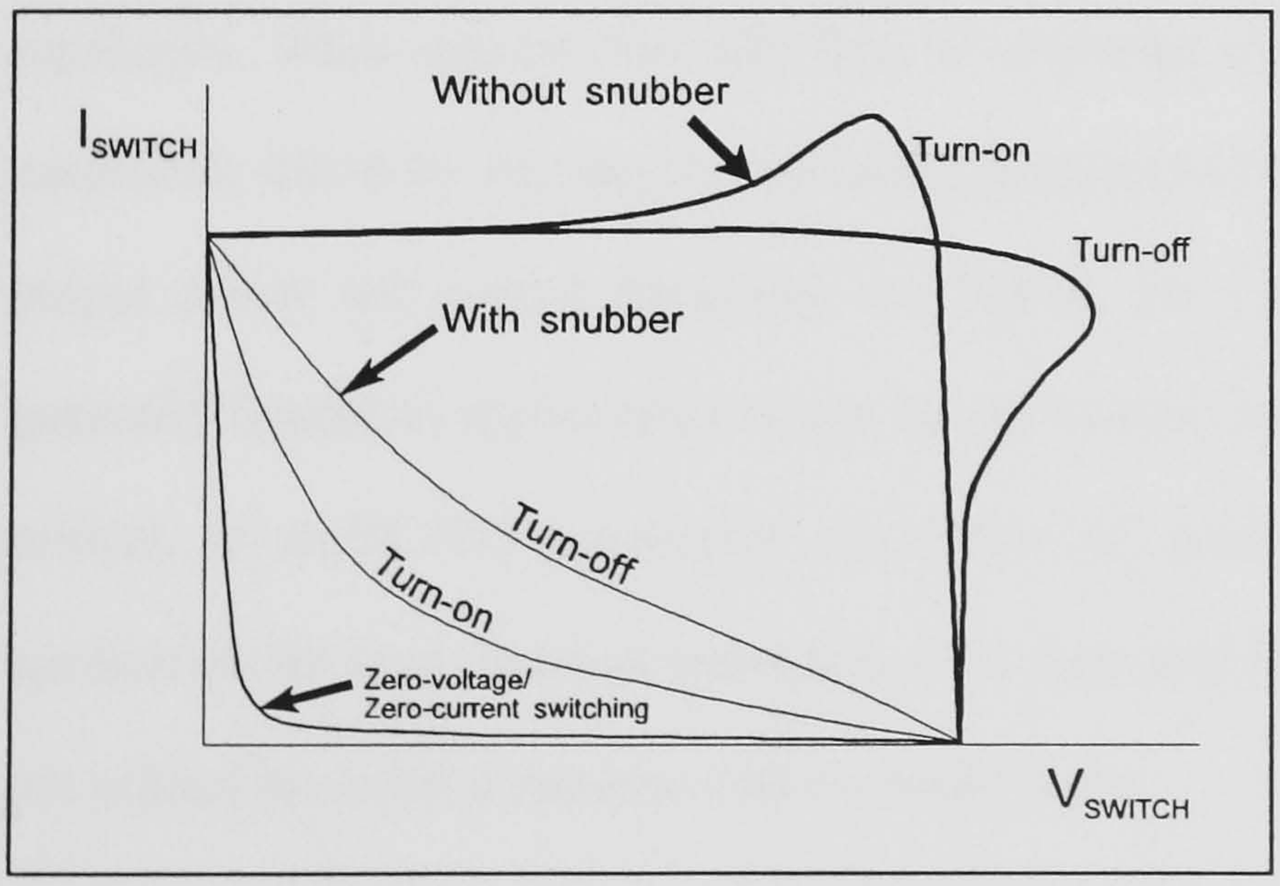

Figure 2.4 Switching Trajectories

Although resonant converters have been known for some time [4] widespread acceptance in variable speed applications did not follow. This was due to various problems including the large number of devices required, and the high VA rating required for the L and C components. However in 1986 Divan introduced a more promising topology which addressed these problems [1]. The next section charts the development of resonant converters, discussing their relative merits and disadvantages.

2.2 A Review of Resonant Converters

2.2.1 Classification of Resonant Converters

Resonant converters may have many different modes of operation and subtle variations in circuit topology. As a consequence classification is very difficult. There is no universally accepted system of classification, though it is helpful to apply an arbitrary system to aid comparison. In the following discussion of resonant converter development the classes listed below will be used:

i) Load Resonant Converter

ii) High Frequency Link Converter

iii) Resonant Switch Converter

The converters of most interest here are the Resonant DC Link type which are members of group (ii). Below a review of each class is presented.

2.2.2 Load Resonant Converters

This type of converter is most commonly used in DC/DC and DC/High-frequency-AC conversion, though it is also possible to synthesise low-frequency AC waveforms with certain topologies. What characterises this type of converter is the manner in which the energy flow is controlled; this is by varying the switching frequency of the circuit. This property means that the output power and output frequency are linked. As a consequence, this class of converter is generally limited to applications where an AC output is required but where the frequency is not critical, or to DC/DC conversion where the AC power is rectified and filtered. A common application for load resonant converters is in induction heating where the frequency of the AC is not critical provided it remains within certain limits.

In general load-resonant converters generate a high-frequency square-wave from a DC source, which is applied to an L-C circuit tuned approximately to the desired switching frequency. This is shown schematically in Figure 2.5 for a Voltage-Source Series-Resonant Converter. The L-C

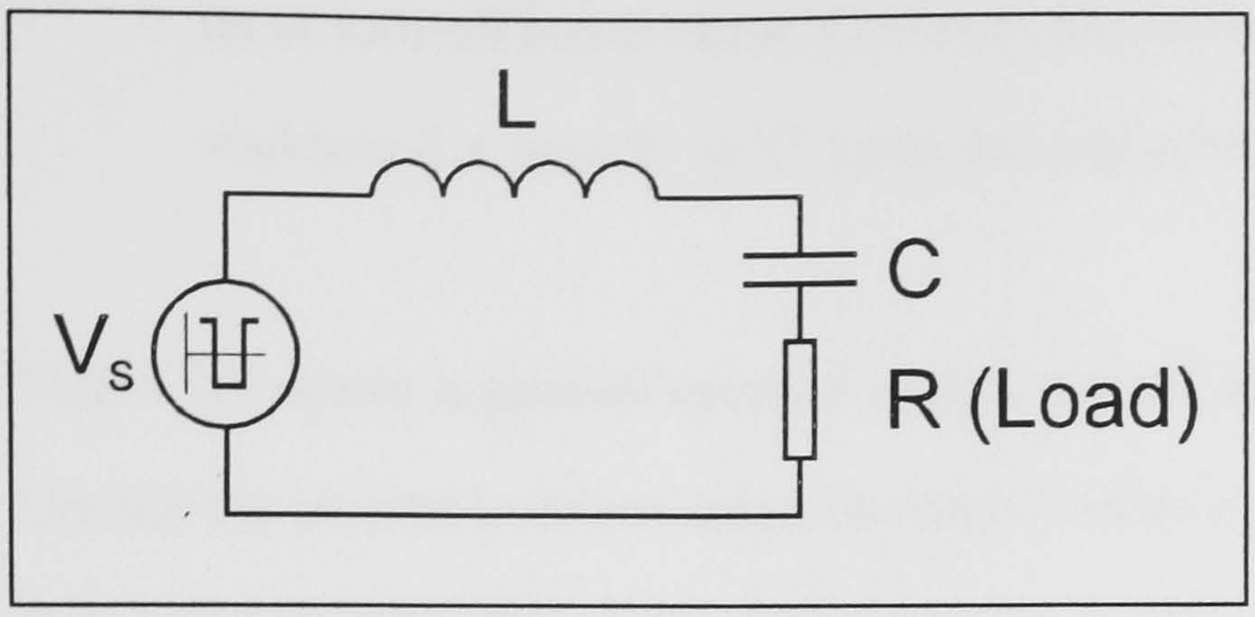

Figure 2.5 Schematic of a Series-Resonant Converter

components, or *resonant-tank*, attenuate the unwanted harmonics of the square wave, allowing fairly sinusoidal voltages and currents to exist.

There are many topological variations of the load-resonant converter. They all employ one of two basic approaches; the AC square-wave is applied to either a parallel or series-resonant circuit. Figure 2.6 shows a series-resonant converter. In this case the load is in series with the resonant components [5], although the load may be placed in parallel with the L or C to give the sub-class of *parallel-loaded series-resonant converter* [4,6]. In [7] it is shown how such converters may be used in the generation of low-frequency AC. In practice the complexity of control or large number of devices required, make this an uncommon application. Load-resonant converters have the *potential* for loss-free switching but whether this potential is realised depends on the way in which the converter is used. For the voltage-source converters described above, two operating modes are possible;

- 'Discontinuous mode' : By definition, the switching is carried out at less than the resonant frequency of the L-C tank. Zeros of voltage or current occur, at which point switching may take place so there are no switching losses.
- 'Continuous mode' : This can be used above or below the resonant frequency. Either turn-

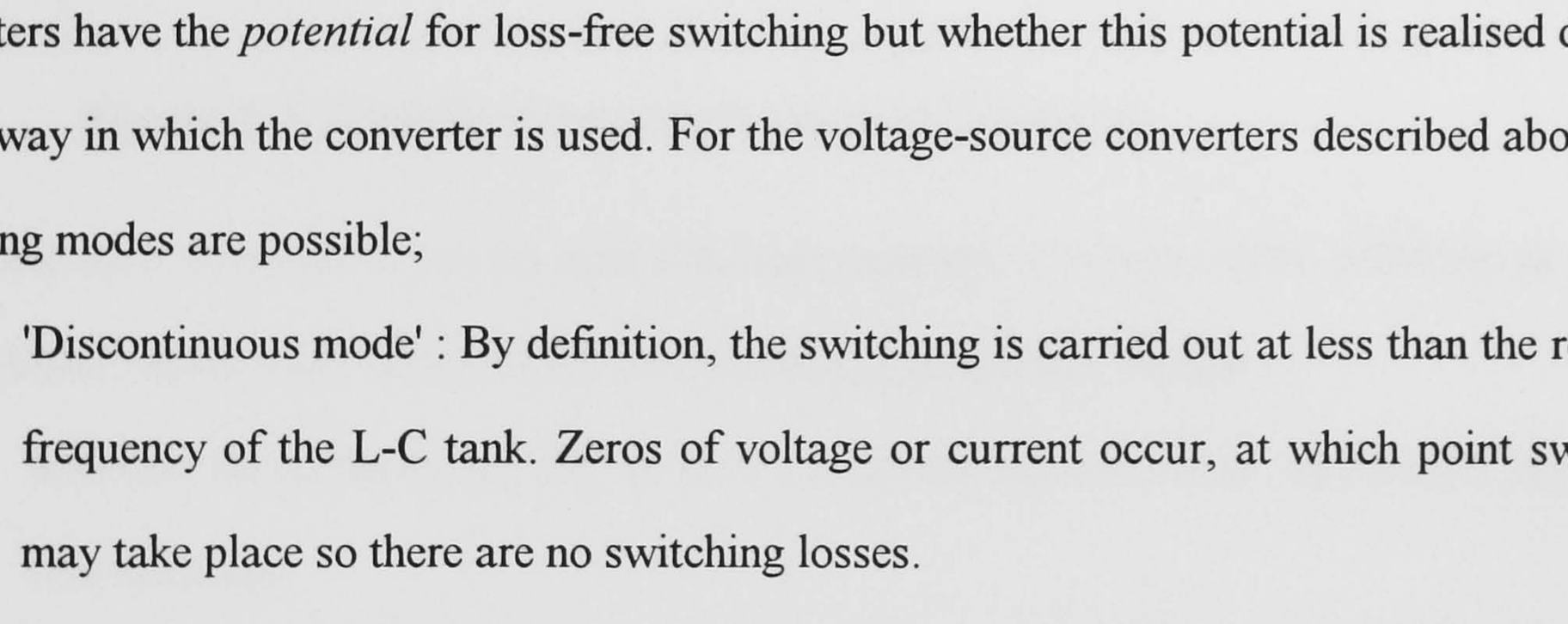

Figure 2.6 Series-Resonant Converter

on or turn-off losses occur. However, due to the way the circuits operate, large loss-less snubbers (i.e. pure 'L' or 'C') may be used to virtually eliminate switching losses.

Figure 2.7 shows a parallel-resonant circuit, typical of the type used in induction heating [8]. Usually the inverter is driven using thyristors and as a consequence must operate at a frequency above the resonant frequency of the tank, to supply the capacitive VARS to commutate the switching devices.

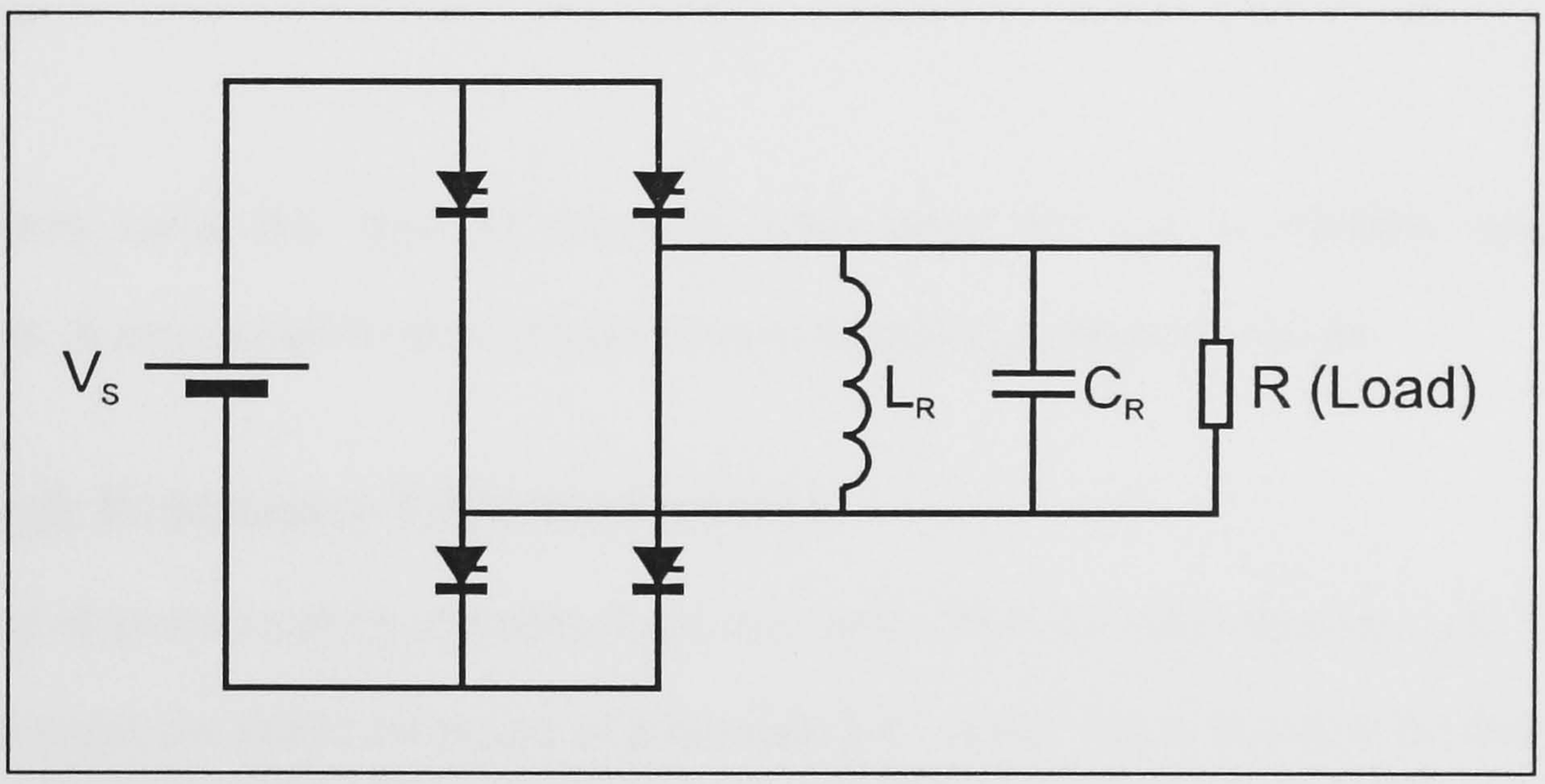

Figure 2.7 Simplified Parallel-Resonant Converter

From this short overview it can be seen that load-resonant converters offer solutions to some of the problems which were identified for hard-switching converters, namely:

- Reduced switching losses due to zero voltage/current switching, and use of large, loss-free snubbers.
- Reduction in the size of reactive components due to the high frequency of operation.
- Medium-speed flywheel diodes may be used, due to the soft-switching mechanism.
- Inaudible circuit operation for frequencies above 18kHz.
- Reduced response time due to higher frequency of switching.

It would appear that load-resonant converters would make a suitable replacement for hard-switching PWM converters. Unfortunately they only partially meet the requirements and themselves suffer from several serious problems:

- Although the size of some of the reactive components may be reduced, a large L-C tank must be introduced. This tank must be rated for very high peak currents or voltages (several times greater than the nominal output values). Due to the range of frequencies over which the circuit operates, optimisation of the tank is difficult.
- Large snubbers may need to be introduced if zero-loss switching is to be achieved.
- Many of the topologies require a large number of switching devices.
- Control of the converters can be complex especially when synthesising low frequency AC.

These factors make this type of converter unattractive for use in variable speed drive applications. A more suitable class of converters is described in the next section.

2.2.3 High Frequency Link Converters

The method of power control separates these converters from the load-resonant type. The input and output stages are linked by means of a resonant L-C circuit but in this case the frequency of operation of the link does not affect the power flow. Instead, this is achieved through modulation of the output stage. The exact function of the L-C components depends on the topology under consideration, but they are responsible for the great versatility of this family of converters. In various circuits they may naturally commutate switching devices, allow for zero-loss switching and permit power flow in either direction between AC/AC, DC/DC or AC/DC systems. The output stage of early High-Frequency Link (HFL) converters consisted of a cyclo-converter employing phase-angle control to vary the power flow. In later topologies *Integral Cycle Modulation* (ICM) was introduced whereby the switches only change state at zeros of voltage or current on the link. This produced a large reduction in the switching losses. Presented below is a brief history of the development of HFL converters beginning with the earliest phase-angle control type. Because of the importance of the ICM types to this work, a system of classification is introduced.

Phase-Angle Control HFL Converters

The High Frequency Link converter was proposed by Bedford in 1973[9]. The basic converter circuit is shown in Figure 2.8. It consists of a high frequency SCR inverter, commutated by a parallel resonant L-C tank. This is connected via a transformer to a network of phase-angle controlled cyclo-converters. The circuit is operated above the resonant frequency of the tank which provides the leading kVA to commutate the thyristors. The operating frequency is varied in response to the load to ensure suitable commutation conditions for the thyristors, though this does not alter the power flow. The family of circuits described by Bedford are capable of operation from an AC or DC supply, and can produce variable DC, or variable voltage and frequency polyphase AC.

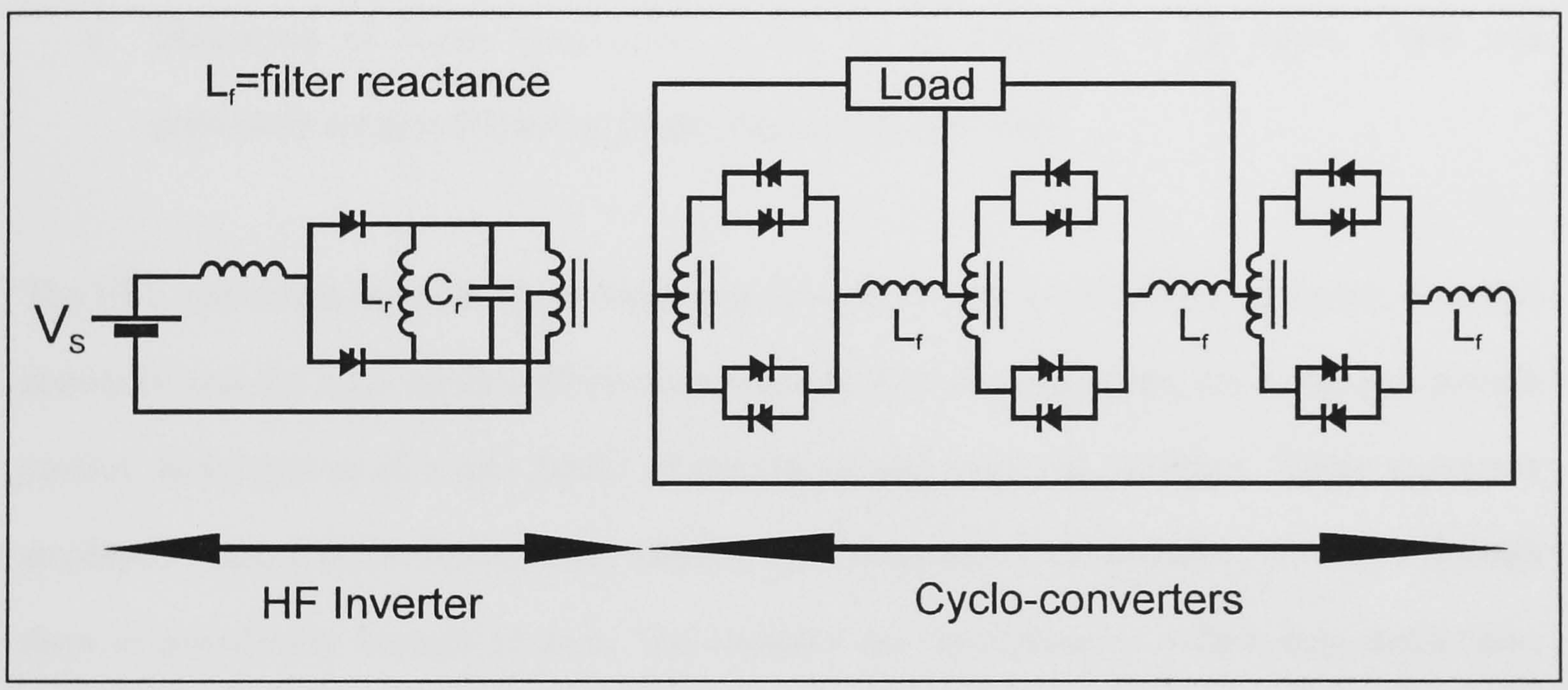

Figure 2.8 Bedford's HF Link Converter

Espelage and Bose [10] expanded on Bedford's work by describing a similar converter comprising two cascaded 12 thyristor cyclo-converters separated by a parallel resonant tank. The tank provides commutation for both cyclo-converters. This marked the introduction of a 'universal' HFL converter, being able to operate from AC or DC supplies with four-quadrant capability. This topology will allow conversion to DC or to variable voltage, variable frequency polyphase AC.

Whilst Bedford, Espelage, and Bose were developing HFL converters for variable-speed drive applications, Gyugyi and Cibulka [11] were independently developing the technology for power systems use. Again the converter consisted of two naturally commutated cyclo-converters used 'back-to-back' and connected via an L-C tank. Due to the high power involved, the link frequency was limited to around 400Hz.

The introduction of HFL converters made available many features previously unattainable from high power conversion systems including:

- Simple commutation of thyristors.
- Inherent four-quadrant capability.
- Independent control of real and reactive power flow.
- Generation of higher frequencies on the output compared to the input, which was previously not possible using single-stage cyclo-converters.

The HFL converters were clearly a major step forward in power conversion. However, a serious drawback was the high stresses which the switching devices experienced due to the phase-angle control. Development of a new family of converters addressed this problem. These converters employed 'Integral Cycle Modulation', wherein the voltage across the switches, or current through them is periodically brought to zero. The switches are constrained to switch only under these conditions, to reduce the switching stress to very low values. The next section analyses the development, and classification of this type of converter.

Integral Cycle Modulation

This type of converter may be classified according to the form of the voltage or current waveform on the link. In the so-called *AC-resonant* types the link waveform oscillates symmetrically about zero, in the *DC-resonant* types the waveform pulsates, reaching zero without passing through it. These two groups may be sub-divided into series and parallel types depending on the form of the link. [12,13] This also determines whether the circuit operates as a current source, or voltage source. In summary the groupings may be presented as follows:

AC Resonant

- Series-resonant AC current-link
- Parallel-resonant AC voltage-link

DC Resonant

- Series-resonant DC current-link
- Parallel-resonant DC voltage-link

Series-resonant AC Current Link Converters

The use of series-resonant circuits in DC/DC converters has been well established for some time. [14] In 1981 Schwarz [15] expanded their application by inclusion in the first 'universal' Integral Cycle Modulation converter. Unfortunately the circuit involved a complex magnetic design which limited its application. Other more suitable circuits have been described in the literature. [16,17] The basic topology of such converters is shown in Figure 2.9. Energy is transferred from the source to the load via the L-C link. The current in the link oscillates sinusoidally about zero, transferring pulses of current through the resonant components. The output stage distributes these pulses to the load in a manner which synthesises the required current waveshape. This synthesis is shown in Figure 2.10. An important advantage of this circuit is the current zeros which exist on the link. This allows the use of thyristors rather than force-commutated devices since the conditions for natural commutation are inherently present. The reversal of the link current necessitates bi-directionally conducting switches which may be implemented using inverse-parallel thyristors.

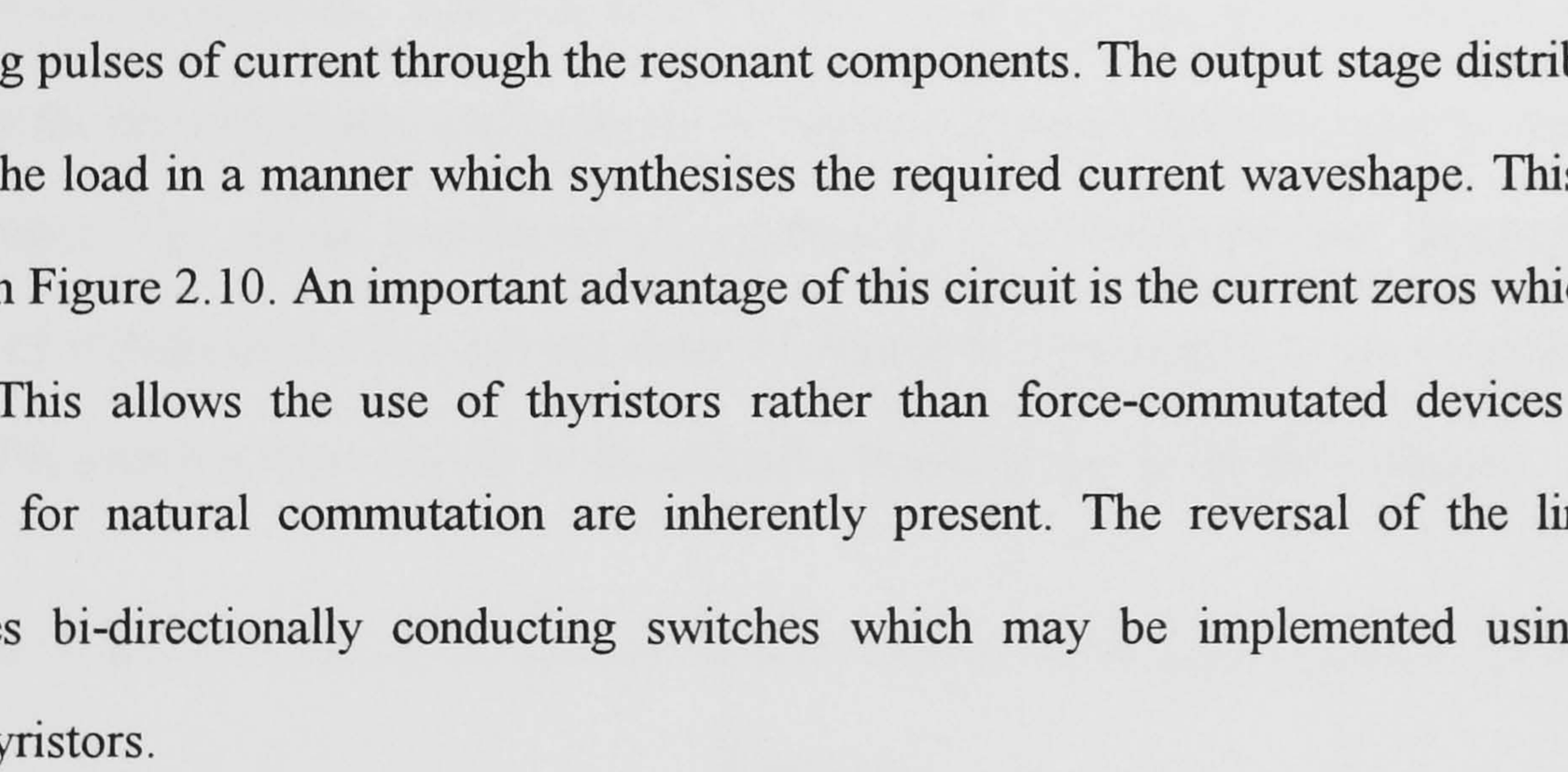

Figure 2.9 Series-Resonant AC Current Link Converter

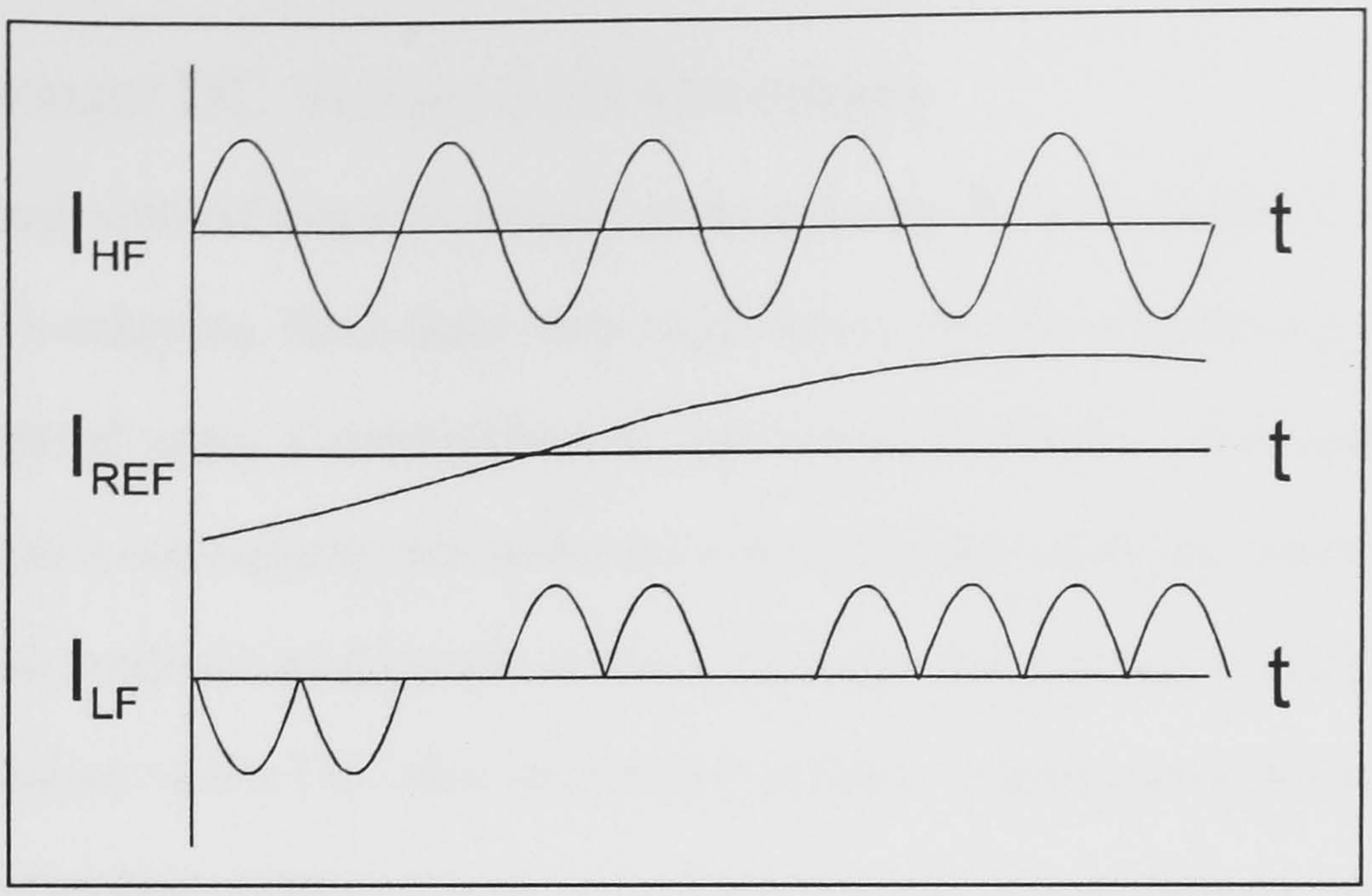

Figure 2.10 Synthesis of Low Frequency A.C.

Parallel-Resonant AC Voltage Link Converters

The first converter of this type was proposed in 1986 by Sood and Lipo. [18,19] It may be thought of as the *circuit dual* of the series-resonant AC converter. In this circuit it is pulses of voltage that are transmitted via the link rather than pulses of current. Figure 2.11 shows the basic topology of such a converter. It can be seen that the shape of the system waveforms is the same as those for the series-resonant link converter in Figure 2.9 except that they refer to voltage rather than to current. The output waveforms are synthesised in a similar manner. Because there are only zeros of voltage on the link and not zeros of current it is necessary to use force-commutated switches. The switches must also be bi-directionally blocking due to the AC voltage.

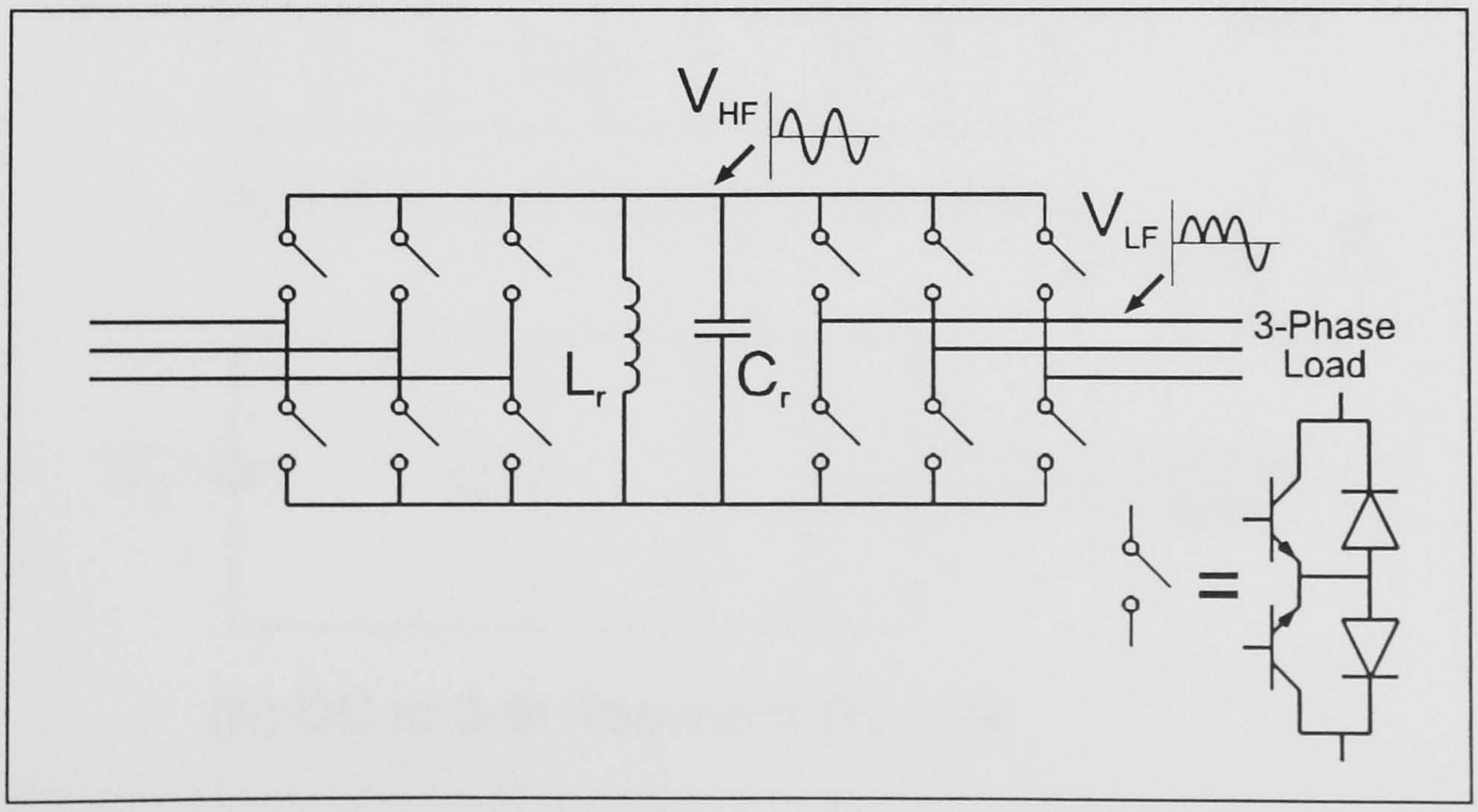

Figure 2.11 Parallel-Resonant AC Voltage Link Converter

Parallel-Resonant DC Voltage Link Converters

A major drawback with AC-resonant circuits is the necessity for the switches to be bi-directional blocking and/or conducting. Since there is no single device capable of achieving this, the switches must be synthesised using a combination of uni-directional devices. This adds to the overall complexity and as a consequence increases cost whilst reducing reliability. An elegant solution to this problem was proposed by Divan[1] in 1986. He suggested a circuit in which the oscillating link voltage is biased with a DC value such that it pulsates, reaching zero but without becoming negative. Since the link voltage polarity is uni-directional single transistors, or GTOs may be used as switches. One possible configuration is shown in Figure 2.12(a). This circuit has many similarities to the parallel-resonant AC link converter shown in Figure 2.11. The main difference being the addition of a DC offset capacitor, C_0. This biases the link voltage to ensure it does not become negative. This allows uni-directionally blocking switches to be used. Figure 2.12(b) shows a different embodiment. Because of the DC supply, the link bias is an inherent property of the circuit, which negates the use of C_0. A potential problem with this circuit is the high voltage which is applied to the switching devices, which may be well over twice the supply voltage. This increases the cost of the converter, or may make its use unfeasible in certain applications. A solution to this problem is *clamping* which is described in more detail below.

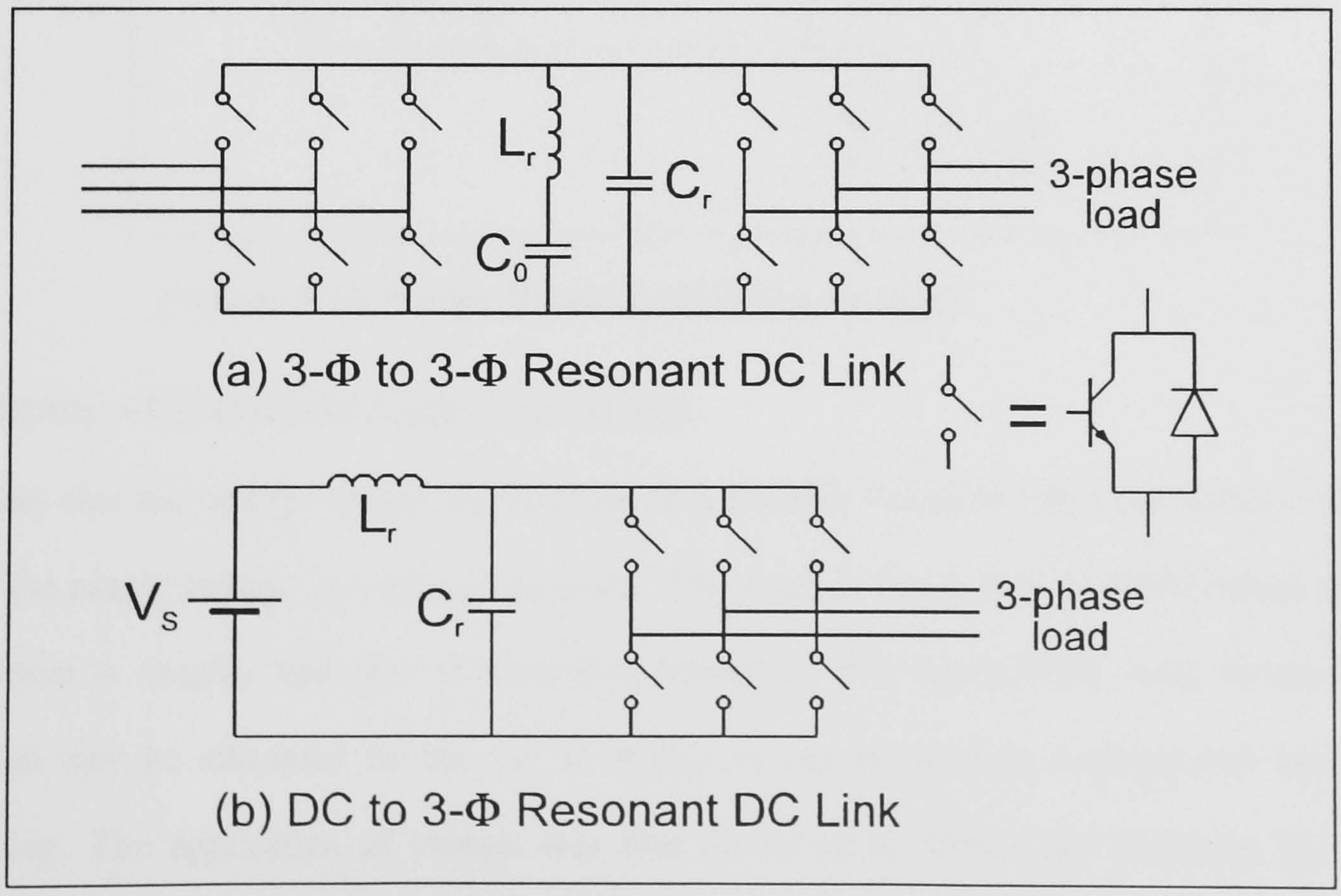

Figure 2.12 Resonant DC Voltage Link Converters

Series-Resonant DC Current Link Converter

The series-resonant DC current link converter is the circuit dual of the parallel resonant DC link converter. In this circuit it is the link *current* which experiences a DC bias rather than the voltage. This topology was proposed by Murai and Lipo in 1988 and is shown in Figure 2.13. [20] The current bias is achieved by means of inductance, L_0. Because the current flow is unidirectional, the switches need no inverse parallel diode. Also because of the current zeros the conditions exist for commutation of thyristors which is a key advantage due to their low cost, ruggedness, and high current carrying capability. In common with the Resonant DC Voltage Link Converter this circuit suffers a slight disadvantage due to the action of the resonant components. This leads to the peak current in the switches being very much higher than the supply currents. This may not be a serious drawback though since thyristors are available with very high peak current capabilities at modest cost. However clamping arrangements are possible to restrict the peak current requirement.

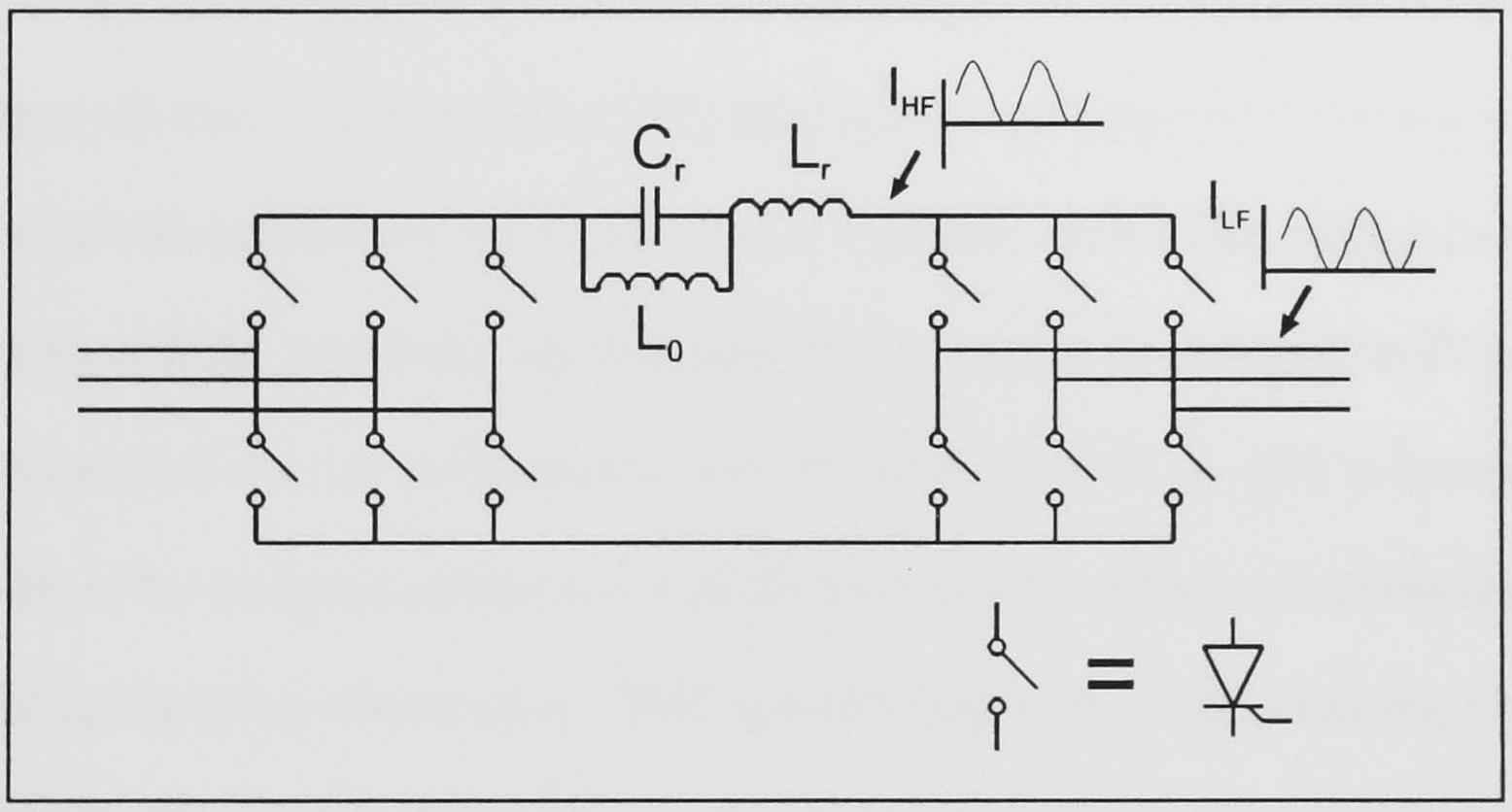

Figure 2.13 Series-Resonant DC Current Link

Clamping of Resonant Link Converters

The fact that the voltage across the switches of a Parallel Resonant DC Link Inverter reaches twice the supply voltage is a severe limitation. The result of this is that the RMS output of such converters is roughly half that of fixed link converters with equivalently rated devices. This problem may be alleviated by the use of voltage or current limiting arrangements known as *clamping*. The application of clamps was first discussed by Divan and Skibinski [2]. They proposed several schemes, the simplest being a passive clamp involving a transformer, which

limits switch stress to 2.5 times the supply voltage (V_S). This is shown in Figure 2.14(a). This circuit has low levels of *dv/dt* and *di/dt*, and consequently generates low levels of Electromagnetic Interference (EMI). Additionally it is simple and rugged. However the clamping level of $2.5V_S$ is onerous for the switching devices and common application may not be seen until higher voltage devices become widely available. A more suitable clamping arrangement for currently available devices is shown in Figure 2.14(b). This limits voltage excursions to $1.2\text{-}1.4V_S$ giving switch voltage-blocking requirements comparable with hard switching converters. The disadvantages associated with this circuit are increased complexity, higher EMI due to the rapid switching of the clamp device, and increased complexity of control. However this topology allows more flexibility in the control of the resonant circuit and can lead to significant improvements in circuit operation as described by Divan *et al.* [21] The circuit of Figure 2.14(b) is referred to as a *boost clamp*. A similar embodiment is the *buck clamp*[2], shown in Figure 2.14(c). In this circuit the peak voltage across the switches is clamped at V_S. This may be attractive in high voltage applications, however the *average* link voltage is less than V_S which might be considered unacceptable in terms of supply voltage utilisation. Lai and Bose [22] adopted a novel approach to voltage limitation by predicting the resonant inductor current before each resonant cycle. This allows presetting of the current to prevent voltage overshoot. By this method the voltage is clamped to $2V_S$. However an overall improvement in system performance was claimed. Smit et al [36] subsequently argued that optimisation of the resonant components could be used as a means of minimising the voltage overshoot, making clamping unnecessary. This would require the devices having a large voltage-withstand capability for reliable operation.

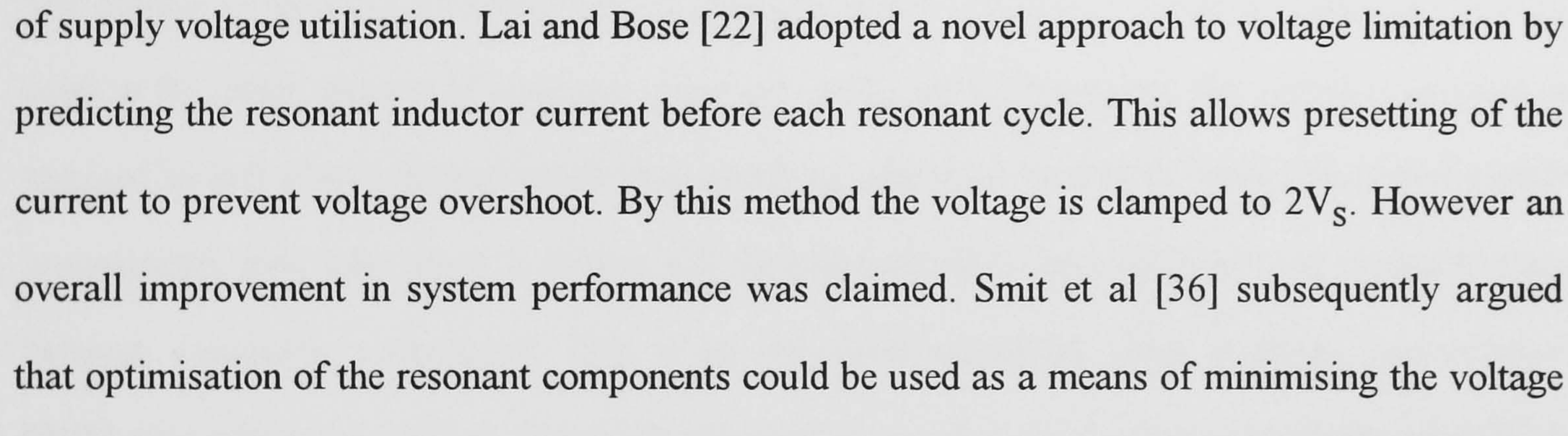

Figure 2.14 Clamped Resonant DC Link Converters

Similarly, clamping may also be used in series-resonant DC link converters to contain the current overshoots. This was investigated by Murai and Lipo [20]. Clamping was achieved by connecting a thyristor across the link capacitance, and about 10% of the inductance to divert the peak resonant current from the switches.

2.2.4 Resonant Switch Converters

There are many topologies which fall into this class. They are characterised by having periods of non-resonant operation interspersed with resonant behaviour. The resonance is used to shape the switch voltage and current at the moment of commutation to achieve zero-voltage or zero-current switching. Included in this class are converters referred to as *resonant-pole*, *pseudo-resonant*, *resonant-transition*, or *quasi-resonant mode*. Because of the subtlety of the differences between topologies, no attempt will be made to assign sub-classes to these converters. Instead the general properties will be discussed, and an example of a resonant-switch converter given.

The manner of avoiding switching loss in resonant-switch converters is basically the same as that used in the other classes of resonant converters seen above. However, the resonant process is engaged as and when required rather than involving continual resonance. This means that switch commutation may take place at almost any desired interval in time (subject to a minimum time between successive switchings). This is an important advantage since it allows conventional PWM strategies to be applied, giving a better control over harmonics than is available using High Frequency Link, or Load-Resonant types. Despite this significant advantage, a major drawback of this type of converter is the high component count, or large current overshoots which occur. [2,21,23] Despite this, the topologies are suitable for high power use and may become more prevalent as devices and passive components improve.

Figure 2.15(a) shows the basic form of a resonant switch (or pole).[23] Each switching device has a resonant capacitor C_r in parallel with it. The output of the pole is via inductance L_r which provides the conditions for resonance. When current is flowing through one of the switching devices, T1 or T2 it is possible to turn the device off with very low losses since the rate of rise of

voltage is slowed by the resonant capacitor. The switch current transfers to both resonant capacitors causing the pole voltage to resonate to the opposite rail voltage. Once this rail voltage has been reached the opposite diode (D2 or D1) begins to conduct, clamping the pole output voltage. The opposite switch (T2 or T1) may then turn on without loss since its parallel diode is conducting. A similar process occurs when this switch is turned off. Figure 2.15(b) shows the voltage and current waveforms for the resonant pole. It can be seen that the switch voltage is clamped at the supply voltage. However due to the resonant effect, the peak current stress on the switches is higher than for the equivalently rated hard switching inverter. In a 3-phase inverter the resonant components must be replicated in each pole, which makes the overall component count rather high.

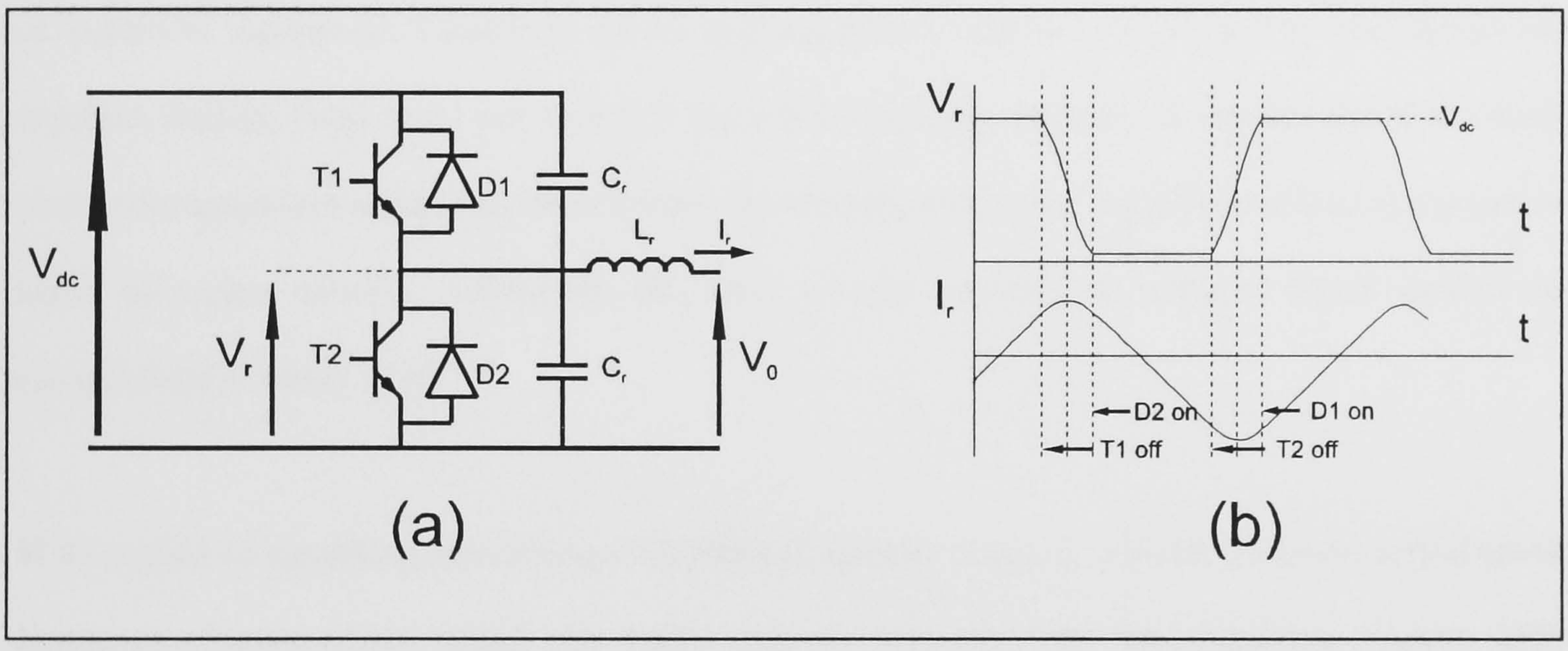

Figure 2.15 A Resonant Pole

2.2.5 Summary of Resonant Converter Classification

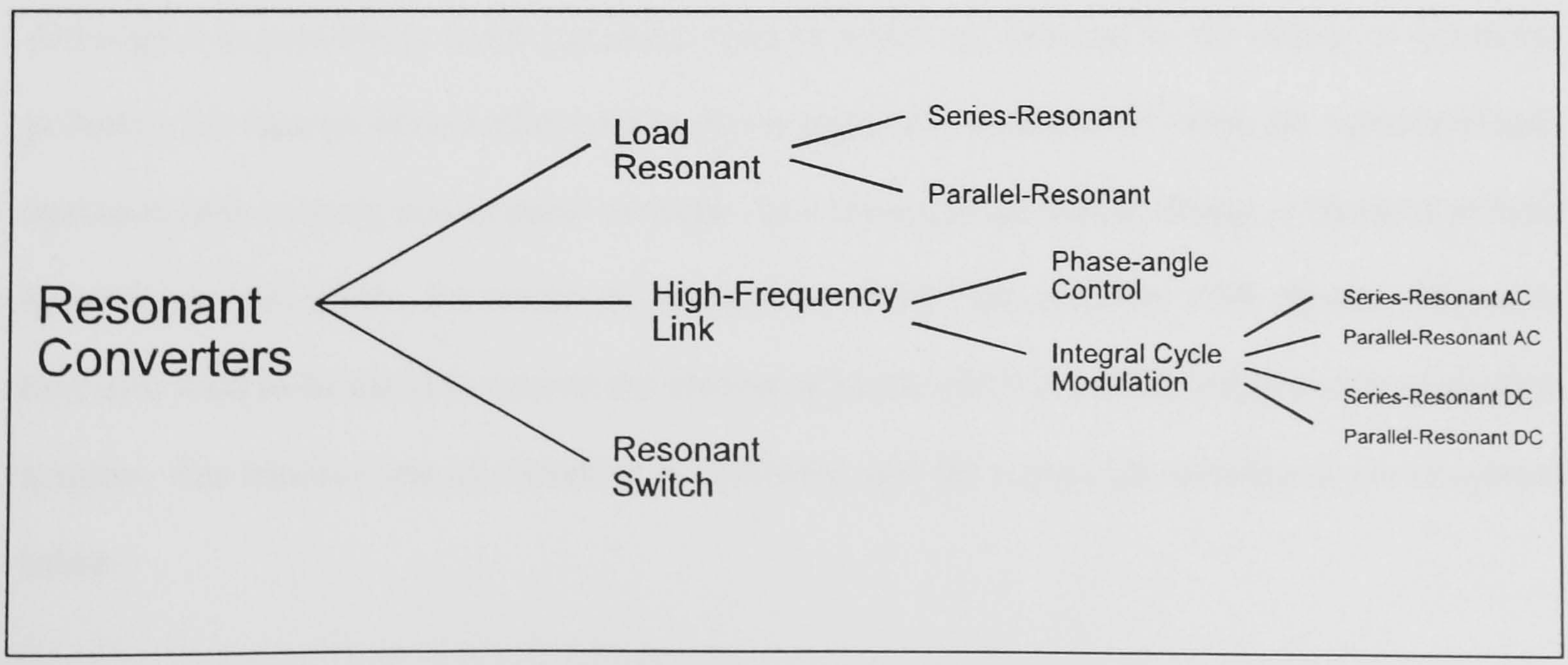

Figure 2.16 Summary of Resonant Converter Classification

2.3 Electromagnetic Compatibility in Railway Equipment

2.3.1 Introduction

The special needs of electrical equipment supplied for use on railways provided the impetus for the work described in this thesis, though the findings are applicable in many other areas. In this section the problem of Electromagnetic Compatibility is reviewed which is of particular importance in the rail traction field due to the co-existence of high power converters and relatively low-power signalling and communications equipment. To prevent collisions on railway systems it is of vital importance that the signalling system detects which sections of track are occupied by vehicles. A failure to do this accurately could cause the loss of many lives and/or a large amount of expensive equipment. Clearly to ensure safe operation, vehicles on the railway and the power supplies feeding them must not interfere with the signalling process. A similar problem exists with communication equipment. Interference by vehicles and power supplies can lead to excessive noise on voice circuits, corruption of data, or even present an electric shock hazard to maintenance workers. [24]

With regard to signalling interference, 'traditional' electric traction vehicles generate well-defined harmonic characteristics which are fairly easy to integrate into the signalling system. [25] However with the advent of three-phase drives, the potential exists for any frequency to be generated by the vehicle which presents the danger of interference with the signalling system. Although it is possible to make signalling systems which are immune to the effects of harmonic pollution, for reasons of cost effectiveness drives must be manufactured which are capable of safe operation over existing non-immune systems. As a consequence careful design is required to limit to predetermined levels, harmonics at frequencies which may interfere with signals. Measures may also need to be taken to control the amount of noise which is introduced into communication systems. The mechanisms of signalling interference, and the means for avoiding it are discussed below.

2.3.2 Review of Signalling Systems and Interference Mechanisms

The most common means by which trains are located is by the use of *track circuits*. These consist of a transmitter which connects between the two running rails at one end of a *section*, and a receiver which detects the signal at the other end. When no vehicle is present the receiver is energised by the transmitter's signal. When a vehicle enters the section its axles short the running rails together which prevents the signal from reaching the detector. The detector de-energises as a result of this. Conventional track circuits operate at one particular frequency, or band of frequencies, which vary from system to system. The potential exists however, for a source other than the transmitter to generate an in-band signal which the detector cannot distinguish from the genuine signal. This is a particular concern in electrified railways where the power supply and vehicles are prolific harmonic generators. The track circuit may be falsely energised by in-band harmonics which leads to a *wrong-side* failure. This is an extremely dangerous situation since a section which may be occupied by a vehicle is flagged as being empty. Thus a collision between two vehicles is possible. Another possibility is that of a *right-side* failure. This is where a track circuit is falsely de-energised by an interference source. This is not dangerous, despite being highly undesirable from an operations point of view. The bandwidth of the signalling system is selected to avoid frequencies which are inherently present in the supply system. For example in DC supplied railways a 50Hz signalling system may be used. In AC supplied railways DC or $83^{1}/_{3}$Hz may be used, though there are many other possibilities. Interference in signalling and communication circuits may be classified by the way in which the interference source couples with the circuit. These coupling mechanisms are described in more detail below.

2.3.2(i) Conductive Coupling

This occurs where two circuits share a common conductor either by design, or due to return currents flowing in the ground. This is a significant effect in *single-rail* track circuits as shown in Figure 2.17, and *double-rail* track circuits as shown in Figure 2.18. The single-rail track circuit is commonly used in the vicinity of points and crossings where it is easier to accommodate than the double-rail type. In this system one rail contains insulated joints which define the section ends, the other is a continuous conductor which constitutes the return path for the traction current. The

voltage drop which this return current develops appears in the track circuit loop and is a potential source of signalling interference. If the impedance per unit length of track is Z, the voltage drop between signal rail and return current rail for a component of return current having angular frequency 'ω' is given by: $V(j\omega) = Z(j\omega) * l * I_T(j\omega)$, where '$l$' is the distance from the receiver to the vehicle. If there is a broken (i.e. electrically disconnected) rail the return current may take a more tortuous path which increases the value of 'l' and also the magnitude of the interfering signal.

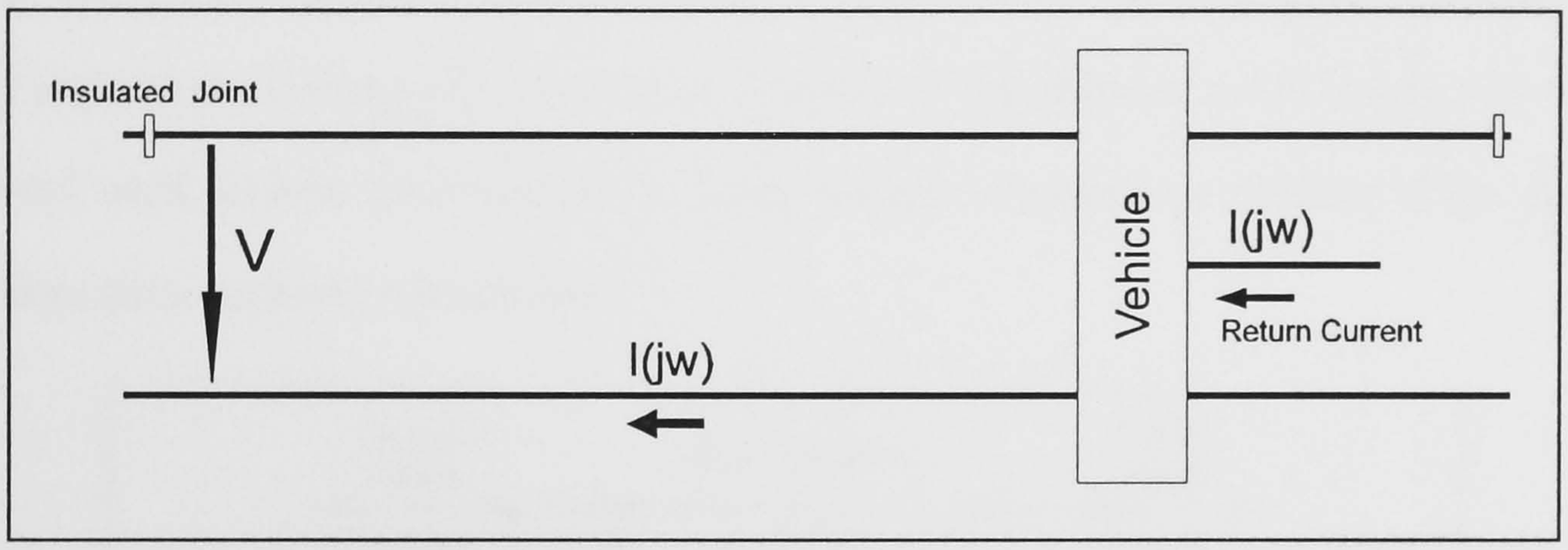

Figure 2.17 Single-Rail Track Circuit

Figure 2.18 shows a double-rail track circuit. These are used extensively in plain areas of track. The section ends are defined by insulated gaps in both running rails. *Impedance bonds* provide continuity for the traction return current, but present a fairly high impedance to the track circuit signal which is at a relatively high frequency. If the return current is divided equally between the rails there is no disturbing voltage applied to the track circuit receiver. However imbalance may be caused due to a broken rail, or by the close proximity of another conductor, such as the 3rd rail power supply conductor in a 750V DC system. The disturbing voltage, V(jω) is defined by; $V(j\omega) = Z(j\omega) * l * \left(I_1(j\omega) - I_2(j\omega)\right)$, where l is the distance from the vehicle to the receiver.

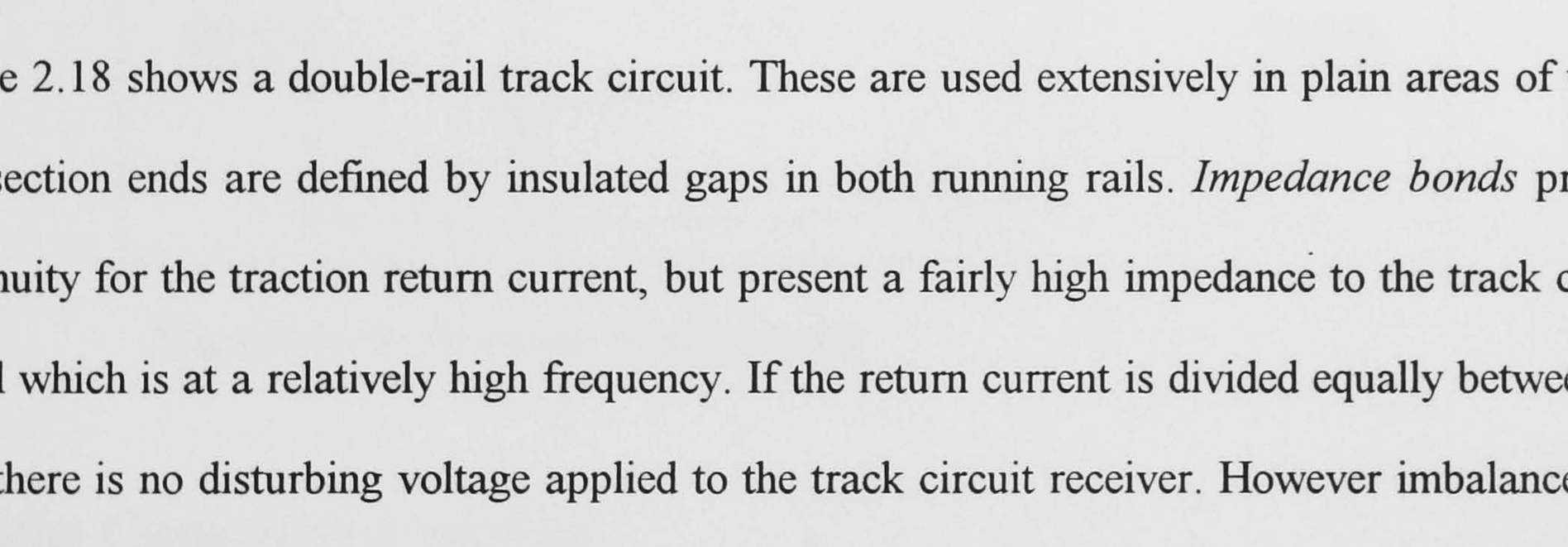

Figure 2.18 Double Rail Track Circuit

Heavy, expensive impedance bonds, and rail electrical discontinuities can be avoided by using *jointless track* circuits. This system exploits the inherent longitudinal impedance of the running rails to define the sections. A typical arrangement is shown in Figure 2.19. The transmitter develops a resonant current in the tuned circuit at the feed end. A small proportion of this current flows into the main section. At the receiving end a short circuit marks the end of the section, whilst a further tuned area enables the track circuit signal voltage to be detected. To avoid cross-talk between sections, different operating frequencies are used. Early jointless track circuit systems were 'carrier-only' and thus susceptible to interference. An imbalance in traction return current between the running rails constitutes a source of interference in this system, as with the double-rail track circuits described above. Later systems employed modulation of the carrier to make them more immune to interference.

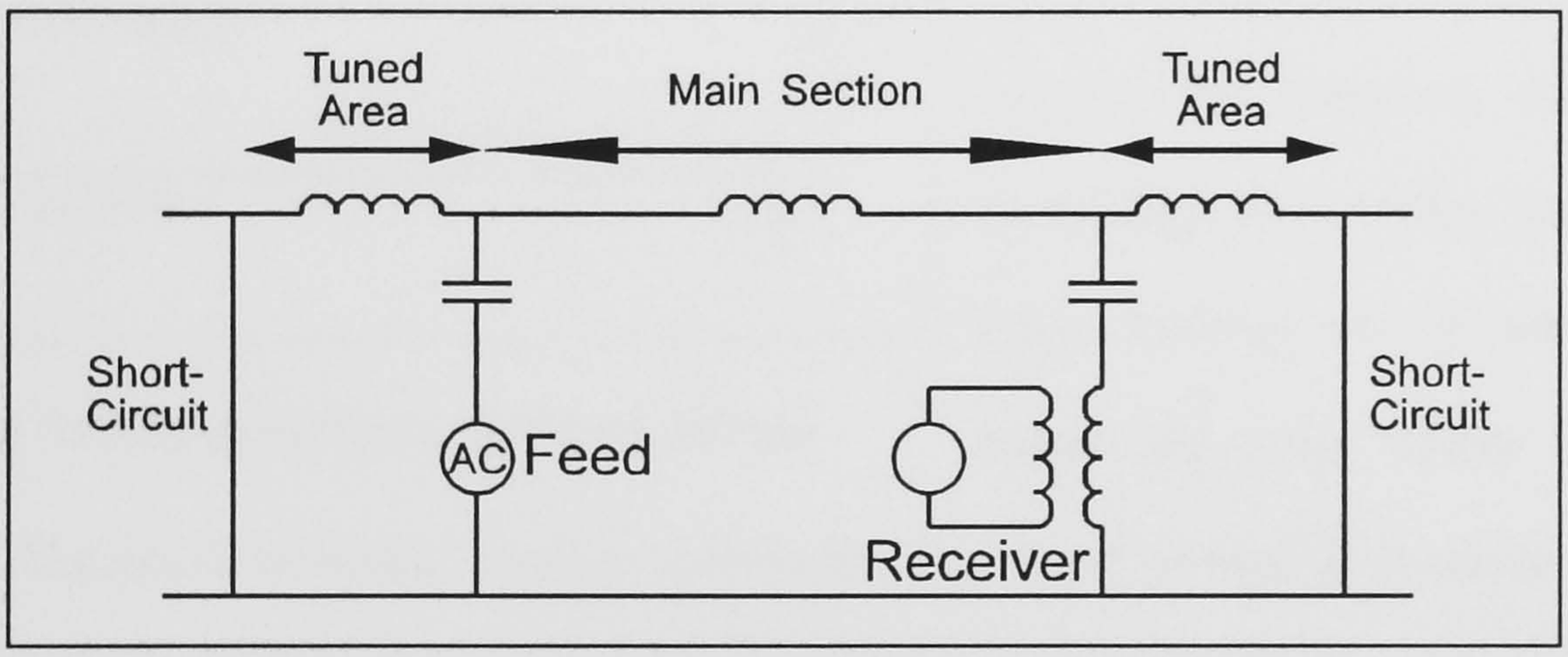

Figure 2.19 Jointless Track Circuit

2.3.2(ii) Capacitive Coupling

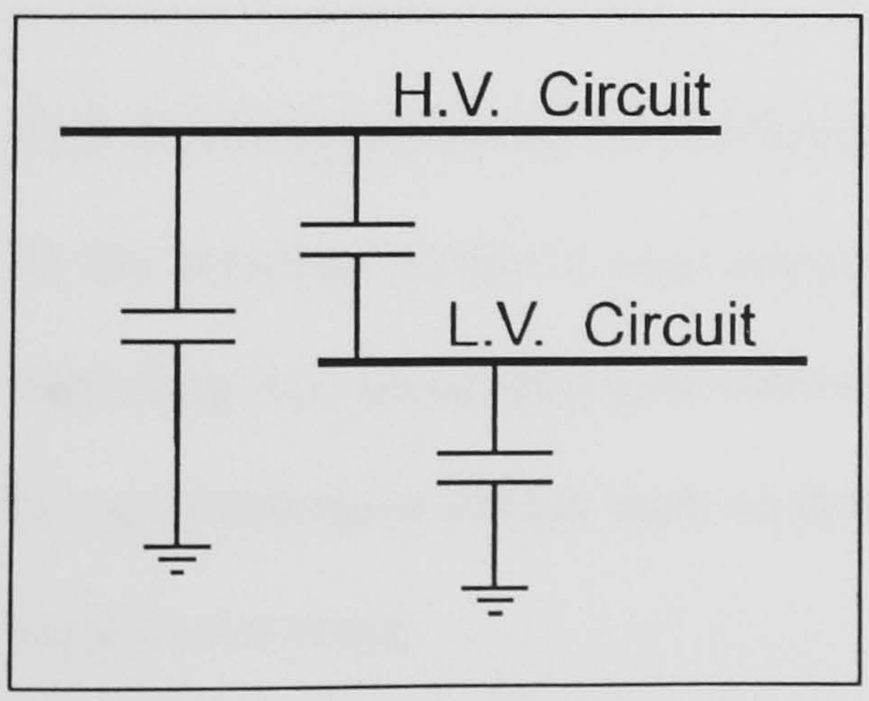

Figure 2.20 Capacitive Coupling

This mechanism of coupling occurs where there are time varying voltages and is more significant where the value of *dv/dt* is high. As a consequence, high voltage power supply cables and inverter or chopper equipment can introduce interference into high impedance signalling and communication systems by this route. Figure 2.20 demonstrates the capacitive path which the interfering signal takes.

2.3.2(iii) Inductive Coupling

Inductive coupling effects manifest themselves in various ways, but are all due to time variations in current. The most important mechanisms are:

- Direct induction by under-car mounted equipment
- Mutual induction between parallel but earth-isolated circuits.
- Mutual induction between parallel circuits which are referenced to ground.

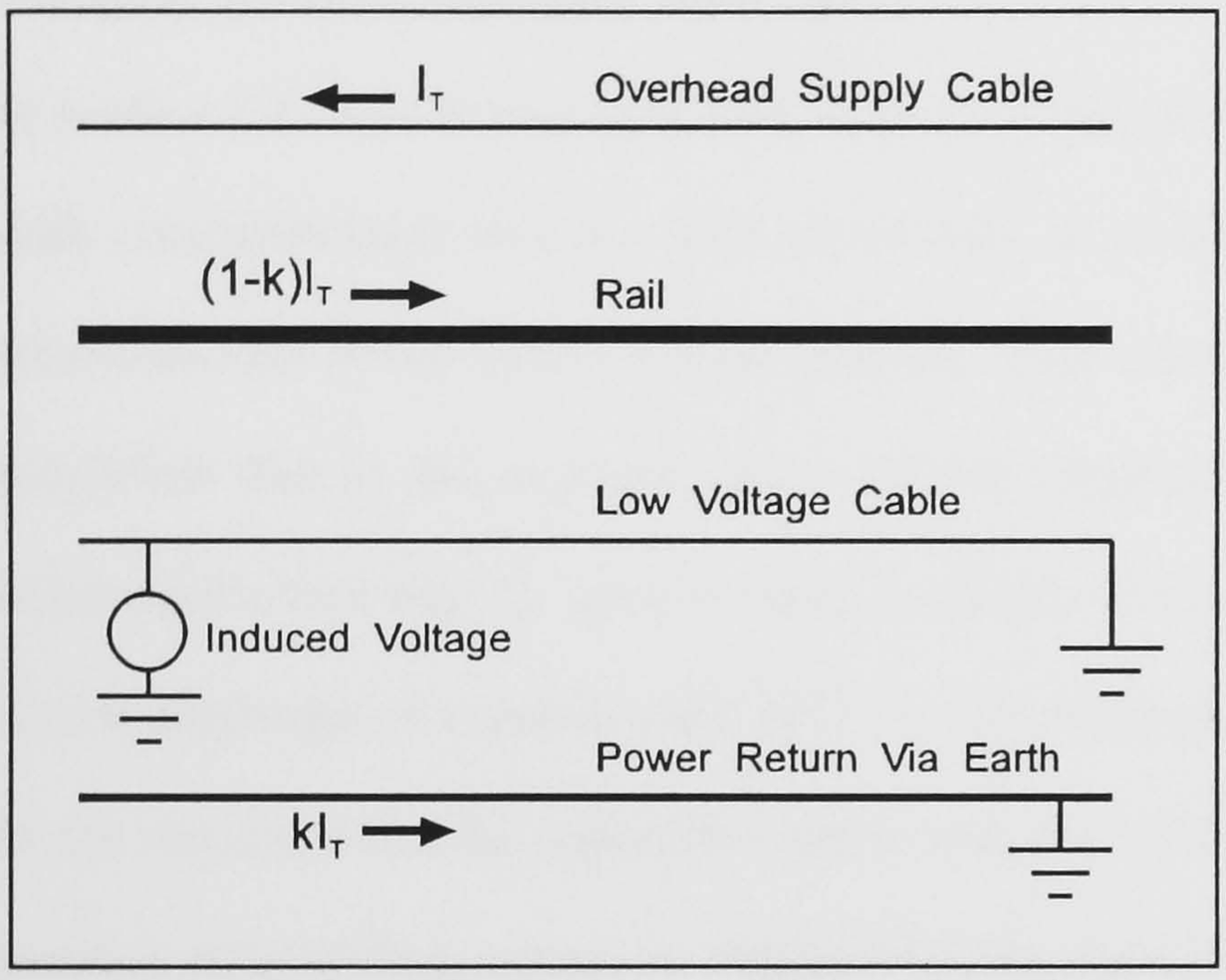

Figure 2.21 Mutual Inductance; Earthed Circuits

Inductive effects are an important issue where mains frequency signalling is used due to the potential for interference from nearby power cables. Induction between circuits connected to ground is a particular problem in railway systems due to the practical difficulties of preventing the traction return current from entering the ground especially where the track ballast is wet and conductive. The result of having traction current flowing in the ground is to create a very large induction loop between traction power supply conductors, and other circuits connected to ground. This applies especially to telephone circuits which are referenced to ground, and constitutes the main source of interference in such systems. Figure 2.21 represents this situation. The interfering voltage induced in the telephone circuit is shown as a lumped source.

2.3.3 Mitigation of Interference Effects

In the previous section it was explained how interference sources can couple with low-voltage signalling and communication circuits. For safe and reliable railway system operation to take place, interference effects such as these must be prevented, or at least attenuated. This may be done in two ways:

- The source of interference can itself be controlled
- The signalling and communication systems can be made less susceptible to interference

Considering the first point, there are two sources of harmonics; [26] either the power supply system, or on-vehicle power conversion equipment. However there is some interaction between these two mechanisms as explained in section 2.3.3(iii). The effects of power conversion equipment are the most relevant to the work described in this thesis, but for completeness other key signalling interference avoidance techniques will be briefly outlined below.

2.3.3(i) Power Supply Effects

In section 2.3.2(iii) it was seen how earth currents can cause problems due to inductive coupling with communication circuits. This effect may be reduced by restricting the amount of traction return current which flows via the ground. This cannot in practice be effectively achieved by insulation due to the exposed nature of the running rails. However current transformers, or autotransformers may be used to force a balance between the current in the feed conductor and return conductor or running rails. [27] By constraining the return current to flow in a conductor or the running rails, the induction loop is reduced, which reduces the problem of interference. In practice magnetising current is required by the transformers and the current containment is not perfect as a consequence.

2.3.3 (ii) Reduction of Signalling Susceptibility to Interference

Communication and signalling systems may be made more immune to interference effects by the use of screening. To implement this, a conducting structure or sheath is placed around the signal-carrying conductors. Frequent connections are then made from the sheath to ground. Clearly this is not an option for the long exposed stretches of running rail which also carry signals. This problem is tackled in modern signalling systems where the transmitter may *code* its output. This is usually done by modulation of the carrier. Amplitude Modulation, Frequency Modulation, or Frequency Shift Keying (FSK) may be used. With FSK transmission the signal can be in the form of a digital message. The advantage of coding is that it reduces the probability of a potential interference source from producing a signal which may be mistaken for a genuine track-circuit signal. The more complex the coding the less likely it is that interference will take place. Indeed

such systems are termed traction immune because of the extremely low probability of disturbance by external sources.

2.3.3(iii) Preventing Inverter Drives from Interfering with the Signalling System

Although traction immune systems are available, replacement of complete existing systems is an extremely expensive undertaking. As a consequence it is cost effective to ensure that new vehicles can operate safely with existing signals. Compatibility can be achieved by careful design of the vehicle power conversion equipment. Potential interference sources which have their origin in the power supply system are of interest to vehicle equipment designers, as well as those generated by the converters themselves. The reason for this is that the input impedance of the converter determines the magnitude of the interfering current which flows. If it can be verified that the power supply is inherently incapable of generating harmonics at signalling frequencies then it may not be necessary to consider the input impedance.

The harmonic currents which the converter generates are ultimately determined by the output of that converter. This in turn is a function of the modulation strategy. As a consequence, selection of the modulation strategy is pivotal in ensuring signalling compatibility [30]. It is possible, through appropriate modulation of the inverter to achieve *harmonic elimination* [31] whereby specific harmonics may be removed from the output spectrum, which leads to harmonic elimination on the input side also. However, due to the modulation process which takes place, two harmonics must be eliminated from the output side to eliminate one harmonic from the input. Harmonics at frequencies above the nominal operating frequency of the converter cannot be eliminated, but may be *minimised* if necessary. If there is a risk of signalling interference by these high frequency harmonics, filters may be employed. In some cases it is sufficient to employ a harmonic minimisation strategy for the entire frequency range, rather than attempt harmonic elimination. Sufficient filtering must be provided however, to limit in-band harmonics. This arrangement is particularly suited to AC supplied systems where the front-end converter and transformer provide attenuation. In an ideal harmonic elimination scheme, the inverter would be

perfectly symmetrical. In practice this is not the case due to parameter variation between components, both passive and active. The result of this is the emergence of otherwise eliminated harmonics. Normally this should not be a problem, but partial inverter failure could lead to serious magnification of this effect, allowing signalling interference to occur. To prevent this situation arising, it is common practice to install fail-safe monitors which shut-down the converter if harmonics at signalling frequencies exceed a certain limit.

Figure 2.22 demonstrates features of an output waveform used to achieve the harmonic elimination process in a hard-switched inverter. When using 'm' *chops* per half cycle, 'm' harmonics may be eliminated from the spectrum. In the figure, m is 2. This allows m/2 harmonics to be eliminated from the input side. The width and position of the chops determines which harmonics are eliminated, and are also responsible for controlling the amplitude of the fundamental.

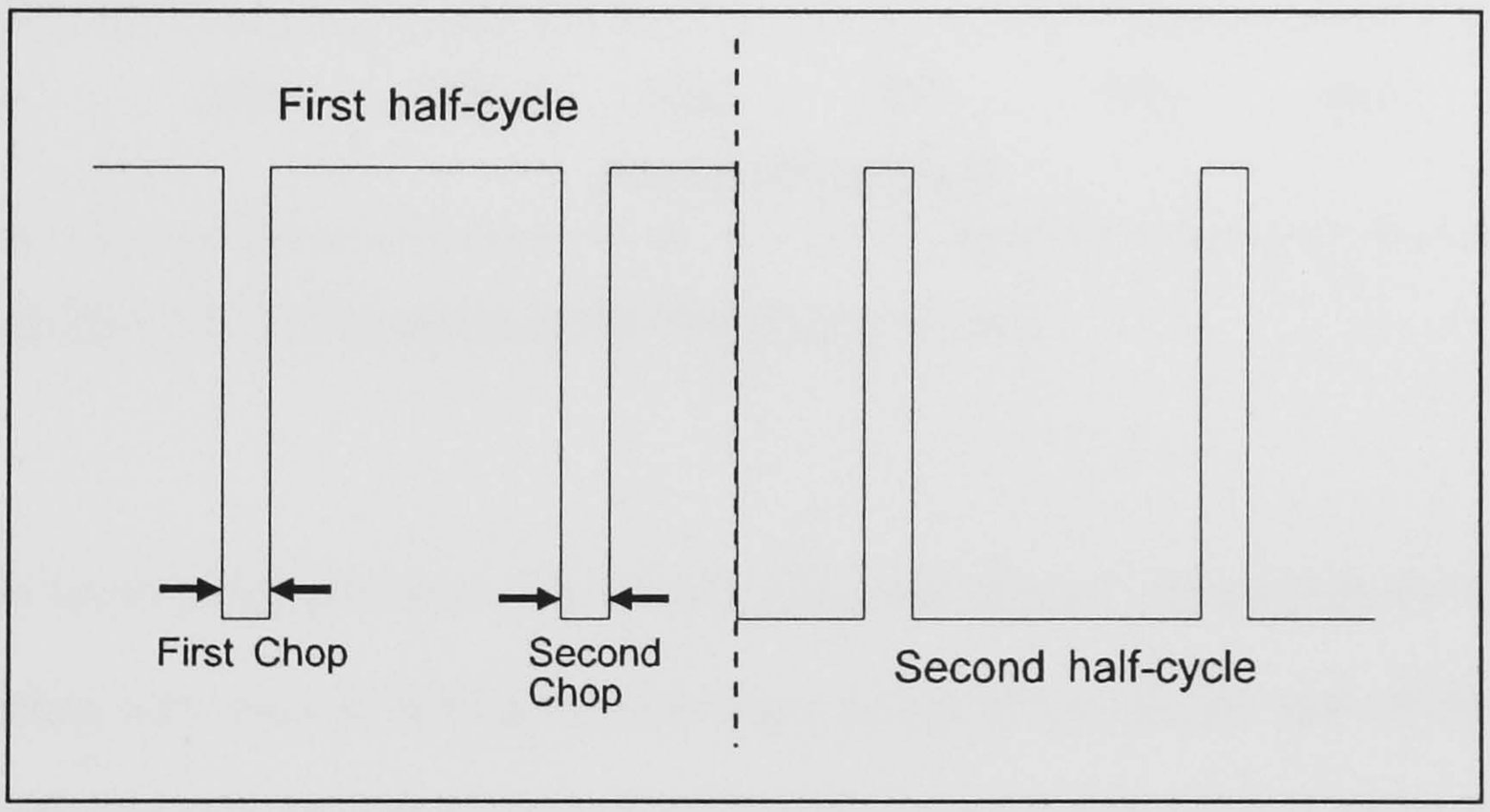

Figure 2.22 Harmonic Elimination PWM with m=2

2.3.4 Quantifying Interference

To allow evaluation of the effects of interference currents on communication circuits, a parameter known as the psophometric current is used. This 'current' is calculated by summing the harmonic currents flowing into a converter, weighted in such a manner that reflects the level of interference perceived by humans. Psophometric current, I_p is defined by:

$$I_p = \sqrt{\sum_{n=0}^{\infty} I_n^2 w_n^2}$$

I_n is the amplitude of the *n*th harmonic of the current waveform, w_n is its weighting factor. The weighting factors normally used are those advised by the International Telegraph & Telephone Consultative Committee (CCITT) in their recommendation No. 041. Figure 2.23 shows the CCITT psophometric weighting curve.

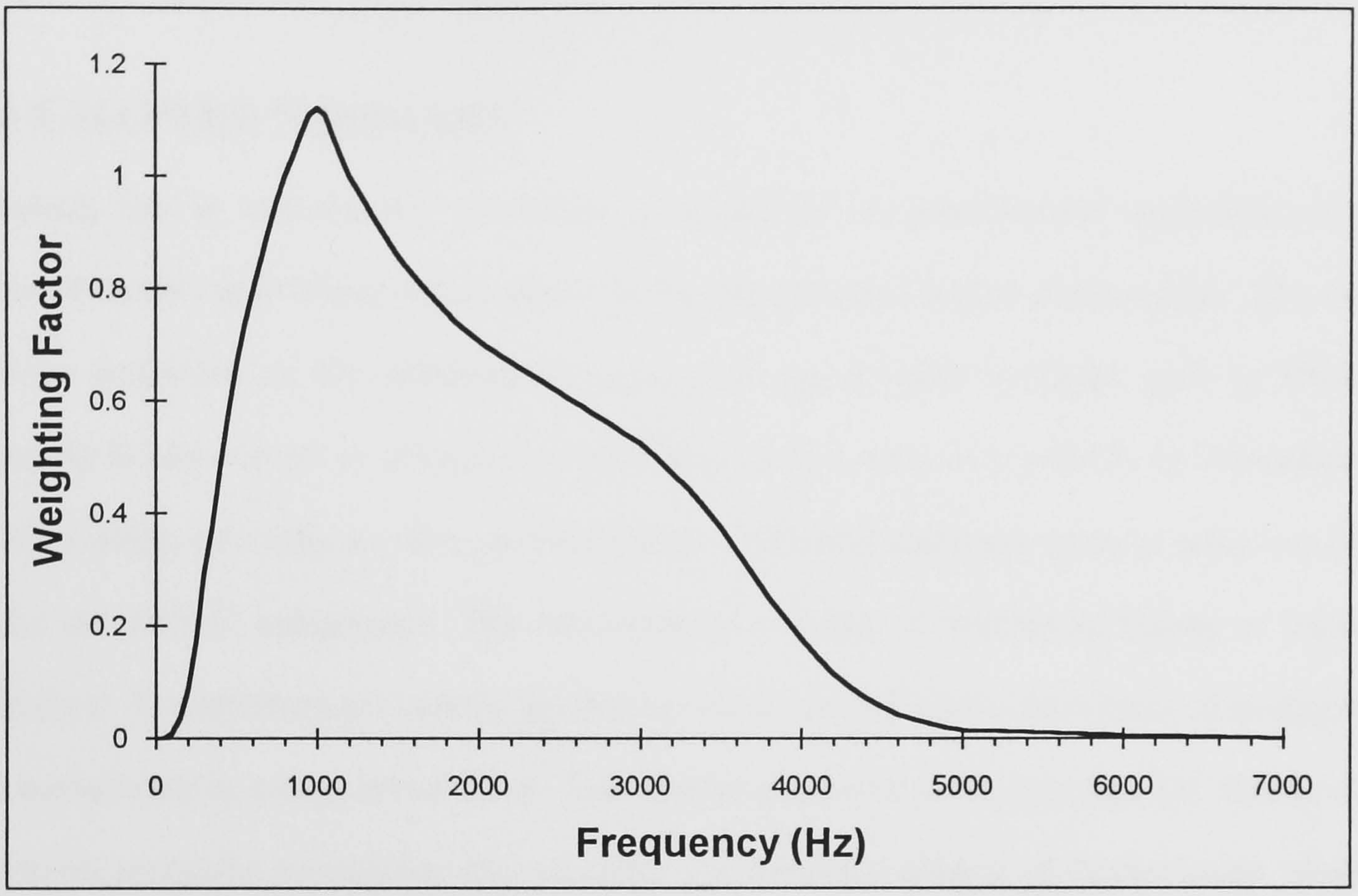

Figure 2.23 CCITT Psophometric Weighting Curve

The acceptable levels of interference vary greatly from one railway administration to another, and this must be taken into account during the converter design phase. In the case of British Rail the levels are established by a specification known as BR1914. [32] A vehicle which complies fully with BR1914 can operate safely (from a signalling point of view) over any section of British Rail track. This is however, an extremely onerous requirement since the specification covers all types of track circuit in existence on BR, and at their most sensitive set-up. If a vehicle is restricted to particular routes then due to the reduced number of signalling systems encountered, it may not be necessary to comply fully with BR1914. This reduces the design complexity and expense of the vehicle concerned, but does restrict the vehicles flexibility and could have far-reaching implications for its use in the future.

BR1914 includes interference levels for harmonics generated by the vehicle or power supply, direct radiated emissions, input impedance and psophometric current. Compliance with the specification must be proven before a vehicle is accepted for use on BR tracks. It is not possible to build a system which can be mathematically proven to *never* fail and in understanding this, British Rail require proof that no more than one undetected failure shall occur in 5.10^9 hours.

2.4 Chapter Summary

Switching loss in 'conventional' converters is caused by the simultaneous application of high values of current and voltage which occurs during the period of switch commutation. This forces a severe restriction on the switching frequency, and causes other problems such as EMI. By arranging for the current or voltage to periodically become zero, it is possible to commutate the switches whilst incurring very low switching losses. The most common means of achieving this is by the use of L-C components. This characterises a family of converters known as 'resonant converters'. Though there are various topologies, many suffer from the drawbacks of having large L-C components or a high device count. One notable exception is the Resonant DC link Inverter. Due to its promising capabilities this topology was made the subject of further study, which is described in this thesis.

When designing power converters for use in the rail traction environment, it is necessary to take account of the effects of interference to ensure that the converter does not prevent the correct operation of the signalling systems or introduce noise or data loss into communication circuits. This requires restrictions to be placed on harmonics generated by converters. The acceptable levels for harmonic generation on British Rail are laid down in the specification BR1914. To allow development of secure systems such as this, it is advantageous to be able to simulate the converter in question. This forms the subject of the next chapter, with a particular emphasis on simulation of the Resonant DC Link Inverter.

Chapter 3

Frequency-Domain Modelling and Simulation of Resonant DC Link Converters

3.1 The Simulation Program

3.1.1 Introduction

To efficiently develop converter topologies and modulation strategies, it is highly desirable to be able to model and simulate the system in question. Simulation may be done using a time-domain method [33], by a frequency-domain method [34], or by a combination of both. The advantages and disadvantages of time and frequency domain methods are outlined below [35,38]:

Time Domain

Advantages:

- Allows the transient response of a system to be modelled

Disadvantages:

- The timesteps taken by the simulation must be small if quantisation errors are to be avoided. This can lead to long simulation run-times. This may be a particular problem when using commercial simulation packages, such as Mentor Graphics' 'Accusim' where the step size is chosen automatically. In the presence of fast switching edges the timestep may be reduced to very small values to attempt to maintain a certain calculation accuracy. The run-time then becomes extremely extended, and in extreme cases the program may stop with an error.
- To establish steady state conditions the simulation may have to be run over many cycles. This further increases simulation time. The inclusion in the circuit of large filter components with long time constants further exacerbates this problem.

- It is often desirable to incorporate the effects of the switching times of semiconductor devices to give a realistic impression of converter behaviour. However to do this accurately demands very short timesteps, and as a consequence devices must be treated simply as ideal switches with zero commutation time.

Frequency Domain

Advantages:

- Computation time is very short compared to time domain methods.
- Due to the rapid computation, complex effects such as device switching time may be incorporated.

Disadvantages:

- Does not allow transient response to be calculated.

In many cases the necessity to simulate the transient response will dictate the use of time domain methods. However, vary large savings in computation time can be made if only the steady state response is needed. The work described in this thesis involves the preliminary investigation of modulation strategies, for which steady-state analysis is perfectly adequate. The remainder of this section describes the development of a frequency domain simulation program which was developed for the purposes of testing modulation strategies for Resonant DC Link Inverters.

3.1.2 The Resonant DC Link Inverter

The specific circuit topology which was modelled and simulated was the Actively Clamped Resonant DC Link Inverter (ACRDLI) as depicted in Figure 3.1(a), although the principles demonstrated could be applied to many other types of converter. In the circuit shown, the clamp switch, T_c, is controlled in such a manner which causes the link voltage to resonate down to zero volts under the influence of the resonant components L_r and C_r. In the no-load case this results in a pulsating link voltage, which is clamped to prevent it rising above a given value as shown in Figure 3.1(b). The operation of the resonant circuit is explained in more detail below:

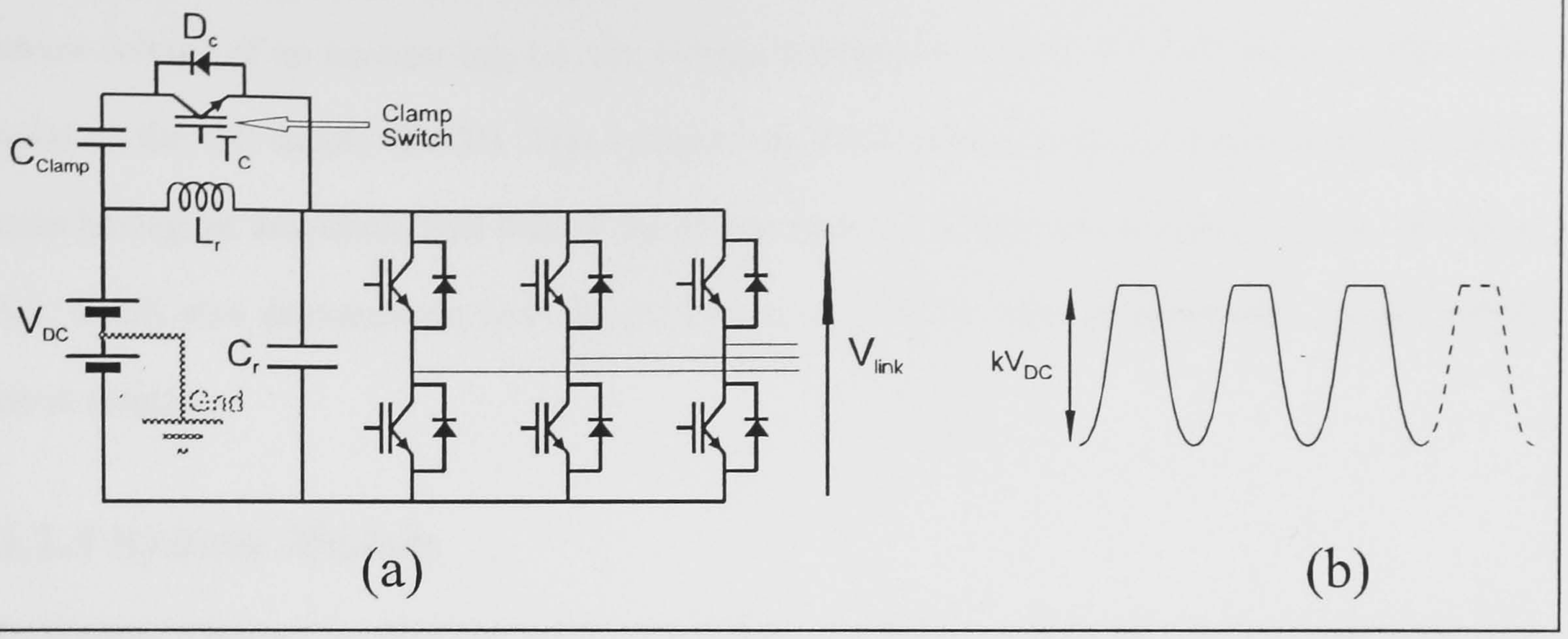

Figure 3.1 Actively Clamped RDCLI and Link Voltage Waveform

Let the voltage on the clamp capacitor, C_{clamp} be $(k-1)V_{DC}$, where k is typically 1.2-1.8. V_{DC} is the DC supply voltage.

- Assume that initially the link voltage, V_{link} is rising. When V_{link} reaches kV_{DC} the diode D_C forward biases, clamping the link voltage and causing the resonant current to flow onto C_{clamp}.
- The clamp switch may then be turned on without loss because the voltage across it is clamped at the forward voltage of D_C.
- The voltage on the clamp capacitor eventually causes the resonant current to reverse direction and flow back through clamp switch, T_C and L_r..
- The current is allowed to increase in L_r until it reaches a value which is sufficient to cause the link voltage to resonate down to zero during the next resonant cycle. At this point T_C is turned off.
- The link voltage resonates down to zero, and the process subsequently repeats.

When the link voltage is at zero the switches of the output stage may change state without incurring any switching losses, and are constrained to switch at these points as a consequence. Thus the output of such converters consists of a series of discrete pulses, selected from the link voltage waveform. Consider the

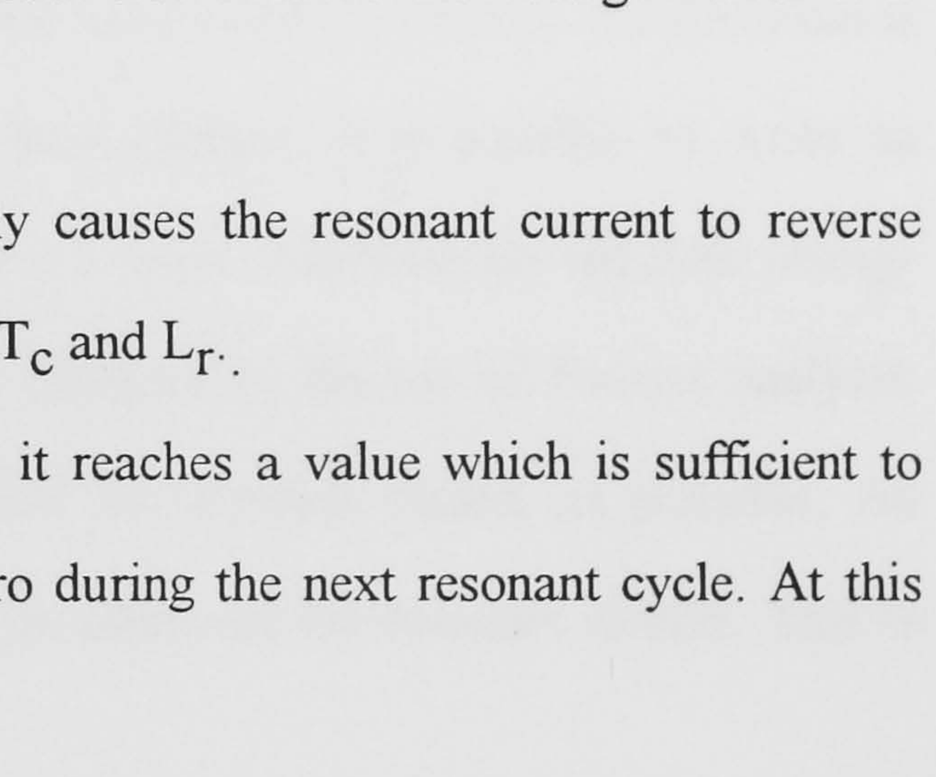

Figure 3.2 Phase Voltage

phase voltage of an inverter leg, i.e. the voltage between an output terminal and a notional mid-point on the DC supply (GND). This voltage waveform comprises positive and negative pulses, each having an amplitude half that of the link waveform. The phase voltage is shown in Figure 3.2, which also demonstrates how the pulses are selected in order to synthesise a given output wave shape.

3.1.3 System Models

In the next section the structure of the simulation program is discussed. In preparation for this, the mathematical models employed in the simulation are described below.

The first task in the simulation of the converter is to derive the harmonic spectrum of the pole voltage waveform to allow the phase currents to be calculated. When simulating 'conventional' hard-switching converters it is fairly easy to write a mathematical expression for the harmonic spectrum [35,37]. However in the case of the RDCLI, due to the complex shape of the pole-voltage waveform and its dependence on the instantaneous value of phase current, the spectrum is considerably more complex. As will be seen in the next chapter, it is possible to write an expression for the spectrum if simplifying assumptions are made. Alternatively the pole voltage may be simulated in the time domain and its spectrum obtained by the use of Fourier analysis. This method was adopted for the simulation, to afford as accurate results as possible. An approximate value of phase current is used to reflect its effect on the resonant circuit. This is explained in more detail in the next section.

The RDCLI may be represented by the simplified circuit depicted in Figure 3.3(a), where I_X represents the current flowing into the output stage of the converter. I_X is assumed to remain constant throughout each resonant cycle which is a reasonable assumption where the time constant of the load is long compared with the period of resonance. This is the case where the load is an induction machine. The shape of the voltage waveform on the resonant capacitor (v_C) is shown in Figure 3.4. It may be considered as consisting of 4 modes, which have been

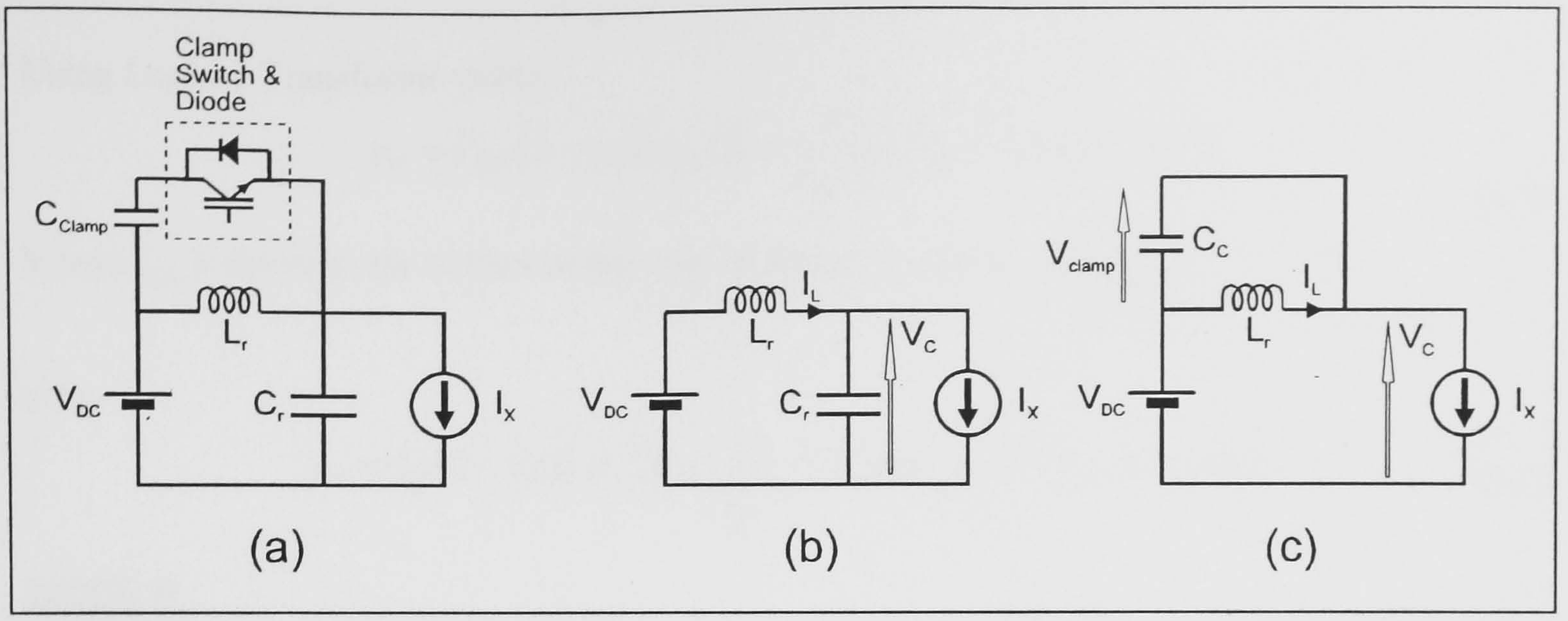

Figure 3.3 RDCLI Simplified circuit representations

indicated as A, B, C, and D. The equations describing the current (i_L) in the resonant inductance, and the voltage (v_c) are described below for each mode:

MODE A

During this mode the resonant converter may be represented by the circuit shown in Figure 3.3(b), assuming that the resistance of the components is negligible. The equations for this circuit may be written as follows:

$$V_{DC} = v_L + v_C \tag{3.1}$$

$$v_C = \frac{1}{C_r}\int i_C dt \tag{3.2}$$

$$v_L = L_r \frac{di_L}{dt} \tag{3.3}$$

$$i_L = I_X + i_C \tag{3.4}$$

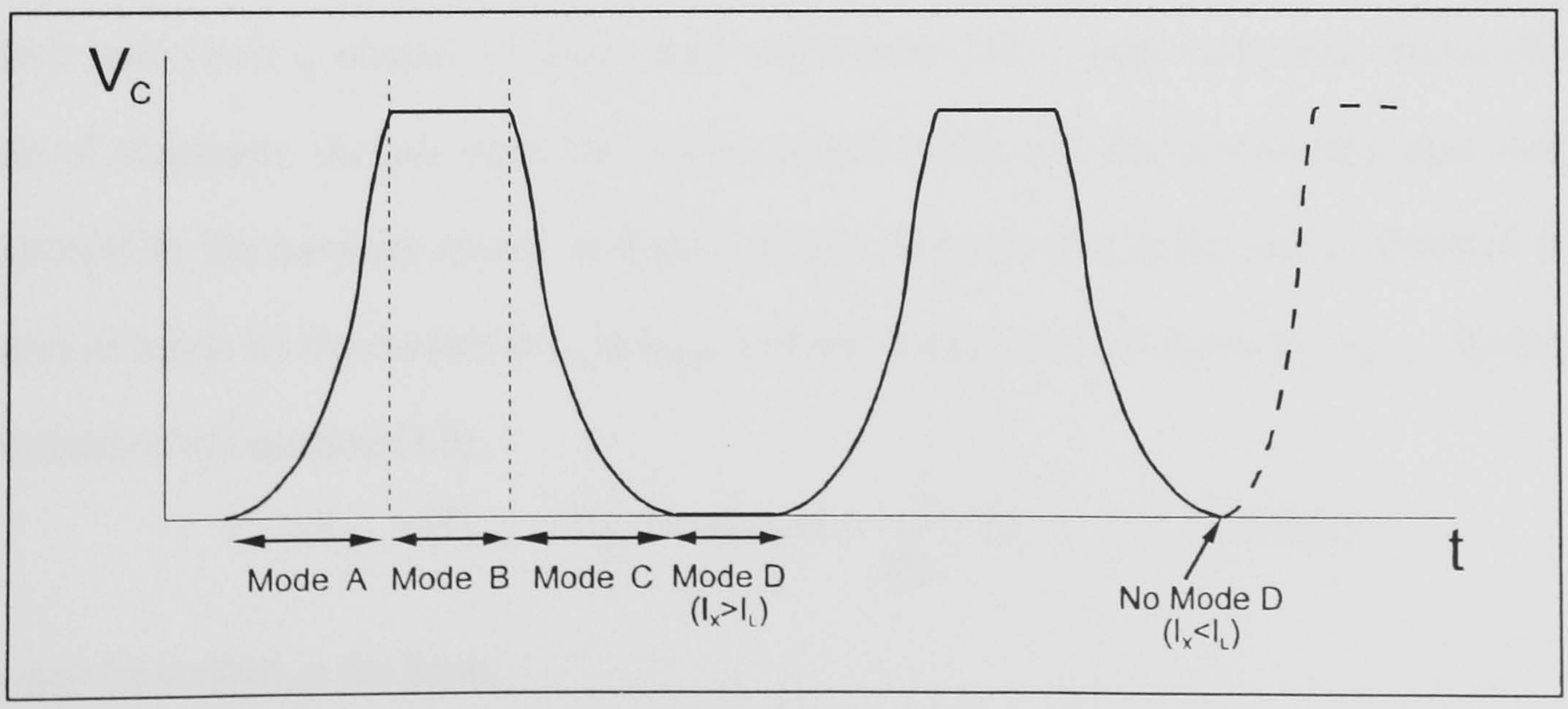

Figure 3.4 RDCLI Link Voltage Waveform

Using Laplace Transforms yields;

$$v_C = V_{DC}\left(1-\cos(\omega_0 t)\right)+\frac{1}{\omega_0 C_r}\left(I_{L0}-I_X\right)\sin(\omega_0 t) \tag{3.5}$$

Where I_{L0} is the inductor current at the start of Mode A, and $\omega_0 = \frac{1}{\sqrt{C_r L_r}}$

also,

$$i_L = I_X\left(1-\cos(\omega_0 t)\right)+\frac{1}{\omega_0 L_r}V_{DC}\sin(\omega_0 t)+I_{L0}\cos(\omega_0 t) \tag{3.6}$$

MODE B

Mode B begins when the clamp diode forward biases causing the resonant current to flow onto the clamping capacitor, This occurs when $v_c = kV_{DC}$. During this mode it is assumed that the voltage change on the clamping capacitor is small, thus the voltage on C_r remains practically constant and the current flowing onto it may be neglected as a consequence. The circuit may then be represented by that shown in Figure 3.3(c). Further, it is assumed that at the start of Mode B the voltage on the clamp capacitor is always $(k-1)V_{DC}$, where k is a constant. This would be achieved in practice by using an auxiliary supply to keep the capacitor charged. During this mode:

$$i_L = I_{LA0}-\frac{1}{L_r}\int_{T_A}^{t+T_A} v_{clamp}.dt \tag{3.7}$$

where I_{LA0} is the current in L_r at the end of Mode A, T_A is the time at the end of Mode A, t is the elapsed time from the start of Mode A, v_{clamp} is the value of v_C during Mode B.

$$v_{clamp} = (k-1)V_{DC}+\frac{1}{C_{clamp}}\int_{T_A}^{t+T_A}(i_L-I_X).dt \tag{3.8}$$

Mode B ends when i_L reaches a value which will ensure that v_C will reach zero during the next period of resonance. At this point the clamp switch opens and the circuit may once more be represented by the topology shown in Figure 3.3(b). Suppose that at the end of Mode B (i.e. at the start of Mode C) the current in L_r is I_{LC0}, and the voltage on C_r is given by V_{CC0}. Similarly to the derivation of equation (3.5);

$$v_c = V_{DC}+(V_{CC0}-V_{DC})\cos(\omega_0 t)+\frac{1}{\omega_0 C_r}\left(I_{LC0}-I_X\right)\sin(\omega_0 t) \tag{3.9}$$

This may be written in the form;

$$v_c = V_{DC}+A.\cos(\omega_0 t-\Phi) \tag{3.10}$$

where;

$$A = \sqrt{\left(V_{CC0} - V_{DC}\right)^2 + \frac{1}{\omega_0^2 C_r^2}\left(I_{LC0} - I_X\right)^2} \qquad (3.11),$$

and

$$\Phi = \tan^{-1}\left(\frac{\frac{1}{\omega_0 C_r}\left(I_{LC0} - I_X\right)}{V_{CC0} - V_{DC}}\right) \qquad (3.12)$$

Because $\omega_0^2 = \frac{1}{L_r C_r}$ and $V_{CC0} = kV_{DC}$, then (3.11) may be written as;

$$A = \sqrt{V_{DC}^2\left(k-1\right)^2 + \frac{L_r}{C_r}\left(I_{LC0} - I_X\right)^2} \qquad (3.13)$$

By inspection of equation (3.10), the condition for v_C to just reach zero is that $A=V_{DC}$. Thus, equating (3.11) to V_{DC} and rearranging gives;

$$\boxed{I_{LC0} = I_X - \frac{V_{DC}}{Z_0}\sqrt{k(2-k)}} \qquad (3.14)$$

where $Z_0 = \sqrt{\frac{L_r}{C_r}}$. Equation (3.14) gives the condition for the clamp switch to be opened such that the voltage on C_r will resonate down to zero. In practice some note may need to be taken of the resistance of the resonant circuit, to account for losses.

MODE C

Mode C commences when the clamp switch has been opened. The circuit topology during this mode is shown in Figure 3.3(b). The voltage on C_r is given by (3.9), and similarly;

$$i_L = I_X + \left(I_{LC0} - I_X\right)\cos\left(\omega_0 t\right) + \frac{1}{\omega_0 L_r}\left(V_{DC} - V_{CC0}\right)\sin\left(\omega_0 t\right) \qquad (3.15)$$

MODE D

When the voltage on C_r reaches zero, the conditions exist for lossless switching. The output stage is switched to a new configuration in accordance with the modulation strategy. This imposes an abrupt change on I_X, and it is this change which determines the form of Mode D. If I_X changes such that I_L is greater than I_X then C_r begins to charge immediately. This constitutes the start of the next cycle and Mode D ends. Alternatively I_X may change such that it is greater at that instant than the value of I_L. In this case C_r cannot charge until I_L has been increased by the voltage on the clamping capacitor, and is equal to I_X. If this occurs then the voltage on C_r remains practically zero whilst I_L is increasing. This constitutes Mode D, which ends when v_C begins to rise. At this point Mode A commences, whereupon the resonant cycle repeats as above.

For the purposes of this simulation the load on the converter was assumed to be a 3-wire star-connected induction machine. This could easily be modified to, say, a delta connected machine or simple RC load with some minor changes to the program. The underlying principles for the simulation would remain the same. The transformer equivalent circuit of the induction motor was used as shown in Figure 3.5.

The fundamental slip, (s) is given by; $$s = \frac{N_s - N_r}{N_s} \tag{3.16}$$

where N_S is the speed of the stator field, and N_r is the speed of the rotor. The harmonics of the fundamental fall into the categories of positive and negative sequence components. For the *n*th positive sequence harmonic (n=7,13,19.....) the slip s_n is given by:

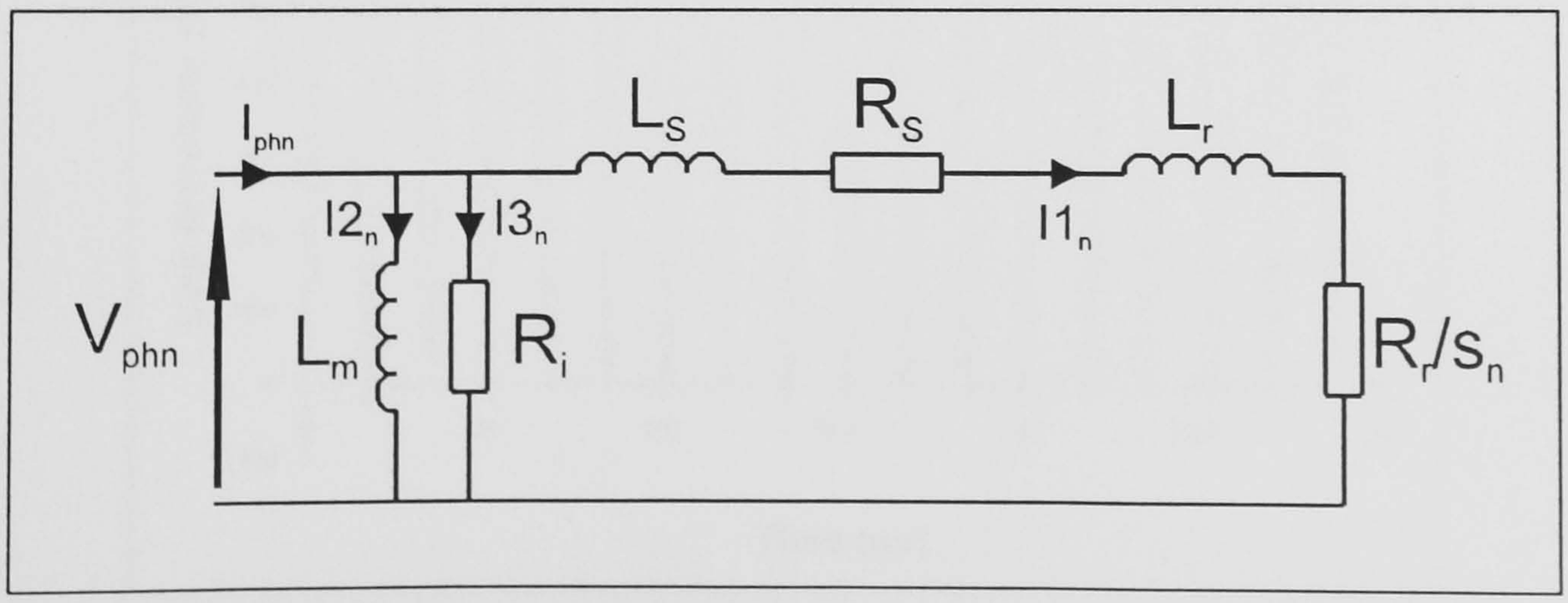

Figure 3.5 Equivalent circuit for one phase of a 3-phase induction machine

$$s_n = \frac{nN_s - N_r}{nN_s} \tag{3.17}$$

Rearranging, and substituting from (3.16) gives [34]:

$$\boxed{s_n = \frac{n-1+s}{n}} \tag{3.18}$$

Similarly for the negative sequence (n=5,11,17):

$$\boxed{s_n = \frac{n+1-s}{n}} \tag{3.19}$$

3.1.4 Calculation of Phase Current

The simulation program must be provided with data describing the modulation pattern of the output stage of the converter. The modulation pattern also determines the amplitude of the fundamental component of the generated waveform. Using this nominal fundamental value, it is possible to calculate an approximate value for the fundamental component of the phase current. This allows an approximate value of link current to be calculated for any instant in time. This is important since it constitutes the value 'I_X' in the equations (3.5) to (3.15) in section 3.1.3. These equations are used to simulate the resonant capacitor voltage (v_c). Figure 3.6 shows a fragment

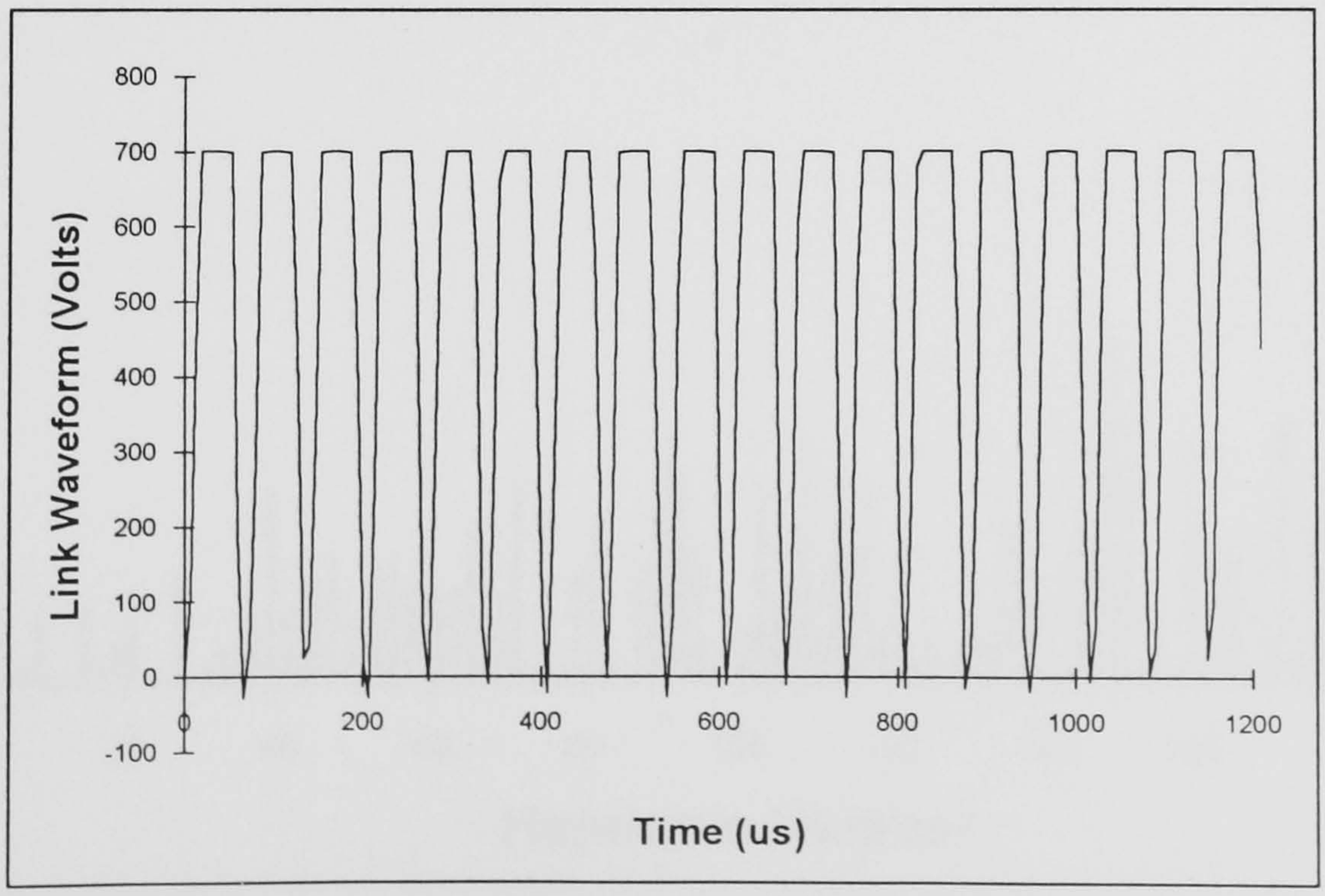

Figure 3.6 Simulated Link Voltage Waveform

of the link voltage waveform obtained from such a simulation.

The phase voltage waveform is constructed by selecting pulses from the link voltage waveform in

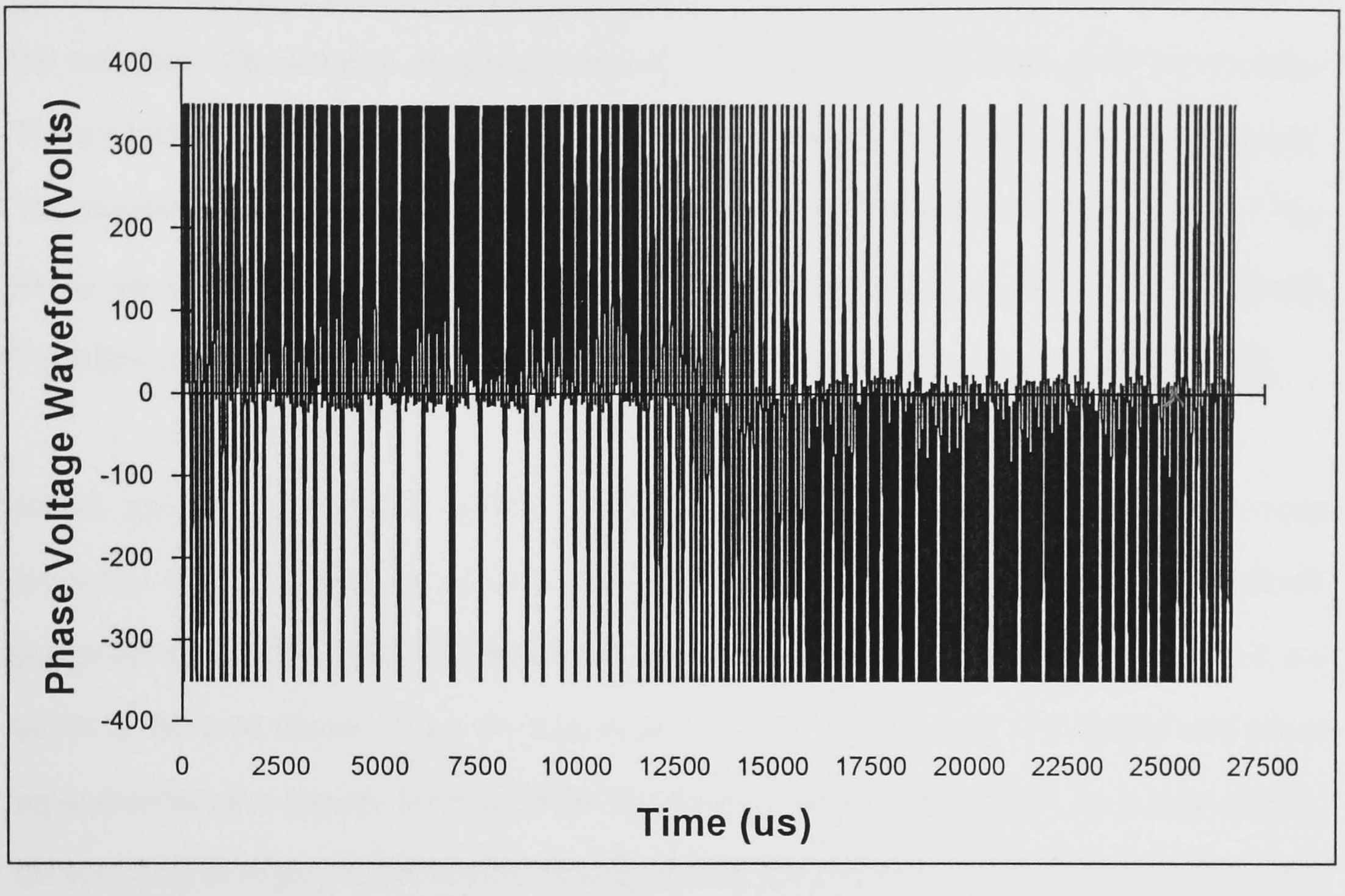

Figure 3.7(a) Phase Voltage Waveform

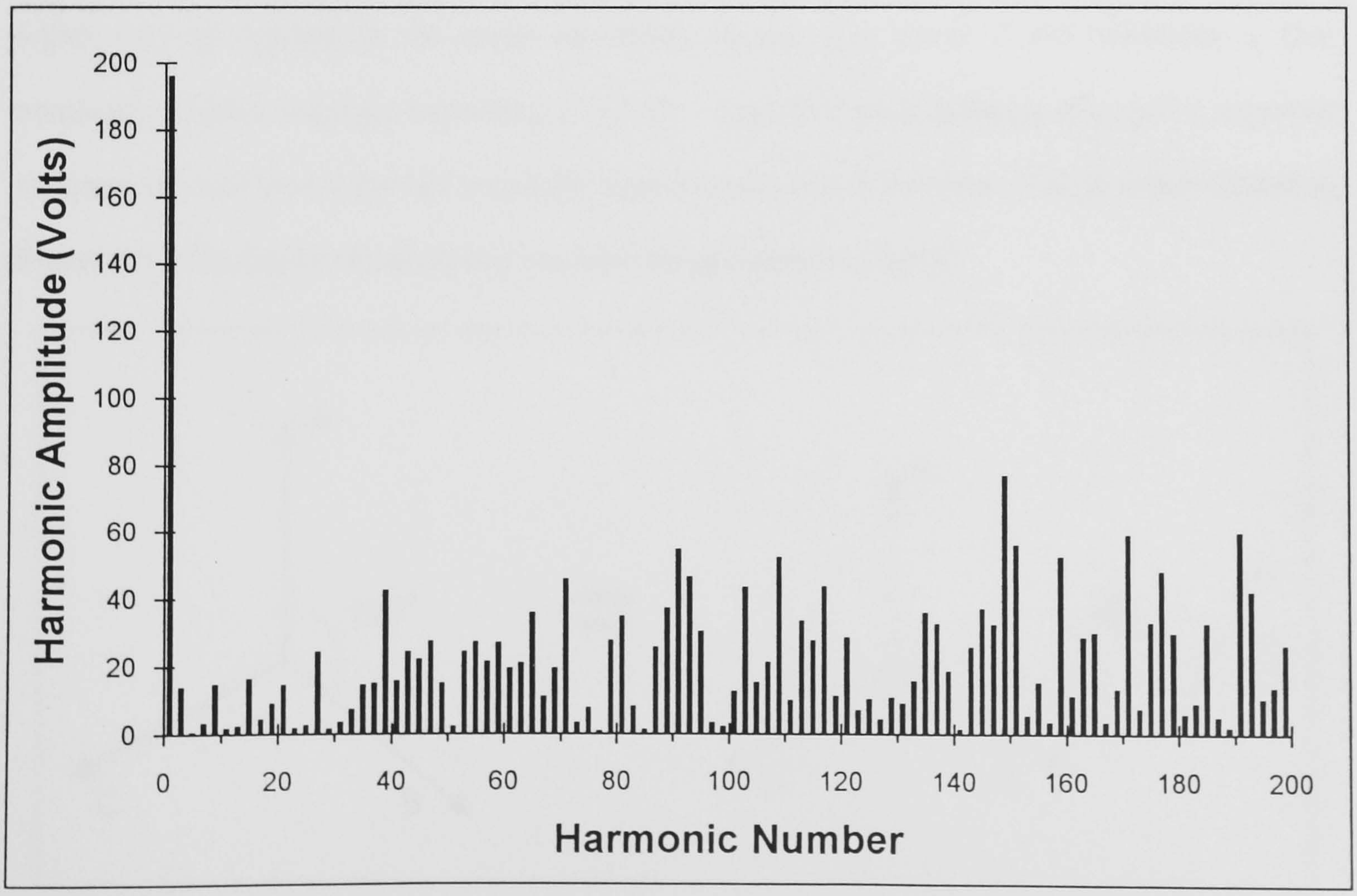

Figure 3.7(b) Harmonic Spectrum of Phase Voltage Waveform

such a way that they appear at the pole as either positive or negative pulses with half the amplitude of the link waveform. The modulation pattern controls the position and number of each polarity of pulse, thus effecting control over the fundamental amplitude and harmonic content of the waveform. The selection of pulses is done by modulation of the switches of the output stage. These switches cannot change state instantaneously and distortion is introduced as a consequence. The simulation approximates this distortion as explained in more detail below. Figure 3.7(a) shows an example of a phase voltage waveform obtained by simulation. A Fast Fourier Transform is performed on this, [39] to yield its harmonic spectrum as shown in Figure 3.7(b).

In this type of converter it is usual to employ an output waveshape which has quarter-wave symmetry, thus the number of pulses in each cycle is a multiple of 4. Additionally, because the pulses are selected from the link waveform, the pulses in one phase are in alignment with the pulses in the other phases. These two factors prevent there being exactly 120 degrees time phase separation between phases. In other words the system is slightly unbalanced. As a consequence, the spectrum in Figure 3.7(b) cannot be used directly to calculate the phase current, instead it must be decomposed into sequence components resulting in a balanced representation of voltages which may be applied to the motor equivalent circuit. The result of the imbalance is that nominally positive sequence harmonics (7,13,19.....) contain small amounts of negative sequence components, and vice versa for nominally negative sequence harmonics. This is demonstrated in Figure 3.8 (The degree of imbalance has been exaggerated for clarity).

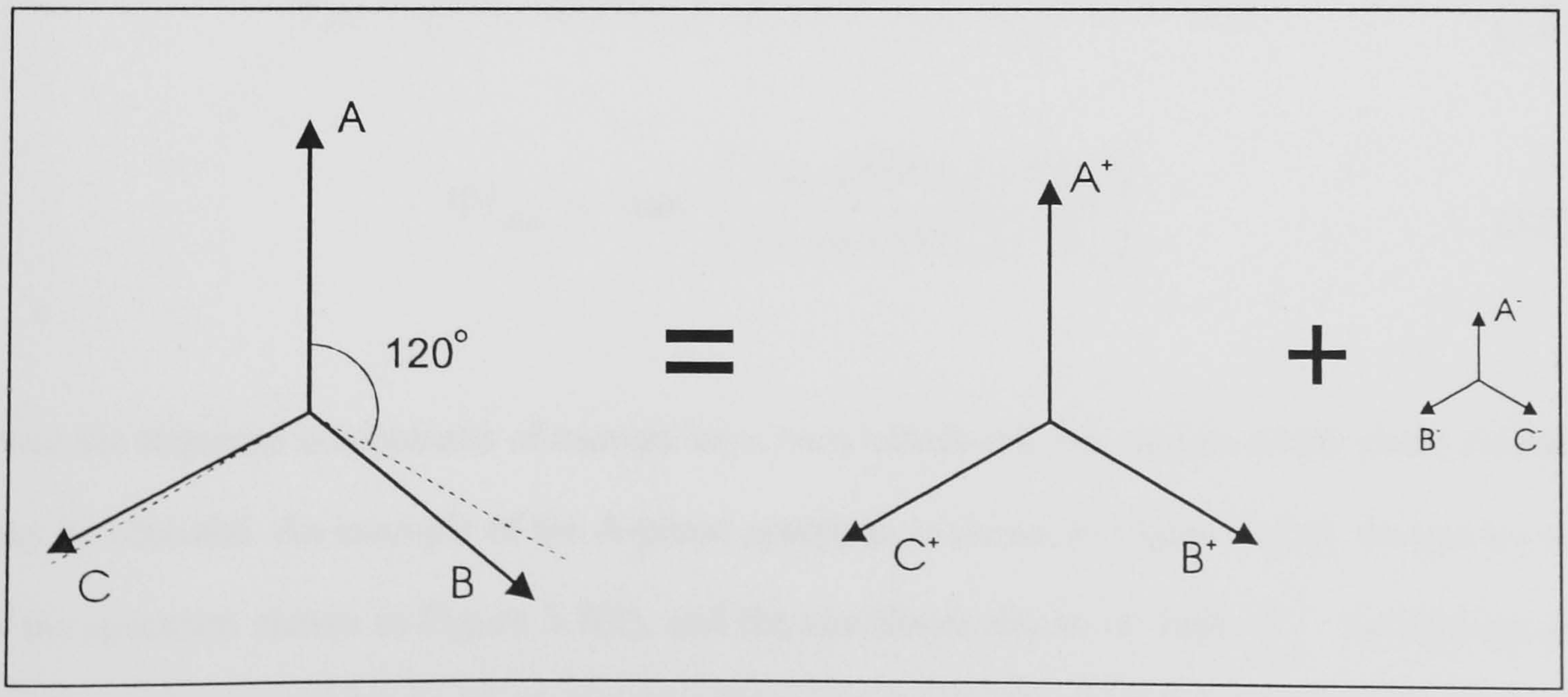

Figure 3.8 Decomposition into positive and negative sequence harmonics

C_r:	0.56μF	L_r:	104μH
k:	1.4	V_{DC}:	500V
Slip:	0.1	R_S:	1Ω
L_S:	10mH	L_r:	5mH
R_r:	1Ω	L_M:	1.6H
R_I:	5kΩ		

Table 3.1 Conditions Used for Simulation

The sequence components of current may then be calculated using the equations given below, (ignoring skin effects) where v_{phn} is the amplitude of the *n*th harmonic voltage, having a slip s_n.

$$I1_n = \frac{V_{phn}}{\sqrt{\left(\left(R_s + \frac{R_r}{s_n}\right)^2 + n^2\omega^2\left(L_s + L_r\right)^2\right)}} \tag{3.20}$$

Phase angle of $I1_n$,

$$\Phi I1_n = -\tan^{-1}\left[\frac{n\omega\left(L_s + L_r\right)}{R_s + \left(\frac{R_r}{s_n}\right)}\right] \tag{3.21}$$

$$\left|I2_n\right| = \frac{V_{phn}}{n\omega L_m} \tag{3.22}$$

$$\left|I3_n\right| = \frac{V_{phn}}{R_i} \tag{3.23}$$

$$I_{phn} = \sqrt{\left(I1_n.\cos\left(\Phi1_n\right) + I3_n\right)^2 + \left(I1_n.\sin\left(\Phi1_n\right) + I2_n\right)^2} \tag{3.24}$$

$$\Phi I_{phn} = -\tan^{-1}\left(\frac{I1_n\sin\left(\Phi1_n\right) + I2_n}{I1_n\cos\left(\Phi I1_n\right) + I3_n}\right) \tag{3.25}$$

Once the sequence components of current have been calculated, the spectra of the phase currents may be obtained. An example of the A-phase spectrum is shown in Figure 3.9(a), derived by use of the spectrum shown in Figure 3.7(b), and the conditions shown in Table 3.1. To improve the scaling of the spectrum, the fundamental component has been removed; its value is 17.2A. By

implementing an Inverse Fourier Transform (IFT) the time domain form of the phase current may be obtained as shown in Figure 3.9(b).

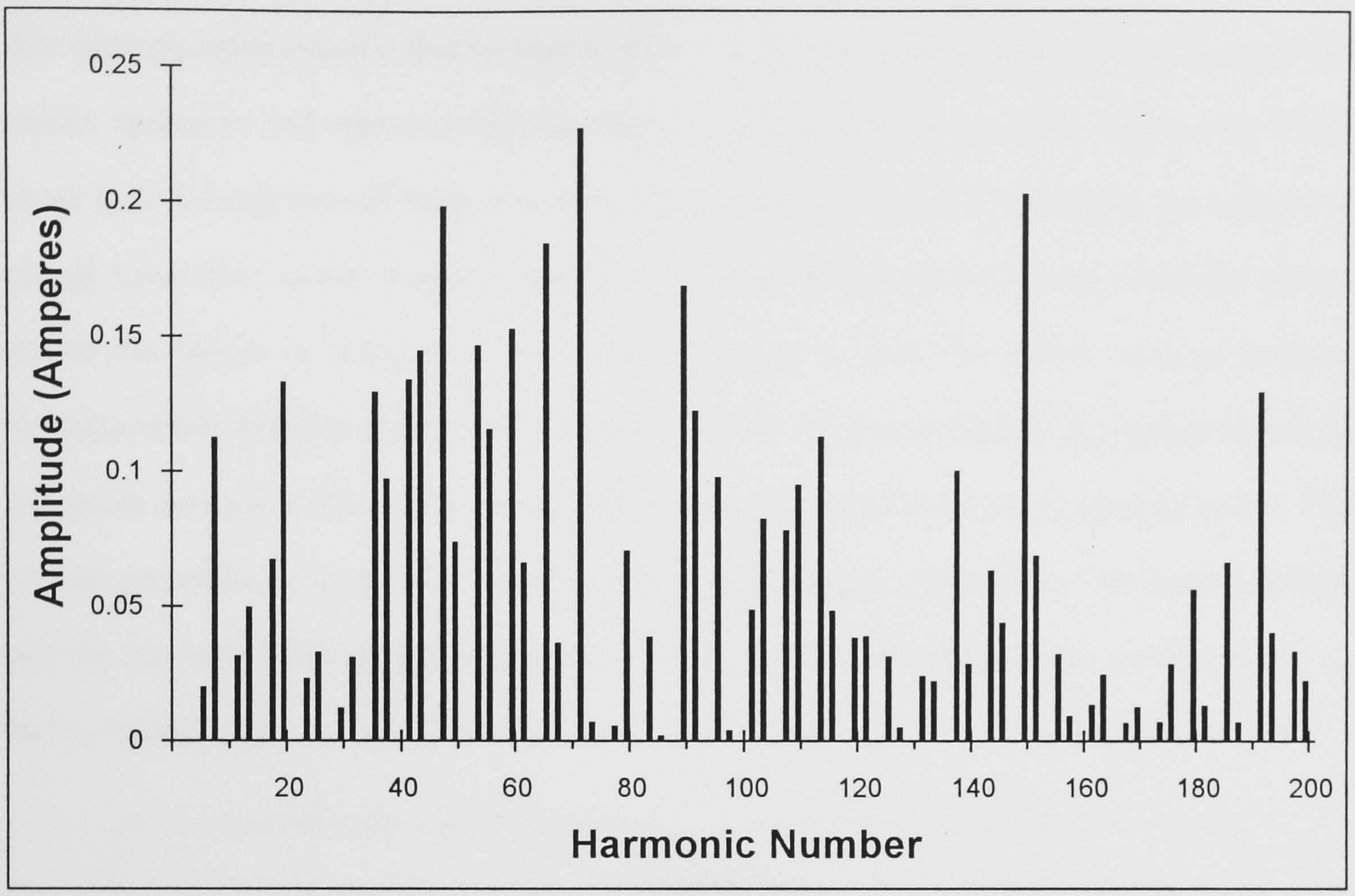

Figure 3.9(a) Spectrum of Phase Current (Fundamental component removed)

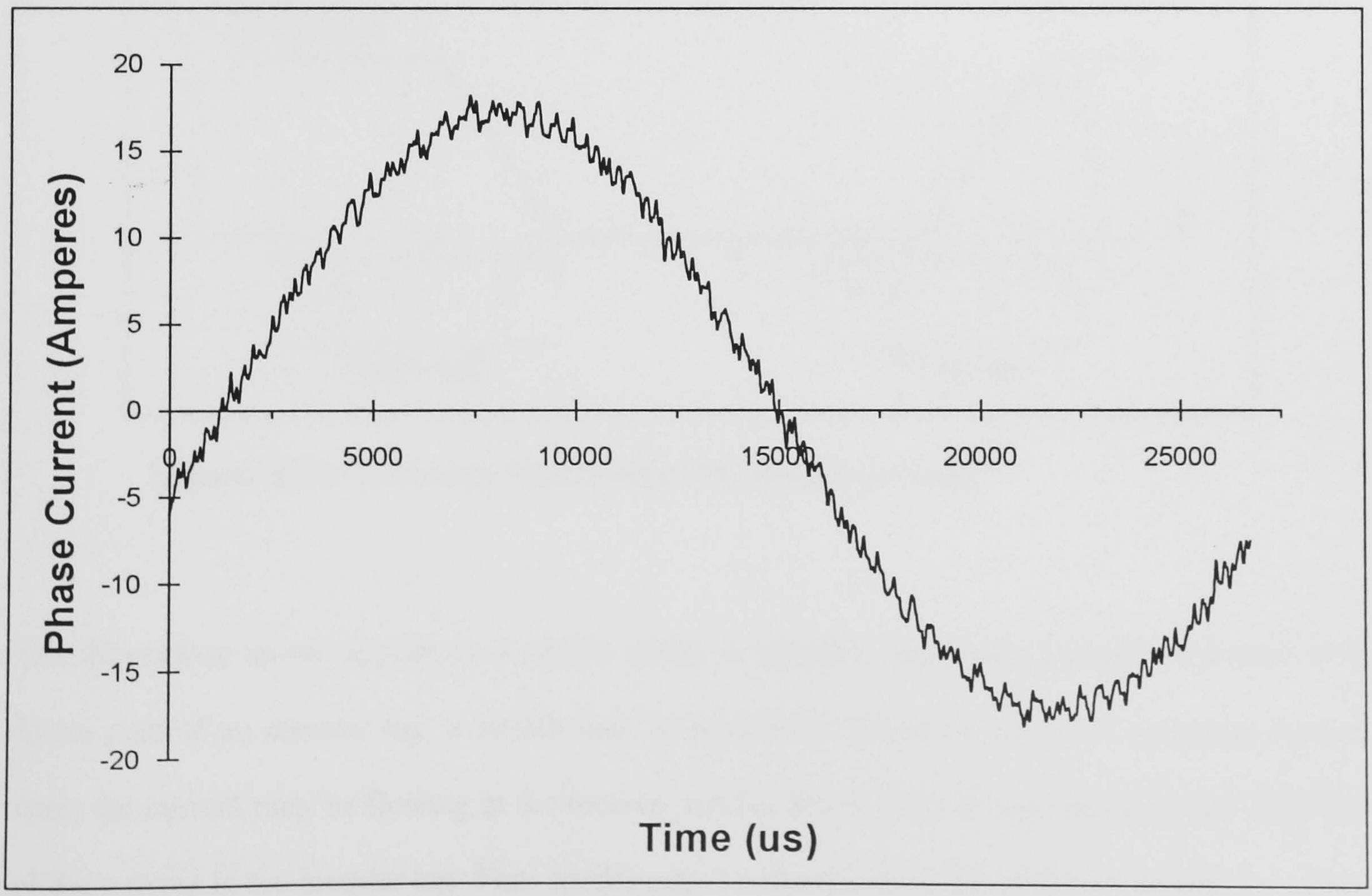

Figure 3.9(b) A-Phase Current

3.1.5 Effect of Switching Times of Devices

The switching behaviour of the power devices is represented by the linear approximation shown in Figure 3.10 [40]. This is a generic model which may be applied to many types of power device. The approximation assumes that the load is fairly inductive. Six parameters are used to model the switch operation, and represent features which are found in most switches, independent of the exact type. During turn-off there is a turn-off delay ($t_{d(off)}$) caused, for example, by a period of charge removal or carrier recombination. This is followed by a period during which the voltage across the device is rising (t_{rv}); the current flowing through the switch remains constant throughout this time due to the load inductance. Finally there is an interval (t_{fi}) during which the current in the switch falls due to its diversion into an anti-parallel diodes or another switch. The turn-on procedure is similar, with a delay time ($t_{d(on)}$) between application of the control voltage and the commencement of conduction. The voltage fall and current rise times are denoted by t_{fv} and t_{ri} respectively.

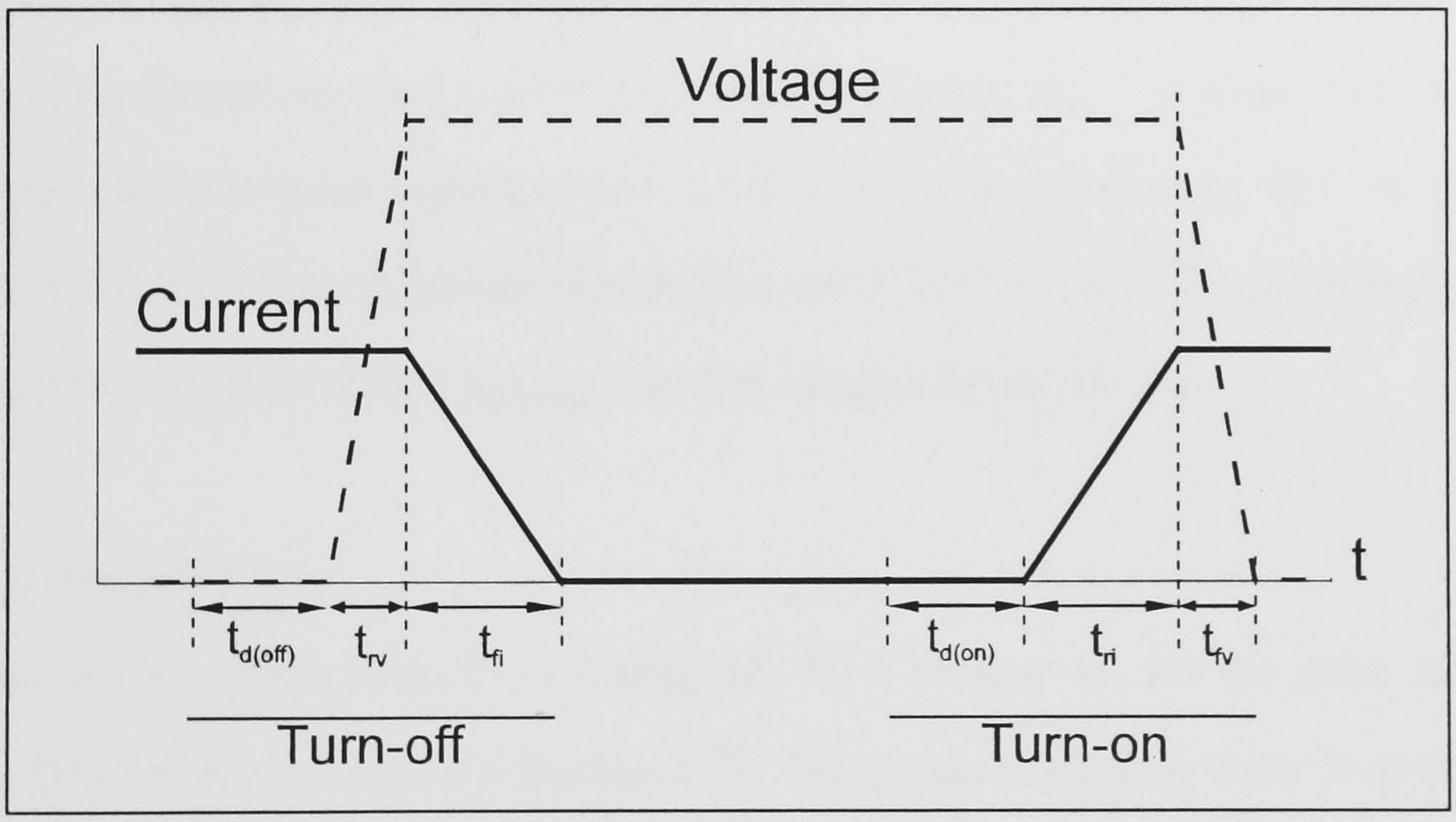

Figure 3.10 Switching Parameters for Inductive Load

The description above applies to a switch which is actually conducting current. However, if it forms part of an inverter leg, a switch may be nominally turned on but not conducting current since the current may be flowing in the inverse parallel diode. This is determined by the direction of the current in the inverter leg. Four modes may be identified for the switching behaviour of the

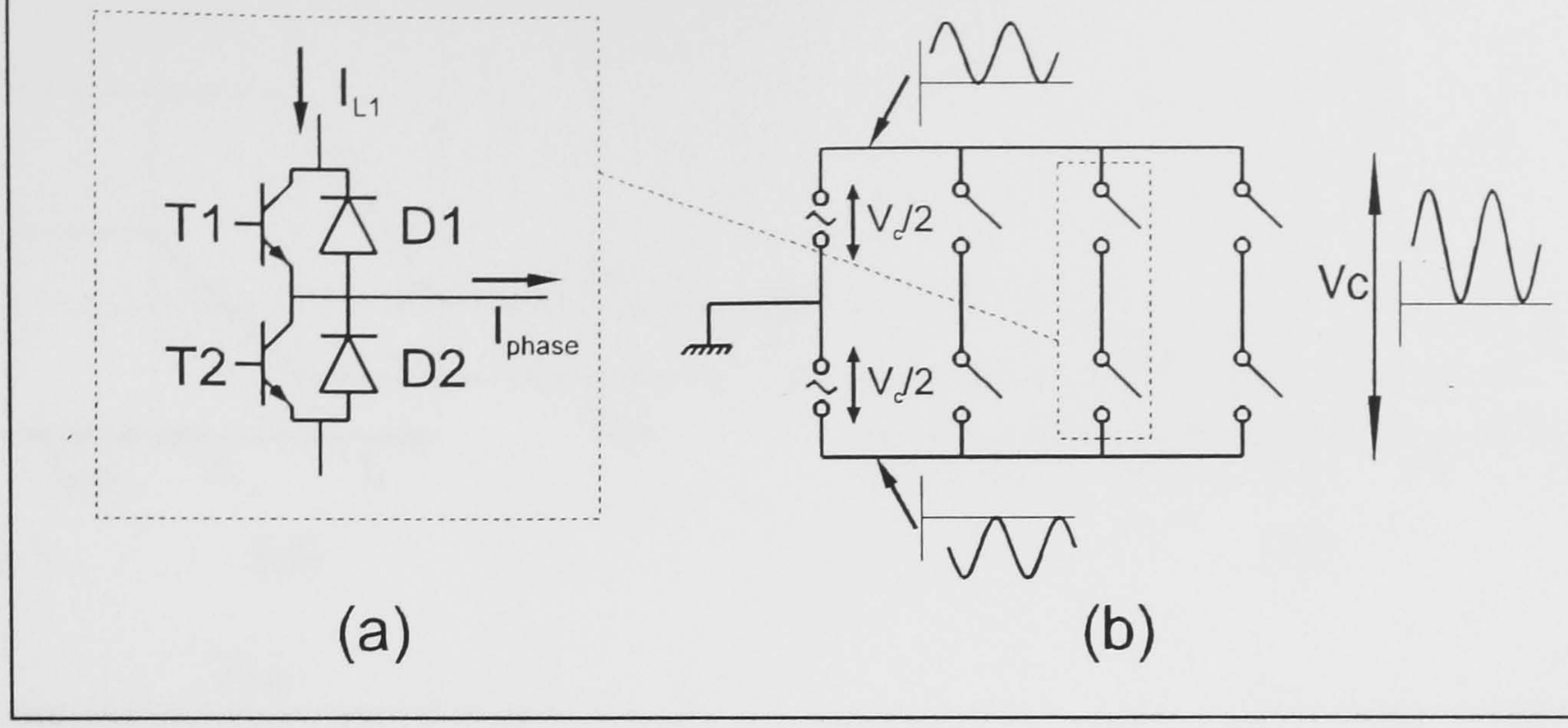

Figure 3.11 Switch Pole Currents and Schematic Representation of RDCLI

inverter pole shown in Figure 3.11(a) relating to the current direction and the order in which the switches are commutating. To aid description of the modes a schematic representation of the inverter may be used as shown in Figure 3.11(b). Here the resonant link is shown as consisting of two voltage sources with a centre-point ground, each having half the amplitude of the resonant link. This allows a symmetrical treatment of the selection of the link pulses by the top and bottom switches of the inverter leg. Each mode will now be considered in turn. The graphs in Figure 3.12 demonstrate the linear approximation of current fall or rise as the switch turns off or on, and also shows how the pole voltage is selected from the link waveform throughout the switching period. It is assumed that the phase current (I_{phase}) remains constant during this time.

MODE 1 (Figure 3.12(a))

This describes the period when T1 is turning off, T2 is turning on, and the phase current is positive. Thus initially the current is flowing in T1. The current commutates from T1 to D2 as T1 turns off. T2 then turns on, but this has no effect on the circuit since the current is flowing in its inverse-parallel diode.

$$\mathbf{0 < t <= t_{d(off)}}: \quad v_{pole} = \frac{v_c}{2}, \quad i_{L1=} I_{phase}$$

where v_c is the instantaneous resonant capacitor voltage, and i_{L1} is the current flowing from the link into the inverter leg.

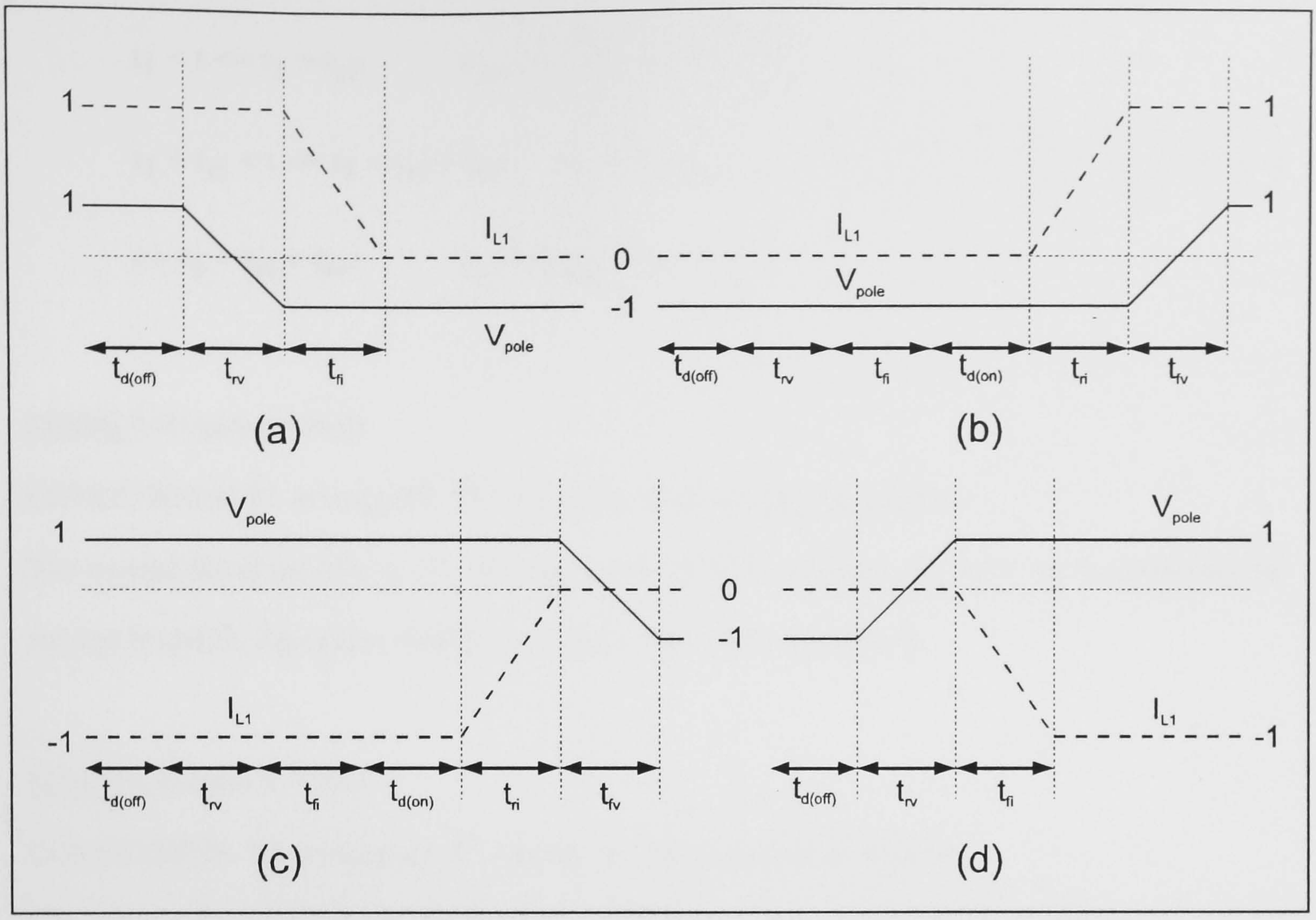

Figure 3.12 Linear Approximation of Inverter Switching Characteristics

$$\mathbf{t_{d(off)} < t < t_{d(off)} + t_{rv}}: \qquad v_{pole} = \left(t - t_{d(off)}\right) \times \left(\frac{-v_c}{2} - \frac{V_{c0}}{2}\right) + \frac{V_{c0}}{2}, \; i_{L1} = I_{phase}$$

Where V_{C0} is the resonant capacitor voltage at the end of $t_{d(off)}$.

$$\mathbf{t_{d(off)} + t_{rv} < t < t_{d(off)} + t_{rv} + t_{fi}}: \qquad v_{pole} = -\frac{v_c}{2}, \; i_{L1} = \frac{\left(t - t_{d(off)} - t_{rv}\right)}{t_{fi}} \times \left(-I_{phase}\right) + I_{phase}$$

$$\mathbf{t > t_{d(off)} + t_{rv} + t_{fi}}: \quad I_{L1} = 0, \; v_{pole} = -\frac{v_c}{2}.$$

MODE 2 (Figure 3.12(b))

This mode is defined by T2 turning off, T1 turning on, and the phase current being positive.

Thus the current is initially in D2. As a consequence when T2 turns off it has no effect on the circuit. T1 then turns on and the current commutates to it from D2. In the description below let $t_1 = t_{d(off)} + t_{rv} + t_{fi} + t_{d(on)}$.

$$\mathbf{0 < t <= t_1}: \qquad i_{L1} = 0, \; v_{pole} = -\frac{v_c}{2}$$

$$\mathbf{t_1 < t <= t_1 + t_{ri}}: \qquad v_{pole} = -\frac{v_c}{2},\ i_{L1} = \frac{(t - t_1)}{t_{ri}} \times I_{phase}$$

$$\mathbf{t_1 + t_{ri} < t <= t_1 + t_{ri} + t_{fv}}: \qquad i_{L1} = I_{phase},\ v_{pole} = \frac{(t - t_1 - t_{ri})}{t_{fv}} \times \left(\frac{v_c}{2} - \frac{V_{c0}}{2}\right) + \left(\frac{V_{c0}}{2}\right)$$

$$\mathbf{t > t_1 + t_{ri} + t_{fv}}: \qquad i_{L1} = I_{phase},\ v_{pole} = \frac{v_c}{2}.$$

MODE 3 (Figure 3.12(c))

CONDITIONS: T1 turning off, T2 turning on. Phase current is negative.

The current flows initially in D1. T1 thus turns off without effect. T2 turns on commutating the current from D1. Equations similar to modes 1 and 2 may be derived.

MODE 4 (Figure 3.12(d))

CONDITIONS: T2 turning off, T1 turning on, phase current is negative.

The current flows initially in T2. T2 turns off which causes the current to commutate to D1. T1 then turns on without effect.

Figure 3.13 shows the effect of varying the switching speed parameters. The 'fast' switches have

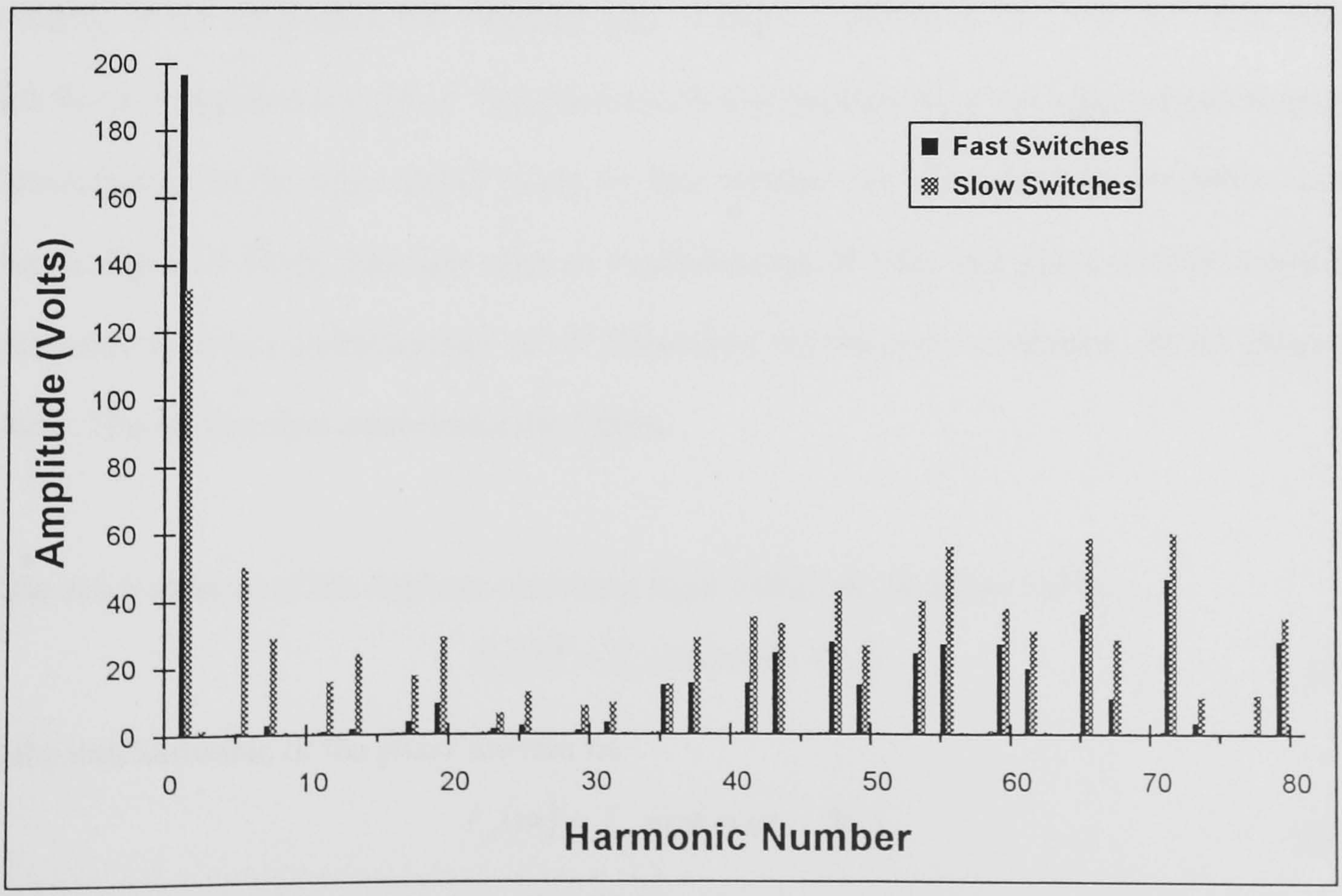

Figure 3.13 Effect of Switching Time on Phase Voltage Spectra

delay times set at 1.5μs and rise and fall times of 1μs. The modulation pattern is one which minimises a given set of harmonics (this is explained in detail in the next chapter). The triplen harmonics have been suppressed for clarity since they have no effect on current flow where the load is a balanced three phase system with no neutral. The first 9 non-triplen harmonics have been minimised. The graph generated using 'slow' devices employed switch times 10 times longer than the first case. Such switches would not be suitable in practice, but it is a useful exaggeration to ease comparison. It can be seen that increasing the switching time, which distorts the phase voltage waveform, has changed the value of the fundamental and increased the magnitude of the otherwise minimised harmonics.

3.1.6 Calculation of Link Current

The *switching logic* function describes the polarity of each pole of the inverter at any point in time. When the logic function for a particular pole is '1', the top switch is on. During this time the phase current in that pole flows from the resonant link via the switch, or returns to the link via the diode depending on its direction. [41] When the logic function is '0' the bottom switch is on. No current flows from the link. An example of this is given in Figure 3.14. Graph (a) shows the logic switching waveform for a modulation pattern with only 20 pulses per quarter cycle (to improve the clarity of the diagrams), the resulting pole voltage is shown in (b), and the phase current which flows is depicted in 3.14(c). The phase current is multiplied by the logic waveform to yield the contribution to the link current made by that inverter leg. The resulting waveform is that shown in Figure 3.14(d). The time domain multiplication of logic and phase current waveforms corresponds to *cross*-multiplication of all harmonics of the two waveforms, in the frequency domain. This is described mathematically below:

Let the *n*th harmonic of the A-phase switching logic waveform be described by:

$$S_A(n) = S_n \cos(n\omega t - \Phi_n) \tag{3.26}$$

and the *m*th harmonic of the phase current be:

$$I_A(m) = I_m \cos(m\omega t - \Psi_m) \tag{3.27}$$

then the spectrum of the contribution to the link current is given by:

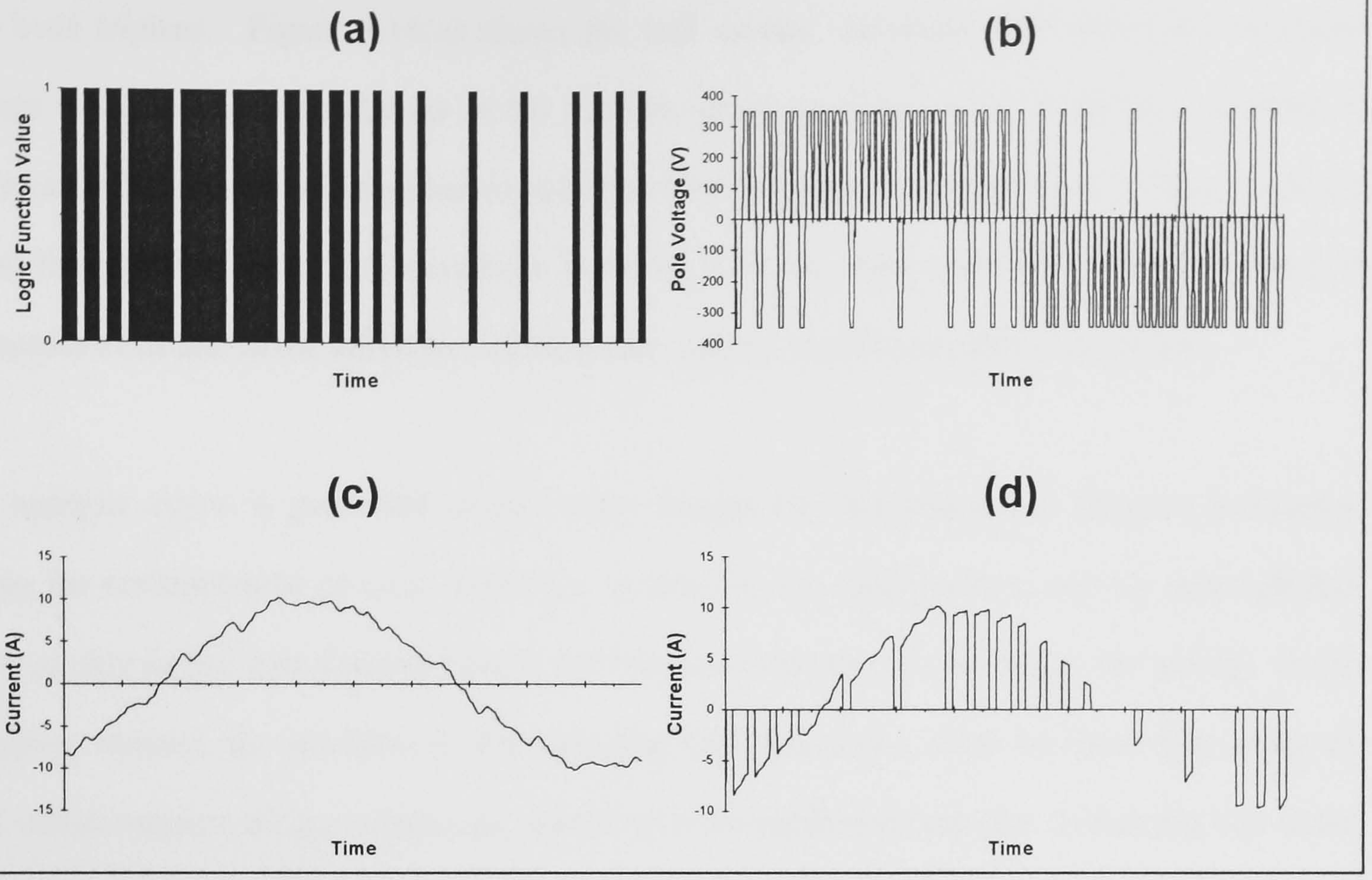

Figure 3.14 Switching Logic, Pole Voltage and Phase and Link Current Waveforms

$$S_A(n)I_A(m) = \frac{S_n I_m}{2}\left[\cos\left((m+n)\omega t - (\Phi_n + \Psi_m)\right) + \cos\left((m-n)\omega t - (\Psi_m - \Phi_n)\right)\right] \quad (3.28)$$

The total link current I_L is a summation of the contribution from each phase. In a 3-phase system this results in the following equation for the *k*th harmonic of link current:

$$I_L(k) = S_A(n)I_A(m) + S_B(n)I_B(m) + S_C(n)I_C(m) \quad (3.29)$$

From equation (3.28) it can be seen that the combination of harmonics of order 'm' and 'n' gives sidebands in the link current of order 'm+n' and 'm-n'. Due to the quarter wave symmetry of the logic waveform it contains only odd harmonics. Also, the phase current only contains odd harmonics for the same reason but further, it does not contain any triplen harmonics which cannot flow in a balanced 3-phase load with no neutral. Thus, when the cross-multiplication occurs it yields only even harmonics. This is shown pictorially in Figure 3.15. In addition to this, when the load is balanced the current harmonics in the link form a symmetrical 3-phase set [30]. Under these conditions the non-triplen harmonics cancel, which leaves

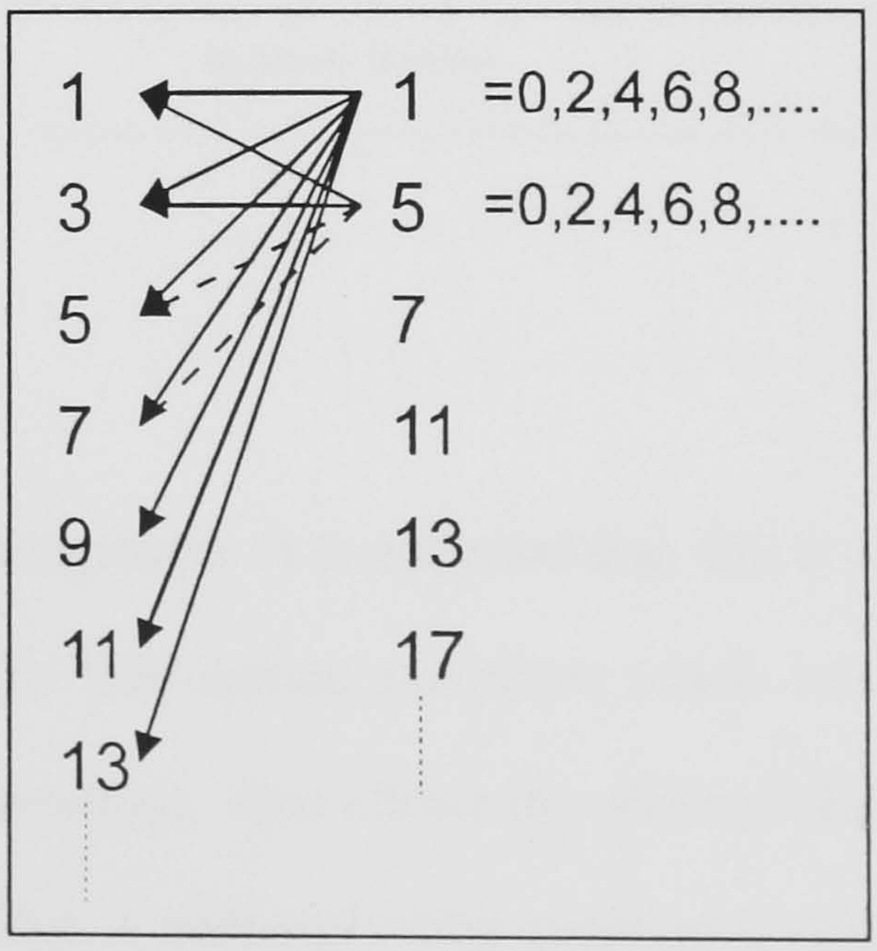

Figure 3.15 Harmonic Multiplication

only even triplens. Figure 3.16(a) shows the link current waveform over one cycle of phase voltage using the same conditions as the example given in Figure 3.14. A pattern repeating 6 times can be seen due to the dominance of the harmonics which are multiples of 6. Figure 3.16(b) shows the spectrum of the link waveform. It can be seen that small amounts of ideally eliminated harmonics exist due to the imbalance of the phase voltage waveforms alluded to earlier.

The analysis above is presented to give some insight into the interaction between harmonics during the multiplication process. However, in practice the multiplication can be accomplished more quickly in the time domain than in the frequency domain. To carry out the process in the frequency domain, the spectrum of the switching logic waveform must be found first using an FFT which requires $n log_2 n$ operations, where 'n' is the number of samples. Following this is the cross-multiplication of harmonics which requires n^2 operations, giving a total of $n log_2 n + n^2$. Although the time-domain multiplication requires an IFT to be performed on the phase current spectra, the multiplication only requires 'n' operations, giving a total of $n log_2 n + n$. Thus a significant saving in computation time can be made where 'n' is large.

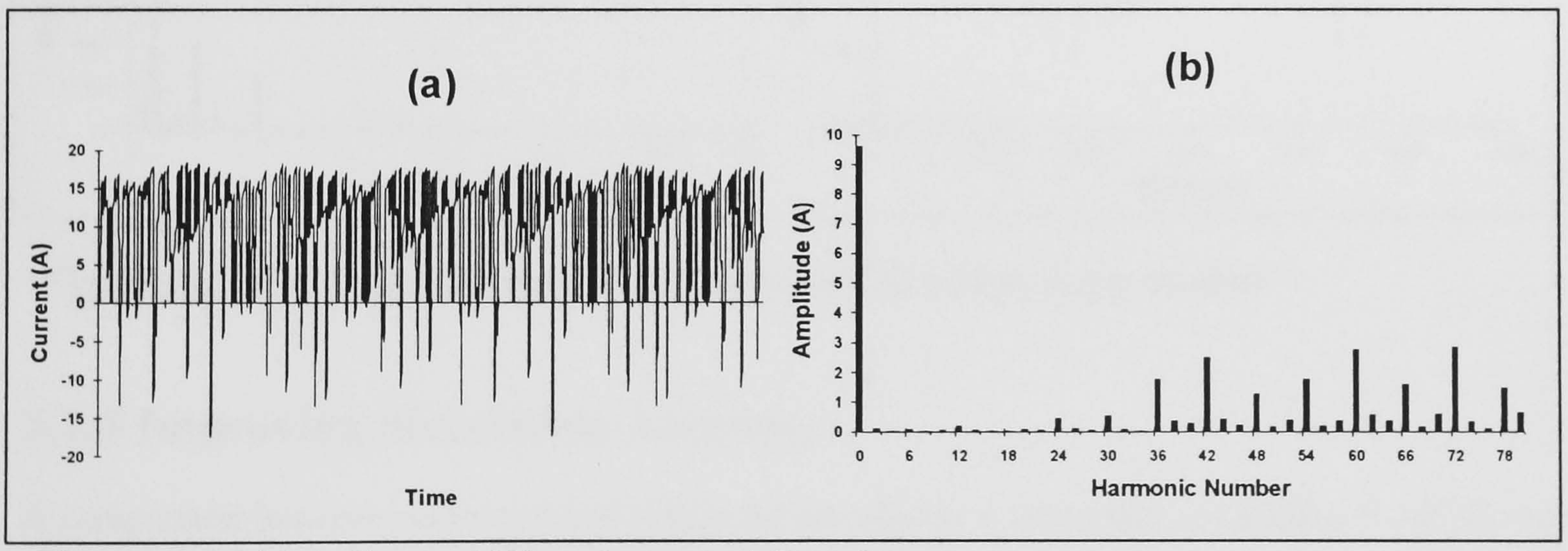

Figure 3.16 Link Current Waveform and Spectrum

3.1.7 Calculation of DC-Input Current

The link of the inverter is normally supplied via a filter arrangement. It is assumed that this is a simple L-C filter in this case. An FFT is performed on the link current waveform which was obtained by a time-domain method, to yield its harmonic spectrum. This allows the effect of the filter to be evaluated using a frequency-domain method. This is achieved using equation (3.30)

which describes the attenuation experienced by a harmonic of the link current (I_L) having order 'k'. The DC link input current is denoted by I_{in}, and ω_0 is the corner frequency of the filter.

$$I_{in}(k) = I_L(k) \times \frac{1}{\left|1 - \left(\frac{k\omega}{\omega_0}\right)^2\right|} \tag{3.30}$$

The BR specification for permitted electrical interference (BR1914) states that for operation on 750V DC systems, the resonant frequency of the filter should be less than 40Hz under worst-case conditions, to ensure that it is not excited by the industrial mains frequency. Figure 3.17(a) shows the spectrum obtained from the link current shown in Figure 3.16, after filtering, where the corner frequency of the filter is 40Hz. The fundamental has been removed from the spectrum to improve the scaling; its value is 2.95A. Figure 3.17(b) shows the time-domain version resulting from an Inverse Fourier Transform.

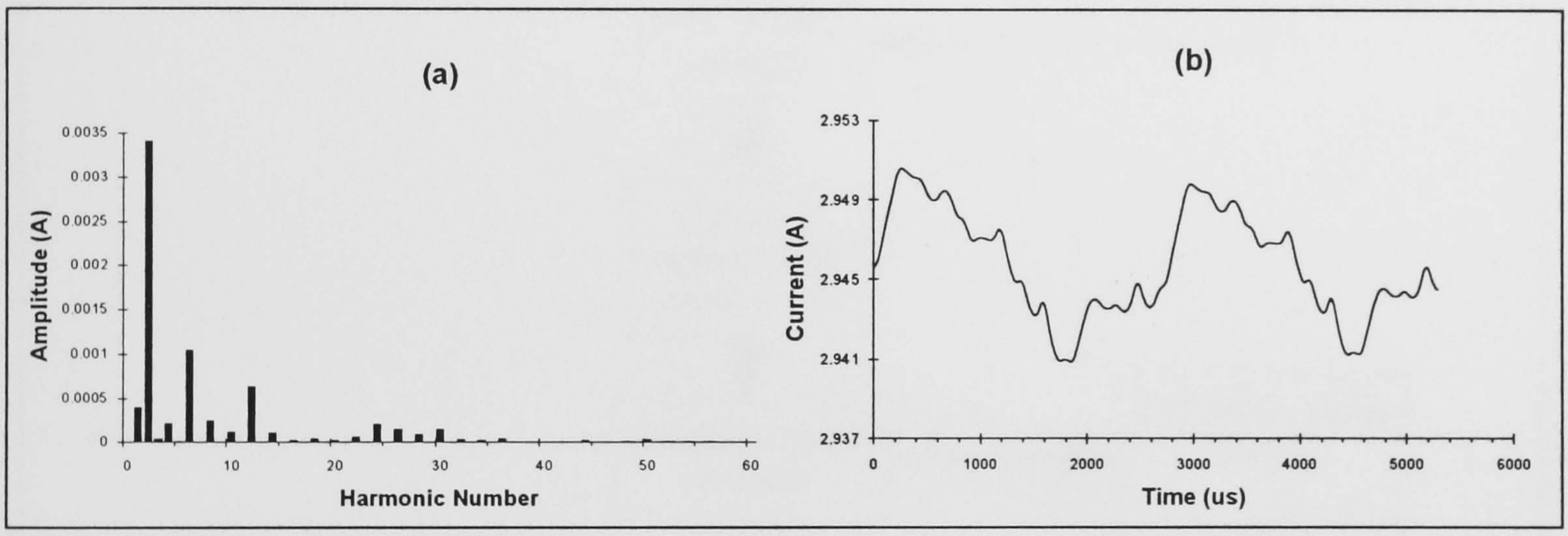

Figure 3.17 DC Input Current and Spectrum (DC Value Suppressed)

3.1.8 Improving Simulation Accuracy

A comparison between measured and simulated waveforms is presented in Chapter 5 and shows close agreement. However, the accuracy of the simulation could be improved by using an iterative process whereby the program is run several times. The reason for doing this is to account for the dependence of the link waveform on the instantaneous load current value. In the program described above, an approximate value of current is used. In an iterative scheme successive runs would use the value of phase current calculated from the previous iteration. By this method the simulation would converge towards a more accurate solution. The disadvantage of doing this is the significant increase in computation time which would occur.

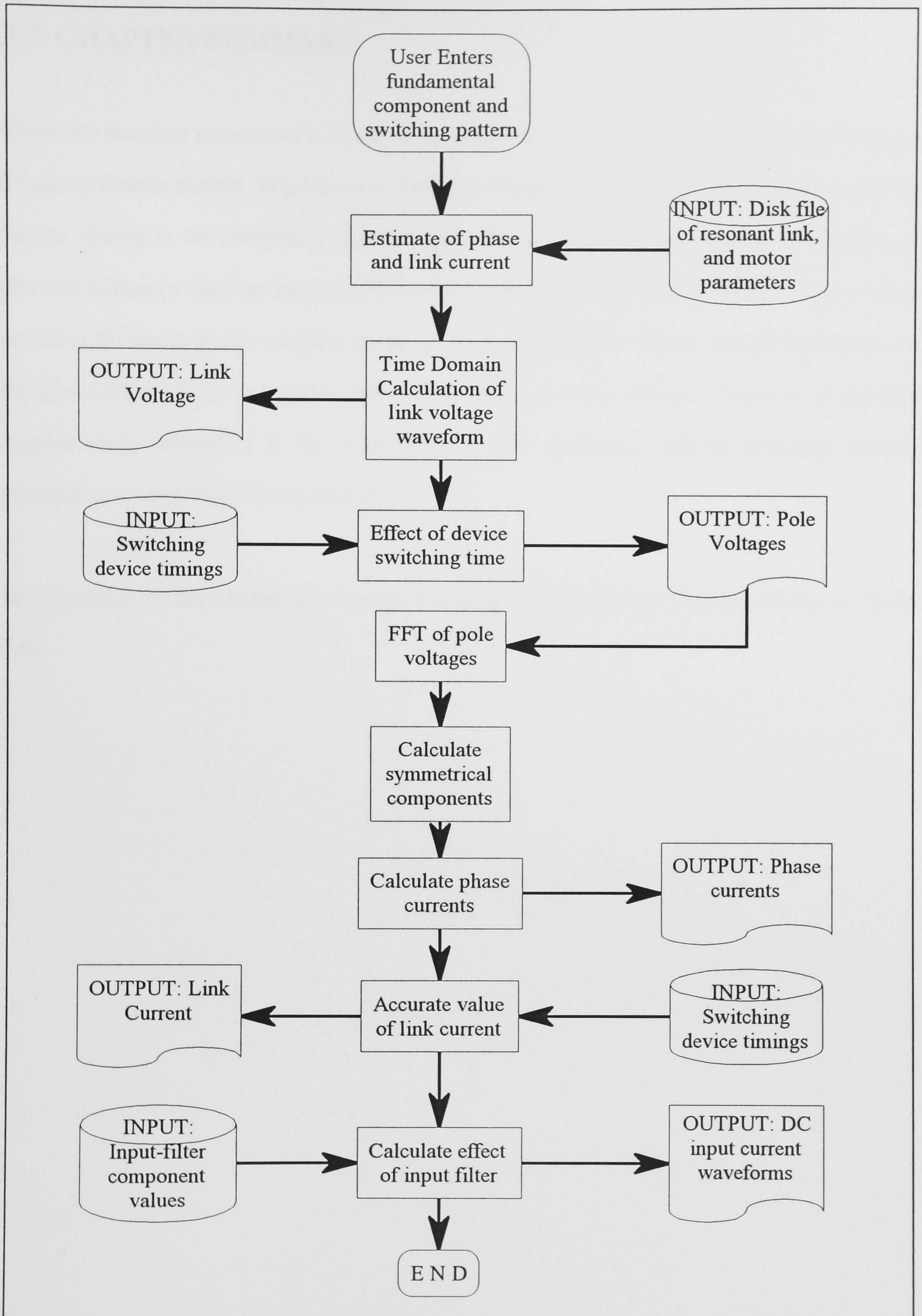

Figure 3.18 Flow Diagram of Simulation Program

3.2 CHAPTER SUMMARY

Where the transient response of a circuit is not required, a simulation may be performed using a frequency domain method. This allows a very large saving in computation time. However, several factors relating to the operation of the Resonant DC Link Inverter mean that a combination of time and frequency domain elements offer a better solution to the task of simulation. One of these factors is the harmonically complex nature of the link voltage waveform, and its dependence on the load current. Also, to examine the circuit operation at the resonant frequency of the link requires many harmonics to be incorporated in the simulation, making frequency domain multiplication of harmonics very time consuming.

The operation of the simulation program is summarised in the flow diagram shown in Figure 3.18.

Chapter 4

Modulation Strategies for Resonant Converters

4.1 Introduction

The modulation strategy of an inverter is an extremely important attribute. It influences many parameters of the generated waveforms such as the fundamental amplitude, Total Harmonic Distortion (THD), and psophometric current. It also affects variables within the inverter itself, such as switching loss. To ensure effective use of an inverter, the modulation strategy must simultaneously match the capabilities of the inverter stage, and the demands of the load. In the case of hard-switched converters it is commonplace to use Pulse Width Modulation (PWM) to achieve control of the output stage, and there is a rich variety of modulation methods available. This includes real-time 'carrier' techniques [42], and strategies optimised for implementation on microprocessors. [43,44,45] A great advantage of the hard-switched converter is that switching may take place at any instant in time (subject to a small minimum time between consecutive switching operations). This is not the case with the Resonant DC Link Inverter where the switching frequency is constrained to the zero voltage periods of the link waveform. The consequence of this is that conventional PWM techniques are not, in general, appropriate for this type of converter. Modified PWM strategies may be employed, and this is explained in more detail in section 4.2.2.

Although the switching instants of hard-switching converters are virtually unconstrained, there is a high penalty in terms of switching loss for each commutation which takes place. This imposes a severe restriction on the upper switching frequency, to confine device losses. The switching loss penalty in resonant converters is dramatically less, and as a consequence there is no upper limit on the switching frequency of the main devices, other than that imposed by the operating

frequency of the resonant link. This is an important consideration in selecting the modulation strategy since it offers clear benefits over hard-switching topologies.

In this Chapter modulation strategies currently used for Resonant DC Link Inverters are reviewed, and a new strategy introduced which is suitable for approximating harmonic elimination or other complex harmonic manipulations. Such strategies are of interest in the rail traction field, where signalling frequencies may need to be avoided.

4.2 A Review of Resonant Converter Modulation Strategies

4.2.1 Delta Modulators

This family of modulators has been known for some time in the communications field where they are applied to the conversion of analogue into digital signals. They operate under the control of a clock and as such may be synchronised with the oscillating link waveform of the Resonant DC Link Inverter. Not all varieties of delta modulator are suitable though, for example the Linear Delta Modulator which despite its name, has an undesirable non-linear frequency response [46]. A highly suitable member of the family is the Sigma Delta Modulator ($\Sigma\Delta$M), and is the technique most commonly used for modulation of resonant converters.[47]

The $\Sigma\Delta$M is shown schematically in Figure 4.1(a). v_o represents the output of the inverter, which is quantised, i.e. it only takes the values +1 and -1. This output is updated at the zero crossing points which are signalled by the link frequency strobe, f_c. Although the output pulses of the $\Sigma\Delta$M are square, they may be considered as representing a real pulse having an equal area. The difference between the output signal and a reference signal is fed to an integrator to produce an error signal, v_i. This error signal feeds the output quantiser. Thus a volt-second balance is maintained between the output pulses and the reference signal. Figure 4.1(b) shows a typical reference signal (which in this case is a sinusoid), and also its corresponding output signal, v_o.

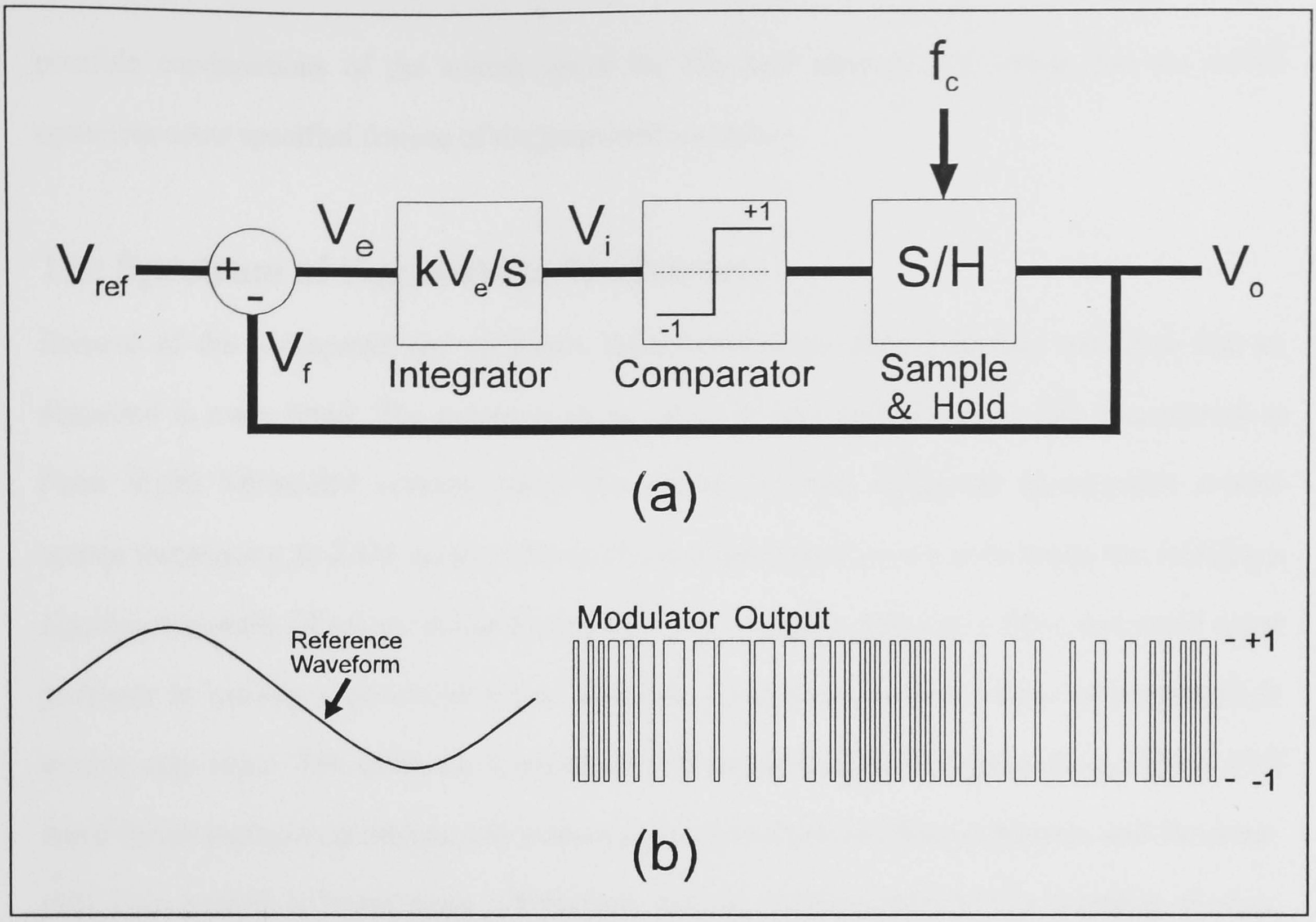

Figure 4.1 Sigma Delta Modulator and Associated Waveforms

Other variants of the Delta Modulator have been described, for example the Current Regulated Delta Modulator (CRΔM). [46] In this scheme, integration processes which are inherently present in the system are used as part of the modulator loop. For example, the circuit inductance acts as an integrator of applied voltage. In this case values of current, rather than voltage are used in the delta modulator, as shown in Figure 4.2. A drawback of the CRΔM is that it only utilises +1 and -1 values as its output. In practice the '0' state is also possible, and corresponds to free-wheeling. This problem is addressed by the Cost Function Regulator (CFR) [48], which analyses all

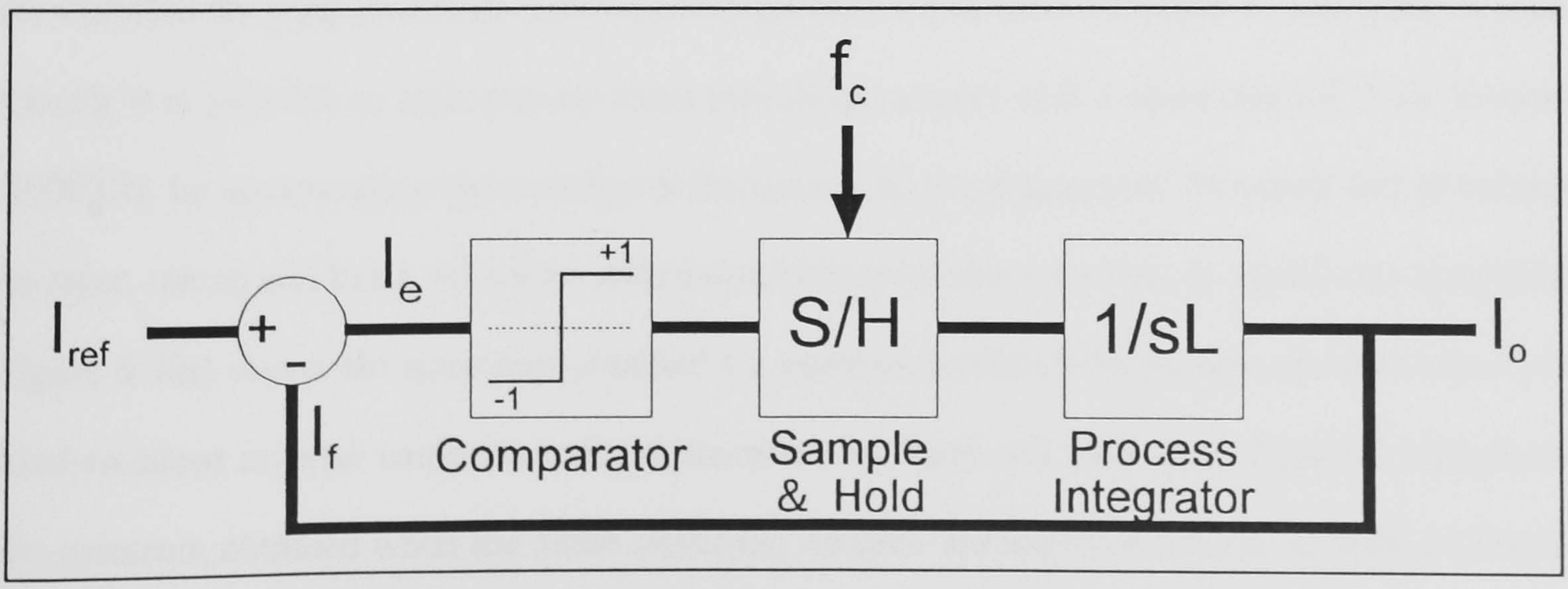

Figure 4.2 Current Regulated Delta Modulator

possible combinations of the switch states for the next interval and selects the one which optimises some specified feature of the generated waveform.

The Spectrum of Sigma Delta Modulators

Because of the widespread use of Sigma Delta Modulators, their frequency spectrum will be discussed in more detail. The spectrum of the ΣΔM is quite different from that encountered in Pulse Width Modulated systems where the output spectrum is in general concentrated around certain frequencies. In ΣΔM systems the spectrum is distributed over a wide range, and includes a significant quantity of energy at low frequencies. This energy is difficult to filter, and could cause problems in railway applications where signalling interference or high values of psophometric current may occur. The spectrum is extremely difficult to analyse; Kheraluwala and Divan [46] opted for an averaging technique, but a more accurate analysis is given by Mertens and Skudelny. [50] This method is based upon a frequency domain representation of the sampling process. However neither approach yields the exact distribution of harmonics. Finney *et al* [47] suggested that analysis may be achieved more satisfactorily using simulation.

4.2.2 Pulse Width Modulation

As stated above, Pulse Width Modulation (PWM) is a very desirable way of controlling hard-switched converters. One of the main benefits for rail traction applications is the relative ease with which harmonic elimination may be implemented. [31,51,52]. This is an important issue when attempting to avoid signalling frequencies. These harmonic elimination techniques rely on the fact that the output devices may be switched with reasonable accuracy at any point in time. Clearly it is possible to approximate these switching instants with a Resonant DC Link Inverter (RDCLI), by commutating the switches at the nearest zero voltage point. However this introduces an error, which can bring otherwise eliminated harmonics into existence in significant quantities. Figure 4.3(a) shows the spectrum obtained by simulation when 6 harmonics are eliminated in a hard-switched inverter using the method described by Patel and Hoft [31]. Figure 4.3(b) shows the spectrum obtained when the same switching instants are approximated in an RDCLI having 400 pulses per synthesised cycle. Small amounts of 'eliminated' harmonics can be seen to exist.

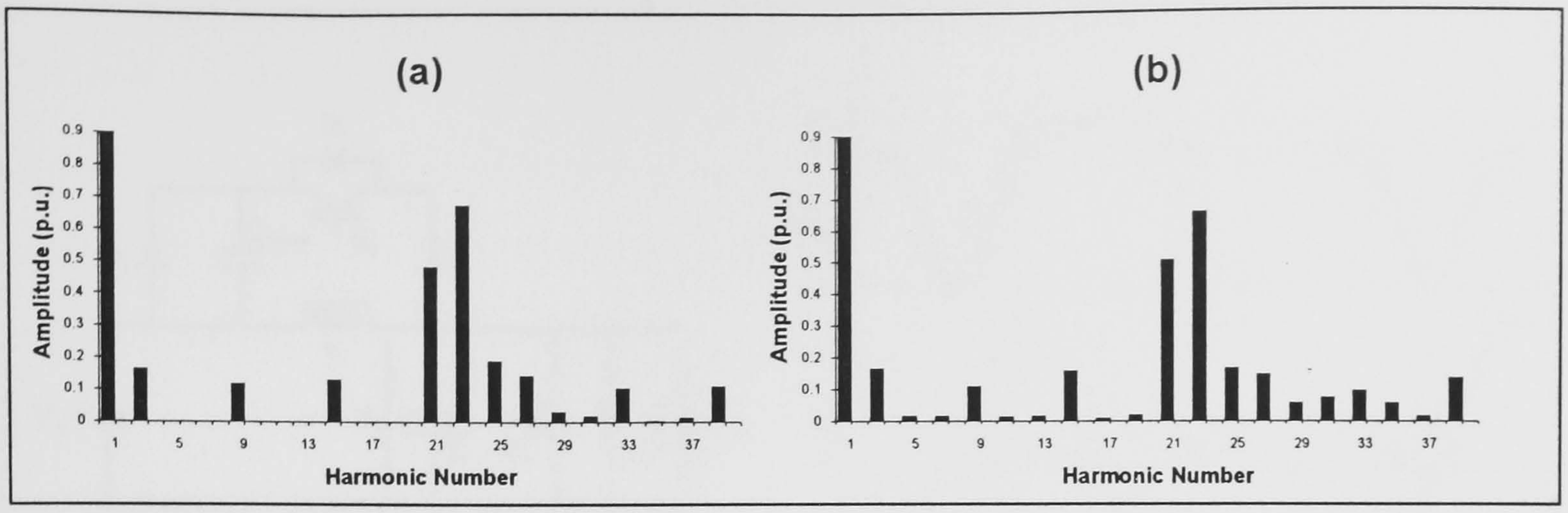

Figure 4.3 Hard-Switched and RDCLI PWM Harmonic Elimination

The effects of the errors become much worse as the number of 'chops' (commutations) increases. Another important reason for not attempting harmonic control in this manner with RDCLIs is that it does not make very good use of the beneficial features of the inverter since the modulation strategies for hard-switched inverters frequently have tightly controlled switching frequencies in order to limit device losses. Such restrictions are unnecessary in the case of the RDCLI as there is very little thermal penalty associated with each switching event.

Pulse Width Modulation may however, be implemented using Resonant DC Link Inverters if certain topology and/or control modifications are made. Several of these techniques are discussed below.

Divan *et al* [53] proposed a scheme using a modified RDLI as shown in Figure 4.4(a). Note the additional diode D2. The output stage and load are represented by a current source, I_X, and inverse-parallel diode, D_3. In practice the bus shorting switch, S_S may be implemented by turning on both switches in one leg of the output stage. The overall aim of this circuit is to achieve periods of zero voltage on the link at arbitrary instants in time. This may be realised, with the proviso of a minimum elapsed time between consecutive voltage zeros. Modification of the operation of the link clamping arrangement is required. This may be explained with reference to Figure 4.4(b) which shows the voltage V_{cr} on capacitor C_r, and resonant current i_r:

- Assume that initially (time=t0) the voltage on C_r is zero, and just about to rise. Unlike the RDCLI, the voltage on the clamp capacitor is zero at this time. As a consequence, when the voltage on C_r reaches the supply voltage, V_S, the diode D1 forward biases (time=t1).

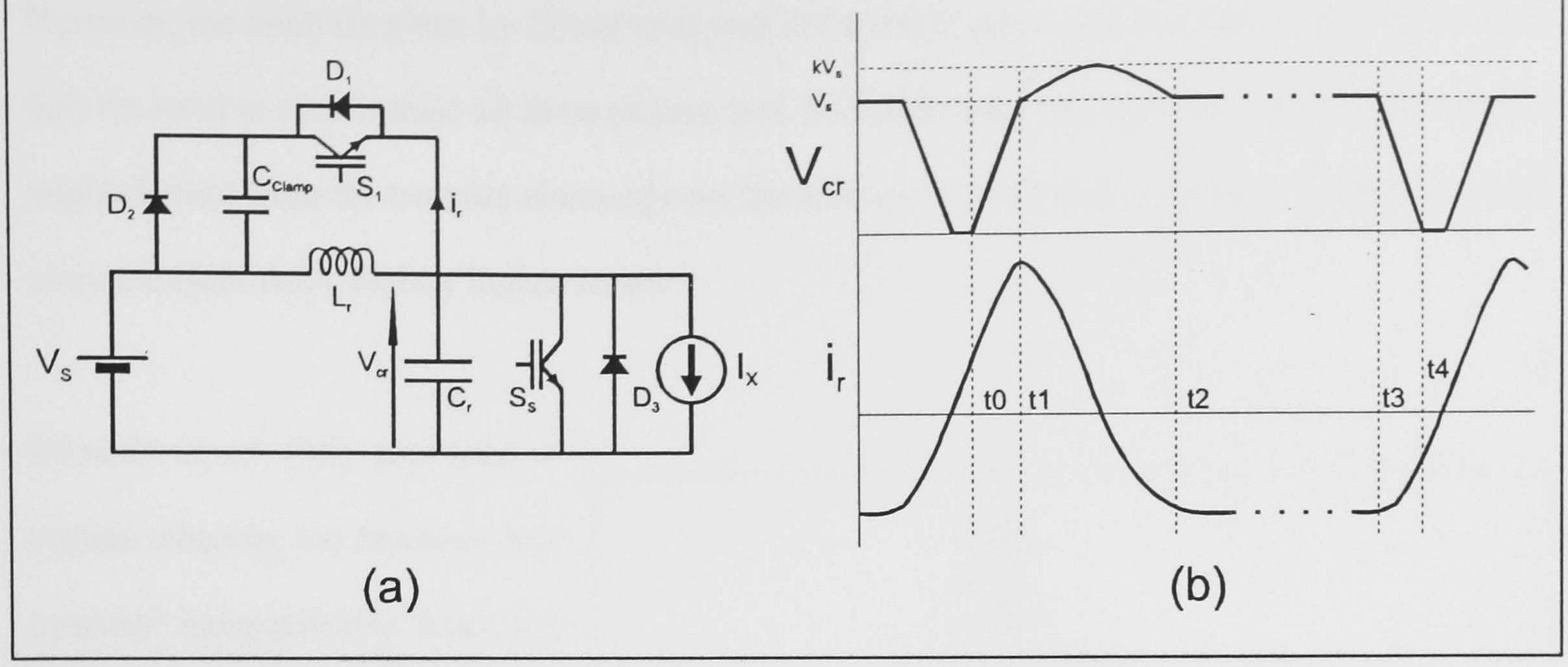

Figure 4.4 Synchronised RDCLI and Voltage & Current Waveforms

- A resonant current flows on the clamping capacitor, C_{clamp}, which must be sized such that the voltage rise across it is limited to the required clamping value, $(k-1)V_s$. The resonant current eventually reverses, flowing back through switch S_1.
- The clamp capacitor is allowed to discharge fully. Once the voltage across C_{clamp} is zero diode D_2 forward biases (time=t2). The resonant bus voltage (V_{cr}) is then held at the supply voltage V_s, until the next zero-voltage crossing of the link is required.
- Between t2 and the next demand for a zero voltage crossing, the resonant current continues to flow via L_r, D_2 and S_1.
- To initiate the next voltage zero, switch S_1 is opened. This causes the resonant current, i_r to transfer to C_r, beginning the next resonant cycle. Once V_{cr} has reached zero the switches of the output stage may be commutated with virtually zero loss.
- S_s is closed momentarily at t4 to make up for losses in the resonant circuit. This ensures that the resonant current flowing in L_r and D_2 during the time between t2 and t3, is sufficient to cause the voltage on C_r to reach zero when S_1 is opened.

Divan *et al* found that the requirement for a minimum dwell time (t_0 to t_2) meant that direct application of a conventional PWM strategy did not constitute the optimum modulation method. Instead they opted for a hybrid PWM, and Discrete Pulse Modulation strategy. It was also found that the use of such a converter eliminated the low-frequency energy normally associated with Delta Modulated RDCLIs. This would be an important benefit in rail traction applications.

However, the analysis given by Divan *et al* was for a single phase system; they expressed concern that the need to synchronise all three phases, and the minimum dwell time in a three-phase system might detract from the benefits obtained over the conventional RDCLI topology. Additionally this circuit suffers from slightly higher losses.

Elloumi *et al* [54] proposed a system whereby the resonant link operates independently from the output stage of the inverter. The topology is shown in Figure 4.5. In this case the bus shorting switch, S_S, which maintains the link oscillations, exists physically and is a high speed device to keep its losses as small as possible.

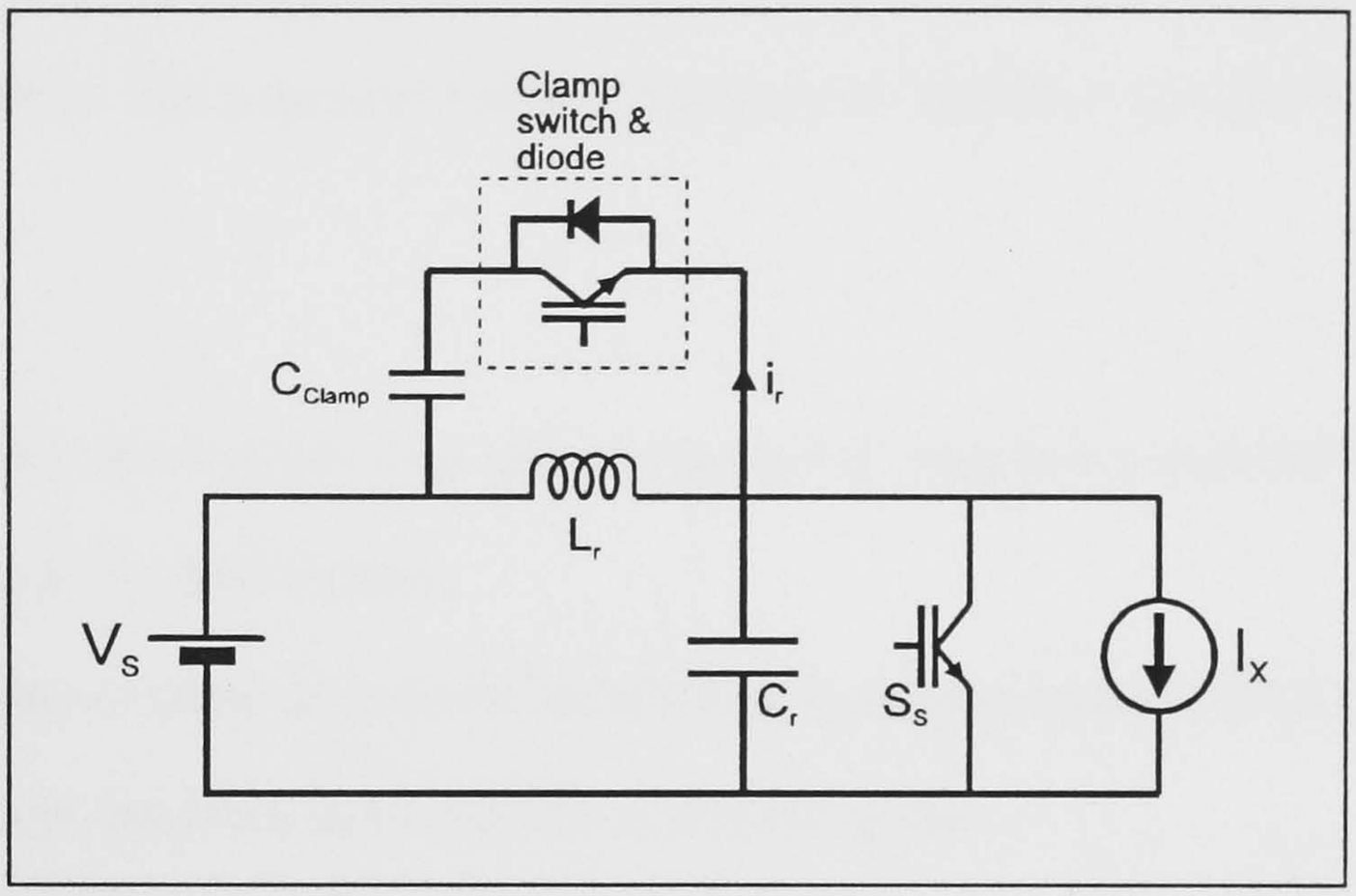

Figure 4.5 Independent Link RDCLI

The output stage consists of slower, higher power devices. These devices are commutated at the zero voltage instants of the link, and a modified PWM strategy is used which minimises the effects of quantisation of the switching instants. The additional switching device required by this system is a drawback. Also the use of low-frequency output stage, although useful for extending the power range of this family of converters, detracts from the benefits offered by the high frequency link.

The two methods outlined above for implementing PWM suffer from fairly serious problems or deficiencies. In addressing these, Venkataramanan and Divan [55] proposed a compromise scheme which does not require any additional semiconductor components and is capable of true PWM in a 3-phase configuration. This is achieved at the expense of significantly increased device losses. The overall losses are typically 50% greater than is the case for the conventional RDCLI. Figure 4.6 shows the circuit layout. In this topology the resonant capacitor, C_r, is distributed across all the switching devices. In every other respect the circuit is like the conventional RDCLI.

The devices of the output stage are turned on if required, at the zero voltage instants of the link. However, they may be turned off again at any point in time since the resonant capacitor in parallel, delays the rate of rise of the voltage across the switch. Thus the turn-off is 'soft'. So, although the commencement of conduction is constrained to particular instants, the period of conduction has arbitrary length. The turn-off of a device during a resonant cycle causes energy to be transferred to the clamp capacitor, allowing charge balance to be maintained on C_{clamp}, whilst also maintaining link oscillations. The increased losses in this type of converter are chiefly due to the following reasons:

- Unlike the conventional RDCLI, the devices of the output stage must conduct a component of resonant current in addition to the load current.
- The effective snubber capacitance across each device is less than in a conventional RDCLI operating at the same frequency; this leads to an increase in switching loss.

A major drawback of this scheme was identified by Venkataramanan and Divan. When the modulation index of the output exceeds 0.5, charge balance of the clamp capacitor can no longer be achieved. It was suggested that a hybrid PWM/Discrete Pulse Modulation strategy be adopted

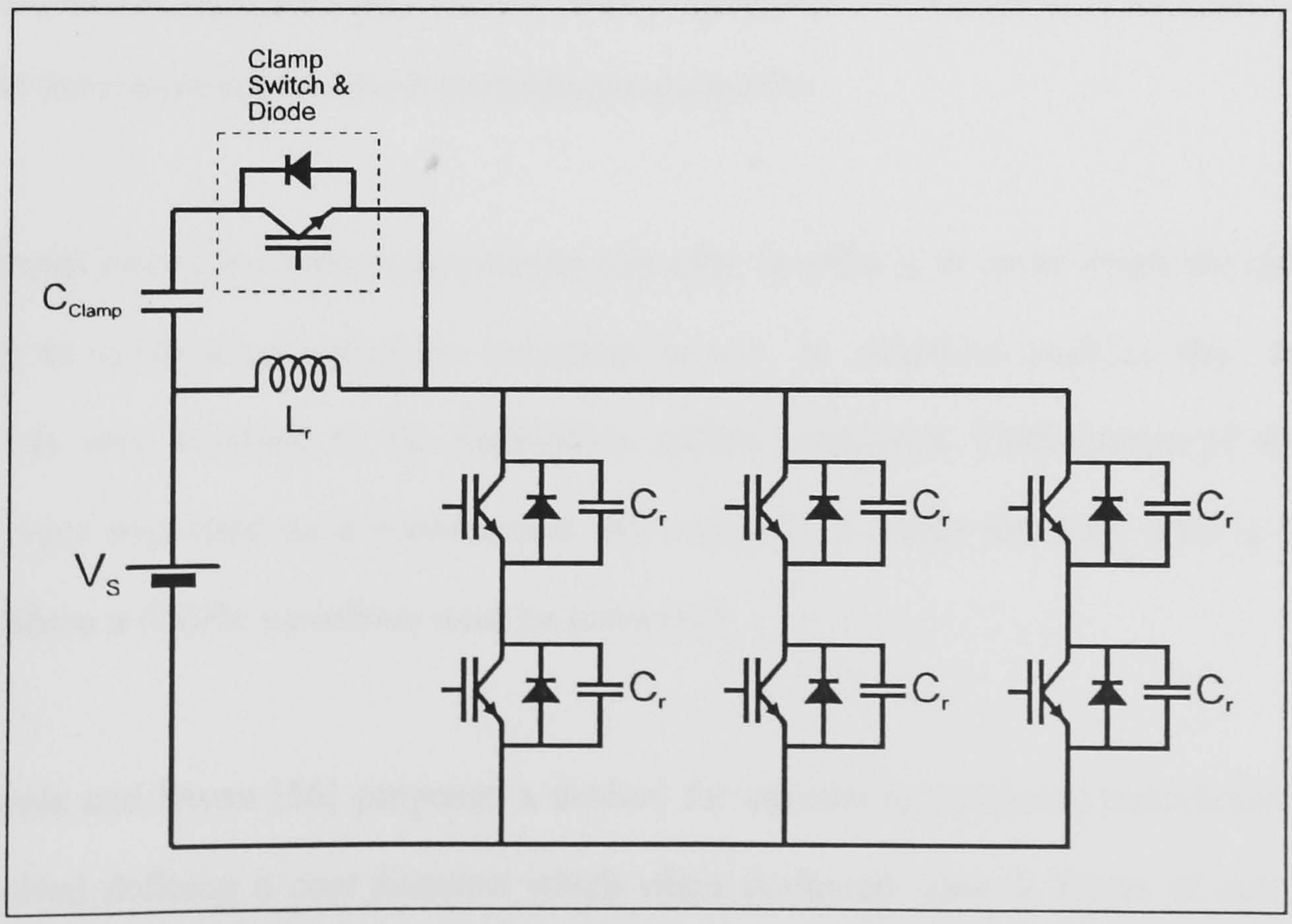

Figure 4.6 PWM-RDCLI with Distributed Resonant Capacitance

to circumvent this difficulty. Additionally it was found that the spectrum of the converter was difficult to analyse since the snubbing arrangement means that the voltage transitions are heavily load dependent. This would be a disadvantage in rail traction applications where a well defined spectrum is desirable.

4.2.3 Pre-programmed Discrete Pulse Modulation

In sections 4.2.1 and 4.2.2 several problems were identified with the modulation strategies, especially where rail traction applications are concerned. The main difficulty lies in accurately predicting the generated spectra. This is chiefly because the modulators operate in real time and as a consequence the switching pattern varies from cycle to cycle. This tends to spread the harmonic energy over a wide range, and in the case of Delta Modulators leads to significant quantities of harmonics at low frequencies where they are difficult to filter. In section 4.2.2 it was seen that PWM methods may be employed to improve the distribution of harmonics, but this is at the expense of increased circuit complexity, or additional losses. The ideal modulation strategy would allow accurate prediction of the generated spectra and be capable of implementation on an unmodified RDCLI topology. *Pre-programmed* Discrete Pulse Modulation strategies are a way of achieving this goal. With this method, optimised pulse patterns are pre-calculated and stored in look-up tables. Because the modulation pattern is identical from one cycle to the next, it is easier to analyse the converter in terms of its harmonic properties.

An additional issue where pre-programming can offer benefits is in cases where the ratio of link frequency to synthesised waveform frequency is low. In situations such as this, the output spectrum is very sensitive to the modulation pattern employed. Optimisation of the pattern becomes very important as a consequence. An example of where this may arise is aerospace systems where a 400Hz waveform must be generated.

Kheraluwala and Divan [56] proposed a method for calculating optimised modulation patterns. This involved defining a *cost function* which when evaluated, gave a 'figure of merit' for the harmonic spectrum generated by the pattern under consideration. For low frequency ratios where

there are few pulses contained in each synthesised cycle, an *exhaustive search* could be carried out. This is where the cost function is evaluated for every possible modulation pattern. Kheraluwala and Divan found, using an Apollo Workstation, that this method was useful for frequency ratios up to 80. The author has found the upper limit to be around 60 using a 386 PC. To extend the application of the method to higher frequency ratios, Kheraluwala and Divan proposed a random search method. This was implemented by evaluating the cost function of patterns selected at random from the set of possibilities. This process was performed for a fixed period of time with the results being stored in 'bins' classified by the magnitude of the fundamental component of the pattern in question. The 'bins' are updated when a pattern is found which generates the corresponding fundamental component, but at lower cost. Thus the longer the process is run, the greater is the probability of improving the contents stored in the bins. This method was found to be useful for ratios up to 100. It was suggested that above this value Sigma Delta Modulation be used.

4.2.4 Optimised Modulation Patterns for High Frequency Ratios

The work described in section 4.2.3 addressed the problem of complex optimisation for low frequency ratios. However, the method cannot be extended to higher frequency ratios due to the large amount of computation time which would be required, even using a mainframe computer. The advantage of being able to do such an optimisation is that it would enable complex harmonic manipulations to be performed, (such as harmonic minimisation) even where the synthesised frequency is low.

The problem is one of large-scale optimisation; Suppose it is required to synthesise a waveform having 'n' pulses per cycle. It is commonplace to employ quarter-wave symmetry in order to eliminate even harmonics so that the waveform consists of 4 similar sections containing $n/4$ pulses. This means that there are $2^{n/4}$ combinations of pulses. 'n' may typically be much greater than 100, and as a consequence the number of combinations can become enormous. The optimisation process has been tackled by Ellams and Mansell [57] and forms the subject of the rest of this chapter.

4.3 Mathematical Description of Resonant DC Link Inverter Waveforms

4.3.1 Introduction

In order to allow investigation of modulation schemes and calculation of cost functions, it is necessary to know the magnitudes of the harmonics generated by a particular pulse pattern. This information may be obtained by performing an FFT on the waveform in question but it is far more efficient in terms of computation time to employ a mathematical description of the harmonic spectrum. This is especially important where spectra must be repeatedly calculated, as is required by the 'Simulated Annealing' algorithm which is described in Section 4.4. A mathematical description of the spectra generated by RDCLIs is given below in two parts. The first part examines the spectrum obtained from an unclamped Resonant DC Link Inverter. This is included as an introduction to the second section which applies to the clamped inverter, and also as useful background information, since this topology may replace its clamped counterpart in many applications when higher voltage switching devices become available.

4.3.2 Spectrum of the Unclamped Resonant DC Link Inverter

It is assumed that the pole voltage waveform of the unclamped inverter consists of perfectly sinusoidal pulses as shown in Figure 4.7. This is a fairly good approximation for an unloaded converter. The waveform is also assumed to possess quarter-wave symmetry, with one complete cycle occupying 360 degrees electrical. The synthesised waveform is constrained to change

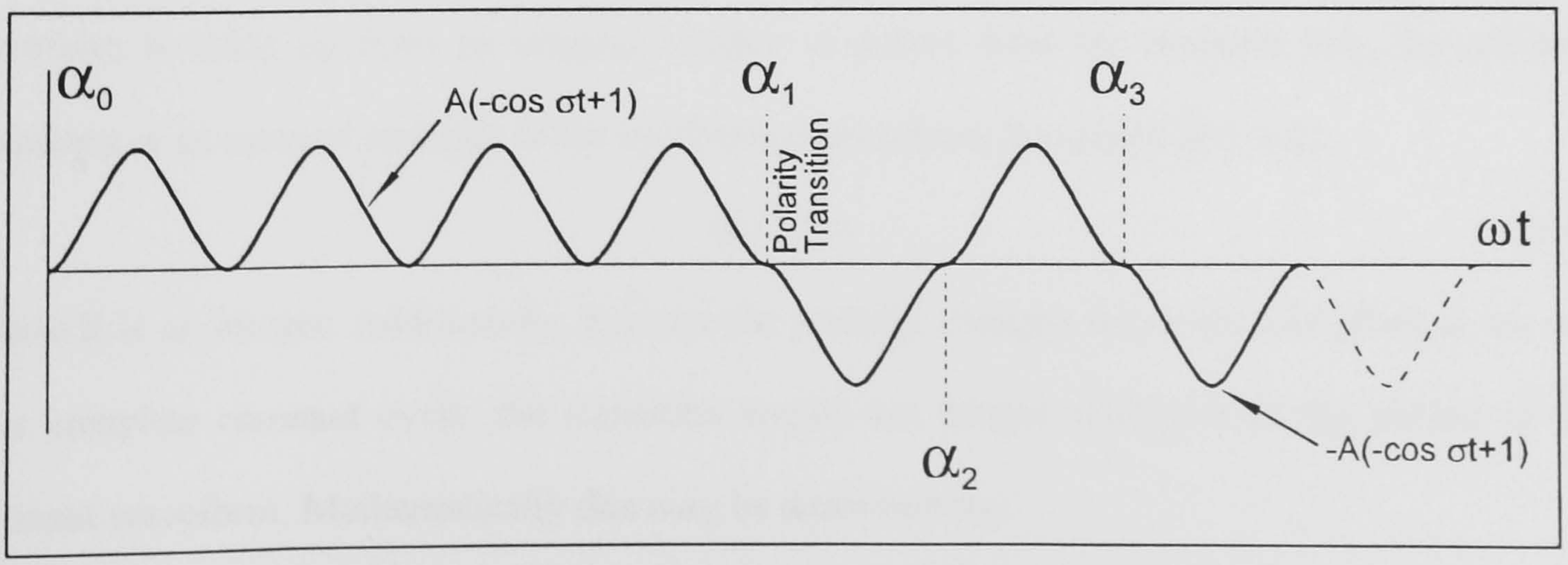

Figure 4.7 Section of Unclamped RDCLI Pole Voltage Waveform

polarity only at instants of zero voltage. Let the angle at which polarity changes occur be denoted by α_0, α_1, α_2,..... Assume that there are 'M' polarity transitions per *quarter* cycle. Thus $\alpha_0=0$, and $\alpha_{2M+1}=\pi$.

The waveform may be represented by a Fourier series, $f(\omega t)$ as follows;

$$f(\omega t)=\sum_{n=1}^{\infty}\left[a_n\cos(n\omega t)+b_n\sin(n\omega t)\right] \tag{4.1}$$

where;

$$a_n=\frac{1}{\pi}\int_0^{2\pi} f(\omega t)\cos(n\omega t)d(\omega t) \tag{4.2}$$

and

$$b_n=\frac{1}{\pi}\int_0^{2\pi} f(\omega t)\sin(n\omega t)d(\omega t) \tag{4.3}$$

Due to the quarter wave symmetry $a_n=0$, for all n. Also, due to the properties of symmetry;

$$f(\omega t)=-f(\omega t+\pi) \tag{4.4}$$

Using the feature described by (4.4), equation (4.3) becomes;

$$b_n=\frac{2}{\pi}\int_0^{\pi} f(\omega t)\sin(n\omega t)d(\omega t) \tag{4.5}$$

Let the angular frequency of the resonant link be denoted by σ. Because the synthesised waveform is made up from an integral number of pulses from the resonant link, the resonant frequency is an integral multiple of the synthesised waveform frequency (ω). i.e.;

$$\sigma=R\omega \tag{4.6}$$

Where R is an integer. Additionally, because the polarity changes may only take place at the end of a complete resonant cycle, the transition angles are integer multiples of the *period* of the resonant waveform. Mathematically this may be described by;

$$\alpha_i = \omega t_i = \omega m \times \frac{2\pi}{\sigma} \tag{4.7}$$

where m is an integer. Substituting for σ in (4.7) from (4.6) gives;

$$\alpha_i = m \times \frac{2\pi}{R} \tag{4.8}$$

Substituting for $f(\omega t)$ in (4.5) gives;

$$b_n = \frac{2}{\pi}\left[\int_{\alpha_0}^{\alpha_1} A\left(-\cos(\sigma t)+1\right).\sin(n\omega t).d(\omega t) - \int_{\alpha_1}^{\alpha_2} A\left(-\cos(\sigma t)+1\right).\sin(n\omega t).d(\omega t) + \ldots + \int_{\alpha_{2M}}^{\alpha_{2M+1}} A\left(-\cos(\sigma t)+1\right).\sin(n\omega t).d(\omega t)\right]$$

(4.9)

this may be re-written as;

$$b_n = \frac{2}{\pi}\sum_{k=0}^{k=2M}(-1)^k \int_{\alpha_k}^{\alpha_{k+1}} A\left(-\cos(\sigma t)+1\right).\sin(n\omega t).d(\omega t) \tag{4.10}$$

Substituting for σ in (4.10) from (4.6), and separating the brackets gives the following;

$$b_n = \frac{2}{\pi}\sum_{k=0}^{k=2M}(-1)^{k+1} \int_{\alpha_k}^{\alpha_{k+1}} A.\cos(R\omega t).\sin(n\omega t).d(\omega t) + \frac{2}{\pi}\sum_{k=0}^{k=2M}(-1)^{k} \int_{\alpha_k}^{\alpha_{k+1}} A.\sin(n\omega t).d(\omega t)$$

(4.11)

Consider the first summation in equation (4.11); this may be rearranged as follows;

$$\frac{2}{\pi}\sum_{k=0}^{k=2M}(-1)^{k+1} \int_{\alpha_k}^{\alpha_{k+1}} A.\cos(R\omega t).\sin(n\omega t).d(\omega t) = \frac{2}{\pi}\sum_{k=0}^{k=2M}(-1)^{k+1} \int_{\alpha_k}^{\alpha_{k+1}} \frac{A}{2}\left[\sin(n+R)\omega t + \sin(n-R)\omega t\right]d(\omega t)$$

(4.12)

Evaluating the integral yields the following;

$$\frac{A}{\pi}\sum_{k=0}^{k=2M}(-1)^{k+1}\left[\frac{-\cos(n+R)\omega t}{(n+R)} - \frac{\cos(n-R)\omega t}{(n-R)}\right]_{\alpha_k}^{\alpha_{k+1}} \tag{4.13}$$

rearranging gives;

$$\frac{A}{\pi\left(n^2-R^2\right)}\sum_{k=0}^{k=2M}(-1)^{k}\left[2n.\cos(n\omega t).\cos(R\omega t) + 2R.\sin(n\omega t).\sin(R\omega t)\right]_{\alpha_k}^{\alpha_{k+1}} \tag{4.14}$$

Expanding the summation gives;

$$\frac{A}{\pi\left(n^2-R^2\right)}\left[\begin{array}{l}2n.\cos(n\alpha_1).\cos(R\alpha_1)+2R.\sin(n\alpha_1).\sin(R\alpha_1)-2n.\cos(n\alpha_0).\cos(R\alpha_0)-2R\sin(n\alpha_0).\sin(R\alpha_0)\\-\left(2n.\cos(n\alpha_2).\cos(R\alpha_2)+2R.\sin(n\alpha_2).\sin(R\alpha_2)-2n\cos(n\alpha_1).\cos(R\alpha_1)-2R.\sin(n\alpha_1).\sin(R\alpha_1)\right)\\+2n.\cos(n\alpha_3).\cos(R\alpha_3)+2R.\sin(n\alpha_3).\sin(R\alpha_3)-2n.\cos(n\alpha_2).\cos(R\alpha_2)-2R.\sin(n\alpha_2).\sin(R\alpha_2)\\-\ldots\ldots\ldots+2n.\cos(n\alpha_{2M+1}).\cos(R\alpha_{2M+1})+2R.\sin(n\alpha_{2M+1}).\sin(R\alpha_{2M+1})-2n.\cos(n\alpha_{2M}).\cos(R\alpha_{2M})\\-2R.\sin(n\alpha_{2M}).\sin(R\alpha_{2M})\end{array}\right] \tag{4.15}$$

But, from (4.8), $R\alpha_i = 2\pi m$. Therefore $\sin(R\alpha_i)=0$, and $\cos(R\alpha_i)=1$. Also remember α_0=0, and α_{2M+1}=π. Thus (4.15) reduces to:

$$\frac{A}{\pi\left(n^2-R^2\right)}\left[-4n-2\sum_{k=1}^{k=2M}(-1)^k 2n.\cos(n\alpha_k)\right] \tag{4.16}$$

Due to the quarter wave symmetry, $\alpha_k = \pi-\alpha_{2M+1-k}$. This allows the summation to be re-written as:

$$\frac{4A}{\pi\left(R^2-n^2\right)}\left[n+2\sum_{k=1}^{k=M}(-1)^k n.\cos(n\alpha_k)\right] \tag{4.17}$$

The second summation of equation (4.11) may be analysed in a similar manner, and gives the result;

$$\frac{4A}{n\pi}\left[1+2\sum_{k=1}^{k=M}(-1)^k \cos(n\alpha_k)\right] \tag{4.18}$$

This may be combined with (4.17) to give the final result which describes the harmonic spectrum of an unclamped RDCLI Discrete Pulse Modulated waveform. This is shown below in a rearranged form, as equation (4.19).

$$b_n = \frac{4A}{\pi}\left[\frac{1}{n}+\frac{n}{\left(R^2-n^2\right)}+2\sum_{k=1}^{k=M}(-1)^k\left(\frac{\cos(n\alpha_k)}{n}+\frac{n.\cos(n\alpha_k)}{\left(R^2-n^2\right)}\right)\right] \tag{4.19}$$

4.3.3 Spectrum of the Clamped Resonant DC Link Inverter

The pole voltage waveform for the clamped RDCLI is assumed to have the general shape shown in Figure 4.8. This consists of intervals of perfect sinusoids during resonant periods, interspersed by periods of constant voltage whilst the clamp is in operation. The 'polarity transitions' are labelled α_0, α_1, α_2,...., in the same way as section 4.3.2.

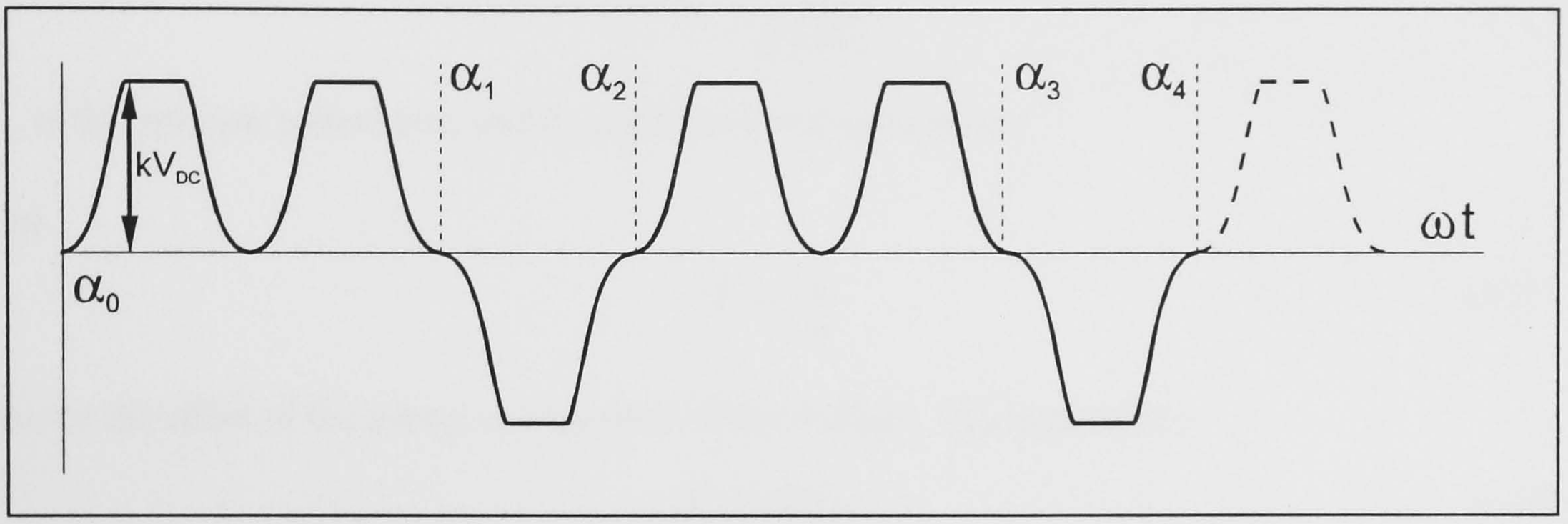

Figure 4.8 Section of Clamped RDCLI Pole Voltage Waveform

Each resonant pulse is deemed to consist of 3 modes, A, B, and C, as defined in Figure 4.9. The length of the modes A, B, and C, are given by t_a, t_b, and t_c respectively. The resonant pulse begins at time T_0, and modes A, B and C end at time T_A,T_B and T_C respectively.

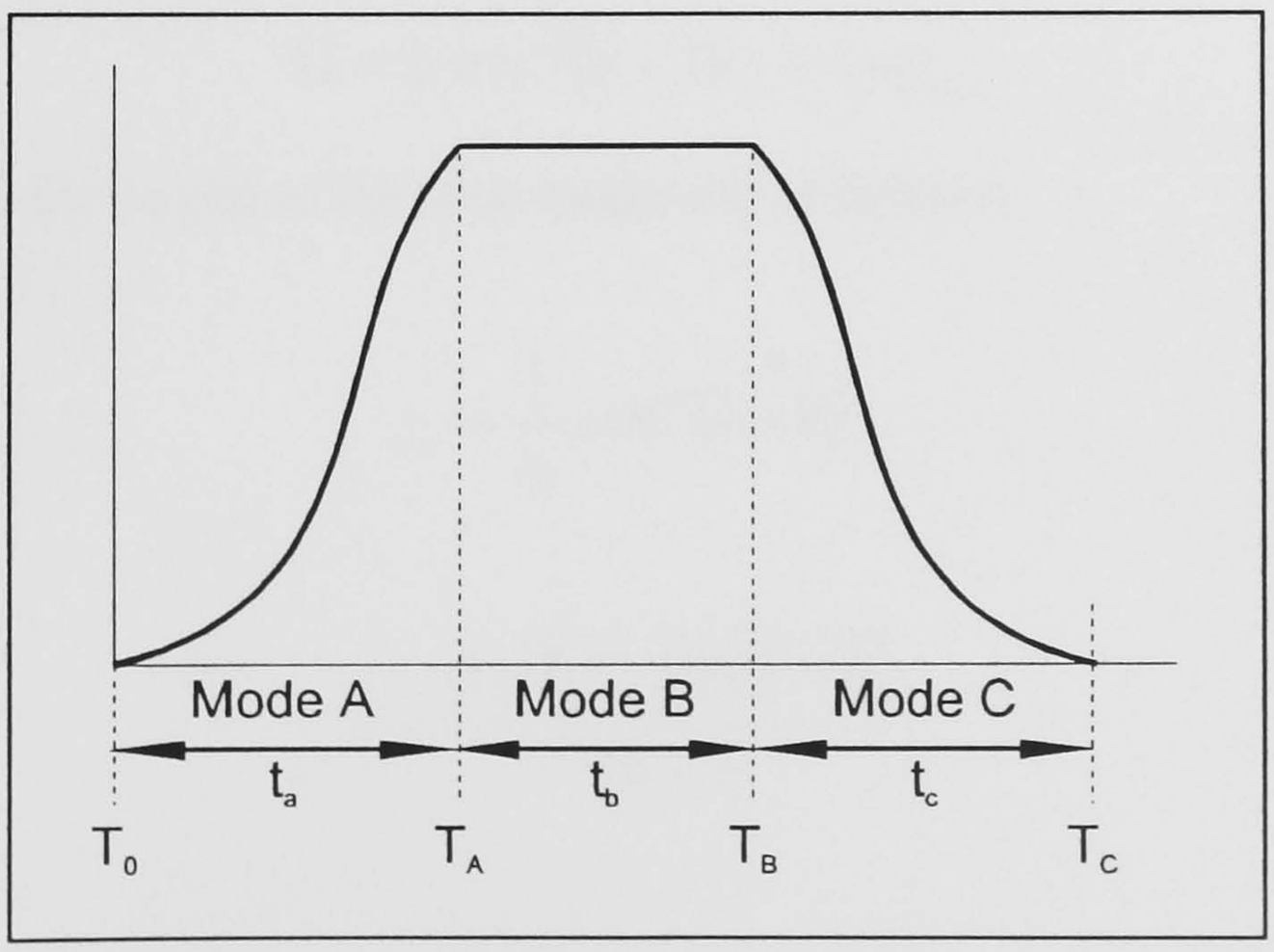

Figure 4.9 Detail of Resonant Pulse

Let the angular frequency of the synthesised waveform be ω, and the undamped angular frequency of the resonant components be ε_0. V_{DC} is the DC supply voltage. The electrical angle

at the start of a resonant pulse is ωT_0. Let this value be denoted by 'β'. Thus the pole voltage waveform during mode A (V_A) is described by the following equation:

$$V_A = V_{DC}\left(-\cos\left(F(\omega t - \beta)\right) + 1\right) \tag{4.20}$$

where

$$\varepsilon_0 = \frac{1}{\sqrt{L_r C_r}} \tag{4.21}$$

L_r is the resonant inductance, and C_r is the resonant capacitance.

and

$$F = \frac{\varepsilon_0}{\omega} \tag{4.22}$$

Due to the effect of the clamp, during mode B the voltage, V_B, is given by;

$$V_B = kV_{DC} \tag{4.23}$$

Where k is the clamping coefficient. During Mode C, the pole voltage, V_C is given by;

$$V_C = V_{DC}\left(\cos\left(F(\omega t - \beta) + G\right) + 1\right) \tag{4.24}$$

where

$$G = 2.\cos^{-1}(k-1) - \pi - \varepsilon_0 t_b \tag{4.25}$$

It may be shown that the lengths of the three modes are as follows;

$$t_a = \frac{1}{\varepsilon_0}\cos^{-1}(1-k) \tag{4.26}$$

$$t_b = \frac{2\sqrt{L_r C_r}\sqrt{k(2-k)}}{(k-1)} \tag{4.27}$$

$$t_c = \frac{1}{\varepsilon_0}\cos^{-1}(1-k) \tag{4.28}$$

Let 'p' be a counter for the resonant pulses, which is reset to zero at each polarity transition. Thus, a general expression may be written for the electrical angle, β, at the start of a resonant pulse after the *k*th polarity transition;

$$\beta = \alpha_k + p\omega T_C \tag{4.29}$$

Using a Fourier series representation as defined by equations (4.1) to (4.3), a_n is zero for all n due to the quarter wave symmetry. 'M' is the number of polarity transitions per quarter cycle. Substituting for $f(\omega t)$ in (4.5), using (4.20), (4.23), and (4.24) gives equation (4.30) as a representation for b_n.

$$b_n = \frac{2V_{DC}}{\pi}\sum_{k=0}^{2M}(-1)^k \sum_{p=0}^{\frac{\alpha_{k+1}-\alpha_k}{\omega T_C}-1}\left[\begin{array}{l}\int_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A}\left(-\cos\left(F(\omega t-\beta)\right)+1\right)\sin(n\omega t)d(\omega t)+\int_{p\omega T_C+\alpha_k+\omega T_A}^{p\omega T_C+\alpha_k+\omega T_B} k\sin(n\omega t)d(\omega t)+ \\ \int_{p\omega T_C+\alpha_k+\omega T_B}^{p\omega T_C+\alpha_k+\omega T_C}\left(\cos\left(F(\omega t-\beta)+G\right)+1\right)\sin(n\omega t)d(\omega t)\end{array}\right] \tag{4.30}$$

Consider the first integral of (4.30);

$$\int_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A}\left(-\cos\left(F(\omega t-\beta)\right)+1\right)\sin(n\omega t)d(\omega t) = \int_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A}\sin(n\omega t)d(\omega t) - \int_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A}\cos(F\omega t - F\beta)\sin(n\omega t)d(\omega t)$$

Rearranging this expression and evaluating the integrals yields;

$$\frac{-1}{n}\left[\cos(n\omega t)\right]_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A} + \frac{1}{2\left(F^2-n^2\right)}\left[(F-n)\cos\left((F+n)\omega t - F\beta\right) - (F+n)\cos\left((F-n)\omega t - F\beta\right)\right]_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A} \tag{4.31}$$

Consider the second integral of (4.30);

$$\int_{p\omega T_C+\alpha_k+\omega T_A}^{p\omega T_C+\alpha_k+\omega T_B} k\sin(n\omega t)d(\omega t) = \frac{1}{n}\left[-k\cos(n\omega t)\right]_{p\omega T_C+\alpha_k+\omega T_A}^{p\omega T_C+\alpha_k+\omega T_B} \tag{4.32}$$

Take the third integral of (4.30);

$$\int_{p\omega T_C+\alpha_k+\omega T_B}^{p\omega T_C+\alpha_k+\omega T_C}\left(\cos\left(F(\omega t-\beta)+G\right)+1\right)\sin(n\omega t)d(\omega t) =$$

$$\frac{1}{2}\left[\frac{-\cos\left((F+n)\omega t+G-F\beta\right)}{(F+n)} + \frac{\cos\left((F-n)\omega t+G-F\beta\right)}{(F-n)}\right]_{p\omega T_C+\alpha_k+\omega T_B}^{p\omega T_C+\alpha_k+\omega T_C} - \left[\frac{\cos(n\omega t)}{n}\right]_{p\omega T_C+\alpha_k+\omega T_B}^{p\omega T_C+\alpha_k+\omega T_C} \tag{4.33}$$

Substituting (4.31), (4.32), and (4.33) back into (4.30) gives an expression (4.34) describing the harmonic spectrum of a clamped RDCLI. The necessity to define 3 separate modes in each resonant cycle makes the final result considerably less elegant than is the case for the unclamped RDCLI.

(4.34)

$$b_n = \frac{2V_{DC}}{\pi}\sum_{k=0}^{2M}(-1)^k \sum_{p=0}^{\frac{\alpha_{k+1}-\alpha_k}{\omega T_C}-1}\left[\begin{array}{l}\left[\frac{1}{2\left(F^2-n^2\right)}\left((F-n)\cos\left((F+n)\omega t-\varepsilon_0 T_0\right)-(F+n)\cos\left((F-n)\omega t-\varepsilon_0 T_0\right)\right)-\frac{1}{n}\cos(n\omega t)\right]_{p\omega T_C+\alpha_k}^{p\omega T_C+\alpha_k+\omega T_A} \\ -\left[\frac{k}{n}\cos(n\omega t)\right]_{p\omega T_C+\alpha_k+\omega T_A}^{p\omega T_C+\alpha_k+\omega T_B} \\ +\left[\frac{1}{2\left(F^2-n^2\right)}\left((F+n)\cos\left((F-n)\omega t+G-\varepsilon_0 T_0\right)-(F-n)\cos\left((F+n)\omega t+G-\varepsilon_0 T_0\right)\right)-\frac{1}{n}\cos(n\omega t)\right]_{p\omega T_C+\alpha_k+\omega T_B}^{p\omega T_C+\alpha_k+\omega T_C}\end{array}\right]$$

4.4 Simulated Annealing

4.4.1 Introduction

Simulated Annealing is the optimisation process by which RDCLI pulse patterns are selected. To assess each pulse pattern a cost function is evaluated and this requires knowledge of the harmonic spectrum which the pattern will generate. This is calculated using the equations derived above. This section begins with an overview of the simulated annealing process, and concludes with examples of its application to harmonic control in Resonant DC Link Inverters.

4.4.2 Optimising Functions Using Simulated Annealing

The optimisation of a function y means finding its maximum or minimum value. For clarity the discussion here will refer exclusively to minimisation, although the principles underlying the two operations are identical. A minimisation procedure can be converted to maximisation by simply changing the sign of y. In engineering the interest in function optimisation stems from the desire to adopt the best solution to a problem from many possibilities. For example, y may represent the area of silicon required for an IC, or the amount of copper wound on an inductor, or a

complicated function of several design variables. Finding an extremum of y then indicates the optimum design which can be achieved. The function y may be considered to be a measure of 'goodness' of the design, and where minimisation is the aim, high values of y correspond to a penalty, or high *cost*. Hence y is referred to as the *cost function*.

In real engineering problems y is not usually a simple function, and as a consequence will have many *local minima*, as shown in Figure 4.10. In this diagram y is a function of one variable, x. Suppose y is evaluated initially at A, and small changes are made in x such that the value of y is reduced. This process could be repeated until point B was arrived at, where y would stop decreasing. The function increases either side of B, so it is known that a minimum has been located but it is only a *local* minimum. By inspection it can be seen that the overall *global* minimum is at C. This example is a trivial one, but it demonstrates that simply moving 'downhill' on a function until it stops decreasing does not necessarily lead to the function's minimum point, and can cause the algorithm to become trapped in a local minimum. When analysing a function of many variables this becomes a serious problem and will frequently prevent a good extremum from being located. Despite this significant deficiency, many optimisation algorithms operate in this manner, by improving the cost function with every step until no further improvements are possible, i.e. by moving towards the nearest minimum. The optimisation problem presented by selection of pulse patterns for RDCLIs is very complex and means that techniques only accepting downhill steps are virtually useless, and will almost immediately become trapped in a local

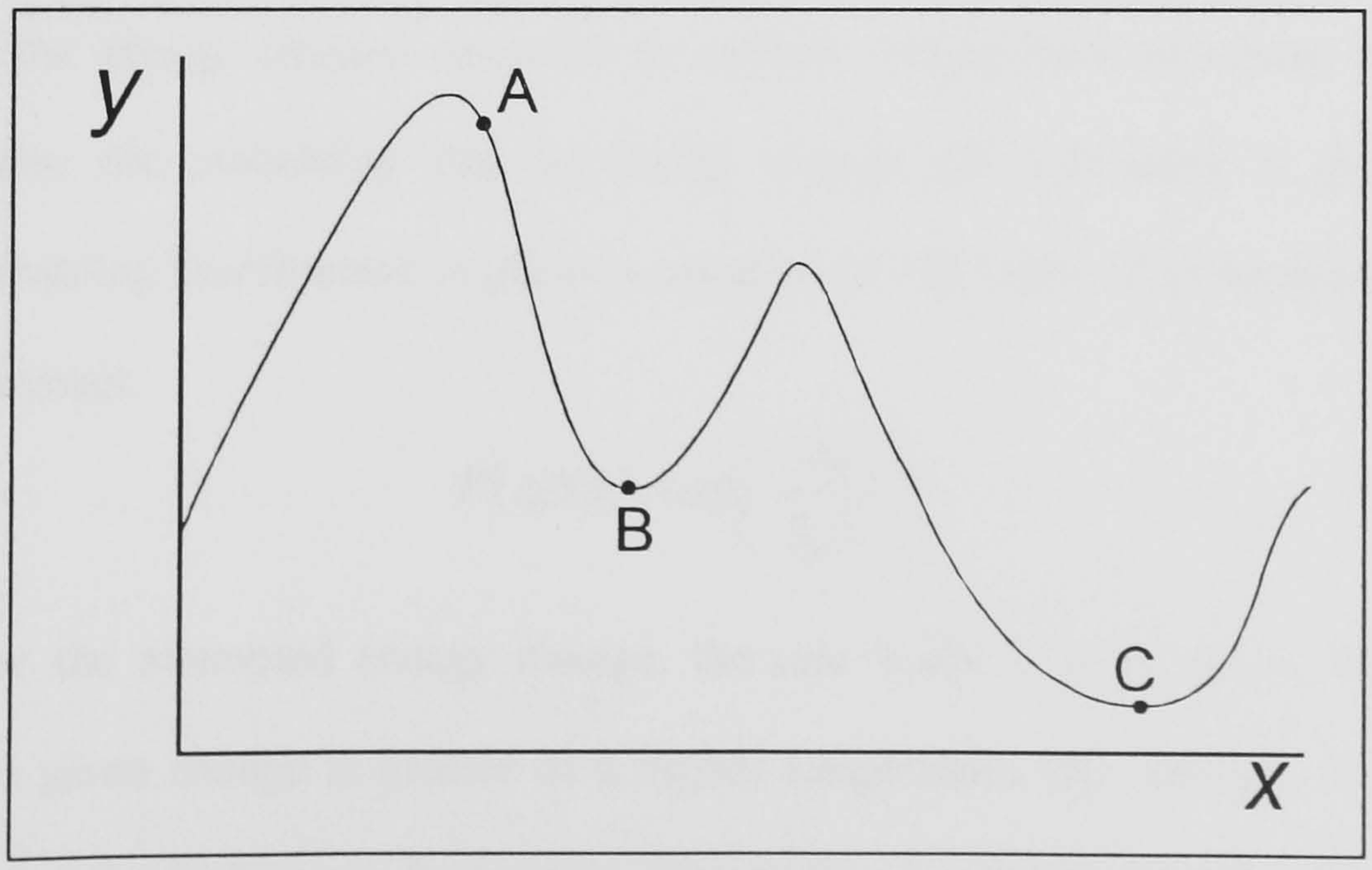

Figure 4.10 Local and Global Minima

minimum. This is not the case with Simulated Annealing techniques. [58,59,60]

In Simulated Annealing algorithms, a proposed change in the variables which causes a decrease in function y (i.e. a downhill step) is always accepted, but additionally a proposed change which causes an uphill move is *sometimes* accepted. The criterion for acceptance is the value of a probability function as explained below. Because uphill steps can be accepted there is a finite probability of the algorithm 'jumping out' of a local minimum, and moving toward a different, and hopefully better, extremum. Initially many uphill moves are accepted allowing a large amount of the variable space to be explored. As the optimisation procedure advances, the probability of acceptance of an uphill step is gradually reduced, allowing improvements in the cost function to be achieved but also giving the chance of escape from local minima. Eventually the probability of uphill moves becomes so low that the algorithm settles into a minimum from which it cannot escape.

As implied by its name, Simulated Annealing has many analogies with the way in which materials order themselves during the cooling or annealing process. At high temperatures substantial atomic rearrangement is possible. If the temperature is reduced slowly enough, the degree of freedom of the constituent particles gradually reduces until the material freezes into an ordered state. The ordered, or crystalline state, of a material usually corresponds to a low-energy condition. In Simulated Annealing algorithms, the proposed moves produce changes in the cost function which correspond to the energy changes incurred by atomic arrangement in nature. In the natural annealing process the probability that an energy change ΔE will occur is governed by the Boltzmann Probability Distribution as given in equation (4.35), where T is temperature, and k_b is Boltzmann's constant.

$$P(\Delta E) = \exp\left(\frac{-\Delta E}{k_b T}\right) \tag{4.35}$$

Thus the larger the attempted energy change, the less likely it is to occur, but overall, the probability of a given change is greater at a higher temperature. By analogy, in the Simulated Annealing process the Boltzmann Probability Distribution is used to describe the probability of

an uphill move in cost function y having magnitude ΔE. It is useful to still refer to T as 'temperature', but the constant 'k_b' is no longer Boltzmann's constant; it is a scaling factor appropriate, and peculiar to, the application.

Although this method provides the possibility of escaping from local minima, there is no guarantee of reaching the global minimum. In fact in a system of many variables it is most unlikely that it will be reached. Instead the aim is to achieve a good local minimum, or a minimum which cannot be significantly improved upon using a reasonable amount of computing effort. There are several factors which can affect the quality of the minimum achieved:

i. STARTING TEMPERATURE: This affects the initial 'random' variable space search.

ii. COOLING SCHEDULE: i.e. how quickly the temperature is reduced. This has a powerful influence on the amount of variable space which is searched, and thus on the quality of the final result.

iii. STARTING POINT: If the algorithm is given a starting point which is in the vicinity of the global minimum it is likely to give a much better result than a random starting point.

The theory behind Simulated Annealing is fairly straight forward. Most of the complications in its application arise from selecting the appropriate cooling schedule and cost function. It is important that the cost function accurately reflects, with suitable weighting, the parameters that are required to be optimised.

4.4.3 Applying Simulated Annealing to Modulation of RDCLIs

As explained above, the output of a clamped RDCL inverter is determined by the combination of positive and negative pulses selected from the resonating link. Consequently the number of possible configurations is finite, though very large. The problem is one of *combinatorial* optimisation and can be conveniently expressed in matrix notation. Consider a general pulse train

typical of the output of clamped RDCL Inverters as shown in Figure 4.11. Let this be the function *pu(ωt)*. The objective is to control the harmonic content of *pu(ωt)*, consequently it is necessary to perform a Fourier Analysis on *pu(ωt)*.

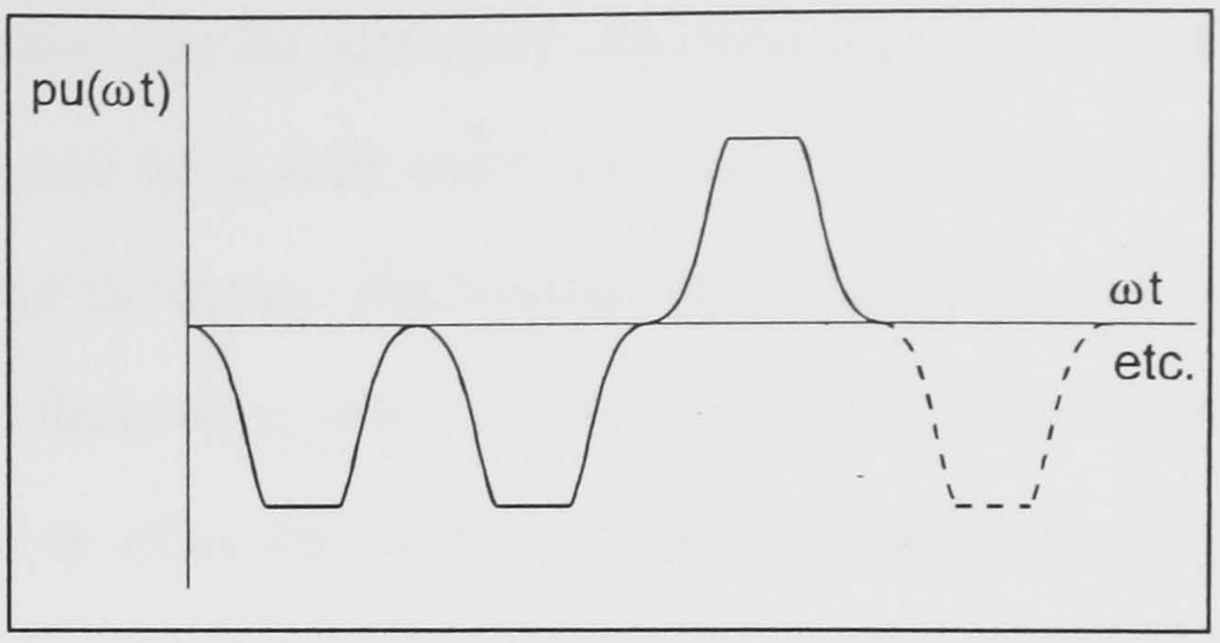

Figure 4.11 Clamped RDCLI Pulse Train

The Fourier coefficients (b_n) resulting from this analysis are given by equation (4.34).

Let s_n be the function which determines the sign of the *n*th pulse. This gives the matrix notation as shown in equation (4.36), where **r** denotes the Fourier Integral evaluated over the period of individual pulses. R is the number of pulses in each cycle of the synthesised output waveform. The general term of matrix **r** is r_{ij} as defined by equation (4.37), where T_P is the period of one resonant pulse.

$$\begin{bmatrix} r_{11} & r_{12} & r_{13} & \cdots & r_{1(R/4)} \\ r_{21} & r_{22} & \cdots & \cdots & r_{2(R/4)} \\ r_{31} & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ s_3 \\ \cdots \\ s_{(R/4)} \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ \cdots \\ \cdots \end{bmatrix} \tag{4.36}$$

$$r_{ij} = \frac{4}{\pi} \int_{(j-1)\omega T_p}^{j\omega T_p} PU(\omega t) \sin(i\omega t) d(\omega t) \tag{4.37}$$

PU(ωt) is a function having the same basic shape as *pu(ωt)*, but with positive pulses only. Due to the quarter-wave symmetry b_n is zero for even n. A cost function may now be derived in terms of the remaining b_n. The optimisation process is concerned with finding the form of **s** such that the cost function is minimised.

4.4.4 Form of the Cost Function

The cost function described below is given as an example of harmonic minimisation, however it may be used to optimise any attribute, or range of attributes, as seen fit by the designer. In this

application the cost function consists of two elements; the first which determines the amplitude of the fundamental component (b_1) of $pu(\omega t)$, and the second which encourages the algorithm to minimise the amplitudes of a given number of harmonics. The fundamental amplitude control is achieved by assigning a high value to cost function, y, if b_1 is more than 5% in error of the desired amplitude, but assigning no cost if it is within this limit. The second element of the cost function is a value derived from the sum of the amplitude of harmonics which are to be minimised, together with a weighting which favours the largest decreases in the low frequency harmonics. Mathematically this may be written as follows:

$$\left|\left(\frac{b_1 - fund}{fund}\right)\right| \times 100\% \leq 5\%: \qquad COST = \sum_{q=1}^{q\max}\left|\left(\frac{q\max - q + 1}{q\max}\right) \times b_{(q)}\right| \tag{4.38}$$

$$\left|\left(\frac{b_1 - fund}{fund}\right)\right| \times 100\% > 5\% \qquad COST = 10^6 + \sum_{q=1}^{q\max}\left|\left(\frac{q\max - q + 1}{q\max}\right) \times b_{(q)}\right| \tag{4.39}$$

'q' is the qth harmonic to be minimised. 'qmax' is the total number of harmonics to be minimised. $b_{(q)}$ is the amplitude of the qth minimised harmonic, 'fund' is the amplitude of the ideal fundamental component.

Many different cost functions could be devised, the specific application determines the characteristics that are considered to be 'good'. In this case a 'good' output spectrum is one in which the controlled harmonics have very low values. Another cost function might, for example, attempt to minimise Total Harmonic Distortion (THD). It is important that all quantities which are required to be minimised are included in the cost function. Using the cost function given as an example above, it may be found that as the controlled harmonics are minimised, the THD rises. If this rise is unacceptable, a further element must be included in the cost function to control it. This means that in practice the cost function becomes the *only* way in which harmonic spectra may be compared since the user should have confidence that it is the ultimate test of 'goodness' for a particular application. If this confidence is not achievable, the implication is that the cost function needs amending.

4.4.5 Progression of the Search Process

In order to improve the chances of achieving a 'high quality' minimum, Sigma-Delta Modulation ($\Sigma\Delta M$) is used to define the starting point for matrix s. $\Sigma\Delta M$ provides a modulation pattern with a fairly well defined fundamental amplitude, and reasonably small low-frequency harmonics. The Simulated Annealing algorithm proposes amendments to s by sequentially cycling through the elements of s, reversing their sign and re-evaluating the cost function. If the sign reversal improves the cost function the move is accepted, if it causes an increase in cost (i.e. an uphill step) acceptance is dependent on the probability equation (4.35). The equation is evaluated for the current temperature, and compared against a pseudo-randomly generated number which takes values between 0 and 1. If the random number is less than the value of equation (4.35) the uphill step is accepted. Otherwise the element of **s** concerned is returned to its original value.

4.4.6 The Cooling Schedule

The cooling schedule has enormous influence over the quality of the final result. The process of finding a good schedule relies on a great deal of trial and error, intuition, and some insight into the particular application. The first requirement is to set the scaling factor, k_b, in equation (4.35). For example in the tests described below, k_b was set such that the probability of acceptance of a typical uphill step was 0.1 when the temperature was 1. This demands a "feel" for the size of typical function changes (ΔE). After much experimentation the following cooling schedule was adopted:

i. STARTING AT T=0, the temperature is *increased* in steps of 0.1 until 10% of uphill moves are accepted. This is analogous to melting a material in the annealing process.

ii. COOLING: During each cycle, the sign of every element of s is reversed to propose a move, as described in 4.4.5. Between cycles the temperature is reduced by 0.5%. This continues until no improvement in the cost function can be achieved.

iii. STEP (ii) is repeated twice using starting temperatures of 50% and 33% of the original.

By incorporating the 'melting' process, the algorithm finds its own starting temperature, appropriate to the particular problem. The initial figure of accepting 10% of uphill moves was used after it was found that allowing too many uphill moves to be accepted initially dissipated the benefit gained from using $\Sigma\Delta M$ as a starting point.

4.4.7 Practical Applications

In practical systems it is usual that an inverter is required to generate variable magnitude and variable frequency outputs. Consequently the above process would be repeated over a range of different fundamental magnitudes and number of pulses (i.e. frequency). The resulting modulation patterns would then be stored in a look-up table for later use by the inverter. Storage of patterns for Resonant DC Link inverters can be done very efficiently. For example, a pattern having quarter wave symmetry and comprising 100 pulses per quarter cycle may be stored as a 25 digit hexadecimal number. Even where many patterns must be stored, the notation is very compact. During operation the inverter controller simply selects the pattern appropriate for the demanded magnitude and frequency conditions, and converts it to a quarter-wave symmetrical binary sequence.

4.4.8 Results of Tests Using Simulated Annealing

Typical results are shown below to allow comparison to be made between Simulated Annealing, and a search method which never accepts uphill steps. This second method will be referred to as the 'direct search' method. The same cost function was used for each method, and moves were suggested in the same manner. To aid comparison some results are shown in tabular form, and some in graphical form.

Table 4.1 shows cost function values obtained using Simulated Annealing and direct search methods. In every case it can be seen that some improvement in cost function was possible. This was found to be true in all tests, though it cannot be proved mathematically. The 'Number of Controlled Harmonics' refers to the number of odd, non-triplen harmonics which the cost function

attempted to minimise. Additionally the fundamental was controlled to within 5% of a given nominal value. The fourth column of the table shows the initial value of cost function obtained after applying Sigma Delta Modulation. This indicates how the final cost function value compares to the starting value in each case.

TEST	Nominal Fund-amental	No. of Controlled Harmonics	Initial Cost Function Value (SIGMA DELTA MODULATION)	Final Cost Function Value (DIRECT SEARCH)	Final Cost Function Value (SIMULATED ANNEALING)	% Improvement In Cost Function
1	0.8	9	0.078796	0.0400	0.0378	5.50
2	0.55	14	0.129647	0.0832	0.07946	4.50
3	0.55	4	0.041216	0.0289	0.0047	83.7
4	0.2	12	$>10^6$	0.1212	0.0379	68.7
5	1.0	14	0.128366	0.1284	0.110	14.3
6	0.65	19	0.18822	0.1364	0.126	7.62
7	0.35	12	0.052944	0.0529	0.0409	22.7
8	1.15	11	$>10^6$	0.1304	0.077	41.0

Table 4.1 Comparison of Search Methods

Figures 4.12(A) and 4.12(B) show, respectively, the theoretical harmonic spectra for a clamped Resonant DC Link Inverter using switching strategies derived by the Simulated Annealing technique, and Direct Search technique. These were obtained by evaluating equation (4.36). The nominal fundamental is 0.2. Nine harmonics were minimised. It can be seen that it is possible to reduce the amplitude of the harmonics to very low values. Typically harmonics can be reduced to less than 2.5% of the fundamental amplitude. Triplen voltage harmonics do not cause currents to flow in three-phase loads without a neutral line, consequently no attempt was made to minimise them. Odd triplens are marked on the spectra with a 'T'. The harmonic labelled 'F' denotes the first un-minimised non-triplen harmonic. Figure 4.13 demonstrates how a band of harmonics, remote from the fundamental, may be minimised. In this test 7 harmonics were minimised starting

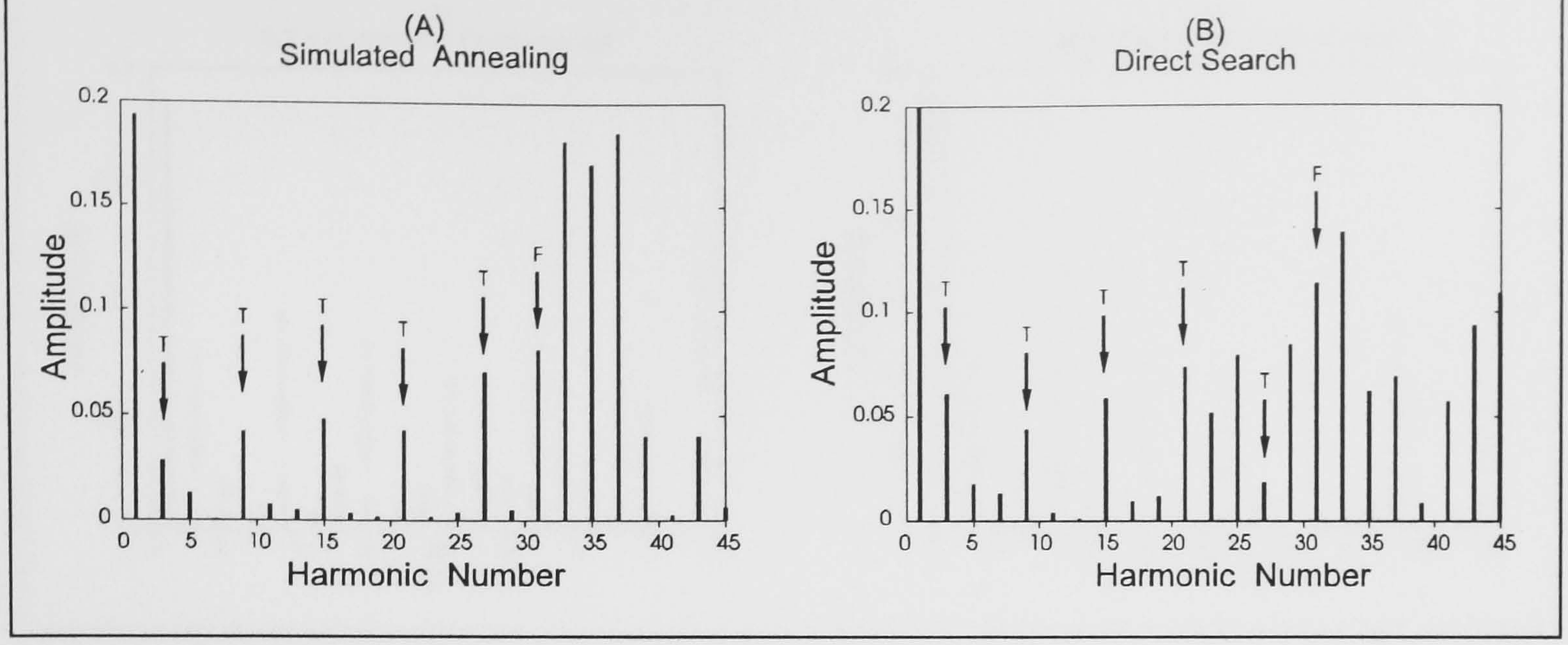

Figure 4.12 Comparison of Simulated Annealing and Direct Search Methods

with the 13th. The nominal fundamental value is 0.55. Figure 4.14 shows the spectra obtained by computer simulated Sigma-Delta Modulation, which is used as the starting point for the simulated annealing process. Figure 4.14(A) was obtained using the same conditions used for Figure 4.12, and Figure 4.14(B) was obtained using the same conditions as Figure 4.13. It can be seen that although ΣΔM produces low values of harmonics, control of individual harmonics is not possible.

Although the Simulated Annealing algorithm relies on a random number generator for its operation, the results shown above are repeatable if the system is cooled slowly enough. The test results were calculated on a desktop PC, taking around 15 to 20 minutes per run. It is not possible to say how close the final results are to the global minimum, although comparisons can

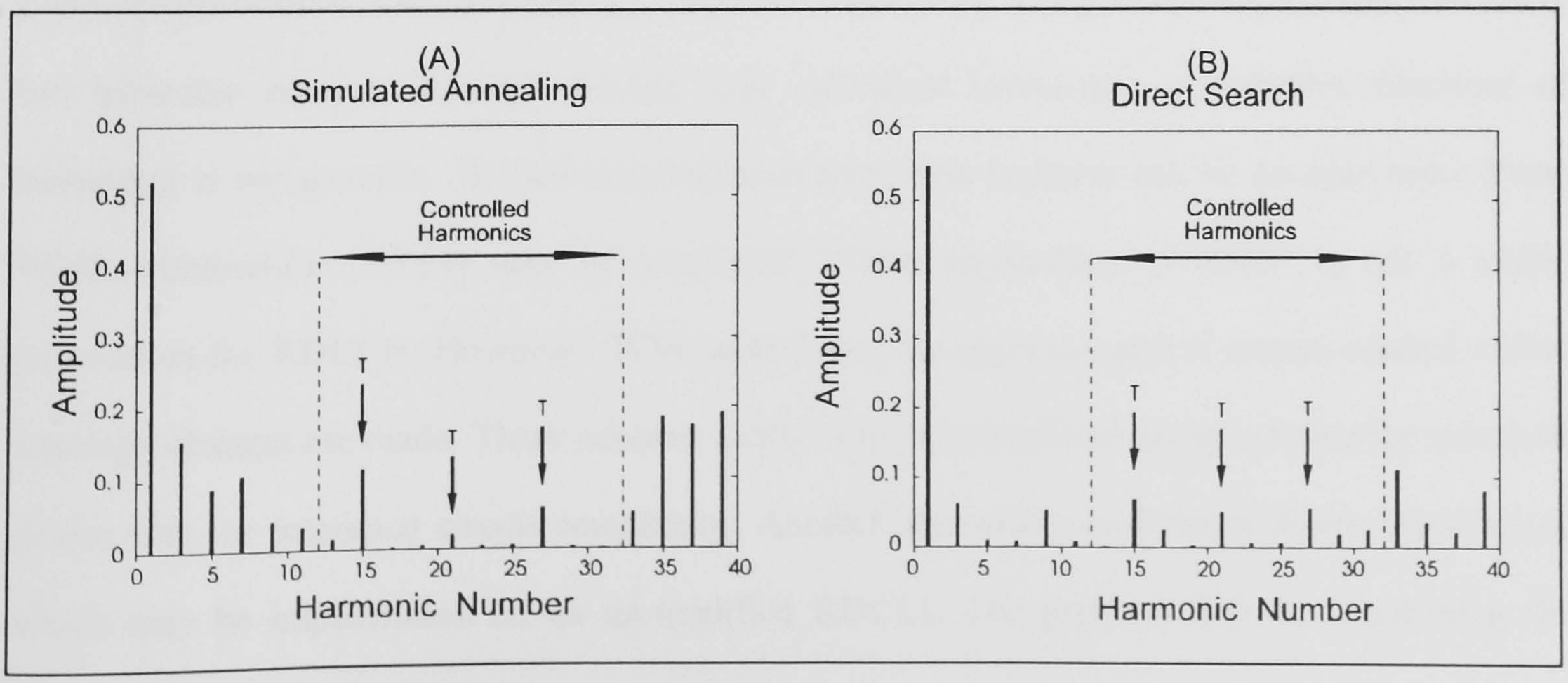

Figure 4.13 Comparison of Simulated Annealing and Direct Search Methods

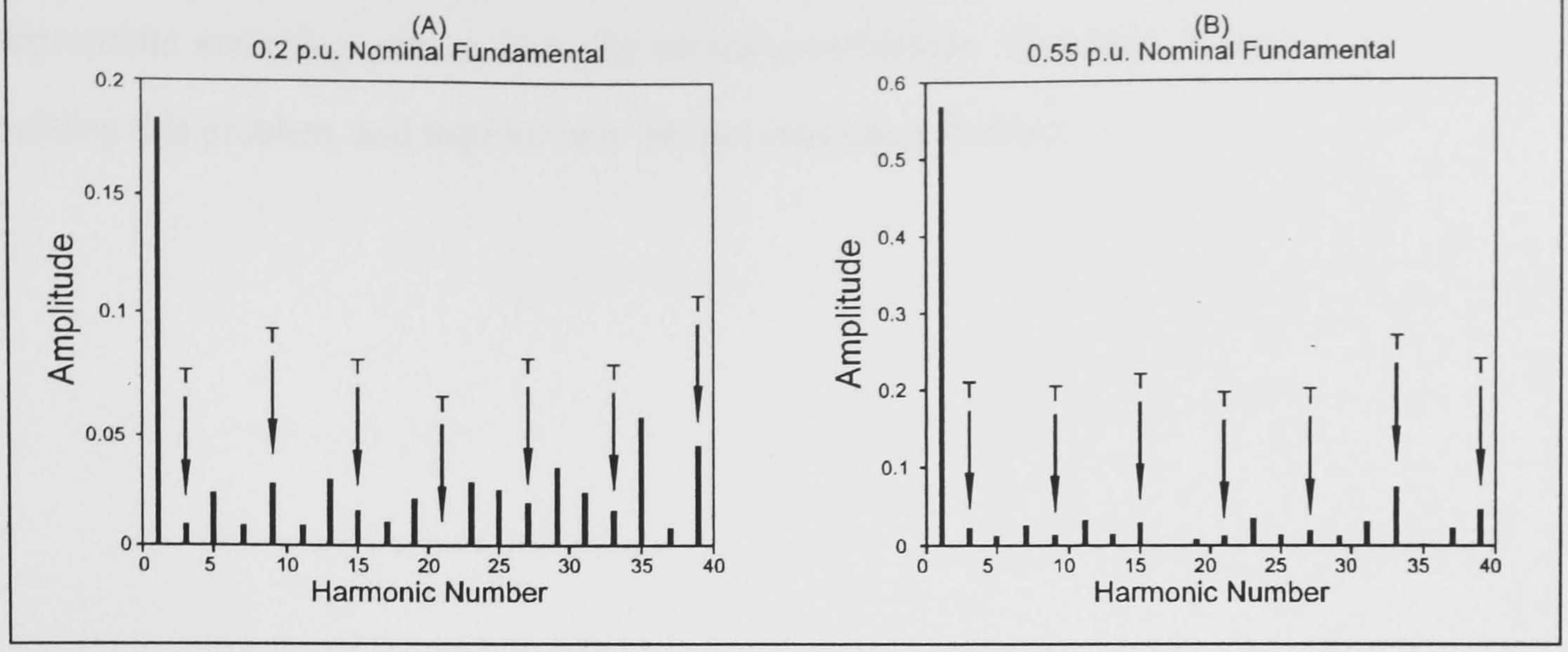

Figure 4.14 Spectra Due to Sigma Delta Modulation

be made against optimisation techniques which only accept downhill steps. These show that Simulated Annealing offers an *improvement* in the minimum which can be obtained. The magnitude of this improvement depends on how good a minimum was found in the first instance. The Cost Function suggested in the work described above is one suitable for approximating harmonic elimination. However many other cost functions could be derived to optimise different parameters.

4.5 Chapter Summary

Delta Modulators are frequently used in conjunction with Resonant Converters since they may be synchronised with the resonant link, are simple to implement, and generate waveforms with fairly low harmonic content. However control over individual harmonics, or complex functions of harmonics is not possible. In hard-switched converters this problem can be avoided since Pulse Width Modulation (PWM) may be employed. Direct application of PWM is not a viable proposition for RDCLIs. However PWM control may be approximated if certain control and/or topology changes are made. These schemes suffer from several disadvantages including increased device loss, or increased circuit complexity. Another alternative is Discrete Pulse Modulation, which may be implemented on an un-modified RDCLI. The problem here is in selecting the

appropriate switching pattern from the myriad possibilities. Simulated Annealing is a way of tackling this problem, and requires only modest computing facilities.

Chapter 5

Implementation of a Laboratory Test Rig

5.1 Introduction

A low power test-rig was constructed, primarily to allow investigation and verification of the modulation process being proposed for the Resonant DC Link Inverter. The converter had a rating of approximately 3kVA, which was selected as a compromise between cost and the desire to operate at power levels which are typical for applications of the RDCLI. This chapter begins with a review of the control requirements of the resonant circuit, followed by a description of the implementation of a micro-processor controller. The performance of a pre-programmed modulation strategy is compared against the theoretical results, this includes a test of the effect which loading the converter has on the efficacy of the modulation process. Finally the design of the major system components is summarised .

5.2 Control Methodology

5.2.1 Basic Control Requirements

The first stage of the test-rig was based on the circuit shown in Figure 3.1. As given by equation (3.14), the condition for the clamp switch (T_c) to be turned off is when the resonant inductor current has the value:

$$I_L = I_x - \frac{V_{DC}}{Z_0}\sqrt{k(2-k)} \qquad (5.1)$$

This ensures that the voltage on C_r reaches zero during the following resonant cycle. Using this equation, the key measurement parameters for control of the resonant circuit can be identified:

- A measurement of I_X to allow evaluation of (5.1)

- A measurement of the current in the resonant inductor to indicate when equation (5.1) has been satisfied.
- An indication that current has begun flowing through the clamp diode, D_C. This is necessary so that T_r may be turned on in anticipation of the subsequent reversal of current which takes place.
- A detector to announce that the resonant voltage has reached zero. This identifies for the controller, the point at which the switches of the output stage may change state.

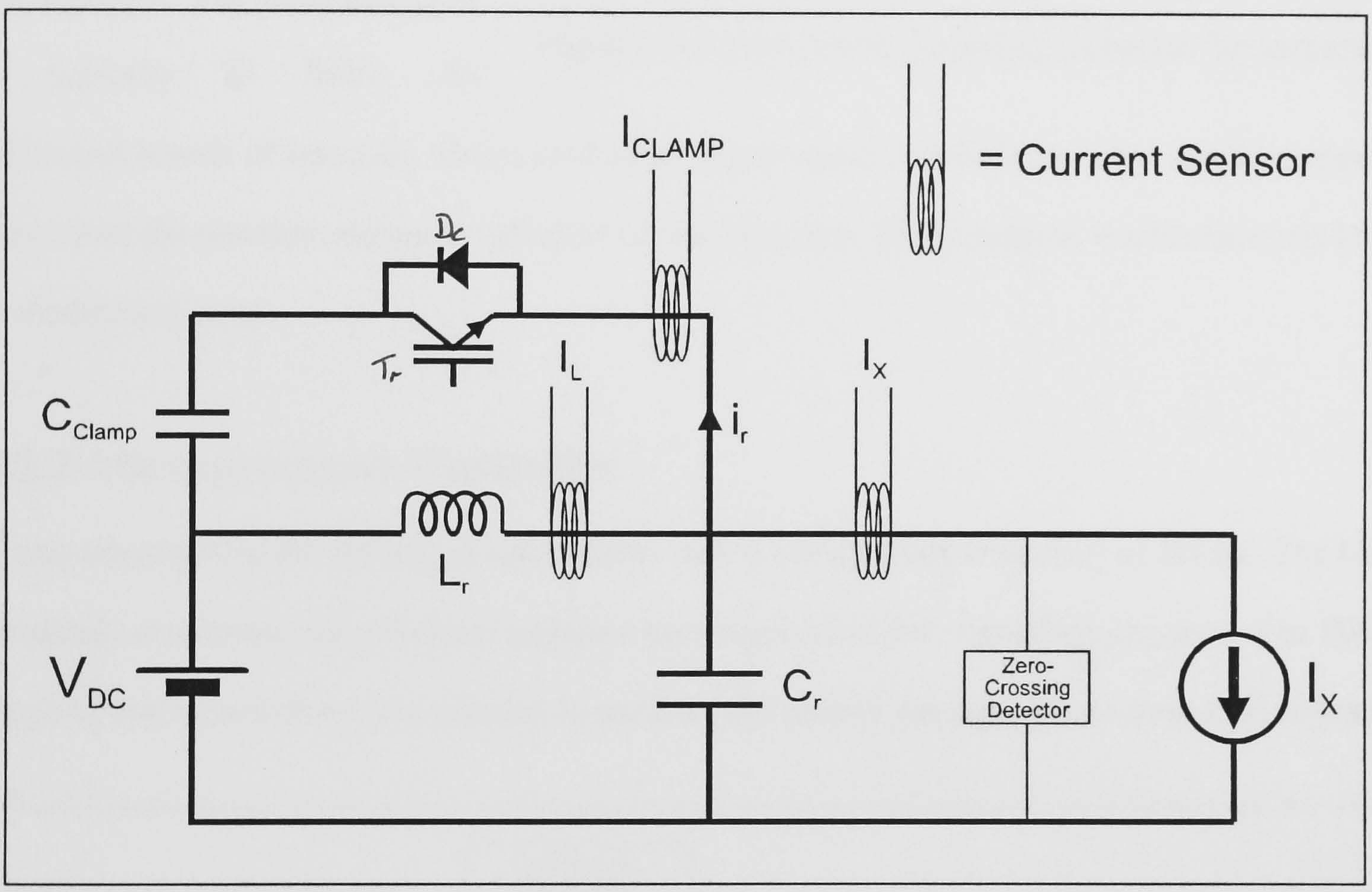

Figure 5.1 Position of Measurement Devices

The values of L_r, C_r, k, and V_{DC} may be considered to be constant and as such are entered into the control system over a serial PC link, by the user. Figure 5.1 shows the resonant components and the positions of the transducers necessary to take the readings described above. The current transducers are of the Hall effect type, having a bandwidth of 100kHz, and range of 50A. The zero-crossing detector requires careful design. Its sense terminals are connected to a high voltage, rapidly changing source. If potential dividing resistors are used, they require a high power dissipation capability, yet low inductance to prevent phase shifts from being introduced into the measurements. Consequently many wirewound varieties are unsuitable. The circuit diagram of

the detector is shown in Figure 5.2. A 'threshold adjustment' is provided to set the voltage level at which the detector indicates 'zero' volts. This allows early triggering in order that the microprocessor can prepare to change the state of the switches. The threshold level is typically 25 Volts. An additional benefit of detection 'above zero' is an improvement in reliability, since rapid transients may cause the resonant voltage to fall short of reaching zero. This condition would otherwise lead to modulation error.

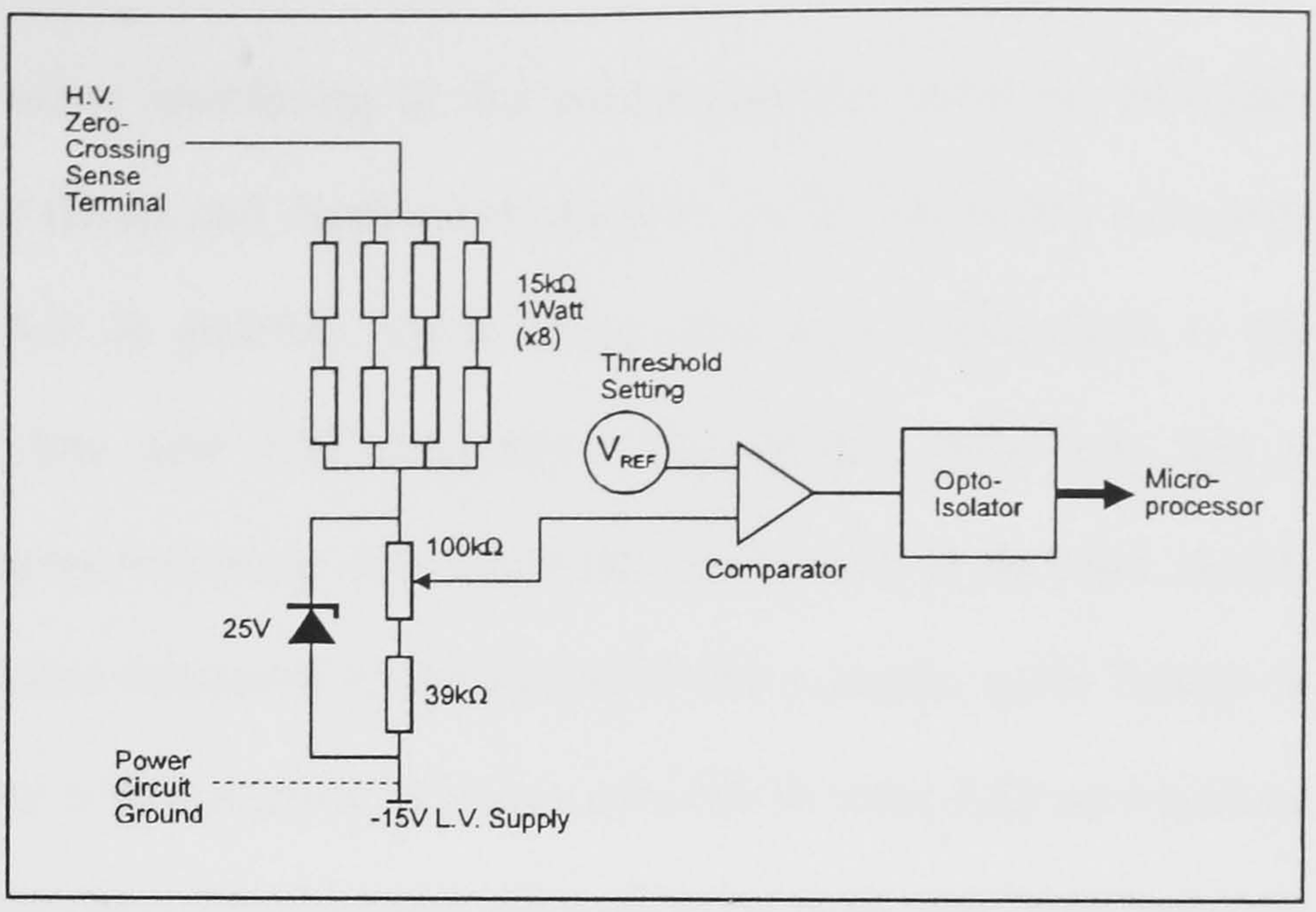

Figure 5.2 Zero Volts Crossing Detector Schematic

5.2.2 Microprocessor Controller

It was intended that the test-rig should operate with a nominal link frequency of 20kHz. The link frequency determines the minimum response time required of the controlling circuitry. The 8051 range of microcontrollers was selected to perform the control function due to their low cost and

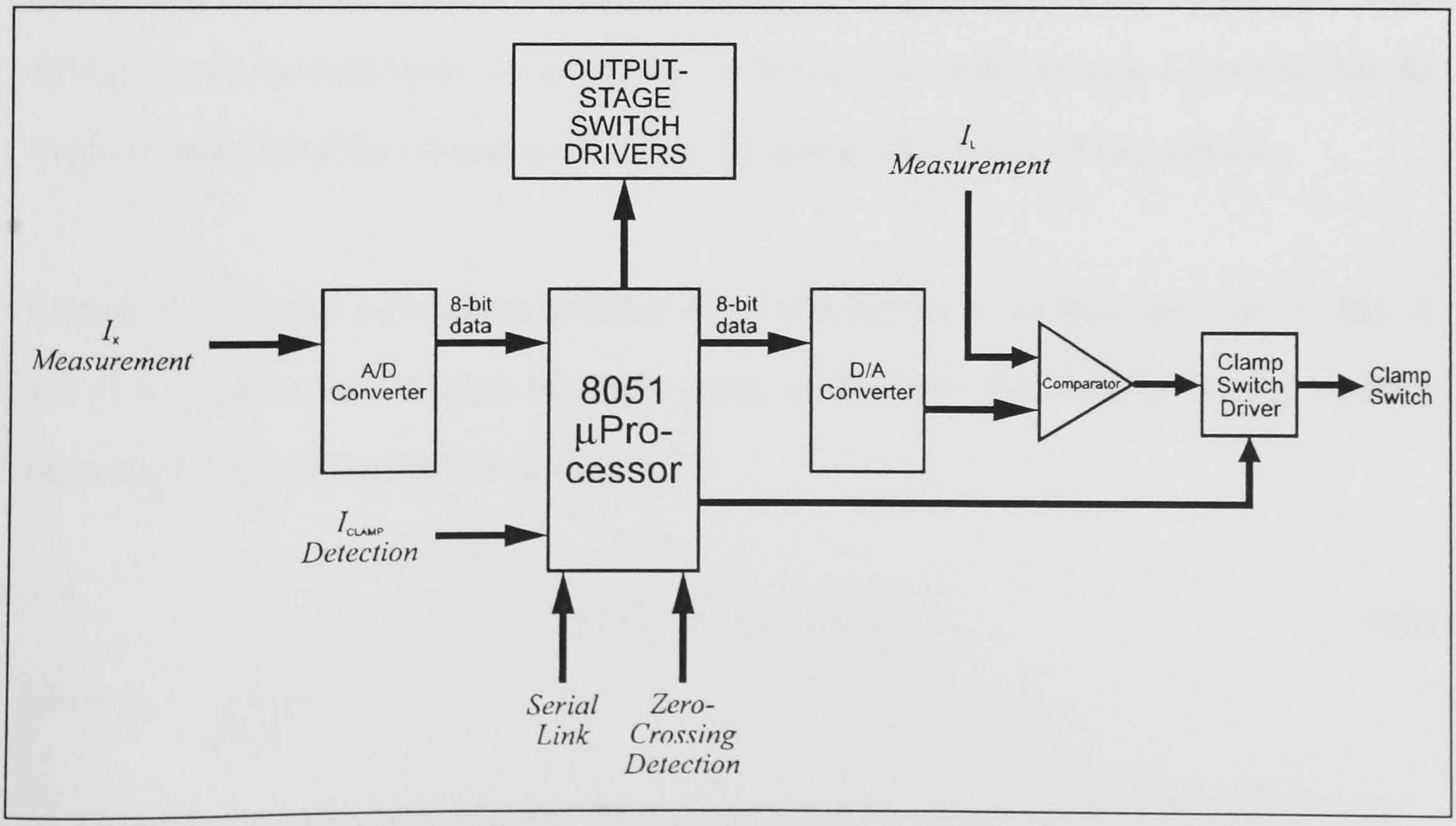

Figure 5.3 Basic Microprocessor Functions

reasonable cycle time of 1μs. To allow interfacing of the microcontroller with the analogue resonant circuit, Digital-to-Analogue (D/A) and Analogue-to-Digital (A/D) converters are used, as shown schematically in Figure 5.3. A problem which exists with this arrangement is the relatively long conversion time of low cost A/D converters. The ZN439 used here has a conversion time of 5μs which compares extremely well with other converters in its price range. However, 5μs is an extremely long time compared to the period of the resonant cycle (which is 50μs in the case of a 20kHz link). As a consequence, it is not possible to treat A/D conversions as 'real-time' readings. To circumvent this difficulty, the value of I_X is read only once into the microprocessor by an A/D converter (I_X does not change appreciably during one resonant cycle). This enables equation 5.1 to be evaluated giving the 'turn-off condition' for I_L. This value is loaded into a D/A converter which allows comparison against the actual value of inductor current in analogue form using a comparator IC. Thus the response to the turn-off condition being met is almost instantaneous.

5.2.3 Microcontroller Program

The 8051 microcontroller has a 1μs cycle time, with instructions taking 1,2, or 4μs to be completed, depending on their complexity. Compared to the resonant period of 50μs, these computation times are significant and require careful distribution of the computation tasks throughout the resonant cycle. To aid the design process it is useful to write expressions for the length of each part of the resonant cycle, given the values of L_r and C_r, as shown below:

Consider the resonant pulse shown in Figure 4.9, which represents the ideal case, where Mode A and C are symmetrical. Assume the pulse starts at time t=0. The equation for the resonant capacitor voltage during Mode A is given by;

$$V_C = V_{DC} - V_{DC}\cos(\varepsilon_0 t) \tag{5.2}$$

where $\varepsilon_0 = \dfrac{1}{\sqrt{L_r C_r}}$

At the point where the clamp engages, the resonant capacitor voltage has the value kV_{DC}. Thus;

$$kV_{DC} = V_{DC}\left(1-\cos\left(\varepsilon_0 t\right)\right) \tag{5.3}$$

therefore;

$$t = \frac{1}{\varepsilon_0}\cos^{-1}\left(1-k\right) \tag{5.4}$$

The length of Mode C is similarly found to be given by equation (5.4). The current in the inductor during Mode A may be described by:

$$i_L = \sqrt{\frac{C_r}{L_r}}.V_{DC}\sin\left(\varepsilon_0 t\right) + I_X \tag{5.5}$$

At the end of Mode A, where the time is given by equation (5.4);

$$i_L = \sqrt{\frac{C_r}{L_r}}.V_{DC}\sin\varepsilon_0\left(\frac{1}{\varepsilon_0}.\cos^{-1}\left(1-k\right)\right) + I_X \tag{5.6}$$

Rearranging using the identity $\sin\varepsilon_0 t = \sqrt{1-\cos^2\left(\varepsilon_0 t\right)}$ yields;

$$i_L = \sqrt{\frac{C_r}{L_r}}.V_{DC}\sqrt{1-\cos^2\left(\cos^{-1}\left(1-k\right)\right)} + I_X \tag{5.7}$$

therefore,

$$i_L = \frac{V_{DC}}{Z_0}\sqrt{k\left(2-k\right)} + I_X \tag{5.8}$$

where $Z_0 = \sqrt{\frac{L_r}{C_r}}$.

This identifies the inductor current at the start of Mode B. Let the resonant component of this current during Mode B be given by I_B, thus:

$$I_B = \frac{V_{DC}}{Z_0}\sqrt{k\left(2-k\right)} \tag{5.9}$$

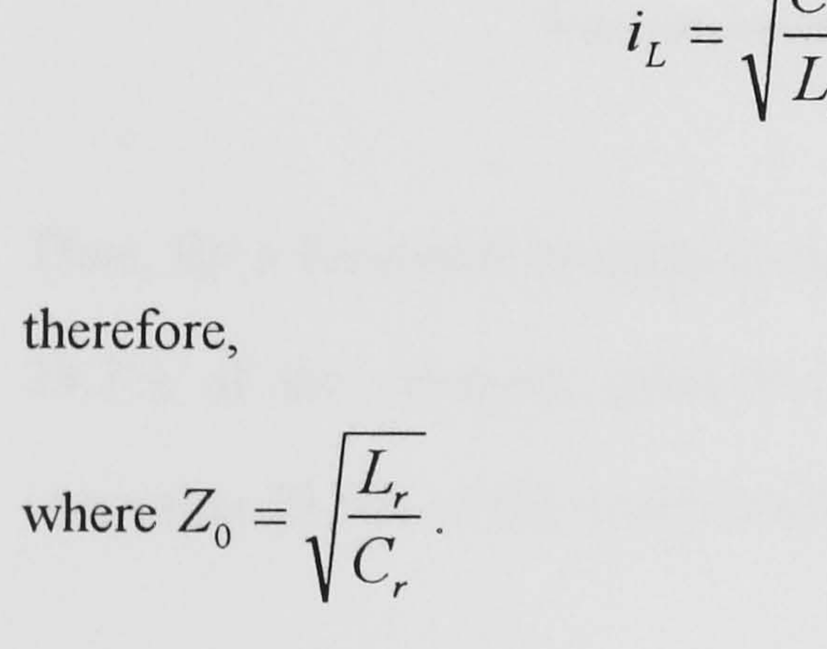

Figure 5.4 Current in L_r

During Mode B the current in I_L changes linearly as shown in Figure 5.4, under the influence of the clamp capacitor. In the ideal system, charge balance would be maintained on the clamp capacitor due to the absence of losses. Thus before

the clamp switch is opened, the resonant component of current would be allowed to reverse direction, and increase until its magnitude was equal and opposite to the initial value. (i.e. all the charge added during clamping would subsequently be removed). As a consequence, the current in L_r changes from I_B+I_X to $-I_B+I_X$. The following expression may therefore be written, having the general form $V = L\frac{di}{dt}$:

$$V_{DC}(k-1) = L_r.\frac{2I_B}{t_b} = L_r\frac{2V_{DC}\sqrt{k(2-k)}}{Z_0 t_b} \tag{5.10}$$

which gives;

$$t_b = \frac{2\sqrt{L_r C_r}\sqrt{k(2-k)}}{(k-1)} \tag{5.11}$$

Combining (5.4) and (5.11) gives an expression for the length of the ideal resonant pulse:

$$t_{pulse} = 2\sqrt{L_r C_r}\left[\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{(k-1)}\right] \tag{5.12}$$

Thus, for a Resonant Inverter having a clamping coefficient of 1.4, Modes A and C each occupy 23.2% of the resonant cycle (11.6μs in a 20kHz link system), and Mode B occupies the remaining 53.6% of the cycle (26.8μs in a 20kHz link system).

Figure 5.5 shows the overall flow of the controlling program. The diagram is fairly self-explanatory, but the following notes are provided to aid understanding:

- An interrupt timer is provided. This continually counts down from a preset value. If it reaches zero (which takes 200μs) the power circuit is shut down. During normal operation the timer is reset each time a zero-voltage crossing is detected. Thus, if the link oscillations cease for any reason, the circuit automatically turns off within 200μs as a safety precaution.
- The 'turn-off condition' entered by the user is the evaluation of the following expression:

$$\frac{V_{DC}}{Z_0}\sqrt{k(2-k)} \tag{5.13}$$

which forms part of equation (5.1). This is transmitted to the 8051 microcontroller via a serial communications link before the resonant circuit is started.

- The output of the comparator which controls the clamp switch is passed through a gate, which enables the microprocessor to determine the periods of time during which the comparator is able to turn on the switch. This is because conditions exist during Modes A and C which would otherwise cause the comparator to (erroneously) turn on the clamp switch. Thus it is only enabled during Mode B.

5.2.4 Implementation of the Clamp Circuit

The clamp is shown in Figure 5.1 simply as a capacitor. In fact, it has a floating DC power supply in parallel with it, which maintains the clamp voltage. This allows a precise and easily variable value of clamp voltage in the experimental environment but in practice it may be prohibitively expensive. The DC supply could be replaced by a simple 'charge pump' circuit which maintains charge balance on the clamp capacitor. Another alternative is to briefly turn on two switches in one leg of the inverter stage during the zero voltage periods of the resonant link. This causes the current in the resonant inductor to increase, which stores energy that is 'dumped' into the clamp capacitor when the clamp engages. Disadvantages of this scheme are that it increases slightly, the switching losses of the inverter devices, distorts the link waveform, and requires fast switches if accurate control is to be achieved.

The 'bus shorting' scheme was tried experimentally. Normally the DC supply to the clamp draws around 300mA when the inverter is on no load. By implementing bus shorting, the current could be satisfactorily reduced to almost zero. However, if the shorting periods are excessive then the clamp voltage rises and the conditions for oscillation can no longer be met. Maintaining charge balance on the clamp capacitor was found to be difficult since the bus shorting mechanism was controlled by the 8051 microcontroller which quantises the shorting periods at 1μs due to its cycle time. As a consequence the control was fairly imprecise. This situation could be resolved by

using a faster microprocessor, for example one of the Analog Devices 210x family of Digital Signal Processors.

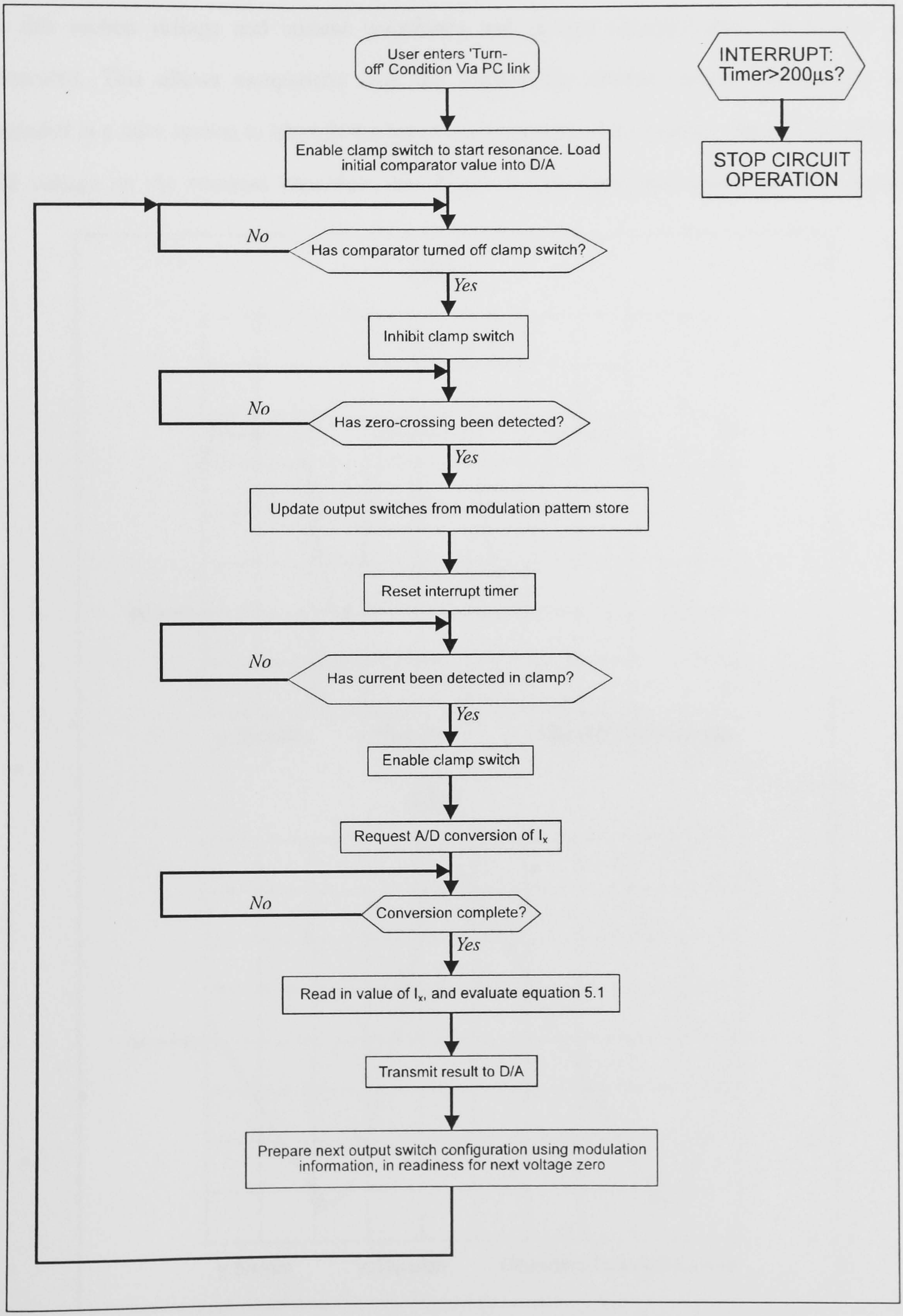

Figure 5.5 Flow Diagram of the Core of the RDCLI 8051 Microcontroller Program

5.3 Practical Results

5.3.1 RDCLI Waveforms

In this section voltage and current waveforms and spectra obtained from the test-rig are presented. This allows comparison with the theoretically derived values. Photographs are included in a later section to identify the various components of the system. Figure 5.6(a) shows the voltage on the resonant capacitor, and Figure 5.6(b) shows the current in the resonant

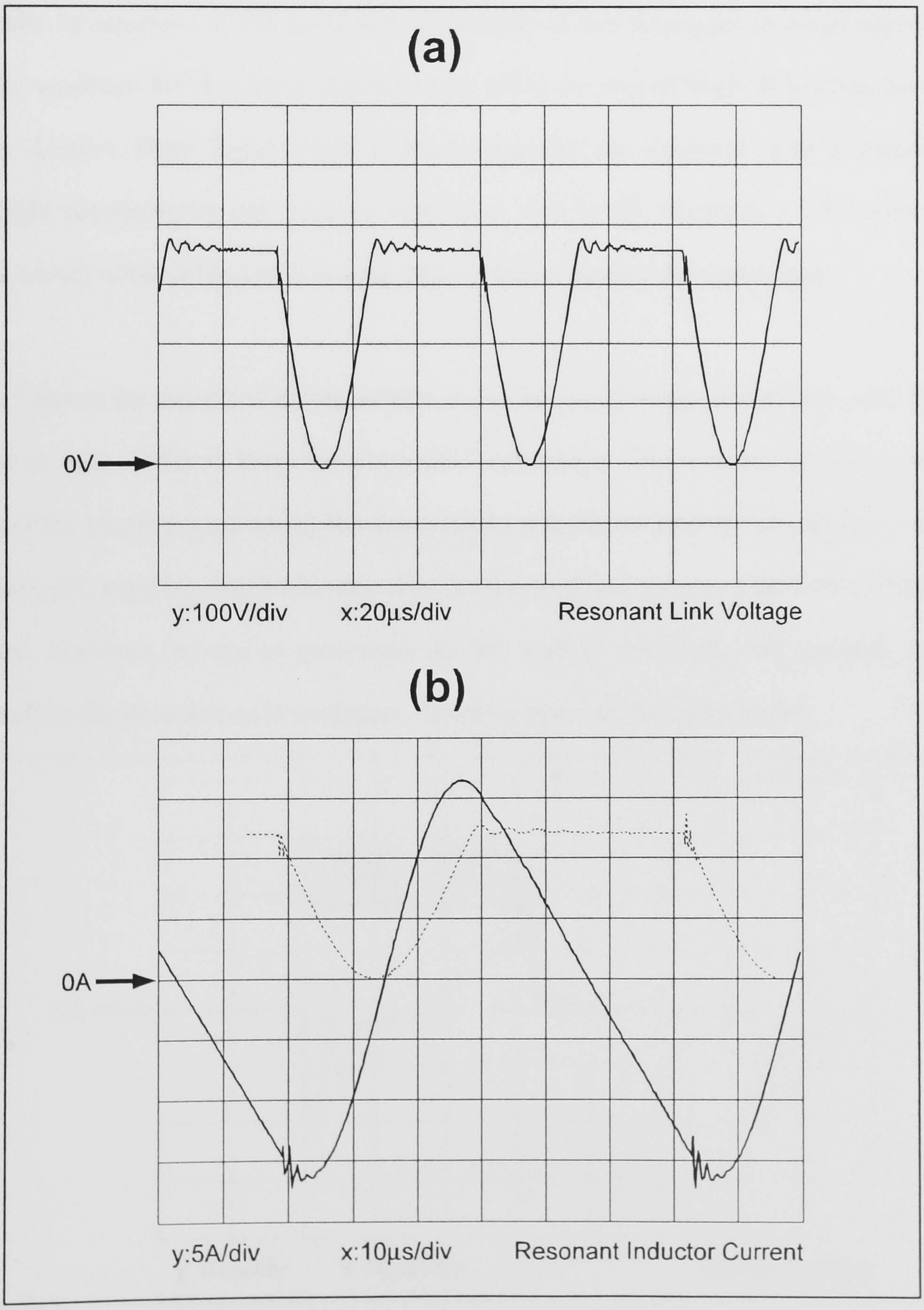

Figure 5.6 Waveforms of Link Voltage, and Inductor Current

inductor with the corresponding link voltage waveform indicated with a dotted line. These images were captured with the inverter on no load, and with the following conditions: V_{DC}=248V, k=1.42, C_r=0.56μF, L_r=102μH.

Using the measured values of k, C_r and L_r, and equation (5.4), the theoretical value for the length of Modes A and B, as defined in Figure (4.9) is 15.2μs. Modes A and B were measured practically, as shown in Figure 5.6(a), and found to be approximately 15μs. Mode B is given theoretically by equation (5.11) as 32.4μs. Practically it was measured as being approximately 32μs. The condition for the clamp switch to turn off at the end of Mode B is given by equation (3.14) as -16.65A. From Figure 5.6(b) it can be seen that the measured value is approximately -15A. Slight discrepancies can occur in this value, due to the 'threshold' of the zero crossing detection circuit which allows resonant operation without 'perfect' zero crossings.

Figure 5.7 shows the measured clamp current. It can be seen that the current flow onto the clamp capacitor is very different from the theoretical waveshape. The 'ringing' of this current is a function of the circuit layout which has introduced a significant quantity of parasitic inductance. The floating DC supplies which maintain the clamp voltage are a major contributory factor to the inductance. However, as can be seen from the link voltage waveform, this parasitic resonance does not affect the overall circuit operation, though it may lead to higher losses.

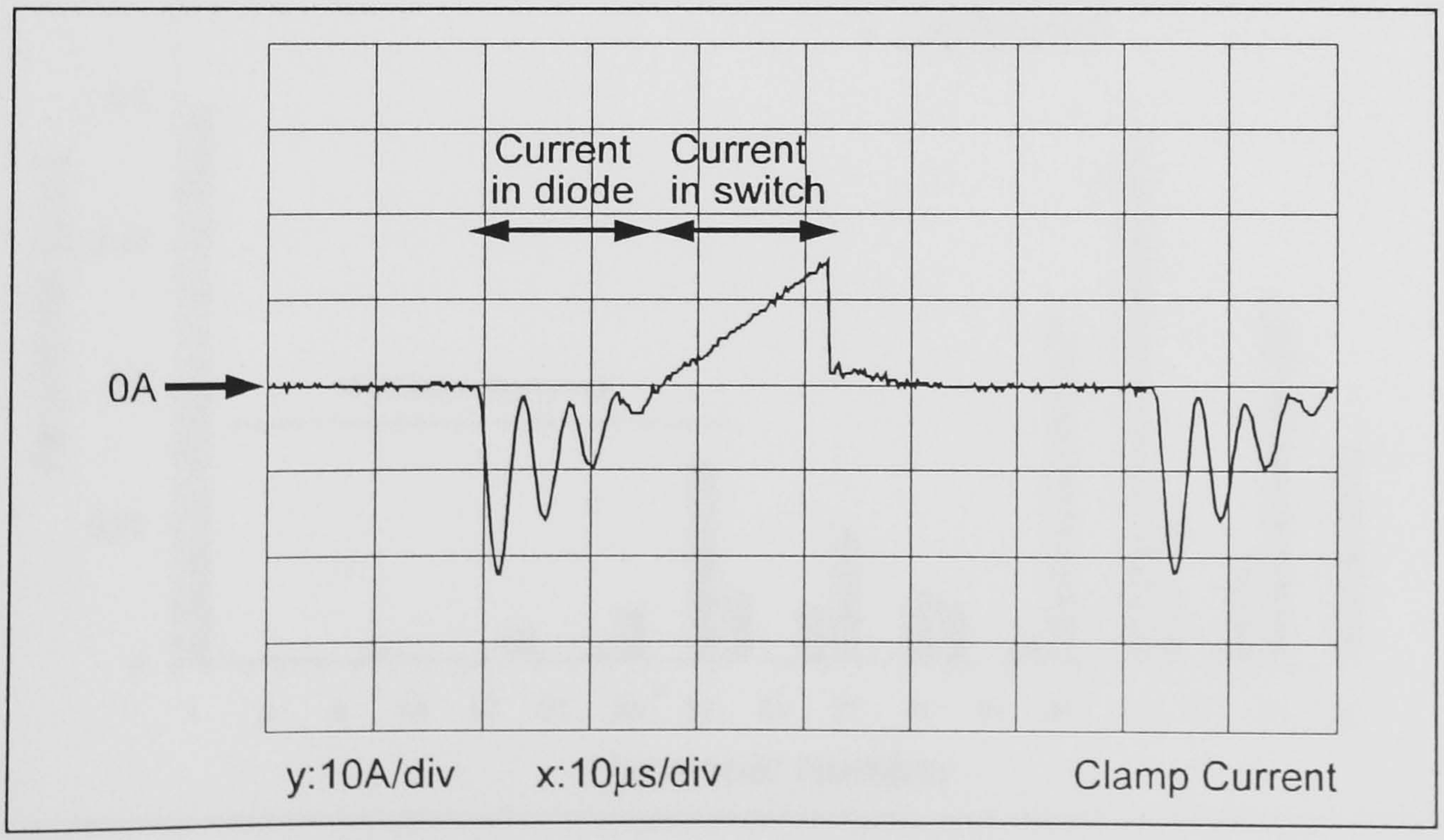

Figure 5.7 Clamp Circuit Current

To allow a complete comparison between the theoretical and practical waveforms, tests were carried out with the inverter driving a static inductive load. The load consisted of a 3-phase, fan cooled, resistive load bank which was impedance-matched using a step-up transformer. Air cored inductors were included to increase the load inductance. Because the inverter does not have the facility to 'ramp-up' its output, it was found that the sudden application of voltage to the matching transformer caused magnetic bias. This bias led to excessive currents, preventing correct operation of the inverter. This problem was cured by supplying the load via a 3-phase variable autotransformer, allowing a 'manual' voltage ramp-up. In practical implementations this problem could be avoided by providing sufficient pre-programmed patterns to allow the output voltage to be stepped up gradually. The parameters of the load were measured for use in the simulation, and are presented below:

R_s: 0.7Ω	L_m: 0.63H
L_s: 0.025mH	L_r: 0.00916mH
R_r: 5.1Ω, or 3.4Ω depending on the load bank setting.	

Figure 5.8 shows the harmonic spectra of the phase voltage for the first load test. This will be referred to as modulation pattern 1. This pattern which was generated using Simulated Annealing,

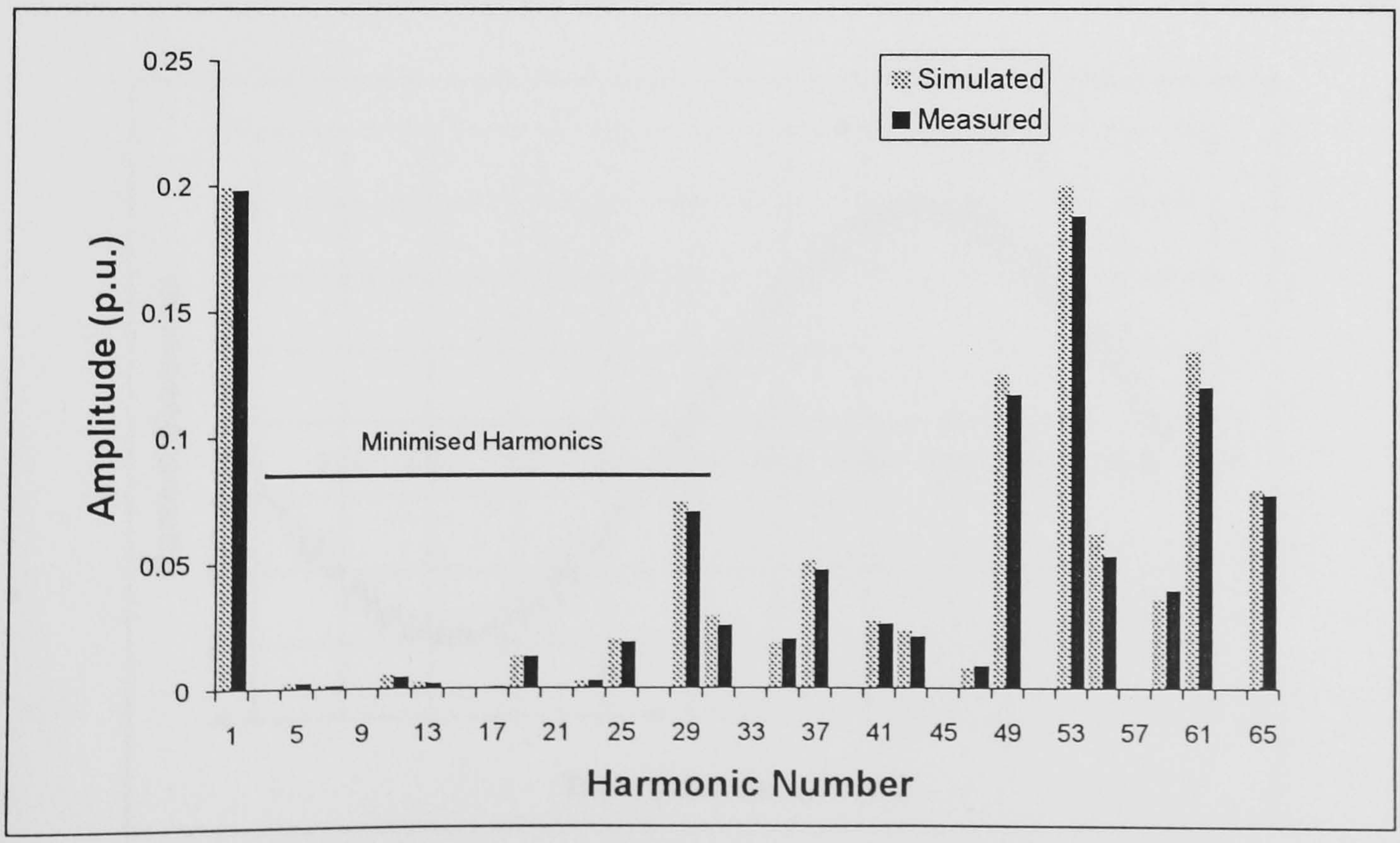

Figure 5.8 Simulated and Measured Spectra for Pattern 1 Phase Voltage

minimises 9 harmonics as indicated in the figure, and produces a fundamental of nominal magnitude 0.2p.u. Note that these conditions are the same as those used for the example spectrum shown in Figure 4.12(a), however there are some differences in individual amplitudes as a slightly different cooling schedule was used in the Simulated Annealing process. It can be seen from Figure 5.8 that close agreement is obtained between the measured and simulated values. Figure 5.9 shows the current waveform which is obtained when this voltage waveform is applied to the load described above.

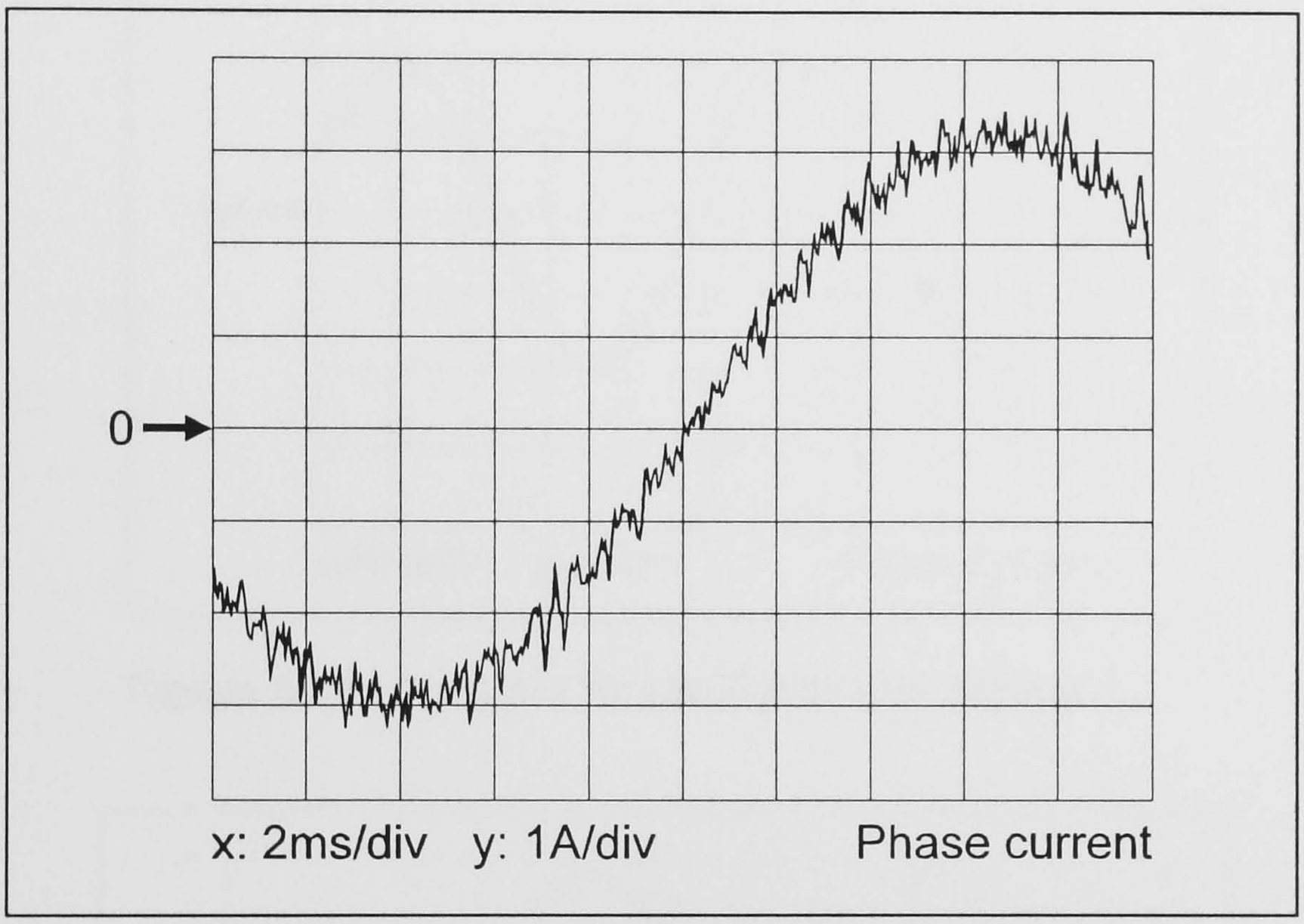

Figure 5.9 Measured Phase Current Waveform

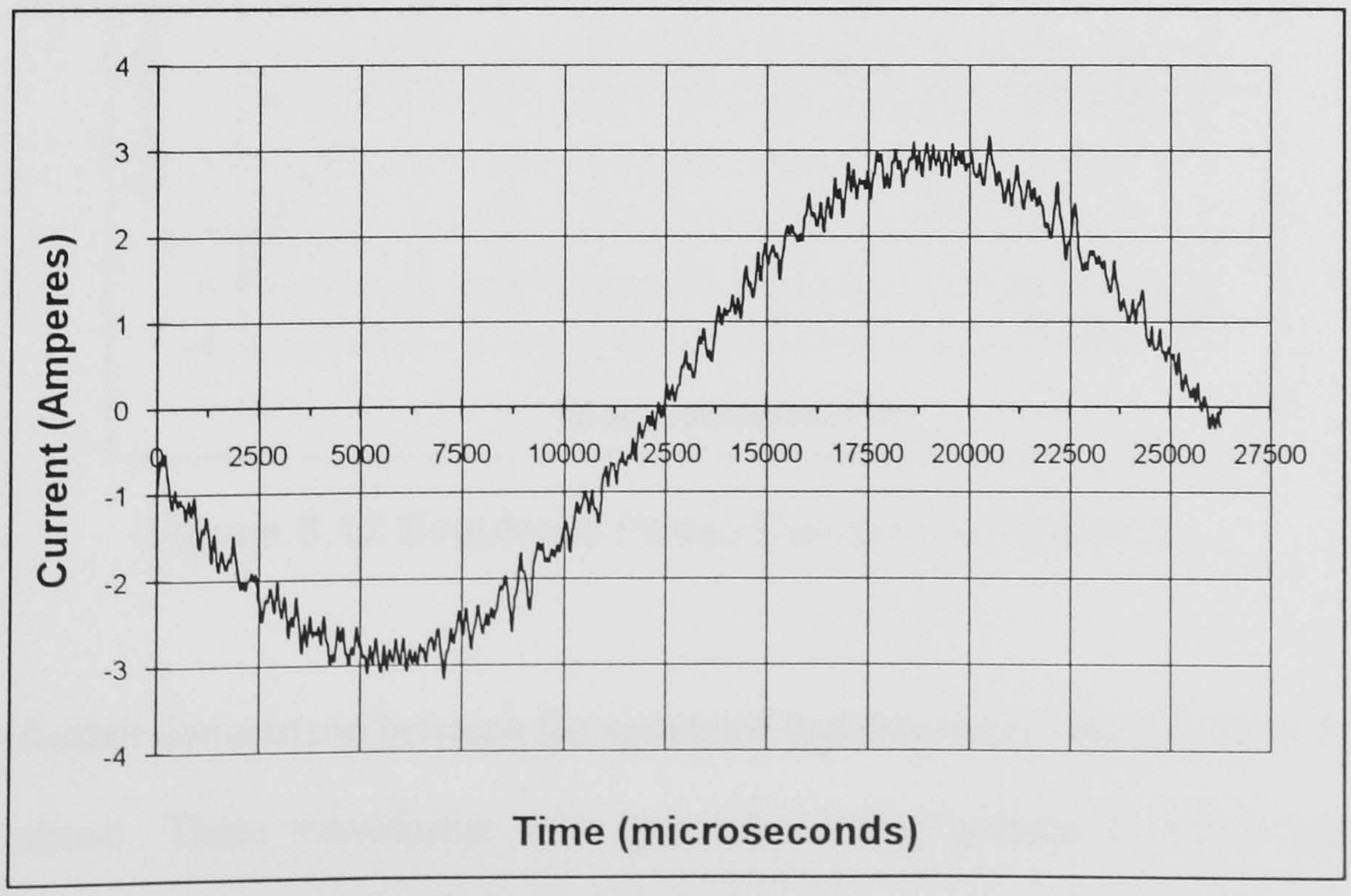

Figure 5.10 Simulated Phase Current for Pattern1

Figure 5.10 shows the current waveform which was obtained by the method of simulation described in Chapter 3. It can be seen that the waveforms are very much alike. Some of the 'spikes' on the practically measured waveform are slightly higher than in the case of the simulated waveform. This is probably due to capacitively coupled currents, for example in the transformer windings, which are not taken into account by the simulation.

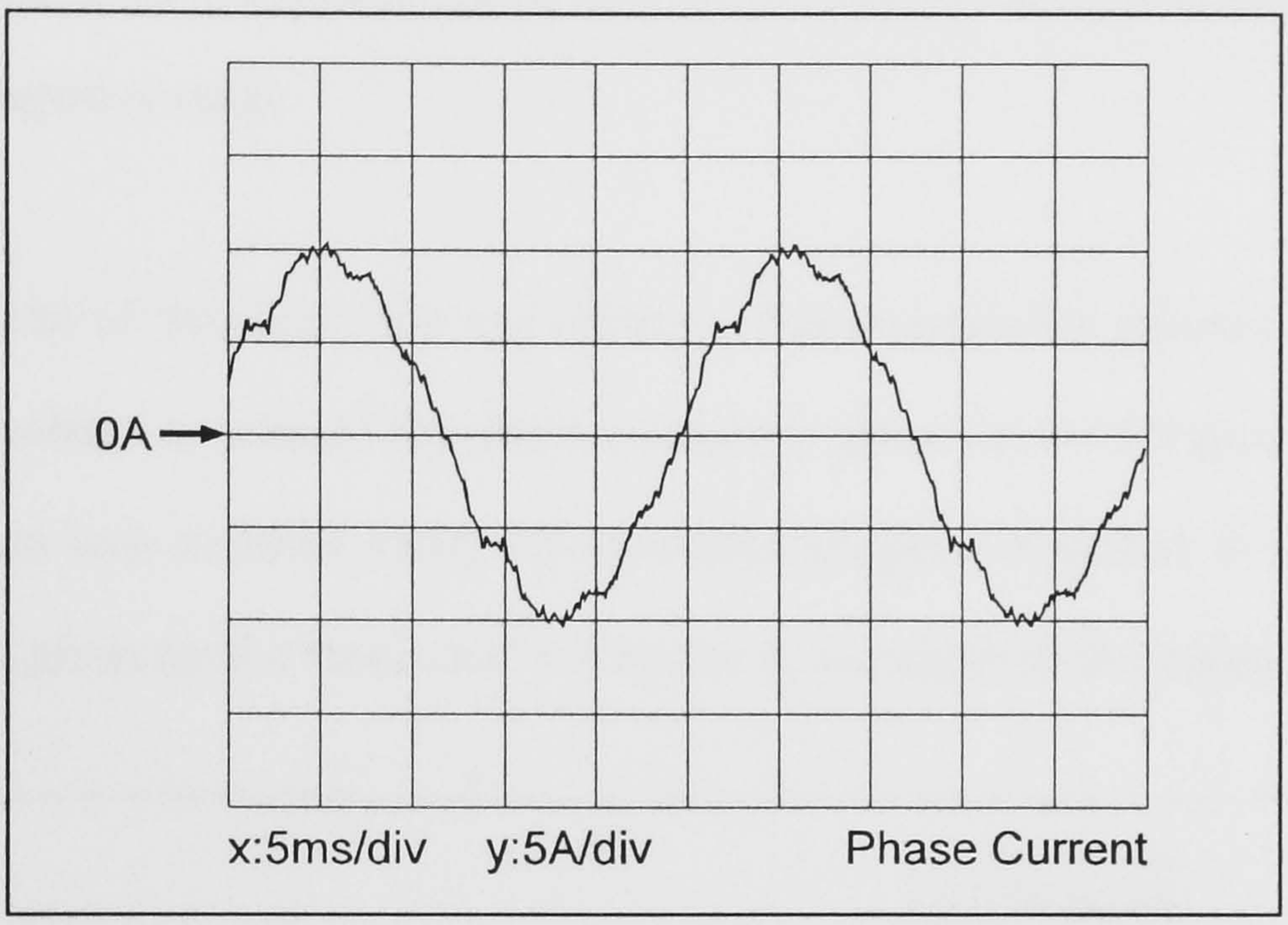

Figure 5.11 Measured Phase Current for Pattern 2

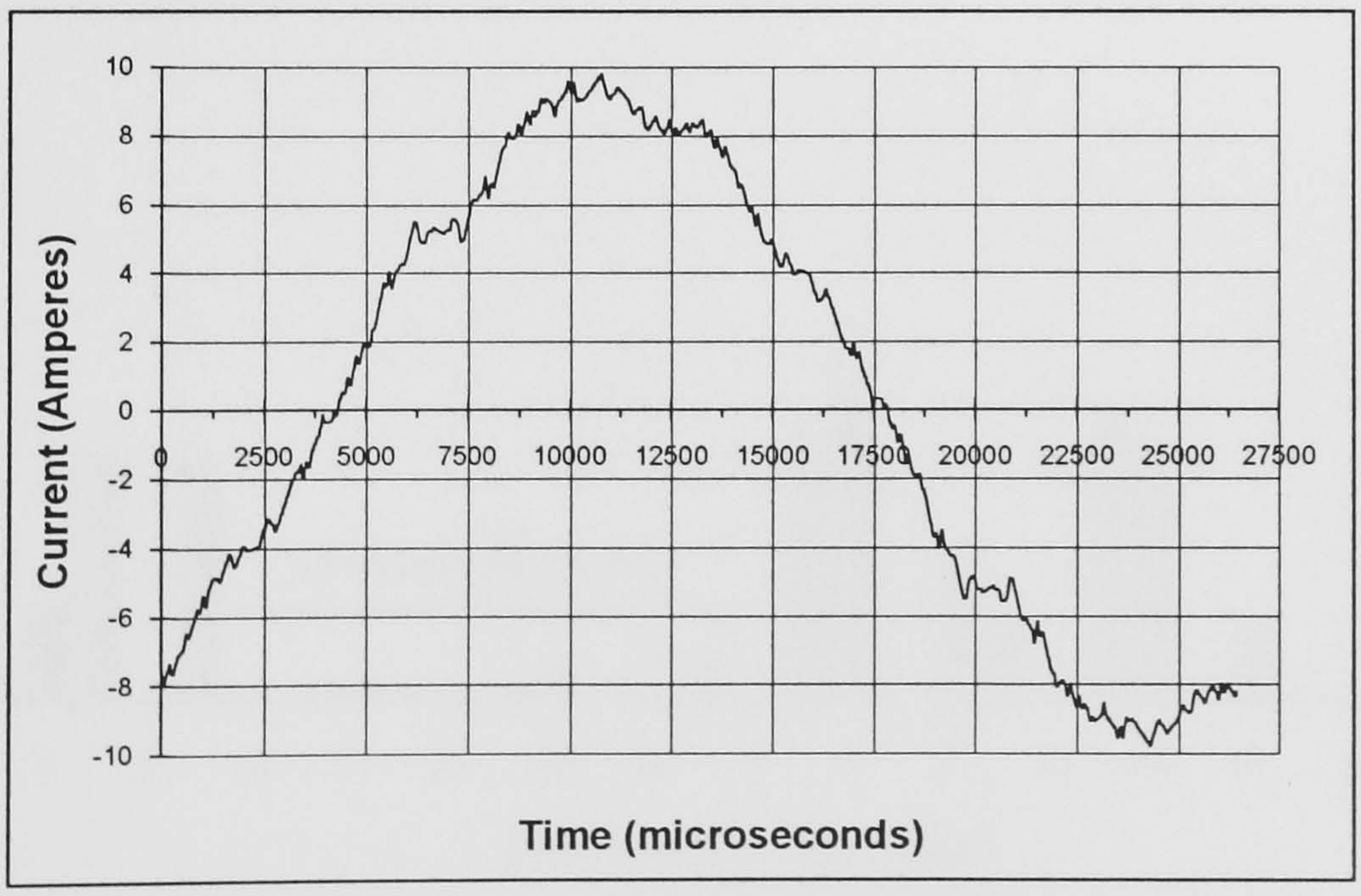

Figure 5.12 Simulated Phase Current for Pattern 2

To allow a further comparison between the simulated and measured values Figures 5.11 and 5.12 are given above. These waveforms were generated using 'pattern 2' which has a nominal fundamental of 0.55 per unit, and 100 pulses per quarter cycle. The minimised harmonics number

7, and lie in a band which commences at the 13th harmonic. It is the fact that a band of harmonics are eliminated, which accounts for the more distorted appearance of the current waveform compared to the tests using pattern 1. The load bank was set to 3.4Ω per phase for this test. Again, it can be seen that agreement is close between the measured and simulated values. However, a further factor which leads to discrepancies is the high frequency behaviour of the load matching transformer. The simulation model does not account for this but assumes a linear model throughout the frequency range.

As an additional test of the simulation and efficacy of the modulation process, a comparison of measured and simulated spectra of the phase voltages is given below in Figure 5.13. Note: The simulated spectrum was obtained using the simulation program described in Chapter 3, rather than the equations given for the 'ideal case' in Chapter 4, and apply to the loaded converter.

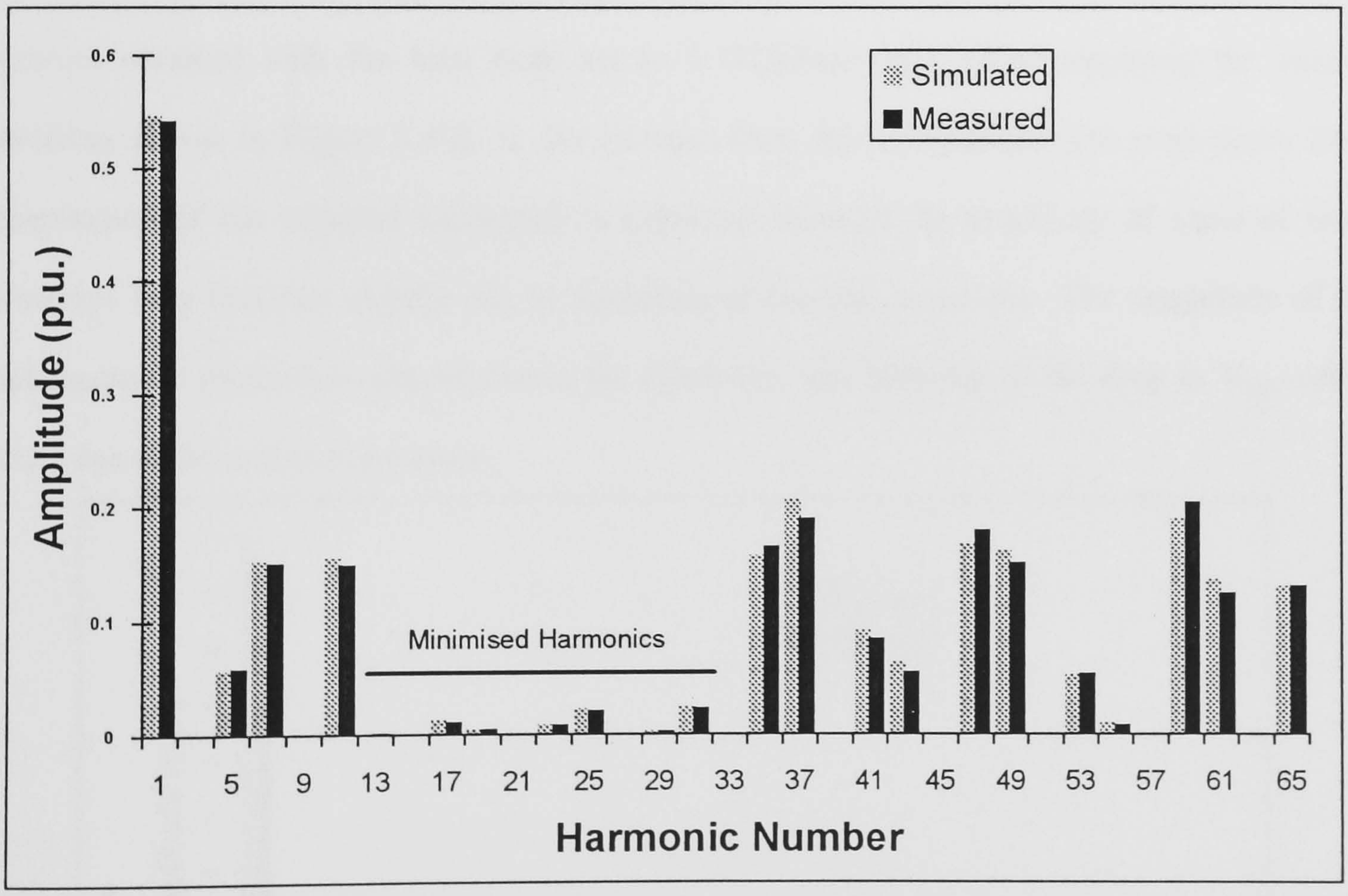

Figure 5.13 Simulated and Measured Spectra for Pattern 2 Phase Voltage

To allow an investigation of the effect which loads have on the modulation process, further tests were carried out using a modulation pattern having a nominal fundamental of 1.0 per unit, with the lowest 11 harmonics minimised, and having 125 pulses per quarter cycle. This generates a

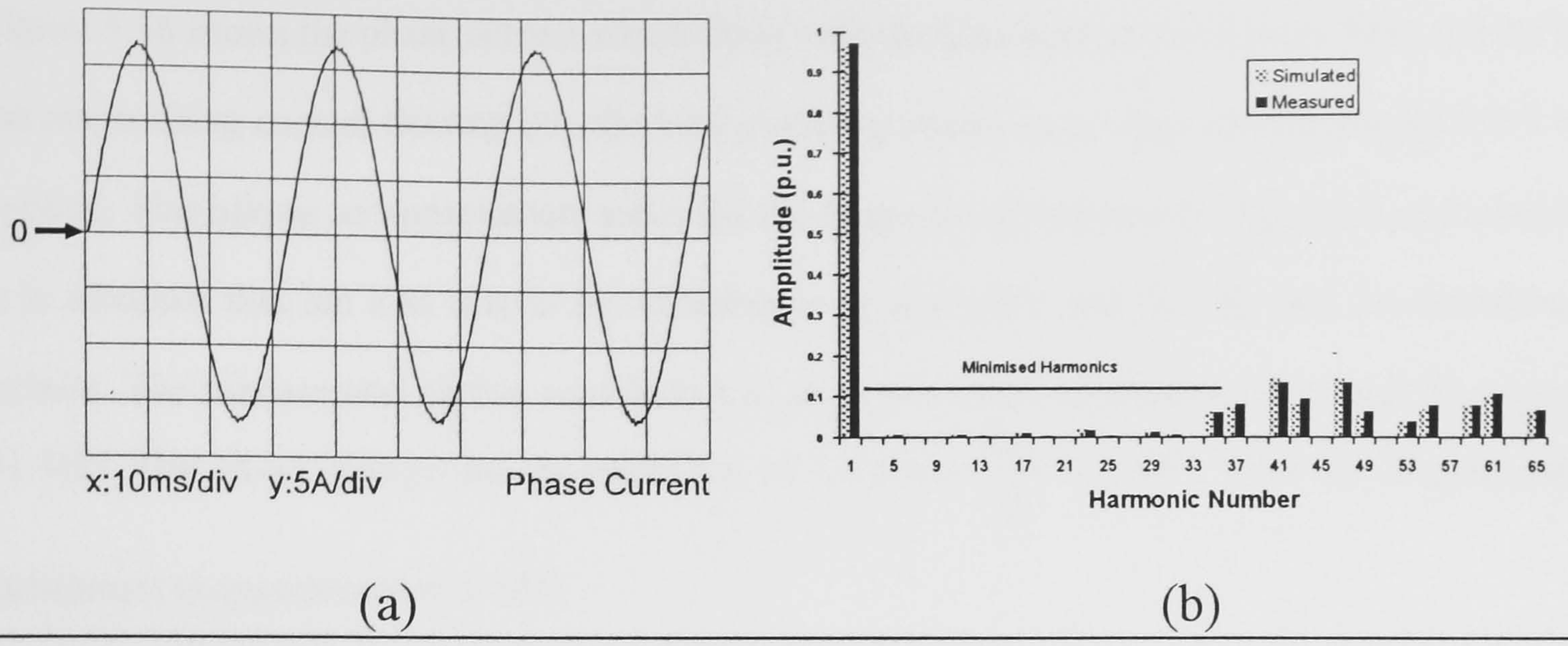

Figure 5.14 Phase Current and Comparison of Measured and Simulated Spectra for Pattern 3

waveform having a fundamental frequency of 31.4Hz. For completeness, the measured phase current is shown in Figure 5.14(a) and a comparison of measured and simulated spectra for the no-load phase voltage waveforms given in Figure 5.14(b). In Figure 5.15 a comparison is given between the spectrum of the phase voltage waveform with no load on the converter, and the spectrum obtained with the load bank set to 5.1Ω/phase. (i.e. when supplying the current waveform shown in Figure 5.14). It can be seen from this comparison that even under load, minimisation of the required harmonics is achieved although the amplitude of some of these harmonics may increase slightly due to distortion of the link waveform. The magnitude of the fundamental is somewhat reduced due to the distortion, and also due to the drop in V_{DC} which occurs due to the source impedance.

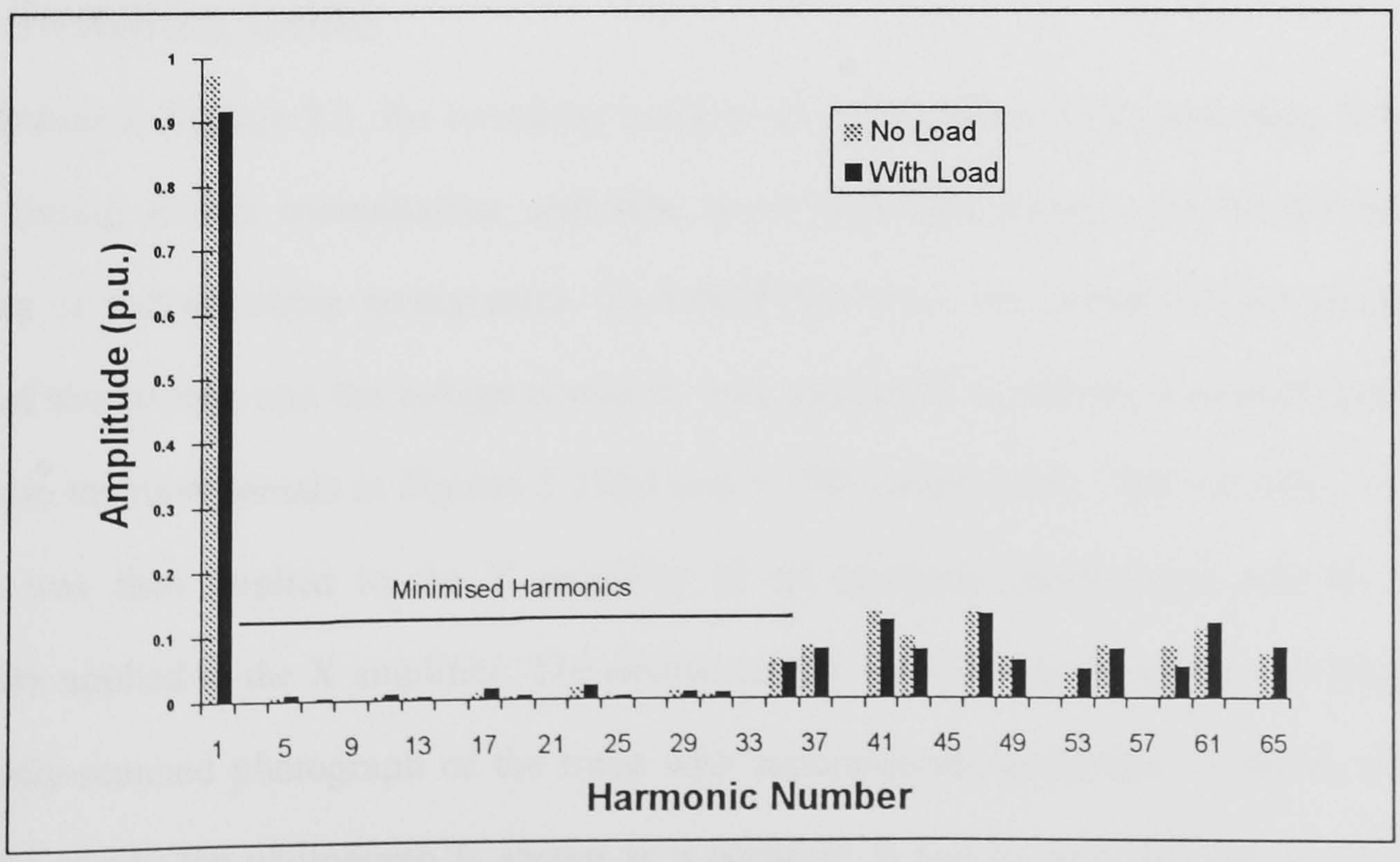

Figure 5.15 Comparison of Phase Voltage Spectra With, and Without Load

Figure 5.16 shows the phase current which flows with the load bank out of circuit. This current is the magnetising current flowing into the load matching transformer when modulation pattern 3 is applied. This allows an approximate value for the Magnetising Inductance, L_m, to be calculated. It is assumed that the iron loss in the transformer is negligible and thus R_i may be considered infinite. The fundamental of this waveform has an approximate amplitude of 1A, and frequency 31.4Hz. The phase voltage has an amplitude of $1.0 p.u. \times \frac{V_{DC}}{2} = 124V$. Thus the Magnetising Inductance is approximately 0.63H.

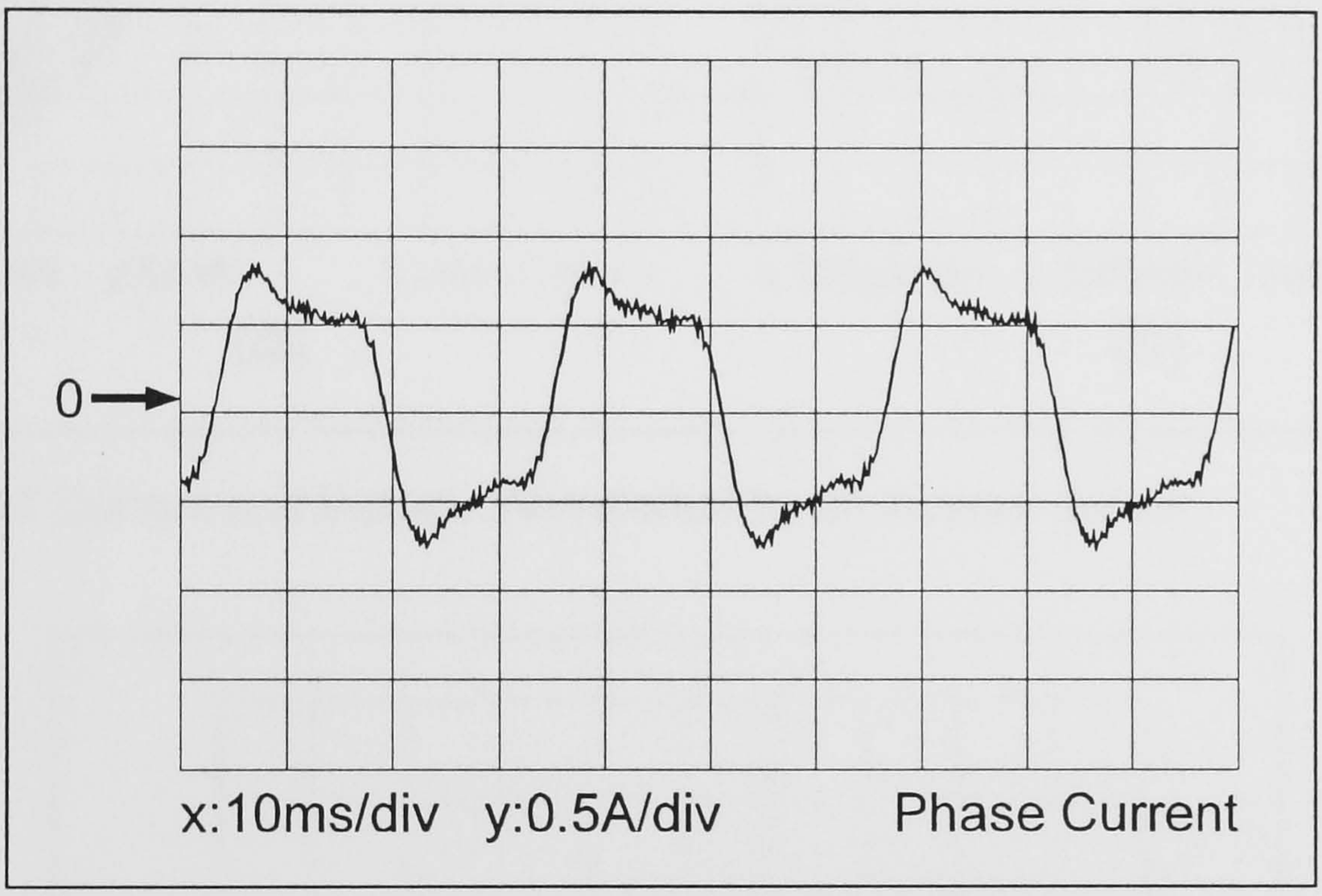

Figure 5.16 No-Load Phase Current With Pattern 3

5.3.2 Switching Locus

As explained in Section 2.1, the switching locus gives an indication of the switching loss which occurs during switch commutation, and thus is an important measure of the efficacy of a snubbing or soft-switching arrangement. To record the locus, the current flowing through one switch of the inverter and the voltage across it, were measured. A section of each of these traces is show in the time domain in Figures 5.17(a) and 5.17(b) respectively. The waveform of switch voltage was then applied to the Y amplifier of an analogue oscilloscope, and the current waveform applied to the X amplifier. The oscilloscope beam then traces out the switching locus. A digitally-scanned photograph of the trace with superimposed graticules, is shown in Figure 5.18. For clarity the photograph is shown as a negative. It can be seen that the area under the

locus is immeasurably small. This is an extremely important result as it points towards very low switching losses. Additionally it may be seen that the theoretical locus shown in Figure 2.4 is in fact somewhat pessimistic in its prediction of the area enclosed by the trajectory.

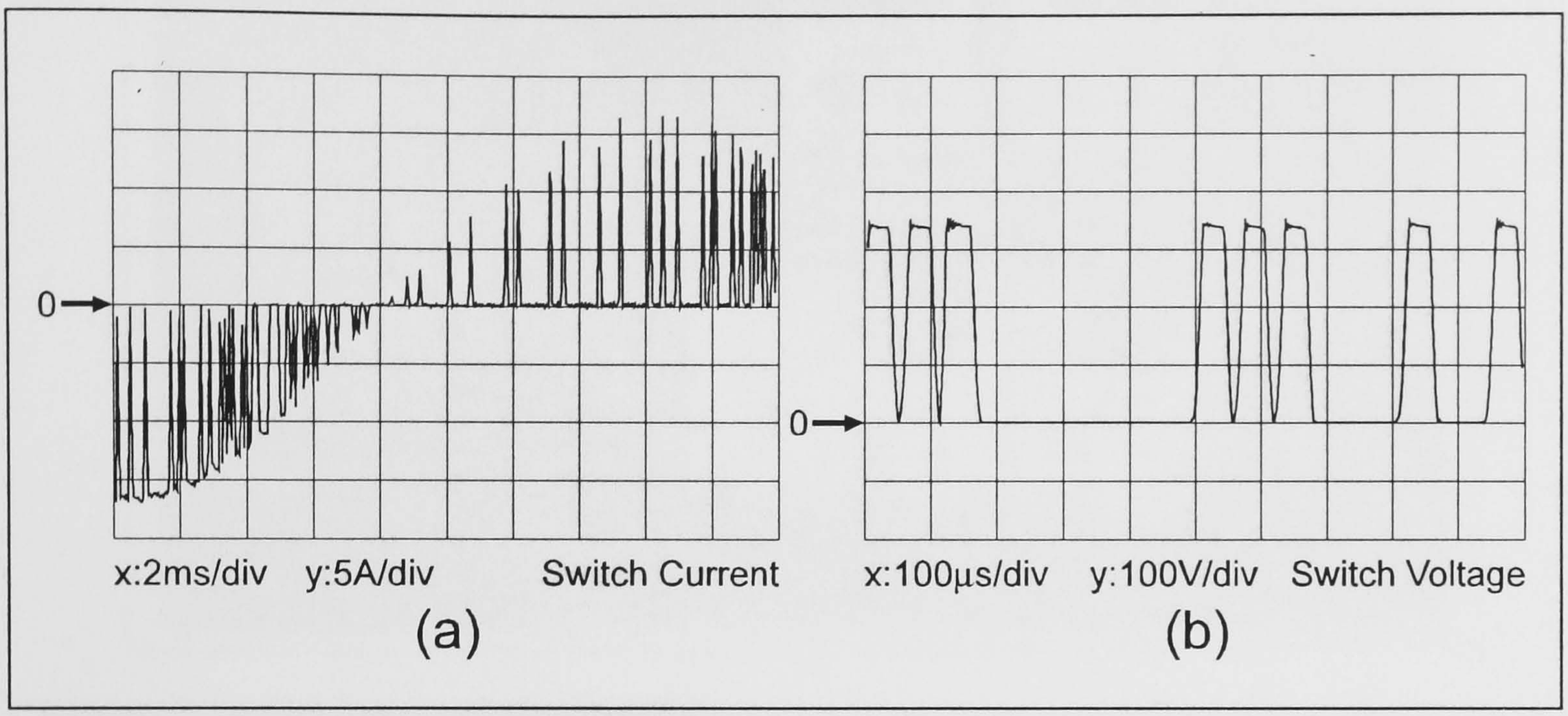

Figure 5.17 Current and Voltage Waveforms for an Inverter Switch

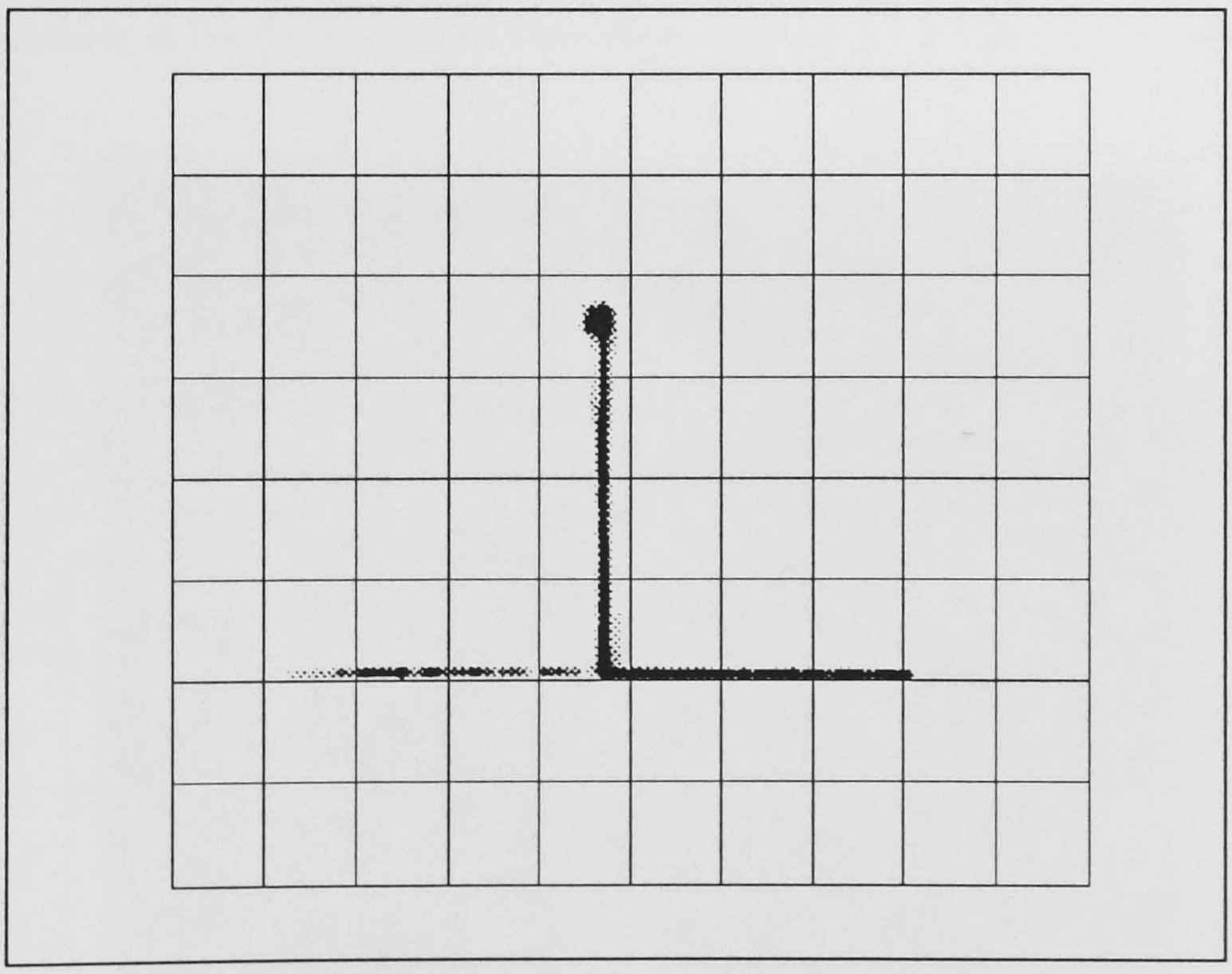

Figure 5.18 Switching Locus. x: 5A/div, y: 100V/div

5.3.3 Photographs of the Test-Rig

In this section photographs of the output stage of the test-rig are presented with a brief description to aid identification of the major components.

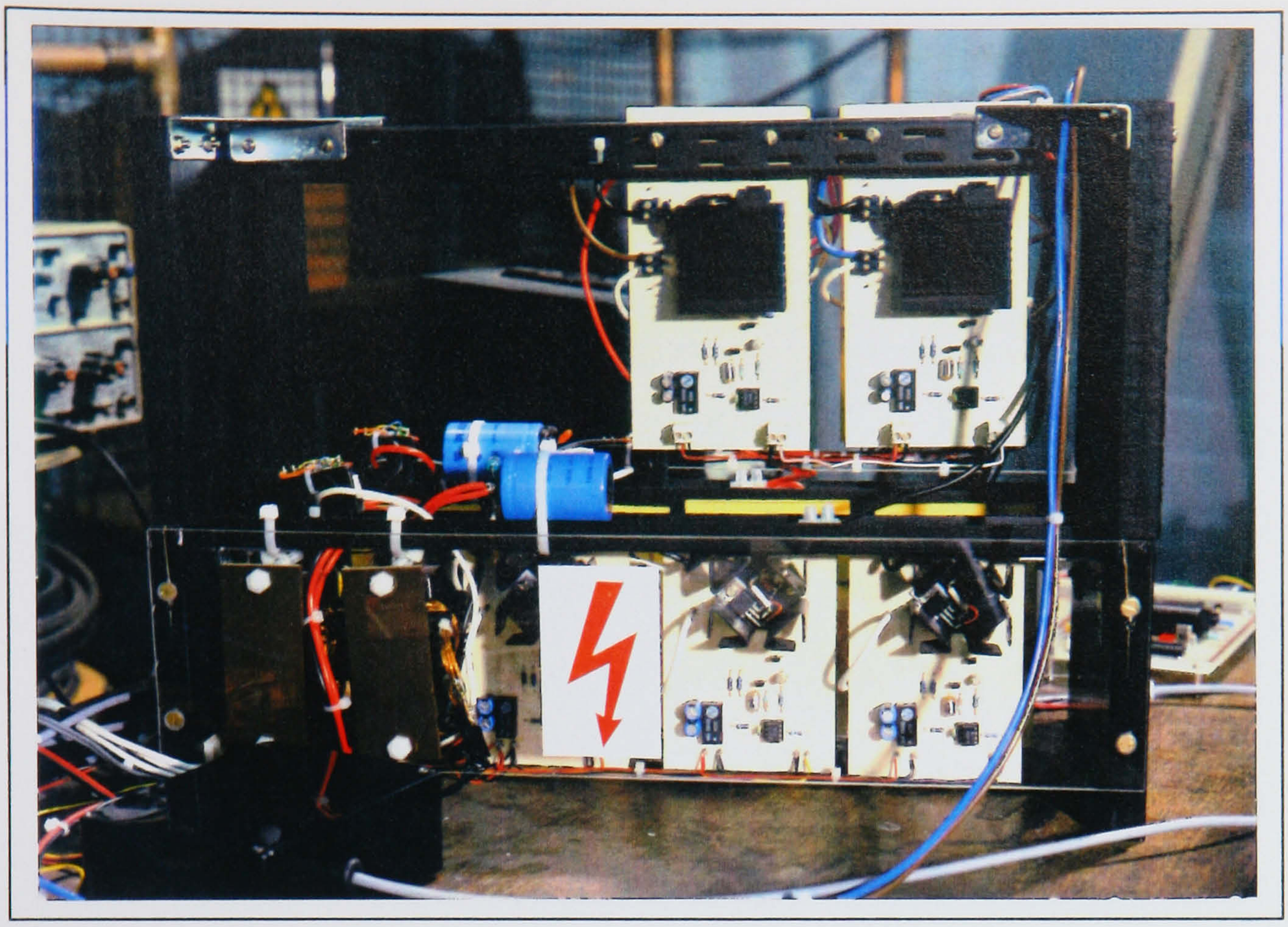

Figure 5.19 Side View of the Test-Rig

On the bottom layer 3 PCBs supporting switches of the output stage can be seen. The two top PCBs form part of the input stage which is described in Chapter 6. To the left of the output switches is the resonant inductor, (divided into two separate inductors). The blue electrolytic capacitor at the front is for power supply smoothing, the one at the back is the clamp capacitor.

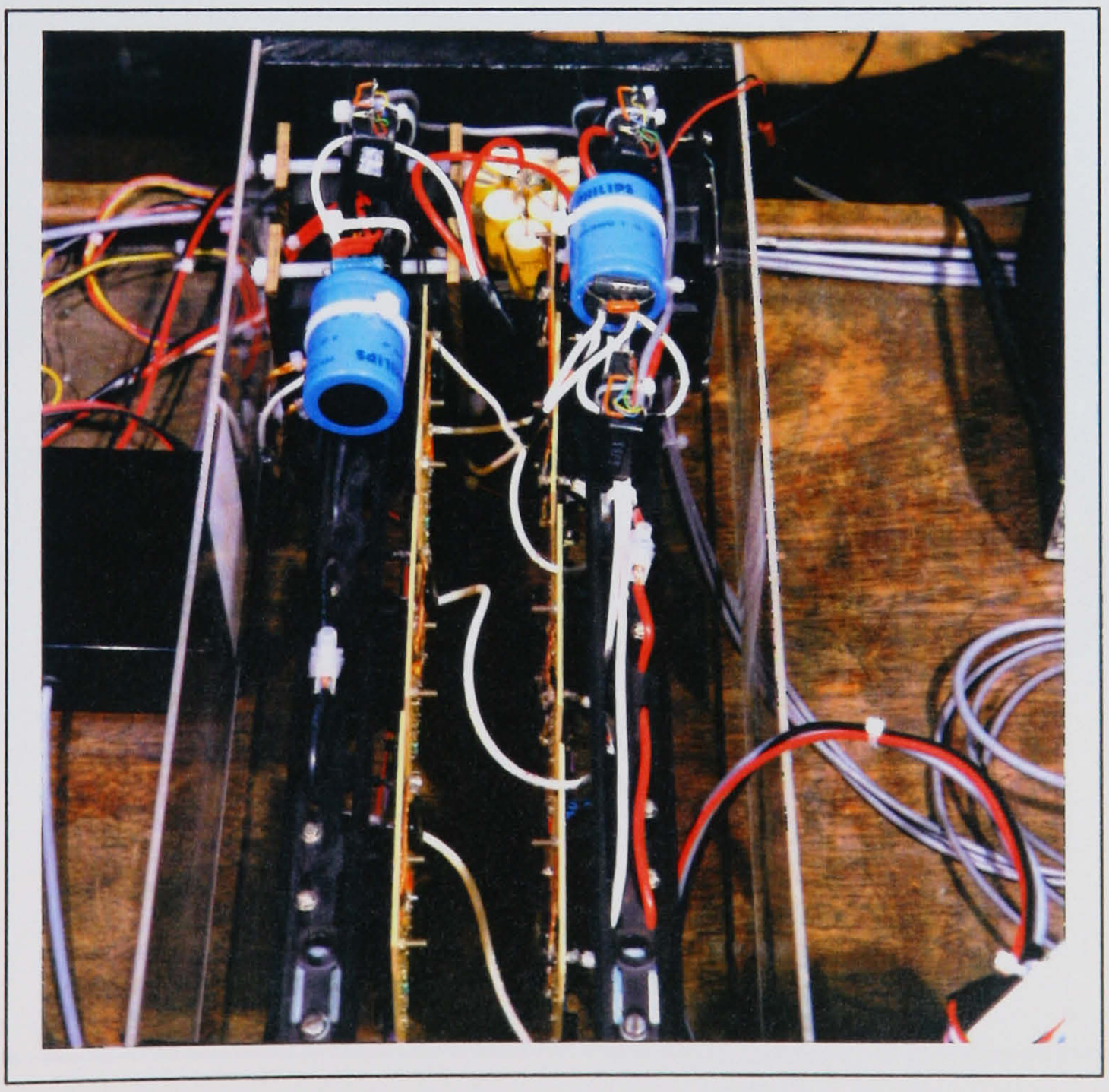

Figure 5.20 Plan View of the Test-Rig (with input stage removed)

The yellow group of capacitors at the far end of the rig form the resonant capacitor.

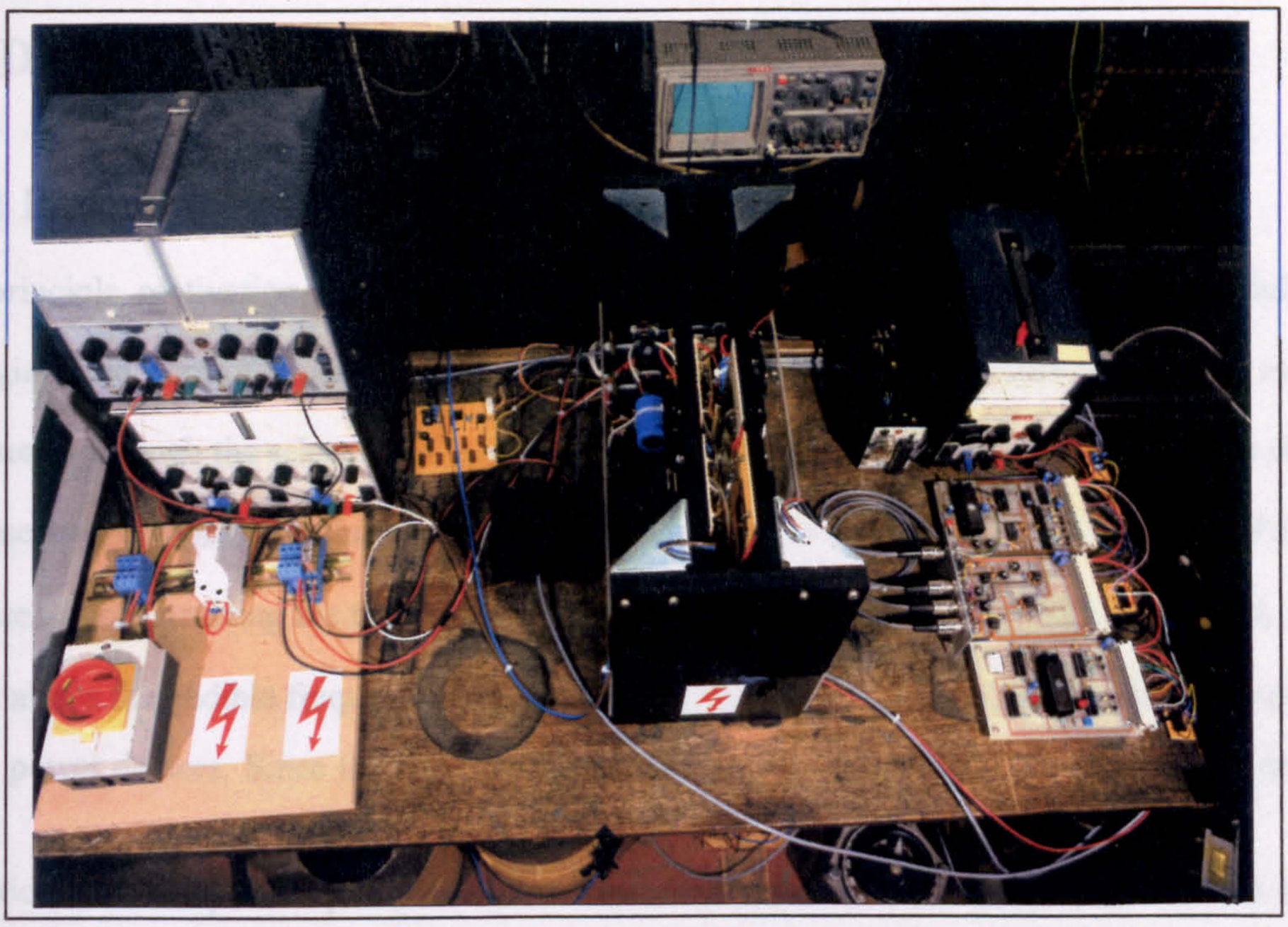

Figure 5.21 Overview of the Test Facility
In the centre lies the power circuit. To the right of this are the signal conditioning and control boards, to the left on a small circuit board is the zero-crossing detector circuit, and to the far left are the supplies feeding the clamp capacitor.

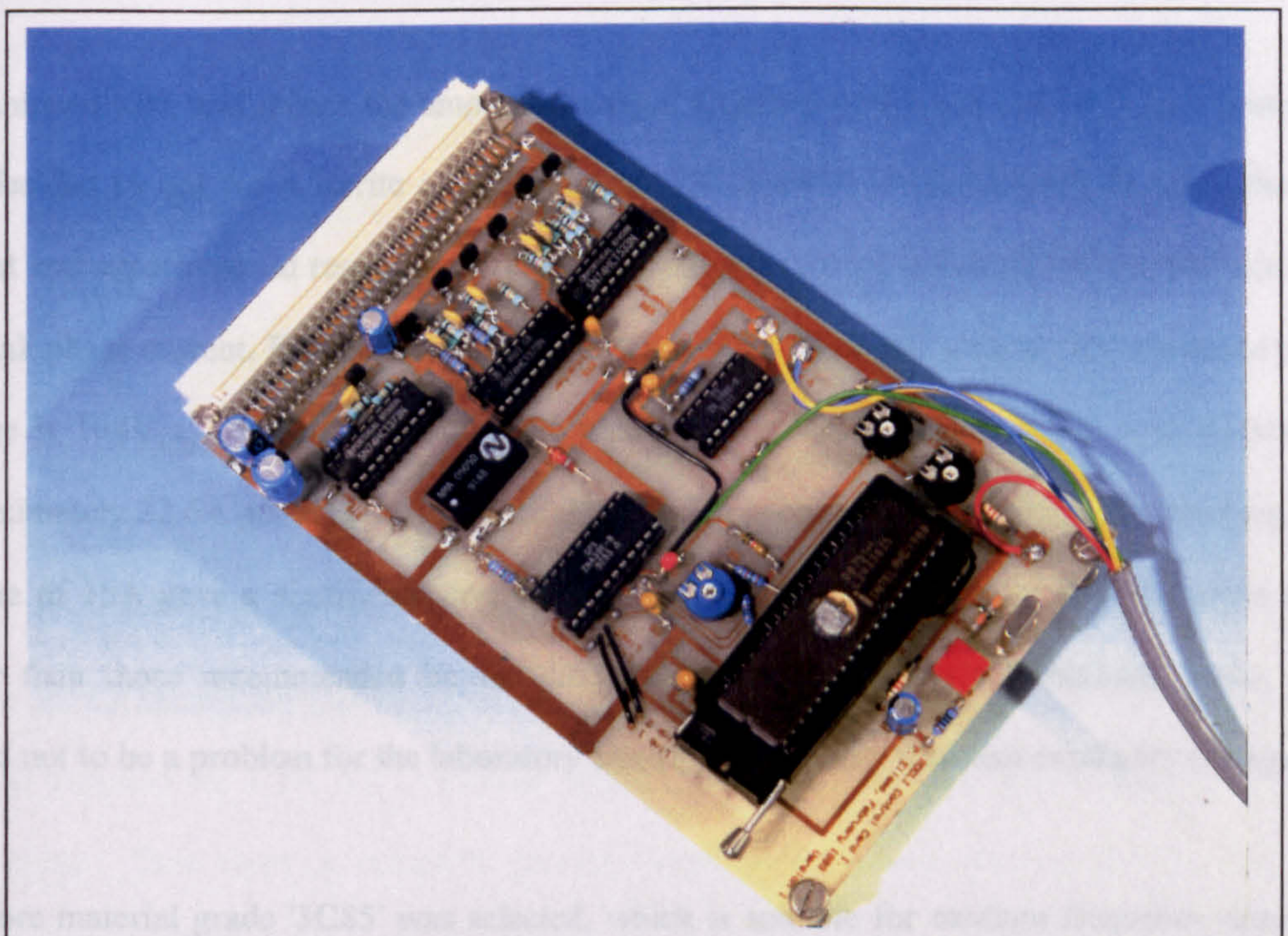

Figure 5.22 Microprocessor Control Board
To the right is the 8051 microcontroller. To its left are the A/D and D/A converters. On the far left are the control circuits for the IGBT drivers.

5.4 Design of the Major System Components

5.4.1 Resonant Inductor and Capacitor Design

The principle motivation for constructing a test rig was for the investigation of modulation strategies, and control procedure. As a consequence, no attempt was made to optimise system parameters through the selection of L_r and C_r values. There are many criteria affecting the choice of these two component values, and these are discussed in some detail in Chapter 7. For the purposes of constructing the test rig, a nominal resonant frequency of 20kHz was selected, since this is above the audible frequency range, yet places modest demands on the switching frequency of the power devices. Since the resonant frequency, f_r, is given by $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, this defines the ratio between L_r and C_r. The actual inductance and capacitance values were selected on an intuitive and cost basis such that the components had similar physical size. The nominal values selected were L_r=100μH, and C_r=0.63μF. The design process for the inductor is an iterative one, but rather than explaining every step taken, the description below simply justifies the final design.

To minimise size, and reduce the amount of copper required (and hence reduce copper losses), it was decided to opt for a ferrite cored inductor. The inductor must be rated to carry the link current and superimposed resonant current. The peak link current is determined by, and equal to, the peak phase current. For a converter such as this with a 240V DC supply, the maximum phase voltage is $108V_{RMS}$, which means that the phase current for operation at 3kVA is 16.04A, or approximately 22.6A peak. However, during the design procedure it was found that working with a value of 15A gave a significant cost saving. The consequence of this is for flux levels to be higher than those recommended by the core manufacturer, leading to increased losses. This proved not to be a problem for the laboratory test-rig, where only transient capability is required.

The core material grade '3C85' was selected, which is suitable for medium frequency operation (i.e. up to 200kHz). The manufacturers supply graphs of 'I_m^2L' for their cores [61], where I_m is the peak current flowing in the windings, and L is the inductance. From equation (5.5) it can be

seen that the peak current in the inductor for these values of L_r and C_r is approximately 19+15=34A. Thus $I_m^2L=34^2x100x10^{-6}=0.1156$. The Philips EE65/32/27 core was selected because of its high I_m^2L value. To allow sufficient space to fit the windings onto the coil former, it was found to be necessary to divide the inductance into two separate components each consisting of two EE65/32/27 core halves, having an I_m^2L value of 0.0578. From the I_m^2L graph it may be found that a 2mm centre-leg air gap is required (or 1mm distributed gap). The core manufacturers also specify an 'A_L' value. This defines the inductance for a given air gap, where $L=N^2A_L$ (in nH). N is the number of turns. A_L for these core halves with a 1mm air gap (defined in the databook as 0.5mm per core half) is approximately 322. Therefore for each inductor (of nominal value 50μH), the number of turns required is $\sqrt{\frac{L(nH)}{A_L}} = 12$ (to the nearest turn). To alleviate the problems of skin effect, bundled strands were used for the windings. The optimum gauge of wire for this application is given in reference [62] as 19AWG (20SWG). To give the required current carrying capability 7 strands are required in each bundle.

The capacitor specification was very straightforward. Polypropylene capacitors were used due to their excellent low-loss high frequency performance, and ability to withstand continuous application of high AC voltages.

5.4.2. Power Device Selection and Gate Driver Circuits

Figure 5.23 shows the IGBT and associated gate drive circuitry. IGBTs were selected for their ease of driving. The International Rectifier IRGBC40U IGBT which was used, is of an ultra-fast variety, rated for use at greater than 10kHz. Its voltage rating of $600V_{CEO}$ and current rating of 40A (at 25°C) are appropriate for the desired converter rating of 3kVA. The drive circuit for the IGBT is supplied via a DC-DC converter which has floating outputs, and is controlled via an opto-isolator. Thus there is complete galvanic separation between the low-voltage and high voltage circuits which reduces the probability of the power circuit interfering with the control circuitry, and allows the necessary high voltage excursions by the gate of the 'top' device in each leg of the inverter bridge.

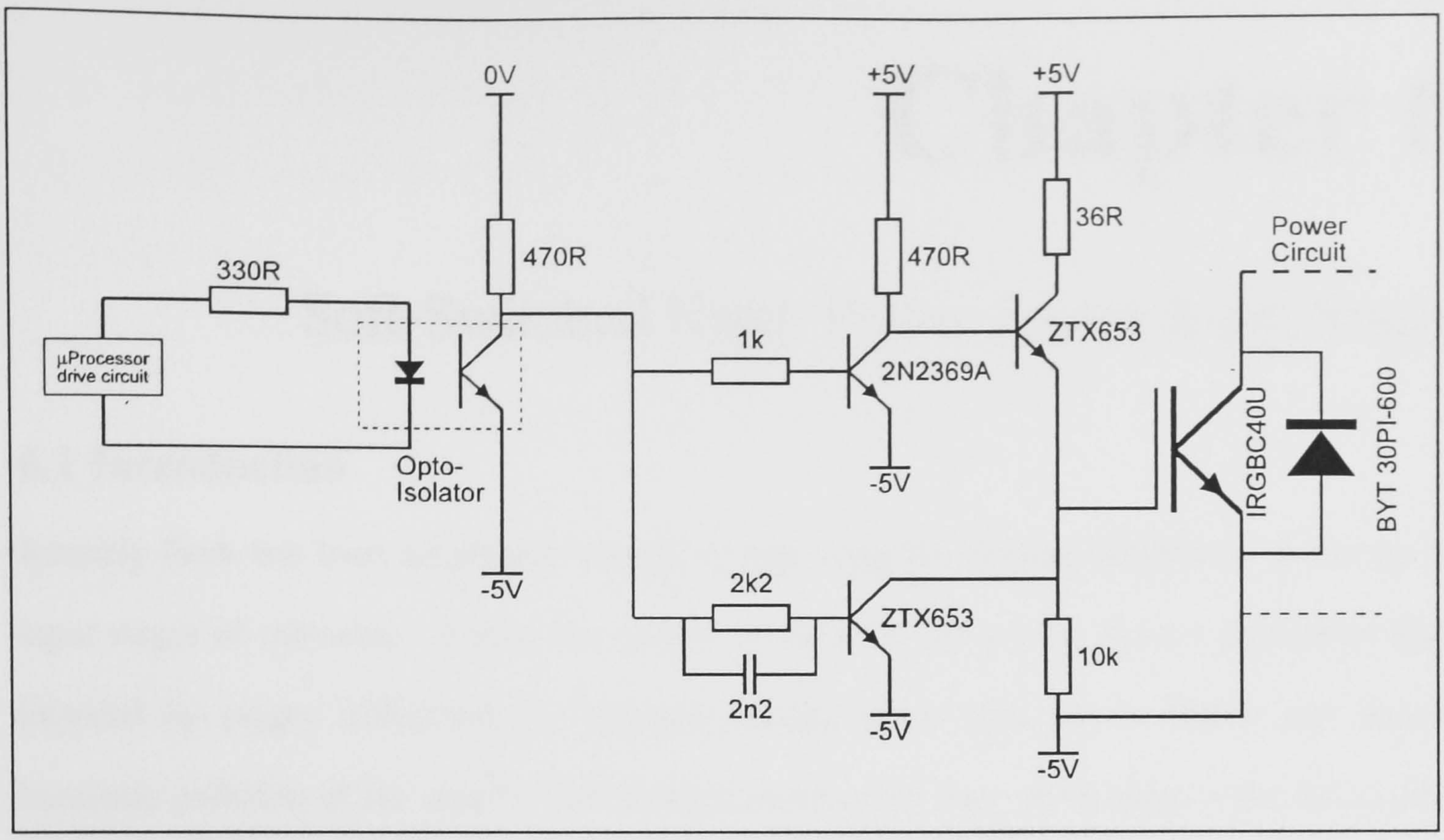

Figure 5.23 IGBT Driver Circuit

5.5 Chapter Summary

It is possible to achieve effective control of a Resonant DC Link Inverter using one fairly simple microcontroller, such as an 8051, in conjunction with A/D and D/A converters. Equations may be derived to describe the time domain operation of the resonant circuit, and also the harmonic spectrum which is generated by the RDCLI when applying a given modulation pattern. These equations were shown to accurately predict the converters operation by comparison between practically measured, and simulated results. Some discrepancy was evident due to approximations and simplifications made in the simulation program. For example, the simulation assumes a linear response for the load over the entire frequency range

It is possible to achieve harmonic minimisation in practice using the modulation techniques outlined in Chapter 4. When the converter is under load some distortion of the resonant link waveform occurs which affects the modulation process to a small extent. but effective harmonic minimisation is still achieved. A measurement taken from one of the inverter switches revealed a very small area contained by the switching locus, indicating that the conditions exist for very low switching loss with this type of converter.

Chapter 6

Soft-Switched Unity Power Factor Input Stages

6.1 Introduction

Recently there has been heightened interest in improving the current waveforms drawn by the input stages of converters. Among the various reasons for this are the stricter regulations being imposed by supply authorities for operating equipment at poor power factor, and limiting harmonic pollution of the supply. The constraints are even more demanding in the rail traction environment where there may be further restrictions imposed to prevent interference with signalling and communications equipment [63]. The problems are compounded yet further where rail vehicles are supplied by single phase AC, compared to the industrial situation where 3-phase AC is most common. The result of this is higher line current for a given load, and thus increased probability of interference.

The discussions so far have centred on the output stage of the Resonant DC Link Inverter, assuming a DC supply to be readily available. However in many cases, rail vehicles are supplied from an AC source which must firstly be rectified by the converter. This may be achieved using a simple diode bridge, but as will be seen in this chapter, this is not desirable in terms of the size and weight of the converter, or the harmonics it generates. This is becoming a more significant factor as the demands on train auxiliaries are becoming greater, fuelled by increases in passenger comfort facilities. Due to the larger auxiliary supplies, they contribute more significantly than ever, to the overall psophometric current of a train. Additionally improvements in traction converter front-ends mean that the level of psophometric current emanating from the auxiliaries is *proportionally* even greater. As a consequence, the argument for improving the quality of the input waveform of auxiliary converters is becoming more convincing.

In this chapter, methods of input-current shaping are briefly reviewed, and a converter system proposed which implements shaping using a soft-switched converter topology, thereby reducing the device losses. This converter is based on the Resonant DC Link Inverter and thus has the associated restriction of Discrete Pulse Modulation. A suitable modulation strategy is outlined, and verified by comparison with results from a low-power test-rig.

6.2 Review of Input-Current Shaping Circuits

6.2.1 Hard-Switching Input-Current Shaping Topologies

A common and very simple active rectifier is the 1-switch variety as shown in Figure 6.1. [64] In general, the inductor may be placed either on the AC or DC side of the rectifier without affecting the circuit operation. The switch T1 is opened and closed momentarily to cause small increments and decrements in the inductor current, thus shaping the input current, I_{IN}. This approach is attractive due to its extreme simplicity and low device count; however, the harmonic control achievable is quite limited. It is not possible to control individual harmonics using this scheme. Other, more efficient topologies are possible, for example the 2-switch H-bridge [64] but the degree of harmonic control is the same as the one switch type.

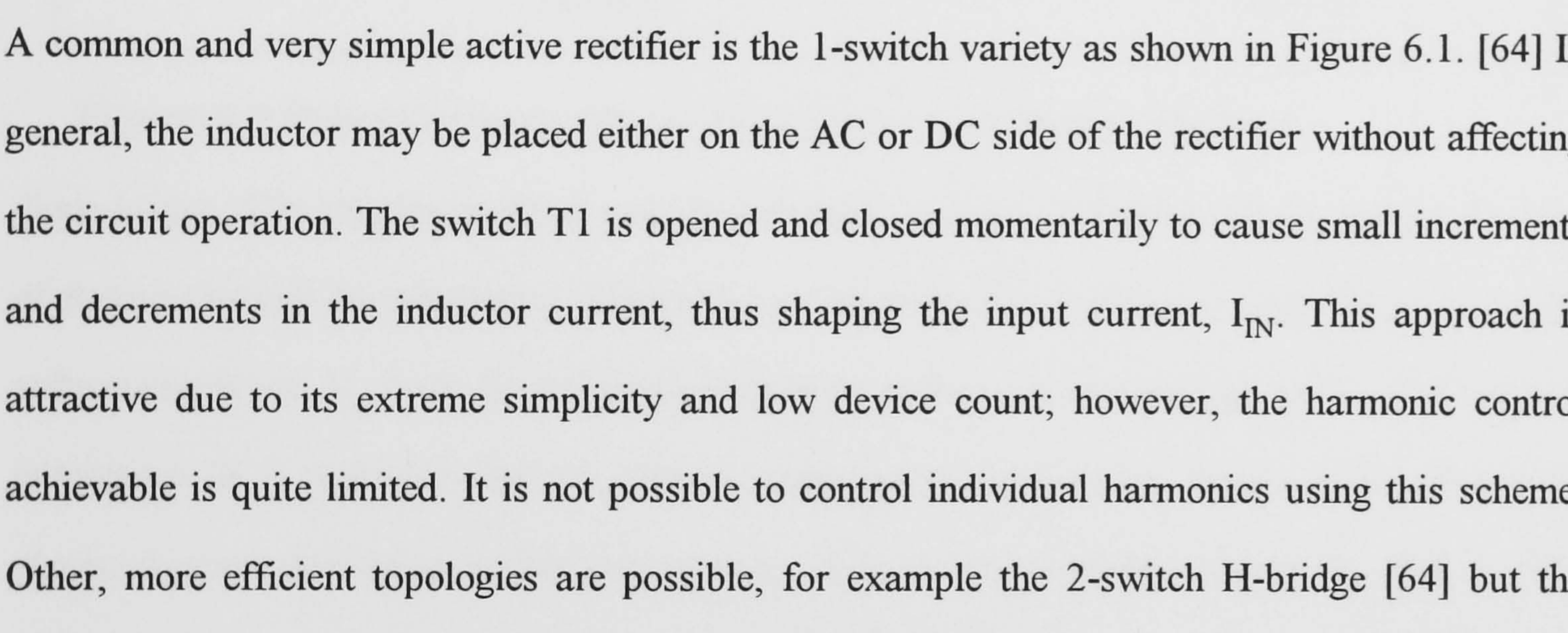

Figure 6.1 1-Switch Active Bridge Rectifier

A more effective, although more complex form of converter is the 'Pulse Converter'. This type of converter may be considered as a single-phase inverter bridge operating in anti-parallel with a

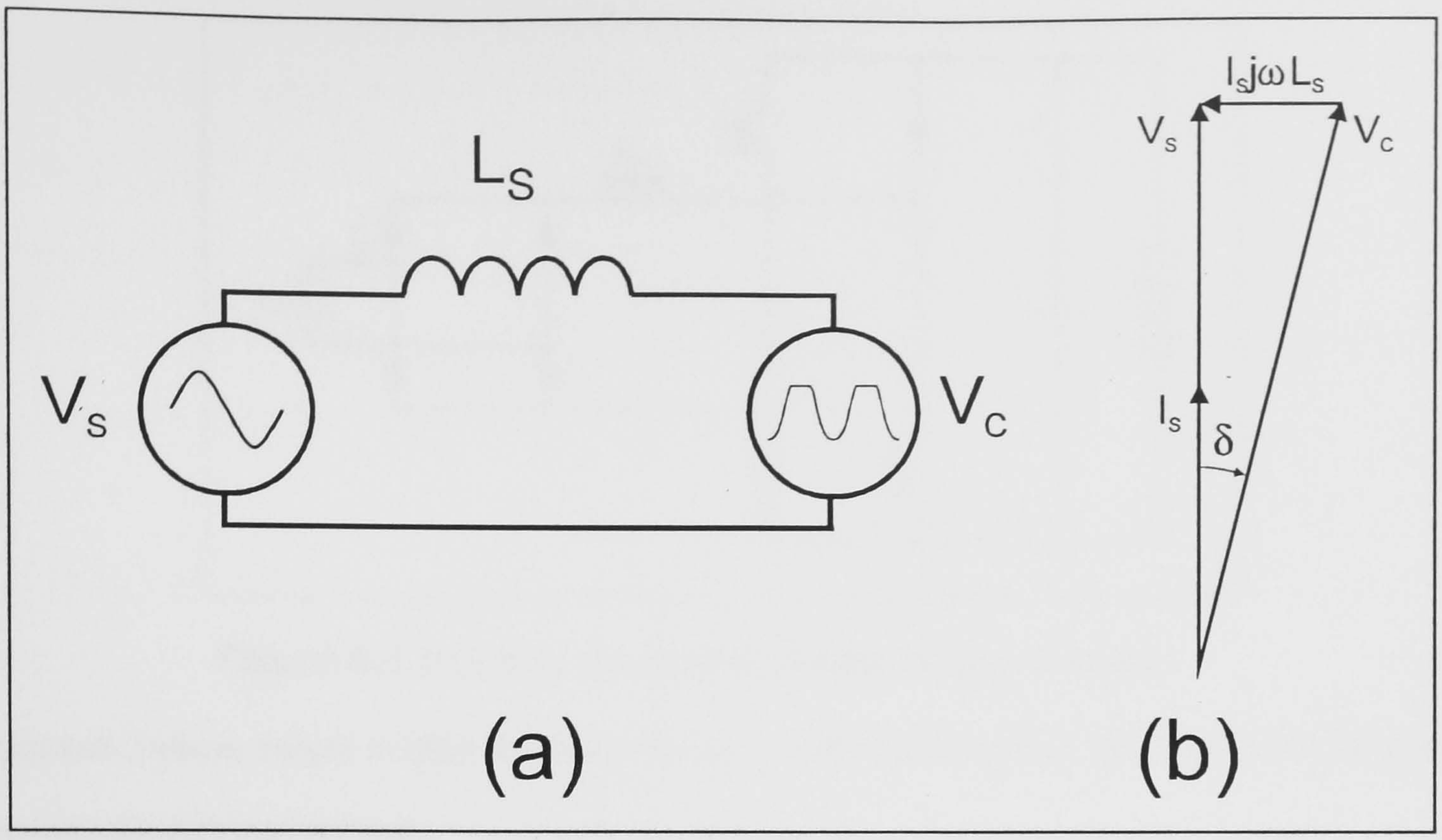

Figure 6.2 Pulse Converter Equivalent Circuit and Phasor Diagram

diode-bridge. The inverter bridge is used to generate a voltage waveform which controls the flow of current through an inductance. This is shown schematically in Figure 6.2(a). V_S is the supply voltage amplitude, V_C is the fundamental component of the converter voltage and L_S is the source inductance (it is assumed that the inductor resistance is negligible). Figure 6.2(b) shows the phasor diagram pertaining to this arrangement, 'δ' is the phase angle between V_S, and V_C. The operation of the pulse converter is discussed in more detail below. A basic implementation of this type of converter is shown in Figure 6.3. A disadvantage of this scheme is the addition of 4 switching devices to the basic rectifier configuration, significantly increasing the cost. Attempts have been made to address this problem, for example the 2-switch asymmetrical half-bridge circuit shown in Figure 6.4. The disadvantage of this implementation is that the input current must pass through 4 semiconductor devices as opposed to 2 in the case of the 4-switch H-bridge scheme. A further possibility was suggested by Enjeti and Rahman [65], which only requires 6 switching devices to implement both

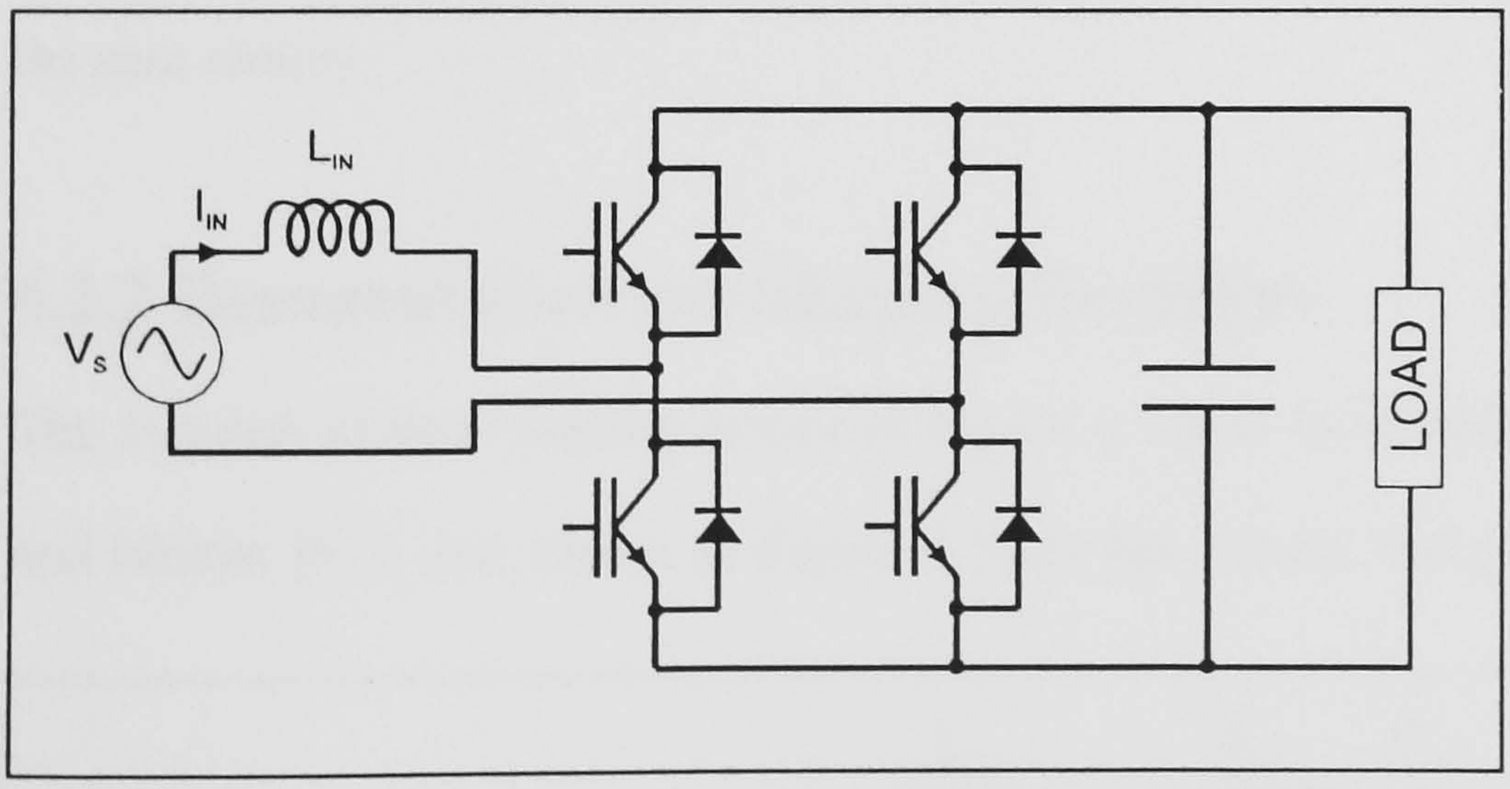

Figure 6.3 4-Switch H-bridge Rectifier

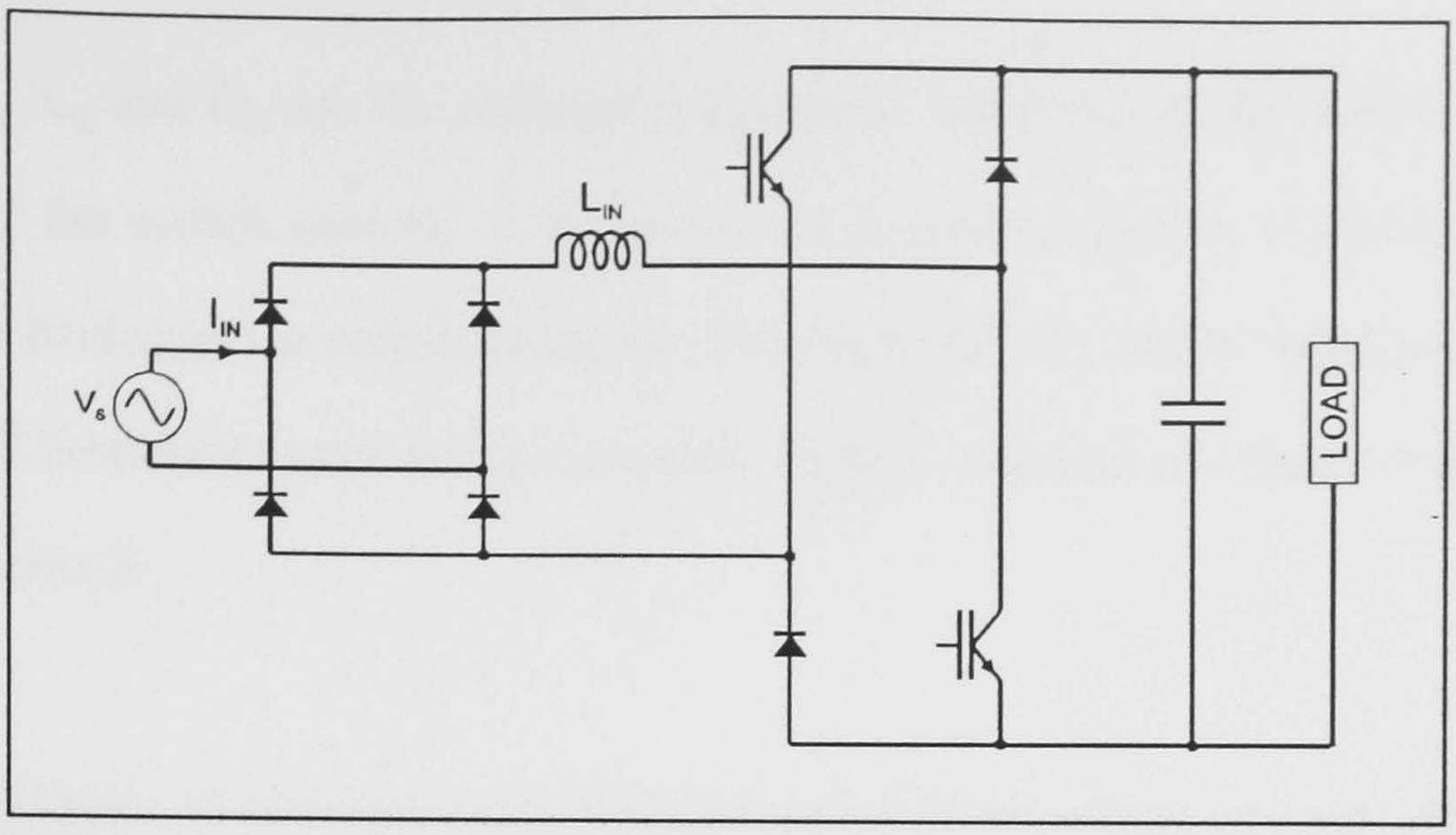

Figure 6.4 2-Switch Asymmetrical Half-Bridge Rectifier

input and 3-phase output control. However it uses a split capacitor link which must be capable of carrying the full load current.

Clearly there are many ways of implementing a converter which has the properties of a pulse converter; however, all the topologies outlined above employ hard switching and thus suffer from high switching losses. In order to alleviate this problem, Thiyagarajah *et al* [66] proposed a 4-switch H-bridge pulse-converter using energy recovery snubbers. However as explained in Chapter 2, this leads to a considerable increase in circuit complexity. An alternative as discussed earlier with regard to the output stage, is to employ resonant topologies, and this is the subject of the next section.

6.2.2 Resonant Current-Shaping Rectifiers

The 1-switch current shaping circuit of Figure 6.1 may be modified as was demonstrated by He and Mohan [67], and shown in Figure 6.5. In this circuit, the switch S_1 shapes the current in

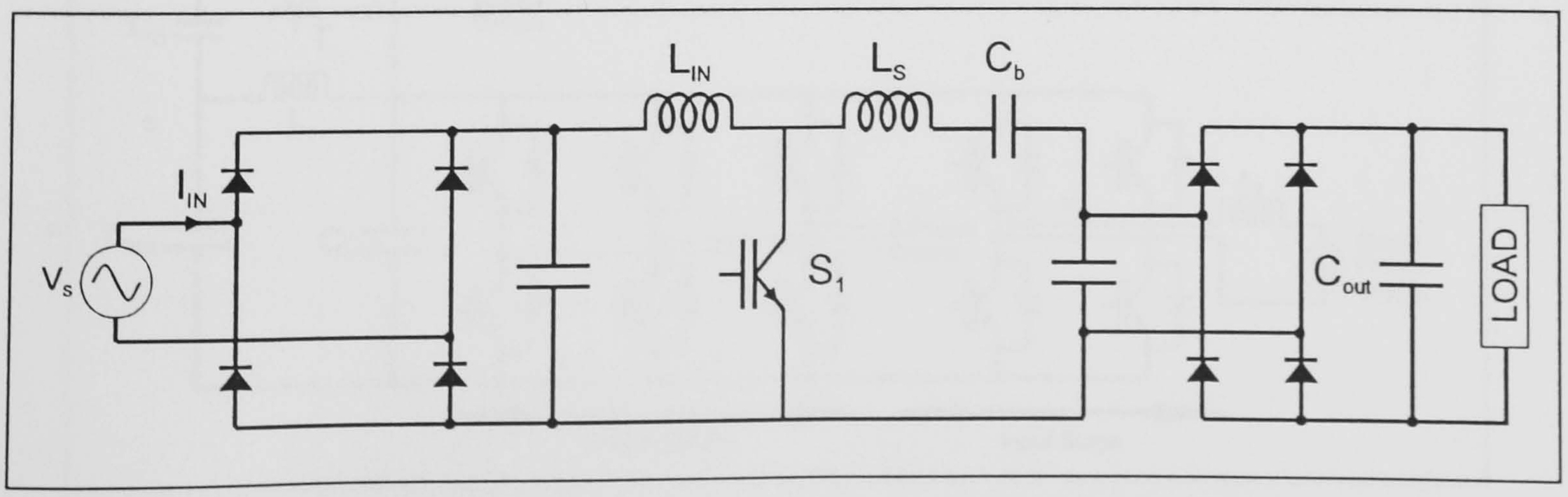

Figure 6.5 1-Switch Resonant Current-Shaping Rectifier

inductance, L_{in}. L_s and C_b are the resonant components which create the conditions for natural commutation of the switch current. A further diode bridge is required to rectify the resonant current in order to charge the output capacitor. This increases the overall conduction loss and in addition, similar limitations exist on the harmonic control properties to those encountered in the hard-switching circuit.

A different approach is to incorporate conventional hard-switching circuits into an existing Resonant DC Link topology. This is shown in Figure 6.6 [68] using the 4-switch H-bridge topology as an example. In this embodiment the zero-crossings of the resonant link are applied to the input stage. Consequently the input bridge circuit may also benefit from soft-switching. An important feature of this type of circuit is that no additional components are required compared to the hard-switching implementation. Many hard-switching circuits may be incorporated into zero-switching topologies in this manner, for example the single switch boost converter [69], which was shown in hard-switching format in Figure 6.1. The disadvantage of doing this is that the input stage is constrained to use Discrete Pulse Modulation. This has far-reaching implications for the modulation strategy and forms the main issue of this chapter. The 4-switch H-bridge pulse converter is used an example throughout, and it is shown how it is possible to implement a pre-programmed modulation strategy in order to achieve complex harmonic control of the input current. There is a significant difference in the control of the input stage compared to the control of the output stage of such converters, since the modulation pattern must be synchronised with the supply waveform.

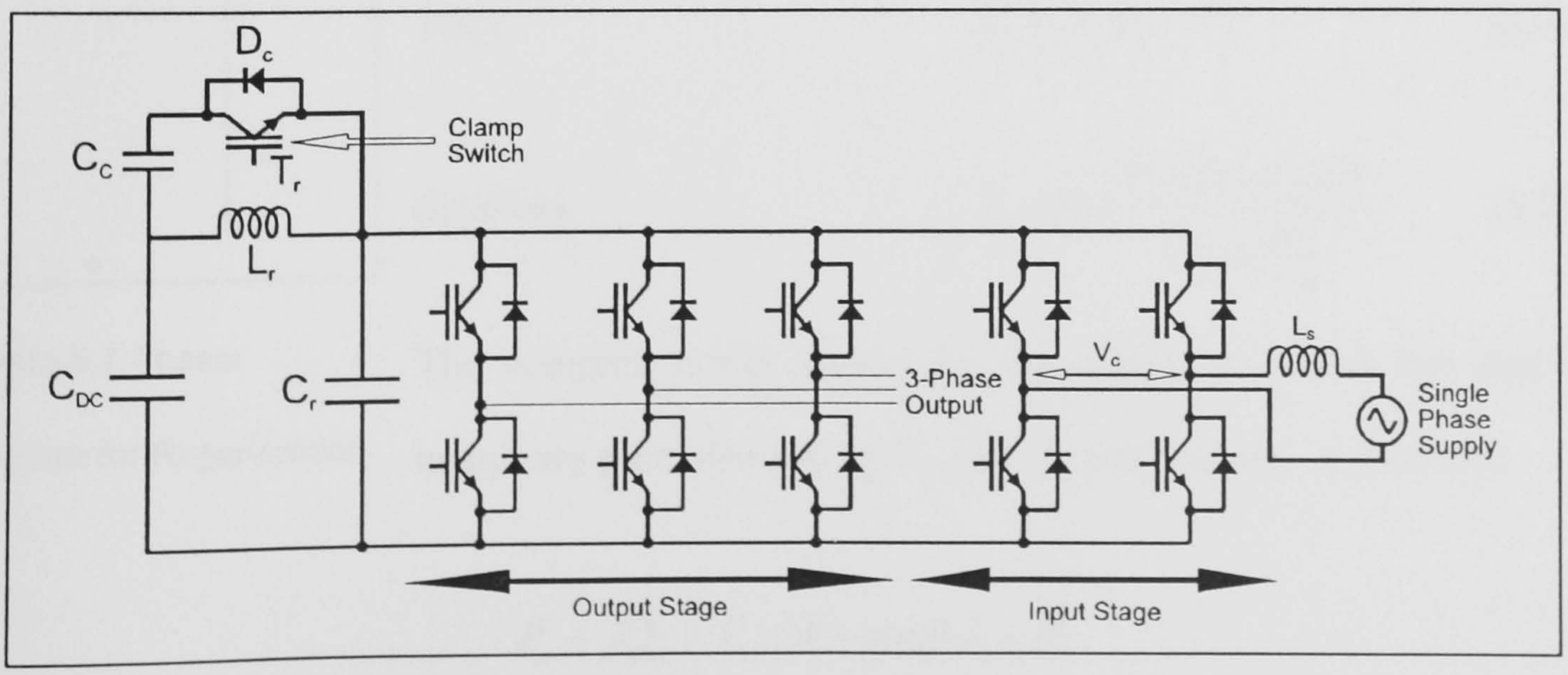

Figure 6.6 ACRDLI with Pulse Converter Input Stage

6.3 PULSE CONVERTER FUNDAMENTALS

6.3.1 Introduction

The use of a pulse converter as the front end for a single-phase to three-phase conversion system allows four-quadrant operation with near-unity power factor. The four-quadrant operation may be described in terms of its two operating regions of 'motoring' and 'regeneration', although in the case of an auxiliary inverter the load is unlikely to consist merely of motors, and it is unlikely that the converter would be required to re-generate. However for simplicity, these terms will be used to describe power flow into, and out of the converter respectively. In this section simple equations will be derived to describe the operation of the pulse converter, and allow simple design criteria to be established. [70]

6.3.2 Power Flow Equations

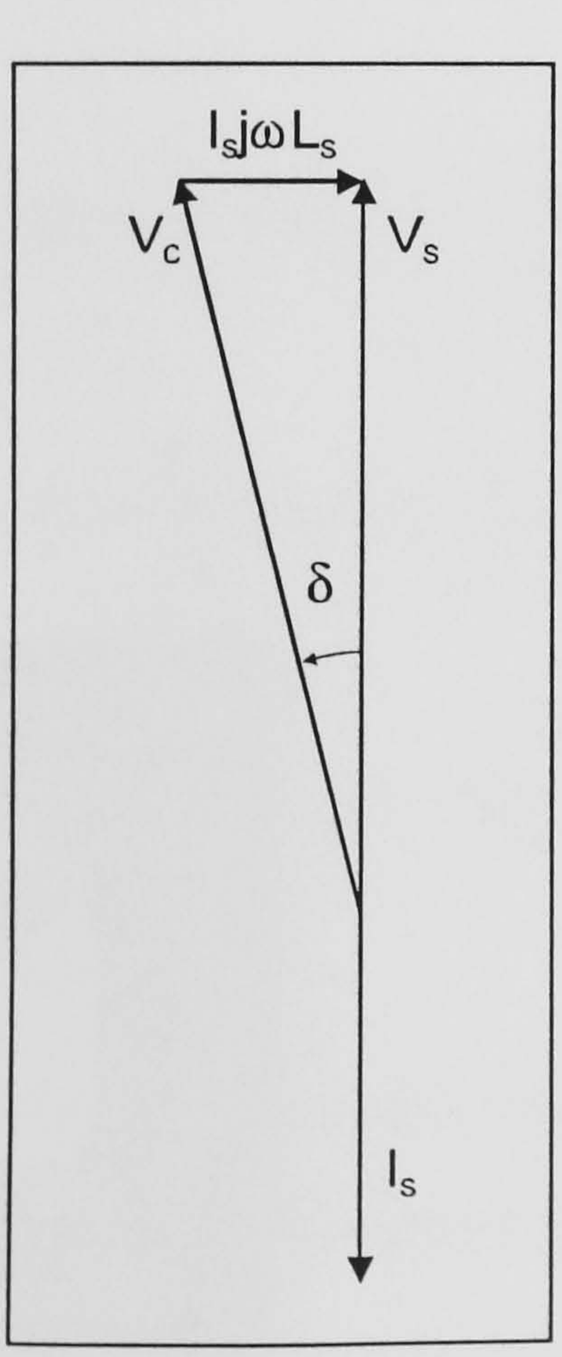

Figure 6.7 Phasor Diagram for Regeneration

Consider the pulse converter equivalent circuit as shown in Figure 6.2(a). The resistance of the input inductor, L_S is assumed to be negligible, and only the fundamental component of the converter waveform, V_C, will be considered. During 'motoring' the phasor diagram is as given in Figure 6.2(a), and during 'regeneration', as that shown in Figure 6.7. 'θ' is the angle between V_S and current, I_S. X_L is the reactance of the inductor L_S.

Thus,
$$\overline{V_s} = \bar{I}_s X_L + \overline{V_c} \qquad (6.1)$$

therefore,
$$I_s\angle\theta = \frac{V_s\angle 0 - V_c\angle\delta}{X_L\angle \pi/2} \qquad (6.2)$$

The complex power drawn by the converter, which has real and imaginary parts denoted by P_C and Q_C respectively, is given by:

$$P_c + jQ_c = V_c\angle\delta \times conj\left(I_s\angle\theta\right)$$

$$= V_c\angle\delta \times \frac{V_s\angle 0 - V_c\angle -\delta}{X_L\angle -\pi/2}$$

$$= \frac{V_c V_s}{X_L}\angle\left(\delta + \pi/2\right) - \frac{V_c^2\angle \pi/2}{X_L} \qquad (6.3)$$

The complex power drawn from the supply is similarly given by P_S and Q_S as:

$$P_s + jQ_s = V_s\angle 0 \times conj\left(I_s\angle\theta\right)$$

$$= \frac{V_s^2\angle \pi/2}{X_L} - \frac{V_s V_c\angle\left(-\delta + \pi/2\right)}{X_L} \qquad (6.4)$$

Separating the real and imaginary parts gives:

$$P_S = \frac{V_s^2}{X_L}\cos\left(\frac{\pi}{2}\right) - \frac{V_s V_c}{X_L}\cos\left(-\delta + \pi/2\right) \qquad = \frac{-V_s V_c}{X_L}\sin(\delta) \qquad (6.5)$$

$$Q_s = \frac{V_s^2}{X_L}\sin\left(\frac{\pi}{2}\right) - \frac{V_s V_c}{X_L}\sin\left(-\delta + \pi/2\right) \qquad = \frac{V_s^2}{X_L} - \frac{V_s V_c}{X_L}\cos(\delta) \qquad (6.6)$$

$$P_c = \frac{V_s V_c}{X_L}\cos\left(\delta + \pi/2\right) - \frac{V_c^2}{X_L}\cos\left(\frac{\pi}{2}\right) \qquad = \frac{-V_c V_s}{X_L}\sin(\delta) \qquad (6.7)$$

$$Q_c = \frac{V_c V_s}{X_L}\sin\left(\delta + \pi/2\right) - \frac{V_c^2}{X_L}\sin\left(\frac{\pi}{2}\right) \qquad \frac{V_c V_s}{X_L}\cos(\delta) - \frac{V_c^2}{X_L} \qquad (6.8)$$

The pulse converter is usually operated at unity power factor, as shown in the phasor diagrams in Figures 6.2(b) and 6.7. This allows the following expressions to be written:

$$\cos(\delta) = \frac{V_s}{V_c} \qquad (6.9) \qquad \sin(\delta) = \frac{-I_s\omega L_s}{V_c} = \frac{-I_s X_L}{V_c} \qquad (6.10)$$

Substituting (6.9) and (6.10) into equations (6.5)-(6.8) allows the following expressions to be written for the pulse converter when operating in the motoring region, with unity power factor:

$$P_s = V_s I_s \qquad (6.11)$$

$$Q_s = 0 \tag{6.12}$$

$$P_c = V_s I_s \tag{6.13}$$

$$Q_c = \frac{V_s^2 - V_c^2}{\omega L_s} = \frac{V_L^2}{\omega L_s} \tag{6.14}$$

where $V_L = I_s \omega L_s$, and is the voltage drop across the input inductance.

6.3.3 Control Procedure for the Pulse Converter

The function of the converter is to generate a voltage waveform, V_C, which is applied to the input inductor, L_S. When V_C is in phase with the supply voltage, V_S, and has equal magnitude, no current flows into the converter. By introducing a small phase shift, δ, between V_C, and V_S, it is possible to cause power to flow into the converter, or to flow out, depending on the sign of the phase shift. However under these conditions the converter is not operating at unity power factor. To achieve this, the amplitude of V_C must also be adjusted until the current and voltage phasors exist as shown in Figure 6.2(b) or 6.7. Calculating the required value of V_C is a simple task, but in order to develop and control the system it is necessary to know what limits exist on the workable values of δ and V_C. These limits are examined in section 6.3.4 and 6.3.5.

6.3.4 Control Limit on δ

From equation (6.9) $V_s = V_c \cos(\delta)$. If this is substituted into equations (6.7) and (6.8), the power flow into the converter may be written as:

$$|P_c| = \frac{V_c \cos(\delta).V_c \sin(\delta)}{\omega L_s} = \frac{V_c^2}{2\omega L_s} \sin(2\delta) \tag{6.15}$$

$$|Q_c| = \frac{V_c^2}{2\omega L_s}(1 - \cos(2\delta)) \tag{6.16}$$

From these equations it can be seen that when δ=0, both P_C and Q_C are zero. As δ increases the active and reactive power increase. P_C reaches a maximum when $\delta = \pi/4$. At this point P_C=Q_C.

Note that even though there is reactive power flow into the converter itself, the current is drawn from the supply at unity power factor. If δ is increased above this value P_C decreases, but Q_C

continues to increase. This is not a useful region for control purposes since not only are the converter losses increased by the excessive flow of reactive power, but very large values of V_c are required to maintain unity power factor. This would be wasteful of the modulation range of the converter. Thus in practice the useful operating range is:

$$0 \leq \delta \leq \frac{\pi}{4}.$$

6.3.5 Control Limit on The Converter Fundamental, V_c

Examination of Figure 6.2(b) shows that the minimum value of V_c occurs when V_c and V_s are in phase (and hence have equal magnitude). Note that this assumes that unity power factor is maintained throughout. Although current would flow if V_c were made smaller than this value, it would not be possible to achieve unity power factor operation no matter what value of δ were used. Thus $V_{c_{min}} = \sqrt{2}V_s$

The practical maximum of V_c occurs for maximum power transfer, when $\delta = \pi/4$. Thus, $\frac{\sqrt{2}V_s}{\cos(\pi/4)} = 2V_s$. However, the converter may not be rated to carry the full theoretical maximum power, in which case $V_{c_{max}}$ will be defined using equation (6.1) as:

$$V_{c_{max}} = \sqrt{V_s^2 + \left(I_{s_{max}} X_L\right)^2} \tag{6.17}$$

where,

$$I_{s_{max}} = \frac{P_{max}}{V_s} \tag{6.18}$$

P_{max} is the maximum input power.

6.3.6 Design of the Link Capacitor

The link capacitor specification is very important since it has a significant bearing on the overall system efficacy and is a fairly expensive item; thus, its rating should not be greater than the required minimum. In this section an equation defining the minimum is derived. Consider the converter system as shown in Figure 6.8. It is assumed that the DC link voltage has negligible ripple, the input current is perfectly sinusoidal, and only the fundamental component of the converter voltage, V_c, is accounted for.

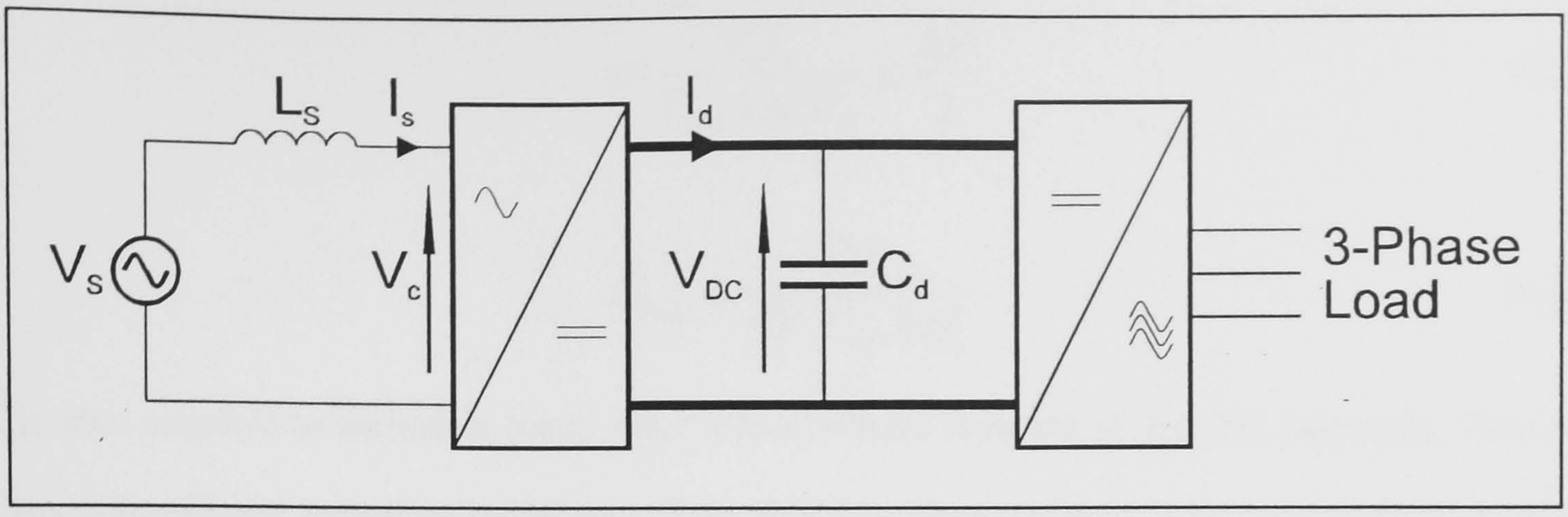

Figure 6.8 Pulse Converter/Inverter System

Thus,
$$i_s(t) = \sqrt{2}\tilde{I}_s \sin(\omega t) \tag{6.19}$$
$$v_c(t) = \sqrt{2}\tilde{V}_c \sin(\omega t - \delta) \tag{6.20}$$

Where $\tilde{I}_S$ and $\tilde{V}_C$ are the RMS values of i_S and v_C respectively. Let the link voltage be V_{DC}, and the link current be $i_d(t)$. Because there are no storage components in the converter, there must be instantaneous power balance between its input and output, i.e.:

$$i_s(t) \times v_c(t) = i_d(t) \times V_{DC} \tag{6.21}$$
$$\Rightarrow i_d(t) = \frac{\sqrt{2}\tilde{V}_c \sin(\omega t - \delta) \times \sqrt{2}\tilde{I}_s \sin(\omega t)}{V_{DC}} \tag{6.22}$$
$$\equiv \frac{\tilde{V}_c \tilde{I}_s}{V_{DC}}\left[\cos(\delta) - \cos(2\omega t - \delta)\right] \tag{6.23}$$

Thus, under these idealised conditions, the link current consists of a DC component which varies with δ, and a component at twice the supply frequency. The twice supply frequency component causes a ripple voltage to appear on the link capacitor. The maximum allowable ripple determines the minimum capacitor value. The ripple specification depends on the operating requirements of the pulse converter and 3-phase inverter. Let f_S be the supply frequency, C_d be the link capacitance, $i_{d2}(t)$ be the 2nd harmonic link current, and the peak to peak ripple be ΔV. To meet the ripple specification;

$$\left|i_{d2}(t)\right| \times X_{C_d} \leq \frac{\Delta V}{2} \tag{6.24}$$

$$\Rightarrow \frac{\tilde{V}_c \tilde{I}_s}{V_{DC} 4\pi f_s C_d} \leq \frac{\Delta V}{2} \tag{6.25}$$

$$C_{d_{\min}} \geq \frac{\tilde{V}_c \tilde{I}_s}{\Delta V . V_{DC} 2\pi f_s} \tag{6.26}$$

It is also possible to include a tuned filter which effects removal of the 2nd harmonic. This can allow a significant reduction in the size of the link capacitor required. In practice a link capacitor is needed even if a 2nd harmonic filter is used, in order to filter the higher frequency harmonics which exist in a practical converter.

6.3.7 Specification for the Input Inductance, L_S

This is an important parameter and is affected by several design criteria. On an AC-supplied rail vehicle an auxiliary converter would usually be powered via a step-down transformer. Thus it is not necessary to provide a separate input inductance, since it may be realised by setting the leakage inductance of the transformer to the appropriate value. If the design value of L_S is large, then the cost of the transformer rises significantly which places an upper limit on L_S. As the value of L_S gets smaller the Psophometric Current and Total Harmonic Distortion figures start to rise, which determines the lower limit on L_S. In section 6.5, graphs are presented showing typical variation of these parameters with the value of input inductance.

6.4 Soft-Switching Pulse Converter Control

6.4.1 Introduction

As was the case for the Resonant DC Link Inverter, the output of the pulse converter consists of a sequence of voltage pulses which are used to synthesise the desired waveform. However there is an important difference in the selection procedure for the pulses. Because the pulse converter is only single phase, and consists of two active 'legs' the control algorithm may implement '+1', '0', and '-1' states, as opposed to the inverter output stage where independent control is only achievable over one leg, allowing simply '+1' and '-1' states to be selected. Thus the voltage waveform is made up of pulses and zeros as shown in Figure 6.9. During zero voltage periods the

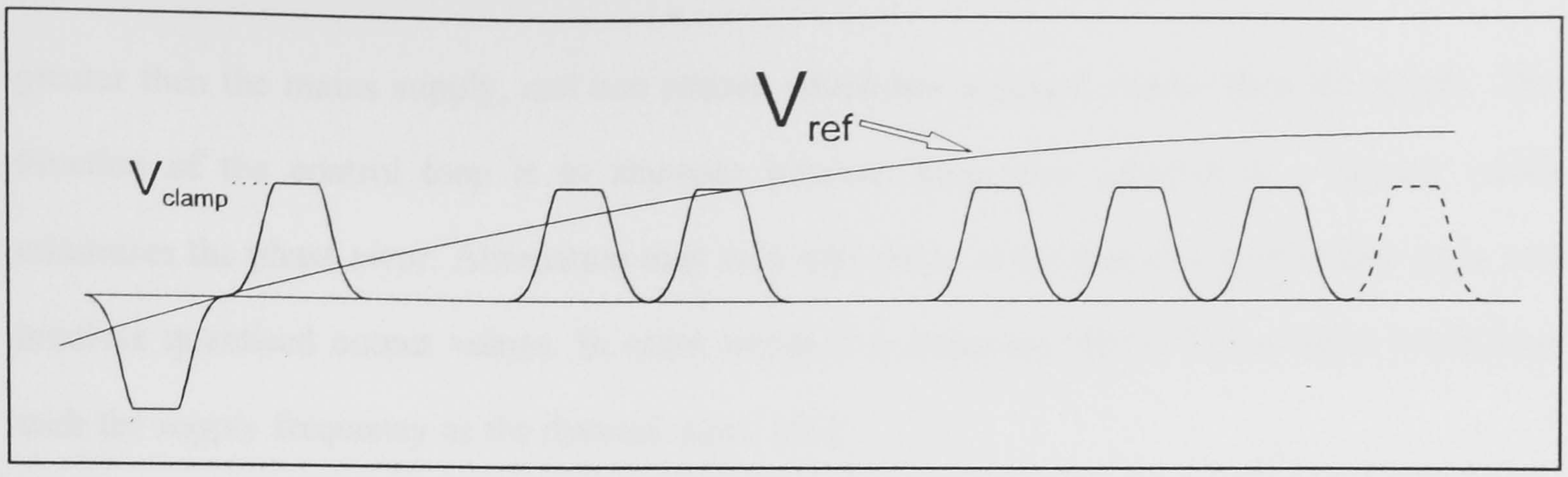

Figure 6.9 Synthesis of Waveforms

current 'free-wheels', being driven by L_S and circulating through the converter. Throughout the period 0°-180° of the voltage waveform, only states '0' and '+1' are allowed. By virtue of symmetry, only the states '0' and '-1' are allowed during the period 180°-360°. This gives the optimum harmonic control for a single phase inverter [52].

Modulation may be achieved 'on-line' using Sigma Delta style circuits however as discussed previously, this does not allow complex harmonic manipulations to be implemented. Therefore the problem of large-scale combinatorial optimisation exists once more. This may be solved using Simulated Annealing as was explained in Chapter 4. A clear difference exists however, between the pulse converter and the Resonant DC Link Inverter, and that is the need for the pulse converter to synchronise itself to the supply waveform, whilst also maintaining the harmonic control described above. This aspect of the control procedure forms the subject of this section.

6.4.2 Supply Waveform Synchronisation

As stated above, one of the key requirements for a pulse converter such as this is the ability to track the mains supply voltage waveform. In a 'conventional' PWM system with unconstrained switching angles, this is not too much of a problem. However, in a discrete pulse system like the Resonant DC Link converter the overall period of the generated waveforms is also constrained to discrete values. The length of the pulses on the resonant link has an arbitrary relationship to the supply frequency. As a consequence, it is necessary to continually correct for phase error between the synthesised waveform and the supply waveform. In the steady state, this control may be implemented by identifying from a table of possibilities, one pulse pattern which has a period

greater then the mains supply, and one pattern which has a period shorter than the supply. The function of the control loop is to alternate between these two patterns in a manner which minimises the phase error. Alternation may only take place at the end of a synthesised cycle and involves quantised output values. In other words it is behaving like a Sigma-Delta Modulator with the supply frequency as the demand input. [50]

At the same time as deciding the overall period of the generated pattern, the controller must determine its fundamental magnitude and harmonic properties. These are intrinsic qualities of the pattern. Consequently it is necessary to generate a table of patterns for each desired value of fundamental. To give the appropriate harmonic properties, a cost function and optimisation procedure such as Simulated Annealing should be used in the formulation of the tables of modulation patterns.

The Sigma-Delta controller described above works well in the steady state. However the supply frequency may change, or the resonant pulse length may vary due to changes in clamping voltage, or loading of the converter. This alters the average number of pulses needed in each supply cycle. Simulations have shown that for a 20kHz link frequency, pulse pattern length may vary over a range of 10-20 as the load on the converter is increased. Changes such as this can be detected by the controller by examining the phase difference between the generated pattern and the supply waveform. This is most easily done at the zero-crossing points of the supply. To prevent the Sigma-Delta controller from saturating, the two patterns used must be updated with new ones which are either longer or shorter, thus allowing correct tracking of the supply to continue. This system of operation has the characteristics of a Digital Phase Lock Loop (DPLL) [71]. To maintain stability of this loop a delay may need to be introduced. The delay causes the system to wait a number of cycles before correcting a phase error, and thus behaves as a low-pass filter. Figure 6.10 shows a block diagram of the phase-lock system. It can be seen from the diagram that it exists as two loops; the inner Sigma-Delta loop, and the outer bandwidth-limited loop to account for transient conditions. Although shown as separate blocks, the phase-lock system, and pattern generation may be implemented on a single microprocessor.

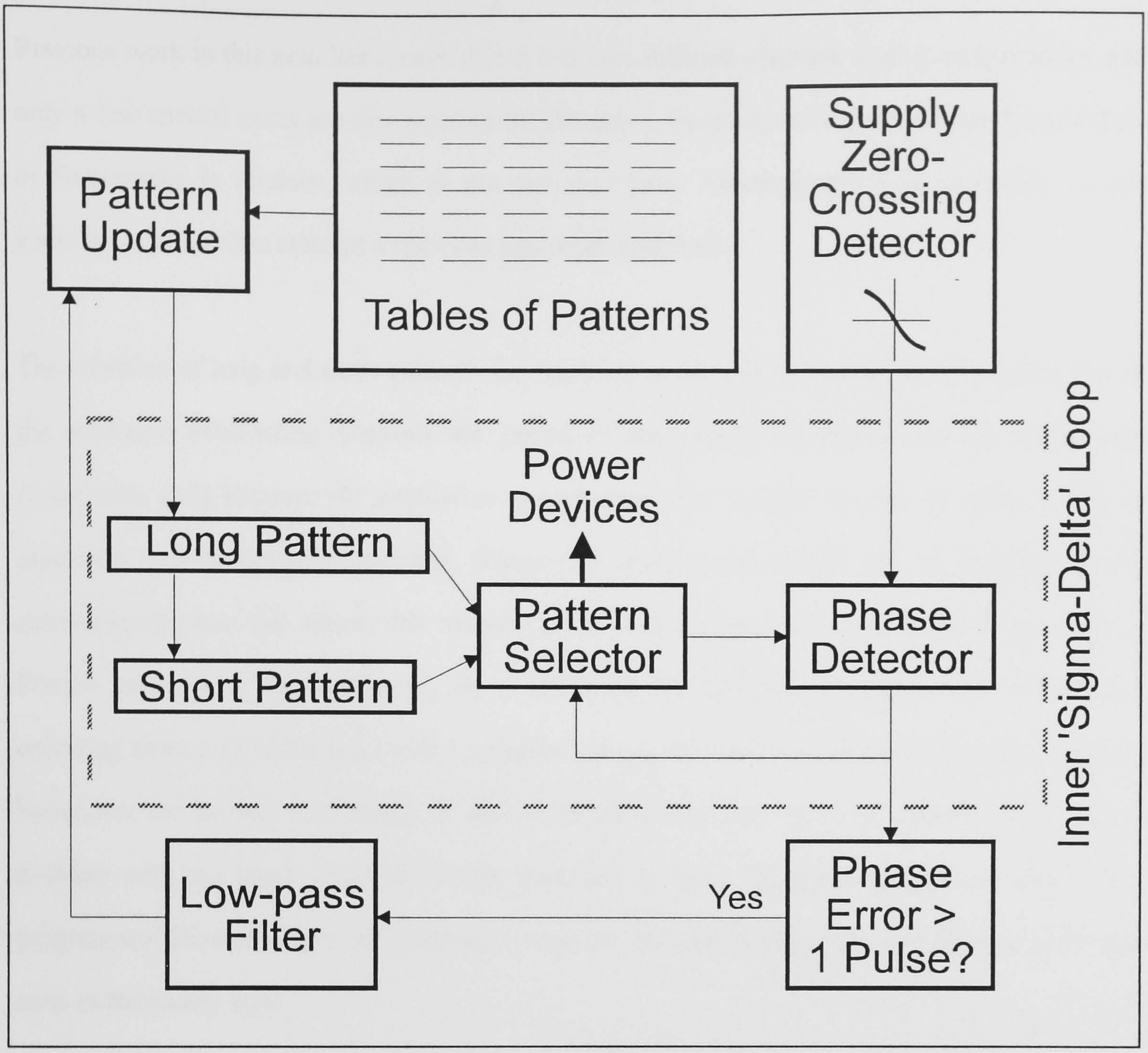

Figure 6.10 Block Diagram of the Phase-Lock System

6.4.3 Analysis and Simulation of the Phase-Lock System

In tracking the supply voltage waveform the controller will normally select the short pattern for one cycle, followed by several cycles of the long pattern, or vice versa. The implication here is that there are modulations of the converter taking place at less than the supply frequency. In other words sub-harmonics may be generated. For this reason it is of interest to be able to model the converter to assess the size of these sub-harmonics, which may experience very low values of impedance and thus cause large sub harmonic currents to flow. Considering only the fundamental of the synthesised voltage waveforms, the converter behaves like an oscillator whose frequency is modulated. This modulation is restricted to the end point of each synthesised cycle. This situation is well known in the communications field as Continuous Phase Frequency Shift Keying [72].

Previous work in this area has shown that it is a very difficult situation to analyse spectrally, and only a few special cases are discussed in the literature. Normally it is assumed that the selection of frequencies is random, which is not the case here. Consequently it is preferable to use simulation rather than attempt a rigorous analytical approach.

The selection of long and short patterns for synthesis is normally a non-repetitive process due to the arbitrary relationship between the period of the supply waveform and the synthesised waveforms. [50] Because the simulation is performed over a finite number of cycles however, repetition is automatically assumed, though the more cycles which can be included in the simulation the less this affects the results. Table 1 shows part of the spectrum obtained from Fourier analysis of the voltage V_c for a simulation of converter operation over 100 cycles, operating from a 15.6kHz link, with a nominal 1.0 p.u. fundamental. It can be seen that the sub-harmonics are in fact very small. It should be noted that sub harmonic oscillation is only a problem with the input stage due to the necessity to track the mains frequency. Where pre-programmed Discrete Pulse Modulation is used on the output stage then sub harmonics do not exist in the steady state.

Frequency p.u.	Magnitude p.u.
0.1	0.000037
0.1111	0.000020
0.1250	0.000011
0.1428	0.000006
0.1666	0.000030
0.2	0.000013
0.25	0.000102
0.3333	0.000008
0.5	0.000001
1.0	**1.009620**
3.0	0.007880
5.0	0.005952
7.0	0.009674
9.0	0.000051
11.0	0.017959

Table 1 Spectrum of Simulated Converter Voltage (V_C)

6.5 Comparison of Converter and Diode-Bridge Input Stages

Many converters have diode-bridge input stages based on the topology shown in Figure 6.11(a). This circuit utilises a simple LC filter but many other configurations are possible. Figure 6.11(b) shows the typical distorted line-current waveforms which may flow using this type of input stage.

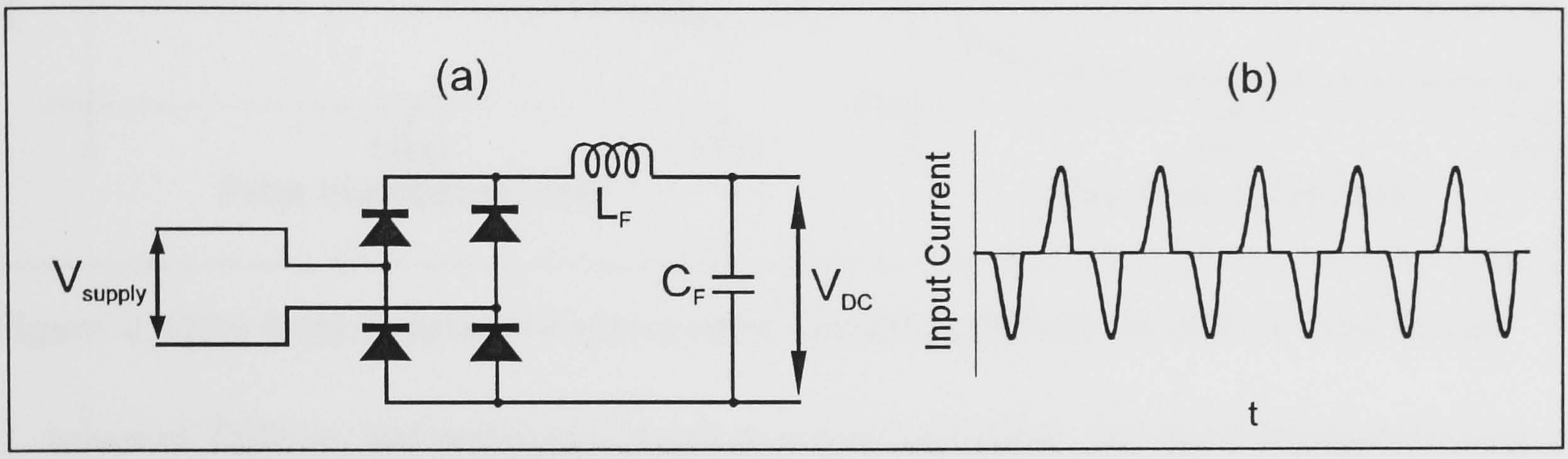

Figure 6.11 Diode-Bridge input stage and current waveform

This waveform clearly has poor attributes as far as Total Harmonic Distortion (THD) and psophometric current (I_p) are concerned. Figure 6.12 allows a fuller comparison to be made. In this example, converter and diode-bridge input stages have been simulated and the respective

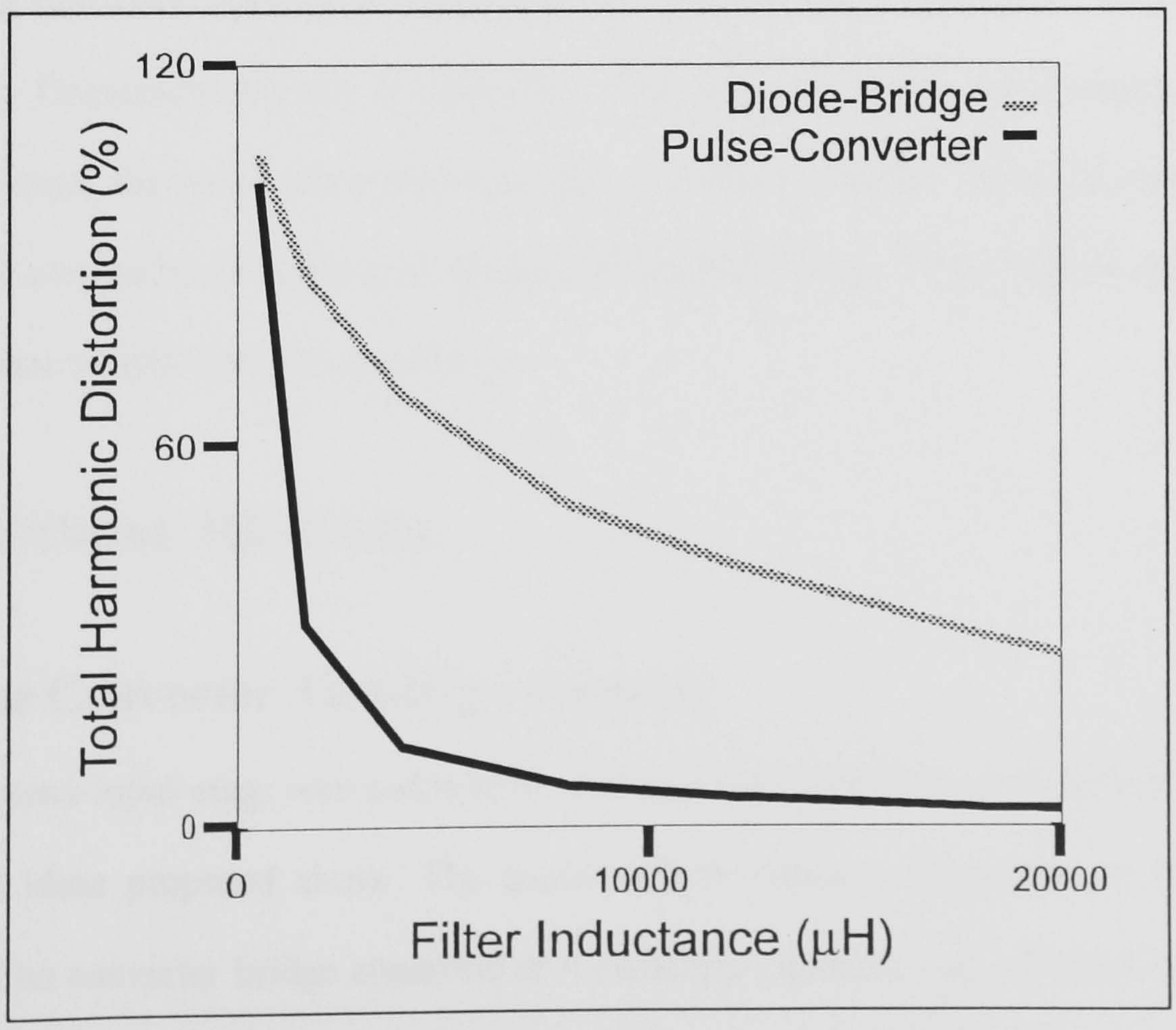

Figure 6.12(a) Graph of THD vs. Filter Value (By Simulation)

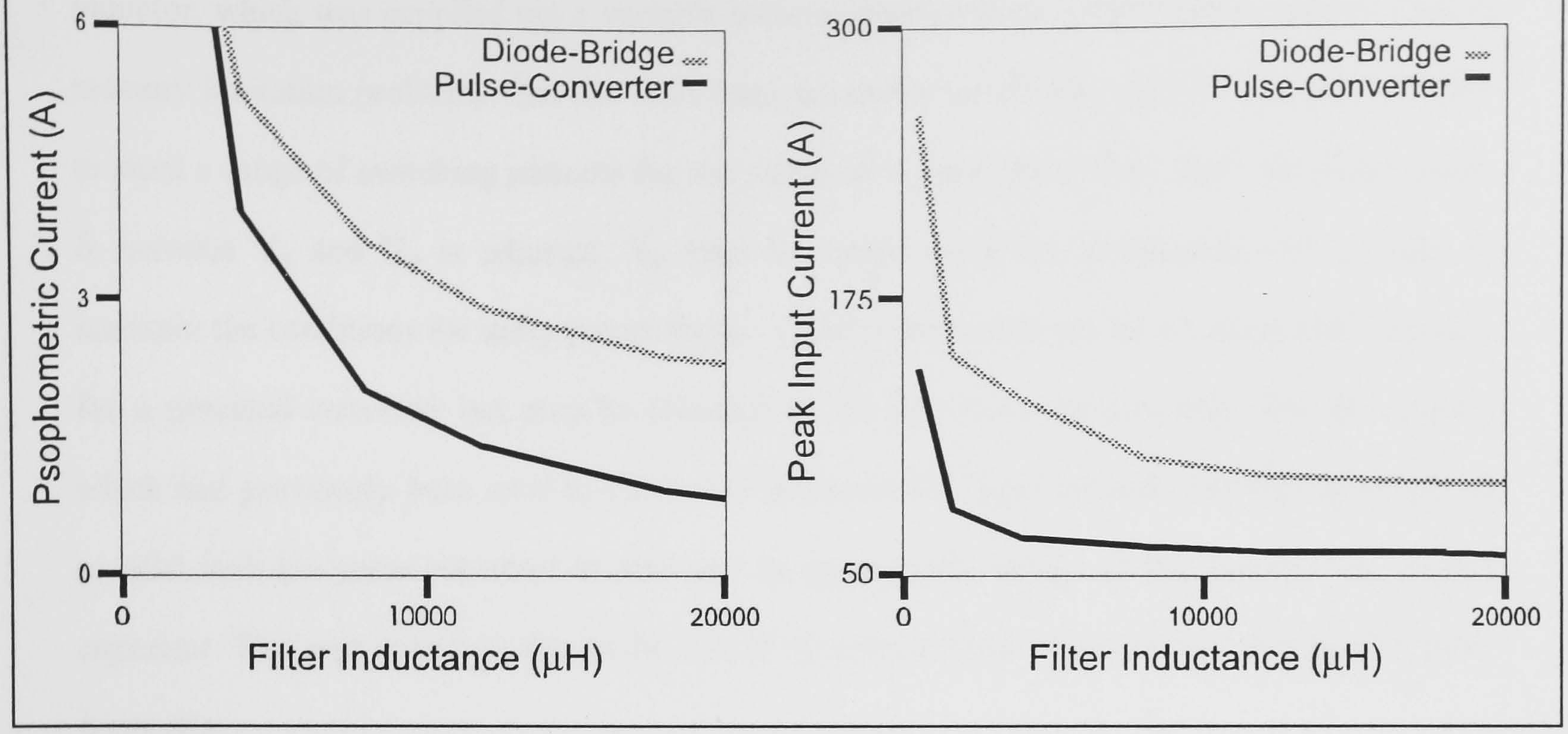

Figure 6.12(b) & (c) Graphs of Psophometric Current and Peak Current vs. Filter Value

values of THD, I_p, and peak input current have been calculated. This has been repeated using various values of filter inductance, whilst varying the filter capacitance to maintain a constant resonant frequency of 8Hz for the filter arrangement. In each case, a resistive load of 40kW was assumed, supplied from a 1000V AC source. In the case of the pulse converter-input circuit, the 'filter' inductance is the line inductor. It can be seen from the graphs in Figures 6.12(a), (b) & (c) that the pulse converter-input circuit possesses significantly lower values of THD, I_p, and peak input current. Conversely it could be said that whilst maintaining the same values of THD, I_p, and peak current, the pulse converter-input type requires a smaller value of inductance. The reduced peak current has a bearing on device and heatsink rating. These factors are particularly important where weight and size are critical.

6.6 Practical Results

6.6.1 Pulse Converter Test-Rig - General

A pulse converter input-stage was added to the resonant DC Link Inverter described in Chapter 5, to verify the ideas proposed above. The circuit had the same configuration as that shown in Figure 6.6. The converter bridge consisted of 4 switching modules, two of which can be seen in the side-view of the test-rig shown in Figure 5.19. The converter was fed via a 170mH air-cored

inductor, which was supplied via a variable autotransformer from a 240V mains supply. Due to memory limitation problems with the 8051 microcontroller which was used, it was only possible to store a range of switching patterns for *one* value of V_c at a time. Thus when the phase angle, δ, between V_s and V_c is adjusted, V_s must be varied using the autotransformer in order to maintain the conditions for unity power factor. Clearly this would not be an acceptable situation for a practical converter but may be tolerated in the laboratory environment. The DC supply which had previously been used to power the Resonant DC Link Inverter was left in circuit, in parallel with the pulse converter to maintain an appropriate voltage on the Inverter DC supply capacitor. This was necessary due to the lack of dynamic control of power flow through the pulse converter.

Figure 6.14 shows a close-up of one of the switching modules, and Figure 6.15 shows the microcontroller board. The controller program for the pulse-converter was interrupt-driven, the two interrupt sources being the zero-voltage crossing strobe of the Resonant DC Link, and a zero-voltage crossing detector for the mains supply. The flow-diagram in Figure 6.13 outlines the mode of operation of the controlling software.

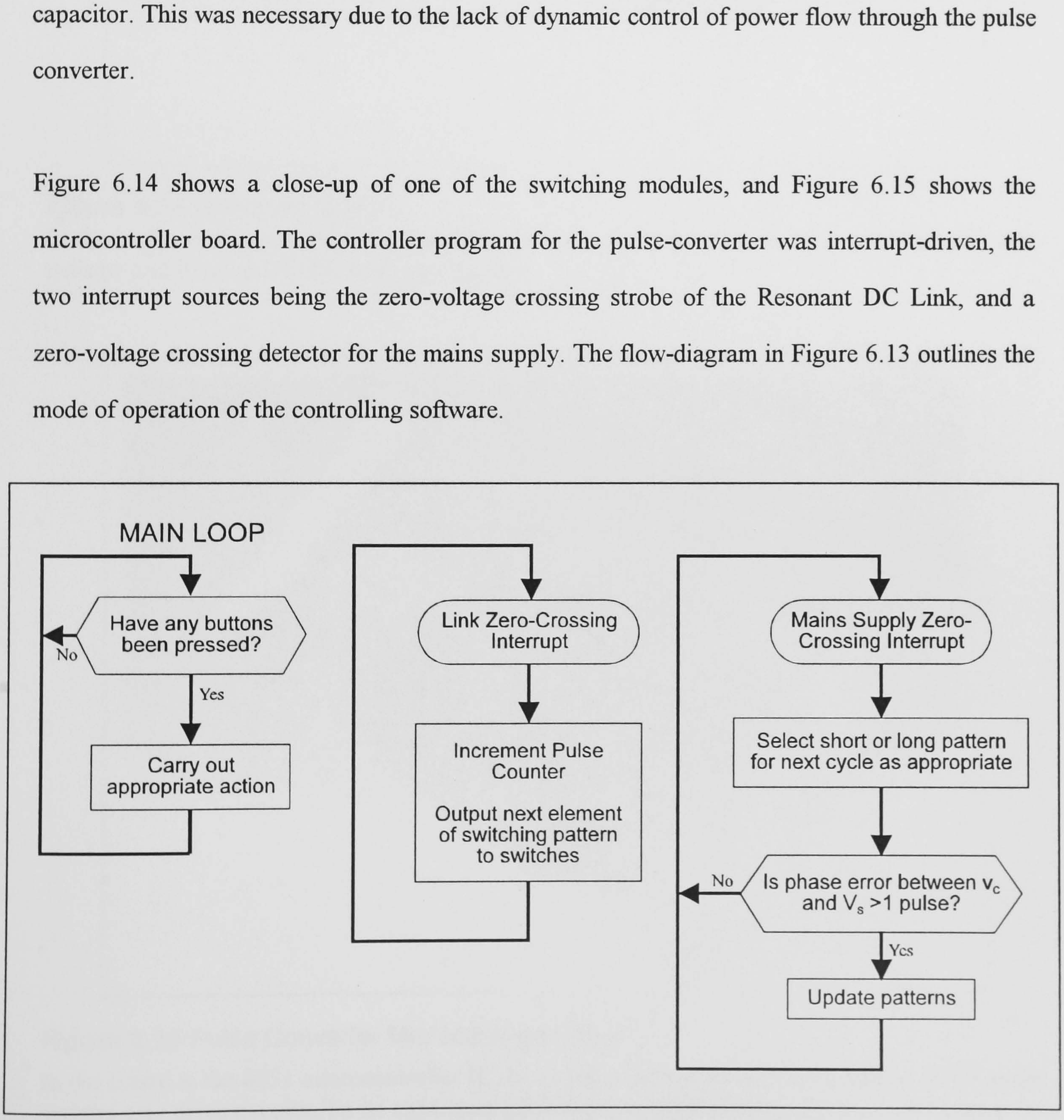

Figure 6.13 Outline of the Pulse Converter Interrupt-Driven Control Software

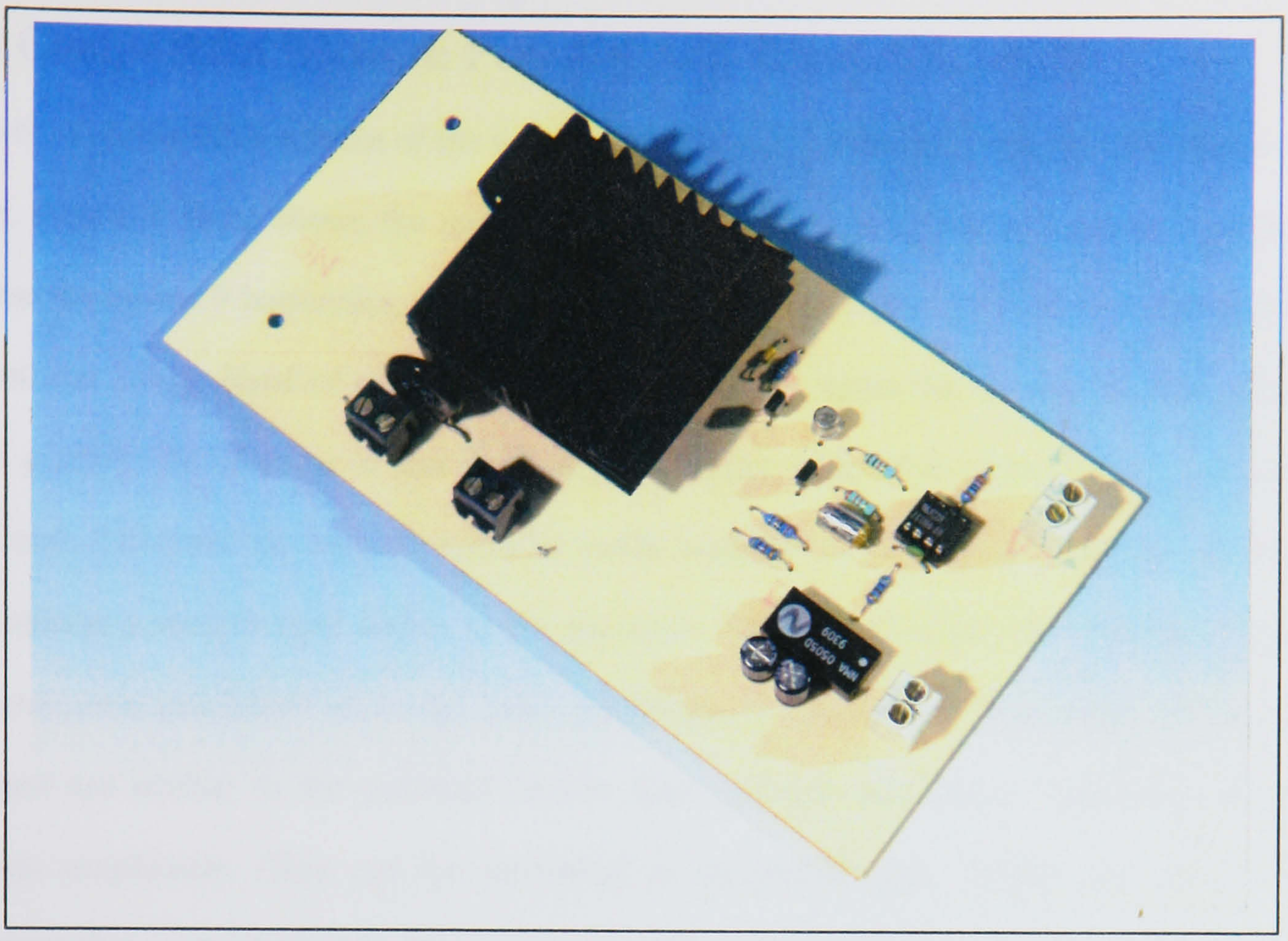

Figure 6.14 Switching Module

In the centre is the power device heatsink. To its right can be seen the drive circuit, with opto-isolator and floating DC-DC converter supply.

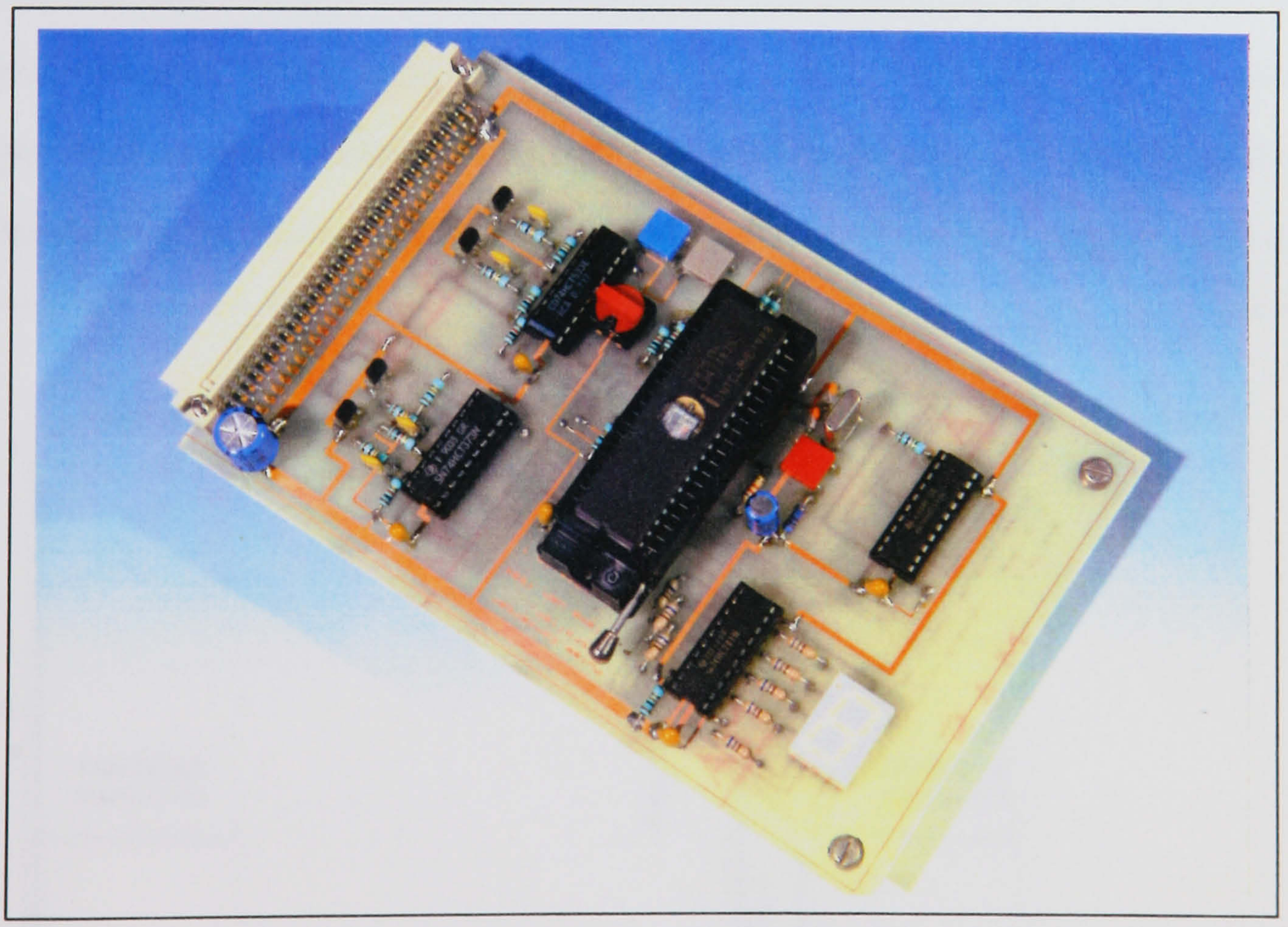

Figure 6.15 Pulse Converter Microcontroller Board

In the centre is the 8051 microcontroller IC, to its left a red rotary switch for setting the 'δ' angle, and the gate drive circuits. To its right is an LED display which indicates the converter status.

6.6.2 Comparison Between Practical and Simulated Results

Figure 6.16 shows the spectrum of the voltage waveform, v_c, obtained from the input-stage of the test-rig. Figure 6.16(a) shows the spectrum obtained when implementing a pattern designed to minimise the lowest 9 harmonics, whilst demanding a nominal 1 p.u. fundamental. Figure 6.16(b) demonstrates how a band of harmonics may be minimised, again the nominal fundamental is 1 p.u. In practice the increase in low frequency harmonics which this causes would probably be undesirable. However the process could be easily modified to reduce low frequency harmonics *and* minimise a remote band higher in the spectrum. Figure 6.17 shows the spectra derived by using computer simulation under the same conditions. It can be seen that whilst the harmonic envelopes are similar to the practical results there is some discrepancy regarding individual harmonic amplitudes. This can be attributed to several factors. Firstly the use of 8051 microcontrollers, which have a 1μs cycle time. Thus when performing many instructions, as required by the control loops, the computation time can become comparable with the period of link resonance. As a consequence an appreciable degree of error exists in the pattern selection, giving harmonically non-ideal characteristics. This situation could be alleviated by using a faster processor such as a Digital Signal Processor. Another source of discrepancy is the Spectrum Analyser which introduces measurement errors when analysing harmonics of very low amplitude. A further factor is the effect of pattern repetition which is a function of the method of simulation.

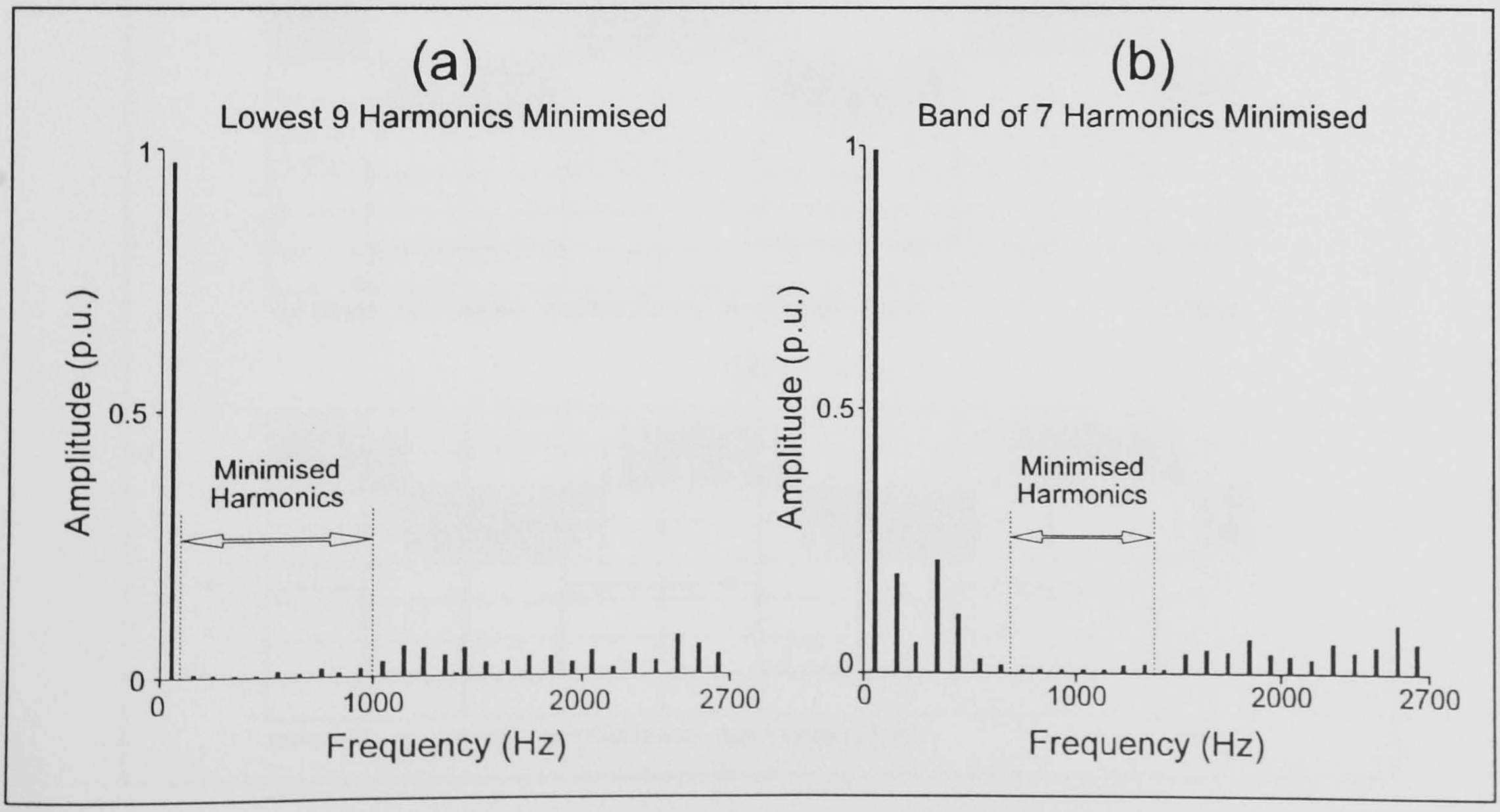

Figure 6.16 Practically Measured Voltage Spectra of Converter-Input Stage

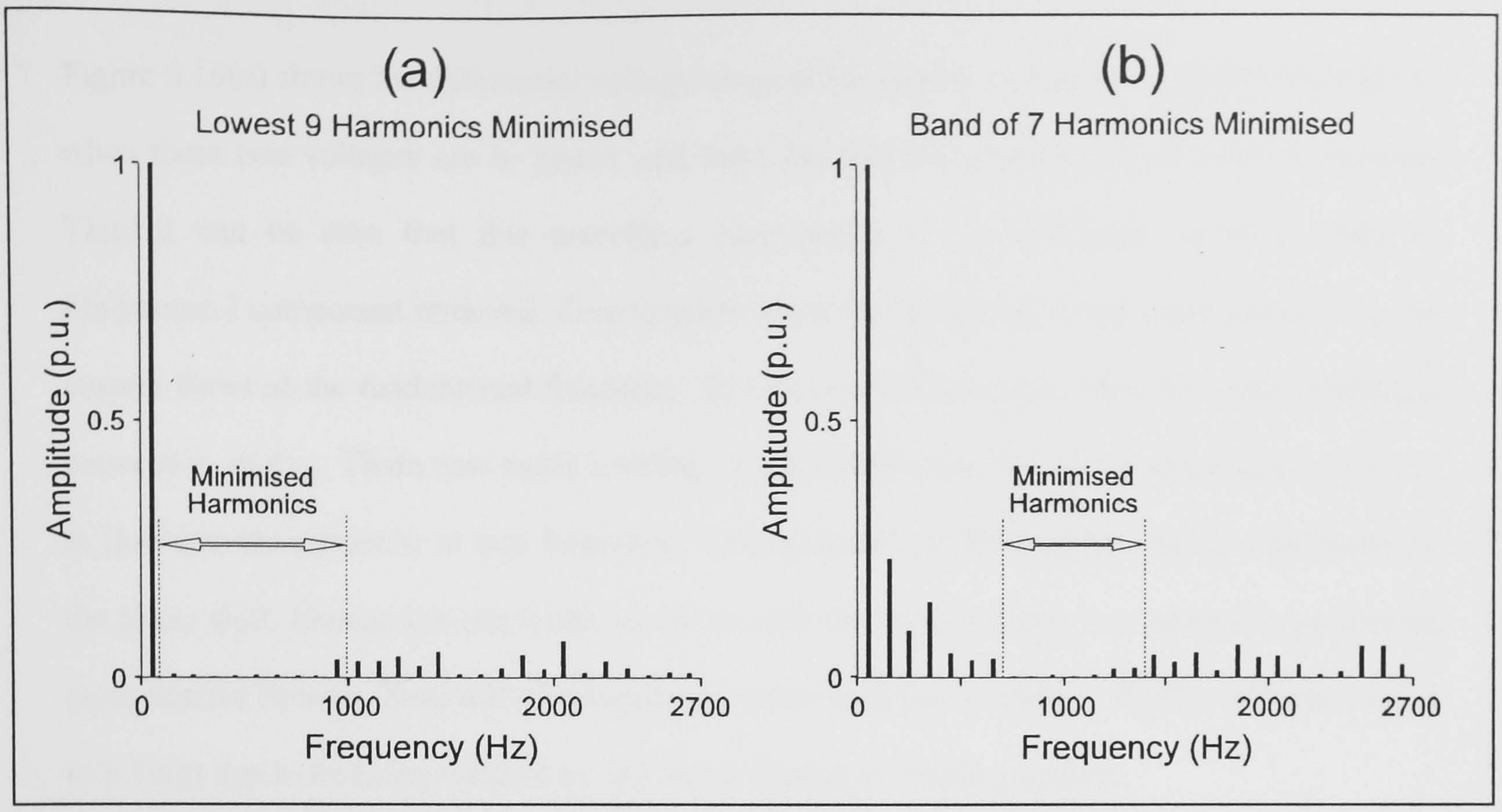

Figure 6.17 Voltage Spectra for Converter-Input Stage Derived by Simulation

6.6.3 Measured Test-Rig Waveforms

In Figures 6.18(a) and (b) waveforms of the pulse converter voltage, v_c, and the mains supply zero-crossing strobe can be seen. These were measured on the test-rig. Figure 6.18(a) shows v_c in phase with the mains supply, but in Figure 6.18(b) a phase shift (i.e. 'δ') of around 35° has been introduced.

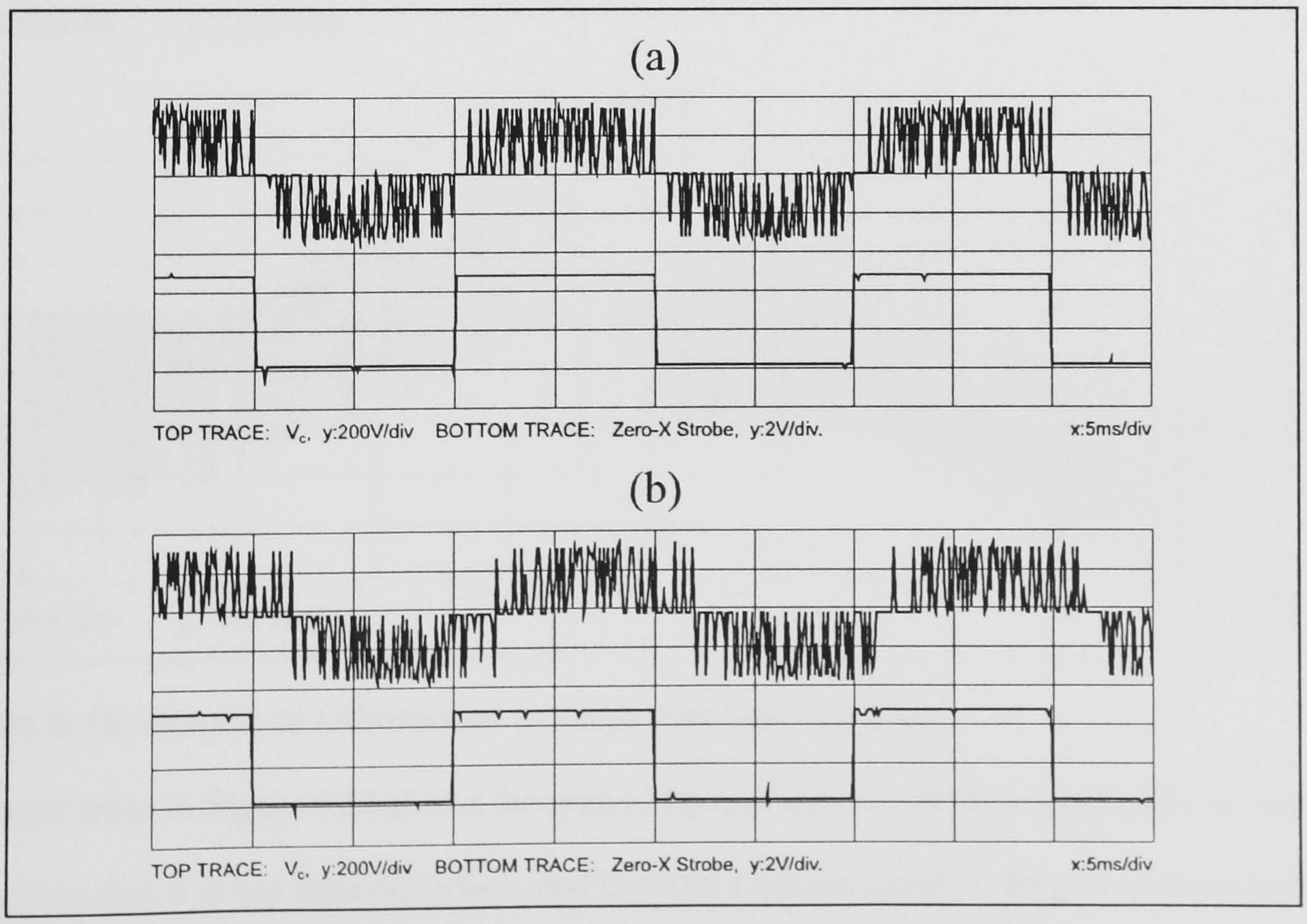

Figure 6.18 Graphs of v_C, and mains zero-crossing strobe

Figure 6.19(a) shows the differential voltage between the supply, v_S, and the converter voltage, v_C when these two voltages are in phase, and have fundamental components of equal magnitude. Thus it can be seen that this waveform corresponds to the converter waveform with its fundamental component removed. Consequently when this is applied to the input inductor L_S, no current flows at the fundamental frequency. In Figure 6.19(b) a phase shift has been introduced between v_S and v_C. There now exists a voltage at the fundamental frequency which causes current to flow into the converter at that frequency. The harmonics of the fundamental are unaffected by the phase shift. During this test a relay in series with the input inductor was opened to prevent an input current flowing. Note that the switching pattern in Figure 6.19(b) is slightly different to that in 6.19(a) due to its being updated by the mains frequency-tracking system.

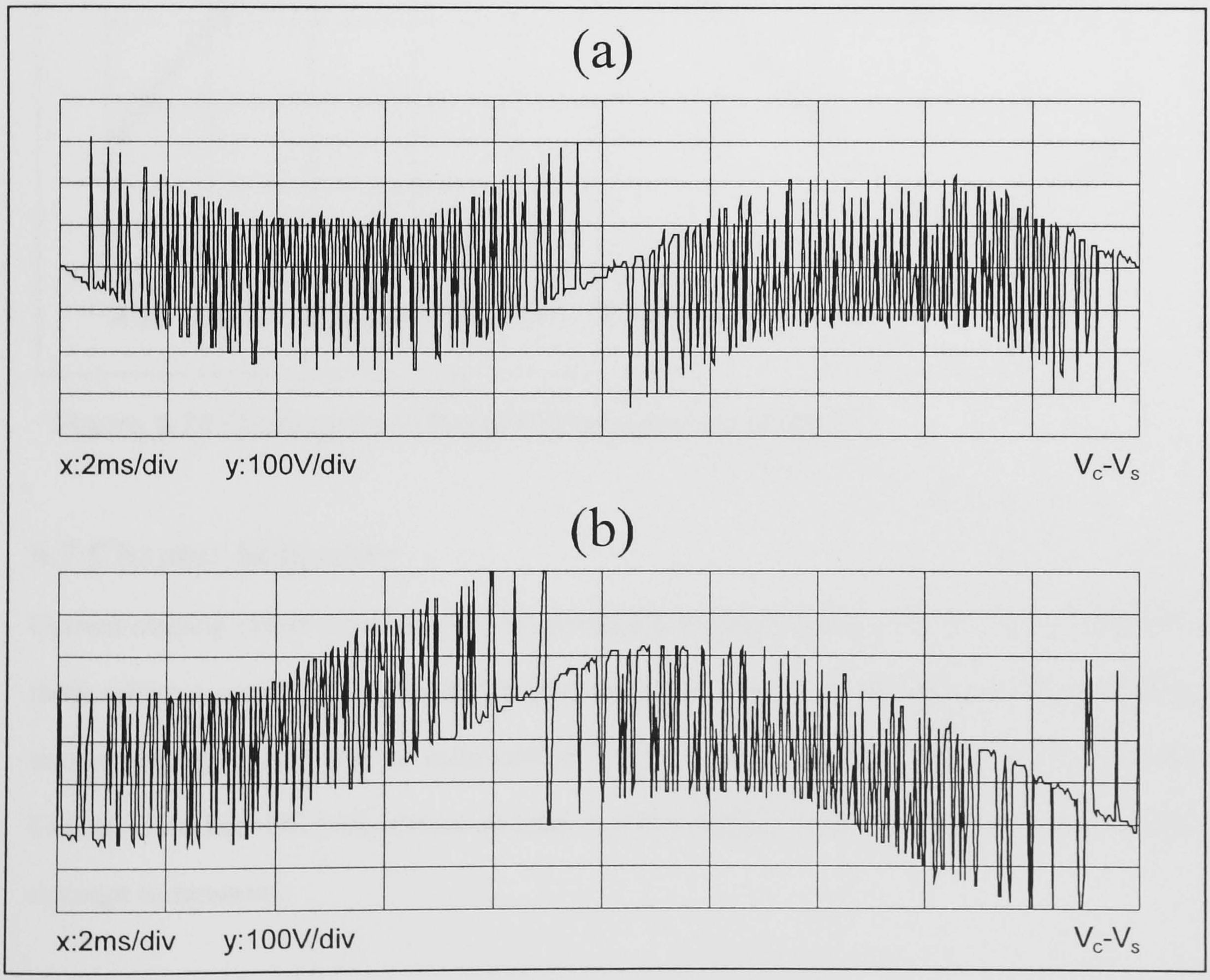

Figure 6.19 Graphs of Differential Voltage Between v_C & v_S

The lower trace in Figure 6.20 shows the typical form of the current flowing into the converter. It can be seen that it is has little distortion, and in phase with the supply voltage waveform (which is depicted in the upper trace) creating the conditions for high power factor. The power factor was

measured under these conditions at 0.99 using an AC power analyser. The distorted appearance of the voltage waveform was due to external harmonic pollution of the laboratory supply and could not be corrected.

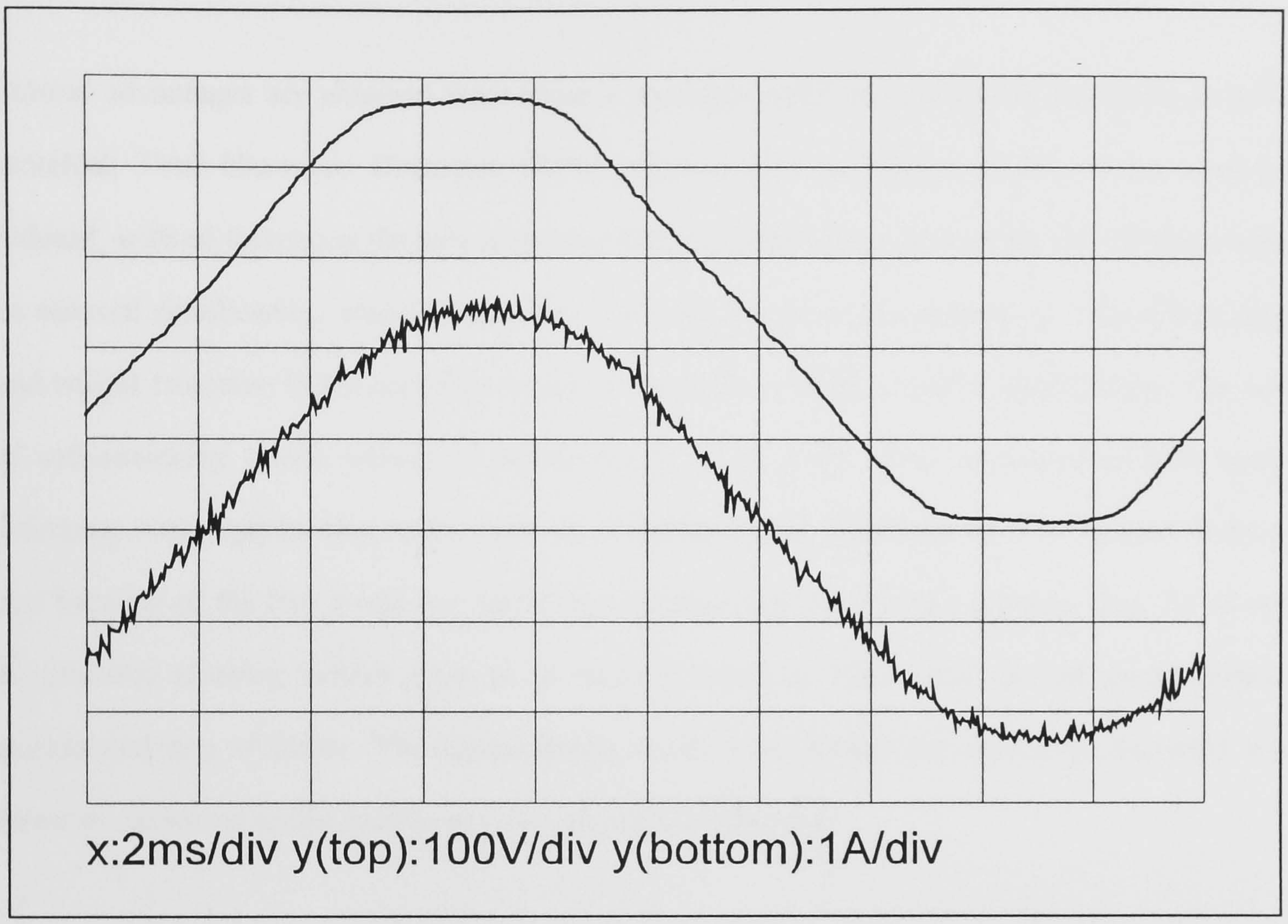

Figure 6.20 Oscillogram of Supply Voltage and Input Current

6.7 Chapter Summary

Current-shaping circuit topologies can be operated in a soft-switching, Discrete Pulse Modulation mode whilst maintaining the benefits of good harmonic control. A 'conventional' hard-switching current-shaping circuit may be incorporated into the design of converters such as the Actively Clamped Resonant DC Link Inverter to achieve soft-switching without the addition of any further resonant components.

Control over specific harmonics or complex functions of the harmonic amplitudes may be achieved at the input side of a converter using a pre-programming method. Simulated Annealing has proved to be a reliable way of searching for appropriate modulation patterns. When using pre-calculated patterns, it is necessary to store a table containing various pattern lengths to

account for changes in supply frequency and resonant pulse length. The control loop used to select the patterns has the characteristics of a Digital Phase Lock Loop, and steps must be taken to ensure its stability.

Several advantages are obtained from using a current-shaped input stage whether hard or soft-switched; Total Harmonic Distortion (THD), peak current and psophometric current may be reduced, without increasing the size of passive filtering components. Indeed the size of filters may be reduced significantly, whilst maintaining the same harmonic characteristics. This allows size and weight reduction in the converter which is especially critical in certain applications. The use of soft-switching allows additional improvements to be made when compared to their hard-switching counterparts. Due to the reduced switching losses, heatsinks may be reduced in size, and because of the low losses per switching operation, the switching frequency may be raised significantly allowing further gains to be made in terms of THD, peak current, psophometric current and size of filters. The improvements made by increasing the switching frequency are however, tempered by the need to use discrete pulse modulation.

Chapter 7

Issues of Design and Performance

7.1 Introduction

The design and performance trade-offs when specifying components for the Resonant DC Link Inverter are extremely complex. This is in addition to the numerous comparisons which may be made in attempting to quantify the improvements which soft-switching offers over its hard-switching counterpart. In this chapter the key design issues are examined, together with an analysis of the impact they have on the overall performance of a converter. This begins with a review of the selection procedure for the resonant components, L_r, and C_r. The values of these two components have far-reaching consequences for the efficiency and harmonic performance of a converter and thus good selection is crucial to a successful design.

Comparisons are made between resonant soft-switching converters, and hard-switching converters both in terms of device rating and performance indicators such as Total Harmonic Distortion. This allows an evaluation of the benefits obtained from the use of Resonant DC Link Inverters which may then be weighed against their increased complexity and difficulty of design.

7.2 Selection of L_r and C_r

7.2.1 Qualitative Discussion

The selection of L_r and C_r may be considered in two stages. The first is to select the *ratio* between their values. This determines the link operating frequency and thus the harmonic qualities of the generated waveforms. This will be discussed later in this chapter. The second stage is to determine the actual values of L_r and C_r. The main factor affecting this decision is loss, both in the resonant components and in the switching devices. These losses are quantified in

section 7.2.2. Chen *et al* [69] suggested that in general, larger values of C_r reduce the losses in the main converter components by reducing *dv/dt*; however, the clamp losses are increased by the increased circulating currents which result. Use of a large value for C_r dictates a small value of L_r (for a given resonant frequency) which additionally leads to higher values of *di/dt* in the clamp circuit. This increases conduction loss in the clamp switch due to an effect which has been termed 'conductivity modulation lag'. If allowed to become too large, the losses in the clamp switch can contribute a significant proportion of overall converter losses and thus require quite careful containment.

In order to effect containment of clamp losses it is possible to operate RDCLIs with circulating currents in the resonant components which have an amplitude less than the peak of the load current. This is achieved by reducing the size of C_r. A problem associated with doing this is that modulation of the link current due to changes of switch positions in the output stage can lead to high *dv/dt* on C_r, which detracts from the conditions required for zero voltage switching. As a consequence, the losses in the main devices increase. Additionally if C_r is made very small, then L_r must be very large which has implications for its losses and also for its size and weight which may become appreciable. The modulation of the link current causes sudden rises in the voltage on C_r, or extension of the periods of link zero-voltage. Either way this leads to link voltage waveform distortion. This is an important consideration when implementing pre-programmed harmonic control schemes such as that described in Chapter 4, as the distortion leads to modulation error and the increase in magnitude of otherwise minimised harmonics. This is a further reason for increasing the size of C_r.

Losses in the clamp circuit have consequences extending further than just efficiency of the converter. The losses must be accounted for in the converter operation in order to maintain the link resonance. This may be done by allowing momentary 'short circuits' of the resonant bus during zero-volt periods, to boost the current in L_r. This however, constitutes a form of link waveform distortion which increases as the losses increase, and lowers the effective operating frequency of the link. An alternative is to provide an auxiliary supply to maintain constant energy

on the clamp capacitor. Clearly the greater the losses, the greater the capacity the auxiliary supply must have, which adds weight, size and cost.

It was argued by Smit *et al* [36] that the criteria for selecting L_r and C_r should be to minimise the overshoot of the link voltage during modulation of the link current. This is not an appropriate approach for the Clamped Resonant DC Link Inverter, but was suitable for the unclamped GTO inverter being investigated by Smit *et al*. They suggested that the resonant current be of the same magnitude as the maximum link current by a suitable choice of L_r and C_r to control the overshoot. Because Smit's inverter employed GTOs with a large voltage withstand capability, no clamping was necessary which resulted in a simple, rugged topology. In many cases however, the cost and gating complexity of GTOs would preclude their use.

It has been shown [73] that the kVA rating of the resonant inductor may be minimised by adjusting the inductance value such that its reactance is the same as the link load impedance. It may not in practice give the optimum design solution by selecting L_r in this isolated manner. However, it may be seen that the curves of kVA rating for L_r and for total converter losses, plotted against resonant inductance value have fairly shallow minima. As a consequence a compromise position may be sought without significantly increasing the overall losses.

It can be seen from the discussion above that there are many inter-dependent considerations which impinge on the choice of L_r and C_r. As a consequence unless there is some overriding consideration, for example an extremely strict harmonic specification, then minimisation of total converter losses would probably give the best design values, or at least the best starting point for the design process. In pursuance of this, the next section gives a detailed account of the calculation of the overall converter losses.

7.2.2 Calculation of RDCL Converter Losses

This section is divided into two parts; the first relates to the losses in a 3-phase inverter, which is relevant to the output stage, and the second part which relates to a single-phase inverter which is appropriate for the pulse converter input stage.

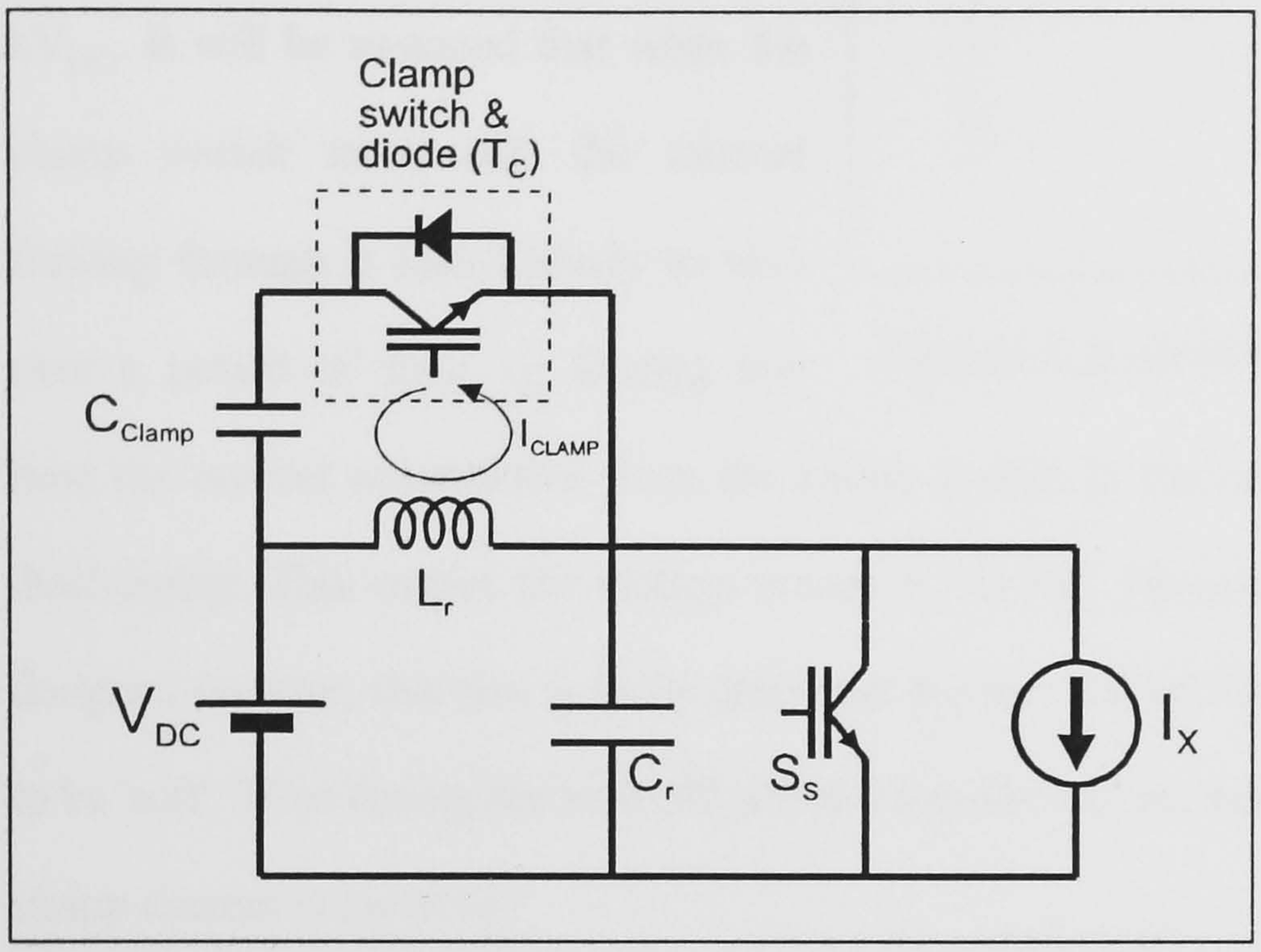

Figure 7.1 RDCLI Detailing Clamp Components

Jahns *et al* [73] described the losses in a 3-phase DC link Inverter. Although this work specifically mentions MCTs as the switching devices, it is also relevant to other gate turn-off devices. Firstly, consider the clamp switch shown in Figure 7.1. The output switches are represented by a current source, I_X. Using equation (5.12) it may be seen that the frequency of the pulses on the resonant link, f_r, is given by:

$$\frac{1}{2\sqrt{L_r C_r}\left(\cos^{-1}(1-k)+\frac{\sqrt{k(2-k)}}{(k-1)}\right)} \tag{7.1}$$

where k is the clamping coefficient.

The turn-off losses of the clamp switch will firstly be considered. The current in the clamp switch in the ideal case is symmetrical in form throughout the period of one pulse in order to maintain charge balance on the clamp capacitor, C_{clamp} as shown in Figure 7.2. The current in the clamp switch at the start of conduction is given by equation (5.9) as $\frac{V_{DC}}{Z_0}\sqrt{k(2-k)}$, and due to symmetry is $-\frac{V_{DC}}{Z_0}\sqrt{k(2-k)}$ when the clamp switch turns off. Let the magnitude of this value be denoted as the peak current, I_p. (NB. $Z_0 = \sqrt{\frac{L_r}{C_r}}$) When the clamp switch is conducting,

current circulates around the loop containing C_{clamp}, T_c, and L_r. No current flows onto the resonant capacitor, C_r and as a consequence its voltage is constant, having the value kV_{DC}. It will be assumed that when the clamp switch turns off, the current flowing through it falls linearly to zero over a period of time, t_f. During this time the current commutates from the clamp switch to the resonant capacitor, which it begins discharging. This causes the voltage across T_c to rise. However due to the size of C_r in a well designed inverter, this rise is fairly slow and the turn-off of the clamp switch may be considered to be 'soft'. Thus during the turn-off period when the current falls from I_p to zero over time t_f, the clamp current is given by:

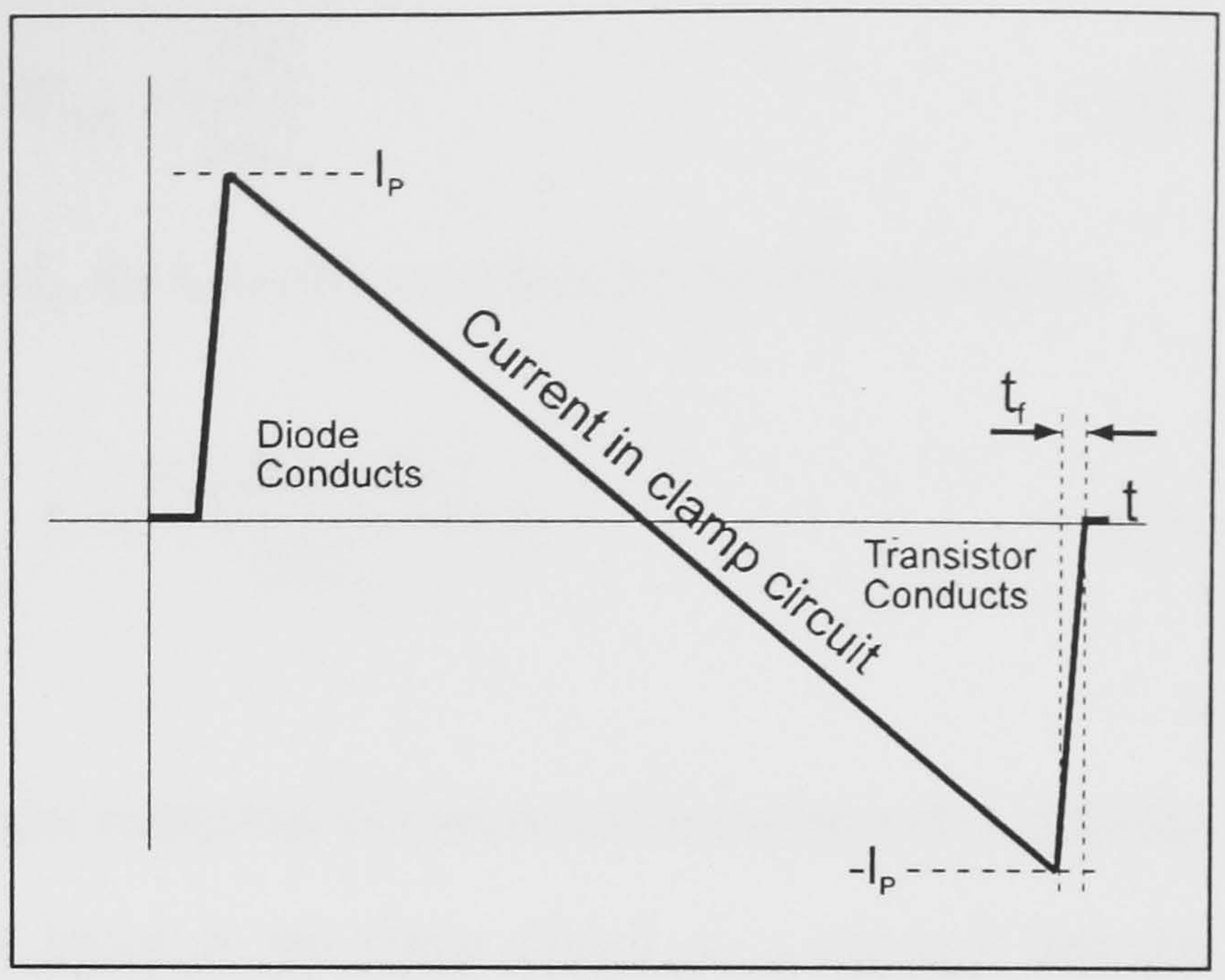

Figure 7.2 Ideal Clamp-Circuit Current

$$i_{clamp} = I_P\left(1-\frac{t}{t_f}\right) \tag{7.2}$$

Consequently, the current in the resonant capacitor which is increasing from zero to I_p is given by:

$$i_{C_r} = I_P\frac{t}{t_f} \tag{7.3}$$

Therefore, the voltage appearing across the clamp switch, T_c, is given by:

$$V_{T_c} = \frac{1}{C_r}\int_0^t i_{C_r}.dt = \frac{I_P}{t_f C_r}\int_0^t t.dt = \frac{I_p t^2}{2t_f C_r} \tag{7.4}$$

Hence the instantaneous power dissipation, P_1, in the clamp switch during turn-off is given by:

$$P_1 = V_{T_c}\times i_{clamp} = \frac{I_p^2 t^2}{2t_f C_r}\left(1-\frac{t}{t_f}\right) \tag{7.5}$$

The total turn-off energy per switching event is then described by:

$$W_{Tot1} = \int_0^{t_f}\frac{I_p^2 t_f^2}{2t_f C_r}\left(1-\frac{t}{t_f}\right).dt = \frac{I_p^2}{2t_f C_r}\left[\frac{t^3}{3}-\frac{t^4}{4t_f}\right]_0^{t_f}$$

$$\Rightarrow W_{Tot1} = \frac{I_p^2 t_f^2}{24 C_r} \tag{7.6}$$

Hence, for an average switching frequency, f_r, the turn-off power loss for the clamp switch is:

$$P_{Tot1} = \frac{I_p^2 t_f^2}{24 C_r} f_r = \frac{V_{DC}^2 k(2-k) t_f^2}{24 L_r} f_r \tag{7.7}$$

The turn-on of the clamp switch occurs under conditions of natural commutation and is virtually lossless. When estimating the *conduction* losses in the clamp switch, it is assumed that the current in the switch has the ideal form shown in Figure 7.2, also that both the diode and gate turn-off device have equal forward voltage drop, V_{fW}, and that the voltage drop is constant no matter what current is being carried. The period of conduction, t_b, is given by equation (5.11) as:

$$t_b = \frac{2\sqrt{L_r C_r}\sqrt{k(2-k)}}{(k-1)} \tag{7.8}$$

Thus, the energy, W_{CC}, due to the conductive loss is given by;

$$W_{CC} = 2 \times \int_0^{t_b/2} V_{fw} \times i_{clamp} . dt \tag{7.9}$$

When $0<t<t_b/2$, i_{clamp} is given by;

$$I_p \left(1 - \frac{t}{t_b/2} \right) \tag{7.10}$$

Substituting for I_p from (5.9) gives;

$$W_{cc} = \frac{V_{fw} V_{DC} C_r k(2-k)}{(k-1)} \tag{7.11}$$

Thus, for a link frequency, f_r, the total conduction power loss in the clamp switch is:

$$\boxed{P_{CC} = f_r W_{CC} = \frac{V_{fw} V_{DC} C_r k(2-k)}{(k-1)} f_r} \tag{7.12}$$

The switching loss in the main devices of the inverter is a little more difficult to deal with. This is because the mode of switching varies from pulse to pulse depending on the instantaneous switch configuration and link current (I_X). If during a zero-voltage period of the link, the switches change in a manner which results in $I_{Lr}<I_X$ (I_{Lr} is the current in the resonant inductor) then the bus remains shorted until $I_{Lr}>I_X$. This gives the switches time to complete their turn-off without switching loss. However, if the switches change such that $I_{Lr}<I_X$ then the bus voltage begins rising immediately which introduces switching loss. In the general case where the modulation strategy is not known in advance, it is not possible to say which mode will occur and how often. Therefore, it is necessary to use some sort of estimate of the likely switching scenario. Divan *et al* [21] proposed that a suitable approximation was to assume that the worst-case current, I_0, is turned off in *half* of the switching cycles, where I_0 is the peak load current. This estimate is probably pessimistic since in many cases the link current is much less than I_0. The current causes the voltage on the resonant capacitor to rise, in the same way that the clamp switch inflicts voltage changes on C_r as it turns off. Thus an expression may be written based on equation (7.7), which describes the power loss, P_{SM}, in the main devices resulting from this:

$$\boxed{P_{SM} = \frac{1}{2} \times \frac{I_0^2 t_f^2}{24 C_r} f_r} \tag{7.13}$$

The conduction loss in the main devices is calculated by assuming that there is an equal forward voltage drop, V_{fW}, for all the switching devices and their inverse parallel diodes, and that the load current consists of a sinusoid having peak value I_0. Therefore the instantaneous power loss in a conducting device is:

$$V_{fw}.i_{load} = V_{fw}.I_0.\sin(\omega t) \tag{7.14}$$

Thus, the average power loss through conduction in the main devices, P_{cm} is given by:

$$P_{CM} = \frac{1}{T} \times 2 \times \int_0^{T/2} V_{fw} I_0 \sin(\omega t) dt \tag{7.15}$$

$$= \frac{\omega V_{fw} I_0}{\pi} \left[\frac{\cos(\omega t)}{\omega} \right]_0^{\pi/\omega} = \frac{2 V_{fw} I_0}{\pi} \tag{7.16}$$

The current in a 3-phase inverter always flows in 3 switches, thus the power loss due to conduction in the main devices is given by:

$$P'_{CM} = \frac{6V_{fw}I_0}{\pi} \tag{7.17}$$

Other sources of loss to be considered are the resonant components themselves. However, capacitors may be specified with extremely good high frequency, low-loss performance (e.g. polypropylene or multilayer ceramic) and as a consequence the capacitor losses are swamped by the losses in the resonant inductor. These losses may become appreciable due to high frequency effects such as skin effect, which can give the inductor an AC resistance which is many times greater than its DC resistance. Such effects may be mitigated by good design, for example by using Litz wire, but still the losses are a cause for concern and a good deal of design attention.

The losses are twofold; comprising an element due to the DC current supplied to the inverter stage, and an element due to the circulating resonant current. In this approximation, it is assumed that the AC and DC resistance of the inductor are equal, and that the resonant circuit is not clamped, thus the resonant current is considered to be sinusoidal. The frequency of operation of the circuit may then be written simply as $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, and the Q factor of the inductor is given by $Q = \frac{\omega_0 L_r}{R}$ where R is the DC resistance of the coil. Thus,

$$R = \frac{\sqrt{L_r / C_r}}{Q} = \frac{Z_r}{Q} \tag{7.18}$$

The DC current supplied to the inverter (assuming a constant DC source) is given by:

$$I_{DC} = \frac{P_0}{V_{DC}} \tag{7.19}$$

where P_O is the output power. Therefore the losses due to the DC component are:

$$\boxed{P_{L_{DC}} = \left(\frac{P_0}{V_{DC}}\right)^2 \times \frac{Z_r}{Q}} \tag{7.20}$$

The peak resonant current is obtained from equation (5.5) and has the value $V_{DC}\sqrt{\frac{C_r}{L_r}}$ in this case, where the resonant circuit is not clamped. Therefore, the RMS value of the circulating component of current is:

$$i_{clamp_{RMS}} = \frac{V_{DC}}{\sqrt{2}}\sqrt{\frac{C_r}{L_r}} \tag{7.21}$$

Therefore the loss in the resonant inductor due to the resonant component of current is:

$$\boxed{P_{L_{AC}} = \left(\frac{V_{DC}}{\sqrt{2}}\sqrt{\frac{C_r}{L_r}}\right)^2 \times \frac{Z_r}{Q} = \frac{V_{DC}^2}{2Z_rQ}} \tag{7.22}$$

Combining the equation above, the total loss in a Resonant DC Link Inverter may be described (with the approximations outlined) as:

$$\boxed{P_{TOT} = \frac{V_{DC}^2 k(2-k)t_f^2}{24L_r} f_r + \frac{V_{fw}V_{DC}C_r k(2-k)}{(k-1)} f_r + \frac{I_0^2 t_f^2}{12C_r} f_r + \frac{6V_{fw}I_0}{\pi} + \left(\frac{P_0}{V_{DC}}\right)^2 \times \frac{Z_r}{Q} + \frac{V_{DC}^2}{2Z_rQ}} \tag{7.23}$$

The next stage is to incorporate the effects of the Pulse Converter into the loss estimate. The Pulse Converter resides directly on the resonant bus as shown in Figure 6.6. Thus it may be considered that there is a nominal flow of current directly from the input stage to the output stage, by-passing the resonant inductor, L_r. It follows therefore, that there would be a subsequent reduction in the average value of the DC component of current in L_r compared to the case of a DC-supplied inverter, allowing L_r to be derated. However Chen *et al* [69] found when using a boost-converter input stage, that the worst case link current became much greater, resulting in higher peak stress levels in the resonant inductor and clamp switch. Consequently derating is not a viable option unless as Chen *et al* proposed, the modulation strategy is modified to reduce the peak current levels experienced on the link. This may be done by restricting modulation of the stages such that only one device may change state at any one time. This however, has adverse effects on the performance of the overall converter. It was suggested that the input stage be given lower priority under operating conditions such as this since the input side could be considered to be less critical. A further advantage of adopting a restricted modulation strategy is to reduce modulation of the voltage on C_r, thus minimising the losses in the clamp switch and main devices. In the light of the above, when incorporating the effect of the pulse converter stage into the loss

estimate, it will be assumed that the losses in the clamp arrangement remain substantially the same as in the previous case. Expressions will now be derived to describe the switching and conduction losses of the input stage.

Suppose the single-phase RMS supply voltage is V_S, thus the peak input current, I_S, is given by:

$$\frac{\sqrt{2}P_o}{V_s} \tag{7.24}$$

A new expression may now be written for the switching loss in the main devices, where 'main' now includes the devices of the input stage. The worst case turn-off current is $(I_o + I_s)$, thus, modifying (7.13) gives:

$$P'_{SM} = \frac{(I_0 + I_S)^2 t_f^2}{12C_R} f_r \tag{7.25}$$

An additional conduction loss term, P_{CI} must be introduced to account for the input stage, where there are always 2 switches in conduction at any one time.

$$\boxed{P_{CI} = \frac{4V_{fw}I_{IN}}{\pi}} \tag{7.26}$$

Thus, the loss estimate for the total conversion system may be written as:

$$\boxed{P_{TOT} = \frac{V_{DC}^2 k(2-k)t_f^2}{24L_r} f_r + \frac{V_{fw}V_{DC}C_r k(2-k)}{(k-1)} f_r + \frac{(I_o + I_S)^2 t_f^2}{12C_r} f_r + \frac{6V_{fw}I_0}{\pi} + \frac{4V_{fw}I_S}{\pi} + \left(\frac{P_0}{V_{DC}}\right)^2 \times \frac{Z_r}{Q} + \frac{V_{DC}^2}{2Z_r Q}}$$

(7.27)

Figure 7.3 shows an evaluation of equations (7.23) and (7.27) over a range of values of L_r. For each point on the graph, C_r is selected such that the resonant frequency of L_r and C_r remains fixed at 20kHz. An output load of 40kW, DC link voltage of 1000V, and peak load current of 100A is assumed. The switching devices are deemed to have a fall time of 1μs, and forward voltage drop of 3.2V which is typical for devices of this rating, such as the Toshiba MG180V2YS40. The Q factor of the coil is set at 150, and the single phase supply voltage

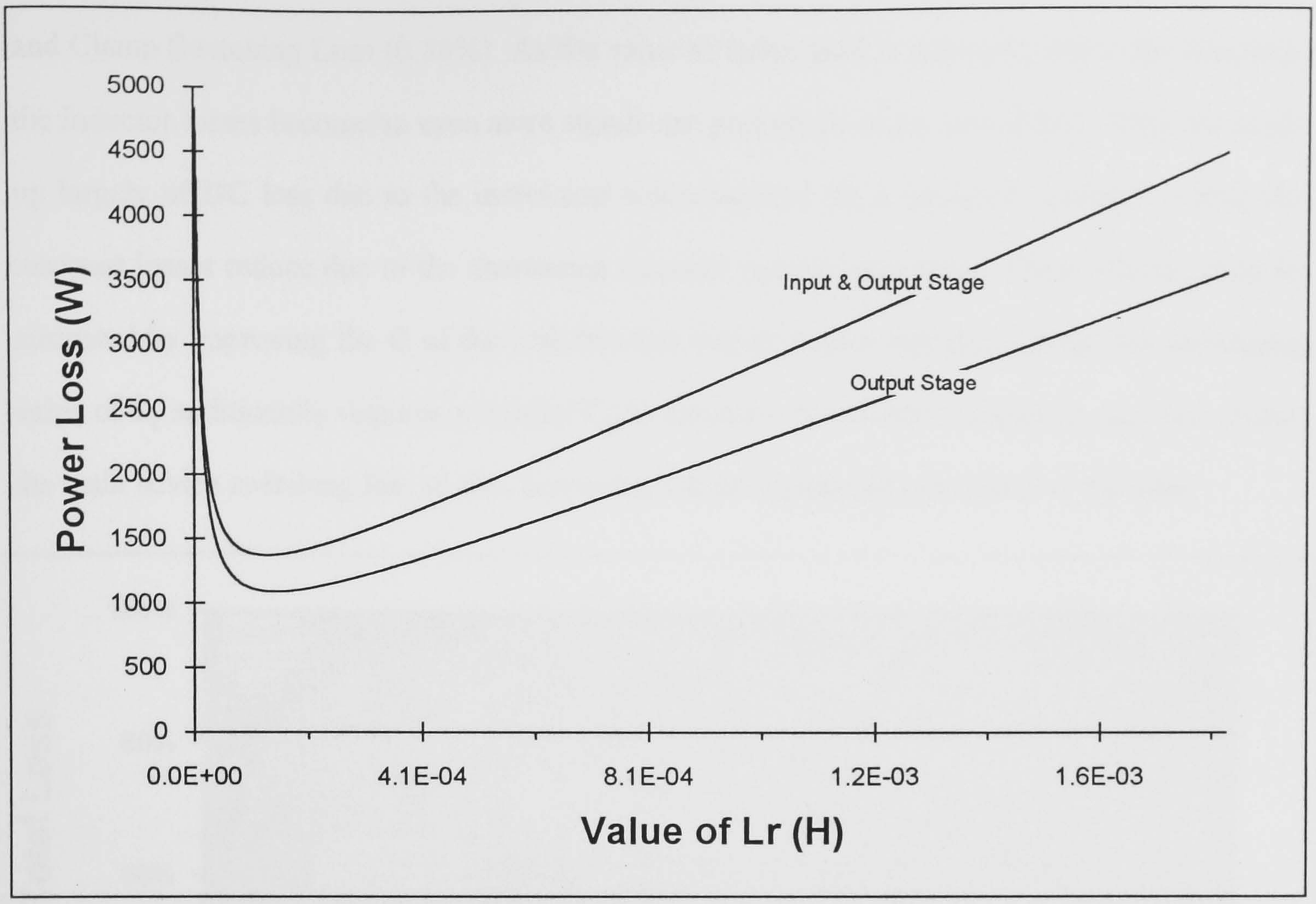

Figure 7.3 Curves of Power Loss for Input and Output Stages

assumed to be 1000V RMS. This means that the supply current has a peak amplitude of 56.57A. The top trace of the graph shows the total power loss when the input and output stages are considered, the lower trace shows the loss for the RDCLI output stage alone. From these curves the optimum value of L_r and C_r may be deduced in order to minimise losses. In the case of the RDCLI, the minimum occurs when L_r=149μH and C_r=0.425μF, and in the case of the combined pulse converter, and output stage the minimum occurs when L_r=135μH and C_r=0.469μF.

Figure 7.4 shows the various loss components as a proportion of the overall losses. It can be seen that for low values of L_r, the clamp switch conduction and switching losses contribute significantly to the total, due to the large circulating clamp current. This current also leads to very high losses in the resonant inductor. As the value of L_r is increased and passes through its 'optimum', the conduction losses become the most significant source of loss constituting 61.3% of the overall converter losses (44.5% in the output stage, and 16.8% in the input stage). At this point the losses consist in magnitude order of, Inductor Resonant Loss (14.3%), Inductor DC Loss (13.16%), Main Device Switching Loss (6.33%), Clamp Switch Conduction Loss (4.59%),

and Clamp Switching Loss (0.38%). As the value of inductance is increased above the optimum, the Inductor losses become an even more significant proportion of the overall loss. They are made up largely of DC loss due to the increasing coil resistance (Q is assumed constant), whilst the resonant losses reduce due to the decreasing resonant current magnitude. These effects could be mitigated by improving the Q of the coil, but this would involve significant cost. The increasing value of L_r additionally requires a smaller C_r to maintain the resonant frequency, and this causes the main device switching loss to rise, becoming a more significant proportion of the total.

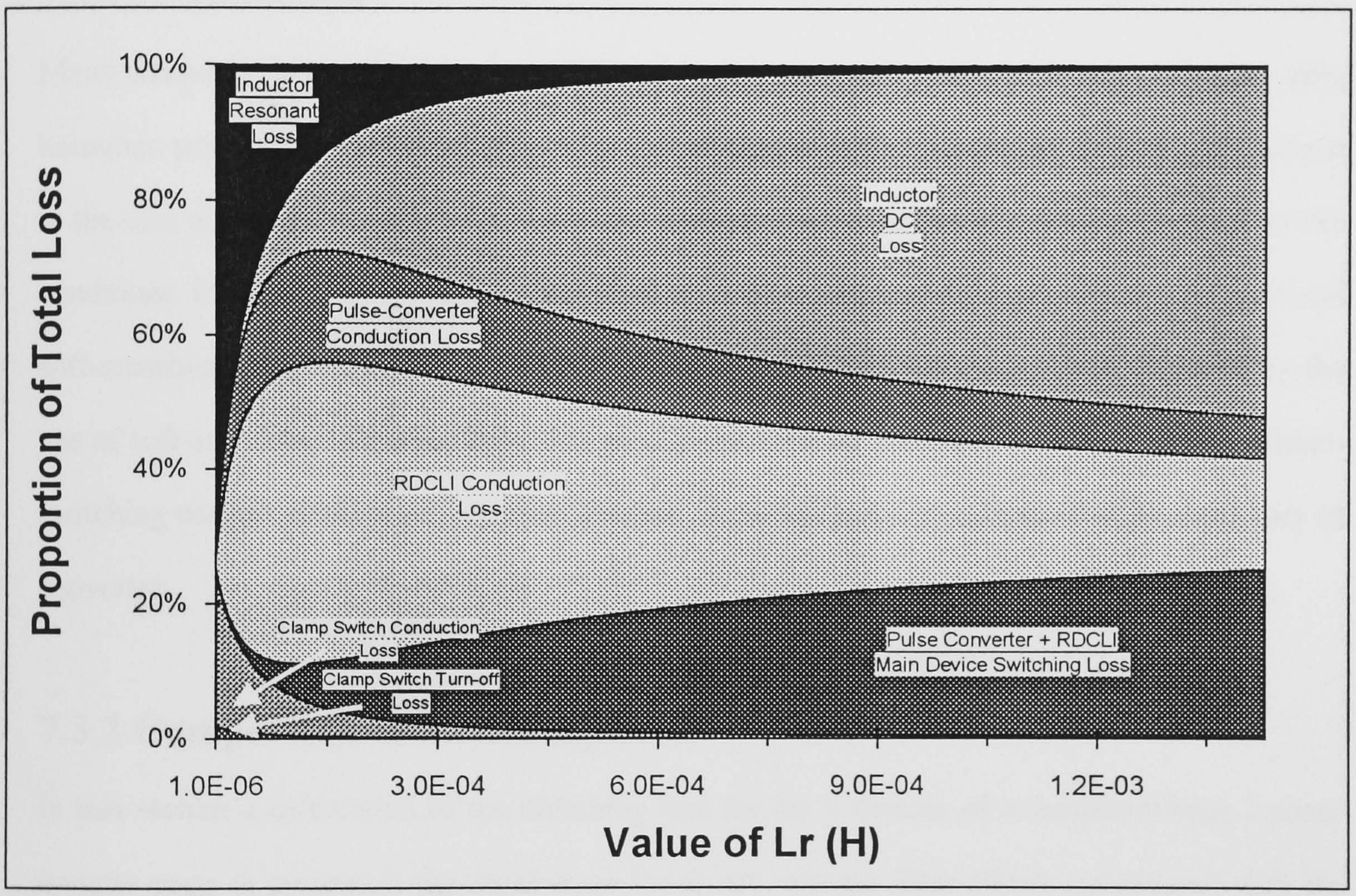

Figure 7.4 Analysis of Loss Components in RDCLI and Pulse Converter

By using graphs such as that shown in Figure 7.3 it is possible to select the theoretically optimum values of L_r and C_r for the resonant frequency desired. A breakdown of losses as shown in Figure 7.4 then allows the designer to select the areas of loss requiring further attention. In the example above it was seen that the conduction losses far outweigh the other losses, as may be expected for a soft-switching converter, and it may be worthwhile addressing this problem. For example, the IGBTs which have a significant on-state voltage could be replaced with MOS-Controlled Thyristors [74] although this would increase cost and may require paralleling of devices to achieve the current carrying capabilities due to the restricted range of these immature devices.

Additionally it was seen that the inductor losses are significant, and in practice may be even higher due to high frequency effects which are not accounted for in the simulation. Thus careful inductor design is important to maximise overall efficiency.

7.3 Comparison Between Hard-Switched and Soft-Switched Converters

7.3.1 Introduction

Many comparisons may be made between varieties of converter, based on for example cost, size, harmonic performance, or efficiency. This makes general comparison quite difficult, in contrast to the case of a specific application where the selection criteria are usually imposed by the service conditions. In the discussion below an attempt is made to evaluate the key properties of hard and soft-switching inverters by evaluation of the improvements in loss which can be achieved by the use of soft-switching and comparing this against the superior harmonic performance of the hard-switching variety. Additionally comparisons are made between device stresses in the two types of converter.

7.3.2 Comparison of Switching Loss

In this section a calculation of the switching loss for the 6 devices of a hard-switching 3-phase inverter stage is presented, the input stage losses are ignored. This allows comparison with the calculation pertaining to the RDCLI described in section 7.2.2. The loss in the active devices is lumped with the loss in their inverse-parallel diodes.

Firstly, consider the conduction loss. When taking account of only the fundamental component of load current in the converter, the conduction losses may be derived in the same manner as was performed for the soft switching converter (equation 7.17) thus,

$$P_{C_{Loss}} = \frac{6V_{fw}I_0}{\pi} \tag{7.28}$$

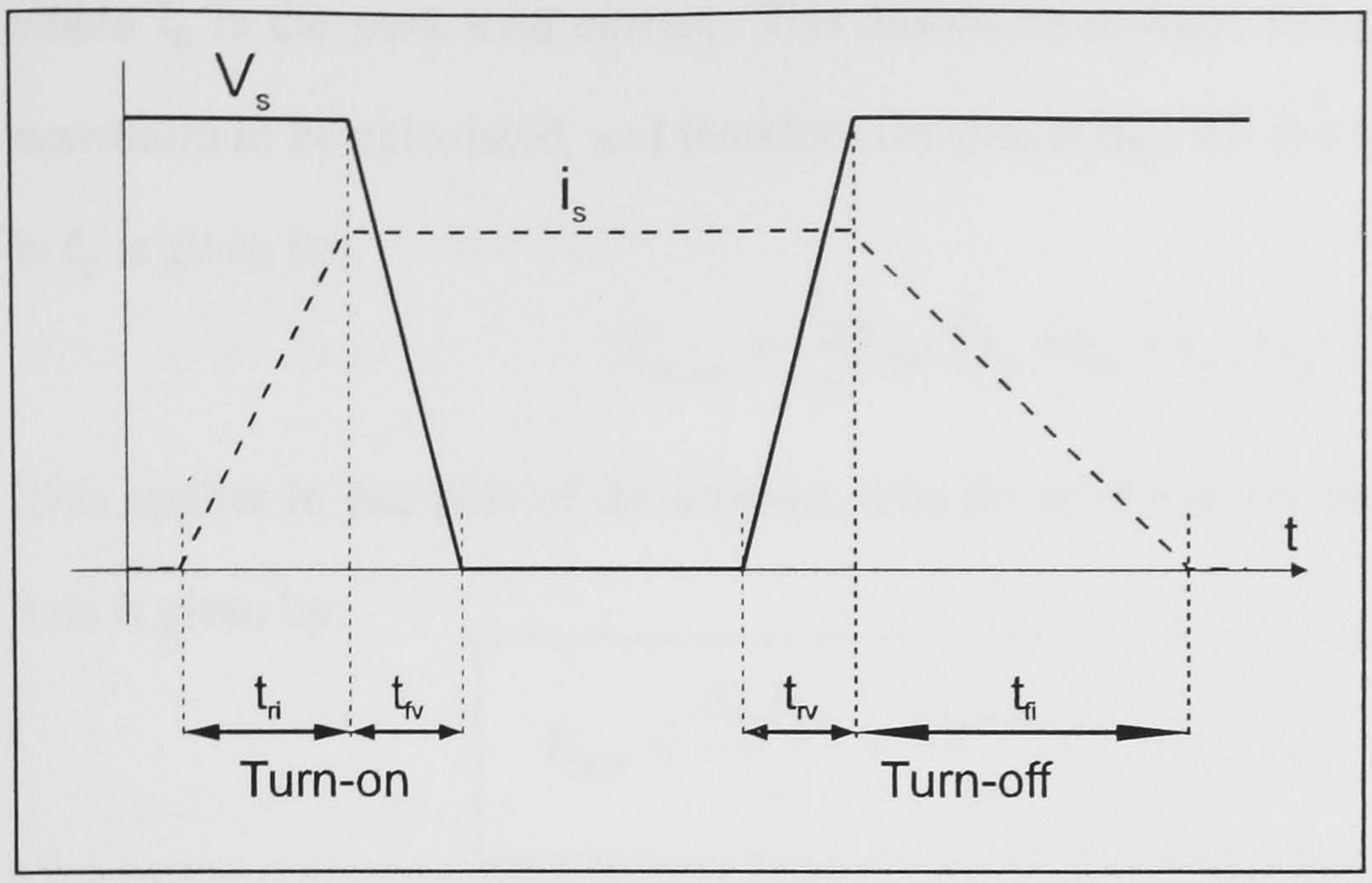

Figure 7.5 Voltage and Current Switching Waveforms for a Generic Semiconductor Switch

In order to calculate the switching loss, the generic model for a semiconductor switch supplying an inductive load will be used. [40] In this case the voltage and current waveforms for turn-on and turn-off are as shown in Figure 7.5. The instantaneous power loss during switching is given by :

$$P_{S_{LOSS}} = i_s v_s \tag{7.29}$$

thus for turn-on, the energy loss is given by:

$$W_{on} = \frac{1}{2}\left(t_{ri} + t_{fv}\right)V_{DC}I_i \tag{7.30}$$

where I_i is the instantaneous switch current. For turn off, the following applies:

$$W_{off} = \frac{1}{2}\left(t_{rv} + t_{fi}\right)V_{DC}I_i \tag{7.31}$$

These values consequently vary depending on the instantaneous current which must be made or broken and this in turn depends on the current point in the output cycle. An expression may be written for the average power loss which occurs: consider one pole of the output stage. As shown in Figure 7.6, on each cycle of the carrier waveform one turn-on and one turn-off occurs. The current to be commutated varies in a sinusoidal manner, thus the average value of current is:

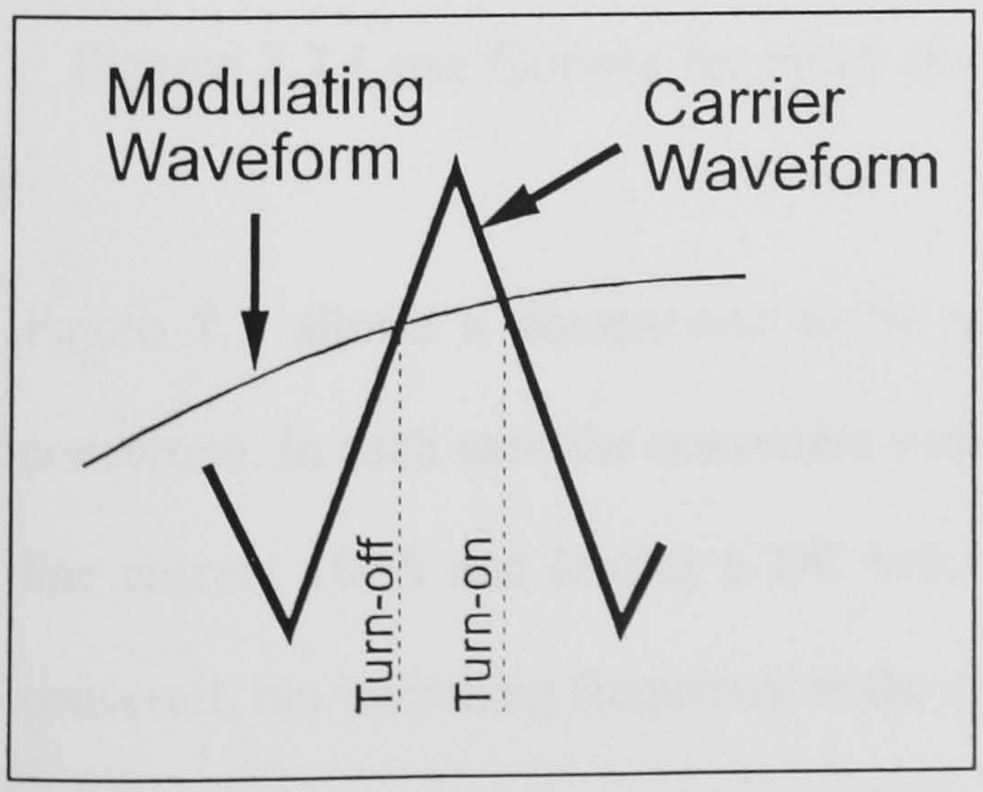

Figure 7.6 PWM Waveforms

$$I_{avg} = \frac{1}{\pi}\int_0^{\pi} I_0 \sin(\omega t).d(\omega t) = \frac{2I_0}{\pi} \tag{7.32}$$

where I_0 is the peak load current. This allows an average energy loss per cycle of the carrier waveform to be calculated, and therefore the power loss for the case where the carrier frequency is f_c is given by:

$$P_{S_{LOSS}} = \frac{I_0}{\pi} V_{DC} . \left(t_{ri} + t_{fv} + t_{rv} + t_{fi} \right) . f_c \tag{7.33}$$

This applies to one pole of the inverter, thus the total loss for the inverter, including conduction loss is given by:

$$\boxed{P_{TOT} = \frac{6 I_0 V_{fw}}{\pi} + \frac{3 I_0 V_{DC}}{\pi} \left(t_{ri} + t_{fv} + t_{rv} + t_{fi} \right) f_c} \tag{7.34}$$

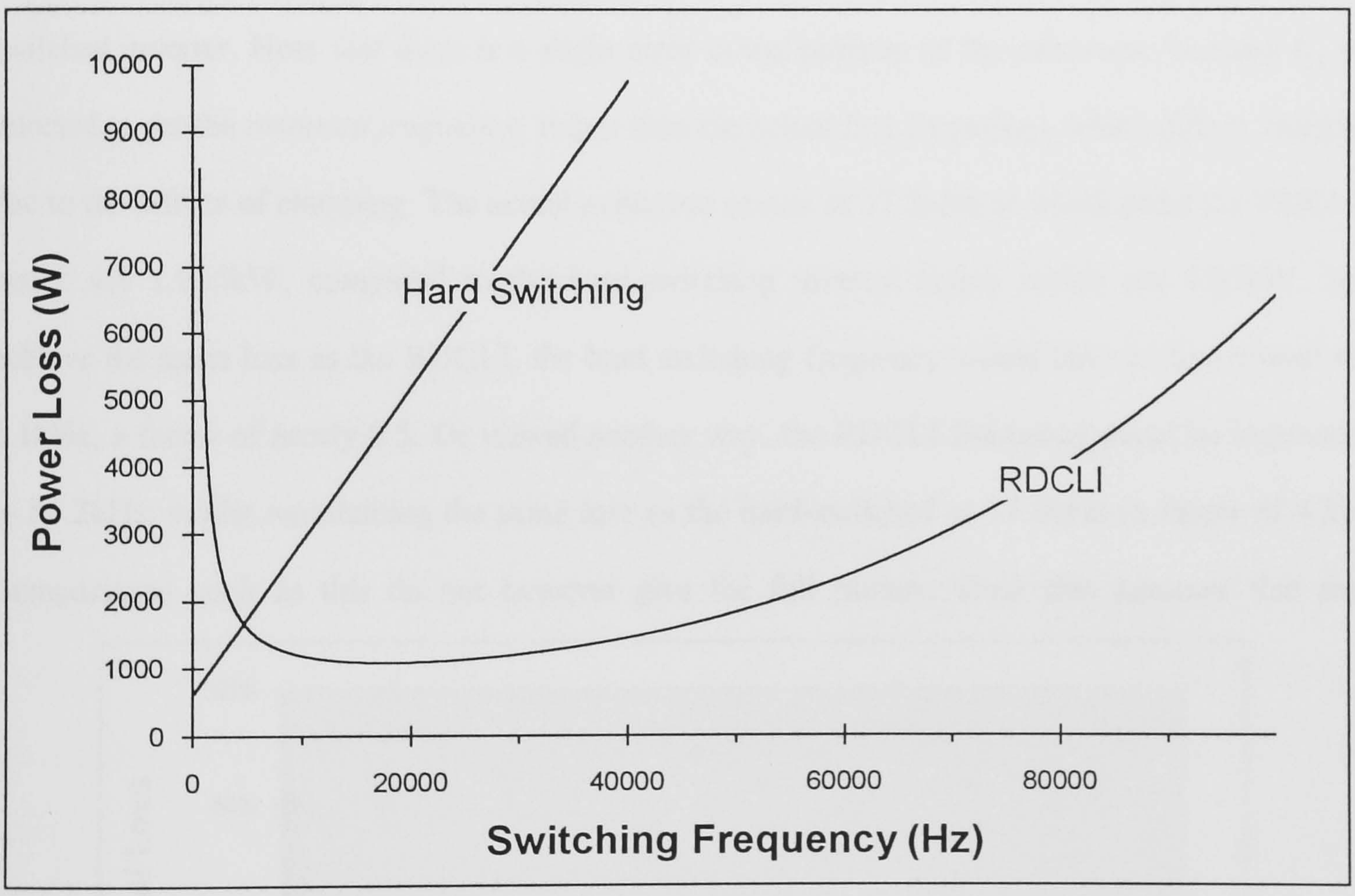

Figure 7.7 Loss Curves for Hard and Soft Switching Converters

Figure 7.7 allows a comparison to be made between the losses of hard and soft-switching converters. In each case the converters were assumed to be supplying a load of 40kW, with peak line current 100A and having a DC link voltage of 1000V. In the case of the hard-switching converter, the 'switching frequency' is the carrier frequency. In order to calculate the losses for the RDCLI the resonant inductance was set at 149μH, and the capacitance value adjusted to give the

appropriate resonant frequency. At low switching frequencies the losses for the RDCLI are seen to rise dramatically; this is due to the effects of using a large capacitance value in order to achieve the desired switching frequency, which leads to very high circulating currents in the clamp circuit with attendant high losses. At high frequencies the effects of loss in the resonant inductance and increased main device loss due to the small resonant capacitance are revealed by the losses increasing once more.

As suggested by previous results, the RDCLI has minimum losses in the region of 20kHz. Clearly this minimum could be moved (although its value would not remain the same) so that it exists at the switching frequency demanded by a specific application. This is not an option for the hard switched inverter. Note that there is a slight error in the position of the minimum, because C_r is selected to set the *resonant frequency*, rather than the actual *link frequency,* which differs slightly due to the effects of clamping. The actual minimum occurs at 17.8kHz at which point the RDCLI losses are 1.085kW, compared to the hard-switching inverter losses which are 4.69kW. To achieve the same loss as the RDCLI, the hard switching frequency would have to be reduced to 2.1kHz, a factor of nearly 8.5. Or viewed another way, the RDCLI frequency could be increased to 86.2kHz, whilst maintaining the same loss as the hard-switched at 17.8kHz (a factor of 4.8). Comparisons such as this do not however give the full picture, since this assumes that the

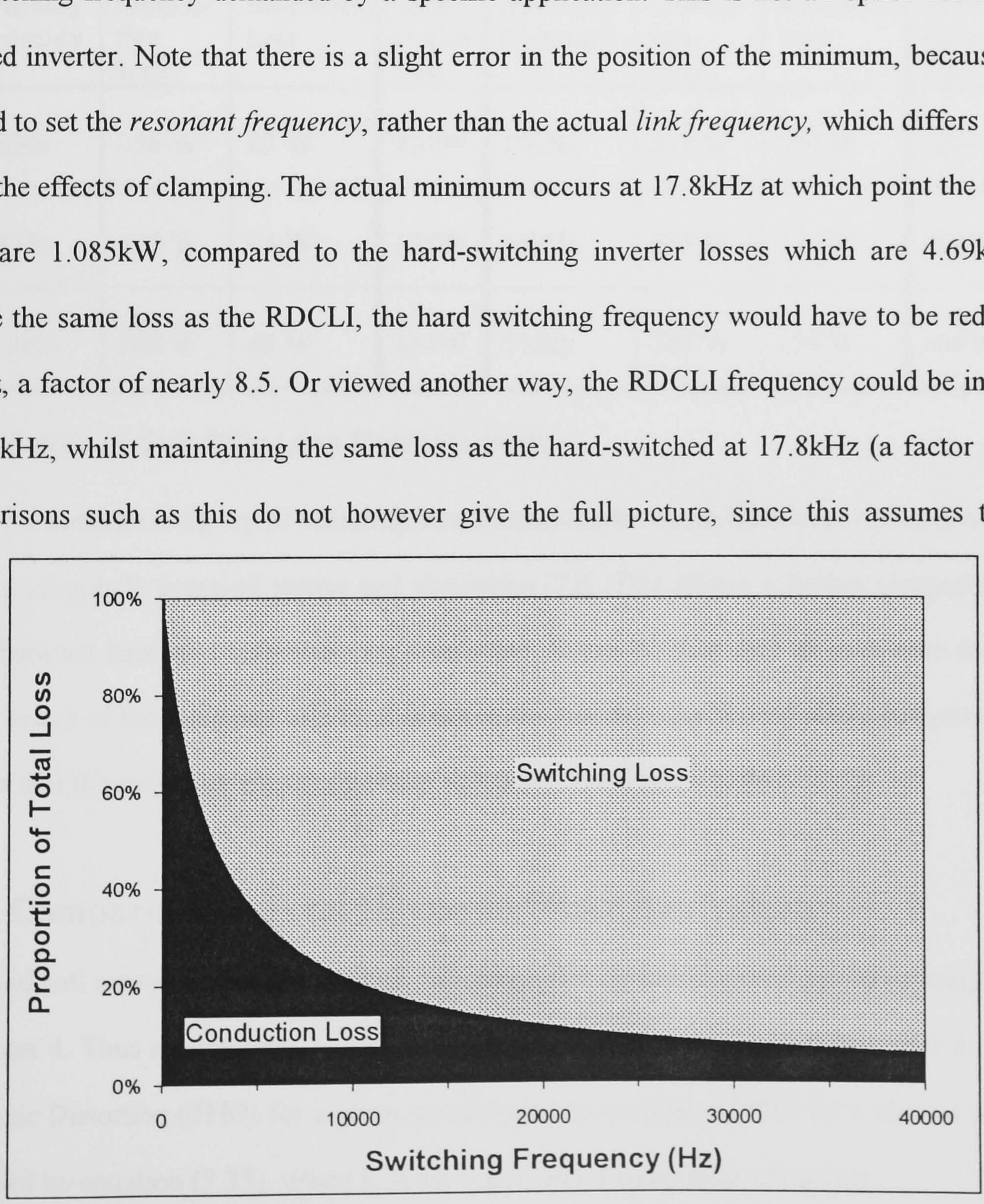

Figure 7.8 Analysis of Loss Components for Hard-Switching Inverter

resonant inductance remains at 149μH. As a consequence when operating at 86.2kHz, the RDCLI is not working near its optimum point anymore. In other words, the converter could be made to operate at even higher frequencies without increasing losses, by reconfiguring the resonant components. The graph in Figure 7.8 shows a breakdown of the losses in the hard-switched converter, and it may be seen how the switching loss rapidly dominates the overall losses as the switching frequency increases.

	Resonant DC Link				Hard-Switching				
Devices Used	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss	Notes
1200V 100A IGBT	60kHz	374 W	87 W	461W	10kHz	352 W	330 W	682W	I_o=55A V_{DC}=600V
600V 100A IGBT	60kHz	480 W	94 W	574W	10kHz	465 W	436 W	901W	I_o=100A V_{DC}=300V P_o=10kW
Simu-lated BJT	25 kHz	283 W	48 W	331W	5 kHz	225 W	434 W	659W	I_o=100A V_{DC}=600V

Table 7.1 Survey of Switching Loss Measurements

Table 7.1 contains a survey of switching loss measurements which have been obtained by several authors using both practical means and simulation [75]. This allows a further comparison to be made between hard and soft-switching converters. It can be seen that in each case the overall device losses of the Resonant DC Link Inverter are less than the Hard-Switched Inverter despite the fact that the switching frequency of the RDCLI is 5 to 6 times higher.

7.3.3 Comparison of Total Harmonic Distortion Values

Hard and soft switching converters have radically differing modulation schemes as was discussed in chapter 4. Thus an important measure of the efficacy of the two types of converter is the Total Harmonic Distortion (THD) for a given set of operating conditions. THD for a current waveform is defined by equation (7.35), where I_1 is the fundamental component of current.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \times 100\% \qquad (7.35)$$

To prepare the data for the graphs presented in Figures 7.9 and 7.10, the spectra of the voltage waveforms of the hard and soft-switched converters were calculated for the situation where the converters were generating a nominal fundamental component of 0.8 p.u. having a fundamental frequency of 50Hz. Currents were then calculated from the harmonic components, assuming a load of resistance 1Ω, and inductance of 1.5mH, thereby allowing the THD to be calculated. A 3-phase system was assumed and as a consequence all triplen harmonics were eliminated.

Figure 7.9 shows a comparison between the THD of the load current for hard and soft-switching converters. It can be seen that the soft-switching converter has higher THD values at all switching frequencies due to constraint of using Discrete Pulse Modulation. At low switching frequencies the THD curve is very erratic, this is due to difficulties experienced by the pattern search algorithm which is optimised to deal with large numbers of pulses and consequently becomes a little unpredictable in this frequency range. Also the search technique was configured to perform harmonic minimisation rather than THD minimisation which may affect the results obtained. In general, the RDCLI has THD values about 4 times greater than the hard-switching

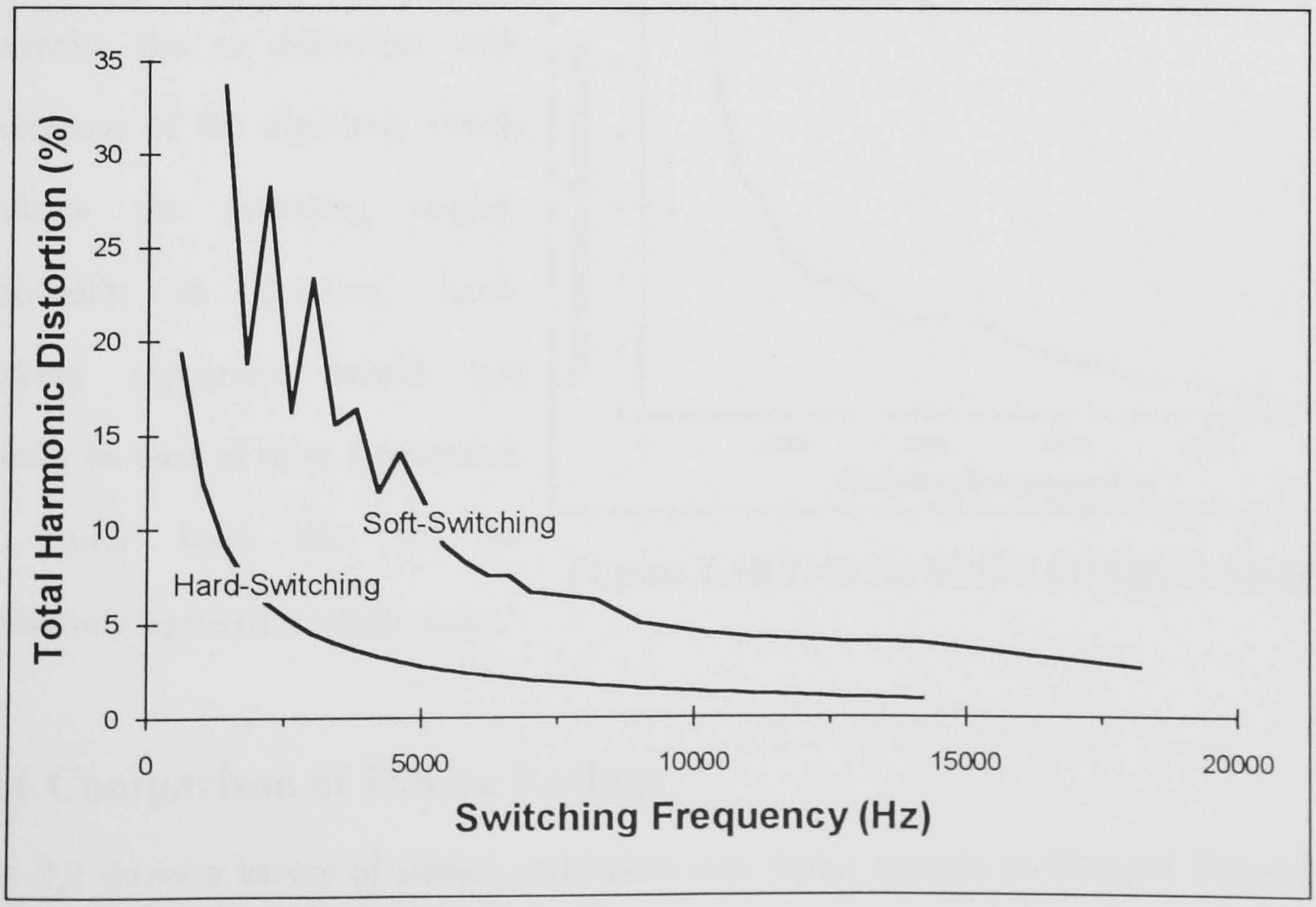

Figure 7.9 Comparison of THD Curves for Hard and Soft-Switching Converters

inverter at a given switching frequency. However, by raising the RDCLI frequency by a factor of 10, the THD figure can be made better than that of the hard-switching converter by a factor of the order 3 to 4. Similar results were also found by Finney et al [47]. It is important to note that increasing the operating frequency of an RDCLI by a factor of 10 does not have the same consequences for the switching loss that would be experienced by a hard switching inverter as long as an optimum design is always used. Calculations performed using the methods outlined in section 7.3.2 show that an RDCLI operating at 4kHz has minimum losses of 1.046kW when L_r=805μH (supplying a load of 40kW). Under these conditions the hard-switching inverter has losses of 1.528kW. The operating frequency of the RDCLI may be increased to 40kHz, whereupon the losses are only slightly greater at 1.212kW using a new optimum value for L_r of 63μH. In other words, an improvement in THD may be achieved over the hard-switching converter whilst still maintaining losses which are less than those experienced by the hard-switching variety. This loss/THD trade-off is extremely complex and varies throughout the operating frequency range but could be investigated to great advantage in the case of a specific application. For completeness, Figure 7.10 shows the very low values of THD which may be obtained using an RDCLI at very high frequencies. Calculations were not carried out for the hard-switching converter at these frequencies due to difficulties with convergence of the algorithm which calculates the switching angles. Additionally in practice, hard-switching converters would not normally be used at these frequencies and power level due to the prohibitively high losses which occur.

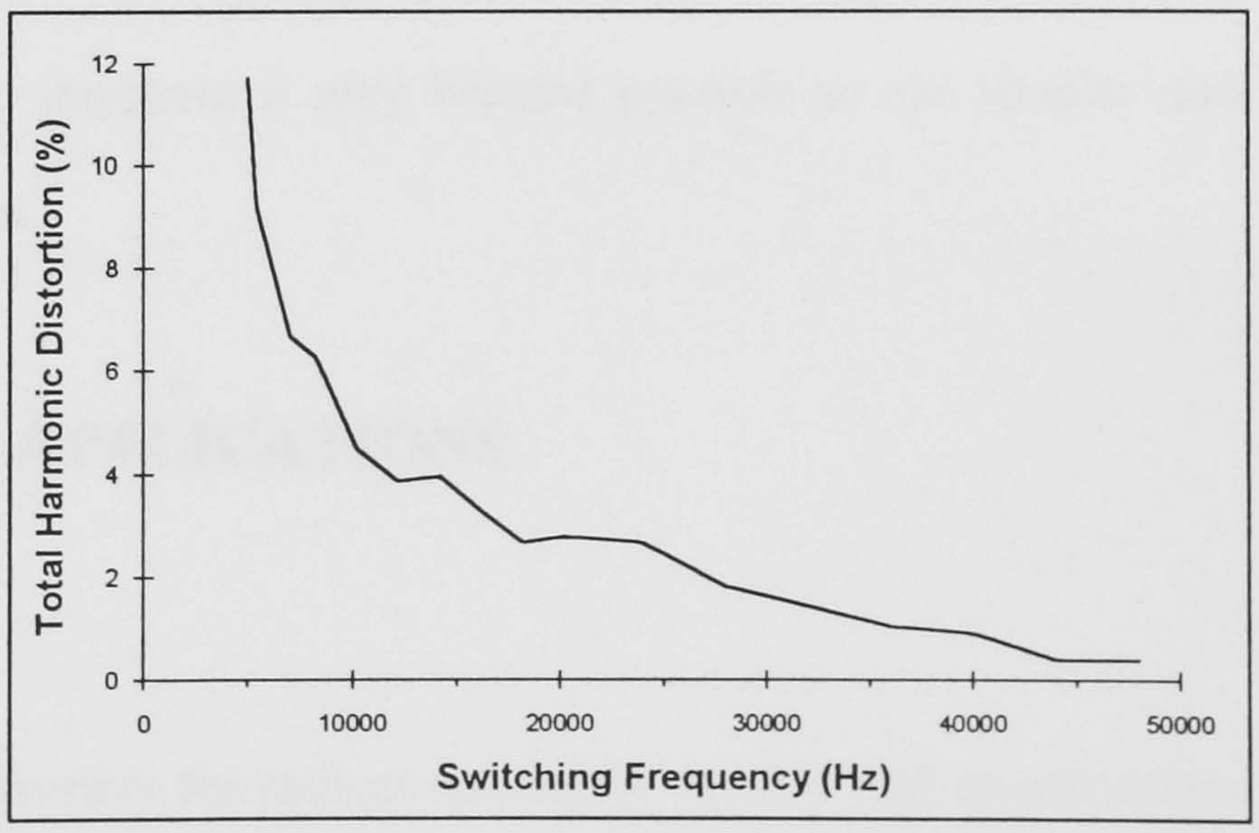

Figure 7.10 THD for RDCLI at High Frequency

7.3.4 Comparison of Device Ratings

Table 7.2 shows a survey of studies undertaken into device stresses in Clamped Resonant DC Link Inverters. [69,21,2] As discussed previously, it may be seen that the current stress on the

	HARD SWITCHED		SOFT SWITCHED		
	Peak Voltage Stress	**Peak Current Stress**	**Peak Voltage Stress**	**Peak Current Stress**	**Switching Frequency**
Survey 1	Main Devices		Main Devices		
	305V	108A	424V	108A	
20kW, 230V AC			Clamp Device		
			424V	108A	
Survey 2	Main Devices		Main Devices		Hard:5kHz
	300V	150A	460V	136A	Soft:25kHz
10kW, V_S=300 Vdc			Clamp Device		
			-	33A (RMS)	
Survey 3	Main Devices		Main Devices		Hard:2kHz
	1 p.u.	1 p.u.	1.3 p.u.	1 p.u.	Soft:20kHz

Table 7.2 Survey of Device Stresses

devices is the same in the case of the soft and hard-switching converters. The voltage stress is important for railway traction applications. A nominal 750V DC railway supply may vary between 400 and 900 Volts, thus by selecting a clamping level of $1.4V_{DC}$ it is possible to implement an inverter without using a pre-conditioning chopper by use of currently available 1.7kV IGBTs. As the device technology improves it may become possible to use simpler and more rugged passively clamped topologies.

7.4 Design for Railway Applications

7.4.1 Introduction

Many of the design requirements for converters for railway use apply equally well to converters in other applications. However there are aspects of the rail environment which make the needs more acute, for example the weight of a converter which has a direct bearing on the overall vehicle performance and thus has significant cost implications. In this section the requirements for auxiliary converters which relate to the choice of topology are reviewed, and the ability of Resonant DC Link Inverters to satisfy these needs are discussed. Optimisation of auxiliary

converters is of greater importance now than ever before, due to the rising demands of railway customers which in turn makes greater demands on equipment levels. [76,77] In addition high reliability is required since failure of the auxiliaries may necessitate removal of a vehicle from revenue-earning service.

7.4.2 Design Overview

SIZE

Competition for space on rail vehicles is fierce, especially between the space made available for equipment, and that set aside for passengers. Passenger space is of a premium since it influences the revenue-earning capacity of the vehicle and as a consequence converter size must be minimised. Converter size is largely affected by its overall losses. This is where the use of Resonant Converters can have a significant impact due to their considerably reduced losses, which allows a reduction in heatsink area. However, the reduction in size is tempered to some extent by the need to provide space for the resonant components, and clamping device if used.

WEIGHT

Weight requires careful control to ensure that the overall vehicle performance specification can be met and from the operator's point of view, to limit track damage and propulsion costs. Once again the increased power density of Resonant Converters due to reduced heatsink area is an important factor.

NOISE LEVEL

Noise must be limited to levels where staff and passengers are not disturbed by its presence. This is particularly important for power converters as they often have associated with them a high frequency 'whine'. Resonant Converters are capable of alleviating problems due to their frequency of operation which is normally above the range of audibility, a feature made possible by the very low levels of switching loss.

GENERATED WAVEFORM QUALITY

The complex electronic equipment which is fitted to modern rail vehicles frequently requires higher quality power supplies than has been previously made available. Due to the higher operating frequencies possible with resonant converter, it is possible to generate waveforms with reduced harmonic content without significantly increasing switching loss. However, as was seen earlier in this chapter some of the increase in switching speed is offset by the need to use Discrete Pulse Modulation. Additionally there is still a trade-off between size and weight, and waveform quality, although the use of Resonant Converters presents the designer with considerably more flexibility.

COST

The initial cost of Resonant Converters may be a disincentive for their use. The design of hard-switching converters is well known and understood, requiring few components and simple control strategy. The same cannot be said of Resonant Converters, which increases the design and build time and costs. This situation may improve as the technology matures but is currently a significant factor. The 'ownership costs' are difficult to assess at the moment due to the small quantity of Resonant DC Link Inverters currently in use, but the topology is associated with reduced device stress which may reduce failure of devices compared to hard-switching circuits.[1]

SIGNALLING AND ELECTROMAGNETIC COMPATIBILITY

As has been discussed previously, the converter must not interfere with the signalling systems. Where elimination of specific harmonics is required, hard-switching PWM converters have extremely desirable control characteristics. However it has been shown that harmonic minimisation is possible both in the DC and AC supply case, even with the restriction of Discrete Pulse Modulation. With regard to Electromagnetic Compatibility (EMC), due to the reduced rates of *di/dt* and *dv/dt* encountered in Resonant Converters, problems relating to EMC are lessened. Apsley and Skinner [78] found a reduction of 15dB in conducted interference over the range 150kHz-2Mhz when comparing a 10kVA soft-switching converter against a 10kVA hard-

switching converter. This is an extremely important attribute of the soft-switching converter, both for railway and other industrial applications.

7.5 CHAPTER SUMMARY

Selection of the resonant components may be considered in two stages. The first is to select the ratio which sets the operating frequency, and the second is to select the actual values, which has a strong influence on the overall losses. In general a large value of resonant capacitance leads to lower main device losses, but higher clamp circuit losses. A useful way to select the resonant components is by investigation of the loss mechanisms. In pursuance of this equations have been derived which allow an approximation of the loss to be calculated both for the Resonant DC Link Inverter, and for the Pulse Converter Input stage. Evaluation of the equations enables the minima of the loss curves to be located.

Comparison between hard and soft switching converters is quite difficult due to the complex trade-offs which exist between various parameters such as loss and harmonic quality of the generated waveforms. In general however, it was seen that soft-switched converters have a lower loss, but higher Total Harmonic Distortion (THD) at a given operating frequency. The switching frequency may be increased to improve the THD without significantly increasing the overall losses. The Actively Clamped Resonant DC Link Converter requires devices with equal current carrying capabilities to the equivalent hard-switched converter and devices with a voltage rating approximately 1.4 times that of the hard-switched type, depending on the clamping ratio used.

Soft-switching converters were seen to possess many desirable qualities which are useful in rail traction applications, but suffer from a higher initial cost and increased design complexity.

Chapter 8

Conclusions

Hard-switching converters have much to commend them; they allow simple circuit topologies to be used and are easy to control. However, they suffer from high switching loss which restricts their operating frequency and power density, and causes problems with Electromagnetic Interference (EMI). It has been shown that resonant converters may alleviate these problems by the introduction of voltage or current zeros at the instant of device switching. Not only is the switching loss significantly reduced but also the *di/dt* and *dv/dt* values, thereby diminishing the problem of EMI and device stresses. Furthermore, the increased frequency of operation allows improvements to be made in power density of converters.

Resonant converters may be divided into 3 families:

- 'Load Resonant' which are best suited to high frequency AC generation where the generated waveform has the same frequency as the oscillation frequency of the resonant components. However large circulating currents or voltages occur which require components with high ratings.
- 'Resonant Switch' converters which have good spectral characteristics since they allow true Pulse Width Modulation (PWM) control but require one set of resonant devices per inverter pole since the resonant components are on the output side. This can lead to a high component count.
- 'High Frequency Link' converters where the output stage is modulated to facilitate the generation of low frequency output waveforms. Usually only one set of resonant components is required.

Of particular note is the Resonant DC Link Inverter (RDCLI) which belongs to the 'High Frequency Link' family of converters. This shows great promise for use in 3-phase drive

applications due to its uni-polar link which allows a low device count. In addition, the converter may be implemented using active clamping which reduces the voltage stress on the devices. As high-speed power device technology improves, it may become feasible to utilise the more rugged and efficient, passively clamped Resonant DC Link Inverter.

In order to allow rapid and inexpensive evaluation of converter topologies and modulation strategies, it is beneficial to be able to perform computer simulation. Some proprietary time-domain simulation packages are unable to deal effectively with rapidly switching circuits due to difficulties in maintaining accuracy. It was shown that a simulation may be implemented quite easily using a frequency-domain method. However certain procedures which depend on instantaneous circuit conditions, were performed in the time-domain for simplicity. It was noted that a disadvantage of the frequency-domain method is that only steady-state analysis may be performed. Despite this, it is a useful tool for many circuit assessment exercises and may be implemented using a desktop PC. Results obtained from the simulation program were compared against those obtained from a low-power test-rig. Close agreement was observed, though some discrepancy was in evidence which may be due to approximations made in the circuit model. Chiefly these were the assumption of zero resistance for the converter components, and a linear frequency response for the load. The simulation could be enhanced to incorporate features such as skin effect at higher frequencies to achieve even more accurate results.

Selection of a modulation strategy is a crucial factor in achieving a successful overall design for a converter since it affects the ability of the converter to generate the required output waveforms and to control its internal losses. The constraint of using Discrete Pulse Modulation (DPM) which is placed on most high frequency link converters, makes development of modulation strategies much more difficult. A commonly used strategy for Resonant DC Link Inverters is Sigma Delta Modulation ($\Sigma\Delta M$) which is quite effective in generating waveforms having low Total Harmonic Distortion (THD) but the spectrum of the waveforms cannot be shaped at will, and often contains harmonics of significant amplitude at low frequencies, where they are difficult to filter. This may cause problems in the rail traction environment where harmonics could appear

at signalling frequencies. It was seen that topologies have been described in the literature which allow approximate or true PWM to be implemented on a High Frequency Link converter but this is done at the expense of undesirable increases in losses or circuit complexity.

A pre-programmed modulation strategy has been proposed, based on an optimisation procedure known as Simulated Annealing. It has been shown by simulation and experimental results that this strategy is capable of achieving minimisation of individual harmonics, or groups of harmonics in a converter constrained to use Discrete Pulse Modulation, such as the RDCLI. This could have important applications in the rail traction environment for signalling frequency avoidance. Because the pre-programming method is based on evaluation of a cost function, complex harmonic manipulations may be implemented by inclusion of the appropriate weighting factor in the cost function. For example THD or Psophometric Current could be minimised. Thus the proposed modulation method could be applied to many other specialist applications, as well as routine use in industrial 3-phase drives.

The search algorithm used to select the pre-programmed modulation pattern assumes an 'ideal' link waveform consisting of sinusoidal curves. In practice as the converter is loaded, the modulation of the link current introduces distortion into the link waveform by causing sudden voltage changes on the resonant capacitor. It was shown that this can lead to otherwise minimised harmonics becoming larger than in the previous no-load condition (and vice versa for non-minimised harmonics). However it was noted that satisfactory minimisation was still achieved. It was suggested that the resonant capacitor be made as large as possible to minimise the link waveform distortion which results from link current modulation. The selection of the capacitor should however be done within the constraints of overall loss minimisation as outlined in Chapter 7.

The proposed modulation strategy furnishes the RDCLI with some of the harmonic control attributes which are normally the preserve of hard-switching PWM converters. In addition, the pre-programming technique may be implemented using modest computing facilities. Mitigation of

the effects of link waveform distortion could be incorporated into the modulation strategy by the development of the pre-programming selection procedure.

It has been shown that an RDCLI can be controlled using a simple microcontroller such as an 8051. On the test-rig, both the modulation of the output devices and the control of the resonant circuit were handled by one 8051. The rapid voltage comparisons required to control resonance may be performed externally in an analogue circuit and interfaced to the microcontroller using A/D and D/A converters. If the link frequency is raised above about 20kHz, it would exceed the capabilities of the 8051 but a faster processor such as a member of the Analog Devices 210x family of Digital Signal Processors (DSPs) could be used. This would also allow integration into one Integrated Circuit, comprehensive converter control features such as voltage regulation and motor control loops.

Measurements on the test-rig showed a very small area bounded by the switching locus indicating that the conditions were satisfied for low-loss switching. No particular attention was given to circuit layout of the test-rig but this did not cause any difficulties, because of its small size. However, it is likely that a larger converter would suffer problems due to inductance of the resonant bus upon which the output devices are mounted. This would increase the voltage at the 'zero-volt' point of the resonant waveform, thereby increasing switching losses. An improved circuit layout would probably include laminated bus bars, and distributed resonant capacitors.

On DC supplied railways, converter harmonics may be eliminated on the input side by implementing an elimination strategy on the output side. The situation is more complex in the case of an AC-fed vehicle where a rectifier must abut the supply. This drastically modifies the harmonic qualities of the converter. It was shown that large inductances are required to reduce THD and Psophometric Current levels if a simple diode rectifier is used. This adds cost, size and weight. The situation can be improved by the use of a Pulse-Converter front end. It has been shown that the Pulse-Converter could be implemented in a soft-switching format by inclusion into an RDCLI circuit. A modulation scheme has been proposed which demonstrates harmonic control

of the input current, whilst also synchronising with the supply waveform. This would allow compatibility with signalling systems and minimisation of psophometric current levels, in addition to the advantages already outlined for soft-switching converters. The modulation scheme was verified by comparison between simulated data, and results from a low-power test-rig. This showed that harmonic elimination was achieved in the desired frequency bands but there were discrepancies between the amplitude of individual harmonics. This was partly attributed to the lack of computation speed of the microcontroller. Development of a more robust controller, perhaps using a DSP chip, would make the results more predictable. This would be a necessity if the scheme was to find application in the railway environment.

It is possible to write simplified loss equations for the Resonant DC Link Inverter and Pulse-Converter input stage. Similar equations may be written for hard-switching converters and these show that for a given switching frequency, the value of THD for the hard-switching converter is lower than that of the soft-switching converter. This is due to the constraint of using DPM in the case of the soft-switched converter. However it may be deduced that the switching frequency of the RDCLI may be raised significantly without appreciably increasing overall losses. Thus, it is possible to simultaneously achieve lower losses and a better THD figure than the hard switching converter, provided optimisation of the values of the resonant components is undertaken.

The current rating of the devices in the RDCLI is the same as for an equivalently rated hard-switching converter, though the required voltage rating is approximately 1.4 times greater depending on the clamping arrangement.

Additional areas of study may be identified: The upper power limit for RDCLIs is currently considered to be around 200kW but this has not been fully discussed in the literature. There may be scope to improve this figure, which has been attributed to the point at which losses in the resonant components become excessive.

For rail traction applications the input impedance of converters is very important since harmonics in the supply voltage may cause interference currents to flow into the converter. This may be investigated by analytical means [28], or by the use of computer simulation.

A study into the transient stability of the Resonant DC Link Inverter would be useful, especially for rail traction applications where the supply is frequently interrupted by intentional gaps in the electrical feed, or by contact bounce. This could cause problems in the maintenance of resonance. Mitigation of instability in the presence of transients could form the basis for further study, possibly involving the use of DSP chips to provide a rapid reaction to changing circuit conditions.

In summary, it may be concluded from the above that Resonant DC Link Converters can offer benefits in rail traction use; advances can be made in terms of converter size, weight, and interference problems. The modulation schemes proposed in this work also allow harmonic control in a manner not previously possible, enabling signalling frequency avoidance and psophometric current minimisation to be achieved. Using appropriate clamping, RDCLIs may be used without pre-conditioning choppers on 750V DC supplied rail systems using currently available devices. However, the upper power limit for the RDCLI of 200kW restricts application to auxiliary converters and perhaps light rail packages.

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Appendix

Copies of Published Work

In this section, the papers listed below are presented. All the papers were written by P. Ellams and Dr A.D. Mansell.

i. "Simulated annealing in the analysis of resonant DC link inverters", *IEE Proceedings-B*, **Vol.141, No.3**, May 1994, pp.163-168.

ii. "Using resonant DC link inverters in traction auxiliary supplies", *IMechE Railtech '94 Conference Record*, **Vol. C478/11/042**, May 1994.

iii. "Soft-switching single-phase to three-phase converters with near unity power factor", *accepted for publication in IEE Proceedings-B*.

Simulated annealing in the analysis of resonant DC link inverters

P. Ellams, BEng
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Indexing terms: Resonant DC link inverter, Simulated annealing, Optimisation, Sigma-delta modulation, Harmonic elimination

Abstract: A technique is proposed for calculating preprogrammed modulation patterns for convertors having outputs comprising discrete pulses, such as the resonant DC link inverter. The problem is one of large-scale combinatorial optimisation. An algorithm based on simulated annealing is introduced which proceeds by minimising a cost function that describes the system parameters which are to be optimised. Results are presented using an example cost function appropriate for implementing an approximation to harmonic elimination. Harmonic spectra are included which allow comparisons to be made between simulated annealing, 'conventional' optimisation techniques, and sigma-delta modulation. Simulated annealing is found to allow improved control of the spectra generated by discrete pulse convertors.

1 Introduction

Despite the considerable advances that have been made in the design of power semiconductor devices, one of the limitations that continues to constrain the designers of equipment utilising them are the switching losses. These are the losses that occur when a power device is switched on or off; the switching process demands finite time and a period exists when both the current through the device and voltage across it are not zero. The energy loss manifests itself as heat and this is in addition to the conduction losses.

It follows therefore, that if the switching frequency is raised, even to relatively modest frequencies, the energy dissipation caused by the switching increases and can become comparable to the conduction losses. Given that there is a maximum permitted temperature that can be sustained within a device before failure occurs, a limit to these losses exists above which reliable operation cannot be maintained.

Because there are a number of applications, and inverters are one of them, where this limitation is a major restraint, designers have sought to reduce or eliminate the switching losses and therefore extend the upper switching frequency limit. One solution is to ensure that at the instant of switching, either the current or the voltage in the circuit is temporarily zero. In pursuance of this, a technique that has received considerable attention is the resonant DC link (RDCL) inverter [1, 2].

In many inverter applications it is desirable, and sometimes essential, to control the harmonic content of the output. Techniques such as pulse width modulation (PWM) are used and to achieve the desired harmonic content the DC link voltage is switched at closely controlled instants.

A restriction that resonant DC link inverters impose is that there is no longer complete freedom to choose the instant when the switching occurs. To achieve the aim of eliminating the switching losses, the inverter switches can only be switched when the link voltage passes through zero under the action of the resonant circuit. This means that harmonic elimination is that more difficult and this paper describes a method that can be used to optimise this process.

2 Harmonic elimination in inverters

From the inception of power inverters, designers have been conscious of the need to control the harmonic content of the output. Early computational work concentrated on the calculation of the magnitude of the harmonics and this in turn gave way to efforts to formulate general rules that could be invoked to ensure either harmonic elimination or minimisation.

The major breakthrough could be described as the paper by Patel and Hoft [3]. The basic premise was that given the desire to eliminate certain harmonics, then by utilising the technique of pulse width modulation (PWM), it should be possible to compute the phase angles at which the 'chops' must occur to achieve it. The technique demands the solution of a set of nonlinear equations, and in addition to a description of the generalised methods, solutions were presented for the elimination of up to five harmonics. The paper demonstrated that it is possible to eliminate as many harmonics as there are chops per halfcycle.

The accuracy of the phase angles of the 'chops' was ahead of the technology of the time. However, since then, even though the precision of the method is adversely affected by the inconsistent, finite switching times of the device, the advent of microprocessor control has seen its wide implementation.

In principle, the technique can be applied to inverters incorporating a resonant DC link. However, the fact that switching is only permitted when the link voltage is zero means that the complete freedom of action that Patel and Hoft assumed, is not open to the designer. Instead, a less than optimum implementation must be accepted and the

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problem that presents itself is that of optimising the harmonic content of the output to satisfy the specification of the particular application.

It should be added that although the RDCL permits switching only at certain prescribed points, an important bonus is the ability to increase the number of chops and thus improve the control of the output waveform, with no thermal penalty.

3 Optimisation of the harmonic content of RDCL inverters

The output waveform generated by an inverter employing a resonant DC link is synthesised from a series of identical positive and negative polarity pulses. The pulses are of a relatively high frequency compared to the fundamental component of the output waveform, and the harmonic content is determined by the combination of the number and location of the positive and negative pulses in the output waveform.

Generally, in systems using precalculated switching patterns, the output waveforms are made to have quarter wave symmetry in order to eliminate all even harmonics. Because of this symmetry, the problem of deciding on the form of the synthesised waveform and its analysis is reduced somewhat. However, a considerable optimisation problem still exists. Some measure of this can be gained from the example of a 50 Hz output being produced from a DC link that resonates at 20 kHz. For such an inverter, each full cycle of the output will be synthesised from a combination of 400 positive and negative polarity pulses.

If quarter wave symmetry is assumed, it still means that each quarter wave will be formed from a combination of 100 pulses. These 100 pulses can be arranged into 2^{100} different combinations and the predicament facing the designer is to choose from this very large number, the combination that will produce the best output in terms of spectral content and harmonic distribution for the particular application under consideration.

In the early 1980s, the use of delta modulators in the control of inverters was reported and Kheraluwala and Divan [4] described their use in the control of resonant link inverters. Of these the sigma-delta modulator has much to commend it. It operates by a sampling method and maintains a volt-second balance between its output and a reference, which, in the case of an inverter of the type under consideration, will be a sinusoid.

A schematic diagram of the circuit is shown in Fig. 1. The comparator switches in response to the sign of the

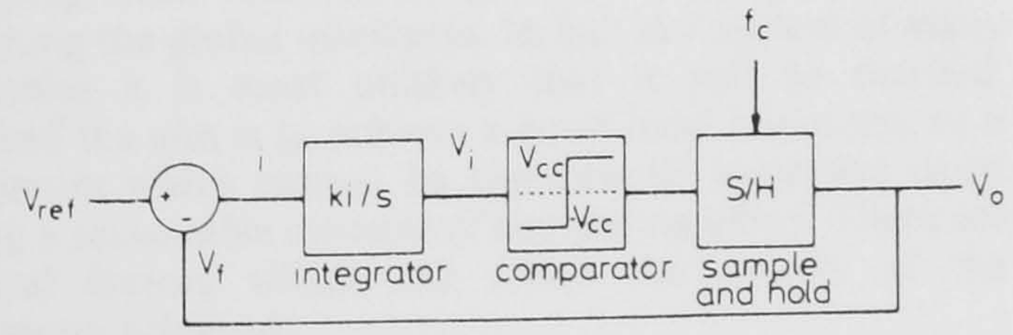

Fig. 1 *Sigma-delta modulator*

integral with respect to time of the difference between the reference signal and the feedback signal. The output is stored in a sample and hold circuit and this is updated at the sampling frequency (f_c).

Kheraluwala and Divan found that this type of modulator, which runs in real time, offered effective harmonic minimisation although significant harmonic energy existed at subharmonics of the sampling frequency. This is a characteristic of sampled control systems. Another way of implementing modulation of inverters is by the so-called preprogrammed method whereby the switching pattern is calculated offline and stored in a look-up table or encoded in an easily calculated algorithm to allow it to be recalled by the inverter control system. An advantage of preprogramming is that sophisticated control algorithms may be applied since the time for computation is not critical. It is this type of modulation method which is proposed in this paper.

4 Simulated annealing in function optimisation

The optimisation of a function y means finding its maximum or minimum value. For clarity the discussion here will refer exclusively to minimisation, although the principles underlying the two operations are identical. A minimisation procedure can be converted to maximisation by simply changing the sign of y. In engineering the interest in function optimisation stems from the desire to adopt the best solution to a problem from many possibilities. For example, y may represent the area of silicon required for an IC, or the amount of copper wound on an inductor, or a complicated function of several design variables. Finding an extremum of y then indicates the optimum design which can be achieved. The function y may be considered to be a measure of 'goodness' of the design, and where minimisation is the aim, high values of y correspond to a penalty, or high *cost*. Hence y is referred to as the *cost function*.

In real engineering problems y is not usually a simple function, and as a consequence will have many *local minima*, as shown in Fig. 2. In this diagram y is a function

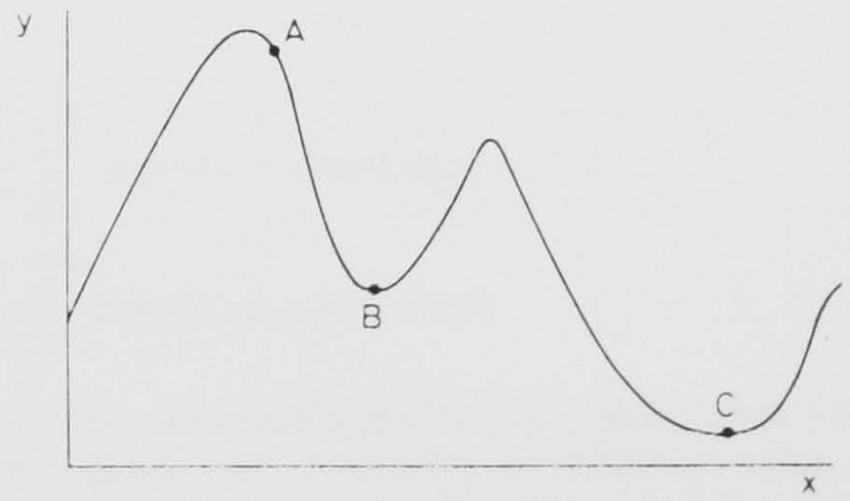

Fig. 2 *Local and global minima*

of one variable, x. Suppose y is evaluated initially at A, and small changes are made in x such that the value of y is reduced. This process could be repeated until point B was arrived at, where y would stop decreasing. The function increases either side of B so it is known that a minimum has been located but it is only a *local* minimum. By inspection it can be seen that the overall *global* minimum is at C. This example is a trivial one, but it demonstrates that simply moving 'downhill' on a function until it stops decreasing does not necessarily lead to the function's minimum point, and can cause the algorithm to get stuck in the local minimum. When analysing a function of many variables this becomes a serious problem and will frequently prevent a good extremum from being located. Despite this significant deficiency, many optimisation algorithms operate in this manner, by improving the cost function with every step until no further improvements are possible, i.e. by moving

towards the nearest minimum. This is not the case with simulated annealing techniques [5–7].

In simulated annealing algorithms a proposed change in the variables which cause a decrease in function y (i.e. a downhill step) is always accepted, but additionally a proposed change which causes an uphill move is sometimes accepted. The criterion for acceptance is the value of a probability function as explained below. Because uphill steps can be accepted there is a finite probability of the algorithm 'jumping out' of a local minimum, and moving towards a different, and hopefully better, extremum. Initially many uphill moves are accepted allowing a large amount of the variable space to be explored. As the optimisation procedure advances, the probability of acceptance of an uphill step is gradually reduced, allowing improvements in the cost function to be achieved but also giving the chance of escape from local minima. Eventually the probability of uphill moves becomes so low that the algorithm settles into a minimum from which it cannot escape.

As implied by its name, simulated annealing has many analogies with the way in which materials order themselves during the cooling or annealing process. At high temperatures substantial atomic rearrangement is possible. If the temperature is reduced slowly enough, the degree of freedom of the constituent particles gradually reduces until the material freezes into an ordered state. The ordered, or crystalline, state of a material usually corresponds to a low-energy condition. In simulated annealing algorithms, the proposed moves produce changes in the cost function which correspond to the energy changes incurred by atomic arrangement in nature. In the natural annealing process the probability that an energy change ΔE will occur is governed by the Boltzmann probability distribution as given in eqn. 1, where T is temperature and k is Boltzmann's constant:

$$P(\Delta E) = \exp\left(\frac{-\Delta E}{kT}\right) \tag{1}$$

Thus the larger the attempted energy change, the less likely it is to occur, but overall, the probability of a given change is greater at higher temperature. By analogy, in the simulated annealing process the Boltzmann probability distribution is used to describe the probability of an uphill move in cost function y having magnitude ΔE. It is useful to still refer to T as 'temperature', but the constant 'k' is no longer Boltzmann's constant; it is a scaling factor appropriate for, and peculiar to, the application.

Although this method provides the possibility of escaping from local minima, there is no guarantee of reaching the global minimum. In fact in a system of many variables it is most unlikely that it will be reached. Instead the aim is to achieve a good local minimum, or a minimum which cannot be significantly improved upon using a reasonable amount of computing effort. There are several factors which can affect the quality of the minimum achieved.

(i) Starting temperature: this affects the initial 'random' variable space search.

(ii) Cooling schedule: i.e. how quickly the temperature is reduced. This has a powerful influence on the amount of variable space which is searched, and thus on the quality of the final result.

(iii) Starting point: if the algorithm is given a starting point which is in the vicinity of the global minimum it is likely to give a much better result than a random starting point.

The theory behind simulated annealing is fairly straightforward. Most of the complications in its application arise from selecting the appropriate cooling schedule and cost function. It is important that the cost function accutately reflects, with suitable weighting, the parameters that are required to be optimised.

5 Simulated annealing in this application

5.1 General principles

As explained above, the output of a clamped RDCL inverter is determined by the combination of positive and negative pulses selected from the resonating link. Consequently the number of possible configurations is finite, though very large. The problem is one of combinatorial optimisation and can be conveniently expressed in matrix notation. Consider a general pulse train typical of the output of clamped RDCL inverters as shown in Fig. 3. Let this be the function $pu(\omega t)$.

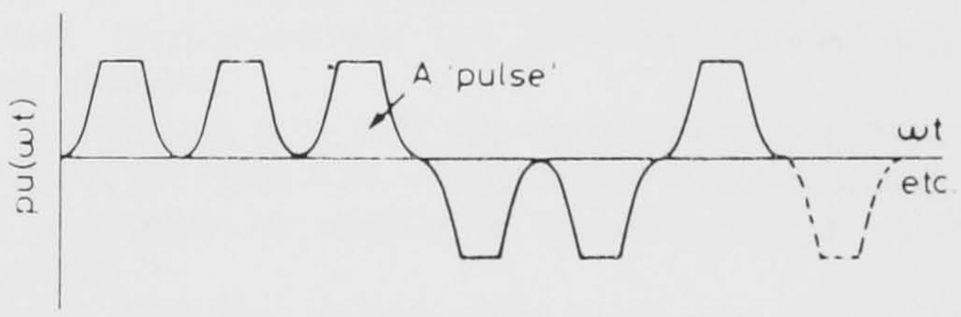

Fig. 3 *Clamped RDCL inverter pulse train*

The objective is to control the harmonic content of $pu(\omega t)$, consequently it is necessary to perform a Fourier analysis. The Fourier series is given by

$$pu(\omega t) = \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \tag{2}$$

where

$$a_n = \frac{1}{\pi}\int_0^{2\pi} pu(\omega t)\cos(n\omega t)\, d(\omega t) \tag{3}$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} pu(\omega t)\sin(n\omega t)\, d(\omega t) \tag{4}$$

In general, the modulation process determines that $pu(\omega t)$ shall have quarter wave symmetry to eliminate even harmonics, consequently a_n is zero for all n. Also the expression for b_n may be rewritten as follows:

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} pu(\omega t)\sin(n\omega t)\, d(\omega t) \tag{5}$$

Let s_n be the function which determines the sign of the nth pulse. This gives the matrix notation as shown in eqn. 6, where $\boldsymbol{r}$ denotes the Fourier integral evaluated over the period of individual pulses. R is the number of pulses in each cycle of the synthesised output waveform. The general term of matrix $\boldsymbol{r}$ is r_{ij} as defined by eqn. 7., where T_p is the period of one resonant pulse.

$$\begin{bmatrix} r_{11} & r_{12} & r_{13} & \cdots & r_{1(R/4)} \\ r_{21} & r_{22} & \cdots & \cdots & r_{2(R/4)} \\ r_{31} & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ s_3 \\ \cdots \\ s_{(R/4)} \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ \cdots \\ \cdots \end{bmatrix} \tag{6}$$

$$r_{ij} = \frac{4}{\pi}\int_{(j-1)\omega T_p}^{j\omega T_p} PU(\omega t)\sin(i\omega t)\, d(\omega t) \tag{7}$$

$PU(\omega t)$ is a function having the same basic shape as $pu(\omega t)$, but with positive pulses only. Due to the quarter wave symmetry b_n is zero for even n. A cost function may now be derived in terms of the remaining b_n. The optimisation process is concerned with finding the form of s such that the cost function is minimised.

5.2 The cost function

The cost function consists of two elements: the first determines the amplitude of the fundamental component (b_1) of $pu(\omega t)$, and the second encourages the algorithm to minimise the amplitudes of a given number of harmonics. The fundamental amplitude control is achieved by assigning a high value to cost function y if b_1 is more than 5% in error of the desired amplitude, but assigning no cost if it is within this limit. The second element of the cost function is a value derived from the sum of the amplitude of harmonics which are to be minimised, together with a weighting which favours the largest decreases in the low-frequency harmonics. Mathematically this may be written as follows:

$$\left|\left(\frac{b_1 - ideal}{ideal}\right)\right| \times 100\% \leqslant 5\%:$$

$$COST = \sum_{q=1}^{q_{max}} \left|\left(\frac{q_{max} - q + 1}{q_{max}}\right) \times b_{(q)}\right| \tag{8}$$

$$\left|\left(\frac{b_1 - ideal}{ideal}\right)\right| 100\% > 5\%:$$

$$COST = 10^6 + \sum_{q=1}^{q_{max}} \left|\left(\frac{q_{max} - q + 1}{q_{max}}\right) \times b_{(q)}\right| \tag{9}$$

where q is the qth harmonic to be minimised, q_{max} is the total number of harmonics to be minimised, $b_{(q)}$ is the amplitude of the qth minimised harmonic and *ideal* is the amplitude of the ideal fundamental component.

Many different cost functions could be devised, the specific application determines the characteristics that are considered to be 'good'. In this case a 'good' output spectrum is one in which the controlled harmonics have very low values. Another cost function might, for example, attempt to minimise total harmonic distortion (THD). It is important that all quantities which are required to be minimised are included in the cost function. Using the cost function given as an example above, it may be found that as the controlled harmonics are minimised, the THD rises. If this rise is unacceptable, a further element must be included in the cost function to control it. This means that in practice the cost function becomes the only way in which harmonic spectra may be compared since the user should have confidence that it is the ultimate test of 'goodness' for a particular application. If this confidence is not achievable it implies that the cost function needs amending.

5.3 Proposed moves

In order to improve the chances of achieving a 'high quality' minimum, sigma–delta modulation ($\Sigma\Delta M$) is used to define the starting point for matrix s. $\Sigma\Delta M$ provides a modulation pattern with a fairly well defined fundamental amplitude, and reasonably small low-frequency harmonics. The simulated annealing algorithm proposes amendments to s by sequentially cycling through the elements of s, reversing their sign and re-evaluating the cost function. If the sign reversal improves the cost function the move is accepted, if it causes an increase in cost (i.e. an uphill step) acceptance is dependent on the probability eqn. 1. The equation is evaluated for the current temperature and compared againt a pseudo-randomly generated number which takes values between 0 and 1. If the random number is less than the value of eqn. 1 the uphill step is accepted. Otherwise the element of s concerned is returned to its original value.

5.4 Cooling schedule

The cooling schedule has enormous influence over the quality of the final result. The process of finding a good schedule relies on a great deal of trial and error, intutition and some insight into the particular application. The first requirement is to set the scaling factor k in eqn. 1. For example in the tests described below, k, was set such that the probability of acceptance of a typical uphill step was 0.1 when the temperature was 1. This demands a 'feel' for the size of typical function changes (ΔE). After much experimentation the following cooling schedule was adopted:

(i) Starting at $T = 0$, the temperature is increased in steps of 0.1 until 10% of uphill moves are accepted. This is analogous to melting a material in the annealing process.

(iii) Cooling: during each cycle, the sign of every element of s is reversed to propose a move, as described above. Between cycles the temperature is reduced by 0.5%. This continues until no improvement in the cost function can be achieved.

(iii) Step (ii) is repeated twice using starting temperatures of 50% and 33% of the original.

By incorporating the 'melting' process, the algorithm finds its own starting temperature, appropriate to the particular problem. The initial figure of accepting 10% of uphill moves was used after it was found that allowing too many uphill moves to be accepted initially dissipated the benefit gained from using $\Sigma\Delta M$ as a starting point.

5.5 Practical applications

In practical systems it is usual that an inverter is required to generate variable magnitude and variable frequency outputs. Consequently, the above process would be repeated over a range of different fundamental magnitudes and number of pulses (i.e. frequency). The resulting modulation patterns would then be stored in a look-up table for later use by the inverter. Storage of patterns for resonant DC link inverters can be done very efficiently. For example, a pattern having quarter wave symmetry and comprising 100 pulses per quarter cycle may be stored as a 25 digit hexadecimal number. Even where many patterns must be stored the notation is very compact. During operation the inverter controller simply selects the pattern appropriate for the demanded magnitude and frequency conditions, and converts it to a quarter wave symmetrical binary sequence.

6 Results

Typical results are shown to allow comparison to be made between simulated annealing, and a search method which never accepts uphill steps. This second method will be referred to as the 'direct search' method. The same

Table 1 : Comparison of search methods

Test	Nominal fundamental	Number of controlled harmonics	Initial cost function value (sigma-delta modulation)	Final cost function value (direct search)	Final cost function value (simulated annealing)	Percentage improvement in cost function
1	0.8	9	0.078796	0.0400	0.0378	5.50
2	0.55	14	0.129647	0.0832	0.07946	4.50
3	0.55	4	0.041216	0.0289	0.0047	83.7
4	0.2	12	$>10^6$	0.1212	0.0379	68.7
5	1.0	14	0.128366	0.1284	0.110	14.3
6	0.65	19	0.18822	0.1364	0.126	7.62
7	0.35	12	0.052944	0.0529	0.0409	22.7
8	1.15	11	$>10^6$	0.1304	0.077	41.0

cost function was used for each method, and moves were suggested in the same manner. To aid comparison some results are shown in tabular form and some in graphical form.

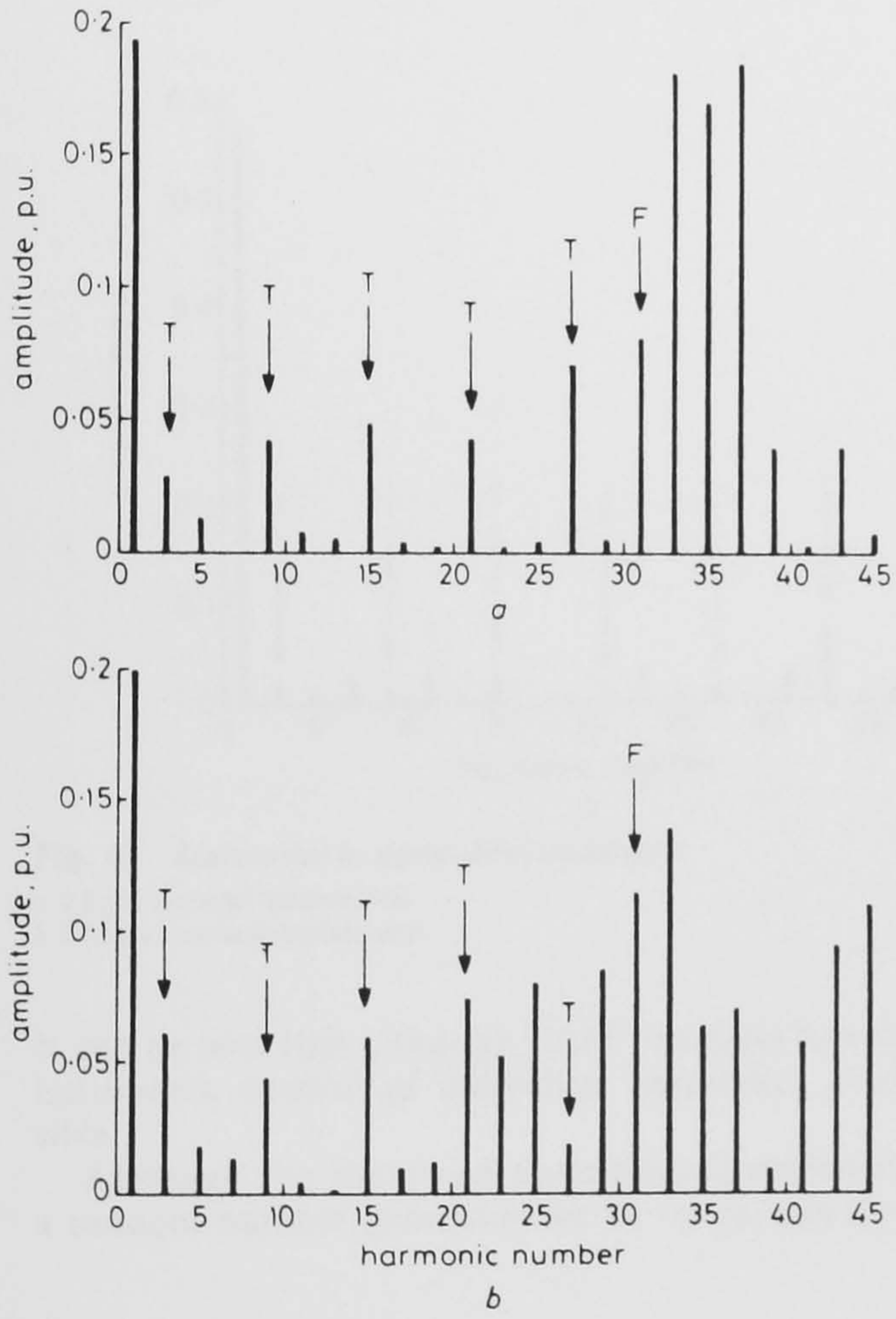

Fig. 4 *Comparison of spectra*
a simulated annealing
b direct search

Table 1 shows cost function values obtained using simulated annealing and direct search methods. In every case it can be seen that some improvement in cost function was possible. This was found to be true in all tests, though it cannot be proved mathematically. The 'number of controlled harmonics' refers to the number of odd, nontriplen harmonics which the cost function attempted to minimise. Additionally, the fundamental was controlled to within 5% of a given nominal value. The fourth column of the table shows the initial value of cost function obtained after applying sigma-delta modulation. This indicates how the final cost function value compares with the starting value in each case.

Fig. 4*a* and *b* show, respectively, the theoretical harmonic spectra for a clamped resonant DC link inverter using switching strategies derived by the simulated annealing technique and direct search technique. These were obtained by evaluating eqn. 6. The nominal fundamental is 0.2 p.u. Nine harmonics were minimised. It can be seen that it is possible to reduce the amplitude of the harmonics to very low values. Typically harmonics can be reduced to less than 2.5% of the fundamental amplitude. Triplen voltage harmonics do not cause currents to flow in three-phase loads without a neutral line, consequently no attempt was made to minimise them. Odd triplens are marked on the spectra with a 'T'. The harmonic labelled 'F' denotes the first unminimised nontriplen harmonic. Fig. 5 demonstrates how a band of harmonics,

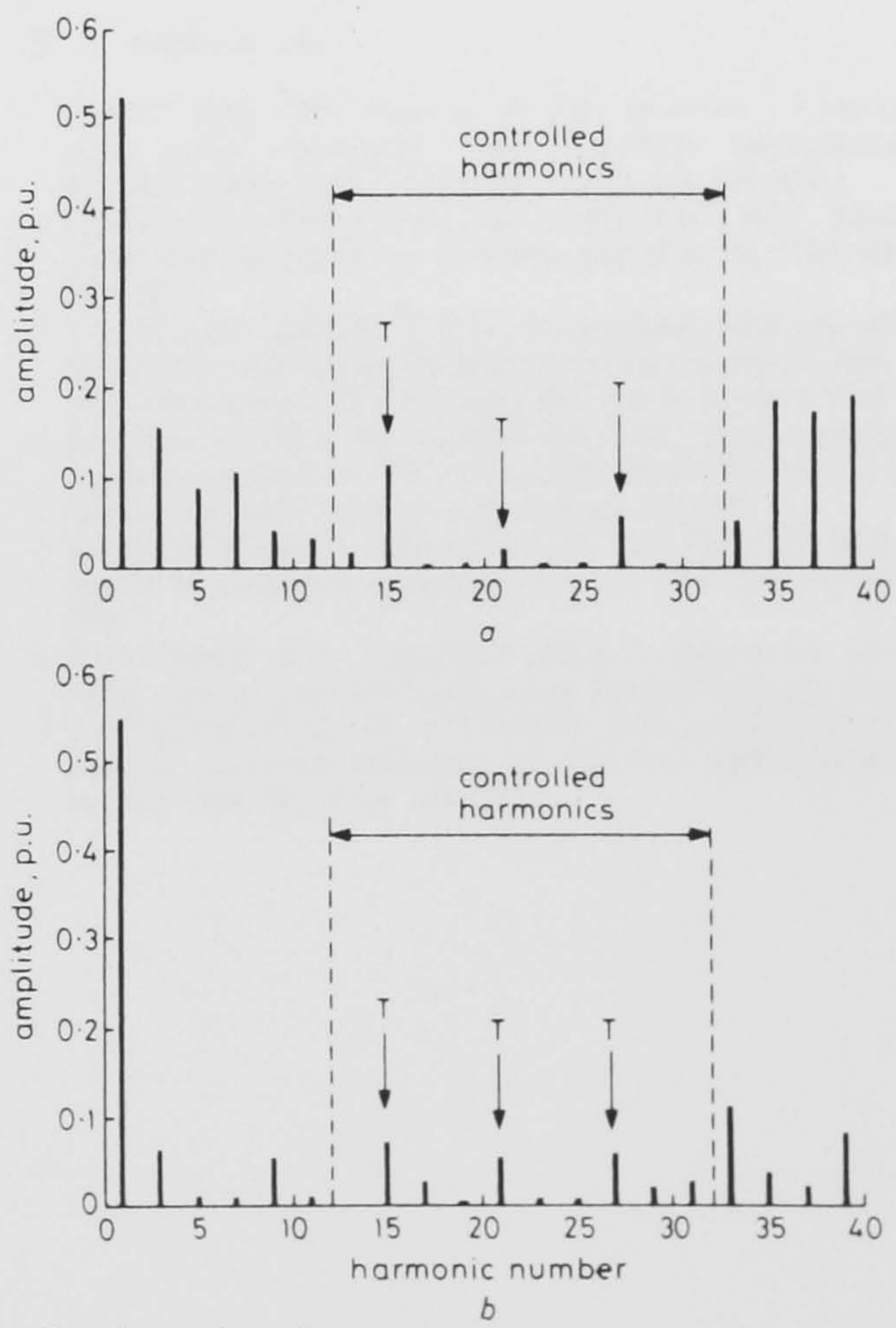

Fig. 5 *Comparison of spectra*
a simulated annealing
b direct search

remote from the fundamental, may be minimised. In this test seven harmonics were minimised starting with the 13th. The nominal fundamental value is 0.55 p.u. Fig. 6 shows the spectra obtained by computer-simulated sigma-delta modulation, which is used as the starting

point for the simulated annealing process. Fig. 6*a* was obtained using the same conditions used for Fig. 4, and Fig. 6*b* was obtained using the same conditions as Fig. 5.

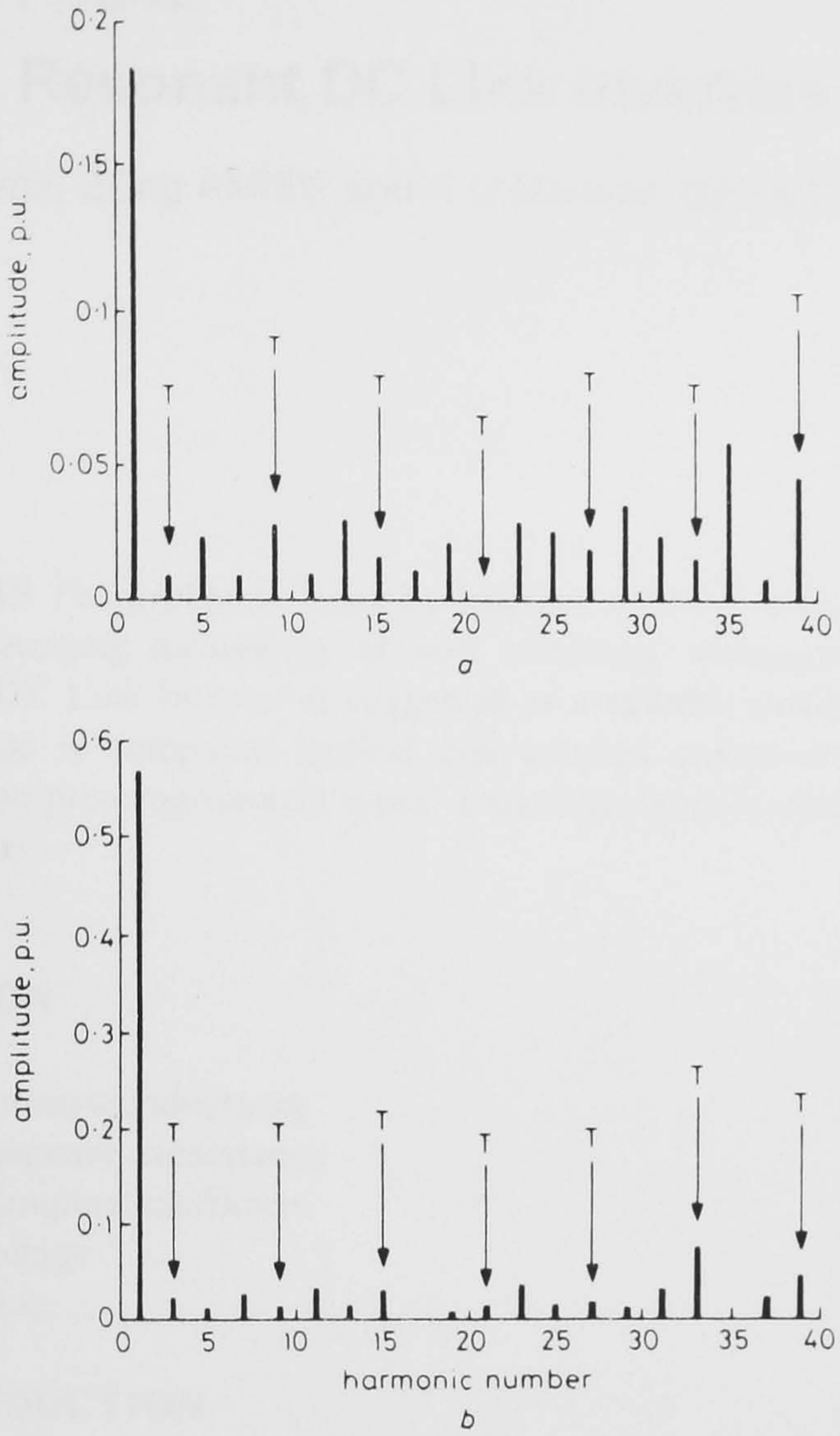

Fig. 6 *Spectra due to sigma–delta modulation*
a 0.2 p.u. nominal fundamental
b 0.55 p.u. nominal fundamental

It can be seen that although ΣΔM produces low values of harmonics, control of individual harmonics is not possible.

Although the simulated annealing algorithm relies on a random number generator for its operation, the results shown above are repeatable if the system is cooled slowly enough.

7 Conclusions

Simulated annealing has been shown to be an appropriate tool for tackling the problem of large-scale optimisation that is encountered when attempting to calculate preprogrammed patterns for resonant DC link inverters. The proposed method requires only modest computing facilities. The results shown were calculated on a desktop PC, taking around 15–20 minutes per run. It is not possible to say how close the final results are to the global minima, although comparisons can be made with optimisation techniques which accept only downhill steps. These show that simulated annealing offers an improvement in the minimum which can be obtained. The magnitude of this improvement depends on how good a minimum was found in the first instance.

The cost function suggested in this paper is one suitable for approximating harmonic elimination. However, many other cost functions could be derived to optimise different parameters. The theorem of simulated annealing could also be applied to other types of resonant convertors and indeed, to many other engineering problems which require optimisation for their solution.

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Using Resonant DC Link Inverters in Traction Auxiliary Supplies

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SYNOPSIS The problems faced by traction auxiliary converters employing hard-switching devices are examined, and the emerging technology of 'soft switching' introduced which promises to alleviate these difficulties. The Resonant DC Link Inverter is suggested as a suitable soft-switching topology for the traction environment, and its performance is compared against conventional converters. Control strategies are examined with a particular emphasis on pre-programmed types. Experimental data obtained from a low-power test rig is presented in support of the theory.

NOTATION

L_r	Resonant inductance
C_r	Resonant capacitance
k	Clamping coefficient
V	Voltage
t	Time

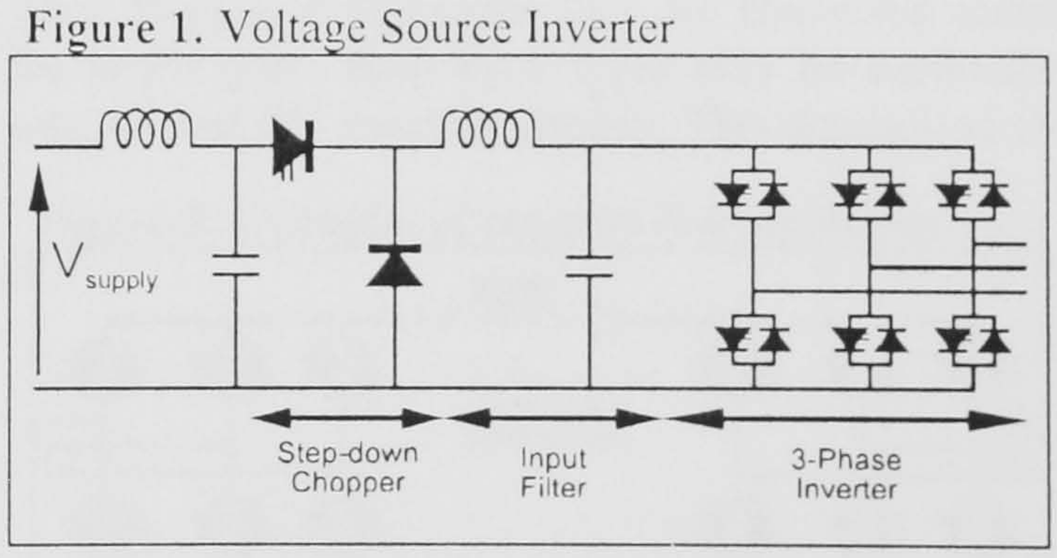
1. INTRODUCTION

Traction auxiliary converters perform an important function, supplying power to systems essential for passenger comfort, safety, and normal train operation. Increasing levels of sophistication in traction vehicle equipment are placing ever higher demands on the specification of auxiliary converters. The generated waveforms must be of very high quality, but the converter needs to be as small and light as possible. The failure of an auxiliary converter can make a vehicle unusable, consequently reliability is also an important consideration, to prevent loss of revenue. The replacement of Motor-Alternator (MA) sets by the static converter as a source of auxiliary power met many of the requirements in terms of reduced maintenance and increased flexibility. However these converters are usually based on conventional 'hard-switching' technology and tend to be larger than equivalently rated MA sets. Further, the quality of the generated waveforms is limited by the low switching frequencies. These problems can be traced to the high switching loss of 'hard-switching' converters. 'Soft switching' is an emerging technology which addresses some of the problems of conventional converters by reducing the switching loss to very low values. The two methods of switching are compared in more detail below.

2. STATIC AUXILIARY INVERTERS

Static converters have effectively replaced the Motor-Alternator set as the means of generating appropriate supplies for auxiliary loads on railway vehicles(1). The most common circuit configuration is based on the Voltage Source Inverter (VSI) as shown in Figure 1.

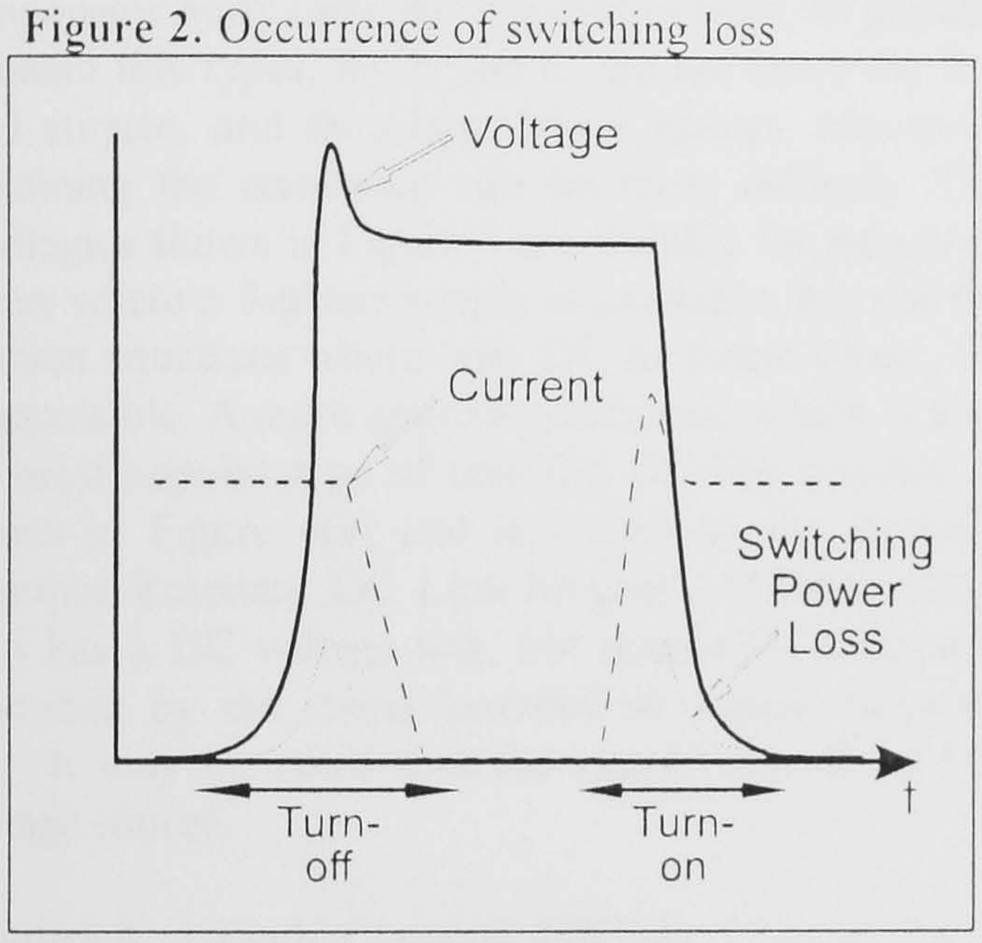
Figure 1. Voltage Source Inverter



This circuit is popular due to its extreme simplicity (only six switching devices are needed), its well understood design procedure, and the fairly simple control strategies which may be used. However each time one of the inverter switches is required to turn on, or turn off, energy is dissipated in the switch in addition to the conduction losses. This occurs because during switching, the device experiences simultaneously, high levels of voltage and current as shown in Figure 2. The switching loss forms a significant proportion of overall device losses. To

prevent overheating, a limit exists on the amount of power which may be dissipated in a switching device with a given heatsink. Consequently this limits the frequency at which a device may be switched. Operating frequencies for such converters are typically less than 5kHz. This low frequency results in high harmonic content of the converter waveforms, which demands large, costly filters. Higher switching frequencies enable smaller filters to be used, but necessitate larger heatsinks for the power devices. Thus a trade-off exists between filter and heatsink size.

Figure 2. Occurrence of switching loss



In inverters of the type shown in Figure 1, *snubber networks* are placed in parallel with power devices to provide protection from over-voltage during commutation. Snubbers may also be used to reduce device switching loss by diverting voltage and current during switching. However the *overall* switching loss is not reduced, and may even be increased, and still leaves the problem of dissipating the energy from the snubber network. Energy recovery (loss-less) snubbers are available, but the penalty for their use is a significant increase in circuit complexity. An additional problem is caused by the abrupt changes in voltage and current which occur during switch modulation which can cause Electromagnetic Interference (EMI), and subject the devices to high levels of stress.

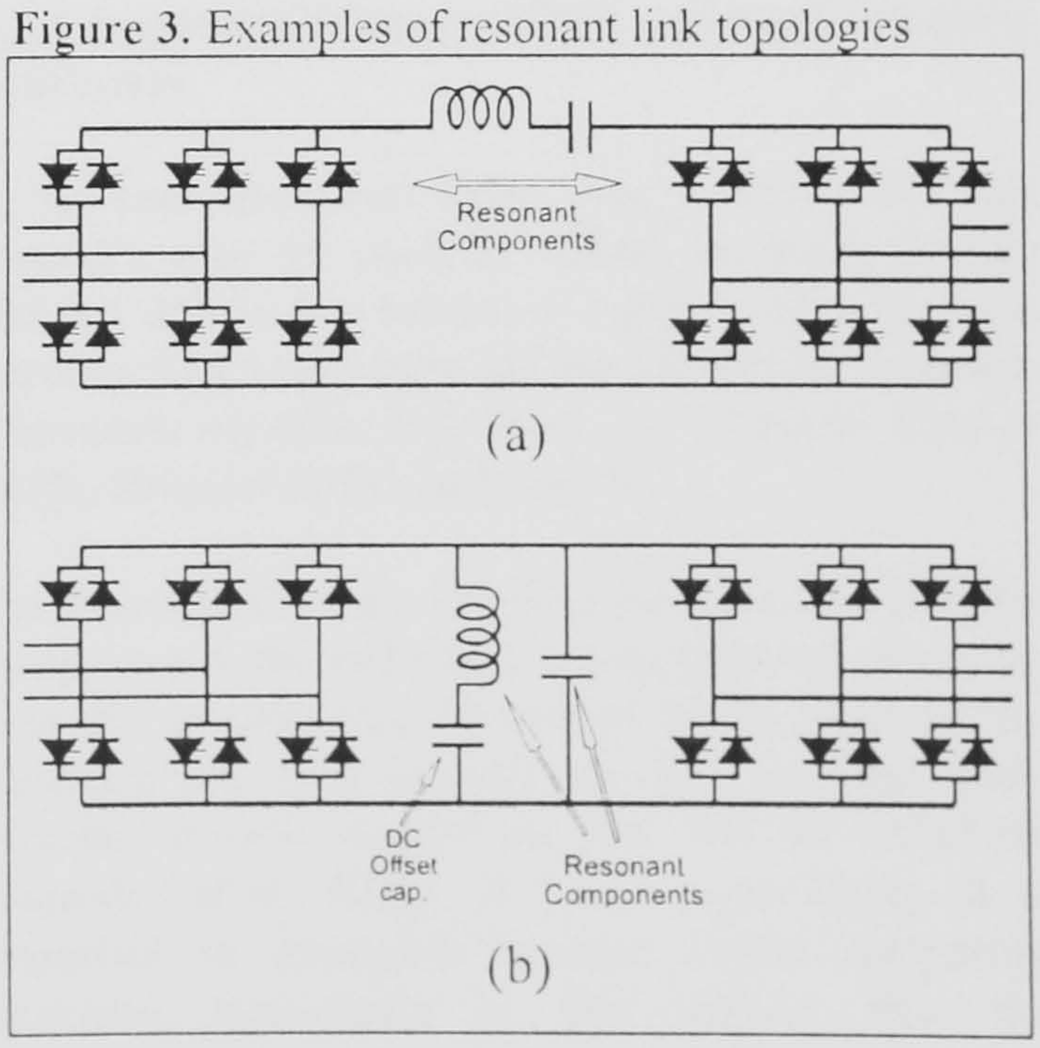
3. INTRODUCTION TO RESONANT INVERTERS

Soft switching is currently receiving a considerable amount of attention as a means of alleviating the problems of switching loss described above(2,3). In soft switched converters the voltage across the devices, or current through them is brought smoothly to zero at periodic intervals. Under these zero voltage or current conditions the switches may be commutated without any energy loss. This differs from *hard switching* where the switches are used to inflict abrupt changes on the voltage or current. As implied by their name, resonant converters achieve soft switching by means of a resonant Inductance-Capacitance (LC) circuit. The function of the resonant components is to produce the periodic voltage or current zeros. In practice there is always some loss associated with commutating devices, but soft switching converters reduce it to very low values. This enables the frequency of switching to be raised significantly. The higher switching frequency offers the potential for improved harmonic control of the converter output, and increased power density (i.e. smaller volume or increased throughput). There are also other important advantages:

- In some topologies device snubbers are not required. This has implications in terms of cost, and improved reliability.
- Due to reduced rates of change of voltage (dV/dt) there is a reduction in radiated Electromagnetic Interference (EMI).
- Device turn-on and turn-off stresses are reduced.

Many different converter topologies are possible. Additionally they may be classified in many different ways. One system of classification indicates the manner in which the resonant components are connected in circuit, which yields the names *parallel link*, and *series link* circuit. In series link circuits the L and C components lie in series with the path of power flow. In parallel topologies they are connected across the power path. Both these types may be subdivided into *AC* and *DC* resonant circuits. This depends on the

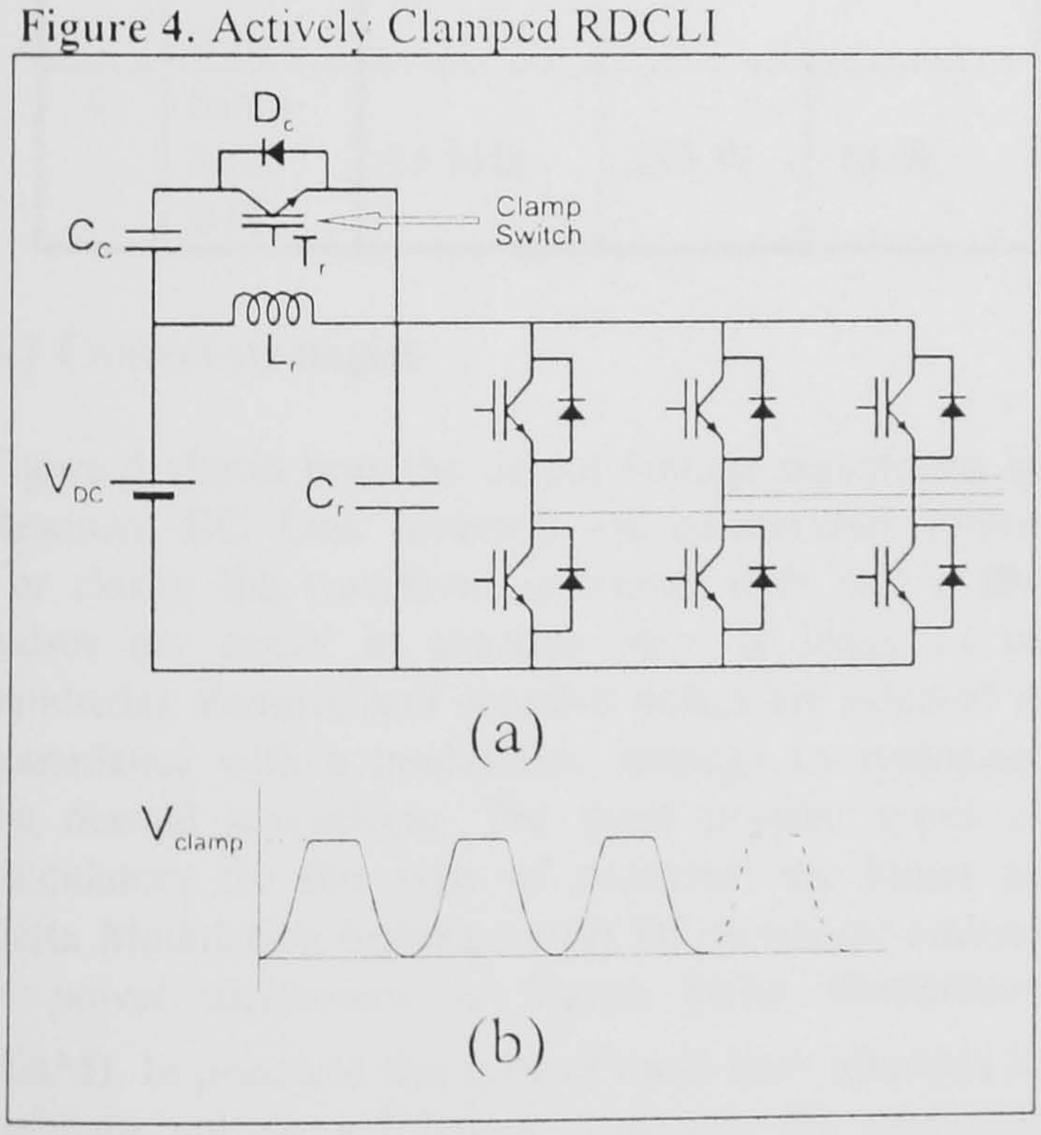
Figure 3. Examples of resonant link topologies



manner in which the resonant components operate. In AC types the L and C experience bi-directional voltages and currents. In DC types the voltage or current has a DC offset such that it pulsates but does not cross zero. Figure 3(a) shows an example of a series-resonant AC link converter, Figure 3(b) shows a parallel-resonant DC link converter.

Series resonant links switch at zero *current* points, which allows the use of naturally commutated devices which are cheap and rugged. However both resonant components must carry the full load current. In parallel resonant link types, the L and C do not carry the full load current, and thus have lower ratings. However, sustaining the resonance can be more difficult. The topologies shown in Figure 3 are suitable for industrial drives where a 3-phase supply is available, but not for traction situations where only DC or single phase AC is accessible. A more appropriate circuit, which is also the most popular type of resonant DC-link inverter, is shown in Figure 4(a) and is known as the Actively Clamped Resonant DC Link Inverter (ACRDCLI)(**4**). This has a DC voltage link, but cannot be accurately described by the terms 'parallel' or 'series' resonant link. It may be noted that the supply is a fixed DC voltage source.

Figure 4. Actively Clamped RDCLI



In this circuit the link voltage periodically resonates down to zero as shown in Figure 4(b). At this point any required commutations take place. The link frequency is typically 20 to 60 kHz. A significant feature of this circuit is the use of clamping. The clamp performs protection and control functions. Firstly the link voltage excursions are limited by the diode D_c and clamping capacitor C_c. The voltage on C_c is controlled typically to 0.2-0.4V_s, where V_s is the DC supply voltage. Consequently this limits the maximum voltage applied to the switching devices to 1.2-1.4V_s. To achieve the necessary link frequencies, and to simplify the base drive requirements, the most suitable switching device is currently the Insulated Gate Bipolar Transistor (IGBT). A nominal 750V DC railway supply may vary between 400 and 900 Volts. Thus, by selecting a clamping level of 1.4V_s implementation of an ACRDCLI, without a pre-conditioning chopper, is possible using currently available 1.7kV IGBTs. The second function of the clamp is to control the resonance of the link. During operation, the voltage on the resonant capacitor C_r swings upwards until diode D_c forward biases, allowing the resonant current to flow into the clamping capacitor C_c. Eventually this current reverses, flowing back through transistor T_r. T_r is turned off at a point in time calculated so that the voltage on C_r resonates back to zero without significant overshoot, or undershoot. This allows the resonance to be controlled on a cycle-by-cycle basis.

It is possible to implement the clamp using passive, rather than active components. This gives an extremely robust and low-loss topology, but the inverter devices experience voltages as high as 2V_s. Consequently this is not a viable option for operation from traction supply voltages at the moment, but may be the preferred choice when higher voltage devices become available.

4. CONTROL AND DESIGN CONSIDERATIONS

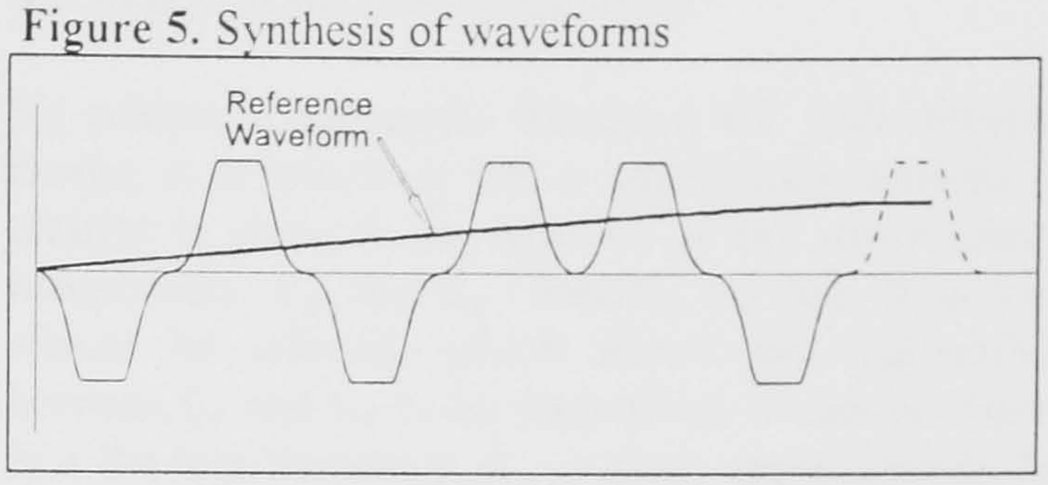
4.1 Comparison between RDCL and hard-switching converters

It has been explained above how resonant DC link inverters may be used to reduce switching losses; Table 1 allows a quantitative comparison to be made between RDCL inverters and hard-switching inverters. The results are taken from work carried out by Chen *et al* (**5**), Divan *et al*(**6**) and Divan(**7**).

For Resonant DC Link Inverters the table also includes energy loss in the additional clamping device. It can be seen that in each case the overall device losses of the Resonant DC Link inverter are less than the hard-switched inverter despite the fact that the switching frequency of the RDCL is 5 to 6 times higher. It is important to remember however, when comparing switching frequencies in this manner that the

commutation of devices in RDCL converters is constrained to the zero voltage points of the link, whilst the switches in a hard-switched converter may change state at any point in time. This constraint on switching has far-reaching implications for the harmonic qualities of the output waveforms of the RDCL Inverter. The type of PWM schemes adopted for the hard-switching inverters are consequently inappropriate for this type of resonant converter. Other types of soft-switching converter are emerging (8) which allow true PWM switching, but do so at the expense of significantly increased circuit complexity.

Figure 5. Synthesis of waveforms



hard-switching inverter to produce output waveforms with equivalent, or superior Total Harmonic Distortion (THD). Even with this restriction it can be seen from

Table 1. Comparison of switching loss

		Resonant DC Link				Hard-Switching			
Test	Devices Used	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss
A	1200V 100A IGBT	60kHz	374 W	87 W	461W	10kHz	352 W	330 W	682W
B	600V 100A IGBT	60kHz	480 W	94 W	574W	10kHz	465 W	436 W	901W
C	Simu-lated BJT	25 kHz	283 W	48 W	331W	5 kHz	225 W	434 W	659W

4.2 Control strategies

Figure 5 shows how the output voltage waveforms of Resonant DC Link Inverters are constructed. (Note: For clarity the waveform is shown with just a few pulses per cycle, in practice there is likely to be hundreds). Positive and negative pulses are selected in accordance with a modulation strategy to synthesise the desired waveshape. The most popular types of modulators for this type of converter are based on Delta Modulation techniques.(9) Of particular interest in power electronics is Sigma Delta Modulation ($\Sigma\Delta M$). In principle this type of modulator attempts to maintain volt-second balance between the converter discrete output pulses, and a reference waveform (which is usually a sinusoid). This process is done in real time. Comparisons were made by Finney *et al* (2) between resonant DC link converters using $\Sigma\Delta M$ and hard-switched converters employing pulse-width modulation. They suggest that the frequency of the RDCLI needs to be 4 to 5 times greater than that of the Table 1 that an energy loss reduction would be achievable without increasing THD. A potential problem with $\Sigma\Delta M$ is the sub-harmonics which are generated due to the aperiodic nature of its operation.

An alternative to real-time modulation strategies is to use a pre-programmed strategy. Here the modulation pattern is calculated off-line and stored in a look-up table or encoded in an algorithm which can be calculated quickly in real time. During operation the converter recovers the appropriate pattern for the desired frequency and voltage conditions. A significant advantage of pre-programmed methods is that *quarter-wave symmetry* may be employed. By making all four quarters of the generated waveform symmetrical, all even harmonics are eliminated, reducing harmonic distortion. Determining the appropriate modulation pattern in a discrete system such as this involves selecting the pattern which gives the most desirable harmonic characteristics from a finite, but extremely large, set of possibilities. In mathematical terms this

corresponds to combinatorial optimisation on a large scale. For example, in a system utilising a 20kHz link frequency which is synthesising a 50Hz output waveform, 400 pulses are incorporated in each synthesised cycle. Assuming quarter-wave symmetry, this means that the modulation pattern consists of 100 pulses. The total number of possible combinations of these pulses is 2^{100}. It is not possible in practice to search all these combinations as it necessitates enormous amounts of computer time. The authors have however, succeeded in implementing an optimisation algorithm based on a process known as *Simulated Annealing*(**10,11**). This procedure involves a directed search of the combinations. Consequently not all possibilities are evaluated, and so it is not possible to say that the *absolute optimum* pattern is located, but a *good* solution is obtainable using a sensible amount of computing time.

Pre-programmed techniques are especially useful in the traction field since they allow prediction and control of individual harmonics. This is particularly pertinent where signalling interference may be a problem. Figure 6 shows the spectrum of a RDCLI output where a group of harmonics have been minimised using simulated annealing, whilst at the same time achieving a certain desired value of fundamental voltage. Note the harmonics marked 'T' are triplens. These do not cause current to flow in a three phase system without a neutral line, and therefore no attempt is made to minimise them. This type of control is not possible using techniques such as ΣΔM.

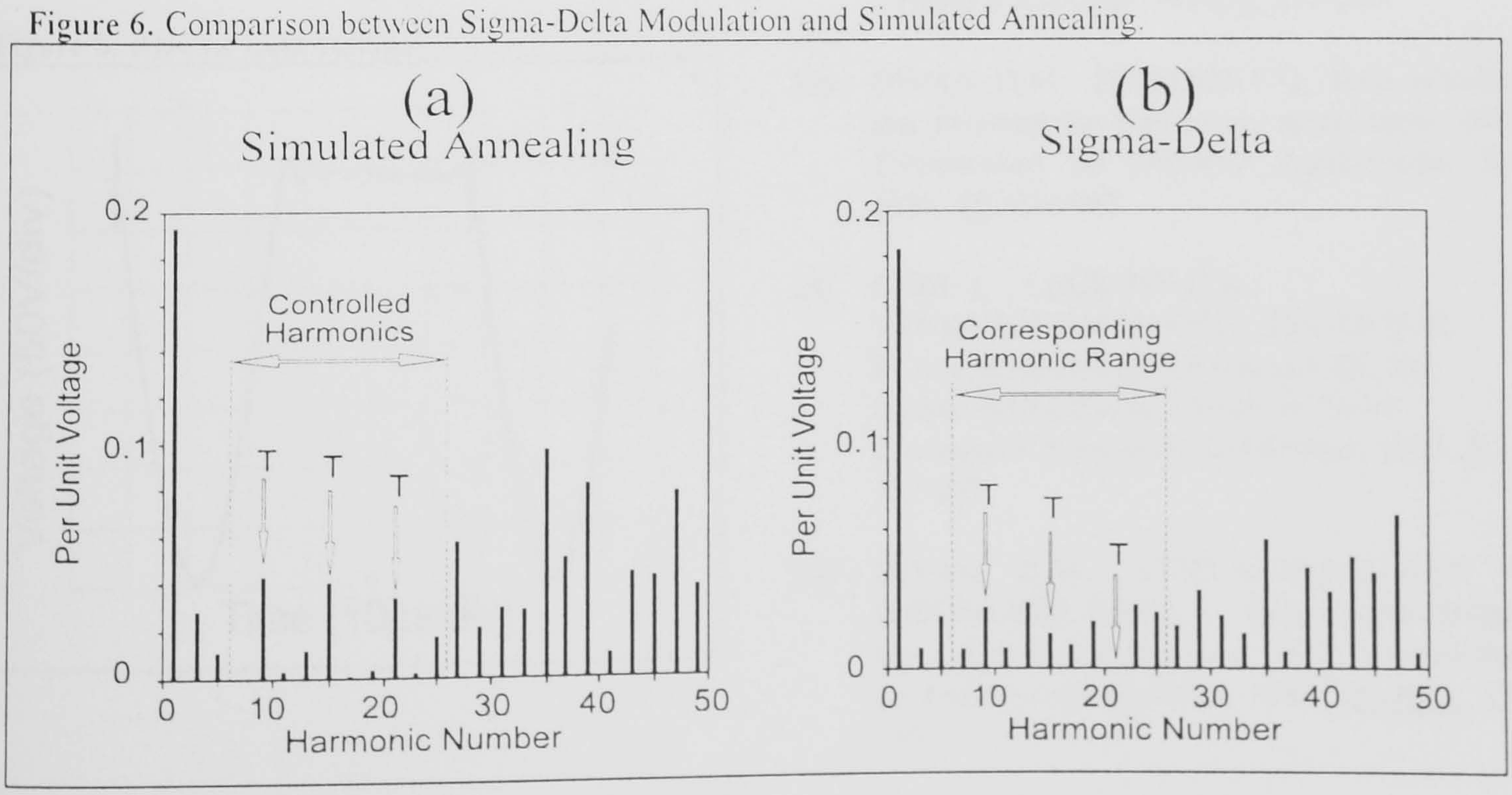
4.3 Design of the link components

To achieve a successful Resonant DC Link Inverter design, it is important that a considerable amount of thought is given to the selection of the two resonant components, L_r and C_r. Initially the link frequency should be selected, which allows the relationship between L_r and C_r to be determined. It can be shown that the link frequency, f_L, is given approximately by equation (1), below, where k is the clamping coefficient.

$$f_L = \frac{1}{2\sqrt{L_r C_r}\left[\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right]} \qquad (1)$$

Selection of an appropriate link frequency is a non-trivial task, since it requires balancing the minimum acceptable harmonic quality, which becomes poorer at low frequencies, against the overall converter losses, which rise with increasing frequency. With this ratio established, there is considerable freedom in the actual values that can be assigned to L_r and C_r. There are several factors to consider. More stable link operation is possible if C_r is made as large as possible, which reduces the size of L_r (to keep the link frequency constant). Consequently abrupt changes in link current caused by switch modulation only induce small voltages in L_r. This is an especially important factor for pre-programmed strategies which are calculated assuming a regular link waveform. Also a large value of L_r requires a large, expensive inductor if losses are to be kept low. However, though this situation is

Figure 6. Comparison between Sigma-Delta Modulation and Simulated Annealing.



desirable in terms of link stability, when C_r is large the circulating resonant currents become larger, increasing losses in the clamping device. A good design will balance link stability against clamp switch losses.

5. PRACTICAL RESULTS

Figure 7 shows the results obtained from a 3kVA test-rig operating with the same modulation pattern which was used to derive the theoretical results shown in Figure 6(a). The theoretical values are shown as crosses in Figure 7 to allow comparison. For clarity the triplens have been suppressed.

Figure 7. Practical simulated annealing measurements

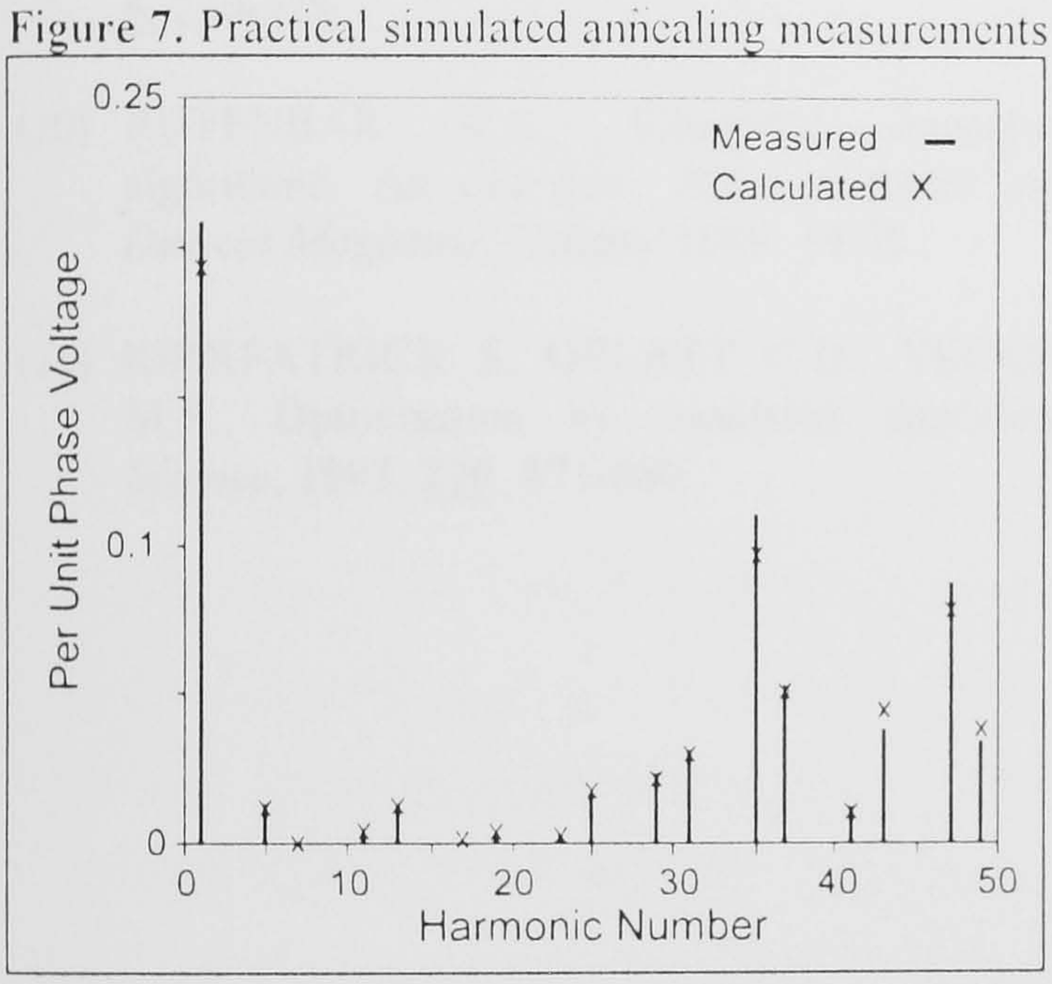
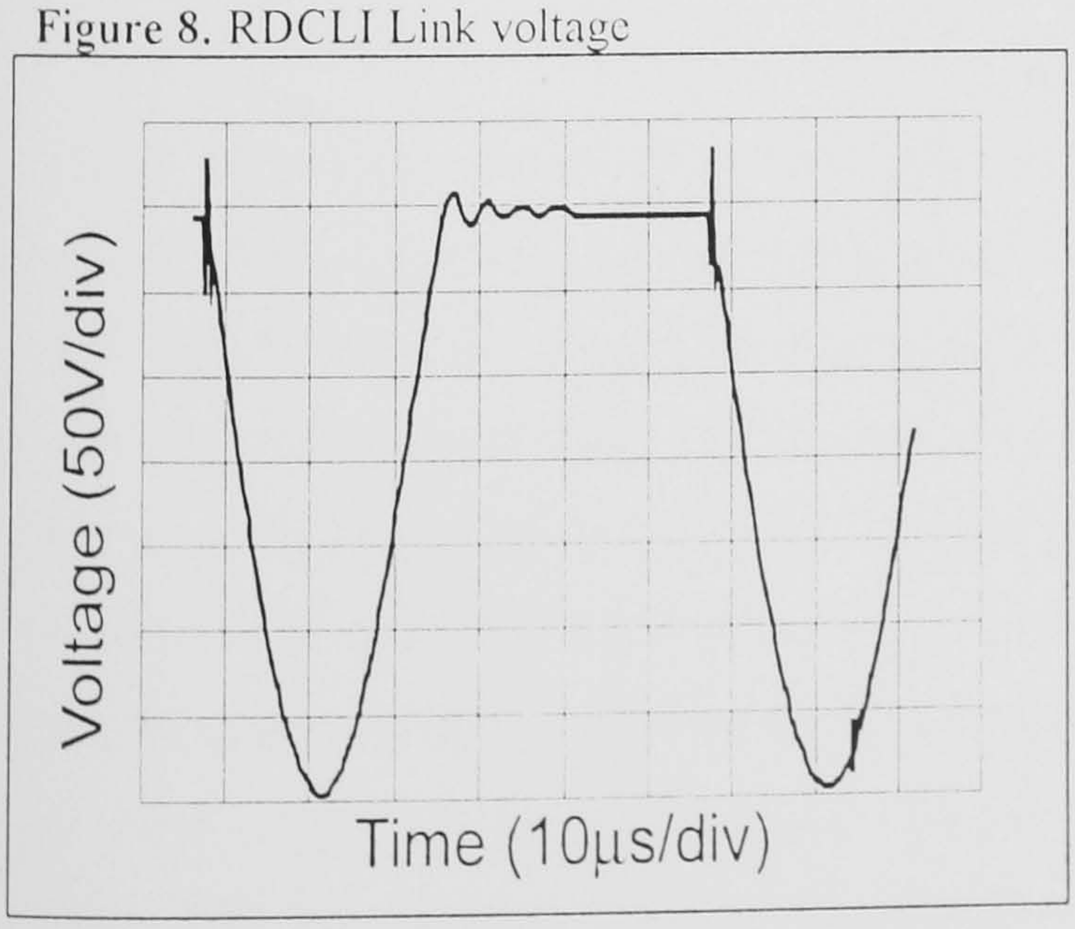


Figure 8 demonstrates the form of the link voltage in an actively clamped resonant DC link inverter. This waveform was also measured on the 3kVA test-rig.

Figure 8. RDCLI Link voltage



6. CONCLUSIONS

Soft-switching inverters are a significant development in converter technology, offering important benefits such as increased power density, improved harmonic content of output spectra, removal of snubbers, and reduced EMI. As switching devices improve it is likely that topologies such as the passively clamped RDCLI will become feasible, further extending the benefits obtained from such circuits. However care must be taken when comparing hard-switching and resonant DC link converters as the constraint that RDCLIs must switch at zero voltage points detracts to some extent, from the benefit of increased switching frequency. Nevertheless, the overall reduction in switching loss makes the RDCL topology a viable one, and offers traction equipment manufacturers the means of reducing the values of crucial characteristics such as size, weight and harmonic distortion, to levels previously unattainable using hard-switching technology.

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Soft-Switching Single-Phase to Three-Phase Converters with Near Unity Power Factor

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ABSTRACT A converter system is proposed which incorporates soft-switching both on the output stage, and on the single-phase input stage which is capable of operating in 4 quadrants and with near-unity power factor. The circuit discussed as an example is based on the Resonant DC Link Inverter topology and consequently employs Discrete Pulse Modulation. This has far-reaching consequences for the modulation strategy. Despite this, it is shown that control over individual harmonics is possible, allowing the designer to determine the characteristics of the input stage. The converter topology is compared against conventional diode-bridge input types and found to have improved figures for Total Harmonic Distortion, Peak Input Current, and Psophometric current which is an important indicator in the rail traction field. It is also seen that the weight and size of the converter may be reduced due to the lower filtering and heatsinking requirements. The results obtained by simulation are compared with practical results derived from a low-power test-rig.

1. Introduction

Recently there has been heightened interest in improving the current waveforms drawn by the input stages of converters. Among the various reasons for this are the stricter regulations being imposed by supply authorities for operating equipment at poor power factor, and limiting harmonic pollution of the supply. In the rail traction environment there are often additional restrictions on the generation of specific harmonics, or bands of harmonics, to avoid interference with signalling systems. Furthermore there are usually limits on levels of psophometric current; this is a summation of the harmonics in the supply current, weighted in a manner which reflects the perceived level of interference in communication circuits.

Many circuit topologies have been examined for use in current-shaping rectifiers [1,2]. Some circuits have employed resonant techniques to achieve soft-switching, which virtually eliminates switching losses. [3]. The topologies usually associated with 'hard-switching' and described in [1] and [2] may however be incorporated into soft-switching circuits such as the Resonant DC Link Inverter allowing them to benefit from soft-switching without the addition of any components. An example of such an application is given below using the 4-switch H-bridge topology. The disadvantage of doing this is that the converter is constrained to use Discrete Pulse Modulation. In other words the switching of the devices in the converter is restricted to specific moments in time. This has far-reaching implications for the modulation strategy and it is this issue which is the main subject of this paper.

Typically Resonant DC Link circuits are suitable for the 1-200 kW power range. Thus in the traction field they are ideally suited for use in auxiliary converters. This is an example of the kind of application where pre-programmed modulation strategies are advantageous since they allow control of individual harmonics, and can thus be used to control properties such as psophometric current, or harmonics which would otherwise interfere with signalling systems. It is shown below how pre-programming may be implemented in a Discrete Pulse Modulation input-stage.

2. Proposed Converter Topology and Modulation Strategy

The proposed converter is based on the Actively Clamped Resonant DC Link Inverter (ACRDCLI) which is shown in Figure 1(a). [4] The inductor, L_r, and capacitor, C_r, form a resonant circuit. Figure 1(b) shows the waveform of the voltage on C_r. This voltage resonates upwards until it reaches the same voltage as that on the upper plate of the clamping capacitor, C_c. At this point the clamping diode, D_c, forward biases allowing current to flow onto C_c. During this period the voltage on C_r is clamped at a value kV_{DC}, where k is the clamping coefficient which typically has a value 1.2-1.8. The current flowing onto C_c eventually reverses direction and is allowed to flow back via the switch T_r. This results in a negative, and increasing value of current in L_r. When T_r is turned off, the current in L_r initiates the next resonant cycle, causing the voltage on C_r to resonate down towards zero. The instant at which T_r is turned off is selected such that the voltage on C_r *just* reaches zero at its lowest point. At these zero voltage points the devices may be switched with very low switching loss. Consequently within the constraint that the devices are commutated at the zero voltage points, they may be switched as frequently as desired without significantly increasing the overall device losses. Table 1 [5] allows a comparison to be made between hard and soft switching converters. It can be seen that in each case the overall device losses of the Resonant DC Link Inverter are less than the hard-switched inverter, despite the fact that the switching frequency of the RDCLI is some 5 to 6 times higher. The current rating of the main devices in an RDCLI is approximately the same as for an equivalently rated hard switching inverter. However due to the oscillating resonant link, the devices experience a significantly higher voltage stress.

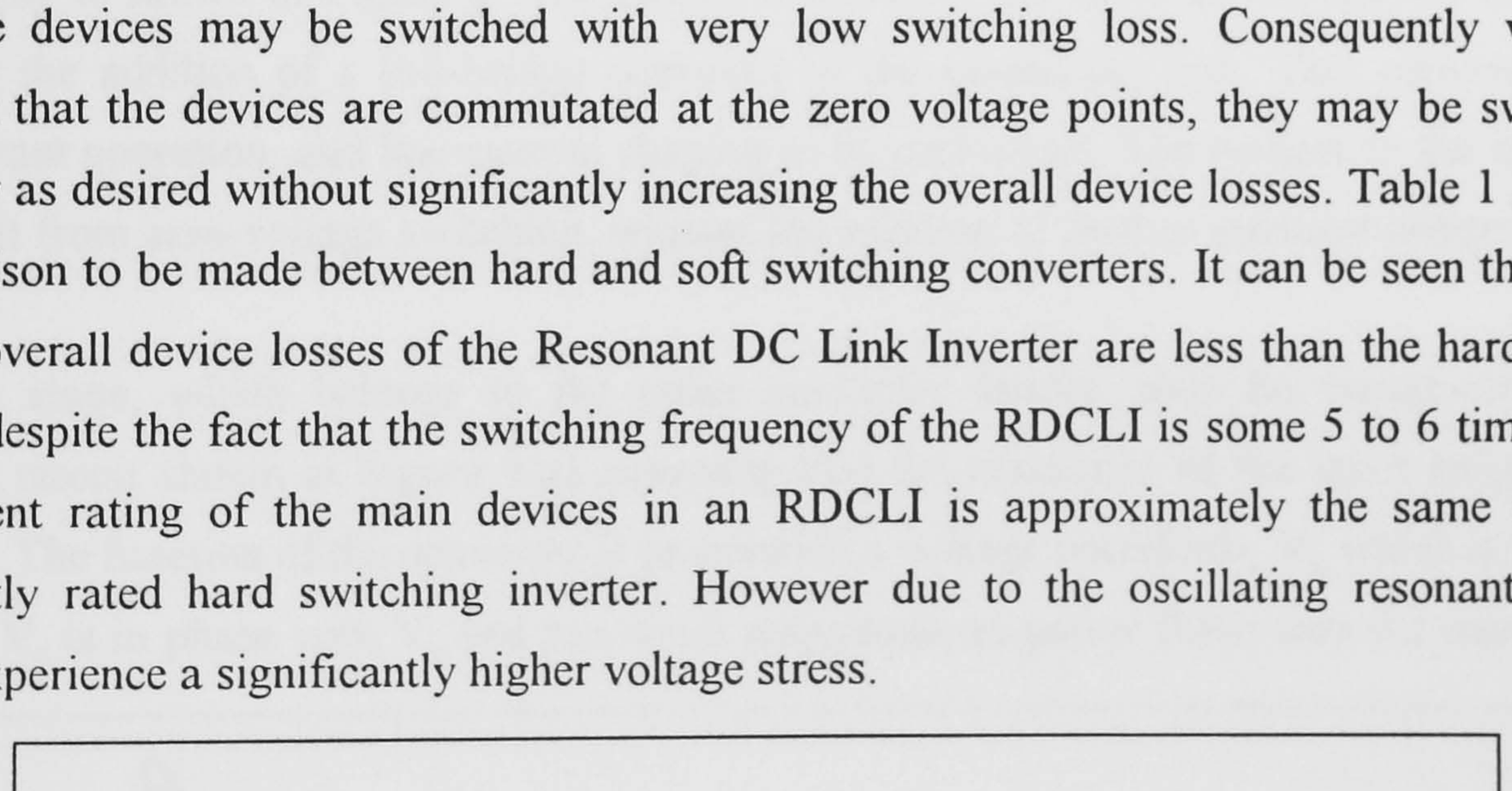

Figure 1. Actively Clamped Resonant DC Link Inverter

	Resonant DC Link				Hard-Switching				
Devices Used	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss	Switching Frequency	Conduc-tion Loss	Switching Loss	Total Device Loss	Notes
1200V 100A IGBT	60kHz	374 W	87 W	461W	10kHz	352 W	330 W	682W	I_o=55A V_{DC}=600V
600V 100A IGBT	60kHz	480 W	94 W	574W	10kHz	465 W	436 W	901W	I_o=100A V_{DC}=300V P_o=10kW
Simu-lated BJT	25 kHz	283 W	48 W	331W	5 kHz	225 W	434 W	659W	I_o=100A V_{DC}=600V

Table 1 Comparison of Soft and Hard-switching Inverters

A disadvantage of this, and many other types of converter, is the need to provide a DC supply. This often involves the use of a simple rectifier with capacitor smoothing. Unfortunately though being simple, this type of front end is undesirable because of its poor power factor. The problem is exacerbated when the circuit is fed from a single-phase supply. Various methods may be used to improve this situation by shaping the input current. The circuit proposed for use with a single-phase supply is shown in Figure 2. The circuit is basically the same as that shown in Figure 1 except for the addition of a full-bridge converter to the resonating link. This converter allows four-quadrant operation, and line-current shaping to be performed. The devices in the input stage also benefit from zero-voltage switching, without the addition of further resonant components.

The input stage, which belongs to the pulse converter family, may be represented by the equivalent circuit shown in Figure 3(a) assuming that the resistance of the input inductor L_s is negligible. The function of the converter is to generate a voltage waveform, V_c which is applied to L_s. When V_c is in phase with V_s and has equal magnitude no power flows into the converter. By

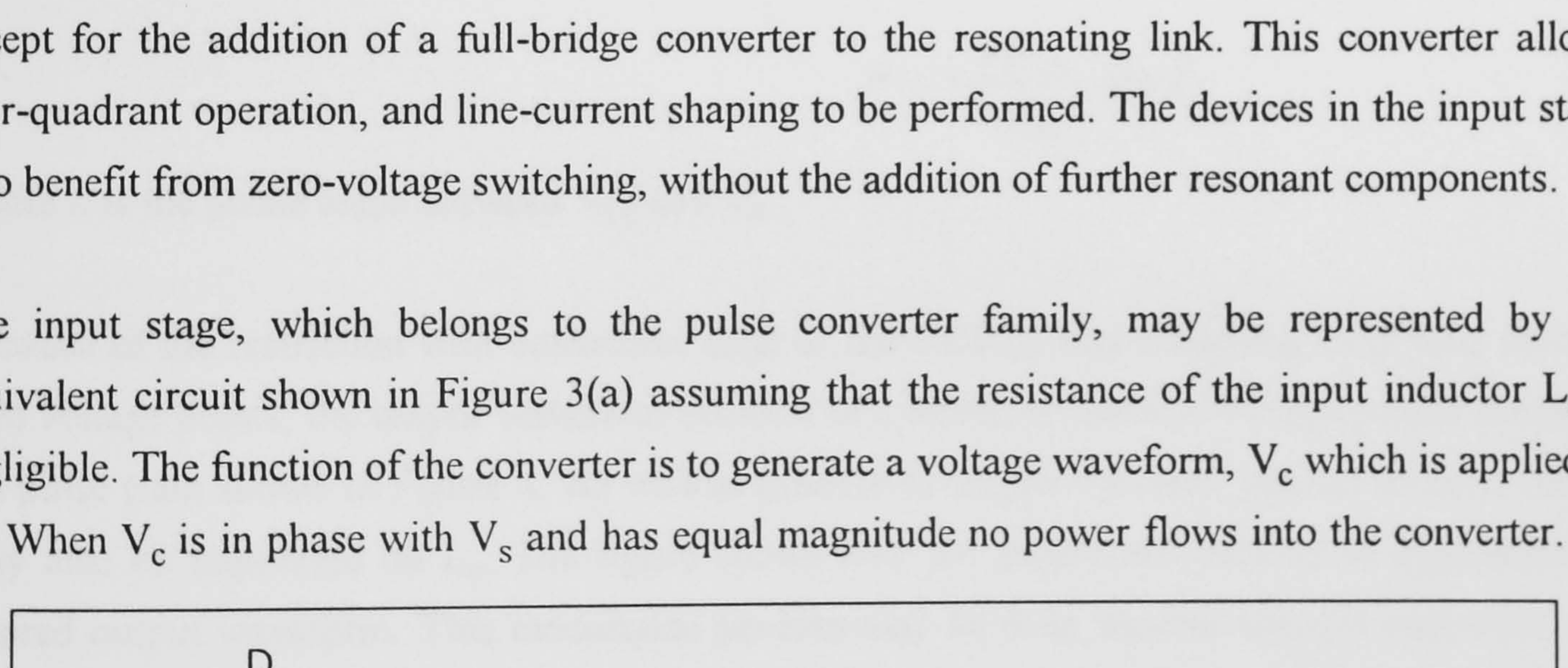

Figure 2. ACRDCLI with Pulse Converter Input Stage

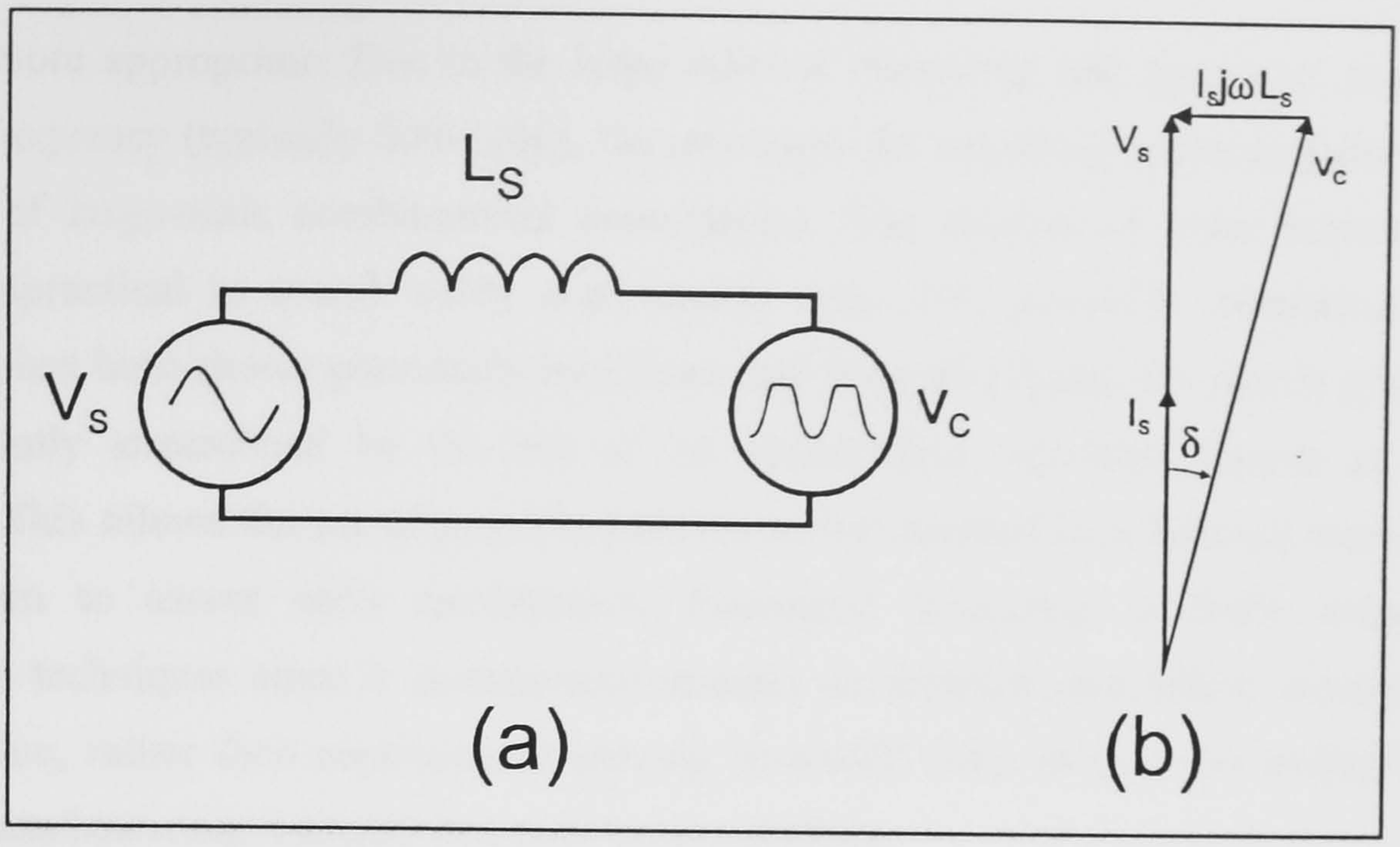

Figure 3. Pulse Converter Equivalent Circuit and Phasor Diagram

introducing a small phase shift between V_c and V_s, it is possible to cause power to flow into the converter, or to flow out (re-generation). By making appropriate changes in the magnitude of V_c the input stage can be made to operate at unity power factor. Figure 3(b) shows the phasor diagram for the pulse converter operating at unity power factor. 'V_{c1}' represents the fundamental component of the converter voltage waveform, V_c. The equation for power flow through the input inductor is:

$$P = -\frac{V_s V_{C1}}{\omega L_s} . \sin \delta \qquad (1)$$

where δ is the phase angle between V_{c1} and V_s.

Because of the restriction with converters such as the RDCLI that switching must take place at zero voltage points, the output waveform consists of a series of identical voltage pulses similar to the pulse train shown in Figure 4. As well as positive or negative pulses, periods of zero voltage may also be impressed on L_s. The figure shows how the pulses are selected to synthesise the desired output waveform. This modulation process may be done 'on-line' using a controller such as the Sigma-Delta Modulator [6]. However, if it is necessary to control specific harmonics, or a complex function of the harmonics within the output waveform, then a pre-calculated modulation

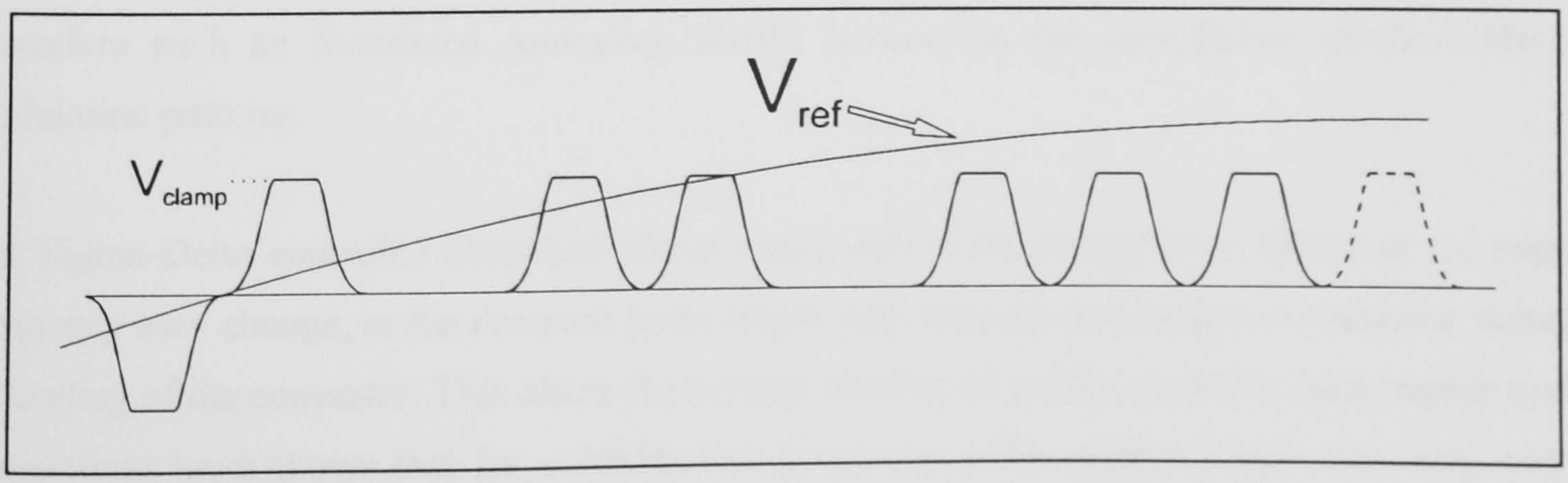

Figure 4. Synthesis of Waveforms

process is more appropriate. Due to the large ratio of resonating link frequency to synthesised waveform frequency (typically 300-1200), the procedure for obtaining optimum pulse patterns is a problem of large-scale combinatorial optimisation. The number of pulse patterns possible makes it impractical to search every combination even with powerful computing resources. However, it has been shown previously by Ellams and Mansell [7] that the search procedure can be significantly streamlined by the use of an optimisation algorithm known as Simulated Annealing. This allows the set of possible patterns to be searched in a directed manner using a cost function to assess each combination. Simulated Annealing is fairly unique among optimisation techniques since it occasionally accepts an iterative step which worsens the cost function value, rather than continuously moving 'downhill'. This reduces the probability of the search process becoming 'trapped' in a poor local minimum.

3. Pulse Converter Control

One of the key requirements for a pulse converter such as this is the ability to track the mains supply voltage waveform. In a 'conventional' PWM system with unconstrained switching angles, this is not too much of a problem. However, in a discrete pulse system like the Resonant DC Link converter the overall period of the generated waveforms is also constrained to discrete values. The length of the pulses on the resonant link has an arbitrary relationship to the supply frequency . As a consequence, it is necessary to continually correct for phase error between the synthesised waveform and the supply waveform. In the steady state, this control may be implemented by identifying from a table of possibilities, one pulse pattern which has a period greater then the mains supply, and one pattern which has a period shorter than the supply. The function of the control loop is to alternate between these two patterns in a manner which minimises the phase error. Alternation may only take place at the end of a synthesised cycle and involves quantised output values. In other words it is behaving like a Sigma-Delta Modulator with the supply frequency as the demand input. [8]

At the same time as deciding the overall period of the generated pattern, the controller must determine its fundamental magnitude and harmonic properties. These are intrinsic qualities of the pattern. Consequently it is necessary to generate a table of patterns for each desired value of fundamental. To give the appropriate harmonic properties, a cost function and optimisation procedure such as Simulated Annealing should be used in the formulation of the tables of modulation patterns.

The Sigma-Delta controller described above works well in the steady state. However the supply frequency may change, or the resonant pulse length may vary due to changes in clamping voltage, or loading of the converter. This alters the average number of pulses needed in each supply cycle. Simulations have shown that for a 20kHz link frequency, pulse pattern length may vary over a

range of 10-20 as the load on the converter is increased. Changes such as this can be detected by the controller by examining the phase difference between the generated pattern and the supply waveform. This is most easily done at the zero-crossing points of the supply. To prevent the Sigma-Delta controller from saturating, the two patterns used must be updated with new ones which are either longer or shorter, thus allowing correct tracking of the supply to continue. This system of operation has the characteristics of a Digital Phase Lock Loop (DPLL) [9]. To maintain stability of this loop a delay may need to be introduced. The delay causes the system to wait a number of cycles before correcting a phase error, and thus behaves as a low-pass filter. Figure 5 shows a block diagram of the phase-lock system. It can be seen from the diagram that it exists as two loops; the inner Sigma-Delta loop, and the outer bandwidth-limited loop to account for transient conditions. Although shown as separate blocks, the phase-lock system, and pattern generation may be implemented on a single microprocessor.

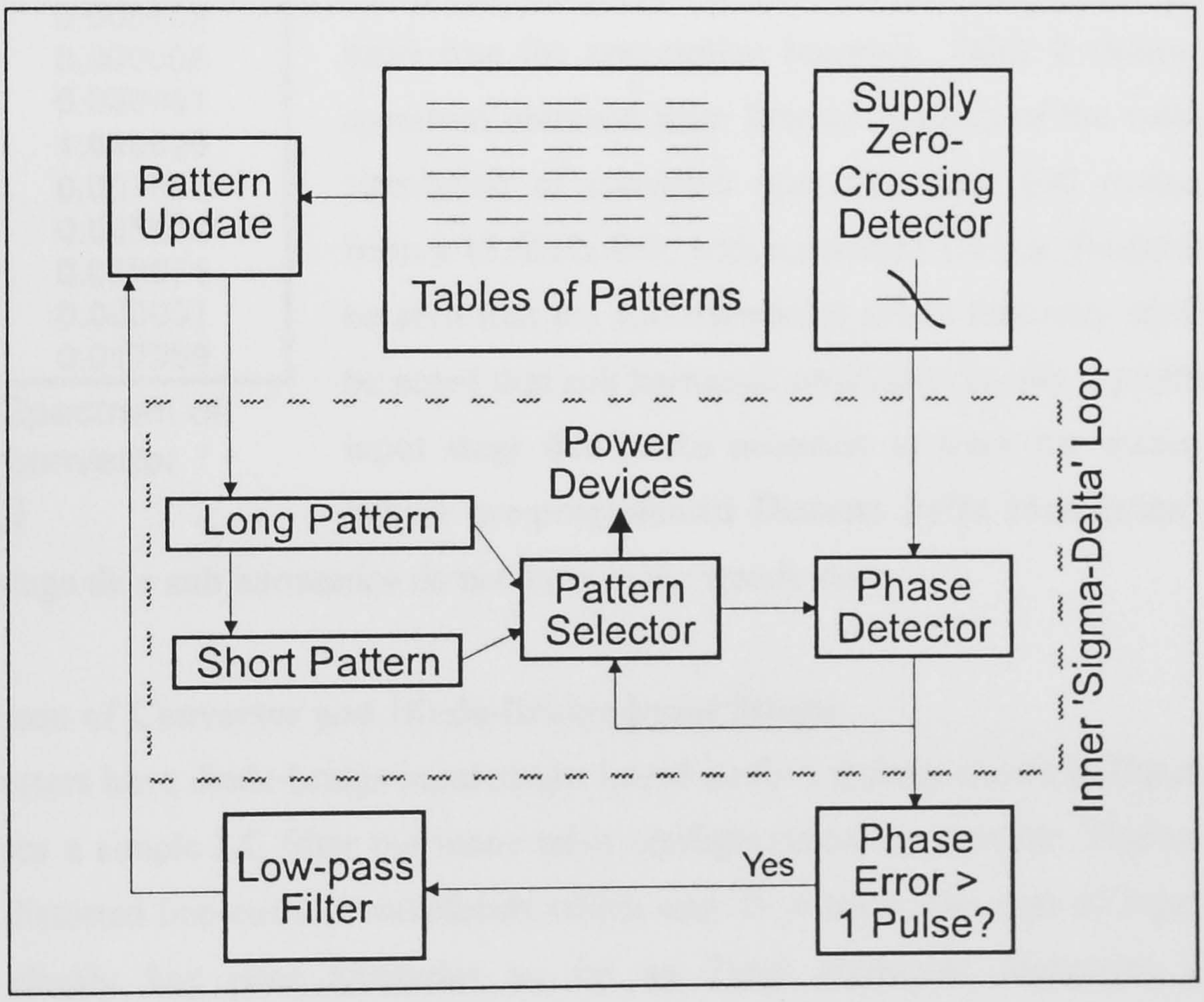

Figure 5. Block Diagram of Phase-Lock System

4. Analysis and Simulation of the Phase-Lock System

In tracking the supply voltage waveform the controller will normally select the short pattern for one cycle, followed by several cycles of the long pattern, or vice versa. The implication here is that there are modulations of the converter taking place at less than the supply frequency. In other words sub-harmonics may be generated. For this reason it is of interest to be able to model the converter to assess the size of these sub-harmonics, which may experience very low values of impedance and thus cause large sub harmonic currents to flow. Considering only the fundamental of the synthesised voltage waveforms, the converter behaves like an oscillator whose frequency is

modulated. This modulation is restricted to the end point of each synthesised cycle. This situation is well known in the communications field as Continuous Phase Frequency Shift Keying [10]. Previous work in this area has shown that it is a very difficult situation to analyse spectrally, and only a few special cases are discussed in the literature. Normally it is assumed that the selection of frequencies is random, which is not the case here. Consequently it is preferable to use simulation rather than attempt a rigorous analytical approach.

Frequency p.u.	Magnitude p.u.
0.1	0.000037
0.1111	0.000020
0.1250	0.000011
0.1428	0.000006
0.1666	0.000030
0.2	0.000013
0.25	0.000102
0.3333	0.000008
0.5	0.000001
1.0	**1.009620**
3.0	0.007880
5.0	0.005952
7.0	0.009674
9.0	0.000051
11.0	0.017959

TABLE 2 Spectrum of simulated converter voltage (v_c)

The selection of long and short patterns for synthesis is normally a non-repetitive process due to the arbitrary relationship between the period of the supply waveform and the synthesised waveforms. [8] Because the simulation is performed over a finite number of cycles however, repetition is automatically assumed. The more cycles which can be included in the simulation, the more true the assumption becomes. Table 2 shows part of the spectrum obtained from Fourier analysis of the voltage v_c for a simulation of converter operation over 100 cycles, operating from a 15.6kHz link, with a nominal 1.0 p.u. fundamental. It can be seen that the sub-harmonics are in fact very small. It should be noted that sub harmonic oscillation is only a problem with the input stage due to the necessity to track the mains frequency. Where pre-programmed Discrete Pulse Modulation is used on the output stage then sub harmonics do not exist in the steady state.

5. Comparison of Converter and Diode-Bridge Input Stages

Many converters have diode-bridge input stages based on the topology shown in Figure 6(a). This circuit utilises a simple LC filter but many other configurations are possible. Figure 6(b) shows the typical distorted line-current waveforms which may flow using this type of input stage This waveform clearly has poor attributes as far as Total Harmonic Distortion (THD) and psophometric current (I_p) are concerned. Figure 7 allows a fuller comparison to be made. In this example, converter and diode-bridge input stages have been simulated and the respective values of THD, I_p, and peak input current have been calculated. This has been repeated using various

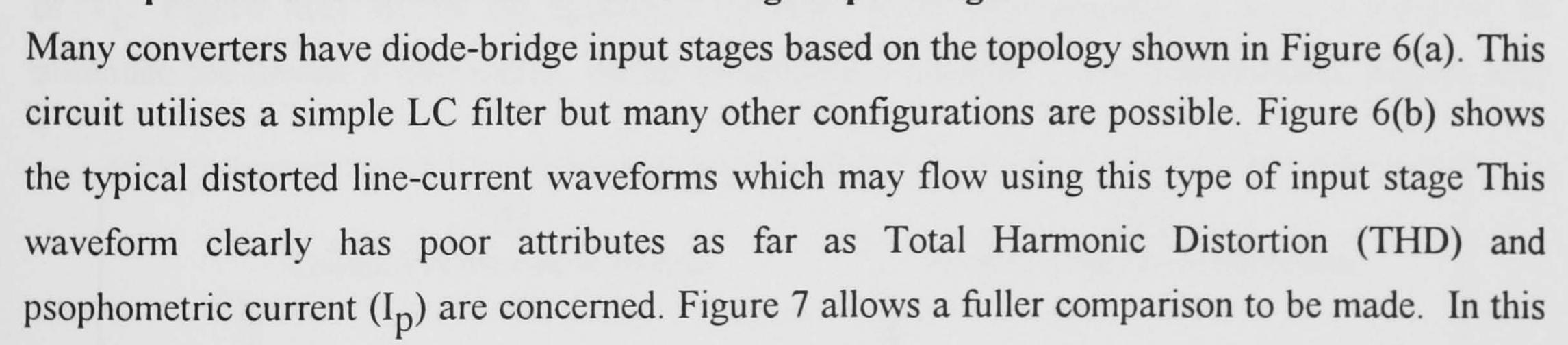

Figure 6. Diode-Bridge input stage and current waveform

values of filter inductance, whilst varying the filter capacitance to maintain a constant resonant frequency of 8Hz for the filter arrangement. In each case, a resistive load of 40kW was assumed, supplied from a 1000V AC source. In the case of the pulse converter-input circuit the 'filter' inductance is the line inductor. It can be seen from the graphs in Figures 7(a), (b) & (c) that the pulse converter-input circuit possesses significantly lower values of THD, I_p, and peak input current. Conversely it could be said that whilst maintaining the same values of THD, I_p, and peak current, the pulse converter-input type requires a smaller value of inductance. The reduced peak current has a bearing on device and heatsink rating. These factors are particularly important where weight and size are critical.

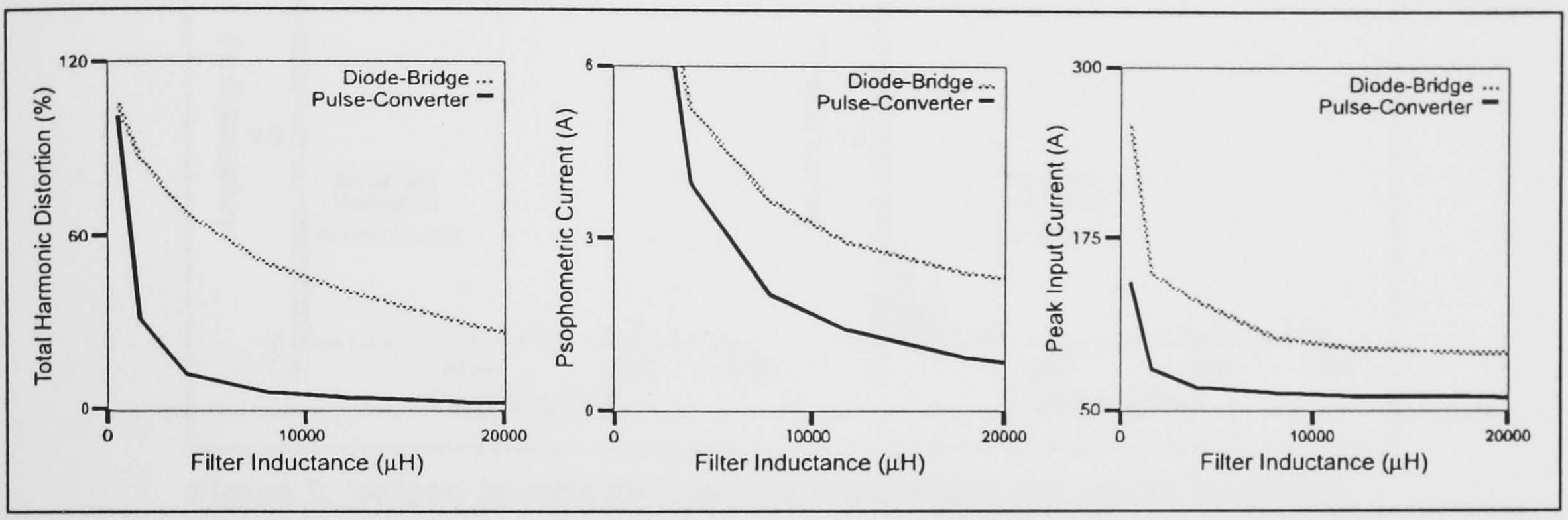

Figure 7. Graphs of THD, I_p, and peak current for the input stages (obtained by simulation)

6. Practical results

Figure 8 shows the spectrum of the voltage waveform obtained from the input-stage of a low power test-rig having the same circuit configuration as shown in Figure 2. i.e. it is the spectrum of V_c. Figure 8(a) shows the spectrum obtained when implementing a pattern designed to minimise the lowest 9 harmonics, whilst demanding a nominal 1 p.u. fundamental. Figure 8(b)

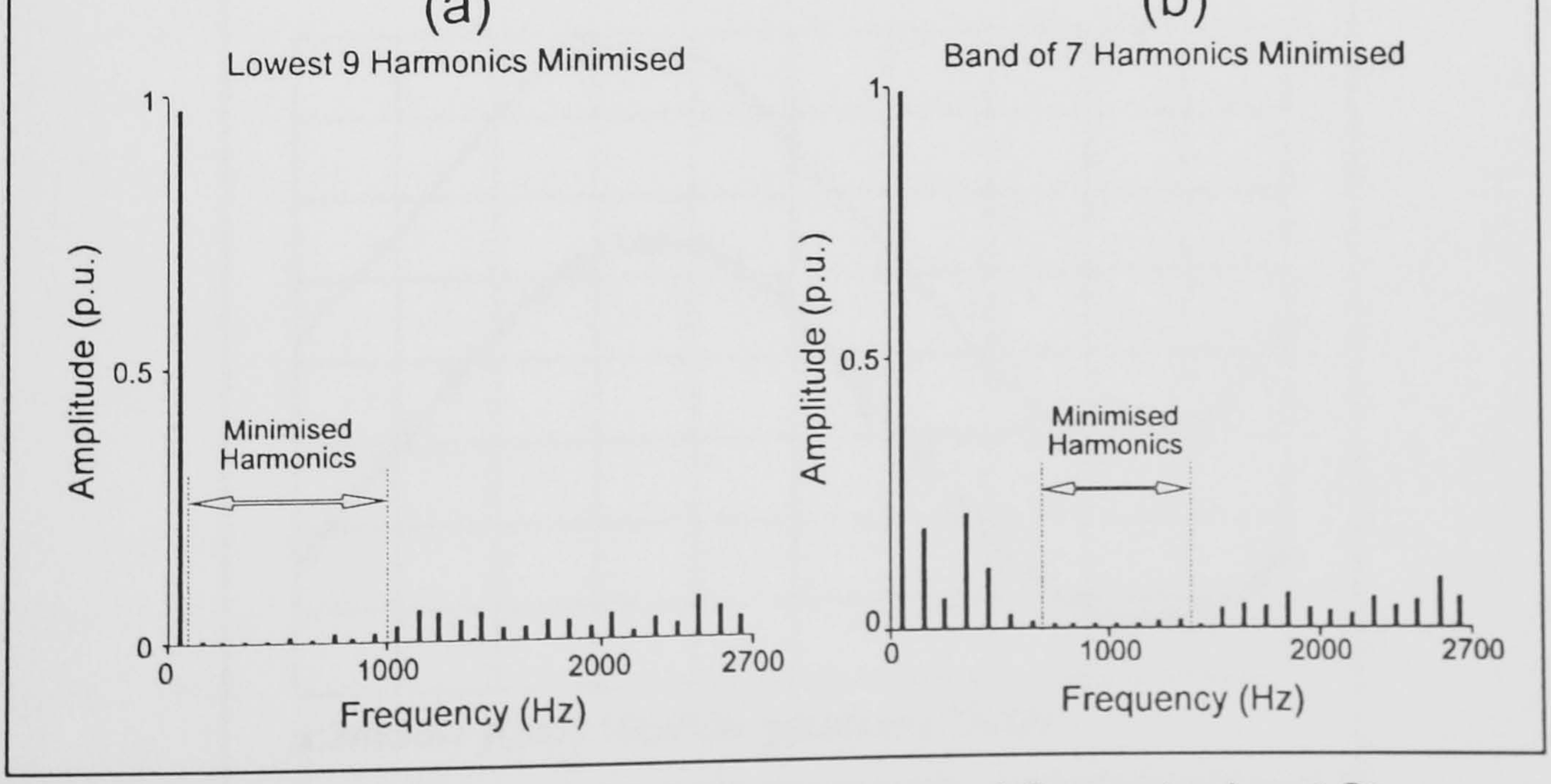

Figure 8. Practically Measured Voltage Spectra of Converter-Input Stage

demonstrates how a band of harmonics may be minimised, again the nominal fundamental is 1 p.u. In practice the increase in low frequency harmonics which this causes would probably be undesirable. However the process could be easily modified to reduce low frequency harmonics *and* minimise a remote band higher in the spectrum. Figure 9 shows the spectra derived by using computer simulation under the same conditions. It can be seen that whilst the harmonic envelopes are similar to the practical results there is some discrepancy regarding individual harmonic

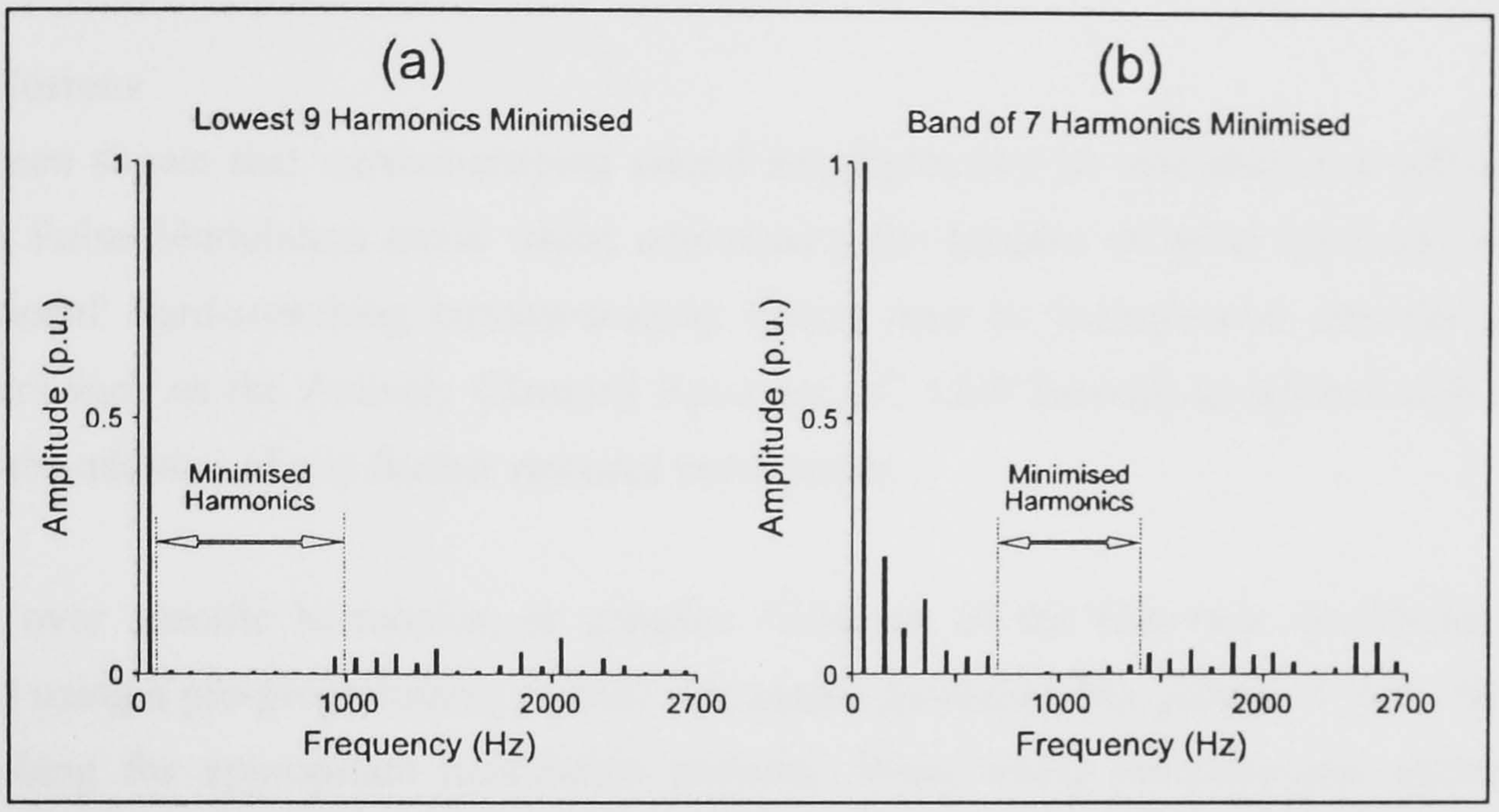

Figure 9. Voltage Spectra for Converter-Input Stage Derived by Simulation

amplitudes. This can be attributed to several factors. Firstly the test-rig was controlled using 8051 microcontrollers which have a 1μs cycle time. Thus when performing many instructions, as required by the control loops, the computation time can become comparable with the period of link resonance. As a consequence an appreciable degree of error exists in the pattern selection, giving harmonically non-ideal characteristics. This situation could be alleviated by using a faster processor such as a Digital Signal Processor. Another source of discrepancy is the Spectrum Analyser which introduces measurement errors when analysing harmonics of very low amplitude. A further factor is the assumption of pattern repetition upon which the simulation is based.

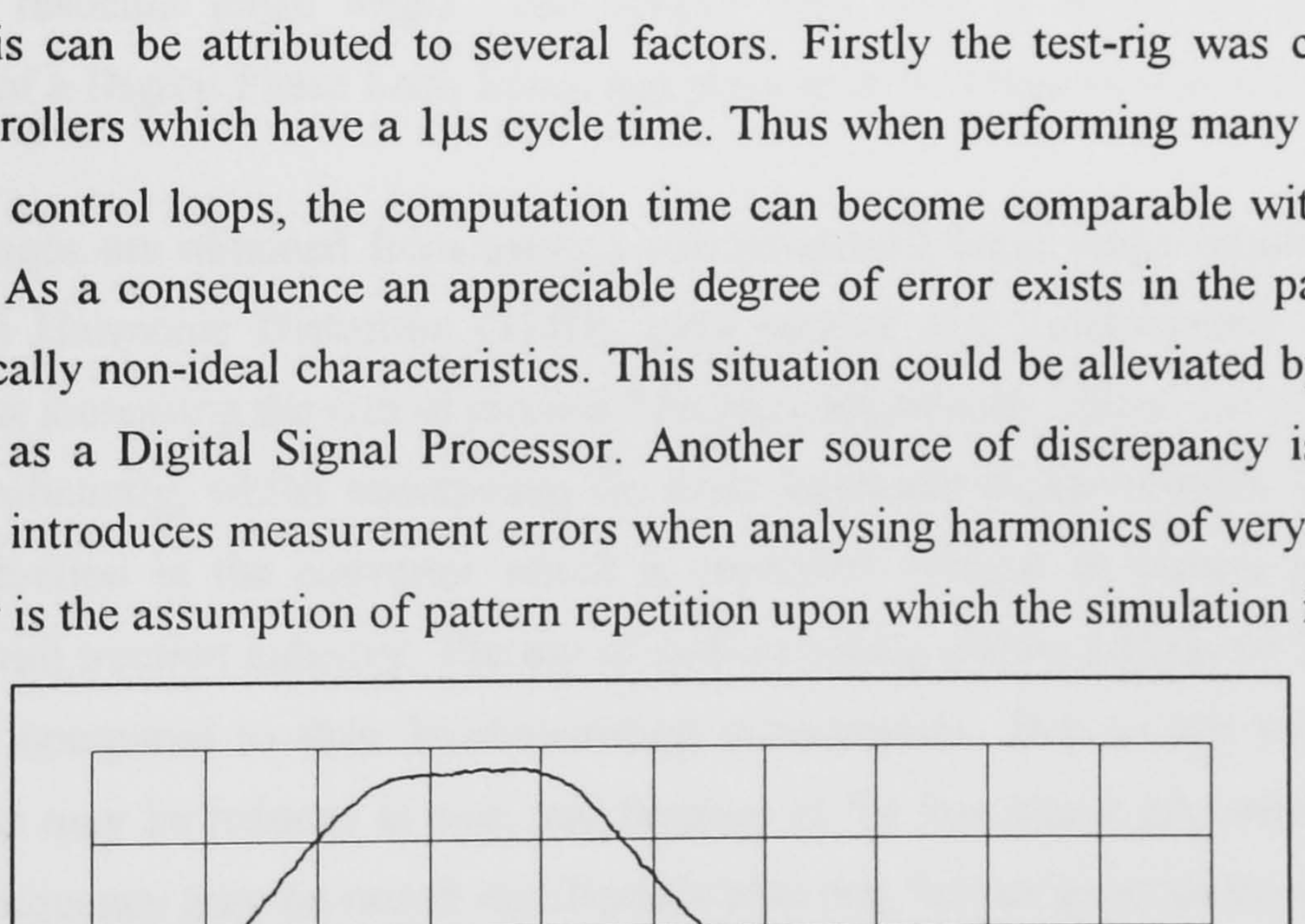

Figure 10. Oscillogram of Supply Voltage and Input Current

The lower trace in Figure 10 shows the typical form of the line current flowing into the converter. It can be seen that the current is harmonically fairly pure, and in phase with the supply voltage waveform (upper trace) creating the conditions for high power factor. The power factor was measured at 0.99 using an AC power analyser. The distorted appearance of the voltage waveform was due to external harmonic pollution of the laboratory supply. This however serves as an example of the effects of operating converters without power factor corrected front-ends.

7. Conclusions

It has been shown that current-shaping circuit topologies can be operated in a soft-switching, Discrete Pulse Modulation mode whilst maintaining the benefits of good harmonic control. A 'conventional' hard-switching current-shaping circuit may be incorporated into the design of converters such as the Actively Clamped Resonant DC Link Inverter to achieve soft-switching without the addition of any further resonant components.

Control over specific harmonics, or complex functions of the harmonic amplitudes may be achieved using a pre-programming method. Simulated Annealing has proved to be a reliable way of searching for appropriate modulation patterns. When using pre-calculated patterns, it is necessary to store a table containing various pattern lengths to account for changes in supply frequency and resonant pulse length. The control loop used to select the patterns has the characteristics of a Digital Phase Lock Loop, and steps must be taken to ensure its stability.

Several advantages are obtained from using a current-shaped input stage whether hard or soft-switched; Total Harmonic Distortion (THD), peak current and psophometric current may be reduced, without increasing the size of passive filtering components. Indeed the size of filters may be reduced significantly, whilst maintaining the same harmonic characteristics. This allows size and weight reduction in the converter which is especially critical in certain applications, for example in the rail traction industry. The use of soft-switching allows additional improvements to be made when compared to their hard-switching counterparts. Due to the reduced switching losses, heatsinks may be reduced in size, and because of the low losses per switching operation, the switching frequency may be raised significantly allowing further gains to be made in terms of THD, peak current, psophometric current and size of filters. The improvements made by increasing the switching frequency are however, tempered by the need to use discrete pulse modulation.

The example above utilised a 4-switch H-bridge topology which gives good harmonic control properties, and allows 4-quadrant operation. This is at the expense of a full complement of switching devices. Other, lower-cost topologies are possible some of which are described in the literature. These may also benefit from the harmonic control principles described in this paper.

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