



# THE UNIVERSITY *of* EDINBURGH

This thesis has been submitted in fulfilment of the requirements for a postgraduate degree (e. g. PhD, MPhil, DClinPsychol) at the University of Edinburgh. Please note the following terms and conditions of use:

- This work is protected by copyright and other intellectual property rights, which are retained by the thesis author, unless otherwise stated.
- A copy can be downloaded for personal non-commercial research or study, without prior permission or charge.
- This thesis cannot be reproduced or quoted extensively from without first obtaining permission in writing from the author.
- The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the author.
- When referring to this work, full bibliographic details including the author, title, awarding institution and date of the thesis must be given.

# **Development of pyroelectric sensor integrated with two-dimensional transistor**



**Stephen Chukwuemeka Mbisike**

A Thesis Submitted for the Degree of  
Doctor of Philosophy (PhD)

**The University of Edinburgh**

2022

# **DECLARATION**

I hereby declare that this thesis has been produced entirely by myself from research I have carried out from 2017 – 2022 at the University of Edinburgh under the supervision of Prof. Rebecca Cheung. The work in this thesis has not been submitted for another qualification or to any other University.

Stephen C. Mbisike

University of Edinburgh

June 2022

# ACKNOWLEDGMENT

My sincere gratitude to my PhD supervisor Prof. Rebecca Cheung for all her guidance and support throughout my studies. I also thank my assistant supervisor Dr. Alister Hamilton, my first teaching and demonstration (T&D) role in 2018 was at his digital systems laboratory A MSc class. I sincerely appreciate the petroleum technology development fund (PTDF) and the Nigerian government for funding my PhD.

I cannot thank enough the clean room staff of the Scottish Microelectronics Centre for training and guidance throughout my laboratory research; Dr. Camelia Dunare, Stewart Ramsay, Ewan McDonald, Dr. Graham Wood and Dr. Peter Lomax. Other notable assistance from staff at the university includes Dr. Andrey Gromov for Raman and Photoluminescence spectroscopy and Dr. Nicola Cayzer for SEM and EBSD studies. My PhD colleagues also made the journey worthwhile; Andrew Mugisha, Yulin Geng to name a few.

My sincere appreciation also goes to Dr. John Phair, CTO of Pyreos Ltd. I collaborated with Pyreos on one of their technologies from which I benefited immensely from the exposure. The wafer manager Lutz Eckart provided valuable insight and direction on the technology and his trusted technician Gavin Logan was always happy to help.

I am pleased to acknowledge the Engineering Graduate School (EGS) for hosting programs like Firbush. Firbush was not only a recreational activity but also an avenue to get to know other research students and develop professional relationships. My sincere appreciation also goes to the EGS for the support I received during the COVID-19 pandemic.

Finally, I want to thank my family and friends for their support throughout this journey and believe that I would complete the PhD satisfactorily.



THE UNIVERSITY  
of EDINBURGH

## Lay Summary of Thesis

The lay summary is a brief summary intended to facilitate knowledge transfer and enhance accessibility, therefore the language used should be non-technical and suitable for a general audience. [Guidance on the lay summary in a thesis](#). (See the Degree Regulations and Programmes of Study, General Postgraduate Degree Programme Regulations. These regulations are available via: [www.drps.ed.ac.uk](http://www.drps.ed.ac.uk).)

Name of student:	Stephen Chukwuemeka Mbisike	UUN	S1791725
University email:			
Degree sought:	Doctorate	No. of words in the main text of thesis:	26539
Title of thesis:	Development of high performance infrared sensor integrated with two-dimensional transistor		

Insert the lay summary text here - the space will expand as you type.

Progress in the complementary metal-oxide semiconductors (CMOS) integrated circuit technology and the acceptance of silicon based microelectronics have revolutionized the electronics world. Advancement in human endeavor relies on the improvement of our processes and the discovery of new materials with beneficial properties. The advent of two dimensional (2D) materials has created exciting new possibilities. Possibilities that not only include the replacement of silicon in microelectronics but also for application in other areas such as photonics. Also, the quest to move beyond silicon and its oxide has seen increased interest in potential high dielectric and/or pyroelectric materials.

The primary motivation for this work is to improve the output of a lead zirconium titanate (PZT) based pyroelectric sensor by integrating the device with a 2D WSe<sub>2</sub> field effect transistor (FET). A systematic approach has been taken to realize this goal by exploring the material properties individually.

From varied literature, two dimensional (2D) materials have shown promise in both electrical and optical properties. In this work, studies have been conducted on a 2D material WSe<sub>2</sub>, which has been deposited via exfoliation and pulse laser deposited (PLD). Though the PLD WSe<sub>2</sub> offers good control during deposition, findings show that the exfoliated WSe<sub>2</sub> has better electrical and optical properties. A mask-less lithographic method has been employed for the fabrication of the devices and tests have been carried out using a Keithley parameter analyser, Raman and Photoluminescence spectroscopy.

Analysis have also been conducted on the PZT pyroelectric device to understand its surface profile using energy back scatter diffraction (EBSD) and a factorial design of experiment. The result and understanding from the studies have enabled the integration of PZT with a WSe<sub>2</sub> FET and the result shows improvement in the overall current output. Thus, we have succeeded in amplifying the output of the PZT pyroelectric based sensor by integrating with a WSe<sub>2</sub> FET.

### Document control

K:\AAPS\ID-AcademicAdministration\02-CodesOfPractice,Guidelines&Regulations\24-MainReferencesCopies\Policies\01-Current\Assessment BOE SCC & Feedback\Forms\ThesisLaySummary

If you require this document in an alternative format please email [Academic.Services@ed.ac.uk](mailto:Academic.Services@ed.ac.uk) or telephone 0131 651 4990.

Date last revised:  
20.06.19

# ABSTRACT

Progress in the complementary metal-oxide semiconductors (CMOS) integrated circuit technology and the acceptance of silicon based microelectronics have revolutionised the electronics world. Advancement in human endeavour relies on the improvement of our processes and the discovery of new materials with beneficial properties. The advent of two dimensional (2D) materials has created exciting new possibilities. Possibilities that not only include the replacement of silicon in microelectronics but also for application in other areas such as photonics. Also, the quest to move beyond silicon and its oxide has seen increased interest in potential high dielectric and/or pyroelectric materials.

The primary motivation for this work is to improve the output of Pyreos's lead zirconium titanate (PZT) based pyroelectric sensor by integrating the device with a 2D tungsten diselenide ( $\text{WSe}_2$ ) field effect transistor (FET). A systematic approach has been taken to realise this goal by first exploring the material properties individually.

From varied literature, two dimensional (2D) materials have shown promise in both electrical and optical properties. In this work, studies have been conducted on the 2D material  $\text{WSe}_2$ , which has been deposited via exfoliation and pulse laser deposition (PLD). Though PLD  $\text{WSe}_2$  offers good control during deposition, our findings show that the exfoliated  $\text{WSe}_2$  has better electrical and optical properties. The field effect mobility calculated for the exfoliated  $\text{WSe}_2$  and PLD- $\text{WSe}_2$  FET is  $12.06 \text{ cm}^2/\text{Vs}$  and  $5.66 \times 10^{-2} \text{ cm}^2/\text{Vs}$  respectively. A maskless lithography method has been employed for the fabrication of the devices and tests were carried out using a Keithley parameter analyser, Raman and photoluminescence (PL) spectroscopy. The PL spectra showed that the

exfoliated WSe<sub>2</sub> has a bandgap of 1.6 eV while the PLD WSe<sub>2</sub> possessed no bandgap, thereby limiting its applications.

We studied the breakdown characteristics of a 20 nm anodic tantalum, a potential high dielectric gate oxide. At an electric field of 1.5 MV/cm, the leakage current extracted for the as-deposited, 200 °C and 400 °C annealed anodic tantalum are 10<sup>-5</sup>, 10<sup>-2</sup> and 1 A/cm<sup>2</sup> respectively while the breakdown field is 5.4, 5.1 and 3.3 MV/cm respectively. Upon integration of the anodic tantalum with a WSe<sub>2</sub> FET, a field effect mobility of 0.9 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> has been realised.

Analysis has also been conducted on the PZT pyroelectric device to understand its surface profile using energy backscatter diffraction (EBSD) and a factorial design of experiment. From the EBSD analysis, the sputtered PZT possesses a grain size of about 100 nm and exists in tetragonal crystals having good correlation for an orientation along the [111] direction normal to the surface. Results and understanding from the factorial design of the experiment enabled the integration of PZT with a WSe<sub>2</sub> FET. While the standalone PZT based sensor possesses a 1 nA/mm<sup>2</sup> current density output, the integrated PZT based WSe<sub>2</sub> FET has an output of 16 nA/mm<sup>2</sup>. This improvement in the overall current output is over ten orders of magnitude. Thus, we have succeeded in amplifying the output of the PZT pyroelectric based sensor.

The experimental outcomes of this thesis would help the research community in developing higher performing integrated sensors and possibly exposing other areas of interest on inexpensive and simple methods for producing materials with high dielectric constants.

## Journal Publications

**S. C. Mbisike**, S. Seo, S. Lee, J. Phair, and R. Cheung, “Parametric study of pulsed laser deposited (PLD) WSe<sub>2</sub> 2D transistors,” *Microelectron. Eng.*, vol. 230, p. 111368, Jun. 2020, doi: 10.1016/j.mee.2020.111368.

**S. C. Mbisike**, L. Eckart, J. W. Phair, P. Lomax, and R. Cheung, “Amplification of pyroelectric device with WSe<sub>2</sub> field effect transistor and ferroelectric gating,” *J. Appl. Phys.*, vol. 131, no. 14, p. 144101, Apr. 2022, doi: 10.1063/5.0086216

**S. C. Mbisike**, Andreas Tsiamis, Peter Lomax and Rebecca Cheung, “Anodic Tantalum: Fabrication, Breakdown Characteristics of Capacitor and Integration with a WSe<sub>2</sub> Field Effect Transistor”, *Solid-state electronics*, Vol.196, p.108423, 2022, DOI: 10.1016/j.sse.2022.108423

# Table of Contents

DECLARATION .....	i
ACKNOWLEDGMENT .....	ii
ABSTRACT .....	v
Journal Publications.....	vii
List of Figures.....	xii
List of Tables .....	xv
Abbreviations and Acronyms .....	xvi
Chapter 1.....	1
Introduction .....	1
1.1 Overview .....	1
1.2 Aims and Objectives.....	3
1.3 Research Review .....	4
1.4 Thesis Structure .....	5
Chapter 2.....	8
Literature Review .....	8
2.1 Background of two dimensional (2D) materials.....	8
2.1.1 Exfoliated tungsten diselenide (X-WSe <sub>2</sub> ).....	9
2.1.2 Pulsed laser deposition (PLD) WSe <sub>2</sub> .....	11
2.1.3 Timeline of 2D Materials .....	12
2.2 Dielectrics .....	15
2.2.1 Silicon dioxide (SiO <sub>2</sub> ) - The gate dielectric.....	15
2.2.1.1 Scaling and performance .....	17
2.2.1.2 Scaling challenges of SiO <sub>2</sub> .....	19
2.2.2 High-κ dielectric .....	20
2.2.2.1 Characteristics of high-κ dielectric required for CMOS application.....	21
2.2.2.2 Anodization .....	23
2.2.3 Application of novel high-κ dielectric.....	24
2.2.3.1 Ferroelectric gate field effect transistor (FeFET) .....	24
2.3 Pyroelectricity.....	26
2.3.1 Ferroelectricity.....	29
2.3.1.1 Perovskites.....	30
2.3.1.2 Lead Zirconate Titanate (PZT) .....	31
2.3.2 Applications of Polar Materials .....	32
2.4 Conclusions .....	37

Chapter 3.....	37
Materials and Methods .....	37
3.1 Preparation and deposition of exfoliated WSe <sub>2</sub> (X-WSe <sub>2</sub> ).....	37
3.1.1 Substrate preparation .....	38
3.1.2 WSe <sub>2</sub> deposition .....	38
3.2 Deposition of pulse laser deposited (PLD) WSe <sub>2</sub> .....	39
3.3 Atomic Force Microscopy (AFM).....	41
3.4 Raman and photoluminescence (PL) spectroscopy tool.....	42
3.4.1 Raman spectroscopy .....	43
3.4.2 Photoluminescence (PL) spectroscopy .....	46
3.5 Anodic tantalum development.....	47
3.6 Pyroelectric current measurement .....	50
3.7 Two-dimensional (2D) material field effect transistor (FET) Test Setup .....	54
3.8 Conclusions .....	55
Chapter 4.....	56
Fabrication and electrical characterization of pulsed laser deposited WSe <sub>2</sub> (PLD-WSe <sub>2</sub> ) and exfoliated WSe <sub>2</sub> (X-WSe <sub>2</sub> ) field effect transistor (FET) .....	56
4.1 Introduction .....	56
4.2 Experimental.....	57
4.2.1 Deposition of exfoliated WSe <sub>2</sub> (X-WSe <sub>2</sub> ) and pulse laser deposited (PLD-WSe <sub>2</sub> ) .....	57
4.2.2 Fabrication of WSe <sub>2</sub> field effect transistor (FET).....	60
4.2.3 Electrical characterization of X-WSe <sub>2</sub> and PLD-WSe <sub>2</sub> FET's .....	62
4.3 Results and Discussion .....	63
4.3.1 Optical Characteristics.....	63
4.3.1.1 Raman spectroscopy .....	64
4.3.1.2 Photoluminescence spectroscopy .....	68
4.3.2 Transfer Characteristics .....	70
4.3.2.1 Exfoliated WSe <sub>2</sub> (X-WSe <sub>2</sub> ) FET .....	70
4.3.2.2 Pulsed Laser Deposited (PLD-WSe <sub>2</sub> ) FET .....	73
4.3.2.3 Transfer Length Measurement (TLM) .....	76
.....	76
4.4 Conclusions .....	78
Chapter 5.....	78
Anodic tantalum: fabrication, breakdown characteristics of capacitor and integration with a WSe <sub>2</sub> field effect transistor.....	78
5.1 Introduction .....	78

5.2 Experimental.....	79
5.2.1 Anodic tantalum .....	79
5.2.2 Fabrication of Ta <sub>2</sub> O <sub>5</sub> capacitor .....	81
5.2.3 Fabrication of WSe <sub>2</sub> FET based on Ta <sub>2</sub> O <sub>5</sub> .....	83
5.3 Results and Discussion .....	85
5.3.1 Anodic tantalum (Ta <sub>2</sub> O <sub>5</sub> ) capacitor .....	85
5.3.1.1 Current voltage (I-V) asymmetry for the Ta <sub>2</sub> O <sub>5</sub> capacitor .....	86
5.3.1.2 Capacitor-voltage (CV) hysteresis.....	87
5.3.1.3 Capacitor-voltage (CV) electrode area test for calculating dielectric constant ( $\kappa$ ) ...	89
5.3.2 Conduction mechanism .....	91
5.3.3 WSe <sub>2</sub> FET based on anodic tantalum .....	97
5.4 Conclusions .....	100
Chapter 6.....	101
Integration of pyroelectric device with WSe <sub>2</sub> field effect transistor .....	101
6.1 Introduction .....	101
6.2 Experimental.....	102
6.2.1 Fabrication of standalone pyroelectric device (SPD) .....	102
6.2.2 Fabrication of integrated pyroelectric device (IPD) .....	104
6.2.2.1 Design of experiment (DoE) to improve WSe <sub>2</sub> adhesion on PZT.....	105
6.3 Results and Discussions.....	109
6.3.1 PZT Surface characteristics - investigation of PZT surface using a scanning electron microscope (SEM) and electron backscatter diffraction (EBSD) imaging .....	109
6.3.2 Electrical Characteristics .....	114
6.3.2.1 Standalone Pyroelectric Device (SPD).....	114
6.3.2.2 Integrated Pyroelectric Device (IPD) .....	118
6.4 Conclusions .....	124
Chapter 7.....	124
Conclusions and future work.....	124
7.1 Final Conclusion.....	124
7.2 Achieved Objectives.....	125
7.3 Future Work.....	126
8. References .....	128
Appendix A – Run sheet of WSe <sub>2</sub> FET fabrication – Chapter 4 .....	140
Appendix B – Run sheet of anodic tantalum production and capacitor fabrication – Chapter 5 .....	143
Appendix C - Full factorial computation.....	144
Appendix D – AFM Graphs (X-WSe <sub>2</sub> and PLD WSe <sub>2</sub> ).....	147

Appendix E – Fits of Raman plots (X-WSe <sub>2</sub> and PLD WSe <sub>2</sub> ) .....	149
---	-----

# List of Figures

Figure 1.1: Thesis Structure.....	5
Figure 2.1: Hexagonal structure of a TMD [14].....	9
Figure 2.2: Picture of exfoliated WSe <sub>2</sub> on a SiO <sub>2</sub> /Si substrate (SMC cleanroom, University of Edinburgh).....	10
Figure 2.3: The n-channel MOSFET.....	17
Figure 2.4: Moore's Law [45], [51].....	19
Figure 2.5: Relationship between bandgap and dielectric constant for some high- $\kappa$ materials [54]. .....	20
Figure 2.6: Low- $\kappa$ interface layer formed between high- $\kappa$ gate and silicon substrate. ....	22
Figure 2.7: Schematic of a FeFET: (a) on state (b) off state. ....	25
Figure 2.8: Schematic of the MFIS. ....	26
Figure 2.9: The pyroelectric effect [71]. Dipole of a pyroelectric material (top), showing charge distribution on the material surface. Electrodes placed on opposite surfaces of the material forms a circuit with an ammeter (middle) showing no flow of current. Current begins to flow as a result of a change in temperature of the pyroelectric material (bottom). ....	27
Figure 2.10: (a) Polarisation vs electric field ( $P$ - $E$ ) of a polar dielectric (b) Hysteresis loop of a ferroelectric material.....	29
Figure 2.11: The perovskite structure. The blue spheres represent the monovalent or divalent cation at the (A sites), the red spheres are the tetra- or pentavalent cation (B sites) and the black sphere is the oxygen ion. ....	31
Figure 2.12: Schematic of PZT unit cell [78]. ....	32
Figure 3.1: Schematic of exfoliation and transfer of 2D WSe <sub>2</sub> onto a SiO <sub>2</sub> /Si substrate.....	39
Figure 3.2: Schematic illustrating the working principle of PLD [20]. Performed at the clean room of the Gwangju Institute of Science and Technology, Korea.....	40
Figure 3.3: Schematic illustration of the working principle of an AFM [118]. The laser beam is deflected off the back of the cantilever and onto a photodiode detector. The bending of the cantilever displaces the laser spot on the photodiode.....	42
Figure 3.4: Conventional Raman / PL Microscope [119]. ....	43
Figure 3.5: Energy level diagram showing the states involved in Raman spectra [121] ....	44
Figure 3.6: Raman Spectrum of X-WSe <sub>2</sub> . ....	45
Figure 3.7: Photoluminescence Spectrum of X-WSe <sub>2</sub> .....	46
Figure 3.8: Diagram of tantalum anodization System [130]. ....	48
Figure 3.9: Anodization current vs time graph.....	49
Figure 3.10: Anodic tantalum prepared with an applied potential of 5 V, 10 V and 20 V.....	50
Figure 3.11: Typical pyroelectric IR sensor. ....	51
Figure 3.12: Setup used for measuring pyroelectric current showing probe connection to the device [133].....	52

Figure 4.1: X-WSe <sub>2</sub> flake of various thicknesses and dimensions on SiO <sub>2</sub> substrate. ....	57
Figure 4.2: PLD WSe <sub>2</sub> deposited across a 1.5 by 1.5 cm chip. ....	59
Figure 4.3: Fabrication of X-WSe <sub>2</sub> FET: (a) Schematic outlining the fabrication process (b) Lithographic pattern prior to metal deposition. ....	61
Figure 4.4: (a) Schematic outlining the fabrication process of PLD-WSe <sub>2</sub> FET (b) Patterned PLD-WSe <sub>2</sub> channel using vapour XeF <sub>2</sub> . ....	61
Figure 4.5: (a) Schematic of the fabricated WSe <sub>2</sub> FET showing geometrical dimensions; Actual device fabricated on SiO <sub>2</sub> / Si substrate: (b) X-WSe <sub>2</sub> FET (c) PLD-WSe <sub>2</sub> FET. ....	62
Figure 4.6: Raman spectroscopy of singular plots of exfoliated WSe <sub>2</sub> flakes A, B, C and D. ....	64
Figure 4.7: Raman spectroscopy of singular plots of PLD sample 1, 2 and 3. ....	65
Figure 4.8: Raman Spectroscopy of combined (a) X-WSe <sub>2</sub> (b) PLD-WSe <sub>2</sub> . ....	65
Figure 4.9: PL Spectroscopy of (a) X-WSe <sub>2</sub> and (b) PLD-WSe <sub>2</sub> . ....	68
Figure 4.10: Transfer Characteristics of X-WSe <sub>2</sub> FET with a channel area of 5 by 2 $\mu\text{m}$ . (a) Pristine (b) XeF <sub>2</sub> treated. ....	70
Figure 4.11: Transfer characteristics for PLD WSe <sub>2</sub> transistor; (a) for different lengths (17.3, 83.4 and 323.4 $\mu\text{m}$ ) and fixed width (14 $\mu\text{m}$ ); (b) for different widths (14 and 850 $\mu\text{m}$ ) and fixed length (1000 $\mu\text{m}$ ). ....	73
Figure 4.12: TLM electrode spacing. ....	76
Figure 4.13: Resistance values of the transistors plotted against their electrode spacing at various values of back-gate voltage. The y-intercept indicates a negative contact resistance. ....	76

Figure 5.1: Cross-sectional schematic of the device fabrication process (a) During anodization; the electrolyte is dispensed on the desired tantalum area and a potential applied between anode and cathode (b) After anodization, a thin layer of Ta <sub>2</sub> O <sub>5</sub> has been grown on top of the remaining bulk tantalum (c) Ta <sub>2</sub> O <sub>5</sub> capacitor (d) WSe <sub>2</sub> FET integrated with the Ta <sub>2</sub> O <sub>5</sub> gate dielectric and with tantalum as the back-gate. ....	80
Figure 5.2: Degradation of anodic tantalum annealed in nitrogen gas furnace. ....	82
Figure 5.3: WSe <sub>2</sub> flakes on anodic tantalum showing a relationship between the flake colour and their thickness. ....	84
Figure 5.4: Schematic of anodic tantalum capacitor test set-up. ....	85
Figure 5.5: I-V asymmetry observed in anodic tantalum. ....	86
Figure 5.6: Schematic of the schottky barrier in a rectifying contact [179] (a) the reverse bias raises the barrier height and limits charge flow (b) zero bias has no effect on barrier height (c) forward bias lowers the barrier height and allows charges flow easily. ....	87
Figure 5.7: Hysteresis graphs of anodic tantalum capacitors measured by interchanging test probe position on sample: (a) As-deposited (b) 200 °C annealed (c) 400 °C annealed. ....	88
Figure 5.8: Anodic tantalum capacitor consisting of various electrode area. ....	89
Figure 5.9: Breakdown characteristics of 20 nm thick and 600 square $\mu\text{m}$ Ta <sub>2</sub> O <sub>5</sub> capacitors annealed at different temperatures. The breakdown potential and leakage current varies with their annealing temperature. ....	92
Figure 5.10: Energy-band diagram showing conduction mechanism of (a) Schottky emission and (b) Poole-Frenkel emission. ....	93
Figure 5.11: Schottky plot of the as-deposited and annealed Ta <sub>2</sub> O <sub>5</sub> capacitors. ....	94
Figure 5.12: Poole-Frenkel plot for the as-deposited and annealed Ta <sub>2</sub> O <sub>5</sub> capacitors. ....	95
Figure 5.13: Schematic of WSe <sub>2</sub> FET on anodic tantalum. ....	97

Figure 5.14: Transfer Characteristics of WSe<sub>2</sub> FET based on Ta<sub>2</sub>O<sub>5</sub> dielectric. The device fabricated is shown in the in-set figure; WSe<sub>2</sub> FET with its electrodes on a Ta<sub>2</sub>O<sub>5</sub> substrate. ....98

Figure 6.1: Fabrication process of a standalone pyroelectric device.....	103
Figure 6.2: Actual device fabricated showing WSe <sub>2</sub> FET on PZT (IPD).....	104
Figure 6.3: Line plot of design factors showing that temperature and oxygen are relevant adhesion factors .....	108
Figure 6.4: Image of PZT surface profile with donut shape provided by Pyreos Ltd [199]. The colour profile depicts donut shape appearance of wafer under bright light only .....	110
Figure 6.5: SEM surface profile (left images) and 70° tilt SEM image (right). (a)(b) wafer centre, (c)(d) wafer mid-region and (e)(f) wafer edge. ....	111
Figure 6.6: Electron diffraction pattern of a single point on the PZT .....	112
Figure 6.7: Pole figures of the (001) and (111) crystal facet, mapped from a single PZT grain.....	113
Figure 6.8: Schematic of PZT sandwiched with a top and bottom metal.....	114
Figure 6.9: Pyroelectric current of the SPD against temperature .....	115
Figure 6.10: Schematic of WSe <sub>2</sub> -PZT FET on a SiO <sub>2</sub> /Si substrate with dimensions.....	118
Figure 6.11: Output characteristics of WSe <sub>2</sub> -PZT FET with gate voltage from 0 to -20 V. ....	119
Figure 6.12: Transfer characteristics of WSe <sub>2</sub> FET based on PZT with visible ferroelectric behaviour. The gate voltage has been applied from -16 to 16 V with incremental steps of 2 V. ....	120
Figure 6.13: Current density of the integrated device and the standalone device under the single influence of changes in device temperature.....	122

Figure 7.1: (a) Schematic of WSe<sub>2</sub> PZT based FET with floating gate (FG). (b) Top view of proposed device .....

Figure A.1: Line plot of effects .....	145
Figure A.2: Interaction plot of the design <i>effects</i> .....	146
Figure A.3: AFM profile of exfoliated WSe <sub>2</sub> flake A, B, C and D .....	147
Figure A.4: AFM profile of PLD WSe <sub>2</sub> sample 1, 2 and 3 .....	148
Figure A.5: FWHM fit of Raman plots for the exfoliated WSe <sub>2</sub> flakes A, B, C and D .....	149
Figure A.6: FWHM fit of Raman plots for the PLD WSe <sub>2</sub> sample 1, 2 and 3 .....	150

## List of Tables

Table 2.1: Experimental and theoretical timeline of 2D materials [23], [24], [25], [26] .....	12
Table 2.2: Current and future applications of 2D materials [25], [29], [30], [31].....	13
Table 2.3: Properties of SiO <sub>2</sub> gate dielectric [48] .....	16
Table 2.4: Comparison of some deposition techniques [45] .....	22
Table 2.5: Historical application of polar materials [77], [87], [88], [89].....	33
Table 2.6: Applications of piezo-, pyro- and ferro-electric ceramics [77], [98], [99], [100] .....	35
Table 4.1: Flake A, B, C and D thicknesses .....	58
Table 4.2: Thickness of PLD WSe <sub>2</sub> Sample 1, 2, 3 .....	60
Table 4.3: Properties of the exfoliated WSe <sub>2</sub> .....	67
Table 4.4: Properties of the PLD WSe <sub>2</sub> sample 1, 2 and 3 .....	68
Table 4.5: Parameters for X-WSe <sub>2</sub> FET .....	71
Table 5.1: Anodic tantalum sample characteristics .....	81
Table 5.2: Capacitance of anodic tantalum for the as-deposited sample.....	90
Table 5.3: Experimental and theoretical slopes of the SE and PF conduction mechanism.....	96
Table 6.1: Experimental parameters for testing WSe <sub>2</sub> adhesion to PZT .....	106
Table 6.2: 2 <sup>3</sup> factorial design to determine the effects of the design factors.....	107
Table 6.3: Pyroelectric properties of samples with different dimensions .....	117
Table A.1: Data from 2 <sup>3</sup> full factorial computation.....	144

## Abbreviations and Acronyms

<b>TMD</b>	Transition Metal Dichalcogenide
<b>WSe<sub>2</sub></b>	Tungsten diselenide
<b>FET</b>	Field Effect Transistor
<b>PZT</b>	Lead Zirconium Titanate
<b>SEM</b>	Scanning Electron Microscope
<b>AFM</b>	Atomic Force Microscope
<b>EBS</b>	Electron Backscatter Diffraction
<b>SPD</b>	Standalone Pyroelectric Device
<b>IPD</b>	Integrated Pyroelectric Device
<b>PLD</b>	Pulsed Laser Deposition
<b>FWHM</b>	Full Width Half Maximum
<b>DI</b>	Deionized
<b>IR</b>	Infrared
<b>PL</b>	Photoluminescence
<b>ALD</b>	Atomic Layer Deposition
<b>CVD</b>	Chemical Vapour Deposition

# Chapter 1

## Introduction

### 1.1 Overview

A significant amount of experimental research has been carried out on two dimensional (2D) materials. Part of the research into 2D materials has been in the creation of field effect transistors (FET) as a replacement for silicon [1]. 2D materials are only a few nanometres in thickness and they include graphene, tungsten diselenide ( $\text{WSe}_2$ ), molybdenum disulphide ( $\text{MoS}_2$ ), to name a few [2]. The current interest in 2D materials began with the exfoliation of a few layers of graphene using a Scotch tape. Since then, other methods for depositing 2D materials have been explored and they include pulse laser deposition (PLD), chemical vapour deposition (CVD), and atomic layer deposition (ALD) and so on. The different deposition techniques vary in output mainly from the speed of deposition, area of material deposited, the precision for thickness control, temperature and so on [3]–[5].

Few layer graphene has a field effect mobility of 3,000 to 10,000  $\text{cm}^2/\text{V.s}$ . However, the drawback in graphene in electronic gate applications is the non-existence of a bandgap [6]. Tungsten diselenide ( $\text{WSe}_2$ ), a prominent contender for gate applications has been deposited via exfoliation, PLD and CVD.  $\text{WSe}_2$  has been used to make field effect transistors (FET), with mechanically exfoliated monolayer  $\text{WSe}_2$  FET exhibiting a mobility of  $250 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , on/off ratio of  $10^6$  and subthreshold slope of 60 mV per decade. On the other hand, monolayer CVD grown  $\text{WSe}_2$  FET demonstrates a mobility of  $90 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  and on/off ratio of  $10^5$  [7]. The PLD technique has not been widely experimented in growing  $\text{WSe}_2$ , it has been studied in this work as the PLD technique

## 1. Introduction

deposits large area 2D materials and also greatly increases the chances of integrating WSe<sub>2</sub> with other materials.

By virtue of the WSe<sub>2</sub> FET performance and the deposition techniques that allow for the formation of hetero-structures, WSe<sub>2</sub> as well as other 2D materials have found additional application in integrated devices, for instance with pyroelectric devices (heat sensitive materials) to achieve improved performance. Sassi et.al [8] integrated graphene with lithium niobate (a pyroelectric material) to improve the temperature coefficient of resistance of their infrared bolometer. One of the highlights of their work was the floating gate structure made from a high- $\kappa$  dielectric that contributed to the overall performance of their device. Furthermore, Xixi et.al [9] integrated tungsten diselenide with Copper indium thiophosphate (CuInP<sub>2</sub>S<sub>6</sub>) and demonstrated potential memory and low power logic applications. Therefore, taking advantage of the advances in 2D material to integrate with Pyreos's pyroelectric sensor is desirable. The standalone Pyreos's pyroelectric sensor produces a pyroelectric current of tens of pico-amps and an integration with a WSe<sub>2</sub> FET is expected to improve the pyroelectric device output.

## 1. Introduction

### 1.2 Aims and Objectives

The aim of the project is to integrate a WSe<sub>2</sub> transistor with Pyreos's PZT pyroelectric sensor in order to improve the pyroelectric sensor current output from a few pico amps. Through fabrication, testing and data analyses, the fundamental principles on material performance have been explored. Also, the design and fabrication challenges for an integrated device have been discussed.

The objectives of the project are:

- To demonstrate and characterise WSe<sub>2</sub> deposited via exfoliation and pulse laser deposition in order to determine its usefulness in an integrated device.
- To demonstrate and characterise PZT as a sensor in order to understand the material and effectively integrate it with other devices.
- To characterise the high- $\kappa$  dielectric developed by anodization; ultimately to determine its usefulness as a floating/top gate dielectric.
- To integrate the WSe<sub>2</sub> transistor with the PZT device in order to improve the standalone PZT sensor.

## 1. Introduction

### 1.3 Research Review

As earlier mentioned, the aim of the current research is to integrate a tungsten diselenide ( $\text{WSe}_2$ ) FET with Pyreo's pyroelectric device to realise a higher current output. Among the techniques used in depositing  $\text{WSe}_2$  is exfoliation and pulse laser deposition (PLD). Both techniques have been explored in the thesis to identify which of the two produces the best results and allows for integration with other devices. Other metrology techniques such as atomic force spectroscopy, Raman and photoluminescence spectroscopy have been employed to characterise the samples.

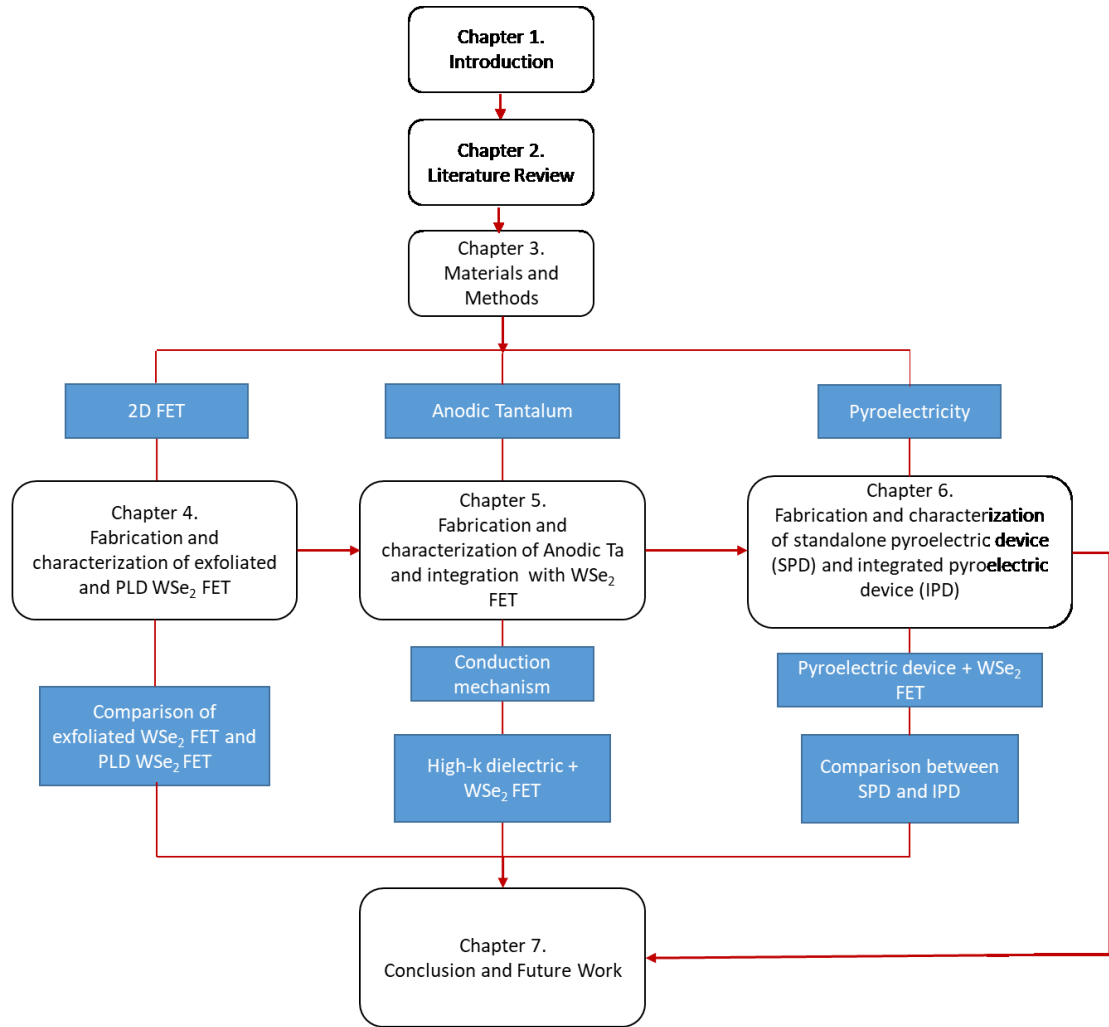
In order to realise an integrated device, a singular pyroelectric device has been developed, measured and the results analysed. The data realised from the standalone pyroelectric device and integrated pyroelectric device allows one to compare and ensure that the objectives have been realised.

One of the methods to further improve integrated devices is the creation of a floating top gate. When a device has both a back and top gate, like in a FinFET, it is encapsulated within an electric field and the device produces higher outputs. The floating gate structure is usually made from a high dielectric constant ( $\kappa$ ) material. Anodization has been employed in this work to create a high- $\kappa$  material to allow for possible / future experimentation of a floating gate structure.

## 1. Introduction

### 1.4 Thesis Structure

This thesis presents two major subjects (*2D materials* and *Pyroelectric devices*) and one minor subject *Anodization*. Figure 1.1 shows a graphical structure of the thesis including the chapters and their associated contents. Details of the thesis are presented in the subsequent chapters.



**Figure 1.1:** Thesis Structure

## 1. Introduction

**Chapter 2** describes the academic and commercial research works related to the general concepts of 2D materials, high- $\kappa$  dielectric and pyroelectric materials. A historic development of the technologies have been presented with relevant information on their application.

**Chapter 3** describes the fabrication processes for the devices. It outlined the materials required, equipment's and the process flow. The test set-up used in this work has also been described with some accompanying test results. In addition, the fundamental principles that describes how the test results are realised was discussed with further details of the test equipment's operating technique.

**Chapter 4** presents analysis on the deposition techniques and properties of 2D exfoliated and pulsed laser deposited WSe<sub>2</sub>. Raman and photoluminescence techniques was employed to characterise the materials optically. The photoluminescence results obtained have exposed possible application of the materials. Furthermore, the electrical performance of the transistors developed have highlighted other material properties.

**Chapter 5** describes the process of anodizing tantalum into a metal oxide. Here, results on the breakdown characteristics of the anodic tantalum capacitor were presented. The data extracted from the capacitor has provided useful information on the leakage current and breakdown voltage. Upon further analysis of the data, the conduction mechanism of the devices have been investigated. The results help to justify the application of anodic tantalum as a gate oxide in further experiments. Furthermore, the high- $\kappa$  anodic tantalum has been integrated with a WSe<sub>2</sub> FET. The fabrication process and FET performance have been discussed.

**Chapter 6** discusses the fabrication process of a pyroelectric device made from PZT. Optical characterization of the PZT was presented using a scanning electron microscope (SEM) and energy

## 1. Introduction

backscatter diffraction (EBSD) technique. The results of the surface topology and crystal structure of the PZT has aided in understanding the device performance. Furthermore, the standalone pyroelectric PZT sensor has been tested and discussed. The device was then integrated with a WSe<sub>2</sub> FET to improve the performance of the standalone PZT sensor. The data realised shows improvements in the device performance and also exposes other possible applications of the integrated device.

**Chapter 7** summarises the content of the thesis and presents the conclusion of the project. Also, the scientific impact and research outcomes have been outlined. The future works related to the project were presented in this chapter, showing possible improvements in the device performance with the inclusion of a floating gate structure.

# Chapter 2

## Literature Review

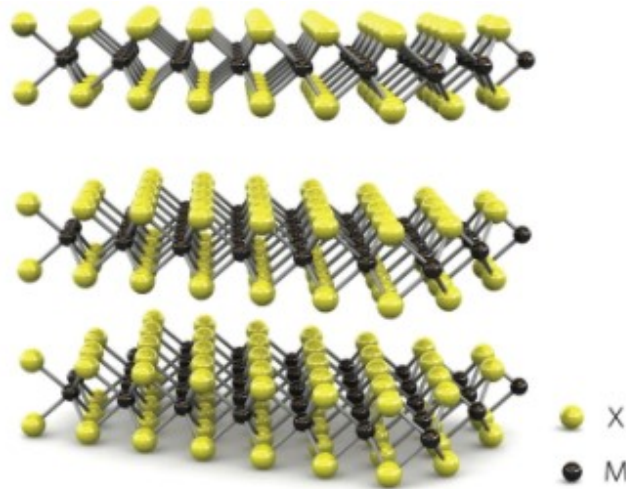
In this chapter, the fundamental concepts and background are established to set the tone for further discussion. Section 2.1 introduces the literature of two dimensional (2D) materials and in particular tungsten diselenide ( $\text{WSe}_2$ ). The chapter then proceeds to discuss dielectrics (silicon oxide) and high- $\kappa$  dielectrics including their characteristics and application. The final section of the chapter discusses the science of pyroelectricity (i.e. ferroelectric, the perovskite structure), and their applications.

### 2.1 Background of two dimensional (2D) materials

2D materials gained attention in 2004 after the successful exfoliation of single layer graphene and the subsequent study of their electric properties [10]. Research into 2D materials have continued to gain traction in order to discover better materials and also to expand their applications [11]. Beyond graphene with its overlapping band structure [10], transition metal dichalcogenide (TMD) have also been investigated. According to Wilson et al. [2], TMD are layered materials that can be cleaved down to less than 100 nm. TMDs consists of one atom of a transition metal and two atoms of a chalcogen element covalently bonded together (X-M-X). The hexagonal structure of a TMD is presented in Fig 2.1, where each layer is held together by weak Van der Waals force. TMDs have gained attention due to their distinctive electrical and optical properties. Electrically, they cover a wide spectrum of properties, including insulators ( $\text{HfS}_2$ ), semiconductors ( $\text{WSe}_2$ ), semimetals ( $\text{TeS}_2$ ) and metals ( $\text{NbS}_2$ ). The diversity of properties in TMD is attributed to the existence of non-bonding d-bands and the degree to which they are filled. Sahin et al. [12] reported that the band gap of semiconducting TMD increases and transforms to a direct band gap with

## 2. Literature Review

decreasing number of layers, thereby showing promise for nanoscale field-effect transistors and solar cell applications [13]. The lack of covalent bonding between TMD layers allows for material stacking thereby enabling the fabrication of hetero-structures. The two techniques for depositing WSe<sub>2</sub> that I have investigated are exfoliation and pulse laser deposition (PLD).

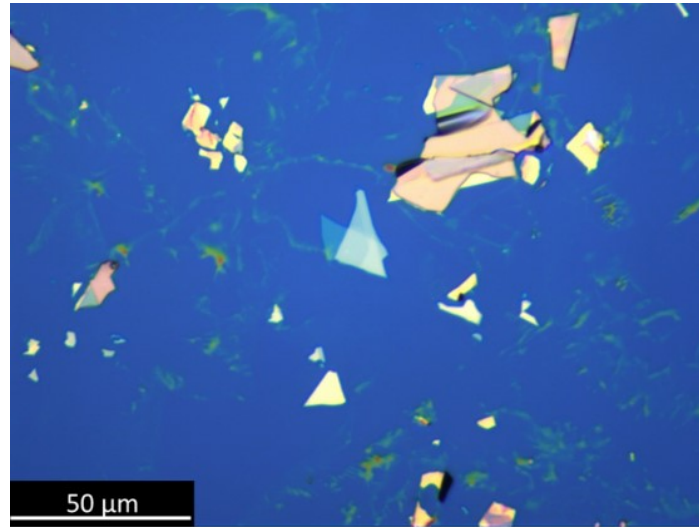


**Figure 2.1:** Hexagonal structure of a TMD [14].

### 2.1.1 Exfoliated tungsten diselenide (X-WSe<sub>2</sub>)

As previously mentioned, exfoliation is one of the methods used to deposit WSe<sub>2</sub> in this experiment. The structural plane of WSe<sub>2</sub> consists of one atom of tungsten (W) and two atoms of selenium (Se) covalently bonded together (Se–W–Se). The atoms of WSe<sub>2</sub> form a hexagonal arrangement with adjacent planes being held together by weak Van der Waals interactions [15]. Due to the layered nature of the WSe<sub>2</sub> and weak inter-layer bonding, the exfoliation used by ref [10] has also been employed to transfer WSe<sub>2</sub> onto a substrate.

## 2. Literature Review



**Figure 2.2:** Picture of exfoliated WSe<sub>2</sub> on a SiO<sub>2</sub>/Si substrate (SMC cleanroom, University of Edinburgh).

WSe<sub>2</sub> flakes have been mechanically exfoliated from bulk WSe<sub>2</sub> using a Scotch tape [13] as shown in Fig 2.2. When WSe<sub>2</sub> is exfoliated and transferred to a substrate, the following is usually observed: random distribution of the material across the substrate, various degree in material thickness and dimension. Though exfoliation produces higher quality samples, it is not possible to control the size and thickness of the material. The inability to control sample size and thickness during exfoliation is inherent in the deposition process. The non-uniformity both in thickness and in dimension makes it difficult to achieve complex fabrication designs including a floating gate structure / hetero-structure design. The size of the 2D material is of importance particularly in IC design and the need to control the material thickness over a large area has necessitated the deployment of bottom up deposition techniques. Pulsed laser deposition (PLD) [3], chemical vapour deposition (CVD) [4] and atomic layer deposition (ALD) [16] are bottom-up deposition techniques that have all been employed in growing 2D materials for larger area, control of material thickness and improving the quality of film produced.

### 2.1.2 Pulsed laser deposition (PLD) WSe<sub>2</sub>

PLD is the second technique that was employed to deposit WSe<sub>2</sub> in this work. Scientists have used this process to deposit an estimate of over two hundred different materials. Investigation into PLD has been in an effort to deposit materials over large substrate sizes with acceptable uniformity [17]. PLD, like CVD, is a bottom-up deposition technique that allows for large area growth (>2 cm) of 2D materials with control in sample thickness and size. The PLD process is a simplified bottom-up deposition technique that requires no additional precursors except the target of the deposited material [3]. The deposition process is relatively quick as samples can be grown in 30 minutes at temperatures of around 450 °C. CVD on the other hand requires a higher growth temperature between 750 - 1000 °C, additional precursors and has a longer processing time [18]. Furthermore, PLD provides excellent thickness control as the material thickness is dependent on the number of laser pulses, thus, possessing high repeatability [3], [19]. Seo et.al [20] reported a centimetre scale monolayer of PLD WSe<sub>2</sub> thin film on SiO<sub>2</sub>/Si substrate. In their analysis of the PLD technique, good layer uniformity and excellent control of the material thickness has been achieved. Moreover, a few challenges exist in the bottom up deposition techniques such as defect, domain size, and stoichiometry control [15].

### 2.1.3 Timeline of 2D Materials

While the PLD technique has not been robustly researched, exfoliation has been widely known since 2004. Early publication on WSe<sub>2</sub> was around 2013 [21], [22], however widespread interest in the various 2D materials began a few years after their initial publications. The table below shows the timeline of the 2D materials:

**Table 2.1:** Experimental and theoretical timeline of 2D materials [23], [24], [25], [26]

Timeline	Material
2004	Graphene
2010	Silicene
2014	Phosphorene; Germanene; Stanene; Borophene
2016	Antimonene; Indiene; Arsenene; Bismuthene; Tellurene; Selenene (WSe <sub>2</sub> )
2018	Gallenene; Aluminene; Plumbene
2021	Beryllonitrene

Table 2.1 shows the chronology of 2D materials. The advent of surface science can be traced to the early 20<sup>th</sup> century from the work of Langmuir. Langmuir's study of thermionic phenomena produced effects that later became the heart of the electronics industry [23]. Notable contributions in surface science is the investigation of metal adsorbents on metal crystal surface [24]. However, renewed interest in 2D materials occurred in 2004 with the successful exfoliation of graphene and the ensuing study of its electronic properties and applications [10]. Further interest in the study of other 2D materials arose due to the new and exciting physics in optoelectronics and so on [11].

## 2. Literature Review

**Table 2.2:** Current and future applications of 2D materials [25], [29], [30], [31]

Electronics	Optoelectronics
Gas and chemical sensing	Detectors / emitters
Flexible / low power electronics	Photonics
Spintronics	Photovoltaics
	Plasmonics
Mechanical Device	Energy
Flexible transistor	Battery
Strain sensor	Super capacitors
Nanogenerator	Thermoelectric
Nanoelectromechanical systems (NEMS) resonator	
Memory	
Resistive random-access memory (RRAM)	
Ferroelectric random-access memories (FeRAM)	
Magnetic random-access memory (MRAM)	

2D materials have found applications in optoelectronics, mechanical devices, energy, memory, electronics and sensing as shown in Table 2.2. 2D materials exhibit advantageous properties including high mobilities, high on/off ratios and high sensitivities to absorbed molecules, making them attractive as field effect transistors and sensors. Few layers of phosphorene is one of the first 2D materials to demonstrate high field effect mobility of  $286 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , and on/off ratio of up to  $10^4$  [25]. Since then, mobility values of up to  $1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  and  $1200 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  have been demonstrated for a few layers of phosphorene and silicene FETs respectively [26], [27]. Gas sensors have also been developed from phosphorous FET capable of detecting about 28 ppm of

## 2. Literature Review

methanol gas [28]. Rui [29] also demonstrated the sensitivity of selenene FET's to  $\text{XeF}_2$  gas. A number of 2D materials including  $\text{WSe}_2$  and black phosphorus can emit photons via electron-hole recombination [30]. As a result, optoelectronic devices including light emitting diodes (LED) have been demonstrated [31]. According to Rui [32], 2D materials possess high anisotropy between the in-plane and out-of-plane axes. Pure 2D materials have covalent bonding with atoms in the same plane resulting in strong in-plane mechanical properties. However, their layers are stacked together by weak Van der Waals forces, which then allows for interlayer sliding when shear stress is applied. Monolayer graphene has been reported by ref [33] to be the strongest material ever measured with a Young's modulus of 1 TPa and breaking point of  $42 \text{ Nm}^{-1}$ . As a result of these mechanical properties, 2D materials have found application as flexible transistors [34], strain sensors [35] and nanogenerators [36] and so on. The incredible properties of 2D materials have also enabled their applications in energy and memory. Miniaturisation of electronics with interest in flexible electronics have given focus to 2D materials due to their form factor and high specific surface areas. 2D materials have been employed in battery design to improve the direction of diffusion across the electrodes, leading to high Li-ion capacity [37]. 2D materials have also been found to exhibit ferromagnetic [38] and ferroelectric [39] properties showing promise in non-volatile memory application.

## 2. Literature Review

### 2.2 Dielectrics

A dielectric is nearly an insulator material that can be polarised upon the application of an electric field. Within an electric field, the electric charges in the dielectric will respond through the change in dielectric polarisation [40]. Furthermore, the energy bandgap of a dielectric can range from 3.3 eV for high- $\kappa$  dielectric such as barium strontium titanate (BST) and to 9 eV for silicon dioxide ( $\text{SiO}_2$ ), a low- $\kappa$  dielectric [41]. A number of dielectric materials exist but the most popular in CMOS processes is silicon dioxide.

#### 2.2.1 Silicon dioxide ( $\text{SiO}_2$ ) - The gate dielectric

Silicon dioxide ( $\text{SiO}_2$ ) is among the most common dielectric materials today owing to its application in the semiconductor industry as the traditional gate dielectric. The rapid progress of complementary metal-oxide semiconductors (CMOS) integrated circuit technology since the late 1980's has attested to the global acceptance of Si-based microelectronics [42].  $\text{SiO}_2$  is native to Si and can be grown thermally. The properties of  $\text{SiO}_2$  that have made it an excellent material choice for over 40 years are shown in Table 2.3.

## 2. Literature Review

**Table 2.3:** Properties of SiO<sub>2</sub> gate dielectric [48]

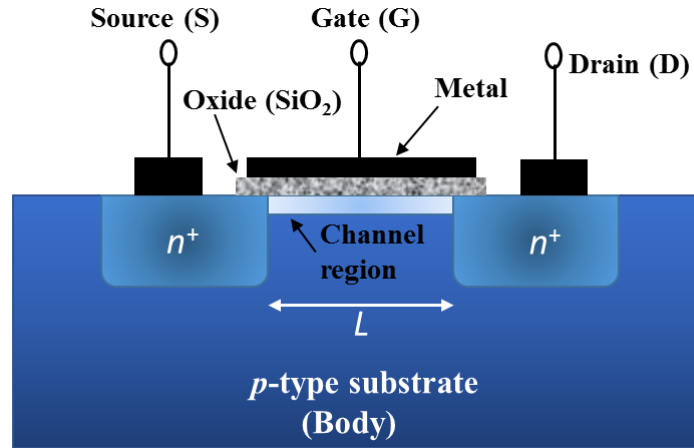
---

SiO <sub>2</sub> is the only stable oxide phase on Si
Melting Point = 1713 °C
Energy gap = 9 eV
Resistivity $\sim 10^{15} \Omega \text{ cm}$
Dielectric constant = 3.9
Dielectric strength $\sim 10 \text{ MV/cm}$
Electron band offset with Si $\sim 3.2 \text{ eV}$
Charge trap density $\sim 10^{10} \text{ cm}^{-2}$

---

The use of SiO<sub>2</sub> in CMOS technology has the following key advantages: high thermal conductivity and stability, high quality Si-SiO<sub>2</sub> interface, superior electrical isolation, ease of formation from simple reaction of silicon with oxygen, high mechanical strength and stiffness, chemical stability among others [40], [42]. The metal-oxide semiconductor field effect transistor (MOSFET) shown in Fig 2.3 has been the building block of the integrated circuit (IC) owing to the economic and technological superiority of SiO<sub>2</sub>. However, one of the challenges of SiO<sub>2</sub> is scaling which will be discussed in the next subsection.

## 2. Literature Review



**Figure 2.3:** The n-channel MOSFET.

### 2.2.1.1 Scaling and performance

The quest for more computing at lower cost has been the driving force in transistor scaling. Scaling has revolutionised the semiconductor industry by way of miniaturising electronics equipment to include complex functions in limited space and with minimum weight [43]. Shrinking the MOSFET implies decreasing its channel length and gate dielectric thickness. By doing so, the density of components that can fit into a silicon wafer increases, hence, significantly reducing the cost of production. Miniaturisation improves the switching speed of devices and increases the drive current of a MOSFET as its physical length is reduced. The model below describes the relationship between the drive current and the physical dimensions [44]:

$$I_D = \frac{W}{L} \mu C_{inv} \left( V_G - V_T - \frac{V_D}{2} \right) V_D \quad Eq. (2-1)$$

where  $W$  is the width of the transistor channel,  $L$  is the channel length,  $\mu$  is the channel carrier mobility,  $C_{inv}$  is the gate dielectric capacitance when the channel is in inversion,  $V_G$  and  $V_D$  are the transistor gate and drain voltages, respectively, while  $V_T$  is the threshold voltage.

## 2. Literature Review

Eq. 2-1 shows that the drain current is proportional to the average charge across the channel ( $\frac{V_D}{2}$ ) and the average electric field ( $\frac{V_D}{L}$ ) along the channel. Hence,  $I_D$  increases linearly with  $V_D$  and saturates when  $V_{D\ sat} = V_G - V_T$  and then yields [42]:

$$I_{D\ sat} = \frac{W}{L} \mu C_{inv} \frac{(V_G - V_T)^2}{2} \quad Eq. (2-2)$$

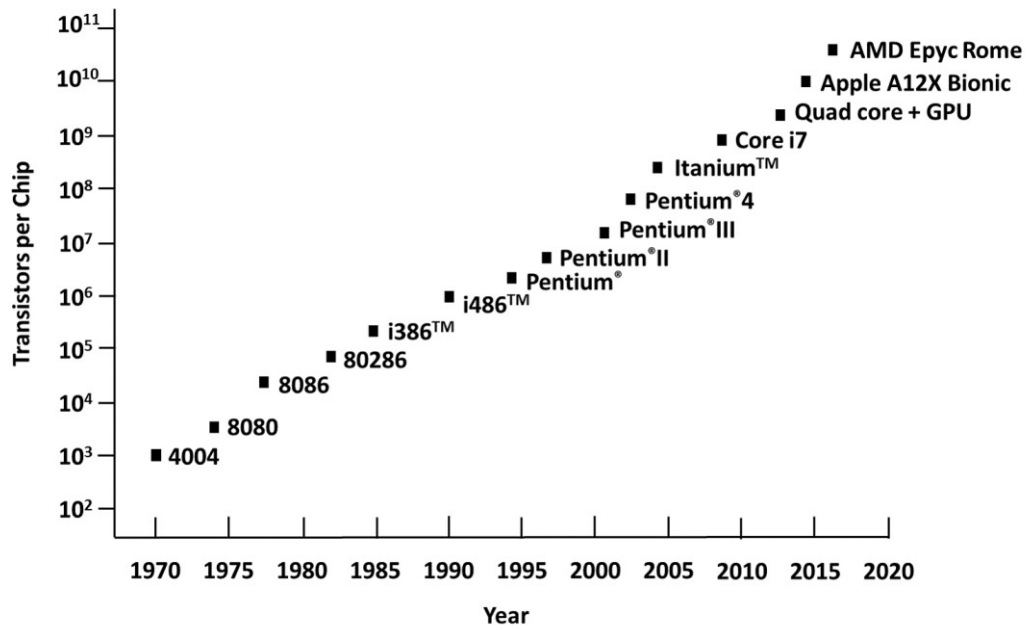
From the simplified models, the  $I_D$  increases from a reduction in channel length or due to increase in the gate dielectric capacitance. In the case of the dielectric capacitance  $C$ , a reduction in channel length would reduce the effect of the gate capacitance on the MOSFET. In order to compensate for this reduced effect, properties of the capacitor have to be taken into account. Consider Eq. 2-3 below:

$$C = \frac{\kappa \epsilon_0 A}{t} \quad Eq. (2-3)$$

Where  $\kappa$  is the dielectric constant,  $\epsilon_0$  the permittivity of free space,  $A$  the area of the capacitor plate and  $t$  the thickness of the dielectric material. From Eq. 2-3, increase in gate capacitance is achieved by reducing the thickness of the dielectric material or employing a high- $\kappa$  dielectric.

Moore predicted in 1965 that the number of transistors per silicon chip would double every 18 months and this is commonly known as Moore's law [43]. In an effort to meet this prediction, scientists have continued to look towards alternative materials in CMOS technology due to the limitations (scaling) of the semiconductor champion, silicon.

## 2. Literature Review



**Figure 2.4:** Moore's Law [40], [45].

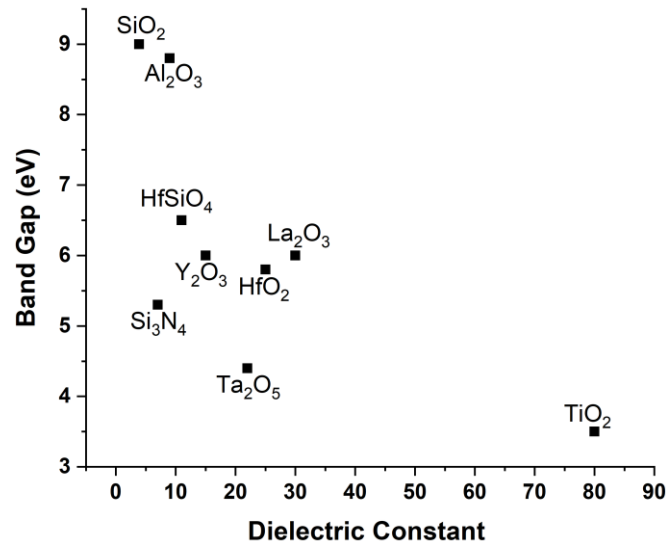
### 2.2.1.2 Scaling challenges of SiO<sub>2</sub>

As the thickness of SiO<sub>2</sub> gate dielectric reduces, scientists have encountered significant concerns which have now dictated the limits to scaling. The thickness limit for the SiO<sub>2</sub> dielectric has been stated to be approximately 1nm [46], [47]. The dielectric leakage current is of particular concern as it affects the operation of CMOS devices in areas of reliability, power dissipation and lifetime. To reduce the leakage current and still maintain the same capacitance, a thicker film with a higher dielectric constant would be required. While a thicker dielectric should reduce the leakage current, another factor to consider is the dielectric bandgap. The barrier height between the electrode and the conduction band of the insulator would put the tunnelling current within reasonable limits [40].

## 2. Literature Review

### 2.2.2 High- $\kappa$ dielectric

High- $\kappa$  dielectrics are defined as insulators with a dielectric constant greater than that of silicon nitride ( $\text{Si}_3\text{N}_4$ ,  $k = 7$ ). There are a number of high- $\kappa$  dielectrics such as titanium oxide ( $\text{TiO}_2$ ), aluminium oxide ( $\text{Al}_2\text{O}_3$ ), hafnium oxide ( $\text{HfO}_2$ ), tantalum oxide ( $\text{Ta}_2\text{O}_5$ ) among others. Some of the more common high- $\kappa$  materials are presented in Fig 2.5 showing their band gap and dielectric constant [40].



**Figure 2.5:** Relationship between bandgap and dielectric constant for some high- $\kappa$  materials [48].

## 2. Literature Review

### 2.2.2.1 Characteristics of high- $\kappa$ dielectric required for CMOS application

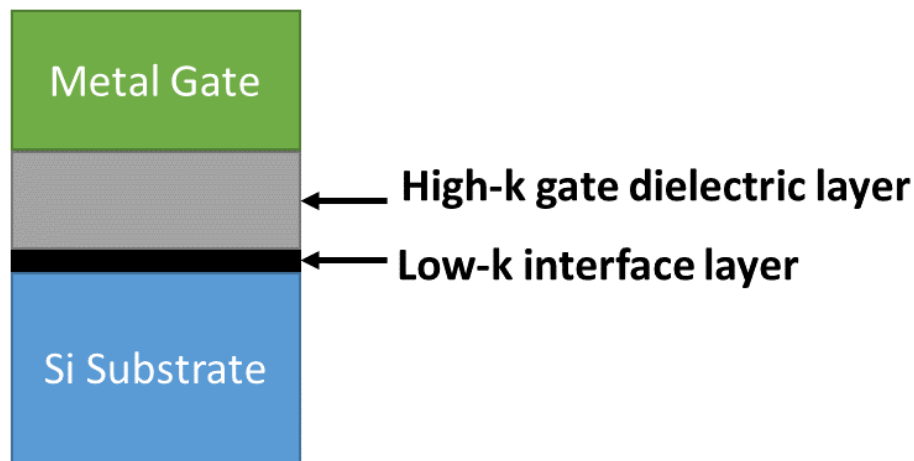
A suitable dielectric to replace  $\text{SiO}_2$  in CMOS application has not been an easy decision as a result of some unresolved issues related to material characteristics and process integration. The issues include:

**Relative permittivity ( $\kappa$ ):** A gate dielectric with a higher relative permittivity ( $\kappa$ ) than that of  $\text{SiO}_2$  is preferable. A  $\kappa$  value of over 10 is required, preferably between 25 and 30 [49]. Fig 2.5 shows that the bandgap  $E_g$  of high- $\kappa$  materials varies inversely with their  $\kappa$  values. So, we might settle for a relatively low- $\kappa$  value [50].

**Bandgap and band offset:** Leakage current increases exponentially with decreasing barrier height for electron tunnelling transport. Additionally, a gate dielectric with a large conduction band offset ( $\Delta E_C$ ) to silicon and other gate metals would decrease the leakage current value. Since the  $\Delta E_C$  value isn't readily available, a general indication would be the bandgap ( $E_g$ ) of the dielectric as a large  $E_g$  tends to correspond to a large  $\Delta E_C$  [42].

**Thermodynamic stability on silicon (Si):** This requirement stipulates that the high- $\kappa$  material does not react with Si to form another interfacial oxide ( $\text{SiO}_2$ ) as shown in Fig 2.6 below. Most of the high- $\kappa$  metal oxides have unstable interfaces with Si forming undesirable interfacial layers. An ultrathin interfacial layer would possess uniformity and reliability concerns as  $\text{SiO}_2$  does in thin form [42].

## 2. Literature Review



**Figure 2.6:** Low- $\kappa$  interface layer formed between high- $\kappa$  gate and silicon substrate.

**Film morphology:**  $\text{SiO}_2$  is an excellent material for CMOS operations as it remains amorphous at temperatures up to 1000 °C [49]. Most high- $\kappa$  oxides easily crystallise at low temperatures [42], particularly  $\text{ZrO}_2$ ,  $\text{TiO}_2$  crystallise at much lower temperatures [51].

**Table 2.4:** Comparison of some deposition techniques [45]

Method	ALD	MBE	CVD	Sputter	Evaporation	PLD
Thickness uniformity	Good	Fair	Good	Good	Fair	Fair
Film density	Good	Good	Good	Good	Poor	Good
Step coverage	Good	Poor	Varies	Poor	Poor	Poor
Interface quality	Good	Good	Varies	Poor	Good	Varies
Number of materials	Fair	Good	Poor	Good	Fair	Poor
Low-temp deposition	Good	Good	Varies	Good	Good	Good
Deposition rate	Fair	Poor	Good	Good	Good	Good
Industrial applicability	Good	Fair	Good	Good	Good	Poor

## 2. Literature Review

**Process compatibility:** The film quality and properties are correlated with the method of depositing the dielectric. The deposition process should be compatible with current CMOS process, cost and throughput. Various techniques exist for the deposition of high- $\kappa$  dielectric and they include: physical vapour deposition (PVD) such as sputtering and evaporation, chemical vapour deposition (CVD), atomic layer deposition (ALD), pulsed laser deposition (PLD) and molecular beam epitaxy (MBE) [42]. ALD is considered among the most promising deposition techniques (from Table 2.4) for ultra-thin high- $\kappa$  dielectric due to its excellent thickness control, uniformity on large areas and so on [52]. Another technique for developing high- $\kappa$  dielectric is anodization and this technique has been explored in this research.

### 2.2.2.2 Anodization

The history of anodization can be traced to ancient Egypt where skilled alchemists and craftsmen used electrochemical processes to coat materials. In some cases, metals were coated to look like gold for religious or personal reasons, in others, iron was coated into iron oxide and proved to be heat resistant. The process of alchemy includes the cooking of objects / metals in chemical solutions [53]. Anodization is a process for developing metal oxide films using an electrolyte and a constant voltage for a set time [54]. As the charges pass, the thickness of the film increases linearly and the final oxide thickness is dependent on the applied electric field [55]. For instance, a potential difference of 10 V results in a grown oxide with a nominal thickness of approximately 20 nm [54]. Diffusion is an important concept that explains the mechanism of anodic oxidation of a metal. Diffusion is defined as the movement of particles from a region of higher concentration to a region of lower concentration. During anodization, metal ions from the bulk metal and electrons from the applied current are transported to the surface of the substrate where they react

## 2. Literature Review

with electrolyzed ions from the electrolyte to form anodic metal oxide [56]. Anodization has been used to grow oxides on aluminium [57], copper [58] and tantalum [59]. The anodization of tantalum (Ta) into  $\text{Ta}_2\text{O}_5$  is an established technique in electronics manufacturing and has been most frequently used to form the dielectric of electrolytic capacitors. Anodization produces a dense and homogeneous oxide of reproducible thickness, having a high dielectric constant [55], [60], [61]. These characteristics, compounded with the fact that the process is relatively simple and inexpensive, makes anodic  $\text{Ta}_2\text{O}_5$  an attractive gate oxide alternative, for the development of high- $\kappa$  electronic devices.

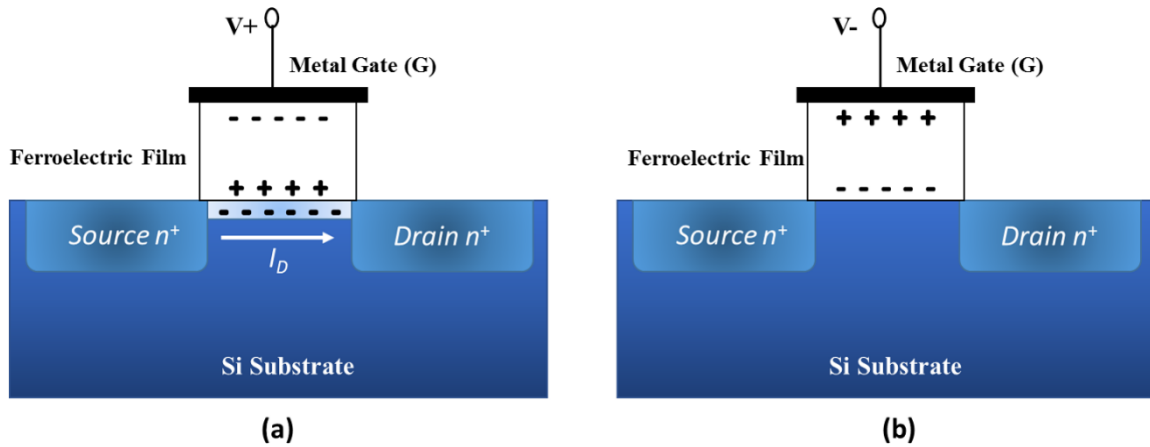
### 2.2.3 Application of novel high- $\kappa$ dielectric

High- $\kappa$  dielectrics have found application in memory devices and field effect transistors (FET). As memory devices, they are fabricated into capacitive structures and leverage is on their ability to store charges. In FET's, their ability to polarise enables the actuation of devices. Also, their high dielectric constant and bandgap could enable miniaturisation. An example application of novel high- $\kappa$  dielectrics is the ferroelectric gate field effect transistor (FeFET) [40].

#### 2.2.3.1 Ferroelectric gate field effect transistor (FeFET)

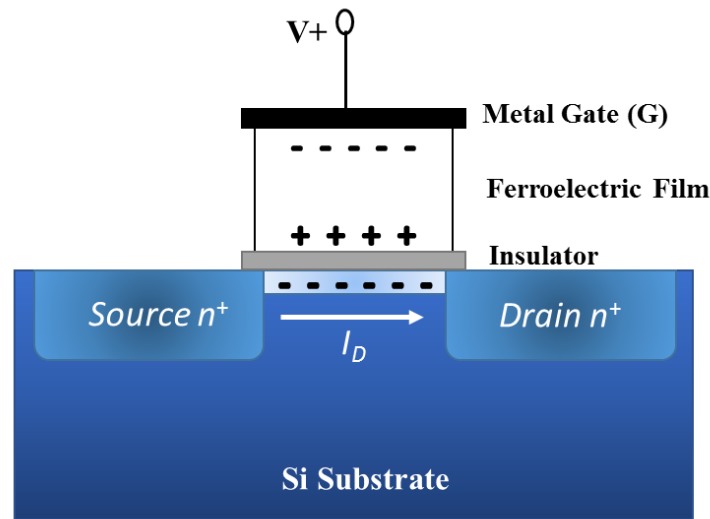
A FeFET has a similar structure as the metal-oxide-silicon (MOS) transistor, the gate dielectric however is replaced with a ferroelectric film. The device works based on the dipole moment of the ferroelectric film which switches the transistor “on” and “off”. Thus, the drain current is controlled by the degree of polarisation of the ferroelectric film. The device configuration and working mechanism is presented in Fig 2.7.

## 2. Literature Review



**Figure 2.7:** Schematic of a FeFET: (a) on state (b) off state.

Ross proposed the FeFET around the 1950's [62] and since then, progress has been made in the field. However, the technology has not been commercialised due to the difficulty to form a good electrical interface between the ferroelectric and semiconductor. A solution was proposed to prevent reactions and charge leakage between the ferroelectric film and silicon substrate. An insulating buffer layer inserted between the ferroelectric film and silicon creates a metal-ferroelectric-insulator-Si (MFIS) structure. The structure is demonstrated in Fig 2.8 and has proven to improve the electrical properties of the device including the data retention time.



**Figure 2.8:** Schematic of the MFIS.

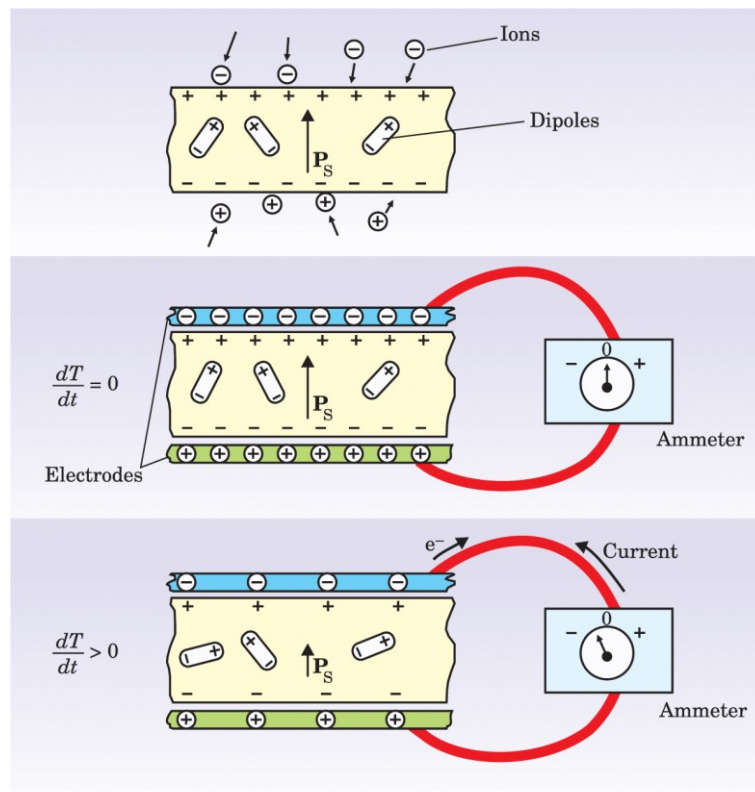
### 2.3 Pyroelectricity

Pyroelectricity is the property of certain crystals to spontaneously polarise in response to a change in temperature [63]. The first observation of pyroelectricity dates back to ancient Greece, more than 23 centuries ago. Then, the mineral lyngourion (presumably tourmaline) was observed to attract ash when hot, and as it cooled, the ash fell off the mineral. In the 17th century, the pyroelectric property of tourmaline was related to electricity. It was described to possess electrical charges of opposite polarity on its two opposing faces. Moreover, major breakthroughs in understanding pyroelectricity occurred in the 19<sup>th</sup> century with the following postulations:

1. The total quantity of electricity produced by a crystal of tourmaline depends uniquely upon the limits within which its temperature is varied;
2. Within the same temperature limits, the quantity of electricity produced during heating is the same as that produced during cooling, but the signs of the charges are reversed; and
3. The quantity of charge produced is proportional to the cross-sectional area of the crystal and is independent of its length.

## 2. Literature Review

Also in the 19<sup>th</sup> century, it was speculated that the electrical effects due to non-uniform heating of crystals might have been by pressure and this led to the discovery of piezoelectricity. Piezoelectric crystals become polarised by an applied mechanical stress. However, it was not until the 20<sup>th</sup> century that applications began with pyroelectric devices such as pyroelectric infrared (IR) detectors [64].



**Figure 2.9:** The pyroelectric effect [65]. Dipole of a pyroelectric material (top), showing charge distribution on the material surface. Electrodes placed on opposite surfaces of the material forms a circuit with an ammeter (middle) showing no flow of current. Current begins to flow as a result of a change in temperature of the pyroelectric material (bottom).

## 2. Literature Review

Spontaneous polarisation of polar materials cannot be measured directly with an electrometer, since charge compensation occurs within the crystal. For this reason, shortening the opposite faces of the crystal does not destroy the spontaneous polarisation. The classic method for detecting spontaneous polarisation is to subject the crystal to a change in temperature. Changes in temperature (increase or decrease) alters the ionic forces within the crystal resulting in a change in the dipole moment. If the temperature of the pyroelectric material remains constant for a considerably long time, surface charges would accumulate on the material and would mask the internal spontaneous polarisation. A rapid change in temperature strengthens the dipoles as there would be no time for charge compensation of the dipoles to occur. Then, by connecting an ammeter between the opposite electrodes of the pyroelectric material, a net current is detected known as pyroelectric current as shown in Fig 2.9 [66]. The relationship between the spontaneous polarisation, pyroelectric current and temperature is shown in Eq. 2-4 below:

$$\Delta P_s = \rho \Delta T \quad \text{Eq. (2-4)}$$

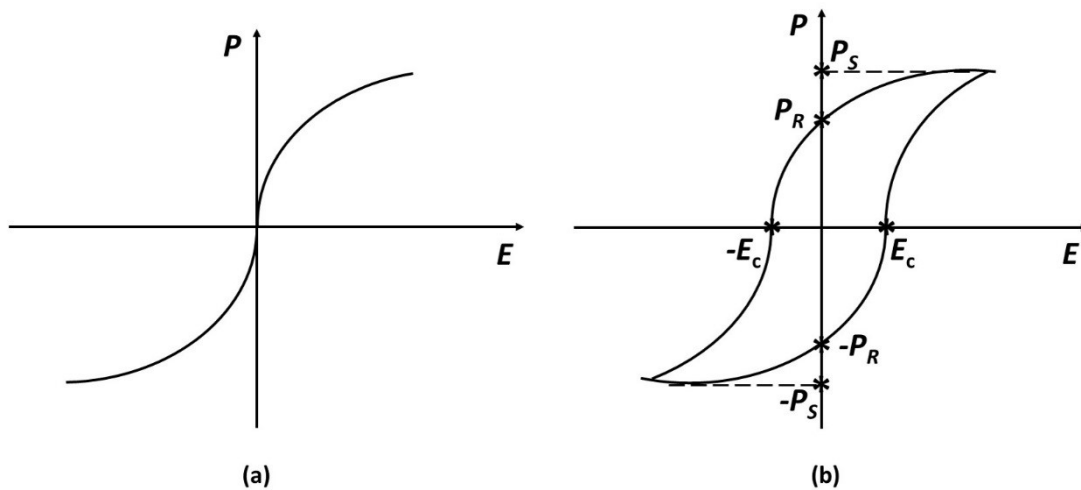
Where  $\Delta P_s$  is the change in polarisation that is the flow of electric charges,  $\rho$  is the pyroelectric coefficient and  $\Delta T$  is the change in temperature.

An important subgroup of pyroelectrics is known as *ferroelectrics*. Materials that fall under the ferroelectric group experience a reversal in polarisation upon the application of an electric field. Ferroelectric is discussed in the sub-section below.

## 2. Literature Review

### 2.3.1 Ferroelectricity

Ferroelectricity is the property of polar dielectrics that possess one or more ferroelectric phases. By 'ferroelectric phase', it implies the spontaneous polarisation can be reoriented by an external electric field [66]. Polar dielectrics that exhibit this property are known as *ferroelectrics* or *Seignette-electrics*. The origin of ferroelectrics dates back to the 17<sup>th</sup> century and was observed in Rochelle salt. Ferroelectrics are a subgroup of pyroelectrics and the term is derived from the analogy with ferromagnetic materials [67]. Both ferroelectrics and ferromagnetics possess a hysteresis loop ( $P$  vs  $E$ ) and show Curie-Weiss behaviour near their phase transition temperature.



**Figure 2.10:** (a) Polarisation vs electric field ( $P$ - $E$ ) of a polar dielectric (b) Hysteresis loop of a ferroelectric material.

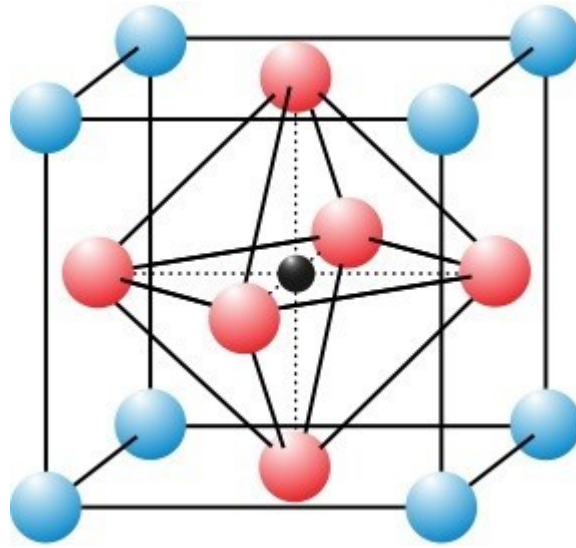
Fig 2.10 (a) shows the  $P$ - $E$  characteristic of a polar material. However, in Fig 2.10 (b), the presence of remnant and saturation polarisation ( $P_R$ ,  $P_S$ ) regions imply the polar material is ferroelectric and has the hysteresis loop as shown. From the hysteresis loop, three parameters are measured and they are: the saturation polarisation  $P_S$ , the remnant polarisation  $P_R$  and the coercive field  $E_C$ . Upon the application of an electric field  $E$ , some domains of the crystal begin to align in the positive

## 2. Literature Review

direction and thus the polarisation  $P$  increases. All the domains align in one direction when the polarisation saturates. At the point of saturation, the crystal is composed of a single domain. As the electric field strength decreases, some domains begin to align in the negative direction, thus reducing the polarisation. Once the electric field is removed, the polarisation does not return to zero rather stops at the remnant polarisation and some of the domains would still remain in the positive direction. When the electric field is increased in the opposite direction, more domains begin to align in the negative direction and the remnant polarisation now begins to reduce. The polarisation becomes zero at the coercive field. Any further increase in the electric field increases the polarisation in the opposite direction as more domains align in the negative direction [66], [67].

### 2.3.1.1 Perovskites

The perovskite structure is a very important group of ferroelectrics known from the mineral perovskite ( $\text{CaTiO}_3$ ). The perovskite forms a large family of oxygen octahedra ferroelectrics with a general formula of  $\text{ABO}_3$  shown in Fig 2.11. It consists of a unit cubic cell, with monovalent or divalent cation at the corners (A sites), tetra- or pentavalent cation at the centre (B sites) and oxygen ions at the face centres [68], [69].  $\text{BaTiO}_3$  was the first ferroelectric perovskite structure to be discovered. This discovery was significant as only hydrogen-bonded crystals were known to exhibit ferroelectricity prior to discovering  $\text{BaTiO}_3$  [70].

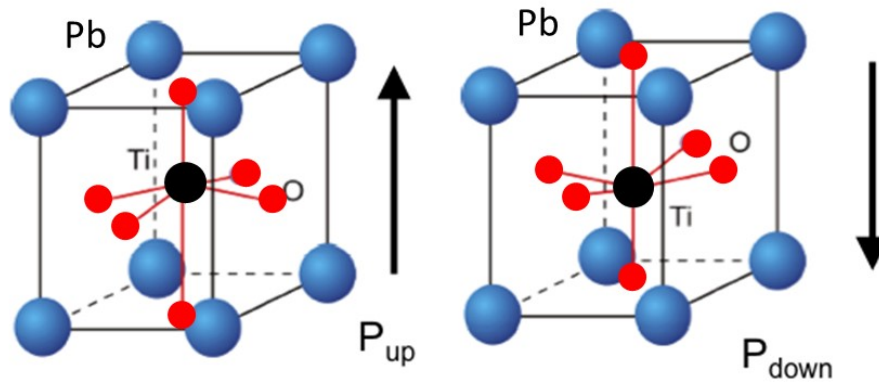


**Figure 2.11:** The perovskite structure. The blue spheres represent the monovalent or divalent cation at the (A sites), the red spheres are the tetra- or pentavalent cation (B sites) and the black sphere is the oxygen ion.

### 2.3.1.2 Lead Zirconate Titanate (PZT)

Lead Zirconate Titanate  $\text{Pb}(\text{Zr}, \text{Ti})\text{O}_3$  has a perovskite structure. The Pb atoms occupy the A-sites, the Ti and Zr atoms occupy the B-sites while the O atoms are located at the centre of the unit cell faces. When an electric field is applied to the unit cell, the Zr and Ti ions move in the direction of the applied field. As a result, the unit cell is randomly oriented with the movement of ions within the crystal lattice. Consequently, the macroscopic changes occur along the dimension of the unit cell and the ceramic as a whole. Fig 2.12 describes the displacement of the Ti ion along one of the six possible axes of the B-site within the unit cell. The direction of polarisation as seen from the arrows in Fig 2.12 is in sync with the movement of the Ti ion. Switching or domain-orientation occurs when many unit cells which are adjacent to each other displace the ion in the B-site along the same direction [71].

## 2. Literature Review



**Figure 2.12:** Schematic of PZT unit cell [72].

### 2.3.2 Applications of Polar Materials

Pyroelectric and ferroelectric materials have found application in astronomy [73], healthcare [74], [75], smart energy systems [76], security [77], pollution monitoring [78], fire sensing [79] and motion tracking [80]. Table 2.5 presents some important historical applications of polar materials and Table 2.6 discusses relevant devices produced from polar materials.

## 2. Literature Review

**Table 2.5:** Historical application of polar materials [77], [87], [88], [89]

Timeline	Event
1941	BaTiO <sub>3</sub> high- $\kappa$ (>1200) capacitors developed
1945	BaTiO <sub>3</sub> reported as a useful piezo transducer, Pat.No. 2 486 560
1954	PZT reported as useful piezo transducer, Pat. No.2 708 244
1957	BaTiO <sub>3</sub> barrier layer capacitors developed
1959	PZT 5A and 5H MPB-type piezo compositions, Pat. No. 2 911 370
1964	FE semiconductor (PTC) devices developed
1980	Electrostrictive relaxor PMN devices developed, Pat. No. 5 345 139
1991	Moonie piezo flextensional devices developed, Pat. No. 4 999 819
1992	RAINBOW piezo bending actuators developed, Pat. No. 5 471 721
1993	Integration of FE films to silicon technology, Pat. No. 5 038 323
1997	Relaxor single-crystal materials developed for piezo transducers
1999	Application in nonlinear optics
2006	Multi Ferroelectrics
2015	Multifunctional application including integration with semiconductors, biosystems and so on

The chronological development in ferroelectrics has been presented in Table 2.5. The need for higher dielectric constant led to research on BaTiO<sub>3</sub> with a dielectric constant of more than 1100 [81]. Further research led to the discovery that ceramic BaTiO<sub>3</sub> is ferroelectric; that an external field could orient the domains within the grains [82]. The ferroelectric property of BaTiO<sub>3</sub> and other materials like PZT identified them to be electrostrictive and electromechanical (piezoelectric), thus, leading to multiple industrial applications [21, 22]. The start of the

## 2. Literature Review

millennium saw more attention set on the domain structures of ferroelectrics, mainly owing to their applications in nonlinear optics [83], [84]. The interrelation between ferroelectricity and superconductivity has also been investigated with emphasis on the pressure [85] and electric field [86] dependence on the superconductivity transition temperature. The captivating property of a multiferroic is that the magnetism and polarity coexist and couple one another [87]. By definition, a single-phase multiferroic material possesses two or all three properties: ferroelectricity, ferromagnetism and ferroelasticity [88]. Areas of interest include transducers, magnetic field sensors and data storage. The emergence of the new frontiers in novel integrated ferroelectrics became popular around 2015. Advances in innovative multifunctional applications have seen application of ferroelectric in bioelectricity, citing benefits such as: exclusion of external electric power source, scalable size and so on [89]. Cutting edge microscopic and macroscopic characterization in the semiconductor industry has witnessed the cross-coupling effects of ferroelectric and 2D materials like graphene [8], WSe<sub>2</sub> [90], and MoS<sub>2</sub> [91].

## 2. Literature Review

**Table 2.6:** Applications of piezo-, pyro- and ferro-electric ceramics [77], [98], [99], [100]

<b>Generators</b>	<b>Motors</b>
<ul style="list-style-type: none"> <li>• Microphones and hydrophones</li> <li>• Accelerometers</li> <li>• Power supplies</li> <li>• Piezoelectric pens</li> <li>• Gas igniters</li> </ul>	<ul style="list-style-type: none"> <li>• Loud speakers</li> <li>• Buzzers</li> <li>• Camera shutters</li> <li>• Inkjet printers</li> <li>• Relays</li> </ul>
<b>Motor / Generator</b>	<b>Resonant Devices</b>
<ul style="list-style-type: none"> <li>• Sonar</li> <li>• Ranging transducers</li> <li>• Medical ultrasound</li> <li>• Fish finders</li> <li>• Filters</li> </ul>	<ul style="list-style-type: none"> <li>• Ultrasonic cleaners</li> <li>• Filters (IF, SAWs)</li> <li>• Transformers</li> <li>• Delay sounding</li> <li>• Radios, TVs and remote control</li> </ul>
<b>Others</b>	<b>Memory</b>
<ul style="list-style-type: none"> <li>• Fire alarms</li> <li>• Gas sensing</li> <li>• Thermal imaging</li> </ul>	<ul style="list-style-type: none"> <li>• Dynamic random-access memory (DRAM)</li> <li>• Nonvolatile ferroelectric random-access memory (NVFRAM)</li> </ul>

The application of piezo-, pyro- and ferro-electric materials cuts across a range of areas including generators, resonators, sensors and memory among others as presented in Table 2.6. The ability to generate electrical charge from mechanical stress in piezoelectric materials has led to the production of piezoelectric based generators. Roundy and Wright [92] developed a 1 cm<sup>3</sup> piezoelectric generator and have demonstrated a power output of 375  $\mu$ W from a vibration source

## 2. Literature Review

of  $2.5 \text{ ms}^{-2}$  at 120 Hz. Energy has been harvested by piezoelectric generators from the motion of the human limbs. In the research of Renaud et. al [93],  $600 \text{ }\mu\text{W}$  has been harvested from a  $25 \text{ cm}^3$  generator at 10 Hz with a 10 cm amplitude linear motion. The electromechanical property of piezoelectricity can be reversed to produce motion upon the application of an electric field. As a result, piezoelectric motors have been developed and powered by either a DC or AC power source. While the DC voltage enables nanoscale high precision movement of 6 nm, the AC voltage allows for high moving velocity 88 mm/s [94]. On the other hand, pyroelectric generators can be used for thermal harvesting as has been presented by ref [95] with a power output of  $3 \text{ }\mu\text{W}$  at a temperature difference of 79.5 K. The resonant frequency of resonators depends on their geometry and mechanical properties [96]. Piezoelectric resonators have found application as electromechanical devices with the quartz crystal being one of the most common [97]. Pyroelectric materials such as ZnO [98] and PZT [99] can produce charges upon the application of heat. As a result, pyroelectric sensors have found application in pollution monitoring [100], flame sensor [101], intruder alarm [77], medicine [102] and gas analysis [75]. Ferroelectric crystals can be polarised in two directions by applying an external electric field as shown in Fig 1.13. This displacement in the positive metallic ion and negative oxygen ion creates a + and – polarisation state. This property of ferroelectrics is applied to nonvolatile ferroelectric random access memories (NVRAMs) to create a logic state “1” and “0” for application in digital memory [103], [104].

### 2.4 Conclusions

The advent of 2D materials as alternative semiconductors in the electronic industry has witnessed their application in numerous areas particularly in flexible electronics. 2D materials are deposited using exfoliation and bottom-up techniques such as pulsed laser deposition. While the techniques have their pros and cons, the relative ease and simplicity of exfoliation allows it to stand out. Research data shows that exfoliated samples possess higher material quality and device performance. Notwithstanding, the bottom-up techniques which rely on deposition tools are controlled better and can produce large material samples fit for CMOS operations.

These 2D materials are often deposited on a silicon dioxide substrate. However, higher dielectric constant ( $\kappa$ ) materials have also been employed to serve as gate oxides for semiconductor operations as their higher capacitances contribute to the overall device performance. Anodization is a method of developing a high- $\kappa$  dielectric material and it is relatively simple and inexpensive to run. By researching anodic oxides, their suitability for 2D FET operations can be assessed and in addition, the performance of the 2D material can be observed.

Another use of 2D materials is in integrated devices, ultimately to improve the overall device output. Research has also shown that pyroelectric devices have attracted interest in the science community and have been integrated with 2D materials. Pyroelectric devices have found application particularly as sensors in fire detection / heat operations, carbon dioxide detection and so on. The relevance of pyroelectric devices has spanned over a century and remains to this today. While pyroelectric materials possess extremely high- $\kappa$  values, they have been used as gate dielectrics and also for applications that require their heat sensing capability.

# Chapter 3

## Materials and Methods

In order to substantiate a result, an experimental validation is often required, and this is commonly achieved through an experimental test set-up. Hence, this chapter describes the main setups used in the experimental work of this thesis. Firstly, the deposition technique for WSe<sub>2</sub> is discussed both for the exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>) and pulse laser deposited WSe<sub>2</sub> (PLD-WSe<sub>2</sub>). Next, the characterization techniques (i.e Raman and Photoluminescence spectroscopy, and atomic force microscopy) for WSe<sub>2</sub> is explained. Section 3.4 then discusses the preparation of Anodic Tantalum, a high- $\kappa$  dielectric and potential gate oxide. PZT; the pyroelectric material used in this project is described in section 3.5. The test set-up for the pyroelectric sensor that allows for the measurement of the pyroelectric current and calculation of the pyroelectric coefficient is also explained. Lastly, the test setup for the electrical characterization of the WSe<sub>2</sub> field effect transistor is described.

### 3.1 Preparation and deposition of exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>)

In this experiment, WSe<sub>2</sub> semiconductor has been exfoliated and transferred onto thermally grown SiO<sub>2</sub> (300 nm)/Si substrates. In order to perform the deposition of WSe<sub>2</sub> on the SiO<sub>2</sub>/Si, the substrate was cleaned to improve the adhesion between the WSe<sub>2</sub> and the substrate. Also, the WSe<sub>2</sub> was exfoliated a few times using Scotch tape to transform the WSe<sub>2</sub> from bulk to thin film before transferring it onto the substrate.

### 3. Materials and Methods

#### 3.1.1 Substrate preparation

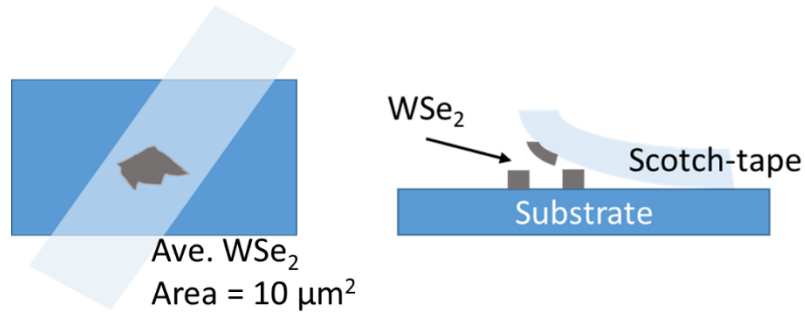
Firstly, the  $\text{SiO}_2/\text{Si}$  substrate is cleaned using acetone, isopropyl alcohol (IPA) and deionized (DI) water in this order. While the acetone removes photoresist residue from any previous steps, the IPA removes the acetone and the DI water rinses off the IPA. The wet substrate is then dried using a nitrogen ( $\text{N}_2$ ) gun. The substrate is further cleaned using oxygen ( $\text{O}_2$ ) plasma. The  $\text{O}_2$  plasma removes any remaining photoresist, completely dries the substrate and aids bonding between the 2D material and the substrate [105]. Once cleaned, the substrate is ready for immediate material deposition before its surface becomes contaminated.

#### 3.1.2 $\text{WSe}_2$ deposition

Exfoliation of 2D materials is a popular method for depositing 2D materials and has been in practice for over a decade. It involves the use of Scotch tape to peel off layers of a bulk 2D material in an effort to thin the sample. The bulk  $\text{WSe}_2$  is placed between two pieces of Scotch tape and when the Scotch tape is carefully separated, the  $\text{WSe}_2$  is cut in half. The process is repeated a few times to thin the  $\text{WSe}_2$  before transferring it onto the substrate. With the  $\text{WSe}_2$  firmly placed against the substrate and sandwiched by the Scotch tape, the set-up is placed on a hot plate to remove air and moisture, hence improving the  $\text{WSe}_2$  adhesion to the substrate. Once the tape is carefully removed, the  $\text{WSe}_2$  remains bonded to the substrate. Due to the delicate nature of the material, care is taken when peeling off the tape as shown in Fig 3.1. To reduce the amount of Scotch tape residue on the substrate, the substrate is immersed in acetone for about 2 hours. It is then cleaned with IPA and DI water respectively. An alternative way of removing tape residue would be to subject the sample to an  $\text{O}_2$  plasma for about a minute. Though  $\text{O}_2$  plasma is faster

### 3. Materials and Methods

and more efficient in removing the tape residue, the risk of oxidising the  $\text{WSe}_2$  is very high and this could change the property / performance of the fabricated device [106], [107].

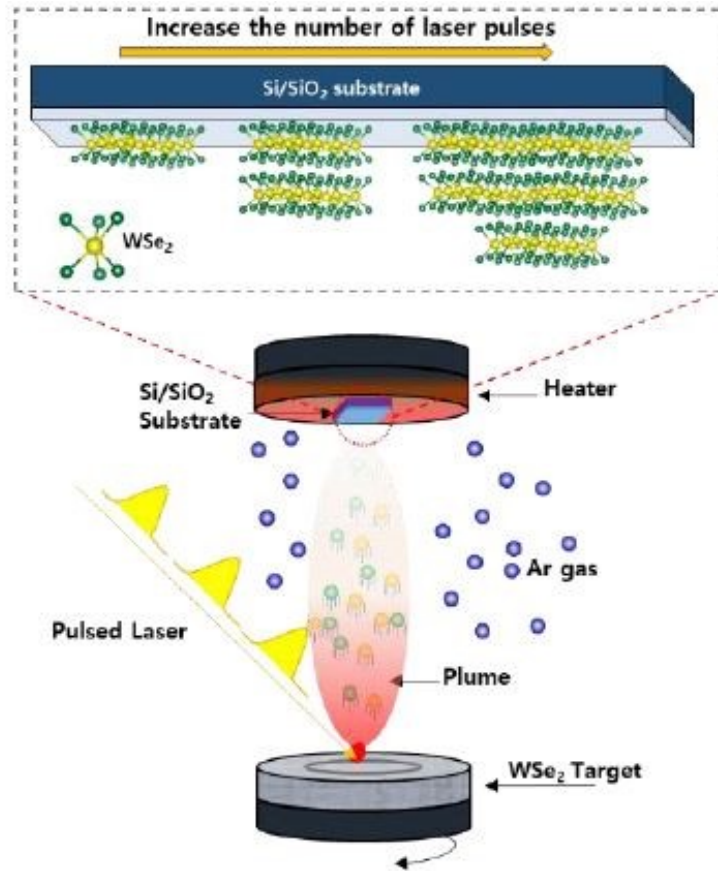


**Figure 3.1:** Schematic of exfoliation and transfer of 2D  $\text{WSe}_2$  onto a  $\text{SiO}_2/\text{Si}$  substrate.

#### 3.2 Deposition of pulse laser deposited (PLD) $\text{WSe}_2$

Pulsed laser deposition (PLD) is a physical vapour deposition process carried out in a vacuum chamber. The operation of PLD is shown schematically in Fig 3.2 and the enclosure consists of a laser source, a target, a substrate and a background gas. To deposit materials off a target, a pulsed laser of sufficient energy is focused onto the material target. With each laser pulse, a small amount of the material vaporises or ablates creating a plasma plume. The plasma plume consisting of the ablated material that has been ejected from the target then scatters onto the substrate [108]. The background gas in PLD serves two purposes. First, some materials require a reactive species as a component of the flux to facilitate multination phase formation. Secondly, the gas helps to slow down the expansion of the ablation plume which could have a kinetic energy in the order of hundreds of electron volts [109].

### 3. Materials and Methods



**Figure 3.2:** Schematic illustrating the working principle of PLD [20]. Performed at the clean room of the Gwangju Institute of Science and Technology, Korea

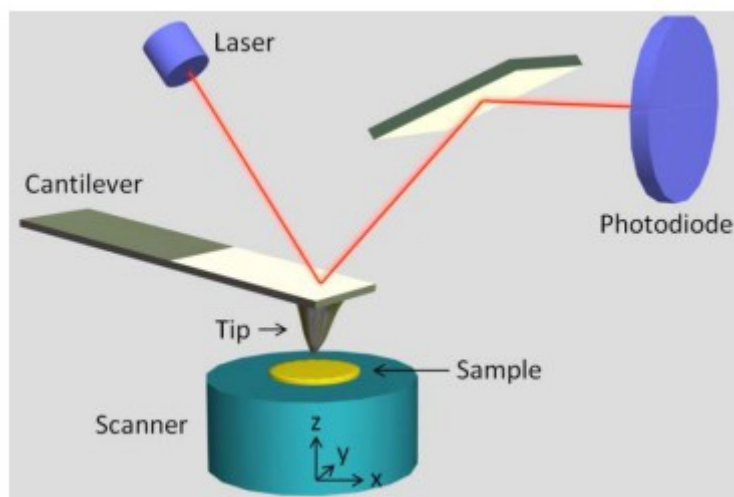
Thin films of WSe<sub>2</sub> were deposited from a WSe<sub>2</sub> target via pulsed laser deposition using a 248 nm KrF (krypton fluoride) excimer laser (Coherent, COMPEXPRO 205F). The WSe<sub>2</sub> film was deposited on 300 nm thick SiO<sub>2</sub> on Si p<sup>++</sup> substrate (1.5 cm × 1.5 cm, chip). Argon (Ar) buffer gas was used to avoid selenium deficiency in the deposited thin film. The growth conditions for the WSe<sub>2</sub> pulse laser deposited thin film are as follows: the pressure is maintained at 100 mTorr under Ar atmosphere; the energy density of the laser is 1 J/cm<sup>2</sup>; the repetition is 3Hz; and the distance between the target and substrate is 5 cm. The frequency of the laser pulses determine the thickness of the WSe<sub>2</sub> films. Therefore, for a 10 nm thick WSe<sub>2</sub>, about 2000 laser pulses are required [110].

### 3. Materials and Methods

#### **3.3 Atomic Force Microscopy (AFM)**

The AFM is a surface characterization tool capable of imaging semi-conducting, insulating as well as conducting surfaces. The AFM uses a nanoscale probe in close proximity with a sample to measure the topography and hardness to name a few. The AFM probe detects intermolecular forces between its sharp tip and the sample. The AFM tip, which is mounted on the end of a micro cantilever beam, deviates as it interacts with the sample's molecular forces. The cantilever acts as a linear spring and deflects in response to the force applied to the sample. The scanning is realised from the movement of either the cantilever tip or the sample by means of piezoelectric actuators in the x and y-direction. As the probe scans across the sample surface, it records the property at particular pixel areas, thereby creating a 3D topographic map of the measured property at a specific location. The scanning by the AFM tip across a sample surface creates deviations in its x,y and z-directions. The forces in the x and y-direction give an indication of surface friction and lateral forces on the cantilever, whilst the z-direction is exclusively the sample topography. An optical level arrangement as shown in Fig 3.3, is commonly used to monitor the cantilever deflection. The laser beam is reflected from the cantilever and onto a photodiode detector. The photodiode records the vertical and lateral motion of the laser beam and is capable of detecting displacements of 1 nm and below with proper design settings.

### 3. Materials and Methods

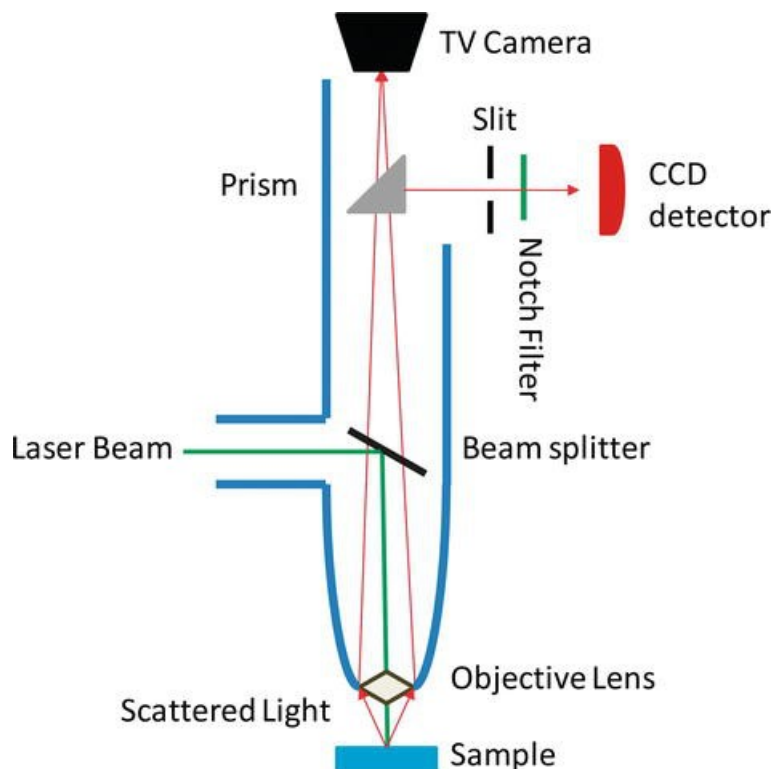


**Figure 3.3:** Schematic illustration of the working principle of an AFM [118]. The laser beam is deflected off the back of the cantilever and onto a photodiode detector. The bending of the cantilever displaces the laser spot on the photodiode.

In this work, the AFM measurements have been carried out with a Bruker D5000 and a NuNano Scout 350R silicon based AFM probe. All measurements were performed at room temperature and in contact mode. The AFM was used to determine the thickness of the WSe<sub>2</sub> and 1 layer of the WSe<sub>2</sub> is approximately 0.7 – 1 nm.

#### 3.4 Raman and photoluminescence (PL) spectroscopy tool

Both Raman and PL spectroscopy have been employed in various studies to characterise the chemical nature or electronic properties of materials. In the experiments, the *inVia Renishaw* equipment was used for both Raman and PL spectroscopy. For PL measurement, the tool's objective lens was changed as a necessary calibration to accommodate the PL scale that extends beyond 2 eV and is significantly broader than the Raman scale which is up to a maximum 0.11 eV.



**Figure 3.4:** Conventional Raman / PL Microscope [111].

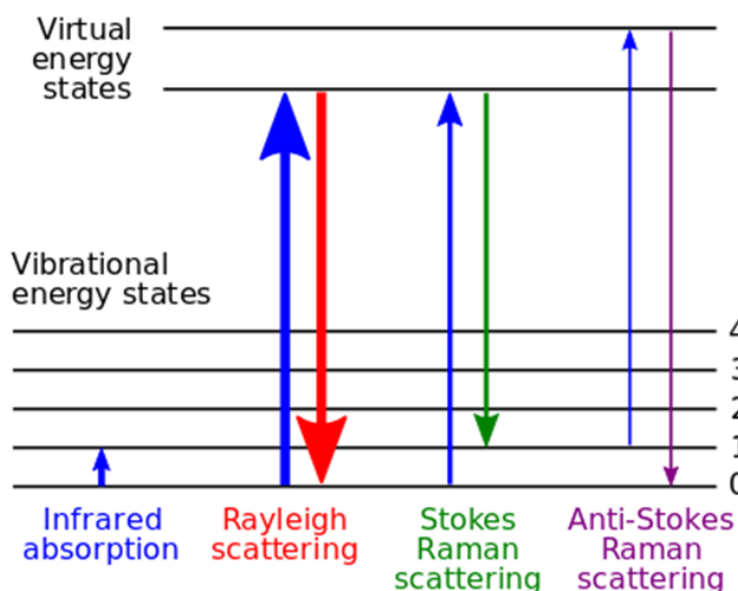
A typical Raman / PL setup has been presented in Fig 3.4. The laser source has a power of 3 mW and about 5% of the power was used to avoid damaging the sample. Raman and PL spectroscopy are non-destructive techniques and usually have no requirement for sample preparation. The laser was focused to approximately 1  $\mu\text{m}$  providing high lateral resolution. Each spectrum acquisition was accumulated at least 10 times to improve the signal to noise ratio of the result.

#### 3.4.1 Raman spectroscopy

Raman is a vibrational spectroscopy technique that has been employed in many areas of science, from fundamental chemistry to material engineering. Raman relies on the inelastic scattering of

### 3. Materials and Methods

phonons to provide a structural fingerprint by which molecules are identified [112]. The Raman technique involves the use of a monochromatic light (usually a laser) to interact with molecules of a material resulting in an upward shift (anti-stokes) or downshift (stokes) in the energy of the laser photons as shown in Fig 3.5. From the vibration of atoms in both position and intensity, detailed information about the molecular structure of a material can be obtained. Characteristic position and intensity of the Raman spectrum gives insight to chemical bonding, inter-and intramolecular forces among others [111].

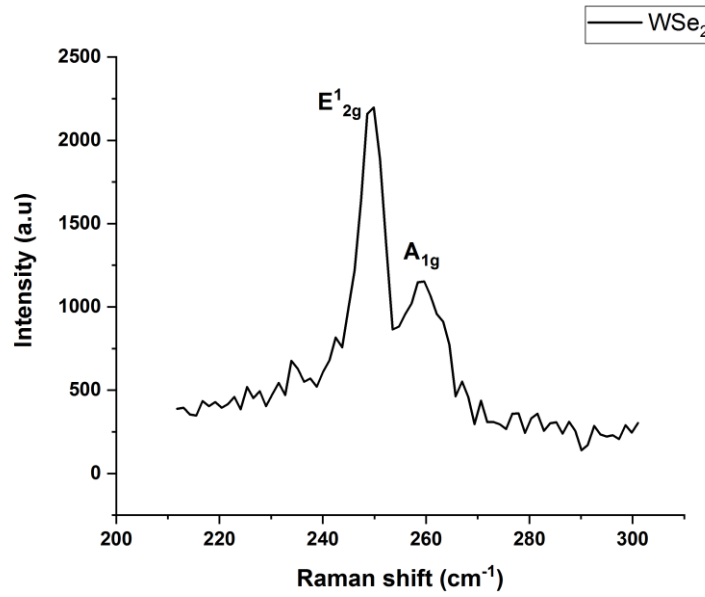


**Figure 3.5:** Energy level diagram showing the states involved in Raman spectra [113]

In the Raman spectrum as shown in Fig 3.5, the energy of the incident photon is absorbed by electrons within the sample. The electron then changes energy state and later, this energy is released resulting in either a higher (anti-stoke mode) or lower (stoke mode) energy of the laser photons. This difference between the magnitude of the released energy and the incident photon determines the Raman mode measured and in our experiment, Stokes Raman scattering has been

### 3. Materials and Methods

measured as the sample is believed to have absorbed some of the incident light energy. Raman spectroscopy has been employed in 2D materials to determine the number of layers of the materials [22], [114], the presence of defects [115] and the doping [116], [117] among others.

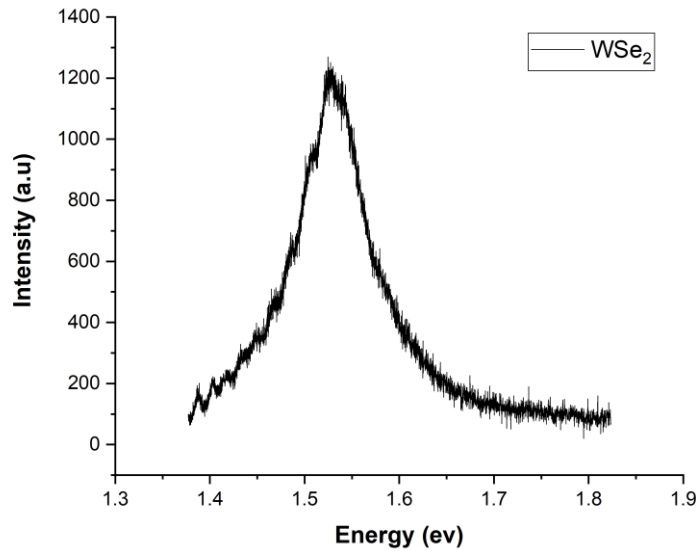


**Figure 3.6:** Raman Spectrum of X-WSe<sub>2</sub>.

The Raman spectrum of a bulk exfoliated WSe<sub>2</sub> is presented in Fig 3.6. From the range of the Raman shift captured (220 – 300 cm<sup>-1</sup>), there are only two noticeable peaks. The in-plane E'<sub>2g</sub> mode from the out-of-phase vibration and the A<sub>1g</sub> mode from the out-of-plane vibrations of WSe<sub>2</sub> [118].

#### 3.4.2 Photoluminescence (PL) spectroscopy

Photoluminescence (PL) is one of the most useful optical methods used in studying semiconductors. PL is capable of detecting impurities and defects in semiconductors and these imperfections could affect the material quality and device performance. PL is also capable of determining semiconductor bandgap, an important parameter in device performance. The technique of PL spectroscopy is similar to Raman as both use incident light to excite an electron into a changing energy state. However, during the PL experiment, the electrons absorb enough energy to leap over the bandgap and into the conduction band thereby creating an electron-hole pair. The excited electron later recombines with the hole with the release of photons [119]. The PL tool then measures the released energy as shown in the figure below.



**Figure 3.7:** Photoluminescence Spectrum of X-WSe<sub>2</sub>.

The photoluminescence spectrum of an exfoliated WSe<sub>2</sub> is shown in Fig 3.7. The single PL peak positioned about the 1.53 eV identifies the A-exciton and trion region. The exciton and trion region

### 3. Materials and Methods

is at the band-edge and contains optically excited electron(s) and hole(s) that are bound together [120], [121]. The bandgap of the WSe<sub>2</sub> is the energy position (1.53 eV) that corresponds with the highest peak [119]. Bandgap extraction from PL plots will be fully described in Chapter 4.

#### 3.5 Anodic tantalum development

The essential components for anodization include a metal anode, the electrolyte, cathode material and externally applied current [56]. With the setup in Fig 3.8, the thickness of the natural oxide of tantalum (other metal) surface can be increased. The details of the procedure is described below:

##### I. Electrolyte Preparation

Items:

- 30 ml Diethylene glycol (Digol),
- 5 g Sodium carboxymethyl cellulose,
- 200 ml DI water,
- 0.6 g Citric acid.

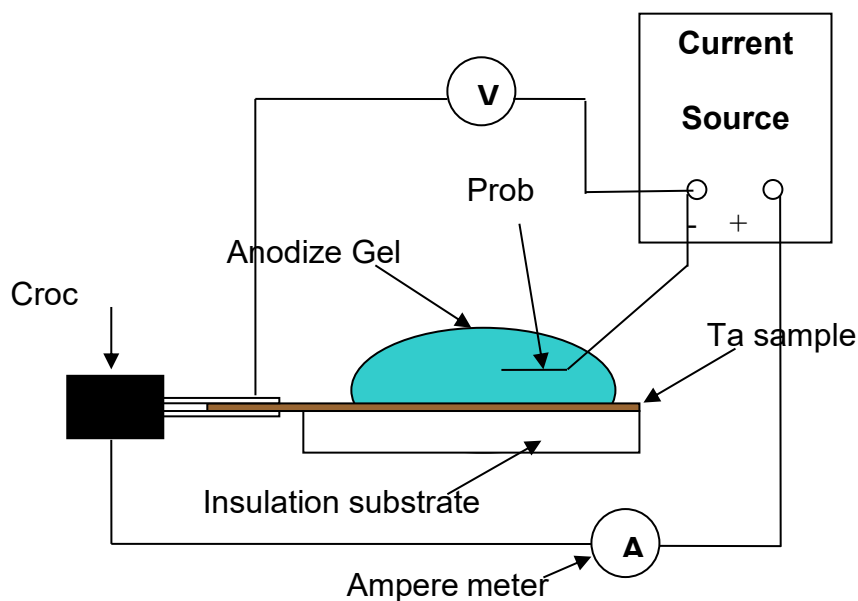
Procedure:

1. Weigh the citric acid and sodium carboxymethyl cellulose (use aluminium foil to hold the sample during weighing and carrying).
2. 100 ml DI water mixed with 20 ml of digol.
3. 5 g of sodium carboxymethyl cellulose is added gradually, at the same time stir it vigorously.
4. Then add 10 ml of digol and 80 ml DI water, stir and leave for 1 hour.

### 3. Materials and Methods

5. Add 0.6 g citric acid and 20 ml DI water, stir and leave for another 1 hour [122].

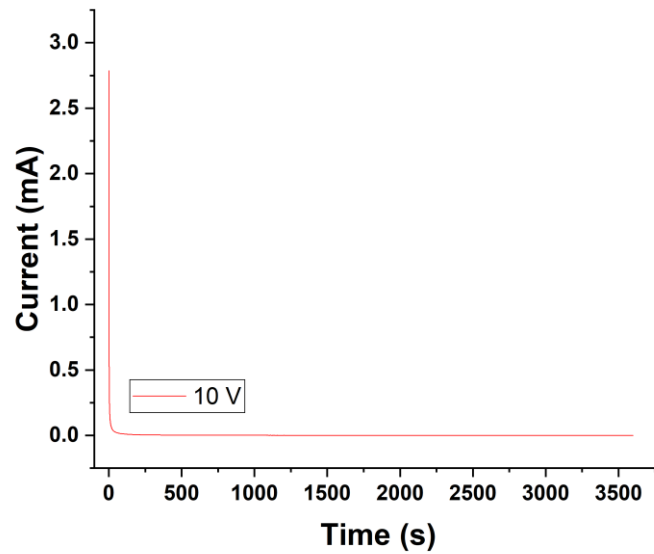
#### II. Anodization Set-up



**Figure 3.8:** Diagram of tantalum anodization System [122].

In this experiment, 470 nm of tantalum (Ta) was sputter deposited on thermally grown silicon dioxide ( $\text{SiO}_2$ ) on a silicon wafer. The wafer was cleaned using Isopropyl Alcohol (IPA), deionized (DI) water and a nitrogen gun ready for anodization. An electrolyte was prepared as stated in “Electrolyte Preparation” above. The electrolyte was dispensed on the selected Ta surface using a pipette and a potential applied between the cathode (probe in contact with the gel) and the anode (probe in contact with the Ta surface) as shown in Fig 3.8. The set-up was left for 60 min and the measured current flowing from anode to cathode reached a value of about  $0.11 \mu\text{A}$ .

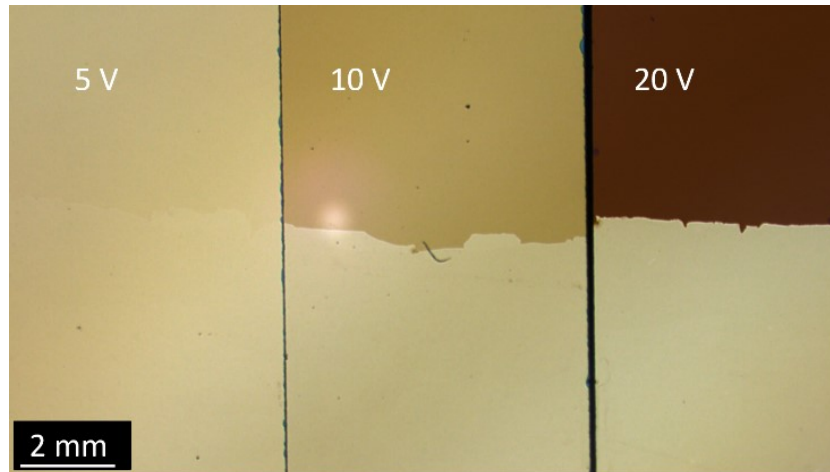
### 3. Materials and Methods



**Figure 3.9:** Anodization current vs time graph.

During the anodization process, the measured current of the applied electric field continually decreases with time as shown in Fig 3.9. This decrease in the measured current is due to the increase in nominal oxide thickness of the sample. As the grown oxide increases, so does the insulation and consequently, the resistance of the sample. Additionally, the quality of the oxide grown improves with time thus reducing the leakage current. From Fig 3.9, at the start of the experiment, a rapid decrease in leakage current can be seen within the first few seconds. This period signifies how quickly the oxide forms at the metal surface. For the remainder of the time, a more gradual oxide formation ensues. The voltage magnitude used for anodization determines the thickness of the metal oxide grown. For an applied potential of 10 V, the grown oxide would have a nominal thickness of approximately 20 nm [54], [122].

### 3. Materials and Methods



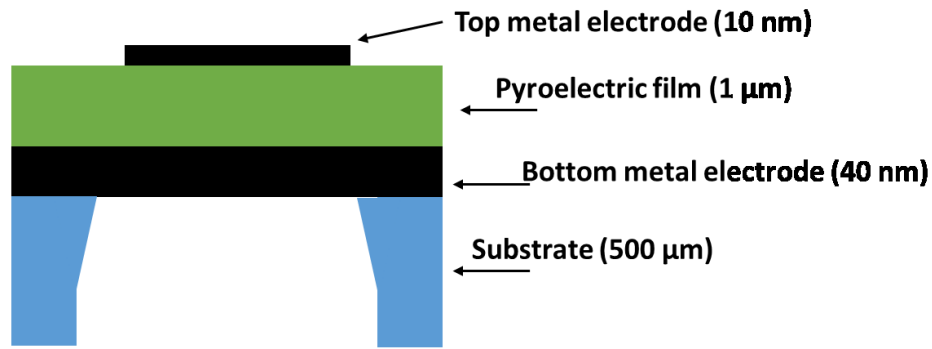
**Figure 3.10:** Anodic tantalum prepared with an applied potential of 5 V, 10 V and 20 V.

Three tantalum metal strips have been anodized and the evidence of the thickness of the grown tantalum-oxide is visible optically as shown in Fig 3.10. The samples show that the anodic tantalum has an area of about  $16 \text{ mm}^2$ . The colour of the tantalum-oxide changes and becomes darker as the thickness increases. Similar observation was made by ref [123], where spectrophotometric measurements were used to estimate the material's thickness.

#### 3.6 Pyroelectric current measurement

A typical pyroelectric infrared (IR) sensor comprises a top electrode (platinum), pyroelectric layer (PZT), bottom electrode and the substrate / membrane. A general schematic is shown in Fig 3.11.

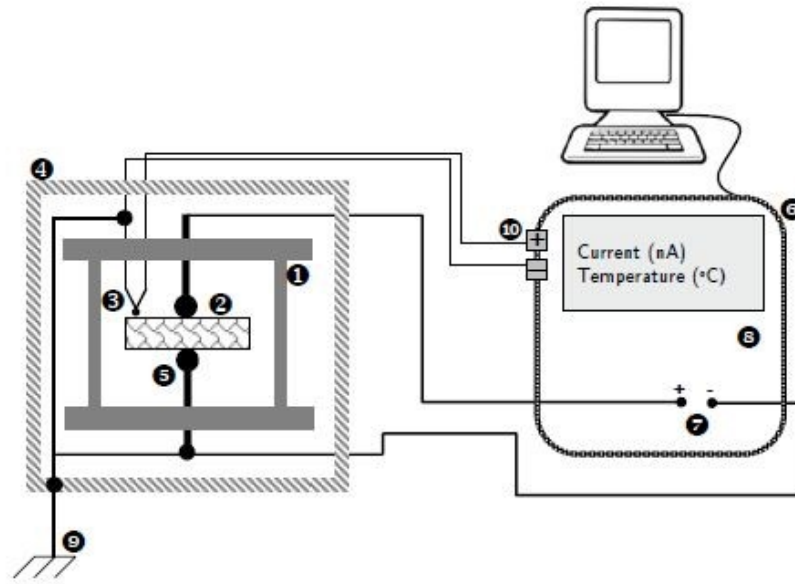
### 3. Materials and Methods



**Figure 3.11:** Typical pyroelectric IR sensor.

The pyroelectric current from a typical pyroelectric IR sensor shown in Fig 3.11 is measured using a static-quasi method (temperature change) [124]. In other words, the PZT sensor is heated by a hot plate during testing. The static-quasi method being the traditional way of measuring pyroelectric properties has been employed to characterise the PZT in this work. The temperature of the heated sample holder was controlled by the “att thermal chuck system”. The cooling effect was produced by “glysantin” (a coolant) which forms part of the att thermal chuck system. The measurement setup is illustrated in Fig 3.12.

### 3. Materials and Methods



**Figure 3.12:** Setup used for measuring pyroelectric current showing probe connection to the device [125].

The setup in Fig 3.12 measures the pyroelectric current and temperature of the pyroelectric sensor. The *sensor* denoted as 2 is placed in the *sample holder* 1 and the *top and bottom contacts* of the sensor are then connected to the probes 5 of the test equipment. Number 3 in the schematic represents the *temperature sensor* which keeps track of the temperature of the sensor all through the testing. 6 represents the *Keithley parameter analyser* which is responsible for collecting measured data. Item 7 and 10 denote the *contact probe and temperature sensor probe* connections respectively. The contact and temperature sensor probe are connected to the keithley parameter analyser which then measures and records the pyroelectric current and temperature of the sensor. The entire setup is *electrically shielded* 4 to prevent external interference and *grounded* 9.

The electrical connection for the pyroelectric sensor is placed on the top and bottom electrode as shown in Fig 3.12. As the incident radiation hits the sample, the temperature of the sensor changes,

### 3. Materials and Methods

thus, the crystals of the pyroelectric layer polarises and produce charges. These charges are then read by the measuring instrument as pyroelectric current.

$$p = \frac{i * t}{A * \Delta T} \quad Eq. (3-1)$$

Where:  $p$  = pyroelectric coefficient

$i$  = pyroelectric current

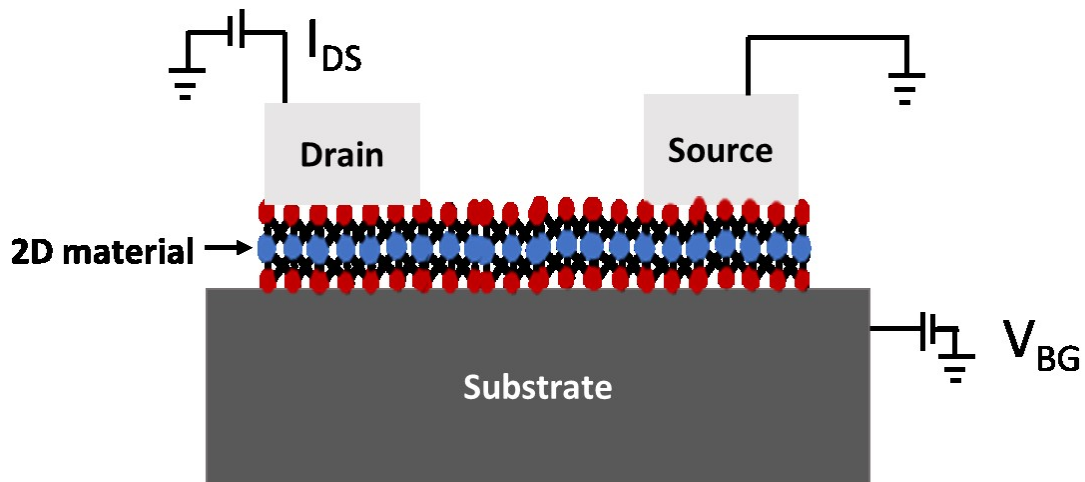
$t$  = time

$A$  = Area of top electrode

$\Delta T$  = change in temperature

#### 3.7 Two-dimensional (2D) material field effect transistor (FET) Test Setup

A generic 2D FET schematic and setup has been presented in Fig 3.13 below. 2D FET's typically consist of a semiconductor material, a metal drain and source contact and a substrate. In order to test the field effect transistor, a Keithley 4200-SCS parameter analyser and a TST-017 Everbeing EB-8 probe station have been employed. The test set-up shows three probes from the test equipment connected to the device's source, drain and substrate. The FET has been back-gated with a potential  $V$  denoted as  $V_{BG}$  which is applied to the highly doped silicon substrate or high- $\kappa$  dielectric substrate. Another potential is applied across the drain and source of the FET, creating a drain-source current denoted as  $I_{DS}$ . The data associated with the  $V_{BG}$  and  $I_{DS}$  is measured and recorded by the test equipment.



**Figure 3.13:** WSe<sub>2</sub> FET schematic showing test set-up

#### 3.8 Conclusions

An overview of the production technique of WSe<sub>2</sub> and anodic tantalum; two key materials used in this project have been presented. WSe<sub>2</sub> has been deposited using mechanical exfoliation and pulse laser deposition (PLD) method. While exfoliation is a relatively simple and less costly method, PLD grows larger sample sizes in addition to good thickness control. To understand and compare the optical properties of the WSe<sub>2</sub>, Raman and Photoluminescence (PL) spectroscopy have been employed. While Raman technique informs on material quality, PL describes the electronic structure. An atomic force microscope (AFM) helps to measure the material thickness to establish synergy with the optical results. Anodization has been employed as a means of producing a high- $\kappa$  dielectric. The relationship between the anodizing current and time gives a hint on the quality of the dielectric formed as lower current values are preferred. Samples from anodic tantalum developed using different voltages have also been presented showing a clear relationship between the colour of the samples and their respective thicknesses. Furthermore, the generic make-up of a pyroelectric sensor has been outlined. The test set-up for characterizing the pyroelectric current and dielectric property of the device has also been discussed. Finally, the test set-up for characterizing the electrical properties of the WSe<sub>2</sub> field effect transistor has been presented and explained.

# Chapter 4

## **Fabrication and electrical characterization of pulsed laser deposited WSe<sub>2</sub> (PLD-WSe<sub>2</sub>) and exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>) field effect transistor (FET)**

### **4.1 Introduction**

In order to meet the project objective of integrating the PZT infrared (IR) sensor with a WSe<sub>2</sub> FET, two deposition techniques (exfoliation and PLD) have been experimented on and the fabricated WSe<sub>2</sub> FET has been studied. The experiments performed in this chapter have enabled us to develop the WSe<sub>2</sub> FET fabrication process and characterisation of the device performance. As previously mentioned, tungsten diselenide (WSe<sub>2</sub>) is a semiconductor consisting of layers held by weak Van der Waals interactions. As a result, exfoliation has been employed to cleave layers of WSe<sub>2</sub> and transfer them on to a substrate. On the other hand, pulsed laser deposition (PLD) has also been employed to deposit WSe<sub>2</sub> on a substrate. In this Chapter, the discussion is centred on WSe<sub>2</sub> deposited via exfoliation and PLD. A number of observations have been made from the physical, optical and electrical properties of the materials with respect to the deposition techniques used. In order to characterise the WSe<sub>2</sub> electrically, field effect transistors have been fabricated, tested and analysed.

## 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

### 4.2 Experimental

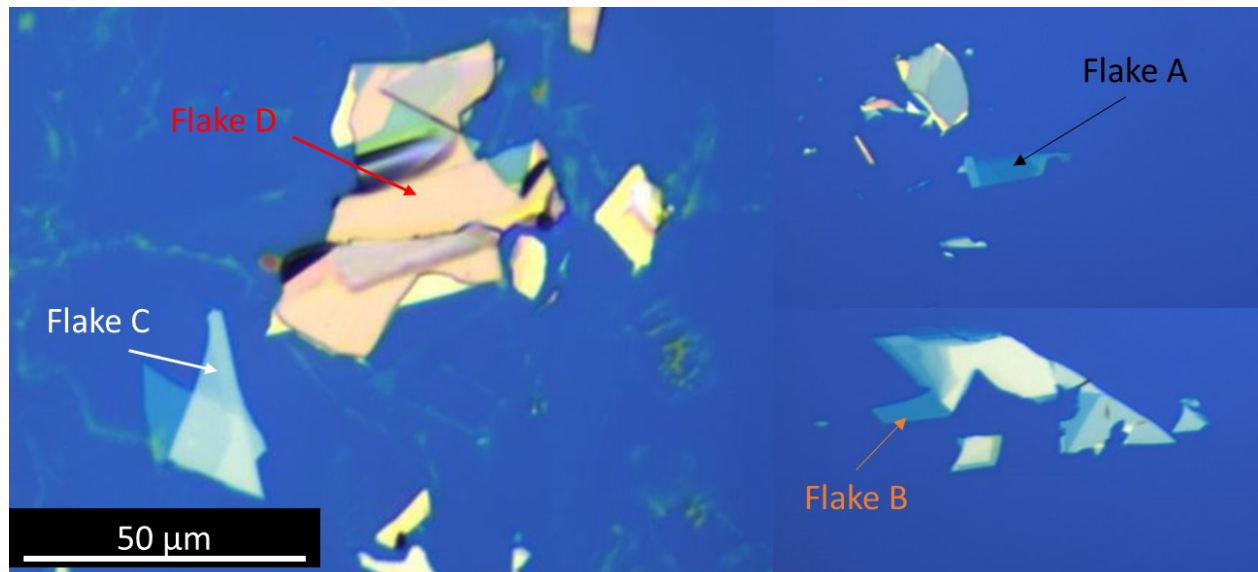
#### 4.2.1 Deposition of exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>) and pulse laser deposited (PLD-WSe<sub>2</sub>)

Reiterating the methodology, Scotch tape has been used to exfoliate a few layers of WSe<sub>2</sub> from bulk WSe<sub>2</sub> and transferred onto thermally grown SiO<sub>2</sub> (300 nm)/Si p<sup>++</sup> substrates. In order to actualize the deposition of WSe<sub>2</sub> on the substrate, the substrate has been prepared thus:

SiO<sub>2</sub>/Si substrate cleaned with Acetone, IPA and DI water;

SiO<sub>2</sub>/Si substrate treated with O<sub>2</sub> plasma for about 30 minutes;

WSe<sub>2</sub> is then transferred onto the substrate and the tape slowly peeled away. As earlier discussed, the X-WSe<sub>2</sub> flakes appear randomly on the substrate with varied shape, size and thickness as shown in Fig 4.1 below:



**Figure 4.1:** X-WSe<sub>2</sub> flake of various thicknesses and dimensions on SiO<sub>2</sub> substrate.

Flakes A, B, C and D are WSe<sub>2</sub> flakes of various thicknesses. The arrows in the graph point to the area of the flakes where the Raman data have been collected. An estimate of the flake thickness

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

can be made from the colouring. Flake D being brown is the thickest, next is the white flake C, followed by the blue one as in Flake B and finally Flake A being semi-transparent. Of course, the colour of the substrate influences the colour of the flakes, however, their thicknesses have been confirmed with an AFM. The method of measuring the WSe<sub>2</sub> thickness with an AFM has been described in Section 3.3 of Chapter 3. The AFM results of the profile scan are shown in Appendix D and they are outlined in Table 4.1 below.

**Table 4.1:** Flake A, B, C and D thicknesses

Flake	Thickness (nm)	Size (μm)
A	5 – 7	20
B	10 – 12	20
C	21 - 24	30
D	46 – 50	50

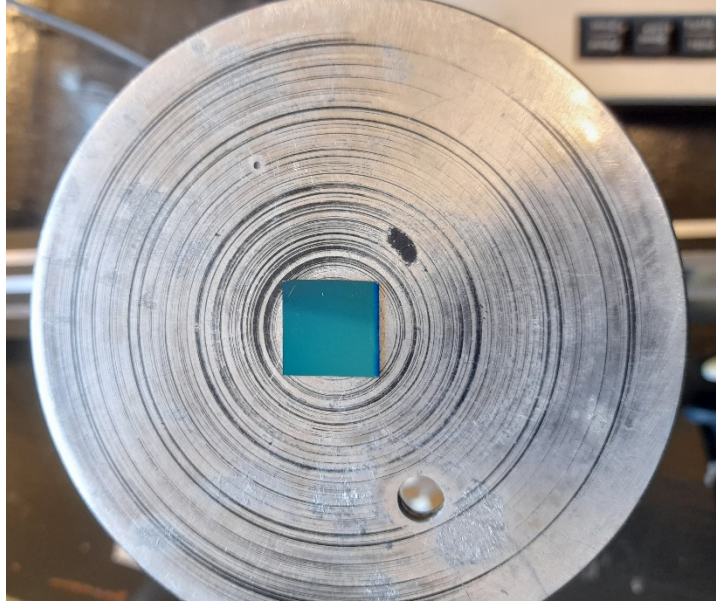
On the other hand, PLD-WSe<sub>2</sub> has been deposited from targets of tungsten and selenium films via pulsed laser deposition with a 248 nm KrF excimer laser (Coherent, COMPEXPRO 205F). WSe<sub>2</sub> film produced has been deposited on 300 nm thick SiO<sub>2</sub> on Si p<sup>++</sup> substrate (1.5 cm × 1.5 cm, chip).

The growth conditions are as follow:

- The chamber pressure maintained at 100 mTorr under Ar atmosphere (Ar buffer gas has been used to avoid Se deficiency);
- Laser energy density of 1 J/cm<sup>2</sup> with a repetition of 3 Hz;

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

- Distance between the target and substrate is 5 cm.



**Figure 4.2:** PLD WSe<sub>2</sub> deposited across a 1.5 by 1.5 cm chip and supplied by the Gwangju Institute of Science and Technology, Korea.

Fig 4.2 shows a 1.5 cm by 1.5 cm SiO<sub>2</sub>/Si chip with PLD-WSe<sub>2</sub> deposited across its entire surface. While the PLD technique has good thickness control and broader deposition area, exfoliation on the other hand produces randomly distributed flakes of varied thicknesses and lateral size. Table 4.2 below shows the sample thickness and the number of laser pulses used for the deposition:

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

**Table 4.2:** Thickness of PLD WSe<sub>2</sub> Sample 1, 2, 3

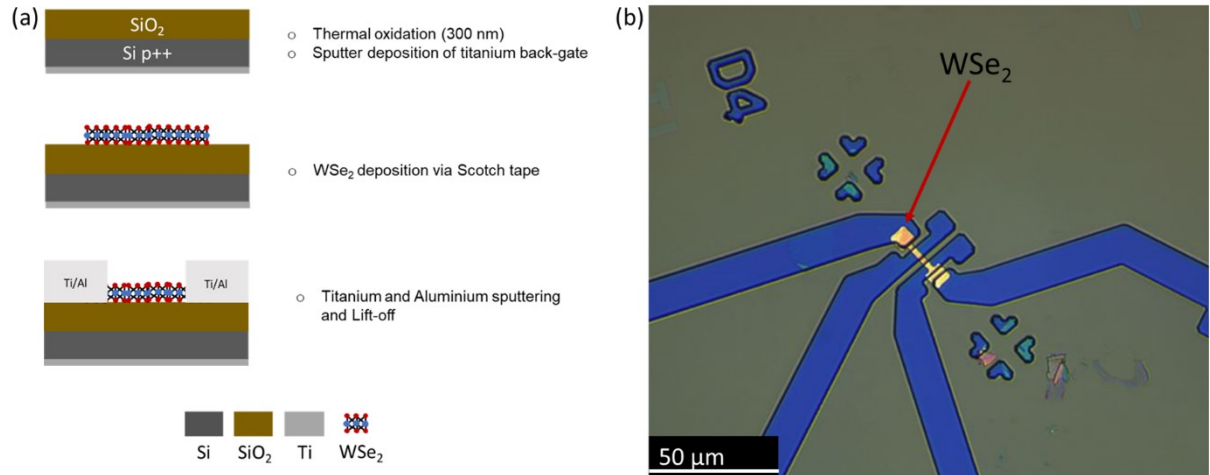
PLD	Number of Laser Pulses	Thickness (nm)
1	500	3 – 4
2	1540	7 - 8
3	2200	10 - 12

The frequency of the laser pulses determine the thickness of the PLD-WSe<sub>2</sub> films. A 10 ( $\pm$  2) nm thickness requires about 2000 – 2200 pulses [126].

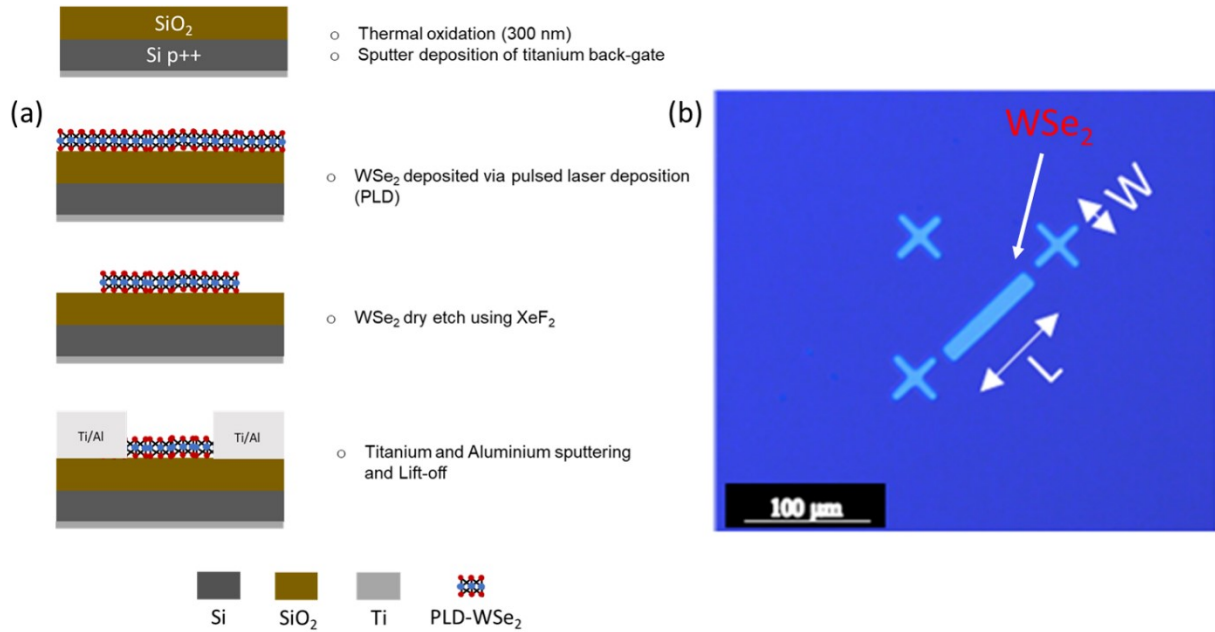
##### 4.2.2 Fabrication of WSe<sub>2</sub> field effect transistor (FET)

Using micro-fabrication techniques as described in Appendix A, the X-WSe<sub>2</sub> FET has been developed as shown in Fig 4.3(a). The substrate which consists of thermally grown SiO<sub>2</sub> on Si has been coated on the back with titanium (to be used as the back-gate). WSe<sub>2</sub> has been exfoliated and deposited onto the SiO<sub>2</sub> surface. Photo-resist has been spin coated on the WSe<sub>2</sub> and with the aid of optical lithography, the photoresist has been patterned as shown in Fig 4.3(b). Titanium and aluminium (Ti/Al) have been sputter deposited onto the WSe<sub>2</sub> and lifted off, thereby forming the drain and source respectively.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>



**Figure 4.3:** Fabrication of X-WSe<sub>2</sub> FET: (a) Schematic outlining the fabrication process (b) Lithographic pattern prior to metal deposition.

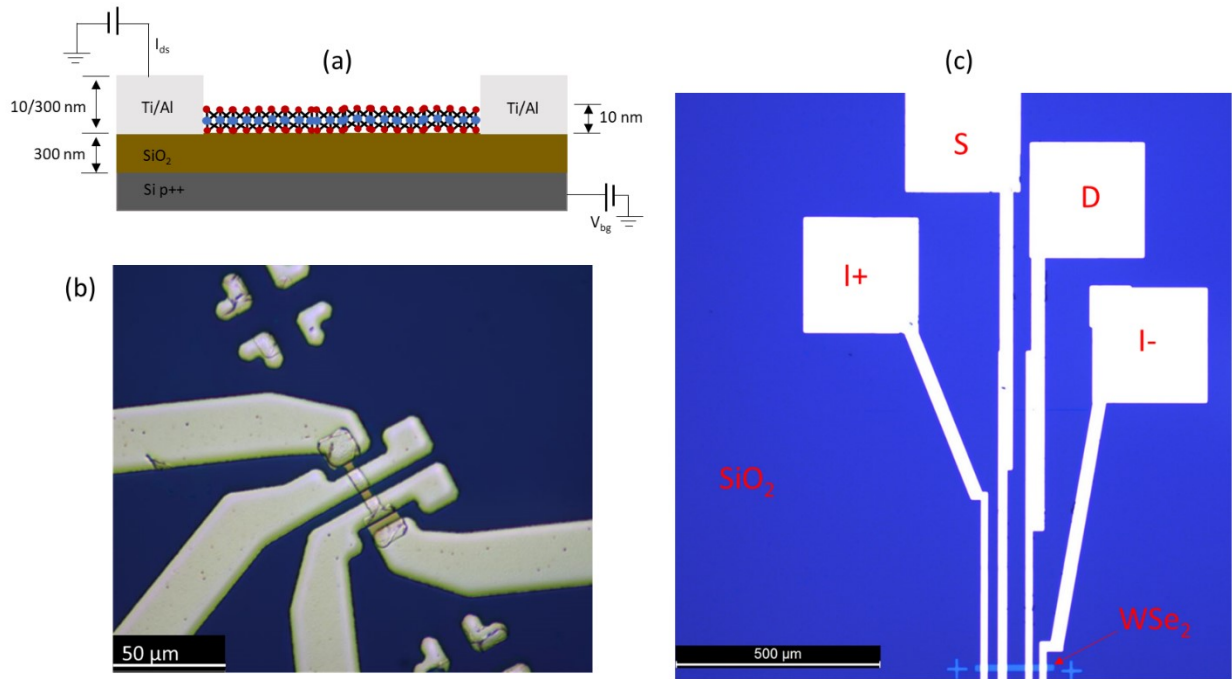


**Figure 4.4:** (a) Schematic outlining the fabrication process of PLD-WSe<sub>2</sub> FET (b) Patterned PLD-WSe<sub>2</sub> channel using vapour XeF<sub>2</sub>.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

The procedure for developing PLD-WSe<sub>2</sub> FET is similar to the X-WSe<sub>2</sub> FET as shown in Fig 4.4(a). The exception is that PLD-WSe<sub>2</sub> is deposited with the aid of an excimer laser via pulse laser deposition. Due to the larger area of the deposited PLD-WSe<sub>2</sub>, the material has been patterned into smaller channels by etching with XeF<sub>2</sub> vapour. The patterned PLD-WSe<sub>2</sub> channel is shown in Fig 4.4(b).

##### 4.2.3 Electrical characterization of X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> FET



**Figure 4.5:** (a) Schematic of the fabricated WSe<sub>2</sub> FET showing geometrical dimensions; Actual device fabricated on SiO<sub>2</sub> / Si substrate: (b) X-WSe<sub>2</sub> FET (c) PLD-WSe<sub>2</sub> FET.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

The electrical properties of the X-WSe<sub>2</sub> and the PLD-WSe<sub>2</sub> transistors fabricated have been characterised. Fig 4.5(a) shows the schematic of the fabricated FET, the material dimensions and also the bias technique. A heavily boron doped silicon substrate has been employed for back-gating the device and a 300 nm SiO<sub>2</sub> dielectric has been deposited on the substrate. The X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> have a channel thickness of 45 ( $\pm$  3) nm and 10 ( $\pm$  2) nm respectively with a Ti/Al contact of 20/300 nm thick. The four Ti/Al electrodes along with the WSe<sub>2</sub> channel of the X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> FET are shown in Fig 4.5(b) and (c) respectively.

The electrical properties of the transistors have been tested using a Keithley 4200-SCS parameter analyser. The field effect behaviour of the X-WSe<sub>2</sub> has been investigated by back-gating the transistor from -30 to +30 V while the PLD-WSe<sub>2</sub> has been back-gated from -130 to +50 V and the transfer characteristics of both devices plotted. From the transfer characteristics, the field effect mobility has been deduced. A transfer length measurement (TLM) has been carried out for the PLD-WSe<sub>2</sub> to further characterise the device.

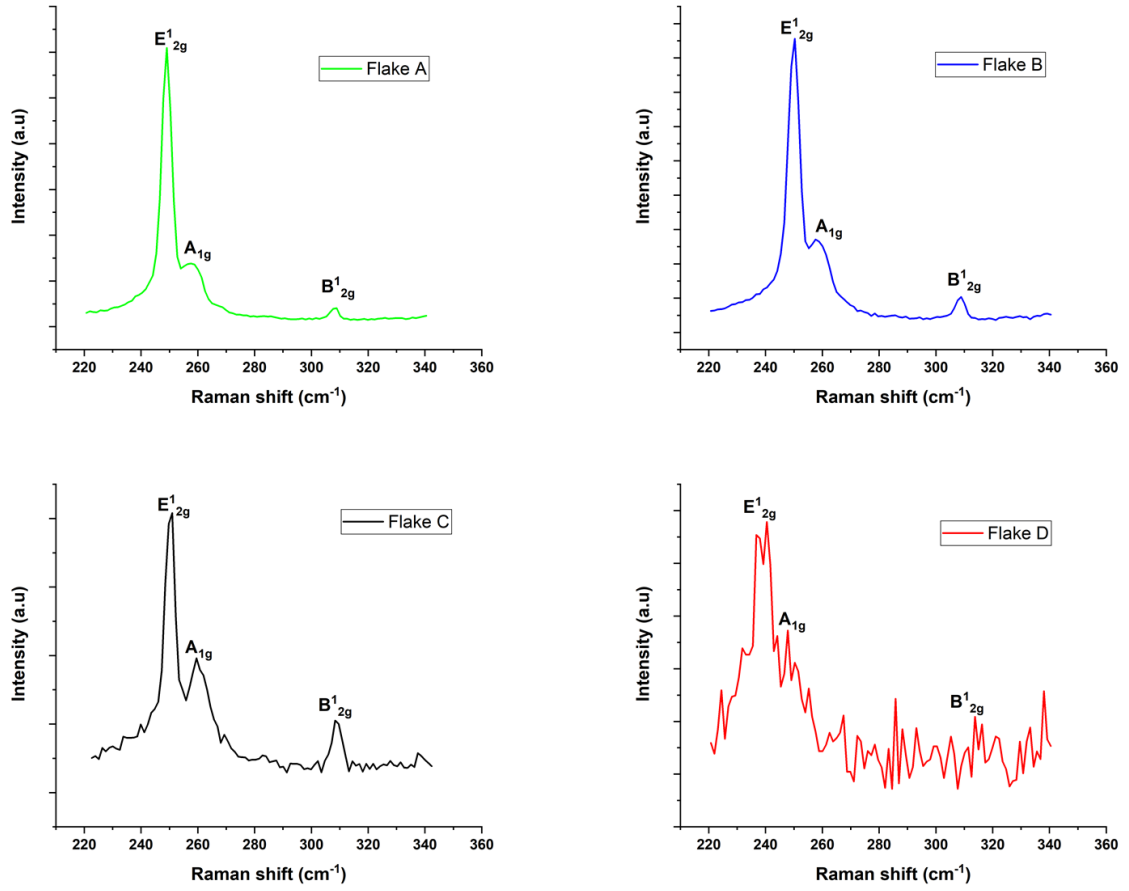
### 4.3 Results and Discussion

#### 4.3.1 Optical Characteristics

Raman and Photoluminescence (PL) spectroscopy have been used to characterise the X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub>. Raman scattering provides information on the crystal quality of the WSe<sub>2</sub> deposited using the Raman modes. The PL spectroscopy on the other hand gives further insight into band-to-band emission arising from excitonic transitions. Both the Raman and PL spectroscopy have been performed at room temperature and atmospheric pressure. To avoid heating or damage to the sample, 5% power of the 3 mW laser has been used for Raman and PL.

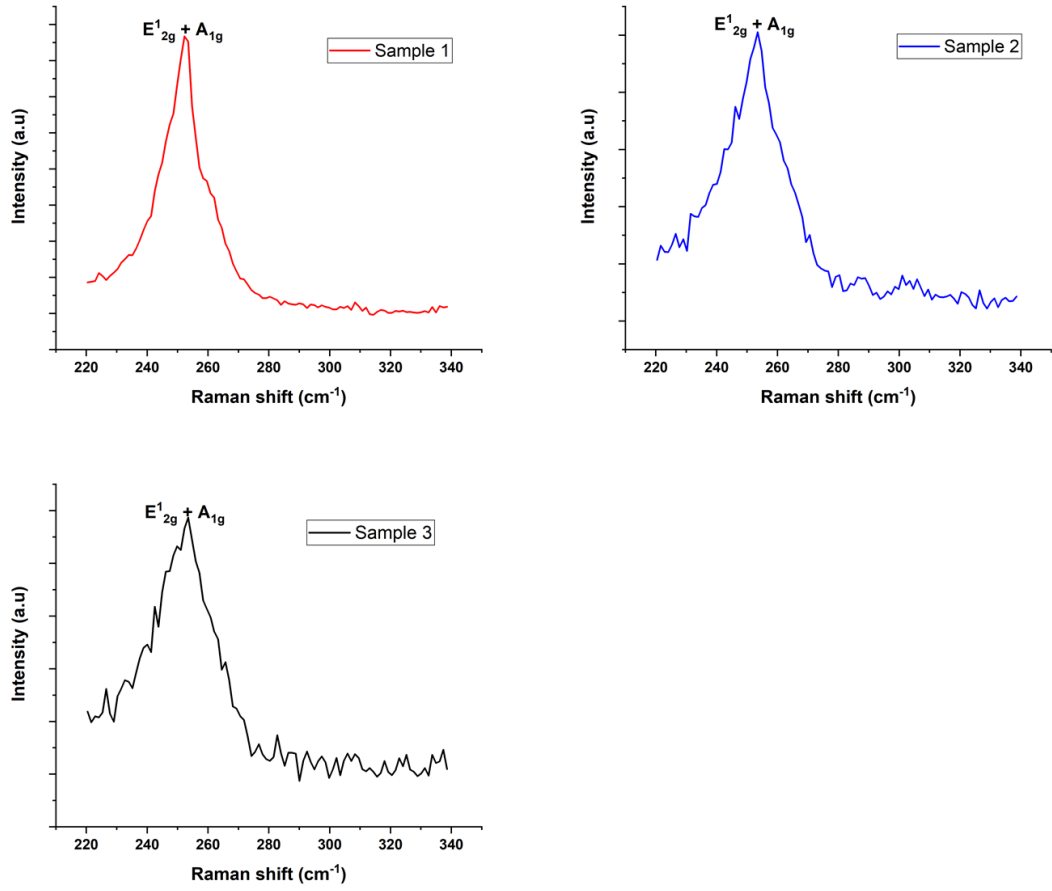
## 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

### 4.3.1.1 Raman spectroscopy

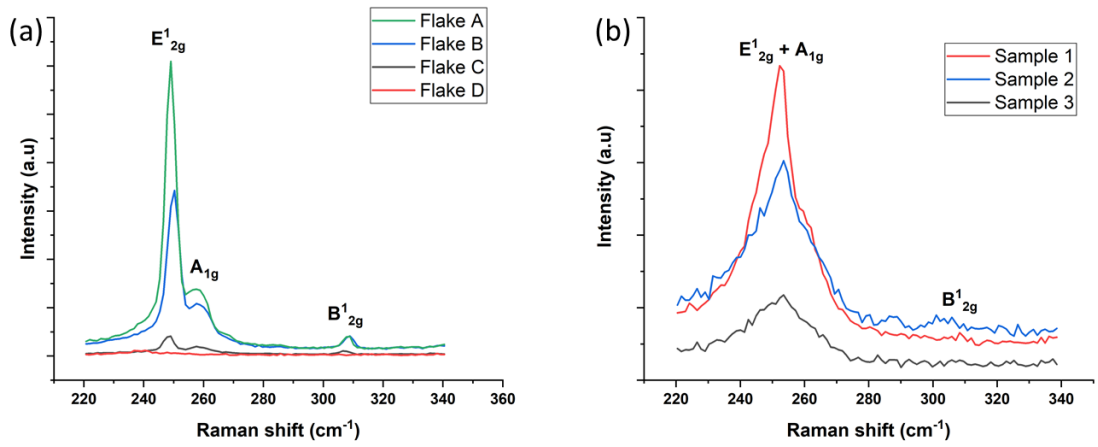


**Figure 4.6:** Raman spectroscopy of singular plots of exfoliated WSe<sub>2</sub> flakes A, B, C and D.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>



**Figure 4.7:** Raman spectroscopy of singular plots of PLD sample 1, 2 and 3.



**Figure 4.8:** Raman Spectroscopy of combined (a) X-WSe<sub>2</sub> (b) PLD-WSe<sub>2</sub>.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

Using a 450 nm laser to excite the WSe<sub>2</sub>, the Raman spectra of the X-WSe<sub>2</sub> and PLD WSe<sub>2</sub> are shown as single plots in Fig 4.6 and 4.7 respectively. The plots are then combined for comparison as shown in Fig 4.8(a) and (b) respectively. Generally, from a Raman spectrum, changes in the structural integrity (surface change or chemical bonding) of a material could be detected [127]. The Raman spectrum is represented by the in-plane ( $E_{2g}^1$ ) mode from the out-of-phase vibration and ( $A_{1g}$ ) mode from the out-of-plane vibrations. From Fig 4.8(a), the Raman peaks ( $E_{2g}^1$  and  $A_{1g}$ ) for X-WSe<sub>2</sub> appear as separate peaks and the positions for the  $E_{2g}^1$  observed for Flake A, B and C is between 249 – 250  $\text{cm}^{-1}$  as has been experienced by Rui [35], and Seung [142] indicating good quality material. Additionally, the intensity of the Raman peak varies with material thickness as Raman spectroscopy is capable of estimating the number of layers in a TMD [80], [129]. Though this comparison has not been researched on this occasion, the plot profiles present some evidence to the statement as the peak intensity decreases from flake A to D.

From Fig 4.8(a), the full width half maximum (FWHM) of the active peaks have been calculated as 5.065 ( $\pm 1$ )  $\text{cm}^{-1}$ , 6.313 ( $\pm 1$ )  $\text{cm}^{-1}$ , 17.153 ( $\pm 2$ )  $\text{cm}^{-1}$  and 18.248 ( $\pm 2$ )  $\text{cm}^{-1}$  for flake A, B, C and D respectively. Values of 3.7 to 4.5  $\text{cm}^{-1}$  for monolayer and 3.8 to 4.6  $\text{cm}^{-1}$  for bilayer have been measured for X-WSe<sub>2</sub> [29] while 4.2 and 5.5  $\text{cm}^{-1}$  have been reported for monolayer CVD WSe<sub>2</sub> [130], [131]. Based on reported values, the FWHM of our samples indicate the flakes are of relatively good quality. The FWHM of X-WSe<sub>2</sub> increases as the number of layers increases as a result of the broadening and diminishing of their peaks. The presence of  $B_{2g}^1$  peak has been reported to be a result of interlayer interaction [3], [132]. Though the  $B_{2g}^1$  peak indicates the presence of multiple layers, few layers of WSe<sub>2</sub> have broader peaks than bulk WSe<sub>2</sub> due to the vibrational damping. This is because as the number of WSe<sub>2</sub> layers increases, the Raman modes are expected to become more rigid resulting in vibrational softening [133]. Table 4.3 below provides a summary of the characteristics of the exfoliated WSe<sub>2</sub> flakes A, B, C and D.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

**Table 4.3:** Properties of the exfoliated WSe<sub>2</sub>

X-WSe <sub>2</sub>	Raman peak position	FWHM (cm <sup>-1</sup> )	Flake thickness (nm)
Flake A	249.06	5.065 ( $\pm 1$ )	5 - 7
Flake B	250.28	6.313 ( $\pm 1$ )	10 - 12
Flake C	251.16	17.153 ( $\pm 2$ )	21 - 24
Flake D	253.46	18.248 ( $\pm 2$ )	46 - 50

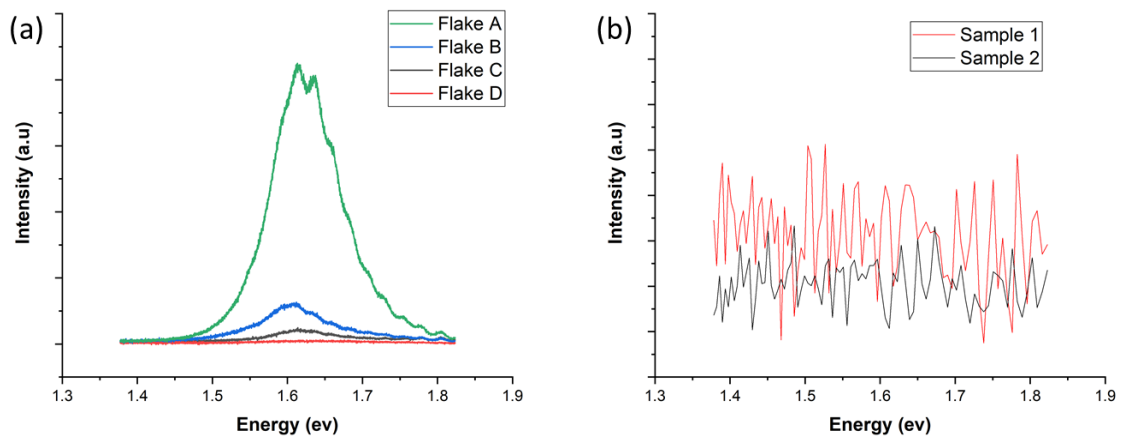
On the other hand, Fig 4.8(b) shows the Raman spectrum of the pulsed laser deposited (PLD) WSe<sub>2</sub>. PLD-WSe<sub>2</sub> is expected to appear about the same region as the X-WSe<sub>2</sub> as has been reported by ref [134], [135]. The active Raman peak for PLD-WSe<sub>2</sub> samples 1, 2 and 3 appear as a single peak within the 252 – 254 Raman shift range. From our samples, (E<sub>2g</sub><sup>1</sup> + A<sub>1g</sub>) peak of PLD WSe<sub>2</sub> appears about the same peak position as X-WSe<sub>2</sub> as shown in Fig 4.8(b). Moreover, the presence of the B<sub>2g</sub><sup>1</sup> peak indicates the sample is not a monolayer. Monolayer PLD WSe<sub>2</sub> has only the primary Raman peaks (E<sub>2g</sub><sup>1</sup> + A<sub>1g</sub>) [134]; same for exfoliated WSe<sub>2</sub> [29]. In addition, the full width half maximum (FWHM) measured for our material is 15 ( $\pm 2$ ) cm<sup>-1</sup>, 20 ( $\pm 2$ ) cm<sup>-1</sup> and 27 ( $\pm 2$ ) cm<sup>-1</sup> for sample 1, 2 and 3 respectively. Values of 12.45 and 14.23 cm<sup>-1</sup> have been reported for monolayer and few (3) layers PLD WSe<sub>2</sub> respectively [134]. The FWHM measured in this experiment shows that both the X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> are of comparatively good quality (composition). Table 4.4 below provides a summary of the characteristics of the PLD WSe<sub>2</sub> sample 1, 2 and 3.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

**Table 4.4:** Properties of the PLD WSe<sub>2</sub> sample 1, 2 and 3

PLD WSe <sub>2</sub>	Raman peak position	FWHM ( $\pm 2$ ) (cm <sup>-1</sup> )	Flake thickness (nm)
Sample 1	252.3	15	3 – 5
Sample 2	253.51	20	7 – 8
Sample 3	253.5	27	10 - 12

##### 4.3.1.2 Photoluminescence spectroscopy



**Figure 4.9:** PL Spectroscopy of (a) X-WSe<sub>2</sub> and (b) PLD-WSe<sub>2</sub>.

Using a 450 nm laser, the samples have been excited and the photoluminescence (PL) spectrum of the X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> is shown in Fig 4.9(a) and (b) respectively. The PL spectrum of the X-WSe<sub>2</sub> in Fig 4.9(a) shows the A-exciton and trion peaks as a single peak between 1.61 – 1.63 eV. The bandgap of the WSe<sub>2</sub> is within the 1.61 – 1.63 eV which corresponds to the position of the A-exciton and trion peak. As the number of layers changes from bulk to fewer layers, the

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

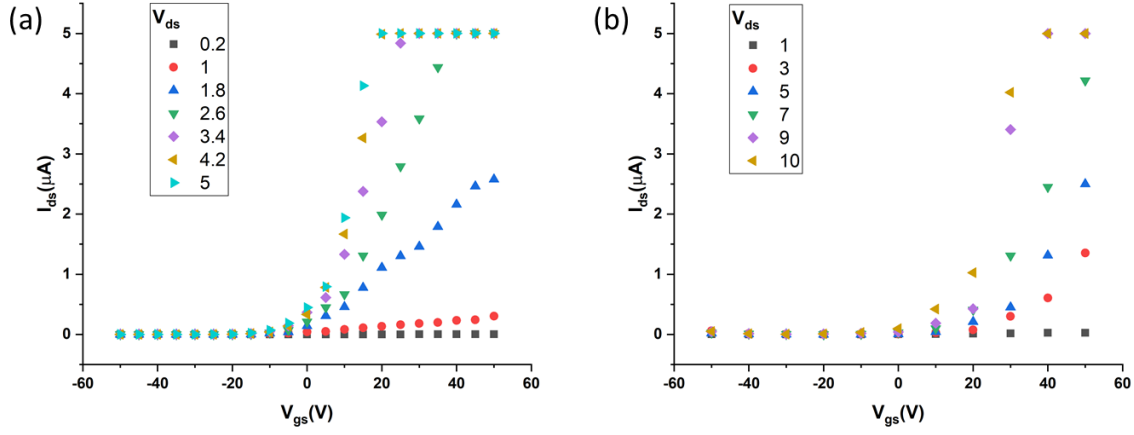
intensity of the PL peak increases significantly. Our result is in corroboration with other PL spectrum of exfoliated WSe<sub>2</sub> [29], [136].

However, from the spectrum shown in Fig 4.9(b), there is no noticeable PL peak at the A-exciton and trion region. The absence of the A-exciton and trion peaks suggests that the PLD WSe<sub>2</sub> has no bandgap. Also, it is possible that there exists non-radiative recombination in the PLD WSe<sub>2</sub> [137]. Grain boundaries can degrade the physical properties of 2D materials by suppressing photoluminescence [138]. The thicker the WSe<sub>2</sub>, the higher the concentration of grain boundaries leading to further quenching of the photoluminescence. The thickness of the PLD WSe<sub>2</sub>; sample 1 and sample 2 is approximately 4 and 7 nm respectively. Generally, monolayer thick (~0.7 nm) semiconducting TMDs are preferred for optoelectronic applications [139] as their band gap increases as well as transforms from indirect into a direct band gap as the TMD's layers decrease [140]. Moreover, due to the PL spectrum of the PLD WSe<sub>2</sub>, a transfer length measurement has been employed to further investigate the bandgap.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

##### 4.3.2 Transfer Characteristics

###### 4.3.2.1 Exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>) FET



**Figure 4.10:** Transfer Characteristics of X-WSe<sub>2</sub> FET with a channel area of 5 by 2  $\mu m$ . (a) Pristine (b) XeF<sub>2</sub> treated.

For the pristine WSe<sub>2</sub> FET shown in Fig 4.10(a), the device has been back-gated from -30 to 30 V. The transfer characteristics indicate an n-type MOSFET as the FET allows continuous flow of current in response to positive voltages. With a  $V_{ds}$  of 5 V, the FET saturates at 20 V while at lower  $V_{ds}$  of 3 V, it saturates at 30 V as considerably more gate voltage is required. Using the green plot ( $V_{ds} = 5$  V), the threshold voltage is approximately -5 V, thus, the transistor appears to be normally on. The on/off ratio of the FET has been calculated to be around 30 – 100, similar values have been found for graphene [141] and WSe<sub>2</sub> [142]. The sub-threshold swing ‘S’ of the FET has been calculated from [143]:

$$S = \frac{\Delta V_{gs}}{\log(\Delta I_{ds})} \quad Eq. (4-1)$$

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

The sub-threshold swing of the FET has been calculated from Eq. (4-1) to be between 6 – 8 V/dec and the field effect mobility  $\mu_{FE}$  has been calculated as 12.06 cm<sup>2</sup>/Vs using Eq. (4-2).

$$\mu_{FE} = \frac{I_{ds}/V_{gs} * L}{WC V_{ds}} \quad Eq. (4-2)$$

The graph in Fig 4.10(b) has been realised from a WSe<sub>2</sub> treated with vapour XeF<sub>2</sub>. The WSe<sub>2</sub> has been etched with the XeF<sub>2</sub> from a thickness of around 48 nm to 26 nm. The WSe<sub>2</sub> FET then developed has been back-gated from -60 to 60 V. The transfer characteristics indicate an n-type MOSFET. With a V<sub>ds</sub> of 10 V, the FET saturates at a gate voltage of 40 V. Using the same plot (V<sub>ds</sub> = 10 V), the threshold voltage is approximately at 0 V, thus, the transistor appears normally off. The on/off ratio of the FET has been calculated to be around 50 – 150, a subthreshold swing between 18 – 40 V/dec and the field effect mobility of 0.72 cm<sup>2</sup>/Vs.

**Table 4.5:** Parameters for X-WSe<sub>2</sub> FET

FET Type	V <sub>ds</sub> (V)	I <sub>ds</sub> (μA)	V <sub>gs</sub> (V)	L (μm)	W (μm)	C <sub>ox</sub> (nF)	μ <sub>FE</sub> (cm <sup>2</sup> /Vs)
Pristine	3	4.99463	30	5	2	11.5	12.06
XeF <sub>2</sub> treated	3	0.299643	30	5	2	11.5	0.72

The parameters used in calculating the field effect mobility for the WSe<sub>2</sub> (pristine and XeF<sub>2</sub> treated) are highlighted in Table 4.5. By using similar values for both FET's, we observe the pristine WSe<sub>2</sub> has a higher field effect mobility. The sub-threshold swing of the pristine WSe<sub>2</sub> is also better than the XeF<sub>2</sub> treated WSe<sub>2</sub>. The performance of the pristine FET is also evident from

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

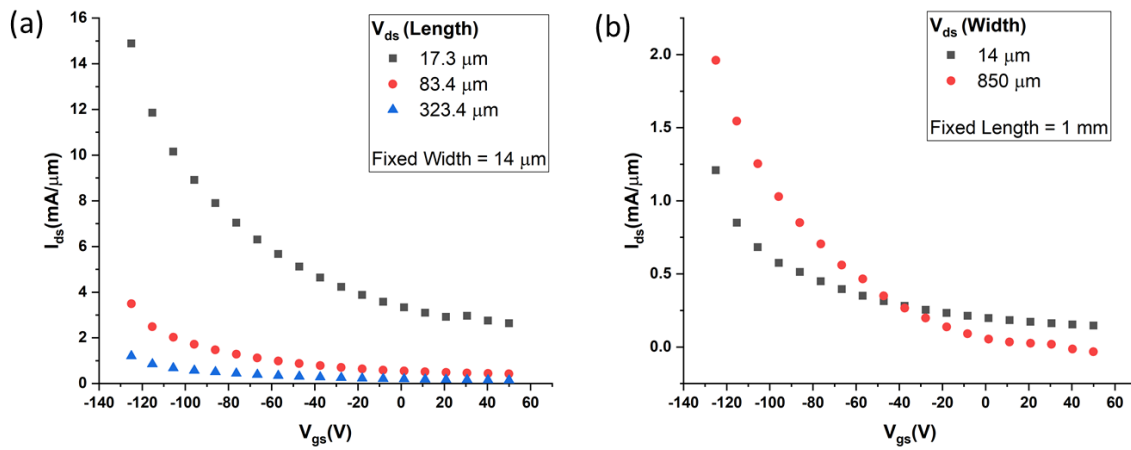
Fig 4.10(a) and (b) where a lower drain-source voltage and gate voltage is required as compared to the XeF<sub>2</sub> etched WSe<sub>2</sub> FET.

According to Akinwande et al. [144], “thinner profile of 2D atomic sheets can result in better device electrostatic control and mechanics while affording mobility similar to bulk semiconductors”. Field effect mobility has been found to be strongly dependent on thickness ‘t’ [145], [146]; however, the relationship between  $\mu_{FE}$  and t for MoS<sub>2</sub> [146] and WSe<sub>2</sub> [147] is non-monotonic. As a result, the 45 nm WSe<sub>2</sub> FET out-performs the 26 nm FET. Additionally, the crystal quality of the X-WSe<sub>2</sub> is altered after etching with XeF<sub>2</sub> which leads to a shift in binding energy [148] as the material is p-doped [29]. This is evident in the shift in threshold voltage of the treated X-WSe<sub>2</sub> to 0 V while the pristine is -5 V. Also, the field effect mobility reduces from 12.06 cm<sup>2</sup>/Vs to 0.72 cm<sup>2</sup>/Vs.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

##### 4.3.2.2 Pulsed Laser Deposited (PLD-WSe<sub>2</sub>) FET

The gated characteristics of the PLD-WSe<sub>2</sub> transistors have been investigated. We have analysed the influence of the transistor channel dimensions (width 14  $\mu\text{m}$ , 850  $\mu\text{m}$  and length 17  $\mu\text{m}$ , 83  $\mu\text{m}$ , 323  $\mu\text{m}$ , 1000  $\mu\text{m}$ ) on the device performance. The drain-source current density has been plotted against the gate voltage as shown in Fig 4.11.



**Figure 4.11:** Transfer characteristics for PLD WSe<sub>2</sub> transistor; (a) for different lengths (17.3, 83.4 and 323.4  $\mu\text{m}$ ) and fixed width (14  $\mu\text{m}$ ); (b) for different widths (14 and 850  $\mu\text{m}$ ) and fixed length (1000  $\mu\text{m}$ ).

The normalised drain-source current against the back-gate voltage for channels with length (17  $\mu\text{m}$ , 83  $\mu\text{m}$  and 323  $\mu\text{m}$ ) and width of 14  $\mu\text{m}$  is presented in Fig 4.11(a). As the back-gated voltage is varied from +50 to over -100V, there has been continuous current flow through the transistor. The transfer characteristics show a p-type behaviour, similar to p-channel depletion type MOSFET [149]. From Fig 4.11(a), it is clear that as the transistor channel length decreases, a higher current density exists. This is likely due to the higher channel resistance which exists as the channel length increases.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

On the other hand, Fig 4.11(b) shows the drain-source current density against the back-gate voltage for the transistor channels with widths of (14  $\mu\text{m}$  and 850  $\mu\text{m}$ ) and length 1000  $\mu\text{m}$ . From the graph, it is clear that as the transistor channel width increases, the drain-source current increases. A larger output current can be seen from the transistor with a channel width of 850  $\mu\text{m}$ . This is believed to be as a result of the transistor having a lower resistance. Additionally, the electric field applied to a larger area could have a significant effect on the transistor transport properties [10]. Chuang et.al [150] reported a drain-source current of about 300  $\mu\text{A}$  at a gate voltage of -130 V for a 7 nm thick and 0.3  $\mu\text{m}$  long transistor. The high drain-source current from their experiment is believed to be as a result of the very short channel and better quality of the exfoliated WSe<sub>2</sub> used. Furthermore, the drain-source current density of the transistors in Fig 4.11(b) shows an exponential rise at a gate voltage greater than -100 V. This observation is believed to be a result of impact ionisation [151] which increases the carrier density of the transistor, leading to a significant increase in the current flow through the PLD WSe<sub>2</sub> FET.

From Fig 4.11(a), the field effect mobility  $\mu_{FE}$  of the transistor can be extracted using Eq. (4-2).

Our calculation shows that the PLD-WSe<sub>2</sub> transistor has a low field effect mobility  $\mu_{FE}$  of  $5.66 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ . where:  $I_{ds} = 7.53 \times 10^{-8} \text{A}$ ,  $V_{gs} = -77.7 \text{V}$ ,  $L = 94 \mu\text{m}$ ,  $W = 14 \mu\text{m}$ ,  $V_{ds} = -10 \text{V}$  and  $C_{ox} = 1.15 \times 10^{-4} \text{F/m}^2$ .

The capacitance of the oxide has been calculated thus:

$$C_{ox} = \frac{\epsilon_0 \epsilon_r}{d} \quad \text{Eq. (4-3)}$$

Where the distance  $d = 300 \text{nm}$  is the silicon oxide thickness which separates the transistor channel from the back-gate. The  $\mu_{FE}$  of  $5.66 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1}$  measured from the 10 nm thick

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

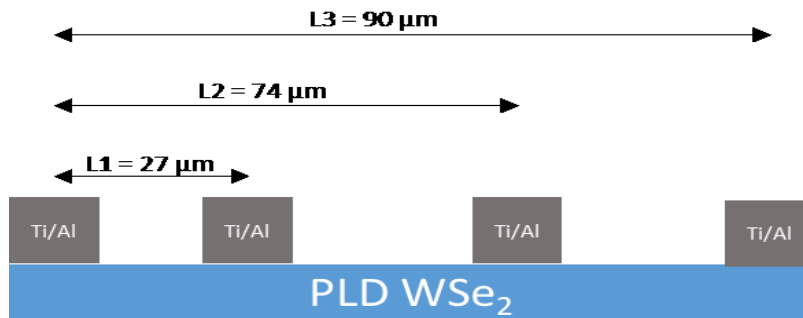
sample is higher than the value ( $5.28 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) obtained by Sehn et.al [134] for their monolayer PLD WSe<sub>2</sub> transistor. The presence of interlayer resistance and interface screening can affect the field effect mobility of 2D WSe<sub>2</sub> [146]. Also, interface roughness scattering present between the 2D material and the substrate could impact on the carrier mobility [152]. Interface roughness effect is more experienced in monolayer transistor channels as these thin channels are more sensitive to the density change of the charge that exists in the substrate [153]. Conversely, thicker channels possess a higher carrier mobility as their layers are further away from the substrate. In addition, thicker channel transistors have relatively more charge density when compared to thinner channels which will serve to screen the effects of scattering between the channel and substrate [151]. However, thicker transistors will have an interlayer resistance that may contribute to scattering. However, Das et al. [146] suggest that interlayer resistance across the transistor layers should not pose serious concern as gating is expected to affect the bottom layers more. Using the equation  $\sigma = ne\mu$  and ( $\sigma = LI_{ds}W^{-1}V_d^{-1}$ ) [154], the carrier density calculated for the PLD WSe<sub>2</sub> transistor is  $4.6 \times 10^{+16} \text{ cm}^{-3}$ . Similar carrier density values have been calculated by Kam et al. [155] for their single crystal WSe<sub>2</sub>. The optimum number of layers in transistor electronics to obtain better device performance in contact resistance and carrier mobility is currently unknown. This is as a result of varied device performance experienced from several studies on 2D materials with different thicknesses [146], [156], [157]. Moreover, an average thickness of 10 nm for WSe<sub>2</sub> [147], MoTe<sub>2</sub> [103] and MoS<sub>2</sub> [98], [105] have been reported to have a higher carrier mobility than fewer layers or bulk samples.

However, from the results of the X-WSe<sub>2</sub> FET and the PLD WSe<sub>2</sub> FET, one can see that the X-WSe<sub>2</sub> outperforms the PLD WSe<sub>2</sub>. The mobility of the pristine X-WSe<sub>2</sub> is over a 100 times larger than the PLD WSe<sub>2</sub>. Additionally, the gate voltage range of the X-WSe<sub>2</sub> is much smaller than the PLD WSe<sub>2</sub> thereby limiting the application of PLD WSe<sub>2</sub> in its current state.

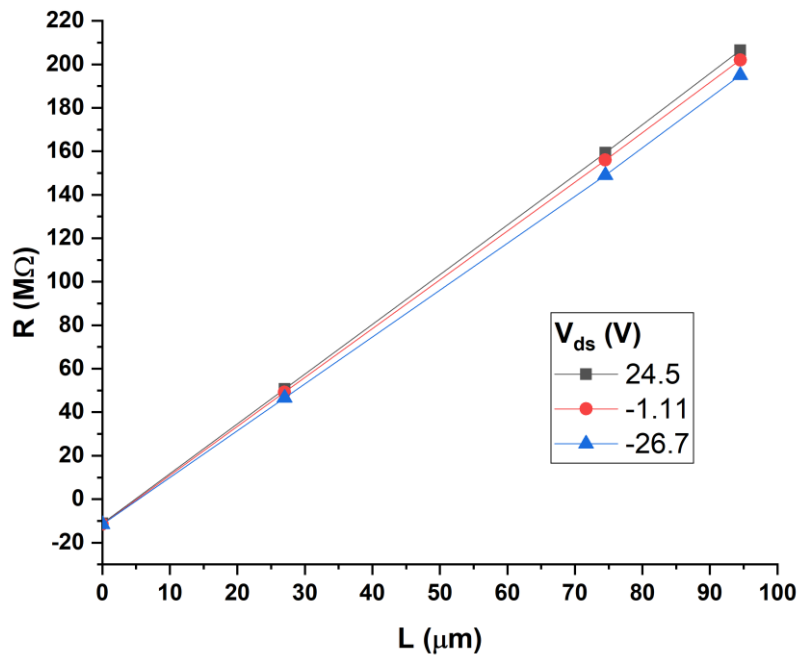
#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

##### 4.3.2.3 Transfer Length Measurement (TLM)

Transfer length measurement (TLM) [158] technique has been employed to further characterise the 14-layer PLD WSe<sub>2</sub> FET as shown in Fig 4.12. The contact resistance  $R_c$  and sheet resistance  $R_{sh}$  of the PLD WSe<sub>2</sub> transistor have been calculated. From the schematic below, the electrode probe spacing is 27  $\mu\text{m}$ , 74  $\mu\text{m}$  and 90  $\mu\text{m}$ .



**Figure 4.12:** TLM electrode spacing.



**Figure 4.13:** Resistance values of the transistors plotted against their electrode spacing at various values of back-gate voltage. The y-intercept indicates a negative contact resistance.

#### 4. Characterization of pulsed laser deposited WSe<sub>2</sub> and exfoliated WSe<sub>2</sub>

The resistance values from the TLM technique have been plotted against the electrode probe spacing at the back-gated voltages of 24.5 V, -1.11 V and -26.7 V as shown in Fig 4.13. From the graph, the contact and sheet resistance have been calculated as 6.11 M $\Omega$ . $\mu$ m and 31.7 M $\Omega$ /□ respectively. A negative contact resistance has been measured for the PLD WSe<sub>2</sub> transistor which indicates a metal-contact doping [159]–[161] and this occurs in materials with Dirac cone systems (no bandgap) [159]. From the PL graph presented in Fig 4.9(b), the absence of a luminescence peak suggests that the PLD WSe<sub>2</sub> has no bandgap. One may then conclude that the negative contact resistance observed from the TLM technique could be due to the absence of bandgap in the PLD WSe<sub>2</sub>.

### 4.4 Conclusions

Similarities and differences between the exfoliated WSe<sub>2</sub> (X-WSe<sub>2</sub>) and the pulse laser deposited WSe<sub>2</sub> (PLD-WSe<sub>2</sub>) have been highlighted. The PLD-WSe<sub>2</sub> and X-WSe<sub>2</sub> have a similar Raman profile in sync with the thickness of the WSe<sub>2</sub>. From a photoluminescence spectrum (PL), while the X-WSe<sub>2</sub> has a PL peak, the PLD-WSe<sub>2</sub> shows no indication of a band gap. Electrically, the X-WSe<sub>2</sub> FET outperforms the PLD-WSe<sub>2</sub> FET due to the higher material quality. The field effect mobility calculated for the X-WSe<sub>2</sub> and PLD-WSe<sub>2</sub> FET is 12.06 cm<sup>2</sup>/Vs and  $5.66 \times 10^{-2}$  cm<sup>2</sup>/Vs respectively. A transfer length measurement further shows that the PLD-WSe<sub>2</sub> possesses no bandgap thus limiting the electrical and optical application of PLD-WSe<sub>2</sub>. Moreover, success was recorded as the PLD WSe<sub>2</sub> FET performed as expected during the variation in the FET length and width. However, the limited performance of the PLD WSe<sub>2</sub> is attributed to the maturity of the PLD technique. The PLD technique is relatively new when compared to other more established deposition techniques like CVD. The PLD technique has merits in terms of material deposition size, lower deposition temperature and ease of the overall process. As a result, the PLD technique has future prospects and is being further developed to perfect the quality of the material deposited. Based on the performance of the X-WSe<sub>2</sub>, it will be integrated with the pyroelectric device in Chapter 6.

# Chapter 5

## **Anodic tantalum: fabrication, breakdown characteristics of capacitor and integration with a WSe<sub>2</sub> field effect transistor**

### **5.1 Introduction**

One of the methods to further improve the performance of the integrated device, is the use of a floating gate. The floating gate creates an additional potential across the integrated device and is typically made from a high- $\kappa$  dielectric. High- $\kappa$  dielectrics allow for an equivalent capacitance to be achieved with physically thicker layers, owing to their high dielectric constant ( $\kappa$ ), thereby showing promise in transistor scaling [162], [163]. High- $\kappa$  dielectrics include titanium dioxide (TiO<sub>2</sub>), zirconium dioxide (ZrO<sub>2</sub>) and tantalum pentoxide (Ta<sub>2</sub>O<sub>5</sub>) among others. A number of techniques have been employed to produce high- $\kappa$  dielectrics such as: pulsed laser deposition (PLD), atomic laser deposition (ALD) and anodization among others [48]. In this chapter, Ta<sub>2</sub>O<sub>5</sub> has been investigated as a possible candidate to be used as a floating gate in future integrated devices. Ta<sub>2</sub>O<sub>5</sub> has been produced via anodization and a capacitor and transistor have been developed from the Ta<sub>2</sub>O<sub>5</sub> dielectric. Anodization of metal into metal-oxides is an established technique in electronics manufacturing and has been mostly used to develop the dielectric of electrolytic capacitors. Anodization produces dense and homogeneous metal oxides of reproducible thicknesses which have a high dielectric constant [108], [158], [159]. These characteristics of anodization along with its relative simplicity and inexpensive process, makes anodic metal oxide an attractive option for the production of high- $\kappa$  dielectric devices. From the anodic Ta<sub>2</sub>O<sub>5</sub> that we produced, capacitors have been fabricated. We have characterised the

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

capacitor's leakage current and breakdown characteristics and also studied their conduction mechanism.

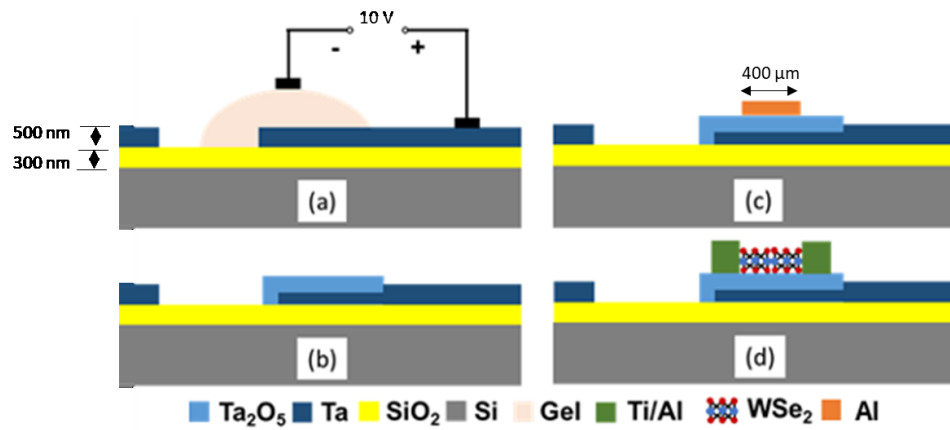
Furthermore, current trends in research have seen the integration of 2D materials such as molybdenum disulfide (MoS<sub>2</sub>) [166] and tungsten diselenide (WSe<sub>2</sub>) [157] with high- $\kappa$  dielectrics. Both Kim [166] and Fang [157] reported improvement in the mobility and power requirement of their field effect transistors after integration with a high- $\kappa$  dielectric. Hence, we have integrated a WSe<sub>2</sub> field effect transistor (FET) with the anodic Ta<sub>2</sub>O<sub>5</sub> and the transfer characteristics of the device have been analysed.

## 5.2 Experimental

### 5.2.1 Anodic tantalum

About 470 nm of tantalum was sputtered on a SiO<sub>2</sub>/Si substrate. After the deposition, the wafer was diced into 2 × 2 cm chips to allow for more experimental samples. To prepare the chips, they were cleaned with isopropyl alcohol (IPA) and then rinsed with deionized (DI) water, before drying them with a nitrogen gun. Details on the process of anodizing tantalum can be found in Section 3.5 of Chapter 3 and the schematic in Fig 5.1 (a) describes the set-up. In summary, an electrolytic gel formed from diethylene glycol (digol), sodium carboxymethyl cellulose and DI water is mixed with citric acid to create an electrolyte. The electrolyte is then dispensed on the selected tantalum area using a pipette and a voltage is applied between the cathode (the electrode in contact with the electrolyte) and the anode (an electrode in contact with the uncoated tantalum surface) for approximately 60 minutes.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



**Figure 5.1:** Cross-sectional schematic of the device fabrication process (a) During anodization; the electrolyte is dispensed on the desired tantalum area and a potential applied between anode and cathode (b) After anodization, a thin layer of Ta<sub>2</sub>O<sub>5</sub> has been grown on top of the remaining bulk tantalum (c) Ta<sub>2</sub>O<sub>5</sub> capacitor (d) WSe<sub>2</sub> FET integrated with the Ta<sub>2</sub>O<sub>5</sub> gate dielectric and with tantalum as the back-gate.

During the anodization of tantalum, every 2 nm of the tantalum metal is converted into 3 nm of tantalum oxide [122]. As we have applied a potential of 10 V on the setup in this experiment, a grown tantalum oxide with an estimated thickness of about 20 nm has been realised [167]. Upon completion of the process, the electrolyte is thoroughly cleaned from the sample using DI water. The grown Ta<sub>2</sub>O<sub>5</sub> layer and the bulk underlying tantalum can be seen in Fig 5.1 (b). This underlying tantalum has been used as the bottom electrode.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

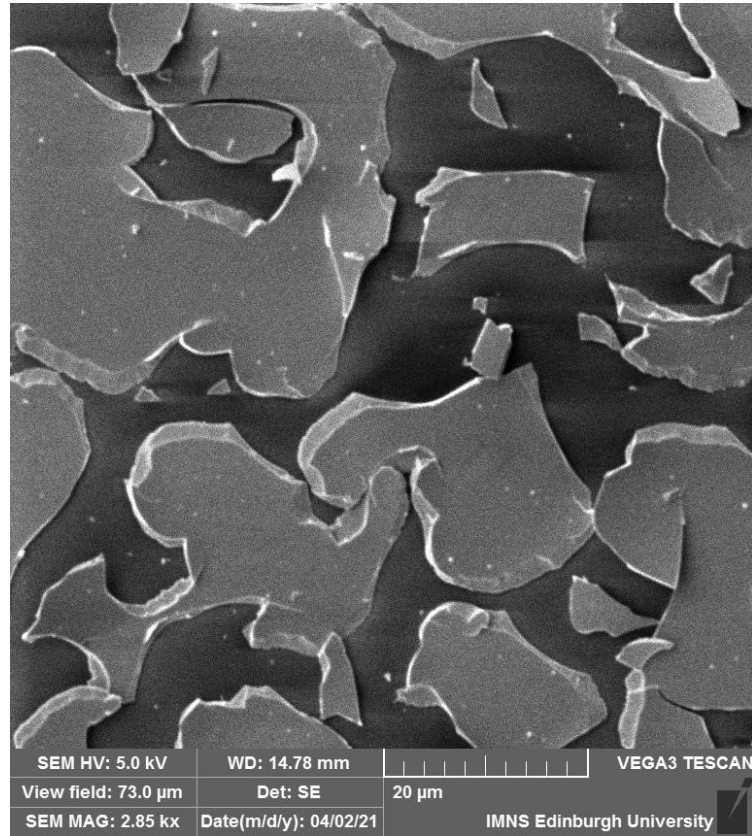
### 5.2.2 Fabrication of Ta<sub>2</sub>O<sub>5</sub> capacitor

Ta<sub>2</sub>O<sub>5</sub> samples have been annealed at 200 °C and 400 °C to study their electrical properties. The anodized samples, both annealed and as-deposited, have been processed further to form a capacitive device as shown in Fig 5.1(c). The process involves spin coating and patterning negative photoresist on the Ta<sub>2</sub>O<sub>5</sub> layer using standard photolithographic techniques. After this step, aluminium is then sputtered and lifted-off to form the capacitive structure. The samples used in this experiment are described in Table 5.1 below:

**Table 5.1:** Anodic tantalum sample characteristics

Sample	Anodizing Voltage (V)	Thickness, d (nm)	Annealing Temp (°C)
As-deposited	10	20	N/A
200 °C	10	20	200
400 °C	10	20	400

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



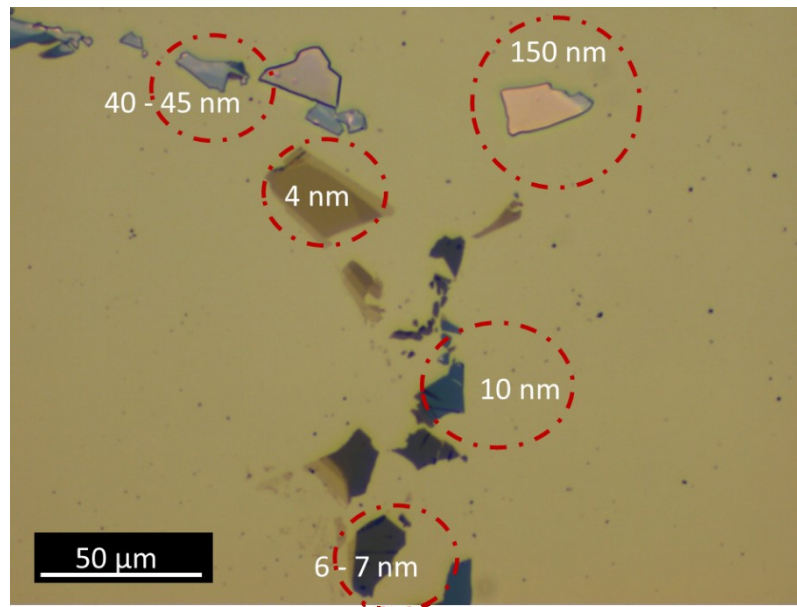
**Figure 5.2:** Degradation of anodic tantalum annealed in nitrogen gas furnace

Prior to annealing the samples in a vacuum chamber, an attempt was made to anneal the samples in a furnace. The furnace uses nitrogen as a carrier gas, for purging among others. After annealing, it was discovered that the material became brittle and disintegrated as shown in Fig 5.2. The degradation of the sample is similar to hydrogen environment embrittlement [168] where the ductility of metals is reduced due to absorbed hydrogen. The rate of degradation has been observed to increase with respect to time and temperature.

### 5.2.3 Fabrication of WSe<sub>2</sub> FET based on Ta<sub>2</sub>O<sub>5</sub>

Using Scotch tape, WSe<sub>2</sub> flakes were exfoliated from the bulk and transferred onto the anodic Ta<sub>2</sub>O<sub>5</sub>. Very good adhesion has been observed between the WSe<sub>2</sub> flakes and the anodic Ta<sub>2</sub>O<sub>5</sub>. We realised a good number of WSe<sub>2</sub> flakes having varied sizes and thicknesses. It has been observed that the colour of the WSe<sub>2</sub> flakes varies with their thickness. This allows for possible estimates of their number of layers as shown within the red-dashed ovals in Fig 5.3. Upon closer examination, the WSe<sub>2</sub> flakes are thickest at their centre and thinner around their edges. On this occasion however, an AFM has been used to confirm the thicknesses of the flakes. In order to develop a WSe<sub>2</sub> FET based on anodic tantalum, photoresist has been spin coated on the WSe<sub>2</sub> flake and the photoresist has been patterned using maskless lithography tool. Titanium/aluminium electrodes have been deposited and lifted off, forming the source and drain of the WSe<sub>2</sub> FET whilst the underlying Ta serves as the back-gate electrode of the FET as shown in Fig 5.1(d). The fabrication schematic is similar to Fig 4.3 in Section 4.2.2 of Chapter 4.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

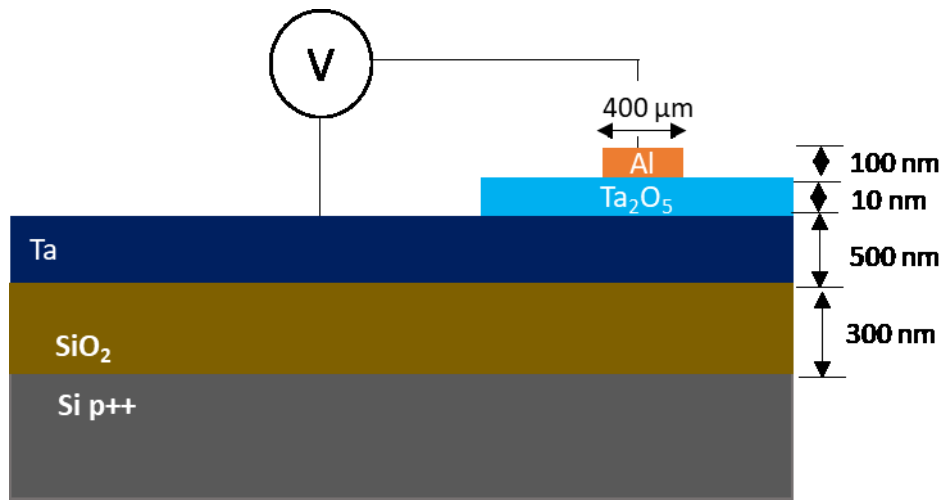


**Figure 5.3:** WSe<sub>2</sub> flakes on anodic tantalum showing a relationship between the flake colour and their thickness

### 5.3 Results and Discussion

In this section, test results from the capacitor and field effect transistor fabricated from the anodic tantalum are presented. The devices have been tested using a Keithley 4200-SCS parameter analyser connected to a shielded “TST-017 Everbeing EB-8” probe station.

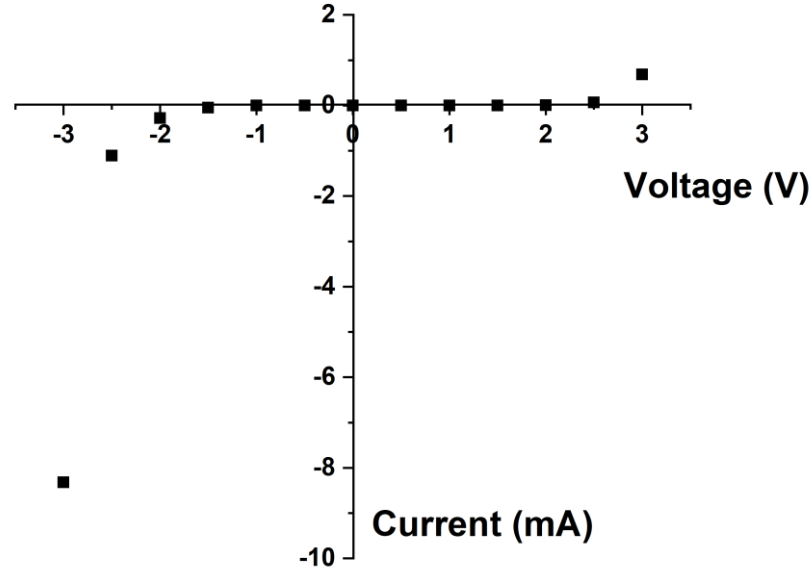
#### 5.3.1 Anodic tantalum (Ta<sub>2</sub>O<sub>5</sub>) capacitor



**Figure 5.4:** Schematic of anodic tantalum capacitor test set-up

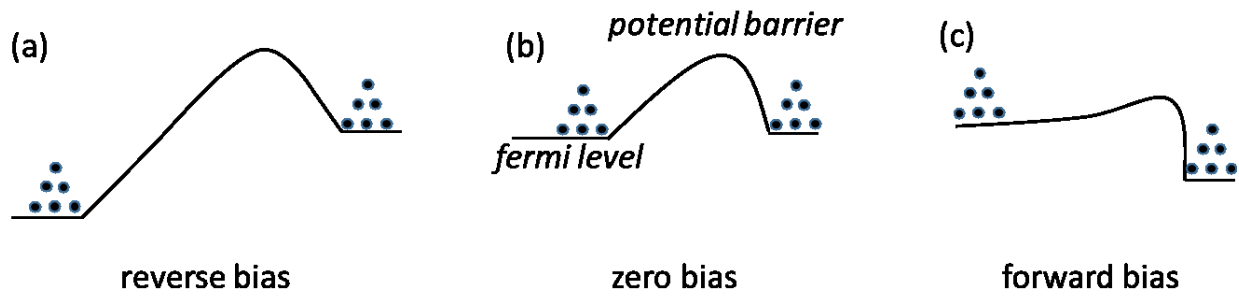
Fig 5.4 shows the anodic tantalum schematic. Details of the device fabricated are presented in Appendix B. From the set-up in Fig 5.4, the current-voltage (I-V) and capacitor-voltage (CV) curves of the Ta<sub>2</sub>O<sub>5</sub> capacitor have been realised. The anodic tantalum dielectric is sandwiched between an aluminium top electrode and a tantalum bottom electrode. The device has been fabricated and characterised to obtain the dielectric properties of the anodic tantalum and determine the suitability of anodic tantalum as a floating gate in future experiments.

### 5.3.1.1 Current voltage (I-V) asymmetry for the Ta<sub>2</sub>O<sub>5</sub> capacitor



**Figure 5.5:** I-V asymmetry observed in anodic tantalum

The I-V plot in Fig 5.5 shows asymmetry in the anodic tantalum. From the distribution of the data points, there is a disproportionate change in the current output when the device is forward and reverse biased beyond 3 V. The result suggests that the device has a rectifying contact. At -3 V, a disproportionate current is measured indicating dielectric breakdown. Asymmetry in Ta<sub>2</sub>O<sub>5</sub> is not an isolated incident as it has been observed by others [164], [169], [170]. The potential barrier of the metal-Ta<sub>2</sub>O<sub>5</sub> contact varies based on the bias condition. As shown in Fig 5.6, in reverse bias, the potential barrier rises limiting the flow of charges. Likewise, when the device is forward biased, the barrier lowers and charges flow more easily.

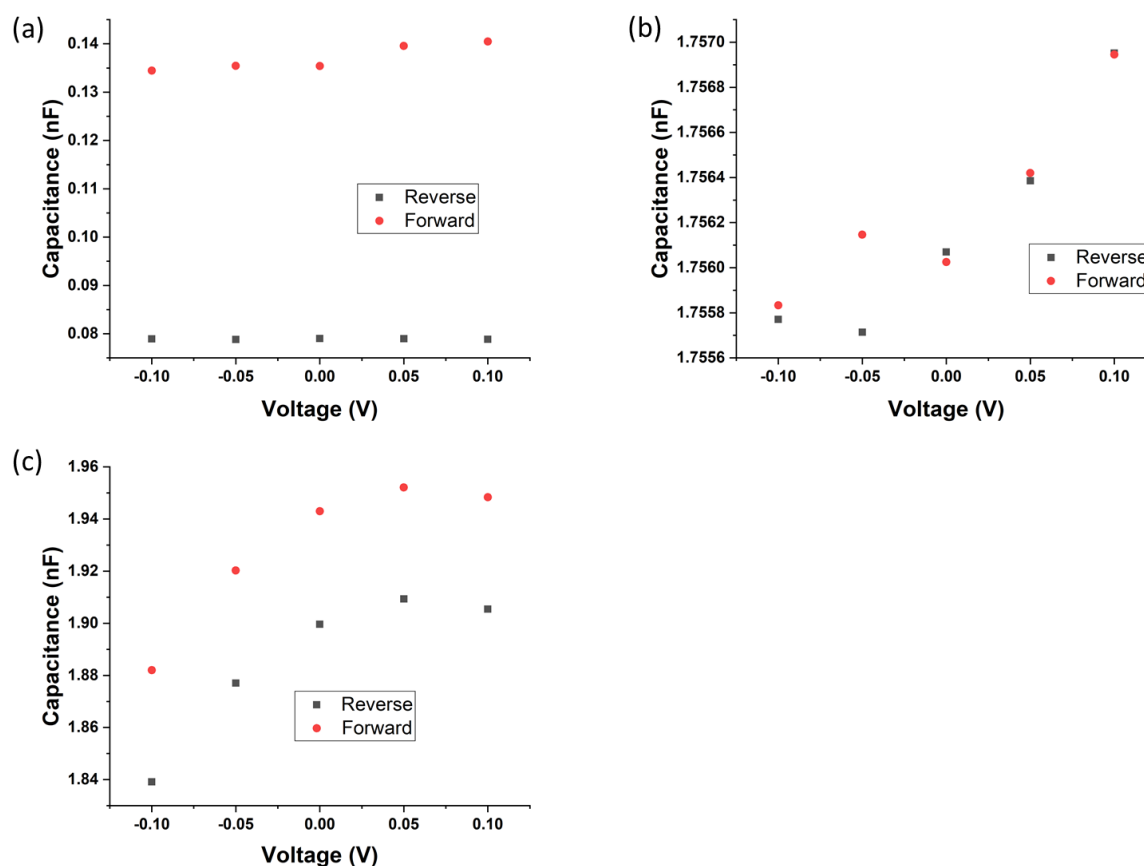


**Figure 5.6:** Schematic of the schottky barrier in a rectifying contact [171] (a) the reverse bias raises the barrier height and limits charge flow (b) zero bias has no effect on barrier height (c) forward bias lowers the barrier height and allows charges flow easily

### 5.3.1.2 Capacitor-voltage (CV) hysteresis

Hysteresis in the anodic tantalum capacitor has been investigated with the as-deposited and annealed samples. Hysteresis occurs due to the build-up of positive and negative charges near the metal-insulator interface, causing a distortion in the potential distribution. When the applied field is then removed, large internal fields remain that prevent some charges from flowing back toward their equilibrium position [172]. These trapped charges result in hysteresis and annealing eliminates interface traps [171]. The anodic tantalum capacitors have varied CV hysteresis as shown in Fig 5.7.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



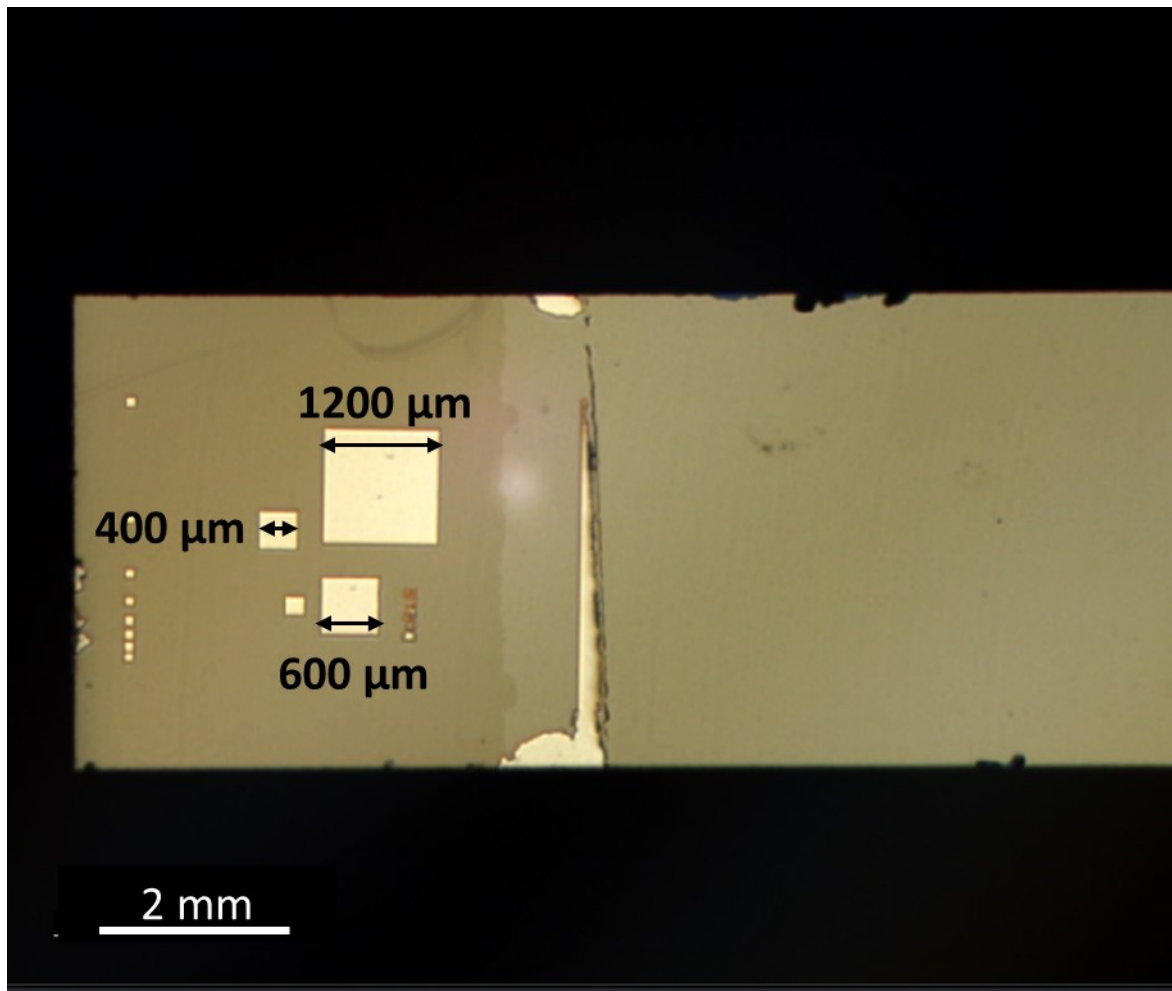
**Figure 5.7:** Hysteresis graphs of anodic tantalum capacitors measured by interchanging test probe position on sample: (a) As-deposited (b) 200 °C annealed (c) 400 °C annealed.

The capacitance tests have been performed using a Keithley 4200-SCS parameter analyser at room temperature. The capacitors have been gated between  $-0.1$  V to  $0.1$  V in steps of  $0.05$  V. The sweep has been confined to  $0.1$  V to achieve the best results and avoid any damage to the dielectric. The CV hysteresis responses were recorded from sweeps in the forward bias mode and after a fixed duration, in the reverse bias direction (by switching the test probes). The hysteresis observed in the as-deposited sample in Fig 5.70(a) is considerably larger than in the annealed samples. The sample annealed at  $200$  °C has been performed in an oxygen rich chamber with a pressure of about  $7.5$  Torr while for the sample annealed at  $400$  °C, it had a base pressure of about  $5$  mTorr. We

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

believe the annealing aided in eliminating some charge traps in the dielectric leading to the better performance of the annealed samples. The result from Fig 5.7(b) and (c) show considerable uniformity in the recorded capacitance values.

### 5.3.1.3 Capacitor-voltage (CV) electrode area test for calculating dielectric constant ( $\kappa$ )



**Figure 5.8:** Anodic tantalum capacitor consisting of various electrode area

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

A few electrodes have been fabricated on the anodic tantalum as shown in Fig 5.8. The sizes of the electrodes are as follows: 400, 600 and 1200  $\mu\text{m}$ . The capacitance and dielectric constant of the as deposited devices have been tested and the results are presented in Table 5.2.

**Table 5.2:** Capacitance of anodic tantalum for the as-deposited sample

S/N	Area, A ( $\mu\text{m}^2$ )	Capacitance, (nF)	Dielectric constant ( $\kappa$ )
1	$1.6 \times 10^5$	2.58	18.24
2	$3.6 \times 10^5$	5.95	18.65
3	$14.4 \times 10^5$	24.78	19.43

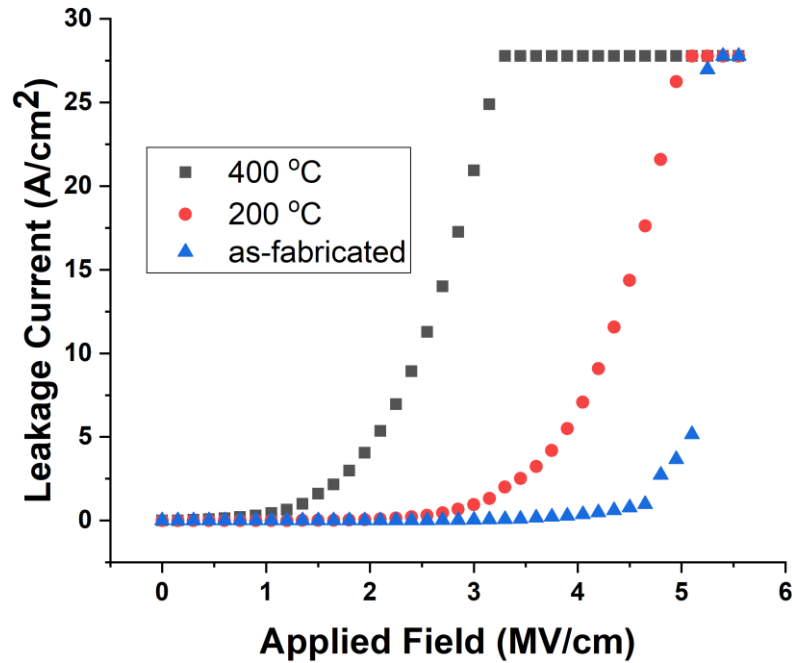
In Table 5.2, the area, capacitance and dielectric constant of the devices are presented. The capacitance increases with area as expected from Eq. (5-1). Using Eq. (5-1), the dielectric constant  $\epsilon$  has been calculated and the mean value is  $18.7 (\pm 6)$ . The dielectric constant of Ta<sub>2</sub>O<sub>5</sub> varies from 10 – 52 based on the deposition method [164]. In the case of anodic tantalum, values of 18 and 27 have been recorded [173]. However, values of 12 and 13 have been calculated for the 200 °C and 400 °C annealed samples respectively.

$$C = \frac{\epsilon A}{d} \quad \text{Eq. (5-1)}$$

### 5.3.2 Conduction mechanism

The breakdown characteristics for a 20 nm thick and 600 sq.  $\mu\text{m}$  Ta<sub>2</sub>O<sub>5</sub> capacitor is presented in Fig 5.9. Three Ta<sub>2</sub>O<sub>5</sub> capacitor samples have been experimented on and while one remained as-deposited, the other two have been annealed at 200 °C and 400 °C. From the graph below, the breakdown field of the as-deposited, 200 °C and 400 °C samples are 5.4, 5.1 and 3.3 MV/cm respectively. The breakdown field of the as-deposited sample is similar to the anodizing voltage. However, the thickness and breakdown voltage of anodic metals depend on the anodizing voltage, concentration of the electrolyte and any other treatment applied to the material [174]. In this experiment, the as-deposited anodic tantalum breaks down around 10 V [4.8 to 5 (MV/cm)]. At an electric field of 1.5 MV/cm, the leakage current extracted for the as-deposited, 200 °C and 400 °C annealed anodic tantalum is  $10^{-5}$ ,  $10^{-2}$  and 1 A/cm<sup>2</sup> respectively. We observed that the as-deposited Ta<sub>2</sub>O<sub>5</sub> has the lowest leakage current and highest breakdown potential while the Ta<sub>2</sub>O<sub>5</sub> annealed at 400 °C possessed the highest leakage current and lowest breakdown potential. What this implies is that the breakdown potential and leakage current is correlated with the annealing temperature. Mohammed and Morgan [175] suggested that the formation of a depletion layer at the Al/Ta<sub>2</sub>O<sub>5</sub> or the Ta<sub>2</sub>O<sub>5</sub>/Ta interface is the origin of current-voltage variation with annealing temperature. This variation in the current-voltage characteristics for samples annealed at different temperatures is presumed to be the result of different energy barriers between the metal-dielectric interfaces, similar to a metal-semiconductor Schottky barrier [172] as shown in Fig 5.6 above.

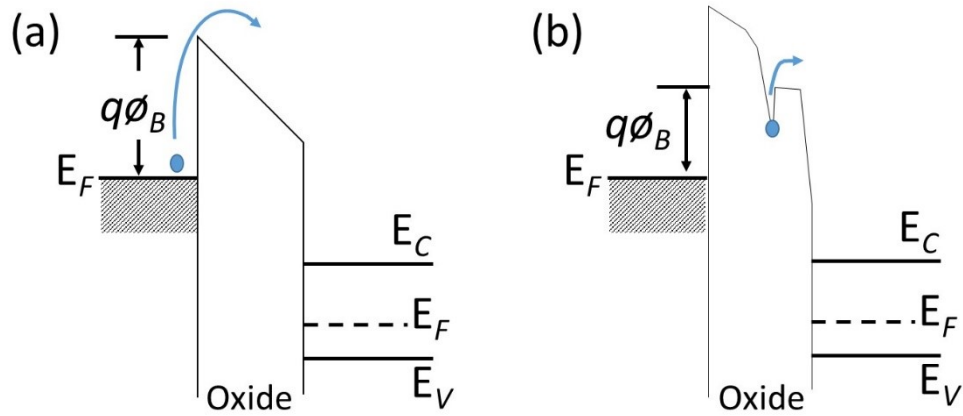
## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



**Figure 5.9:** Breakdown characteristics of 20 nm thick and 600 square  $\mu\text{m}$   $\text{Ta}_2\text{O}_5$  capacitors annealed at different temperature. The breakdown potential and leakage current varies with their annealing temperature.

Conduction mechanisms in dielectrics include Schottky emission (SE) and Poole-Frenkel emission (PF) among others. However, multiple conduction mechanisms may exist in a dielectric [176]. A number of factors affect the conduction mechanism of dielectric films such as: electrode material, electric field, film thickness, temperature, deposition method, imperfections among others [177]. Imperfection implies foreign or impurity atoms, excess or absent atoms, dislocations, mosaic structure and defects [178].

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



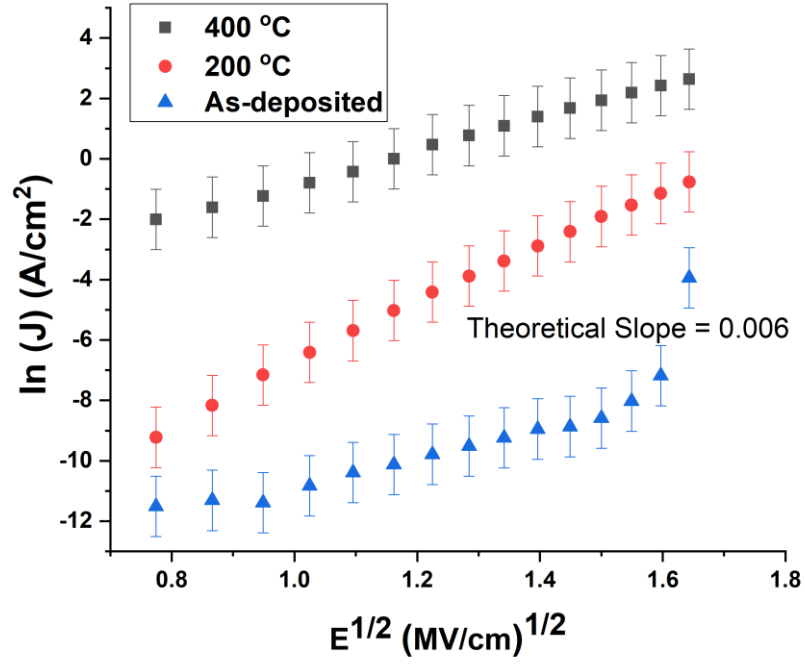
**Figure 5.10:** Energy-band diagram showing conduction mechanism of (a) Schottky emission and (b) Poole-Frenkel emission.

Schottky emission (SE) occurs in devices when electrons possess enough energy to overcome the metal-insulator barrier as shown in Fig 5.10(a). The thermionic emission current (Schottky emission) is proportional to the electron density with energies above the barrier height that is  $q\phi$  for a metal-insulator interface. Therefore, for the anodic tantalum, the current is proportional to  $\exp \frac{q\phi}{kT}$  and the current increases exponentially with decreasing barrier height and increasing temperature [172].

Poole-Frenkel (PF) emission shown in Fig 5.10(b) occurs when trapped electrons are emitted into the conduction band through thermal excitation. While the PF emission is similar to SE, the barrier height for PF is the depth of the trap potential well [172].

The conduction mechanism in the Ta<sub>2</sub>O<sub>5</sub> capacitor has been studied and the graphs are presented below.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



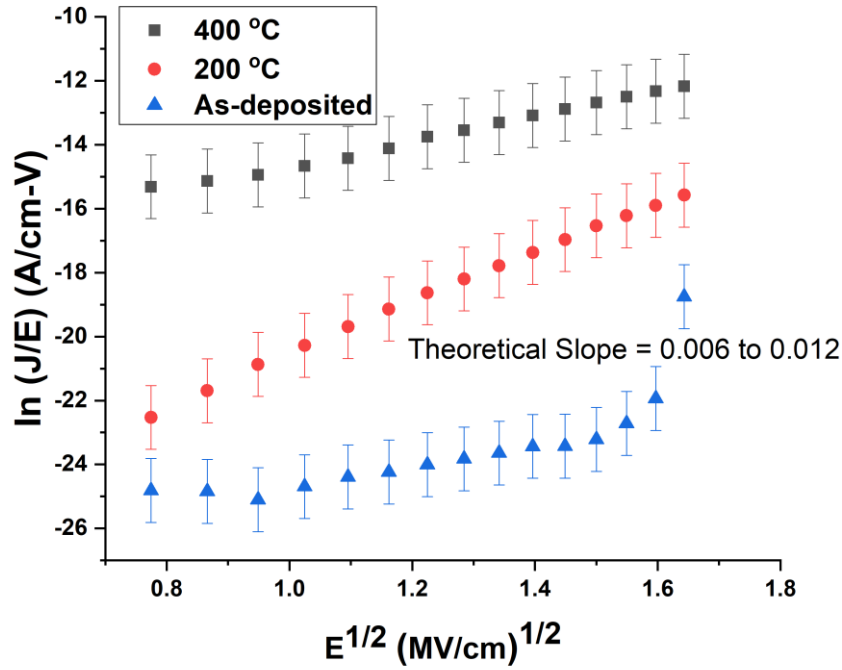
**Figure 5.11:** Schottky plot of the as-deposited and annealed Ta<sub>2</sub>O<sub>5</sub> capacitors.

The Schottky-Richardson equation describes the current density due to SE [176], [179]:

$$\ln(J) = \frac{\beta}{2kT} \sqrt{E} + \ln(AT^2) - \frac{q\phi}{kT} \quad Eq. (5-2)$$

Where  $J$  is the current density,  $T$  the temperature,  $\beta$  is the barrier lowering,  $k$  is Boltzmann's constant,  $A$  is the Richardson constant,  $q$  electron charge, and  $\phi$  is the barrier height.

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET



**Figure 5.12:** Poole-Frenkel plot for the as-deposited and annealed Ta<sub>2</sub>O<sub>5</sub> capacitors.

Eq. 5-3 describes the current density of PF emission:

$$\ln\left(\frac{J}{E}\right) = \frac{\beta}{\xi kT} \sqrt{E} + \ln(C) - \frac{q\phi}{\xi kT} \quad Eq. (5-3)$$

Where  $C$  is a constant and  $\xi$  is dependent on the material property and can vary between 1 and 2 [176], [179].

The Schottky emission (SE) and Poole-Frenkel (PF) plots shown in Fig 5.11 and 5.12 respectively are from the data in Fig 5.9. Both graphs (SE and PF) show that all the samples have good linear fits. Based on the linear fits, SE and PF conduction mechanisms are evident. Table 5.3 shows the experimental and theoretical slopes of the Ta<sub>2</sub>O<sub>5</sub> capacitors. The experimental slopes have been

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

extracted from the best fits in the SE and PF graphs in Fig 5.11 and 5.12 respectively. On the other hand, the theoretical slopes have been calculated from equation  $\frac{\beta}{2kT}$ , described by ref [180].

**Table 5.3:** Experimental and theoretical slopes of the SE and PF conduction mechanism

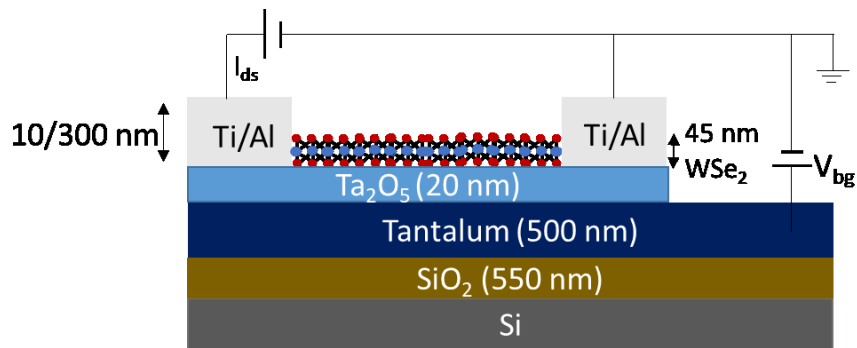
Ta <sub>2</sub> O <sub>5</sub> Capacitor	Theoretical Slope ( $\pm 0.001$ )		Experimental Slope ( $\pm 0.001$ )	
	SE	PF	SE	PF
	(A/(cm <sup>3</sup> .V) <sup>1/2</sup> )	(A.V <sup>1/2</sup> /(cm <sup>3/2</sup> ))	(A/(cm <sup>3</sup> .V) <sup>1/2</sup> )	(A.V <sup>1/2</sup> /cm <sup>3/2</sup> )
As-deposited	0.006	0.006 - 0.012	0.006	0.003
200 °C			0.011	0.009
400 °C			0.006	0.003

From the data in Table 5.3, the experimental slopes of the as-deposited and 400 °C annealed sample are within the same margin of error. Upon further comparison of the experimental and theoretical slope values of these two samples, it appears that the experimental PF slope is outside the margin of error of the theoretical PF slope. Hence, the dominant conduction mechanism in the two samples is SE. Taking a look at the theoretical and experimental slopes of the 200 °C annealed sample, it appears that the dominant conduction mechanism is PF. However, the sample annealed at 200 °C has been performed with a chamber pressure of about 7.5 Torr while for the sample annealed at 400 °C, it had a base pressure of about 5 mTorr. Therefore, PF conduction mechanism observed in the capacitor annealed at 200 °C is deduced to be due to the presence of oxygen in the chamber which resulted in the possible formation of Ta<sub>2</sub>O<sub>5</sub> at the interface between the anodic Ta<sub>2</sub>O<sub>5</sub> and the bulk tantalum. These additional bonding may have contributed to an increase in the

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

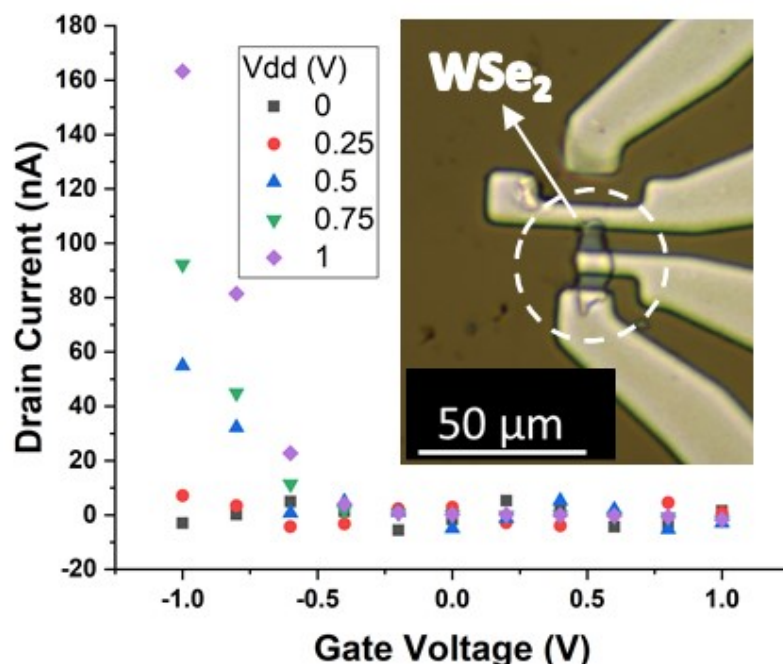
overall traps present within the sample. Meanwhile, a change in conduction mechanism from PF to SE has been experienced by Kerrec et al. [181] in their sputtered Ta<sub>2</sub>O<sub>5</sub> after the bulk traps were annealed.

### 5.3.3 WSe<sub>2</sub> FET based on anodic tantalum



**Figure 5.13:** Schematic of WSe<sub>2</sub> FET on anodic tantalum

From the set-up in Fig 5.13, the transfer characteristics of the WSe<sub>2</sub> FET based on anodic tantalum have been realised. The anodic tantalum served as the gate dielectric and the bulk tantalum as back-gate electrode. The transfer characteristics are shown in Fig 5.14.



**Figure 5.14:** Transfer Characteristics of WSe<sub>2</sub> FET based on Ta<sub>2</sub>O<sub>5</sub> dielectric. The device fabricated is shown in the in-set figure; WSe<sub>2</sub> FET with its electrodes on a Ta<sub>2</sub>O<sub>5</sub> substrate.

From Fig 5.14, the device has been back-gated from -1 to 1 V in steps of 0.2 V. A drain-source voltage ( $V_{ds}$ ) of 0 to 1 V has been applied in steps of 0.25 V. From the graph, at a drain-source voltage value of less than 0.5 V, the drain-source current ( $I_{ds}$ ) appears significantly low. However, a considerable  $I_{ds}$  value of over 150 nA has been realised with a gate voltage of -1 V. With a Ta<sub>2</sub>O<sub>5</sub> thickness of about 20 nm, the FET shows good control from the gate voltage. The transistor threshold voltage extracted is approximately -0.5 V, thus, showing promise in low power operation which is common for high- $\kappa$  FETs [142], [182]. The field effect mobility of the WSe<sub>2</sub> FET on anodic Ta<sub>2</sub>O<sub>5</sub> has been calculated to be about  $0.9 \text{ cm}^2 \text{ V}^{-1} \text{ S}^{-1}$  using Eq. (4-2). From the gate sweep, the WSe<sub>2</sub> FET based Ta<sub>2</sub>O<sub>5</sub> shown in Fig 5.14 exhibits p-type MOSFET behaviour as the device responds more to the negative potential. However, according to ref [183], the interface between the titanium/aluminium contacts and the Ta<sub>2</sub>O<sub>5</sub> is oxygen rich thereby creating a p-type

## 5. Anodic tantalum: capacitor characteristics and integration with WSe<sub>2</sub> FET

layer. In contrast, the interface between the Ta<sub>2</sub>O<sub>5</sub> and the bulk tantalum is oxygen deficient, hence, an n-type layer is present. We believe this existing p and n-type layer in anodic metals may have an influence in the FET behaviour above and capacitor operation in Fig 5.7.

## 5.4 Conclusions

In this chapter, studies conducted on a capacitor fabricated from anodic Ta<sub>2</sub>O<sub>5</sub> and a field effect transistor (FET) fabricated from anodic Ta<sub>2</sub>O<sub>5</sub> and WSe<sub>2</sub> have been presented. The method of producing anodic Ta<sub>2</sub>O<sub>5</sub> via anodization has been discussed as a simple and in-expensive technique. The experimental results from the capacitor and FET have been presented and analysed.

Our findings reveal that the Ta<sub>2</sub>O<sub>5</sub> capacitor has a rectifying contact showing both I-V asymmetry and CV hysteresis. The CV hysteresis highlights the disproportionate distribution of oxygen within the anodic tantalum. However, the effect of the oxygen distribution was better contained in the annealed samples. On the other hand, as the annealing temperature of the samples increased, the breakdown field decreased while the leakage current increased. Whilst Schottky emission (SE) appeared dominant in the samples, Poole Frenkel (PF) emission has been observed when a sample was annealed at 200 °C in higher pressure.

Furthermore, WSe<sub>2</sub> has been transferred onto the anodic Ta<sub>2</sub>O<sub>5</sub> via exfoliation, having good adhesion and producing quality WSe<sub>2</sub> flakes. The Ta<sub>2</sub>O<sub>5</sub> dielectric has been integrated with a WSe<sub>2</sub> FET, showing good gate control of the device. The low threshold voltage of the FET shows promise in low power operations. In addition, the FET exhibits P-type MOSFET behaviour with a field effect mobility of 0.9 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>.

# Chapter 6

## Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

### 6.1 Introduction

The aim of this project, to integrate a WSe<sub>2</sub> FET with Pyreos's pyroelectric device has been met from the works in this chapter. Experimental results from the pyroelectric device have been presented and discussed. Pyroelectric devices have been employed as infrared detectors [184], [185], owing to the property of their crystals to spontaneously polarise in response to changing temperature known as pyroelectricity [66]. Bruchhaus et al. [186] demonstrated a thin-film pyroelectric detector made from lead zirconium titanate (PZT) and the pyroelectric current measured from their device was as a result of changes in temperature. Pyroelectric current is dependent on the device area and typically in the order of tens of pico-amps. In recent time, graphene and other two-dimensional (2D) transition metal dichalcogenides (TMD) have been integrated with pyroelectric devices in order to improve the sensor's output [184] and in other cases, the performance of the 2D field effect transistor (FET) [187]. In this project, PZT has been used for the ferroelectric field effect transistor device due to its high capacitance, chemical stability and compatibility with fabrication processes among others. The ferroelectric property of PZT that allows for a reversal in polarisation has been explored in this experiment to gate test the WSe<sub>2</sub> field effect transistor based on PZT.

We have developed a standalone pyroelectric device (SPD) to benchmark against the integrated WSe<sub>2</sub> FET and pyroelectric device. The SPD is made from PZT sandwiched between a top and bottom electrode. The integrated pyroelectric device (IPD) is a combination of a WSe<sub>2</sub> field effect transistor based on thin film PZT. The pyroelectric current of the SPD and IPD as a function of

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

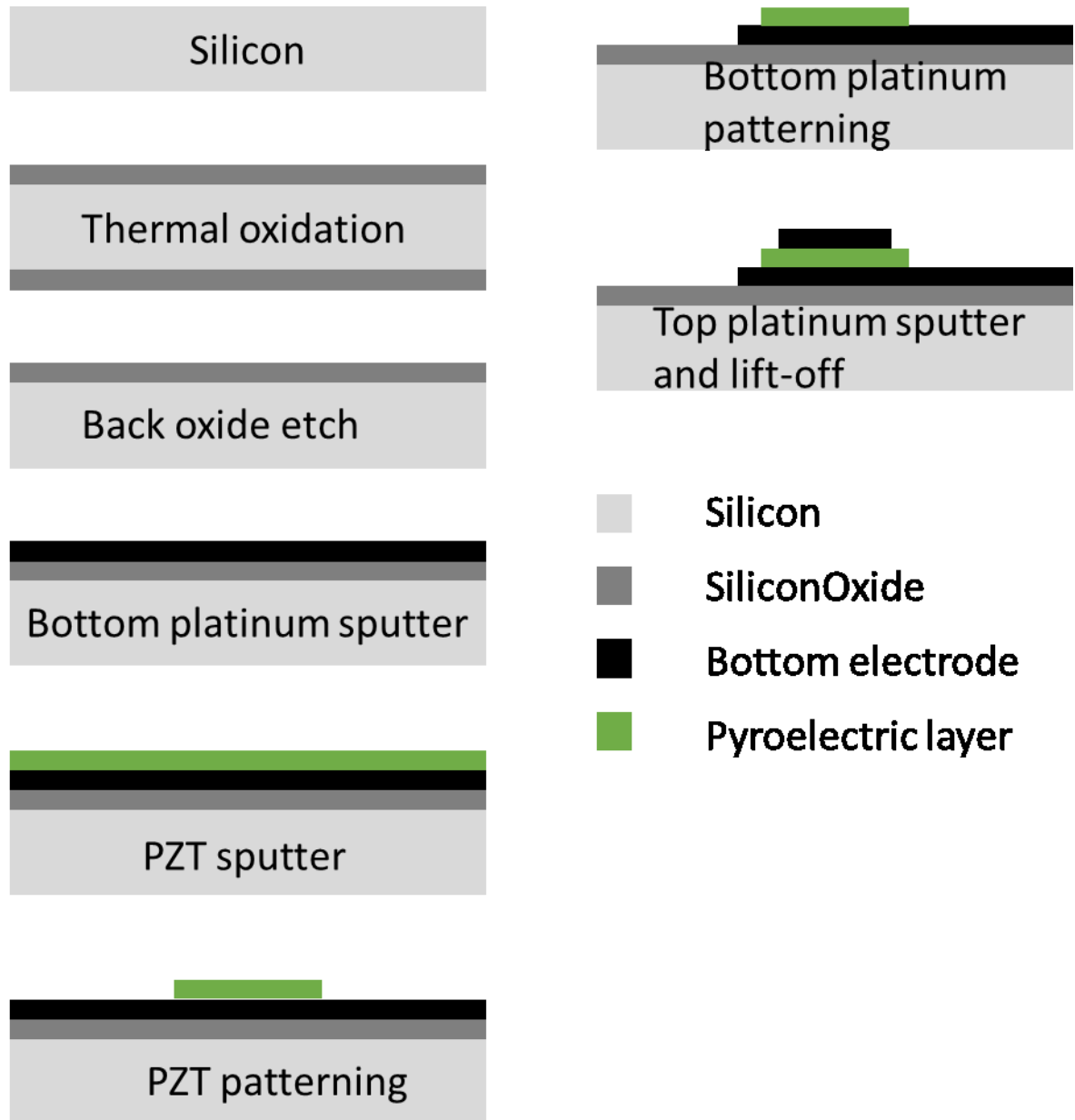
changes in temperature have been studied. Furthermore, the integrated device (PZT based WSe<sub>2</sub> FET) has been gated and the transfer characteristics plotted and analysed.

### 6.2 Experimental

#### 6.2.1 Fabrication of standalone pyroelectric device (SPD)

The standalone pyroelectric device was fabricated from a PZT pyroelectric material sandwiched between metal electrodes on a SiO<sub>2</sub>/Si substrate as described in Fig 6.1.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor



**Figure 6.1:** Fabrication process of a standalone pyroelectric device

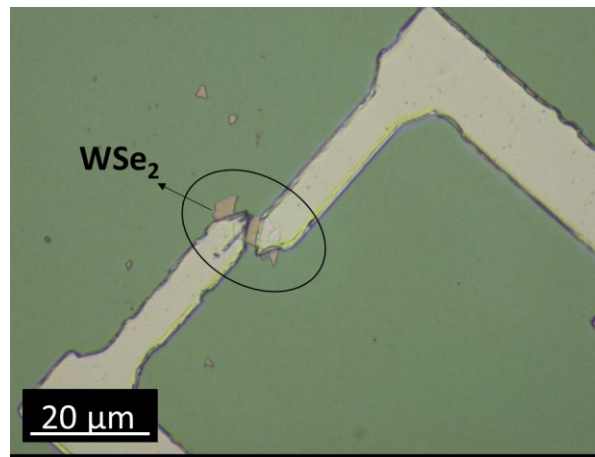
Firstly, 500 nm of SiO<sub>2</sub> was grown on Si substrate by thermal oxidation. Next, 40 nm of platinum was deposited on the SiO<sub>2</sub> serving as the bottom electrode. PZT was then sputter deposited from individual targets of the constituent elements at about 600 °C forming a 700 nm thin-film PZT layer. Using optical lithography, the PZT was patterned with photoresist and wet etched in an acidic solution (HCl : HF : HNO<sub>3</sub> : DIW). Finally, another layer of photoresist was patterned and

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

the platinum top electrode deposited via sputtering. The photo-resist was then lifted off, forming the standalone pyroelectric device of PZT sandwiched between platinum electrodes.

### 6.2.2 Fabrication of integrated pyroelectric device (IPD)

The integrated pyroelectric device consists of a WSe<sub>2</sub> FET on the PZT substrate. The fabrication process of the PZT has been described in Section 6.2.1. Exfoliation has been employed to transfer the WSe<sub>2</sub> onto the PZT surface. We have observed that the WSe<sub>2</sub> has a weak adhesion to PZT when compared to SiO<sub>2</sub>. The strong adhesion between WSe<sub>2</sub> and SiO<sub>2</sub> is believed to be due to the dangling bonds of SiO<sub>2</sub> [188], [189]. By employing the design of experiment (DoE) described below, WSe<sub>2</sub> has been transferred onto the PZT substrate successfully using Scotch-tape. With the aid of maskless lithography, photoresist was patterned and the metal electrodes (titanium/aluminium) have been deposited as the source and drain. The FET fabrication process is similar with the other chapters of this thesis and details can be found in Appendix A.



**Figure 6.2:** Actual device fabricated showing WSe<sub>2</sub> FET on PZT (IPD)

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

Figure 6.2 shows the 45 nm thick WSe<sub>2</sub> flake on PZT substrate with metal electrodes forming the drain and source.

### 6.2.2.1 Design of experiment (DoE) to improve WSe<sub>2</sub> adhesion on PZT

A factorial design has been initiated in an effort to improve the adhesion of WSe<sub>2</sub> on PZT via exfoliation. Our general process for transferring WSe<sub>2</sub> onto a substrate has been described in Section 4.2 of Chapter 4. In summary, the substrate is cleaned with IPA and DI water and then undergoes an oxygen plasma treatment. The WSe<sub>2</sub> is then exfoliated and transferred onto the substrate using Scotch tape. Before the Scotch tape is removed, the substrate is placed on a hot plate at a temperature  $T$  for a time  $t$ . The Scotch tape is only removed after this step. Using a DoE as shown in Table 6.1 below, we have inspected the PZT under a microscope to see the relative quantity of WSe<sub>2</sub> successfully transferred.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

**Table 6.1:** Experimental parameters for testing WSe<sub>2</sub> adhesion to PZT

S/N	T Temp (°C) (± 1)	t Time (secs)	O <sub>2</sub> Oxygen Plasma	Y Concentration of flakes
1	40	20	N	2
2	100	20	N	5
3	40	40	N	1
4	100	40	N	3
5	40	20	Y	10
6	100	20	Y	4
7	40	40	Y	8
8	100	40	Y	7

Three design factors, namely temperature, time and oxygen plasma have been studied. Table 6.1 shows the effect these factors have on the adhesion between WSe<sub>2</sub> and PZT. The temperature value (40 °C and 100 °C) represents the set temperature of the hot plate where the substrate is placed to improve its adhesion to the Scotch tape (described in Section 3.1.2 of Chapter 3). Time indicates the duration the substrate stays on the hot plate. The oxygen plasma was applied to some experiments described as “Y” and exempted for others “N”. Eight experimental runs have been performed with variations in temperature, time and oxygen plasma. Using a microscope to observe the quantity and distribution of the WSe<sub>2</sub> on the PZT substrate, the concentration of flakes (Y) has been allocated to each experimental run subjectively, with “10” having the highest concentration of flakes and “1” having the lowest.

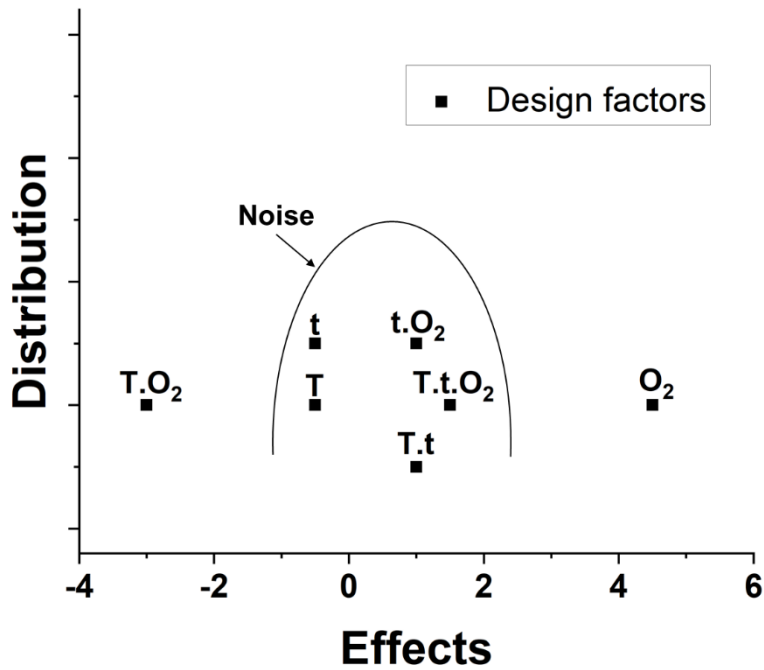
## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

**Table 6.2:**  $2^3$  factorial design to determine the effects of the design factors

$T$	$t$	$O_2$	$Y$	Effect	ID	$\hat{Y}$	$r = (Y - \hat{Y})$
-1	-1	-1	2	5	Avg	1.5	0.5
+1	-1	-1	5	-0.5	T	4	1
-1	+1	-1	1	-0.5	t	1.5	-0.5
+1	+1	-1	3	1	T*t	4	-1
-1	-1	+1	10	4.5	O <sub>2</sub>	9	1
+1	-1	+1	4	-3	T*O <sub>2</sub>	5.5	-1.5
-1	+1	+1	8	1	t*O <sub>2</sub>	9	-1
+1	+1	+1	7	1.5	T*t*O <sub>2</sub>	5.5	1.5

The results of the full factorial ( $2^3$ ) computation have been presented in Table 6.2. The values in the column *effect*, have been used to draw a line plot with the aim of determining the design factors that have had the most impact in resolving the adhesion between the WSe<sub>2</sub> and PZT. The sum of the values in the *residue* (r) column equals zero, indicating that the computation has no error. Detailed description on the factorial computation has been presented in Appendix C.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor



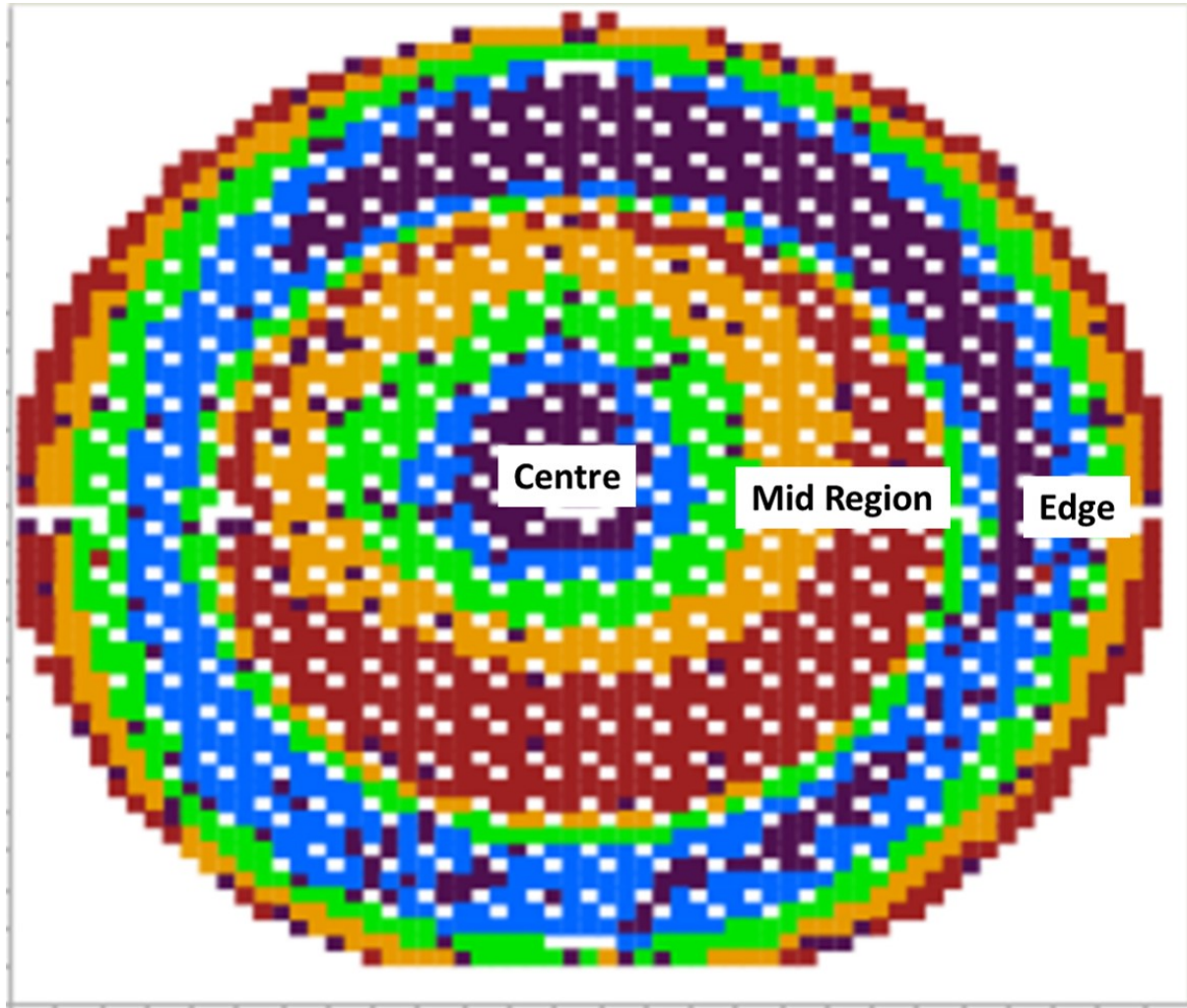
**Figure 6.3:** Line plot of design factors showing that temperature and oxygen are relevant adhesion factors

The line plot presents the design factors as a distribution based on their impact in resolving the adhesion between WSe<sub>2</sub> and PZT. From Fig 6.3, a cluster of single and multiple design factors can be seen between the -1 to +2 scale on the  $x$ -axis. This cluster is described as noise, since no useful information can be processed. On the other hand, temperature,  $T$ , and oxygen plasma,  $O_2$ , exist outside the noisy region, indicating that they have had a significant effect on the adhesion between the WSe<sub>2</sub> and PZT. From the result of the DoE, the selected parameters are  $T = 40\text{ }^{\circ}\text{C}$ ,  $t = 40\text{ secs}$ , and  $O_2 = Y$  with oxygen plasma being the most significant factor.

### **6.3 Results and Discussions**

#### **6.3.1 PZT Surface characteristics - investigation of PZT surface using a scanning electron microscope (SEM) and electron backscatter diffraction (EBSD) imaging**

Scanning Electron Microscope (SEM) and Electron Backscatter Diffraction (EBSD) images have been extracted from the PZT that had been sputtered on a 6 inch wafer. In this study, surface profile differences across the wafer can be determined from the PZT crystal shape and orientation. The experiment was carried out using a Carl Zeiss SIGMA HD VP field emission SEM with Oxford Instruments Aztec Synergy EBSD system. To perform the EBSD, a 10 kV accelerating voltage and a working distance of approximately 12.5 mm was applied to the 70° tilted sample. In the case of the SEM, an accelerating voltage of 3 kV and a working distance of about 5.5 mm were used.

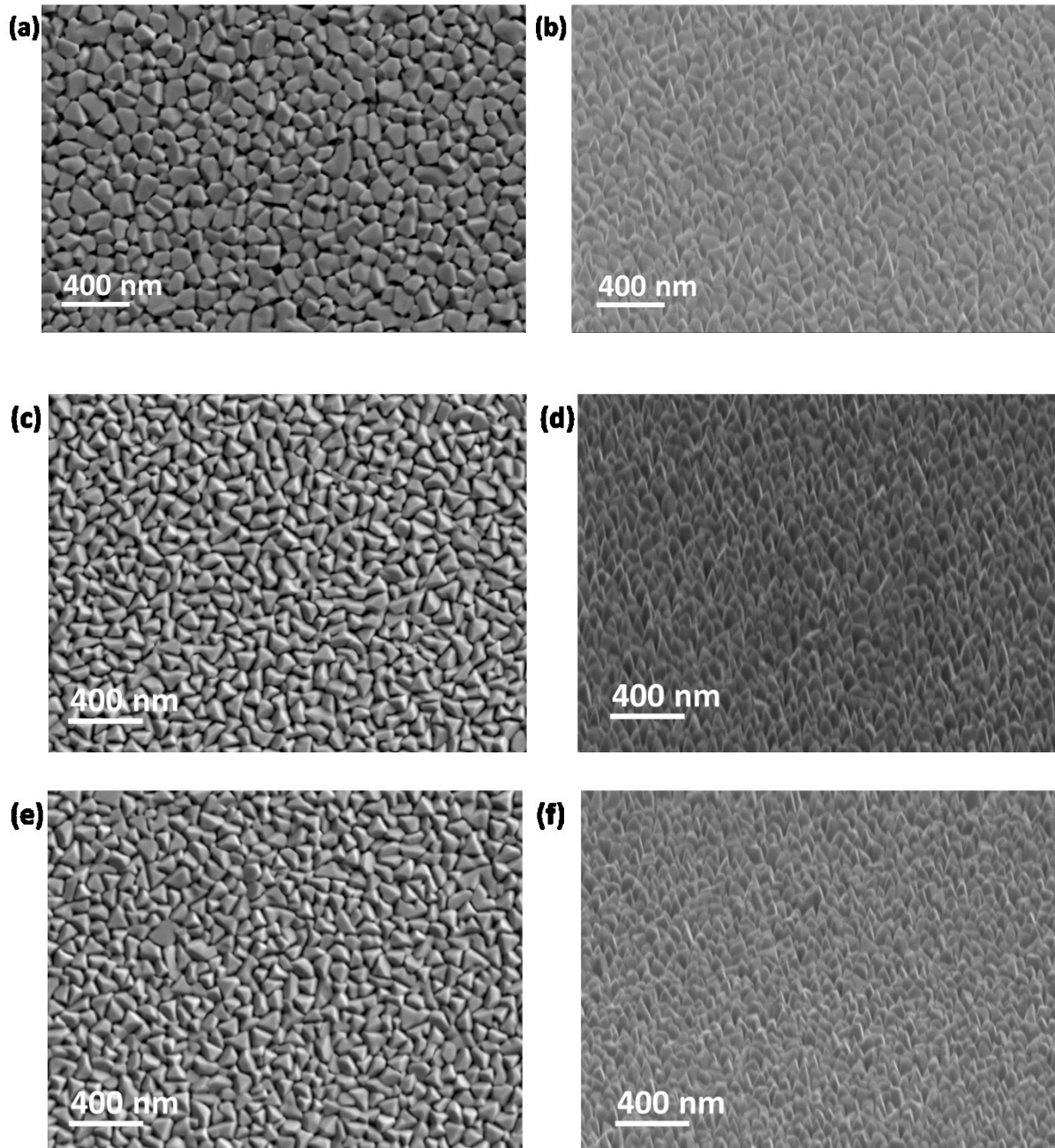


**Figure 6.4:** Image of PZT surface profile with donut shape provided by Pyreos Ltd [190]. The colour profile depicts donut shape appearance of wafer under bright light only

PZT has been sputtered on a 6-inch wafer, and by visual inspection appears to form rings as shown in Fig 6.4. These rings appear as slight colour variations across the wafer, resembling a donut shape. Three samples have been extracted from three sections of the wafer namely:

- Centre;
- Mid-region and
- Edge.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

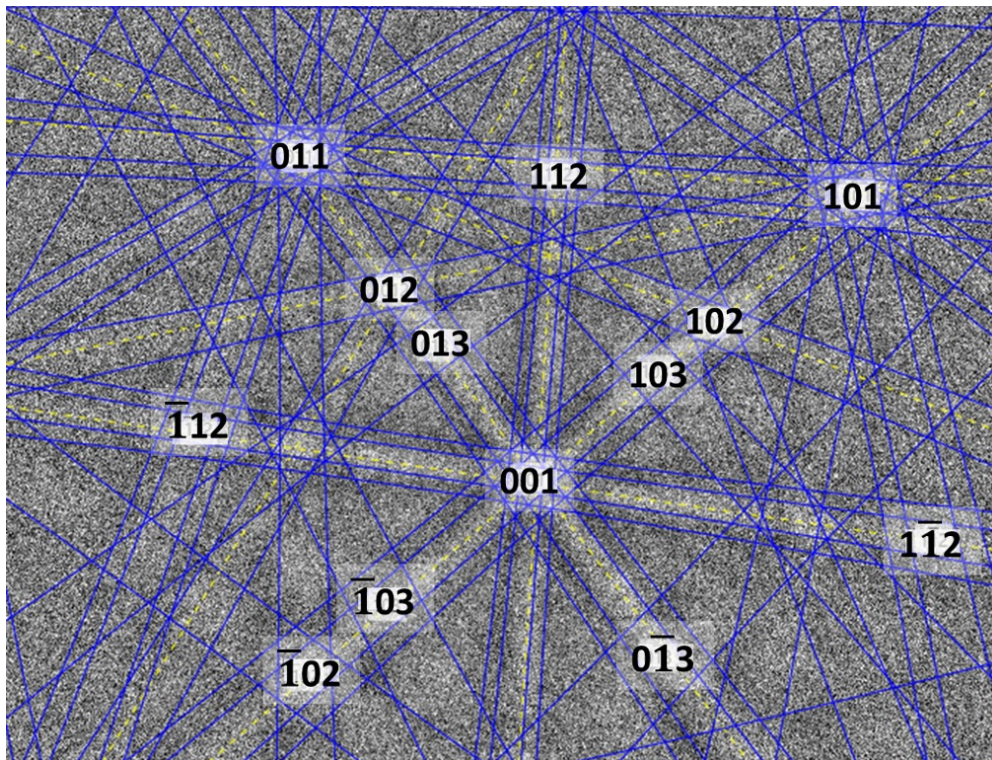


**Figure 6.5:** SEM surface profile (left images) and 70° tilt SEM image (right). (a)(b) wafer centre, (c)(d) wafer mid-region and (e)(f) wafer edge.

The graphs in Fig 6.5 show standard secondary electron (SE) images of the surface of the PZT. The SEM image in Fig 6.5(a), (c) and (e) have been captured directly from the sample top and the grain size measured is approximately 100 nm. However, the images in Fig 6.5(b), (d) and (f) have

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

been captured at an angle of 70°. From the images, it can be seen that many of the crystals grow into a pyramid shape. Many of the crystals can be seen to be narrowing towards the top, though not quite forming a point. Others are like sharp ridges, but there is very little flat (horizontal) surface to the samples, especially for the sample at the mid-region.

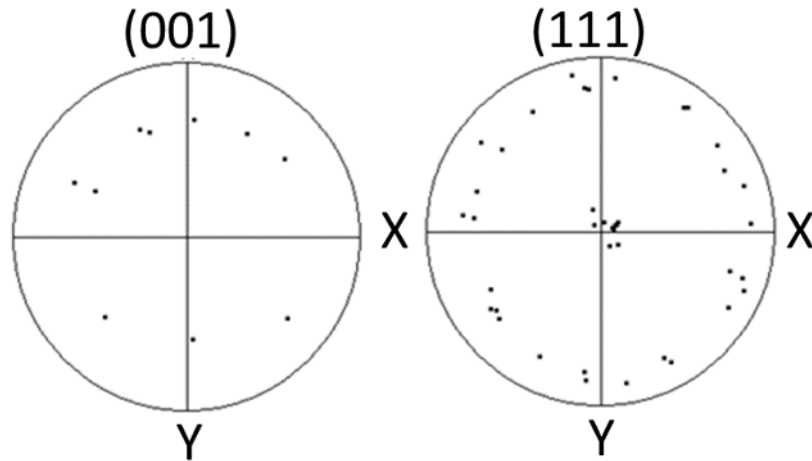


**Figure 6.6:** Electron diffraction pattern of a single point on the PZT

The diffraction pattern of the PZT grown on platinum has been formed by the electron beam interacting with a single point on the sample as shown in Fig 6.6. Using the Aztec system database, the solution for the diffraction pattern has been matched [191]. Upon successful detection and matching of the electron diffraction pattern, it is evident that the PZT exists in tetragonal crystals.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

From the data realised, the centre has about 25-30% useful patterns, the edge has about 20-25% and less than 20% from the mid-region were usable. This variation is likely due to the topography of the samples and the beam not hitting horizontal surfaces.



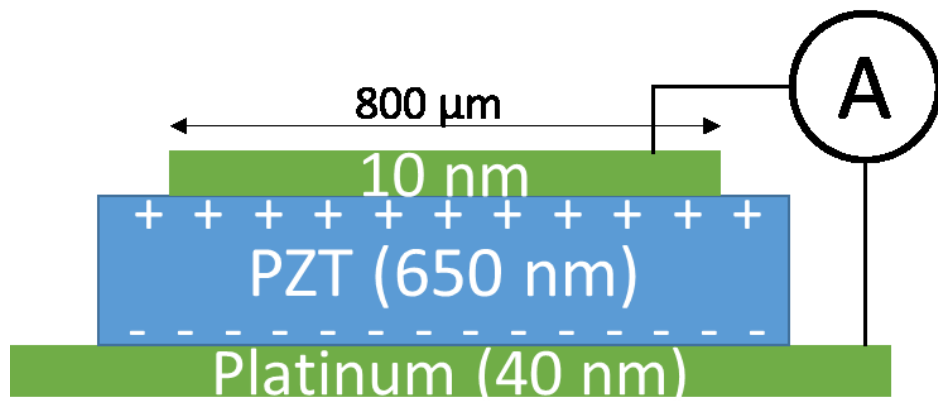
**Figure 6.7:** Pole figures of the (001) and (111) crystal facet, mapped from a single PZT grain

With the aid of the MTEX program, single crystal grains from the PZT have been mapped and plotted as can be seen in Fig. 6.7. The sample has been plotted for the orientation 001 and 111 zone axes. Each point may show more than once in the plot due to symmetry repetition. It can be seen that the data points of the (100) crystal facet are gathered on the side while the data points of the (111) crystal facet are gathered in the centre of the pole figures and this indicates that the PZT has a tetragonal shape. Furthermore, the pole figures show that the PZT with Pt seed layers have an orientation along the [111] direction normal to the surface as demonstrated by Köhler et al. [192].

### 6.3.2 Electrical Characteristics

The standalone and integrated pyroelectric devices formed in this experiment have been tested via heating and also by applying a potential difference. Testing pyroelectric samples by heating is a standard approach as mentioned in the materials and methods chapter and this technique is used by Pyreos.

#### 6.3.2.1 Standalone Pyroelectric Device (SPD)

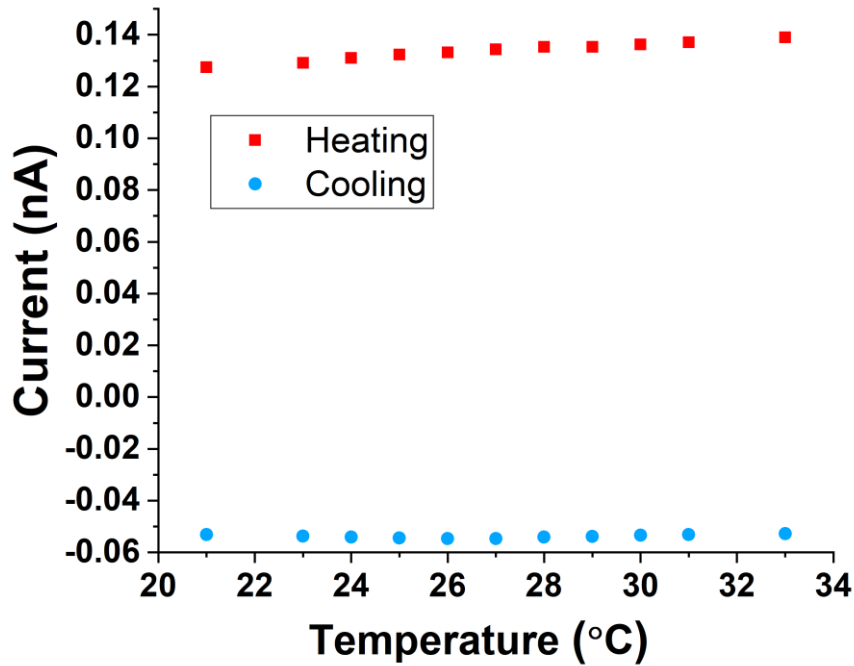


**Figure 6.8:** Schematic of PZT sandwiched with a top and bottom metal

The schematic in Fig. 6.8 is the standalone pyroelectric device which consists of PZT sandwiched between a top and bottom metal electrode. The PZT polarises as its temperature changes and the polarisation creates a separation of charges resulting in a built-in potential difference. These charges from the pyroelectric effect can be measured as pyroelectric current by an ammeter. However, the device has only been tested via two methods: a quasi-static method which remains the traditional method of characterising pyroelectric devices and this method has been described in Section 3.6 of Chapter 3. The second method of testing explored the ferroelectric property of

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

the pyroelectric device by gating the PZT and this method is similar to the FET test described in Section 3.7 of Chapter 3.



**Figure 6.9:** Pyroelectric current of the SPD against temperature

The standalone pyroelectric device has been tested against a controlled change in temperature both during heating and cooling as shown in Fig. 6.9. The heating and cooling system is integrated in the test set-up. For heating, there is an element embedded in the test stage which produces the heating effect while the cooling effect is via the flow of coolant around the stage. During heating (21 – 32 °C) of the device, 124 – 145 pA of pyroelectric current has been measured and when the device cooled (32 – 21 °C), 46 – 55 pA was measured. During heating, a higher degree of polarisation in the PZT has been realised than during cooling and this explains why a larger pyroelectric current has been measured during heating. The degree of polarisation is influenced by

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

the rate of change of temperature of the test element which heats up faster than it cools down. In addition, piezoelectric effect from material expansion can play a role in the overall polarisation achieved in pyroelectric materials, and this could explain the unstable pyroelectric current measured during heating. The heating and cooling effect creates a dipole moment in the PZT which causes the polarisation to reverse thereby changing the polarity of the measured pyroelectric current [64]. The top electrode of the standalone pyroelectric device is 0.64 mm<sup>2</sup> in area and using Eq. (6-1),  $1.755 \times 10^{-4}$  C/m<sup>2</sup>K has been calculated as the pyroelectric coefficient of the PZT. Bruchhaus et al. [186] reported a PZT based pyroelectric device that produced a pyroelectric current between 100 – 120 pA across a temperature range of 30 – 60 °C. Another PZT based device (nanogenerator) was reported by ref [193] to produce a pyroelectric current of about 430 nA, however, their device is 175 mm thick and 5 mm in electrode length.

$$p = \frac{i}{A * (dT/dt)} \quad Eq. (6-1)$$

where ***p*** is the pyroelectric coefficient, ***i*** is the pyroelectric current, ***A*** is the area, and ***dT/dt*** is the rate of change in temperature.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

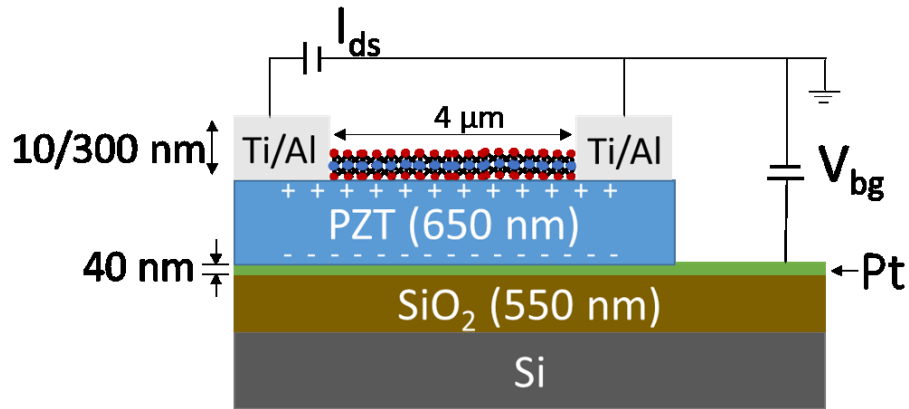
**Table 6.3:** Pyroelectric properties of samples with different dimensions

<b>Pixel-Area (<math>\mu\text{m}^2</math>)</b>	<b>Avg Pyro- Current (pA)</b>	<b>Avg- Pyrocoefficient (<math>\text{mC}/\text{m}^2\text{K}</math>)</b>	<b>Capacitance (nF) @ 1KHz</b>	<b>Dielectric Constant @ 1KHz</b>
450 x 450	0.493	0.1944	0.628	227.6894
700 x 700	1.18	0.1705	1.5	224.8822
750 x 750	1.13	0.1833	1.63	212.6523
8800 x 700	18.8	0.2017	20.5	228.2923

To investigate further the pyroelectric properties of the PZT, four devices have been fabricated with different surface areas as shown in Table 6.3. As the areas of the devices increases, a corresponding increase in pyroelectric current is measured. From the device area and measured current, the pyroelectric coefficient of the devices have been computed using Eq. 6-1. The pyroelectric coefficient of the different devices is relatively similar and the disparity is believed to be due to the surface topography. Similarly, the capacitance of the devices increases with area in agreement with Eq. 4-3 in Chapter 4. It can also be seen that the dielectric constant varies slightly amongst the different devices. Imperfections in the material crystal as was described in Section 6.3.1 (EBSD) is believed to be responsible for these variations in the pyroelectric coefficient and dielectric constant.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

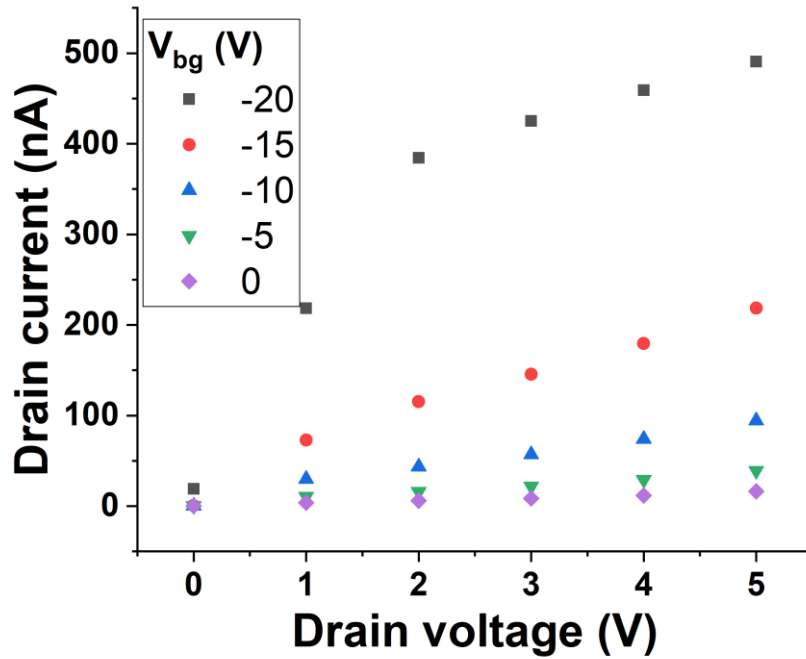
### 6.3.2.2 Integrated Pyroelectric Device (IPD)



**Figure 6.10:** Schematic of WSe<sub>2</sub>-PZT FET on a SiO<sub>2</sub>/Si substrate with dimensions

In Fig 6.10, the device schematic shows the material stack and the electrical connections. The bottom platinum electrode has been used to gate the device. A Keithley parameter analyser fitted with a thermal chuck stage has been used to test the device. An ATT-System module connected to the thermal chuck stage controls and measures the temperature. A temperature range between 21 and 32 °C has been applied to the sample and electrical measurements collected.

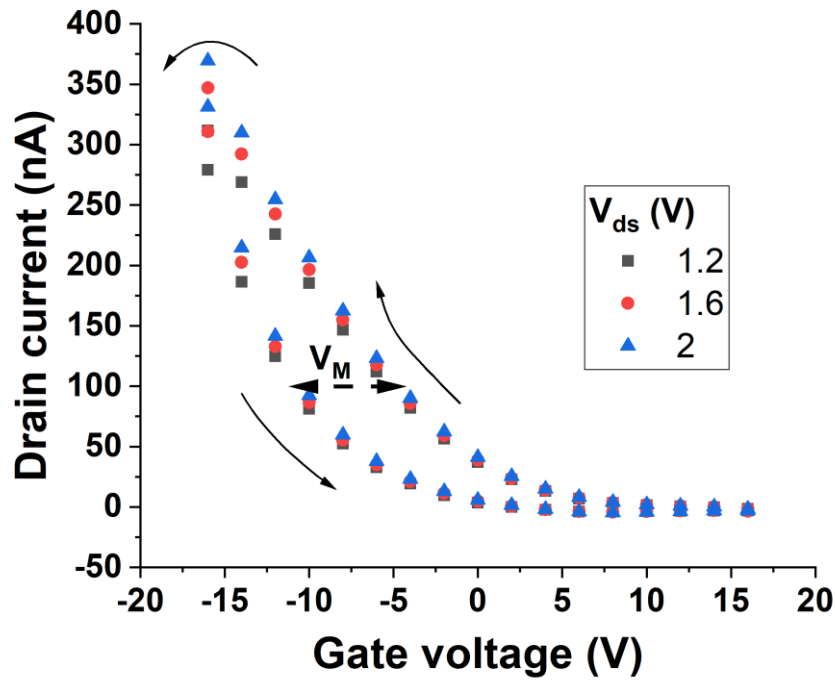
## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor



**Figure 6.11:** Output characteristics of WSe<sub>2</sub>-PZT FET with gate voltage from 0 to -20 V.

The output characteristics of the WSe<sub>2</sub> FET based on PZT is presented in Fig 6.11. The device has been gated from 0 to -20 V with incremental steps of 5 V and a drain-source voltage ( $V_{ds}$ ) from 0 to 5 V has been applied. The drain-source current in the graph begins linearly with incremental drain-source voltage and begins to pinch-off as it nears saturation indicating generic MOSFET behaviour.

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

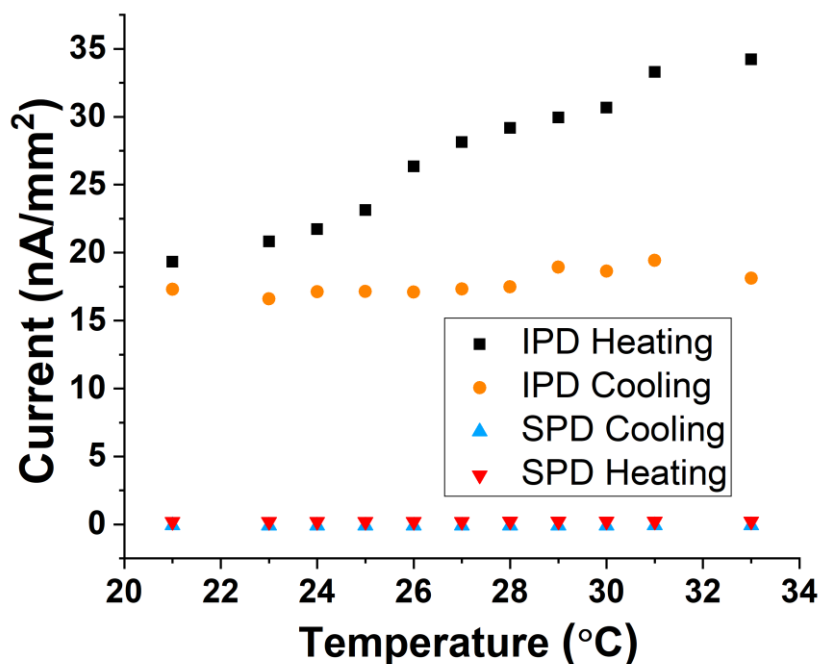


**Figure 6.12:** Transfer characteristics of WSe<sub>2</sub> FET based on PZT with visible ferroelectric behaviour. The gate voltage has been applied from -16 to 16 V with incremental steps of 2 V.

The integrated pyroelectric device has been back-gated from -16 to 16 V under varied drain-source voltage in order to study the ferroelectric behaviour. Each loop in Fig. 6.12 represents the ferroelectric response of the WSe<sub>2</sub> FET to the PZT polarisation. The maximum drain-source current of the WSe<sub>2</sub> FET is achieved at the maximum polarisation of the PZT. At a maximum gate voltage of -16 V, the PZT achieved maximum polarisation leading to a record drain-source current of 0.36  $\mu$ A. Our device is comparable to the ferroelectric WSe<sub>2</sub> FET based on CuInP<sub>2</sub>S<sub>6</sub> developed by Jiang et al. [9] and achieved a current output of 0.5  $\mu$ A. The arrows in the graph show the hysteresis direction of the integrated device and it is in sync with the direction of the polarisation vs voltage (P-V) curve [194]. The anti-clockwise hysteresis behaviour of the ferroelectric gate dielectric shows that the integrated device has a good ferroelectric response. Lu et al. [195] experienced a similar anti-clockwise hysteresis graph with their MoS<sub>2</sub> FET. The origin of

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

hysteresis has not completely been established, though, some reasons for current–voltage hysteresis include: ion migration within the ferroelectric material, the ferroelectric effect, and charge traps [196], [197]. Upon the application of a potential, the ion within a ferroelectric material migrates, leading to a build-up in the internal potential of the material. Current-voltage hysteresis can occur based on the speed of the migrating ions. This build-up in internal potential in ferroelectric materials otherwise called spontaneous electric polarisation is known as the ferroelectric effect. [198]. Research has shown that the ferroelectric effect can be affected by symmetry change within ferroelectric crystals resulting in a disruption in charge carrier extraction [199]. Furthermore, defects within the ferroelectric material can create charge trap sites and charge traps generally impede the charge transport within a material [196], [197], [200]. From Fig 6.11, the memory window of our device can be calculated. The memory window  $V_M$  is defined as the difference in gate voltage that occurs at the current value corresponding to the midpoint of the maximum and minimum possible current values of the device. The memory window of each loop has a very similar range despite changes in the drain-source voltage from 1.2 to 2 V. This indicates the stability of the device's memory window. The memory window has been calculated to be about  $7 (\pm 1)$  V for a gate-source voltage of 32 V (-16 to 16 V). Zhang et al. [201] reported a similar memory window for their MoS<sub>2</sub>-PZT FET, indicating possible deployment in memory application.



**Figure 6.13:** Current density of the integrated device and the standalone device under the single influence of changes in device temperature.

The current output from the corresponding temperature change for both the integrated device and the standalone pyroelectric device is shown in Fig. 6.13. A pyroelectric current density of 1 – 1.8 nA/mm<sup>2</sup> and 0.8 – 1 nA/mm<sup>2</sup> have been measured for the standalone device depicted in red and blue during heating and cooling respectively. The integrated device has been biased with a drain-source voltage of 1 V, represented with the black and orange plots. A current density of 20 – 35 nA/mm<sup>2</sup> and 16 – 19 nA/mm<sup>2</sup> have been measured during heating and cooling respectively. The combined area of the WSe<sub>2</sub> and the electrodes of the integrated device is 0.0526 mm<sup>2</sup>. No gate voltage has been applied to either the integrated or standalone device and the former shows an amplified current output of over ten orders of magnitude higher than the standalone device. We believe that the measured current for the integrated device is a result of a combined bolometric and pyroelectric response. Heat absorbed by the WSe<sub>2</sub> could affect the temperature coefficient of

## 6. Integration of pyroelectric device with WSe<sub>2</sub> field effect transistor

resistance (TCR) of the semiconductor, ultimately affecting the current transport properties of the material and device. Additionally, temperature changes should result in a pyroelectric effect, releasing charges which could modulate the resistance of the WSe<sub>2</sub> [184].

The data from Fig. 6.13 and Fig. 6.12 further reveals the effects of temperature and electric field on the integrated device respectively. While changes in the temperature (21 – 32°C) in Fig 6.13, resulted in an output current density of 15 nA/mm<sup>2</sup>, a current output of 370 nA (7 µA/mm<sup>2</sup>) has been realised from the effect of gate voltage (0 to -15V) as shown in Fig 6.12. From this comparison, it is evident that a higher polarisation in PZT is achieved from the gate potential through the ferroelectric effect than from the temperature change.

### 6.4 Conclusions

In this chapter, the surface properties of sputtered PZT layers, the crystallinity of PZT and the growth orientation of PZT layers on sputtered platinum have been investigated. From the EBSD analysis, sputtered PZT on platinum shows an average grain size of about 100 nm. We have observed that the PZT exists in tetragonal crystals having good correlation for an orientation along the [111] direction normal to the surface.

In addition, the design, fabrication and operation of a WSe<sub>2</sub>-PZT FET (IPD) and a PZT sandwiched between metal electrodes (SPD) have been presented. Adhesion challenges encountered between the PZT and WSe<sub>2</sub> were successfully resolved using a factorial design of experiment (DoE). The DoE showed that oxygen plasma treatment applied to the PZT had the most positive effect on adhesion.

From the measurements, the pyroelectric coefficient of the PZT was calculated to be  $1.755 \times 10^{-4}$  C/m<sup>2</sup>K. The current density output of the IPD and SPD is  $\sim 16$  nA/mm<sup>2</sup> and  $\sim 1$  nA/mm<sup>2</sup> respectively. Thus, the integrated device was a success as it amplified the current output of the standalone device by over ten orders of magnitude. Furthermore, it has been observed that the gate voltage induces more polarisation in the PZT than temperature change alone. Anti-clockwise hysteresis behaviour observed in the device shows direct control of PZT polarisation on the WSe<sub>2</sub> FET.

# Chapter 7

## Conclusions and future work

### 7.1 Final Conclusion

The aim of this research is to improve the measured current from a PZT based sensor by integrating the device with a WSe<sub>2</sub> field effect transistor (FET). We have taken a systematic and comprehensive approach to the research by studying the different materials individually and combined.

Firstly, we have characterised WSe<sub>2</sub> produced via exfoliation and pulse laser deposition (PLD). Our findings reveal that the exfoliated WSe<sub>2</sub> has better electrical and optical properties than the PLD WSe<sub>2</sub>. Photoluminescence spectroscopy confirms the lack of band gap in the PLD WSe<sub>2</sub> thereby limiting its applications. However, the PLD WSe<sub>2</sub> is better suited for integration in CMOS processes as the size and thickness of the deposited WSe<sub>2</sub> can be better controlled. PLD is a much simpler technique than CVD and also deposits materials at much lower temperature. The PLD technique is not as developed as CVD, hence, PLD could possess huge potentials as it matures.

The second aspect to the research is the pyroelectric device. To better understand the PZT crystal, energy backscatter diffraction (EBSD) test has been performed on the sample. The solution of the EBSD shows that the crystals aligned differently across the 6-inch wafer. This discovery has enabled us to understand why there are slight variations in the electrical performance of the PZT across the wafer. In our effort to integrate the exfoliated WSe<sub>2</sub> with the PZT, adhesion challenges have been encountered. With the aid of a 2<sup>3</sup> factorial design of experiment, the adhesion between the PZT and WSe<sub>2</sub> has been improved, mainly from an oxygen plasma treatment. The integrated

## 7. Conclusions and future work

device shows a ten order of magnitude amplification in the current output. Our result indicates that the standalone PZT device can be improved by integrating with a WSe<sub>2</sub> field effect transistor.

Among the emerging techniques in the literature for integrating high- $\kappa$  dielectric with 2D materials, is the double gate structure (shown in section 7.3). The floating gate is usually made of a high- $\kappa$  dielectric material. In consideration to double gate the integrated device, anodization technique has been studied as a means to develop a high- $\kappa$  dielectric material. Anodic tantalum has been created and characterised in the course of this research. A capacitor created from 20 nm Ta<sub>2</sub>O<sub>5</sub> has been tested and it has a dielectric constant of about 18. Moreover, the breakdown characteristics and conduction mechanism of the anodic tantalum has been analysed. Furthermore, we integrated the anodic tantalum with the exfoliated WSe<sub>2</sub> FET, possibly the first ever attempt. Good adhesion exists between the materials and the transistor shows promise for low power operation.

### 7.2 Achieved Objectives

- I have characterised the exfoliated and PLD WSe<sub>2</sub> and concluded that while PLD WSe<sub>2</sub> is better suited for CMOS processes, the lack of bandgap limits its performance and application.
- I have demonstrated and characterised PZT as a standalone sensor. Also, I have highlighted the PZT surface differences across the 6-inch wafer, which has provided some feedback to the company Pyreos.
- I developed a 2<sup>3</sup> factorial design of experiment that has improved the adhesion between WSe<sub>2</sub> and PZT, thereby enabling the device integration.
- I have developed and characterised anodic tantalum as a high- $\kappa$  dielectric and analysed its conduction mechanism. Furthermore, I integrated anodic tantalum with a WSe<sub>2</sub> FET, showing improved FET performance.

## 7. Conclusions and future work

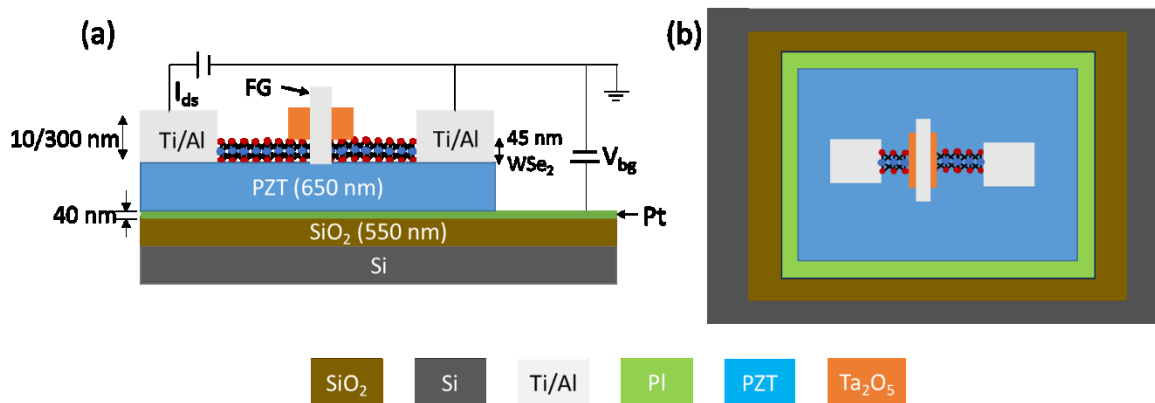
- I developed and demonstrated the integration of PZT and WSe<sub>2</sub> FET, ultimately amplifying the current output of the integrated devices.

### 7.3 Future Work

Our current study has shown that 2D FET output improves as the quality of their substrate dielectric increases. However, future success and continuous improvement will be achieved from choice of material, device design and test procedures. Therefore, the following research areas could enhance future output:

#### Point 1:

A floating gate structure should further enhance our WSe<sub>2</sub> PZT based FET. The floating gate creates a second source of potential emanating from the top of the device as shown in Fig 7.1.



**Figure 7.1:** (a) Schematic of WSe<sub>2</sub> PZT based FET with floating gate (FG). (b) Top view of proposed device

## 7. Conclusions and future work

By depositing a high- $\kappa$  dielectric ( $\text{Ta}_2\text{O}_5$ ) and a metal electrode over the  $\text{WSe}_2$ , the FET is encapsulated. When the platinum bottom gate is ON, the PZT substrate creates a bottom electric field. The floating gate then transports the pyro-current from the PZT substrate across the  $\text{Ta}_2\text{O}_5$ . The  $\text{Ta}_2\text{O}_5$  then creates an electric field at the top of the FET which contributes to the bottom field emanating from the PZT. This top and bottom electric field structure is similar to a FinFET and could further improve the output of the device.

### **Point 2:**

Pulse laser deposition (PLD) technique for depositing  $\text{WSe}_2$  shows promise by virtue of its large deposition area, ease of control of material thickness, simplicity of setup and process and low deposition temperature. The technique is well suited for CMOS operation and allows for integration with other materials. When the PLD technique is matured and can deposit quality yields, the technique will enhance the fabrication process. Furthermore, quality samples will be used in experiments thus improving the experimental results. In addition, the PLD technique will improve the accuracy of material dimensions and allow for the fabrication of complex designs.

### **Point 3:**

The integrated pyroelectric device (IPD) which consists of a  $\text{WSe}_2$  FET based on PZT will provide relevant data when tested using infra-red. In order to actualise the test, the fabricated device will need to be wire-bonded. It should be expected that the resistive properties of the  $\text{WSe}_2$  will be affected by the infra-red. However, the test can be carried out in such a way that the FET is outside the line of sight of the infra-red. Results from such a test can be bench-marked against the static-quasi technique employed in this research and should provide further insights on the integrated device.

## 8. References

- [1] S. Wang, X. Liu, and P. Zhou, “The Road for 2D Semiconductors in the Silicon Age,” *Adv. Mater.*, vol. 34, no. 48, p. 2106886, 2022, doi: 10.1002/adma.202106886.
- [2] J. A. Wilson and A. D. Yoffe, “The transition metal dichalcogenides discussion and interpretation of the observed optical, electrical and structural properties,” *Adv. Phys.*, vol. 18, no. 73, pp. 193–335, May 1969, doi: 10.1080/00018736900101307.
- [3] A. Mohammed *et al.*, “Pulsed laser deposition for the synthesis of monolayer WSe<sub>2</sub>,” *Appl. Phys. Lett.*, vol. 111, no. 7, p. 073101, Aug. 2017, doi: 10.1063/1.4986851.
- [4] M. I. B. Utama, X. Lu, Y. Yuan, and Q. Xiong, “Detrimental influence of catalyst seeding on the device properties of CVD-grown 2D layered materials: A case study on MoSe<sub>2</sub>,” *Appl. Phys. Lett.*, vol. 105, no. 25, p. 253102, Dec. 2014, doi: 10.1063/1.4904945.
- [5] H. G. Kim and H.-B.-R. Lee, “Atomic Layer Deposition on 2D Materials,” *Chem. Mater.*, vol. 29, no. 9, pp. 3809–3826, May 2017, doi: 10.1021/acs.chemmater.6b05103.
- [6] S. V. Morozov *et al.*, “Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer,” *Phys. Rev. Lett.*, vol. 100, no. 1, p. 016602, Jan. 2008, doi: 10.1103/PhysRevLett.100.016602.
- [7] S. Ahmed and J. Yi, “Two-Dimensional Transition Metal Dichalcogenides and Their Charge Carrier Mobilities in Field-Effect Transistors,” *Nano-Micro Lett.*, vol. 9, no. 4, p. 50, Aug. 2017, doi: 10.1007/s40820-017-0152-6.
- [8] K. K. Gopalan *et al.*, “Mid-Infrared Pyroresistive Graphene Detector on LiNbO<sub>3</sub>,” *Adv. Opt. Mater.*, vol. 5, no. 4, p. 1600723, 2017, doi: 10.1002/adom.201600723.
- [9] X. Jiang *et al.*, “Ferroelectric Field-Effect Transistors Based on WSe<sub>2</sub>/CuInP<sub>2</sub>S<sub>6</sub> Heterostructures for Memory Applications,” *ACS Appl. Electron. Mater.*, vol. 3, no. 11, pp. 4711–4717, Nov. 2021, doi: 10.1021/acsaelm.1c00492.
- [10] K.S. Novoselov *et al.*, “Electric field effect in atomically thin carbon films, *Science*,” *Science*, vol. 306, no. 5696, pp. 666–9, 2004.
- [11] S. Z. Butler *et al.*, “Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene,” *ACS Nano*, vol. 7, no. 4, pp. 2898–2926, Apr. 2013, doi: 10.1021/nn400280c.
- [12] R. Yue *et al.*, “Nucleation and growth of WSe<sub>2</sub>: enabling large grain transition metal dichalcogenides,” *2D Mater.*, vol. 4, no. 4, p. 045019, Sep. 2017, doi: 10.1088/2053-1583/aa8ab5.
- [13] H. Sahin *et al.*, “Anomalous Raman spectra and thickness-dependent electronic properties of WSe<sub>2</sub>,” *Phys. Rev. B*, vol. 87, no. 16, p. 165409, Apr. 2013, doi: 10.1103/PhysRevB.87.165409.
- [14] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, “Electronics and optoelectronics of two-dimensional transition metal dichalcogenides,” *Nat. Nanotechnol.*, vol. 7, no. 11, pp. 699–712, Nov. 2012, doi: 10.1038/nnano.2012.193.
- [15] R. Addou and R. M. Wallace, “Surface Analysis of WSe<sub>2</sub> Crystals: Spatial and Electronic Variability,” *ACS Appl. Mater. Interfaces*, vol. 8, no. 39, pp. 26400–26406, Oct. 2016, doi: 10.1021/acsaami.6b08847.
- [16] R. Browning, N. Kuperman, R. Solanki, V. Kanzyuba, and S. Rouvimov, “Large area growth of layered WSe<sub>2</sub> films,” *Semicond. Sci. Technol.*, vol. 31, no. 9, p. 095002, Jul. 2016, doi: 10.1088/0268-1242/31/9/095002.
- [17] J. A. Greer and M. D. Tabat, “Large-area pulsed laser deposition: Techniques and applications,” *J. Vac. Sci. Technol. A*, vol. 13, no. 3, pp. 1175–1181, May 1995, doi: 10.1116/1.579857.

## 8. References

- [18] T. A. J. Loh, D. H. C. Chua, and A. T. S. Wee, “One-step Synthesis of Few-layer WS<sub>2</sub> by Pulsed Laser Deposition,” *Sci. Rep.*, vol. 5, no. 1, p. 18116, Dec. 2015, doi: 10.1038/srep18116.
- [19] G. Siegel, V. Yerva, M. Prestgard, and A. Tiwari, “Growth of centimeter-scale atomically thin MoS<sub>2</sub> films by pulsed laser deposition,” *APL Mater.*, vol. 3, p. 056103, May 2015, doi: 10.1063/1.4921580.
- [20] S. Seo *et al.*, “Growth of Centimeter-Scale Monolayer and Few-Layer WSe<sub>2</sub> Thin Films on SiO<sub>2</sub> /Si Substrate via Pulsed Laser Deposition,” *Adv. Mater. Interfaces*, vol. 5, no. 20, p. 1800524, Oct. 2018, doi: 10.1002/admi.201800524.
- [21] W. Zhao *et al.*, “Origin of Indirect Optical Transitions in Few-Layer MoS<sub>2</sub>, WS<sub>2</sub>, and WSe<sub>2</sub>,” *Nano Lett.*, vol. 13, no. 11, pp. 5627–5634, Nov. 2013, doi: 10.1021/nl403270k.
- [22] P. Tonndorf *et al.*, “Photoluminescence emission and Raman response of monolayer MoS<sub>2</sub>, MoSe<sub>2</sub>, and WSe<sub>2</sub>,” *Opt. Express*, vol. 21, no. 4, pp. 4908–4916, Feb. 2013, doi: 10.1364/OE.21.004908.
- [23] H. Wilman, “Review of The Collected Works of Irving Langmuir. Vol. 9: Surface Phenomena,” *Sci. Prog. 1933-*, vol. 50, no. 200, pp. 687–688, 1962.
- [24] J. P. Biberian and G. A. Somorjai, “Surface structures of metallic monolayers on metal crystal surfaces,” *J. Vac. Sci. Technol.*, vol. 16, no. 6, pp. 2073–2085, Nov. 1979, doi: 10.1116/1.570343.
- [25] H. Liu *et al.*, “Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility,” *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, Apr. 2014, doi: 10.1021/nn501226z.
- [26] L. Li *et al.*, “Black phosphorus field-effect transistors,” *Nat. Nanotechnol.*, vol. 9, no. 5, pp. 372–377, May 2014, doi: 10.1038/nnano.2014.35.
- [27] X. Li, J. T. Mullen, Z. Jin, K. M. Borysenko, M. Buongiorno Nardelli, and K. W. Kim, “Intrinsic electrical transport properties of monolayer silicene and MoS<sub>2</sub> from first principles,” *Phys. Rev. B*, vol. 87, no. 11, p. 115418, Mar. 2013, doi: 10.1103/PhysRevB.87.115418.
- [28] C. C. Mayorga-Martinez, Z. Sofer, and M. Pumera, “Layered Black Phosphorus as a Selective Vapor Sensor,” *Angew. Chem. Int. Ed Engl.*, vol. 54, no. 48, pp. 14317–14320, Nov. 2015, doi: 10.1002/anie.201505015.
- [29] R. Zhang, D. Drysdale, V. Koutsos, and R. Cheung, “Controlled Layer Thinning and p-Type Doping of WSe<sub>2</sub> by Vapor XeF<sub>2</sub>,” *Adv. Funct. Mater.*, vol. 27, no. 41, p. 1702455, 2017, doi: 10.1002/adfm.201702455.
- [30] H. Zhao, Q. Guo, F. Xia, and H. Wang, “Two-dimensional materials for nanophotonics application,” *Nanophotonics*, vol. 4, no. 2, pp. 128–142, May 2015, doi: 10.1515/nanoph-2014-0022.
- [31] Y. J. Zhang, T. Oka, R. Suzuki, J. T. Ye, and Y. Iwasa, “Electrically Switchable Chiral Light-Emitting Transistor,” *Science*, vol. 344, no. 6185, pp. 725–728, May 2014, doi: 10.1126/science.1251329.
- [32] R. Zhang and R. Cheung, *Mechanical Properties and Applications of Two-Dimensional Materials*. IntechOpen, 2016. doi: 10.5772/64017.
- [33] C. Lee, X. Wei, J. W. Kysar, and J. Hone, “Measurement of the elastic properties and intrinsic strength of monolayer graphene,” *Science*, vol. 321, no. 5887, pp. 385–388, Jul. 2008, doi: 10.1126/science.1157996.
- [34] S. Das, R. Gulotty, A. V. Sumant, and A. Roelofs, “All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor,” *Nano Lett.*, vol. 14, no. 5, pp. 2861–2866, May 2014, doi: 10.1021/nl5009037.

## 8. References

- [35] Y. Wang *et al.*, “Strain-induced direct–indirect bandgap transition and phonon modulation in monolayer WS<sub>2</sub>,” *Nano Res.*, vol. 8, no. 8, pp. 2562–2572, Aug. 2015, doi: 10.1007/s12274-015-0762-6.
- [36] C. Chen *et al.*, “Performance of monolayer graphene nanomechanical resonators with electrical readout,” *Nat. Nanotechnol.*, vol. 4, no. 12, Art. no. 12, Dec. 2009, doi: 10.1038/nnano.2009.267.
- [37] C. Zhang, M. Yu, G. Anderson, R. R. Dharmasena, and G. Sumanasekera, “The prospects of phosphorene as an anode material for high-performance lithium-ion batteries: a fundamental study,” *Nanotechnology*, vol. 28, no. 7, p. 075401, Feb. 2017, doi: 10.1088/1361-6528/aa52ac.
- [38] X. Sun *et al.*, “Room temperature ferromagnetism in ultra-thin van der Waals crystals of 1T-CrTe<sub>2</sub>,” *Nano Res.*, vol. 13, no. 12, pp. 3358–3363, Dec. 2020, doi: 10.1007/s12274-020-3021-4.
- [39] F. Liu *et al.*, “Room-temperature ferroelectricity in CuInP2S6 ultrathin flakes,” *Nat. Commun.*, vol. 7, p. 12357, Aug. 2016, doi: 10.1038/ncomms12357.
- [40] G. He and Z. Sun, *High-κ Gate Dielectrics for CMOS Technology*. Weinheim : Wiley-VCH, 2012.
- [41] J. Robertson and C. W. Chen, “Schottky barrier heights of tantalum oxide, barium strontium titanate, lead titanate, and strontium bismuth tantalate,” *Appl. Phys. Lett.*, vol. 74, no. 8, pp. 1168–1170, Feb. 1999, doi: 10.1063/1.123476.
- [42] G. D. Wilk, R. M. Wallace, and J. M. Anthony, “High-κ gate dielectrics: Current status and materials properties considerations,” *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001, doi: 10.1063/1.1361065.
- [43] G. E. Moore, “Cramming more components onto integrated circuits, Reprinted from *Electronics*, volume 38, number 8, April 19, 1965, pp.114 ff.,” *IEEE Solid-State Circuits Soc. Newsl.*, vol. 11, no. 3, pp. 33–35, Sep. 2006, doi: 10.1109/N-SSC.2006.4785860.
- [44] H. C. Casey, Jr., *Devices for Integrated Circuits: Silicon and III-V Compound Semiconductors*. New York: John Wiley & Sons, 1999.
- [45] “Moore’s law,” *Wikipedia*. Feb. 15, 2023. Accessed: Mar. 04, 2023. [Online]. Available: [https://en.wikipedia.org/w/index.php?title=Moore%27s\\_law&oldid=1139518707#References](https://en.wikipedia.org/w/index.php?title=Moore%27s_law&oldid=1139518707#References)
- [46] “The end of the road for silicon? | Nature.” <https://www-nature-com.ezproxy.is.ed.ac.uk/articles/21526> (accessed Aug. 20, 2021).
- [47] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, “The electronic structure at the atomic scale of ultrathin gate oxides,” *Nature*, vol. 399, no. 6738, pp. 758–761, Jun. 1999, doi: 10.1038/21602.
- [48] B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T. J. Marks, and A. Facchetti, “High-κ Gate Dielectrics for Emerging Flexible and Stretchable Electronics,” *Chem. Rev.*, vol. 118, no. 11, Art. no. 11, Jun. 2018, doi: 10.1021/acs.chemrev.8b00045.
- [49] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004, doi: 10.1051/epjap:2004206.
- [50] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.*, vol. 18, pp. 1785–1791, Sep. 2000.
- [51] P. Darmawan, P. S. Lee, Y. Setiawan, J. C. Lai, and P. Yang, “Thermal stability of rare-earth based ultrathin Lu<sub>2</sub>O<sub>3</sub> for high-k dielectrics,” *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.*, vol. 25, no. 4, pp. 1203–1206, Jul. 2007, doi: 10.1116/1.2749526.

## 8. References

- [52] R. L. Puurunen, "Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process," *J. Appl. Phys.*, vol. 97, no. 12, p. 121301, Jun. 2005, doi: 10.1063/1.1940727.
- [53] R. J. Forbes, "On the Origin of Alchemy," *Chymia*, vol. 4, pp. 1–11, 1953, doi: 10.2307/27757160.
- [54] L. Young, "Anodization constants for tantalum," *J Electrochem Soc U. S.*, vol. 124:4, Apr. 1977, doi: 10.1149/1.2133341.
- [55] S. Ezhilvalavan and T. Y. Tseng, "Preparation and properties of tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) thin films for ultra large scale integrated circuits (ULSIs) application – A review," *J. Mater. Sci. Mater. Electron.*, vol. 10, no. 1, pp. 9–31, Mar. 1999, doi: 10.1023/A:1008970922635.
- [56] J. M. Runge, *The Metallurgy of Anodizing Aluminum: Connecting Science to Practice*. Springer International Publishing, 2018. doi: 10.1007/978-3-319-72177-4.
- [57] D. W. H. J, W. C, and C. C, "Impedance measurements during anodization of aluminum.," *J Electrochem Soc*, vol. 126, no. 5, pp. 779–785, 1979.
- [58] X. Wu, H. Bai, J. Zhang, F. Chen, and G. Shi, "Copper Hydroxide Nanoneedle and Nanotube Arrays Fabricated by Anodization of Copper," *J. Phys. Chem. B*, vol. 109, no. 48, pp. 22836–22842, Dec. 2005, doi: 10.1021/jp054350p.
- [59] R. J. Dreiner and T. B. Tripp, "Anodization of Tantalum Over the Temperature Range  $0^\circ$  to  $250^\circ\text{C}$ ," *J. Electrochem. Soc.*, vol. 117, no. 7, p. 858, 1970, doi: 10.1149/1.2407657.
- [60] J. Klerer, "Determination of the Density and Dielectric Constant of Thin  $\text{Ta}_2\text{O}_5$  Films," *J. Electrochem. Soc.*, vol. 112, no. 9, p. 896, Sep. 1965, doi: 10.1149/1.2423725.
- [61] C. Chaneliere, J. L. Autran, R. A. B. Devine, and B. Balland, "Tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) thin films for advanced dielectric applications," *Mater. Sci. Eng. R Rep.*, vol. 22, no. 6, pp. 269–322, May 1998, doi: 10.1016/S0927-796X(97)00023-5.
- [62] I. M. Ross, "Semiconductive translating device," US2791760A, May 07, 1957 Accessed: Aug. 12, 2021. [Online]. Available: <https://patents.google.com/patent/US2791760A/en>
- [63] H. D. Megaw, *Ferroelectricity in crystals*. London: Methuen, 1957.
- [64] S. Lang, "The history of pyroelectricity: From ancient greece to space missions," 1999, doi: 10.1080/00150199908214903.
- [65] S. B. Lang, "Pyroelectricity: From Ancient Curiosity to Modern Imaging Tool," *Phys. Today*, vol. 58, no. 8, pp. 31–36, Aug. 2005, doi: 10.1063/1.2062916.
- [66] J. C. Burfoot and G. W. Taylor, *Polar Dielectrics and their Applications*. London: Macmillan, 1979.
- [67] Y. Xu, *Ferroelectric Materials and Their Applications*. Amsterdam: Elsevier Science & Technology, 1991.
- [68] M. E. Lines, *Principles and applications of ferroelectrics and related materials*. Oxford: Clarendon Press, 1977.
- [69] R. W. Whatmore, "Pyroelectric devices and materials," *Rep. Prog. Phys.*, vol. 49, no. 12, pp. 1335–1386, 1986, doi: 10.1088/0034-4885/49/12/002.
- [70] S. L. Swartz, "Topics in electronic ceramics," *IEEE Trans. Electr. Insul.*, vol. 25, no. 5, pp. 935–987, Oct. 1990, doi: 10.1109/14.59868.
- [71] G. H. Haertling, "Ferroelectric Ceramics: History and Technology," *J. Am. Ceram. Soc.*, vol. 82, no. 4, pp. 797–818, 1999, doi: 10.1111/j.1151-2916.1999.tb01840.x.
- [72] "MattDawber'sGroup[Research]." <https://mini.physics.sunysb.edu/~mdawber/research.htm>. (Accessed Aug. 13, 2021).
- [73] P. L. Richards and C. R. McCreight, "Infrared Detectors for Astrophysics," *Phys. Today*, vol. 58, no. 2, pp. 41–47, Feb. 2005, doi: 10.1063/1.1897522.

## 8. References

- [74] B. F. Jones, "A reappraisal of the use of infrared thermal image analysis in medicine," *IEEE Trans. Med. Imaging*, vol. 17, no. 6, pp. 1019–1027, Dec. 1998, doi: 10.1109/42.746635.
- [75] D. Wilson, J. W. Phair, and M. Lengden, "Performance Analysis of a Novel Pyroelectric Device for Non-Dispersive Infra-Red CO<sub>2</sub> Detection," *IEEE Sens. J.*, vol. 19, no. 15, pp. 6006–6011, Aug. 2019, doi: 10.1109/JSEN.2019.2911737.
- [76] G. C. M. Meijer, *Smart sensor systems / edited by Gerard C.M. Meijer*. Chichester, U.K: J. Wiley & Sons, 2008. doi: 10.1002/9780470866931.
- [77] P. Rudol and P. Doherty, "Human Body Detection and Geolocalization for UAV Search and Rescue Missions Using Color and Thermal Imagery," in *2008 IEEE Aerospace Conference*, Mar. 2008, pp. 1–8. doi: 10.1109/AERO.2008.4526559.
- [78] L. B. Kreuzer, N. D. Kenyon, and C. K. Patel, "Air pollution: sensitive detection of ten pollutant gases by carbon monoxide and carbon dioxide lasers," *Science*, vol. 177, no. 4046, pp. 347–349, Jul. 1972, doi: 10.1126/science.177.4046.347.
- [79] D. D. Evans and D. W. Stroup, "Methods to Calculate the Response Time of Heat and Smoke Detectors Installed Below Large Unobstructed Ceilings," *NIST*, Jul. 1985, Accessed: Mar. 01, 2023. [Online]. Available: <https://www.nist.gov/publications/methods-calculate-response-time-heat-and-smoke-detectors-installed-below-large>
- [80] J. Yun and S.-S. Lee, "Human Movement Detection and Identification Using Pyroelectric Infrared Sensors," *Sensors*, vol. 14, no. 5, Art. no. 5, May 2014, doi: 10.3390/s140508057.
- [81] W. W. Coffeen, "Barium titanate ceramic dielectrics," US2789061A, Apr. 16, 1957 Accessed: Mar. 04, 2023. [Online]. Available: <https://patents.google.com/patent/US2789061/en>
- [82] R. B. Gray, "Transducer and method of making the same," US2486560A, Nov. 01, 1949 Accessed: Mar. 04, 2023. [Online]. Available: <https://patents.google.com/patent/US2486560A/en>
- [83] J. Osman, Y. Ishibashi, K.-H. Chew, D. R. Tilley, and J. F. Webb, "Nonlinear optics of ferroelectrics," *Ferroelectrics*, vol. 230, no. 1, pp. 215–220, May 1999, doi: 10.1080/00150199908214921.
- [84] E. D. Mishina, "Nonlinear Optics of Ferroelectrics: Towards Nanometers and Picoseconds," *Ferroelectrics*, vol. 314, no. 1, pp. 57–72, Jun. 2005, doi: 10.1080/00150190590926102.
- [85] C. Enderlein *et al.*, "Superconductivity mediated by polar modes in ferroelectric metals," *Nat. Commun.*, vol. 11, no. 1, Art. no. 1, Sep. 2020, doi: 10.1038/s41467-020-18438-0.
- [86] K. Ueno *et al.*, "Electric-field-induced superconductivity in an insulator," *Nat. Mater.*, vol. 7, no. 11, Art. no. 11, Nov. 2008, doi: 10.1038/nmat2298.
- [87] H. Schmid, "Multi-ferroic magnetoelectrics," *Ferroelectrics*, vol. 162, no. 1, pp. 317–338, Jan. 1994, doi: 10.1080/00150199408245120.
- [88] W. Eerenstein, N. D. Mathur, and J. F. Scott, "Multiferroic and magnetoelectric materials," *Nature*, vol. 442, no. 7104, pp. 759–765, Aug. 2006, doi: 10.1038/nature05023.
- [89] A. Blázquez-Castro, A. García-Cabañes, and M. Carrascosa, "Biological applications of ferroelectric materials," *Appl. Phys. Rev.*, vol. 5, no. 4, p. 041101, Dec. 2018, doi: 10.1063/1.5044472.
- [90] S. C. Mbisike, L. Eckart, J. W. Phair, P. Lomax, and R. Cheung, "Amplification of pyroelectric device with WSe<sub>2</sub> field effect transistor and ferroelectric gating," *J. Appl. Phys.*, vol. 131, no. 14, p. 144101, Apr. 2022, doi: 10.1063/5.0086216.
- [91] P.-C. Shen, C. Lin, H. Wang, K. H. Teo, and J. Kong, "Ferroelectric memory field-effect transistors using CVD monolayer MoS<sub>2</sub> as resistive switching channel," *Appl. Phys. Lett.*, vol. 116, no. 3, p. 033501, Jan. 2020, doi: 10.1063/1.5129963.

## 8. References

- [92] S. Roundy and P. K. Wright, "A piezoelectric vibration based generator for wireless electronics," *Smart Mater. Struct.*, vol. 13, no. 5, pp. 1131–1142, Oct. 2004, doi: 10.1088/0964-1726/13/5/018.
- [93] M. Renaud, P. Fiorini, R. van Schaijk, and C. van Hoof, "Harvesting energy from the motion of human limbs: the design and analysis of an impact-based piezoelectric generator," *Smart Mater. Struct.*, vol. 18, no. 3, p. 035001, Mar. 2009, doi: 10.1088/0964-1726/18/3/035001.
- [94] S.-T. Ho and S.-J. Jan, "A piezoelectric motor for precision positioning applications," *Precis. Eng.*, vol. 43, pp. 285–293, Jan. 2016, doi: 10.1016/j.precisioneng.2015.08.007.
- [95] S. K. T. Ravindran, T. Huesgen, M. Kroener, and P. Woias, "A self-sustaining micro thermomechanic-pyroelectric generator," *Appl. Phys. Lett.*, vol. 99, no. 10, p. 104102, Sep. 2011, doi: 10.1063/1.3633350.
- [96] C. Chen and J. Hone, "Graphene nanoelectromechanical systems," *Proc. IEEE*, vol. 101, no. 7, pp. 1766–1779, Jul. 2013, doi: 10.1109/JPROC.2013.2253291.
- [97] E. Benes, M. Gröschl, W. Burger, and M. Schmid, "Sensors based on piezoelectric resonators," *Sens. Actuators Phys.*, vol. 48, no. 1, pp. 1–21, May 1995, doi: 10.1016/0924-4247(95)00846-2.
- [98] C.-C. Hsiao, K.-Y. Huang, and Y.-C. Hu, "Fabrication of a ZnO Pyroelectric Sensor," *Sensors*, vol. 8, no. 1, Art. no. 1, Jan. 2008, doi: 10.3390/s8010185.
- [99] C. C. Chang and C. S. Tang, "An integrated pyroelectric infrared sensor with a PZT thin film," *Sens. Actuators Phys.*, vol. 65, no. 2, pp. 171–174, Mar. 1998, doi: 10.1016/S0924-4247(97)01663-4.
- [100] L. B. Kreuzer, N. D. Kenyon, and C. K. N. Patel, "Air Pollution: Sensitive Detection of Ten Pollutant Gases by Carbon Monoxide and Carbon Dioxide Lasers," *Science*, vol. 177, no. 4046, pp. 347–349, Jul. 1972, doi: 10.1126/science.177.4046.347.
- [101] M. Kohli *et al.*, "Pyroelectric thin-film sensor array," *Sens. Actuators Phys.*, vol. 60, no. 1–3, pp. 147–153, 1997.
- [102] S. A. Pullano, S. K. Islam, and A. S. Fiorillo, "Pyroelectric Sensor for Temperature Monitoring of Biological Fluids in Microchannel Devices," *IEEE Sens. J.*, vol. 14, no. 8, pp. 2725–2730, Aug. 2014, doi: 10.1109/JSEN.2014.2315738.
- [103] T. Mikolajick, U. Schroeder, and S. Slesazeck, "The Past, the Present, and the Future of Ferroelectric Memories," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1434–1443, Apr. 2020, doi: 10.1109/TED.2020.2976148.
- [104] K. A. Vorotilov and A. S. Sigov, "Ferroelectric memory," *Phys. Solid State*, vol. 54, no. 5, pp. 894–899, May 2012, doi: 10.1134/S1063783412050460.
- [105] X. Liang, Z. Fu, and S. Y. Chou, "Graphene Transistors Fabricated via Transfer-Printing In Device Active-Areas on Large Wafer," *Nano Lett.*, vol. 7, no. 12, pp. 3840–3844, Dec. 2007, doi: 10.1021/nl072566s.
- [106] Z. Li *et al.*, "Layer Control of WSe<sub>2</sub> via Selective Surface Layer Oxidation," *ACS Nano*, vol. 10, no. 7, pp. 6836–6842, Jul. 2016, doi: 10.1021/acsnano.6b02488.
- [107] M. Yamamoto *et al.*, "Self-Limiting Layer-by-Layer Oxidation of Atomically Thin WSe<sub>2</sub>," *Nano Lett.*, vol. 15, no. 3, pp. 2067–2073, Mar. 2015, doi: 10.1021/nl5049753.
- [108] R. Eason, *Pulsed Laser Deposition of Thin Films: Applications-Led Growth of Functional Materials*, 1. Aufl. Hoboken: Wiley-Interscience, 2007.
- [109] null Chen *et al.*, "Accelerated expansion of laser-ablated materials near a solid surface," *Phys. Rev. Lett.*, vol. 75, no. 25, pp. 4706–4709, Dec. 1995, doi: 10.1103/PhysRevLett.75.4706.
- [110] S. Seo, *Private communication*. Gwangju Institute of Science and Technology, korea, 2019.

## 8. References

- [111] Gustavo Morari do Nascimento, *Raman Spectroscopy*. IntechOpen, 2018.
- [112] D. A. Long, *Raman spectroscopy*. New York: McGraw-Hill, 1977.
- [113] “Raman spectroscopy,” *Wikipedia*. Aug. 05, 2021. Accessed: Aug. 13, 2021. [Online]. Available:  
[https://en.wikipedia.org/w/index.php?title=Raman\\_spectroscopy&oldid=1037307328](https://en.wikipedia.org/w/index.php?title=Raman_spectroscopy&oldid=1037307328)
- [114] S.-L. Li, H. Miyazaki, H. Song, H. Kuramochi, S. Nakaharai, and K. Tsukagoshi, “Quantitative Raman Spectrum and Reliable Thickness Identification for Atomic Layers on Insulating Substrates,” *ACS Nano*, vol. 6, no. 8, pp. 7381–7388, Aug. 2012, doi: 10.1021/nn3025173.
- [115] S. Bertolazzi, S. Bonacchi, G. Nan, A. Pershin, D. Beljonne, and P. Samorì, “Engineering Chemically Active Defects in Monolayer MoS<sub>2</sub> Transistors via Ion-Beam Irradiation and Their Healing via Vapor Deposition of Alkanethiols,” *Adv. Mater.*, vol. 29, no. 18, p. 1606760, 2017, doi: 10.1002/adma.201606760.
- [116] D.-H. Kang *et al.*, “Controllable Nondegenerate p-Type Doping of Tungsten Diselenide by Octadecyltrichlorosilane,” *ACS Nano*, vol. 9, no. 2, pp. 1099–1107, Feb. 2015, doi: 10.1021/nn5074435.
- [117] H. Zhou *et al.*, “Thickness-dependent patterning of MoS<sub>2</sub> sheets with well-oriented triangular pits by heating in air,” *Nano Res.*, vol. 6, Oct. 2013, doi: 10.1007/s12274-013-0346-2.
- [118] S. C. Mbisike, S. Seo, S. Lee, J. Phair, and R. Cheung, “Parametric study of pulsed laser deposited (PLD) WSe<sub>2</sub> 2D transistors,” *Microelectron. Eng.*, vol. 230, p. 111368, Jun. 2020, doi: 10.1016/j.mee.2020.111368.
- [119] S. Perkowitz, *Optical characterization of semiconductors: infrared, Raman, and photoluminescence spectroscopy*. London ; Academic Press, 1993.
- [120] A. M. Jones *et al.*, “Title: Optical Generation of Excitonic Valley Coherence in Monolayer WSe<sub>2</sub>”.
- [121] K. F. Mak *et al.*, “Tightly bound trions in monolayer MoS<sub>2</sub>,” *Nat. Mater.*, vol. 12, no. 3, Art. no. 3, Mar. 2013, doi: 10.1038/nmat3505.
- [122] Y. Li, W. Parkes, L. I. Haworth, A. W. S. Ross, J. T. M. Stevenson, and A. J. Walton, “Room-Temperature Fabrication of Anodic Tantalum Pentoxide for Low-Voltage Electrowetting on Dielectric (EWOD),” *J. Microelectromechanical Syst.*, vol. 17, no. 6, pp. 1481–1488, Dec. 2008, doi: 10.1109/JMEMS.2008.2006827.
- [123] L. Young, “The determination of the thickness, dielectric constant, and other properties of anodic oxide films on tantalum from the interference colours,” *Proc. R. Soc. Lond. Ser. Math. Phys. Sci.*, vol. 244, no. 1236, pp. 41–53, Feb. 1958, doi: 10.1098/rspa.1958.0024.
- [124] H. Zhao, W. Ren, and L. Xuesen, “Design and fabrication of micromachined pyroelectric infrared detector array using lead titanate zirconate (PZT) thin film,” 2017, doi: 10.1016/J.CERAMINT.2017.05.205.
- [125] T. M. Kamel, “Poling and switching of PZT ceramics: field and grain size effects,” Technische Universiteit Eindhoven, 2007. Accessed: Aug. 13, 2021. [Online]. Available: <https://www.narcis.nl/publication/RecordID/oai:pure.tue.nl:publications%2Ffa0faa8d-4847-4c6a-afaf-315e8dcd7e64>
- [126] S. Seo, *Private communication*. Gwangju Institute of Science and Technology, Korea, 2019.
- [127] S.-P. Ko *et al.*, “Capacitance–voltage analysis of electrical properties for WSe<sub>2</sub> field effect transistors with high- $\kappa$  encapsulation layer,” *Nanotechnology*, vol. 29, no. 6, p. 065703, Jan. 2018, doi: 10.1088/1361-6528/aaa1d7.

## 8. References

- [128] Y. Li *et al.*, “Accurate identification of layer number for few-layer WS<sub>2</sub> and WSe<sub>2</sub> via spectroscopic study,” *Nanotechnology*, vol. 29, no. 12, p. 124001, Feb. 2018, doi: 10.1088/1361-6528/aaa923.
- [129] H. Li *et al.*, “From Bulk to Monolayer MoS<sub>2</sub>: Evolution of Raman Scattering,” *Adv. Funct. Mater.*, vol. 22, no. 7, pp. 1385–1390, 2012, doi: 10.1002/adfm.201102111.
- [130] A. Delhomme *et al.*, “Magneto-spectroscopy of exciton Rydberg states in a CVD grown WSe<sub>2</sub> monolayer,” *Appl. Phys. Lett.*, vol. 114, no. 23, p. 232104, Jun. 2019, doi: 10.1063/1.5095573.
- [131] S. Zhao *et al.*, “Strong room-temperature emission from defect states in CVD-grown WSe<sub>2</sub> nanosheets,” *Nano Res.*, vol. 11, no. 7, pp. 3922–3930, Jul. 2018, doi: 10.1007/s12274-018-1970-7.
- [132] H. Li *et al.*, “Mechanical Exfoliation and Characterization of Single- and Few-Layer Nanosheets of WSe<sub>2</sub>, TaS<sub>2</sub>, and TaSe<sub>2</sub>,” *Small*, vol. 9, no. 11, pp. 1974–1981, 2013, doi: 10.1002/sml.201202919.
- [133] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, and S. Ryu, “Anomalous Lattice Vibrations of Single- and Few-Layer MoS<sub>2</sub>,” *ACS Nano*, vol. 4, no. 5, pp. 2695–2700, May 2010, doi: 10.1021/nn1003937.
- [134] S. Seo *et al.*, “Growth of Centimeter-Scale Monolayer and Few-Layer WSe<sub>2</sub> Thin Films on SiO<sub>2</sub>/Si Substrate via Pulsed Laser Deposition,” *Adv. Mater. Interfaces*, vol. 5, no. 20, p. 1800524, 2018, doi: 10.1002/admi.201800524.
- [135] S. C. Mbisike, S. Seo, S. Lee, J. Phair, and R. Cheung, “Parametric study of pulsed laser deposited (PLD) WSe<sub>2</sub> 2D transistors,” *Microelectron. Eng.*, vol. 230, p. 111368, Jun. 2020, doi: 10.1016/j.mee.2020.111368.
- [136] A. McCreary *et al.*, “Distinct photoluminescence and Raman spectroscopy signatures for identifying highly crystalline WS<sub>2</sub> monolayers produced by different growth methods,” *J. Mater. Res.*, vol. 31, no. 7, pp. 931–944, Apr. 2016, doi: 10.1557/jmr.2016.47.
- [137] M. Seki, K. Hachiya, and K. Yoshida, “Photoluminescence excitation process and optical absorption in Ge–S chalcogenide glasses,” *J. Non-Cryst. Solids*, vol. 324, no. 1, pp. 127–132, Aug. 2003, doi: 10.1016/S0022-3093(03)00226-6.
- [138] S. Najmaei *et al.*, “Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers,” *Nat. Mater.*, vol. 12, no. 8, Art. no. 8, Aug. 2013, doi: 10.1038/nmat3673.
- [139] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, “Electronics and optoelectronics of two-dimensional transition metal dichalcogenides,” *Nat. Nanotechnol.*, vol. 7, no. 11, Art. no. 11, Nov. 2012, doi: 10.1038/nnano.2012.193.
- [140] W. Zhao *et al.*, “Evolution of Electronic Structure in Atomically Thin Sheets of WS<sub>2</sub> and WSe<sub>2</sub>,” *ACS Nano*, vol. 7, no. 1, pp. 791–797, Jan. 2013, doi: 10.1021/nn305275h.
- [141] F. Xia, D. B. Farmer, Y. Lin, and P. Avouris, “Graphene Field-Effect Transistors with High On/Off Current Ratio and Large Transport Band Gap at Room Temperature,” *Nano Lett.*, vol. 10, no. 2, pp. 715–718, Feb. 2010, doi: 10.1021/nl9039636.
- [142] P. R. Pudasaini *et al.*, “High performance top-gated multilayer WSe<sub>2</sub> field effect transistors,” *Nanotechnology*, vol. 28, no. 47, Art. no. 47, Oct. 2017, doi: 10.1088/1361-6528/aa8081.
- [143] F. Schwierz, “Graphene transistors,” *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, Jul. 2010, doi: 10.1038/nnano.2010.89.
- [144] D. Akinwande, N. Petrone, and J. Hone, “Two-dimensional flexible nanoelectronics,” *Nat. Commun.*, vol. 5, no. 1, p. 5678, Dec. 2014, doi: 10.1038/ncomms6678.

## 8. References

- [145] M. Wasala, P. Patil, S. Ghosh, L. Weber, S. Lei, and S. Talapatra, "Role of Layer Thickness and Field-Effect Mobility on Photoresponsivity of Indium Selenide (InSe) Based Phototransistors," *ArXiv210200365 Cond-Mat Physicsphysics*, Jan. 2021, Accessed: Jan. 13, 2022. [Online]. Available: <http://arxiv.org/abs/2102.00365>
- [146] S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High Performance Multilayer MoS<sub>2</sub> Transistors with Scandium Contacts," *Nano Lett.*, vol. 13, no. 1, pp. 100–105, Jan. 2013, doi: 10.1021/nl303583v.
- [147] N. R. Pradhan *et al.*, "Hall and field-effect mobilities in few layered p-WSe<sub>2</sub> field-effect transistors," *Sci. Rep.*, vol. 5, no. 1, p. 8979, Mar. 2015, doi: 10.1038/srep08979.
- [148] M. C. Peignon, Ch. Cardinaud, and G. Turban, "Etching processes of tungsten in SF<sub>6</sub>O<sub>2</sub> radio-frequency plasmas," *J. Appl. Phys.*, vol. 70, no. 6, pp. 3314–3323, Sep. 1991, doi: 10.1063/1.350347.
- [149] S. S.M., *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1936.
- [150] H.-J. Chuang *et al.*, "Low-Resistance 2D/2D Ohmic Contacts: A Universal Approach to High-Performance WSe<sub>2</sub>, MoS<sub>2</sub>, and MoSe<sub>2</sub> Transistors," *Nano Lett.*, vol. 16, no. 3, pp. 1896–1902, Mar. 2016, doi: 10.1021/acs.nanolett.5b05066.
- [151] J. Singh, *Electronic and Optoelectronic Properties of Semiconductor Structures*. Cambridge: Cambridge University Press, 2003.
- [152] H. Ji *et al.*, "Tunable Mobility in Double-Gated MoTe<sub>2</sub> Field-Effect Transistor: Effect of Coulomb Screening and Trap Sites," *ACS Appl. Mater. Interfaces*, vol. 9, no. 34, pp. 29185–29192, Aug. 2017, doi: 10.1021/acsami.7b05865.
- [153] F. Chen, J. Xia, D. K. Ferry, and N. Tao, "Dielectric Screening Enhanced Performance in Graphene FET," *Nano Lett.*, vol. 9, no. 7, pp. 2571–2574, Jul. 2009, doi: 10.1021/nl900725u.
- [154] S.-L. Li *et al.*, "Thickness-Dependent Interfacial Coulomb Scattering in Atomically Thin Field-Effect Transistors," *Nano Lett.*, vol. 13, no. 8, pp. 3546–3552, Aug. 2013, doi: 10.1021/nl4010783.
- [155] K.-K. Kam, "Electrical properties of WSe<sub>2</sub>, WS<sub>2</sub>, MoSe<sub>2</sub>, MoS<sub>2</sub>, and their use as photoanodes in a semiconductor liquid junction solar cell," *Retrospect. Theses Diss.*, Jan. 1982, doi: <https://doi.org/10.31274/rtd-180813-7962>.
- [156] W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhrer, "High mobility ambipolar MoS<sub>2</sub> field-effect transistors: Substrate and dielectric effects," *Appl. Phys. Lett.*, vol. 102, no. 4, p. 042104, Jan. 2013, doi: 10.1063/1.4789365.
- [157] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-Performance Single Layered WSe<sub>2</sub> p-FETs with Chemically Doped Contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, Jul. 2012, doi: 10.1021/nl301702r.
- [158] Schroder and K. Dieter, *Semiconductor material and device characterization*. New York: Wiley, 1990.
- [159] R. Nouchi, T. Saito, and K. Tanigaki, "Observation of negative contact resistances in graphene field-effect transistors," *J. Appl. Phys.*, vol. 111, no. 8, p. 084314, Apr. 2012, doi: 10.1063/1.4705367.
- [160] P. Blake *et al.*, "Influence of metal contacts and charge inhomogeneity on transport properties of graphene near the neutrality point," *Solid State Commun.*, vol. 149, no. 27–28, pp. 1068–1071, Jul. 2009, doi: 10.1016/j.ssc.2009.02.039.
- [161] R. Nouchi, T. Saito, and K. Tanigaki, "Determination of Carrier Type Doped from Metal Contacts to Graphene by Channel-Length-Dependent Shift of Charge Neutrality Points," *Appl. Phys. Express*, vol. 4, no. 3, p. 035101, Feb. 2011, doi: 10.1143/APEX.4.035101.

## 8. References

- [162] K. Yim *et al.*, “Novel high- $\kappa$  dielectrics for next-generation electronic devices screened by automated ab initio calculations,” *NPG Asia Mater.*, vol. 7, no. 6, Art. no. 6, Jun. 2015, doi: 10.1038/am.2015.57.
- [163] M. Schulz, “The end of the road for silicon?,” *Nature*, vol. 399, no. 6738, Art. no. 6738, Jun. 1999, doi: 10.1038/21526.
- [164] S. Ezhilvalavan and T. Y. Tseng, “Preparation and properties of tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) thin films for ultra large scale integrated circuits (ULSIs) application – A review,” *J. Mater. Sci. Mater. Electron.*, vol. 10, no. 1, Art. no. 1, Mar. 1999, doi: 10.1023/A:1008970922635.
- [165] C. Chaneliere, J. L. Autran, R. A. B. Devine, and B. Balland, “Tantalum pentoxide ( $\text{Ta}_2\text{O}_5$ ) thin films for advanced dielectric applications,” *Mater. Sci. Eng. R Rep.*, vol. 22, no. 6, Art. no. 6, May 1998, doi: 10.1016/S0927-796X(97)00023-5.
- [166] S. Kim *et al.*, “High-mobility and low-power thin-film transistors based on multilayer  $\text{MoS}_2$  crystals,” *Nat. Commun.*, vol. 3, no. 1, Art. no. 1, Aug. 2012, doi: 10.1038/ncomms2018.
- [167] L. Young, “Anodization constants for tantalum,” *J Electrochem Soc U. S.*, vol. 124:4, Apr. 1977, doi: 10.1149/1.2133341.
- [168] M. Kutz, *Handbook of Environmental Degradation of Materials*. San Diego: Elsevier Science & Technology Books, 2018.
- [169] N. Novkovski and E. Atanassova, “A comprehensive model for the I–V characteristics of metal- $\text{Ta}_2\text{O}_5/\text{SiO}_2$ -Si structures,” 2006, doi: 10.1007/S00339-006-3567-3.
- [170] E. Atanassova, N. Novkovski, A. Paskaleva, and M. Pecovska-Gjorgjevich, “Oxygen annealing modification of conduction mechanism in thin rf sputtered  $\text{Ta}_2\text{O}_5$  on Si,” *Solid-State Electron.*, vol. 46, no. 11, pp. 1887–1898, Nov. 2002, doi: 10.1016/S0038-1101(02)00134-X.
- [171] M. Bai, Y. Zhao, S. Xu, T. Tang, and Y. Guo, “Asymmetric bias-induced barrier lowering as an alternative origin of current rectification in geometric diodes,” *Commun. Phys.*, vol. 4, no. 1, p. 236, Dec. 2021, doi: 10.1038/s42005-021-00735-9.
- [172] S. M. Sze and M. K. Lee, *Semiconductor Devices : Physics and Technology*, 3rd edition. Singapore: Wiley, 2013.
- [173] O. Kerrec, D. Devilliers, H. Groult, and M. Chemla, “Dielectric properties of anodic oxide films on tantalum,” *Electrochimica Acta*, vol. 40, no. 6, pp. 719–724, Apr. 1995, doi: 10.1016/0013-4686(94)00330-4.
- [174] T.-C. Cheng and C.-C. Chou, “The Electrical and Mechanical Properties of Porous Anodic 6061-T6 Aluminum Alloy Oxide Film,” *J. Nanomater.*, vol. 2015, pp. 1–5, 2015, doi: 10.1155/2015/371405.
- [175] M. A. Mohammed and D. V. Morgan, “Reliability of tantalum oxide film capacitors,” *Phys. Status Solidi A*, vol. 115, no. 1, Art. no. 1, 1989, doi: 10.1002/pssa.2211150123.
- [176] M. Mibus, C. Jensen, X. Hu, C. Knospe, M. L. Reed, and G. Zangari, “Dielectric breakdown and failure of anodic aluminum oxide films for electrowetting systems,” *J. Appl. Phys.*, vol. 114, no. 1, p. 014901, Jul. 2013, doi: 10.1063/1.4812395.
- [177] F.-C. Chiu, “A Review on Conduction Mechanisms in Dielectric Films,” *Adv. Mater. Sci. Eng.*, vol. 2014, p. e578168, Feb. 2014, doi: 10.1155/2014/578168.
- [178] A. K. Jonscher, “Dielectric relaxation in solids,” *J. Phys. Appl. Phys.*, vol. 32, no. 14, pp. R57–R70, 1999, doi: 10.1088/0022-3727/32/14/201.
- [179] S. Kimura, Y. Nishioka, A. Shintani, and K. Mukai, “Leakage-Current Increase in Amorphous  $\text{Ta}_2\text{O}_5$  Films Due to Pinhole Growth during Annealing Below 600 °C,” 1983, doi: 10.1149/1.2119599.

## 8. References

- [180] G. F. Alapatt, W. R. Harrell, Y. Freeman, and P. Lessner, "Observation of the Poole-Frenkel effect in Tantalum Polymer capacitors," *Proc. IEEE SoutheastCon 2010 SoutheastCon*, 2010, doi: 10.1109/SECON.2010.5453820.
- [181] E. Atanassova and A. Paskaleva, "Breakdown fields and conduction mechanisms in thin Ta<sub>2</sub>O<sub>5</sub> layers on Si for high density DRAMs," *Microelectron. Reliab.*, vol. 42, no. 2, pp. 157–173, Feb. 2002, doi: 10.1016/S0026-2714(01)00248-7.
- [182] N. Oliva, E. A. Casu, M. Cavalieri, and A. M. Ionescu, "Double gate n-type WSe<sub>2</sub> FETs with high- $\kappa$  top gate dielectric and enhanced electrostatic control," in *2018 48th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2018, pp. 114–117. doi: 10.1109/ESSDERC.2018.8486867.
- [183] S. G. Byeon and Y. Tzeng, "Charge trapping/generation and reliability for high-performance tantalum oxide capacitors," *J. Appl. Phys.*, vol. 66, no. 10, pp. 4837–4842, Nov. 1989, doi: 10.1063/1.343799.
- [184] U. Sassi *et al.*, "Graphene-based mid-infrared room-temperature pyroelectric bolometers with ultrahigh temperature coefficient of resistance," *Nat. Commun.*, vol. 8, p. 14311, Jan. 2017, doi: 10.1038/ncomms14311.
- [185] H. Fang *et al.*, "Infrared light gated MoS<sub>2</sub> field effect transistor," *Opt. Express*, vol. 23, no. 25, pp. 31908–31914, Dec. 2015, doi: 10.1364/OE.23.031908.
- [186] R. Bruchhaus, D. Pitzer, R. Primig, M. Schreiter, and W. Wersing, "Sputtering of PZT thin films for surface micromachined IR-detector arrays," *Integr. Ferroelectr.*, vol. 25, no. 1–4, pp. 1–11, Sep. 1999, doi: 10.1080/10584589908210154.
- [187] C. Zhou *et al.*, "Low voltage and high ON/OFF ratio field-effect transistors based on CVD MoS<sub>2</sub> and ultra high- $\kappa$  gate dielectric PZT," *Nanoscale*, vol. 7, no. 19, pp. 8695–8700, May 2015, doi: 10.1039/C5NR01072A.
- [188] Y.-J. Kang, J. Kang, and K. J. Chang, "Electronic structure of graphene and doping effect on SiO<sub>2</sub>," *Phys. Rev. B*, vol. 78, no. 11, p. 115404, Sep. 2008, doi: 10.1103/PhysRevB.78.115404.
- [189] W. Gao, P. Xiao, G. Henkelman, K. M. Liechti, and R. Huang, "Interfacial adhesion between graphene and silicon dioxide by density functional theory with van der Waals corrections," *J. Phys. Appl. Phys.*, vol. 47, no. 25, p. 255301, Jun. 2014, doi: 10.1088/0022-3727/47/25/255301.
- [190] Pyreos Limited, "Image from Pyreos Limited." 2019.
- [191] J. Joseph, T. M. Vimala, V. Sivasubramanian, and V. R. K. Murthy, "Structural investigations on Pb(Zr<sub>x</sub>Ti<sub>1-x</sub>)O<sub>3</sub> solid solutions using the X-ray Rietveld method," *J. Mater. Sci.*, vol. 35, no. 6, pp. 1571–1575, Mar. 2000, doi: 10.1023/A:1004778223721.
- [192] R. Köhler, N. Neumann, N. Heß, R. Bruchhaus, W. Wersing, and M. Simon, "Pyroelectric devices based on sputtered PZT thin films," *Ferroelectrics*, vol. 201, no. 1, Art. no. 1, Sep. 1997, doi: 10.1080/00150199708228356.
- [193] Y. Yang, S. Wang, Y. Zhang, and Z. L. Wang, "Pyroelectric Nanogenerators for Driving Wireless Sensors," *Nano Lett.*, vol. 12, no. 12, pp. 6408–6413, Dec. 2012, doi: 10.1021/nl303755m.
- [194] R. Köhler, N. Neumann, N. Heß, R. Bruchhaus, W. Wersing, and M. Simon, "Pyroelectric devices based on sputtered PZT thin films," *Ferroelectrics*, vol. 201, no. 1, pp. 83–92, Sep. 1997, doi: 10.1080/00150199708228356.
- [195] Z. Lu *et al.*, "Nonvolatile MoS<sub>2</sub> field effect transistors directly gated by single crystalline epitaxial ferroelectric," *Appl. Phys. Lett.*, vol. 111, no. 2, p. 023104, Jul. 2017, doi: 10.1063/1.4992113.

## 8. References

- [196] R. Singh and M. Parashar, “Origin of Hysteresis in Perovskite Solar Cells,” in *Soft-Matter Thin Film Solar Cells*, AIP Publishing LLC, 2020, pp. 1-1-1–42. doi: 10.1063/9780735422414\_001.
- [197] D. H. Song *et al.*, “A discussion on the origin and solutions of hysteresis in perovskite hybrid solar cells,” *J. Phys. Appl. Phys.*, vol. 49, no. 47, p. 473001, Nov. 2016, doi: 10.1088/0022-3727/49/47/473001.
- [198] Y. Xu, *Ferroelectric Materials and Their Applications*. Amsterdam: Elsevier Science & Technology, 1991.
- [199] C. Quarti, E. Mosconi, and F. De Angelis, “Interplay of Orientational Order and Electronic Structure in Methylammonium Lead Iodide: Implications for Solar Cell Operation,” *Chem. Mater.*, vol. 26, no. 22, pp. 6557–6569, Nov. 2014, doi: 10.1021/cm5032046.
- [200] Y. Wang *et al.*, “Trap-limited charge recombination in intrinsic perovskite film and meso-superstructured perovskite solar cells and the passivation effect of the hole-transport material on trap states,” *Phys. Chem. Chem. Phys.*, vol. 17, no. 44, pp. 29501–29506, Nov. 2015, doi: 10.1039/C5CP04360C.
- [201] X.-W. Zhang *et al.*, “MoS<sub>2</sub> Field-Effect Transistors With Lead Zirconate-Titanate Ferroelectric Gating,” *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 784–786, Aug. 2015, doi: 10.1109/LED.2015.2440249.

# Appendix A – Run sheet of WSe<sub>2</sub> FET fabrication – Chapter 4

## Thermal oxidation

Step	Description	Equipment	Process Parameters	Results/Comments
1	Pre-clean	Wet deck	10 DI : 1 HF : 1 HCL for 30 secs; DI rinse	
2	IPA dry	Maragoni Dryer	45 min	
3	Dry thermal oxide	Furnace 1	SiO <sub>2</sub> 300 nm, Recipe: 3 DRYOX14 (1100°C) 4 h 25 min (total process time ~7.5 h)	
4	Measure thickness	Nanospec 3000	Prog 1 Oxide on Silicon	

## Back side etch

Step	Description	Equipment	Process Parameters	Results/Comments
5	Spin photoresist (PR)	SVG	9,8,1; Manual dispense SPR 220 Hard baking 110°C * 5min	
6	Remove Oxide	Wet deck	Soaked in BHF (7:1) × 4:25 min ~12 nm/min	
7	Sputter Metal	OPT Plasma System 400	Ti 100 nm (Al will react with MF-26A developer)	

## Wafer dicing

Step	Description	Equipment	Process Parameters	Results/Comments
8	Wafer Dicing	Dicer	10.3 × 10.3 mm <sup>2</sup>	
9	Remove PR	Wet Deck	1165 NMP (2 hr in bath) + IPA + DI	
10	Remove PR residue	Electrotech 508 Barrel Asher	30 min	

## Appendices

### 2D Material on chip

Step	Description	Equipment	Process Parameters	Results/Comments
11	Transfer MoS <sub>2</sub> /WSe <sub>2</sub>	Manual	O <sub>2</sub> plasma 15 min; Scotch tape (Heat 40 °C for 3 min on hotplate)	
12	Inspect flakes	Microscope		
13a	Remove tape residue	Heraeus VT 5050 oven	1165 NMP 70 °C × 2~3 h	NMP 75 °C × 30 min works for residue on flakes
b		Wet Deck	Immerse in Acetone (2h) + Rinse IPA + DI	

### 2D Material patterning

Step	Description	Equipment	Process Parameters	Results/Comments
14	<i>Lithography 1</i>	Polo spinner	SPR350 1.35 µm; Prog 48: 700 rpm × 10 s, 4500 rpm × 1 min, Acc 1000; Soft bake: 90 °C × 1 min	4000 rpm gives 1.55 µm
15	Exposure	DMO ML 3	Dose: 68 mJ/cm <sup>2</sup> , PEB 110 °C × 1 min	
16	Develop	Manual	MF 26A for < 40 Secs	Inspect under microscope
17	Etch WSe <sub>2</sub>	MEMSSTAR	XeF <sub>2</sub> 2 min + 1 min.....	Inspect visually and stop process if required
18	Remove tape residue	Electrotech 508 Barrel Asher	O <sub>2</sub> plasma×5 min	
19	Remove PR	Wet Deck	1165 NMP 70 °C × 2~3 h	

### Metal deposition

Step	Description	Equipment	Process Parameters	Results/Comments
------	-------------	-----------	--------------------	------------------

## Appendices

20	<i>Lithography 2</i>	Polo spinner	AZ2035 3.5 $\mu\text{m}$ ; Prog 29: 700 rpm $\times$ 10 s, 4000 rpm $\times$ 1 min, Acc 1000; Soft bake 90 $^{\circ}\text{C}$ $\times$ 5 min	
21	Exposure	DMO ML 3	Dose: 275 mJ/cm <sup>2</sup> , PEB 110 $^{\circ}\text{C}$ $\times$ 1 min	
22	Develop	Manual	AZ Developer $\times$ 1 min + 30 sec + DI rinse	Inspect under microscope
23	E-beam Evaporation	ANS	Ti 10 nm+ Al 300 nm	
24	Lift off	Wet deck	1165 NMP at 70 $^{\circ}\text{C}$ $\times$ 2 h	Use ultrasonic if required
25	Post-clean	Wet deck	IPA + DI rinse	Inspect under microscope

## Appendix B – Run sheet of anodic tantalum production and capacitor fabrication – Chapter 5

### Anodization

Step	Description	Equipment	Process Parameters	Results/Comments
1	Sputter	OPT Plasma lab System 400	500 nm	Ta
2	O <sub>2</sub> clean	Electrotech 508 Barrel Asher	10 mins	
3	Anodization	Electrolytic gel; Voltage source	10 V for 1 hr	~ 20 nm of tantalum anodized

### Metal deposition

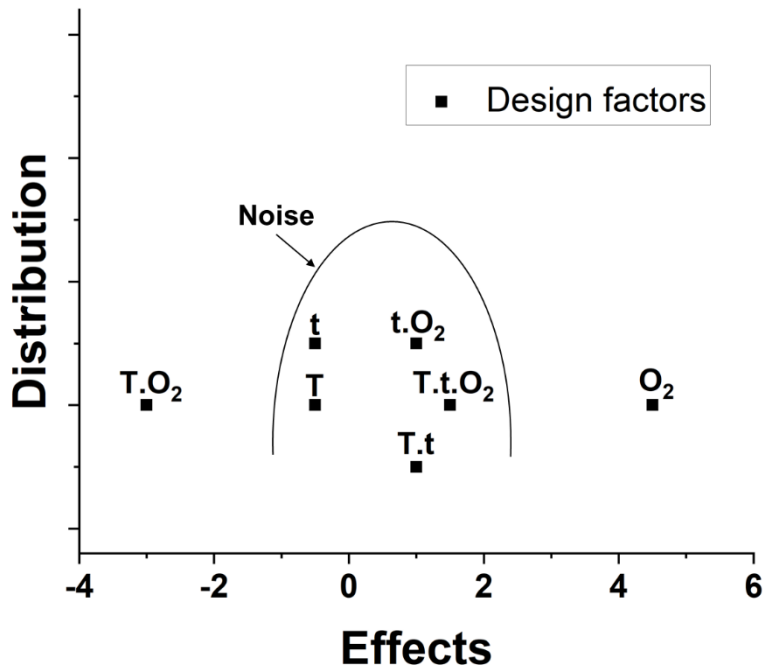
Step	Description	Equipment	Process Parameters	Results/Comments
4	Spin PR	Polos spinner	AZ2035 3.5 $\mu\text{m}$ ; Prog 29: 700 rpm $\times$ 10 s, 4000 rpm $\times$ 1 min, Acc 1000; Soft bake 90 $^{\circ}\text{C}$ $\times$ 5 min	
5	<i>Lithography 1</i>	DMO ML 3	Dose: 275 mJ/cm <sup>2</sup> , PEB 110 $^{\circ}\text{C}$ $\times$ 1 min	
6	Develop	Manual	AZ Developer $\times$ 1 min+30 sec +DI rinse	Unmount chips
7	Sputter	OPT Plasma lab System 400	Al 100 nm	
8	Lift off	Wet deck 2	1165 NMP at 70 $^{\circ}\text{C}$ $\times$ 2 h	Use ultrasonic if required
9	Post-clean	Wet deck	IPA + DI rinse	Inspect under microscope

## Appendix C - Full factorial computation

**Table A.1:** Data from  $2^3$  full factorial computation

$T$	$t$	$O_2$	$Y$	(1)	(2)	(3)	Div	Effect	ID	$\hat{Y}$	$r = (Y - \hat{Y})$
-1	-1	-1	2	7	11	40	8	5	Avg	1.5	0.5
+1	-1	-1	5	4	29	-2	4	-0.5	T	4	1
-1	+1	-1	1	14	5	-2	4	-0.5	t	1.5	-0.5
+1	+1	-1	3	15	-7	4	4	1	T*t	4	-1
-1	-1	+1	10	3	-3	18	4	4.5	$O_2$	9	1
+1	-1	+1	4	2	1	-12	4	-3	$T*O_2$	5.5	-1.5
-1	+1	+1	8	-6	-1	4	4	1	$t*O_2$	9	-1
+1	+1	+1	7	-1	5	6	4	1.5	$T*t*O_2$	5.5	1.5

The data contained in Table A.1 have been computed for the  $2^3$  factorial design. The column  $Y$  represents the concentration of flakes from the different design inputs. The number of WSe<sub>2</sub> flakes observed on the substrate have been used to rank  $Y$ . Columns (1), has been computed by adding two rows of the  $Y$  resulting in a total of four additions which occupy the first four rows of column (1). The last four rows of column (1) have been realised by subtracting the rows in column  $Y$ . Using this system, the other columns (2) and (3) have been filled. The *effect* field has been computed by dividing the values in column (3) and field *Div*. From the field *effect*, a line plot (Fig A.1) has been drawn with the aim of determining the design factors that have had the most impact in resolving the adhesion between the WSe<sub>2</sub> and PZT.



**Figure A.1:** Line plot of effects

### $\hat{Y}$ Model

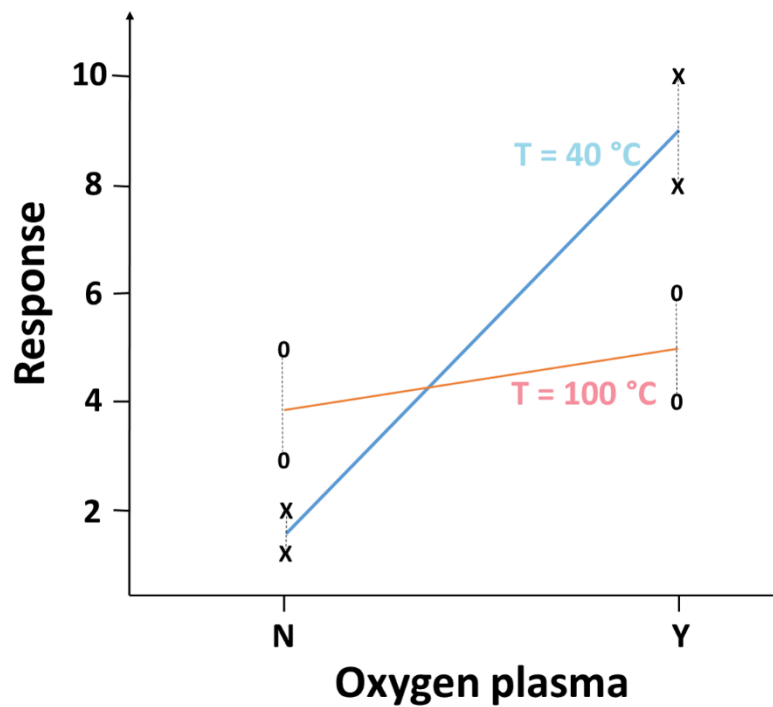
From the line plot in Fig A.1, T.O<sub>2</sub> and O<sub>2</sub> have been confirmed to be the most effective factors. Hence, a model has been deduced to calculate the inverse response of the design factors. The model is shown in Eq. (A.1):

$$\hat{Y} = \text{Avg} + \frac{a1.T}{2} + \frac{a3.O_2}{2} + \frac{a5.T.O_2}{2} \quad \text{Eq. (A.1)}$$

Insert the values from the *effect* column from Table A.1 into Eq. (A.1)

$$\hat{Y} = 5 - 0.25T + 2.25O_2 - 1.5T.O_2 \quad \text{Eq. (A.2)}$$

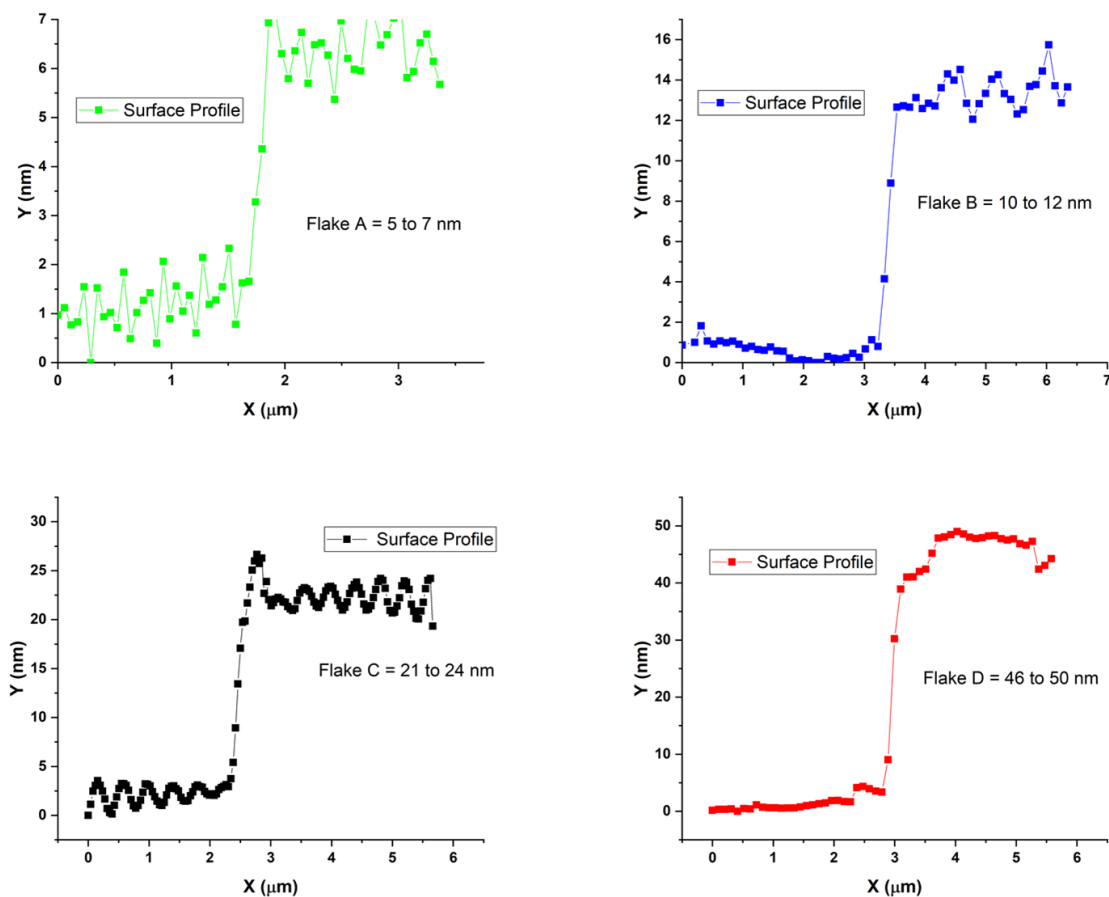
The inverse response enables us to calculate the residue of the 2<sup>3</sup> factorial design. The sum of the values in the *residue* (r) column equals zero, indicating that our computation has no error.



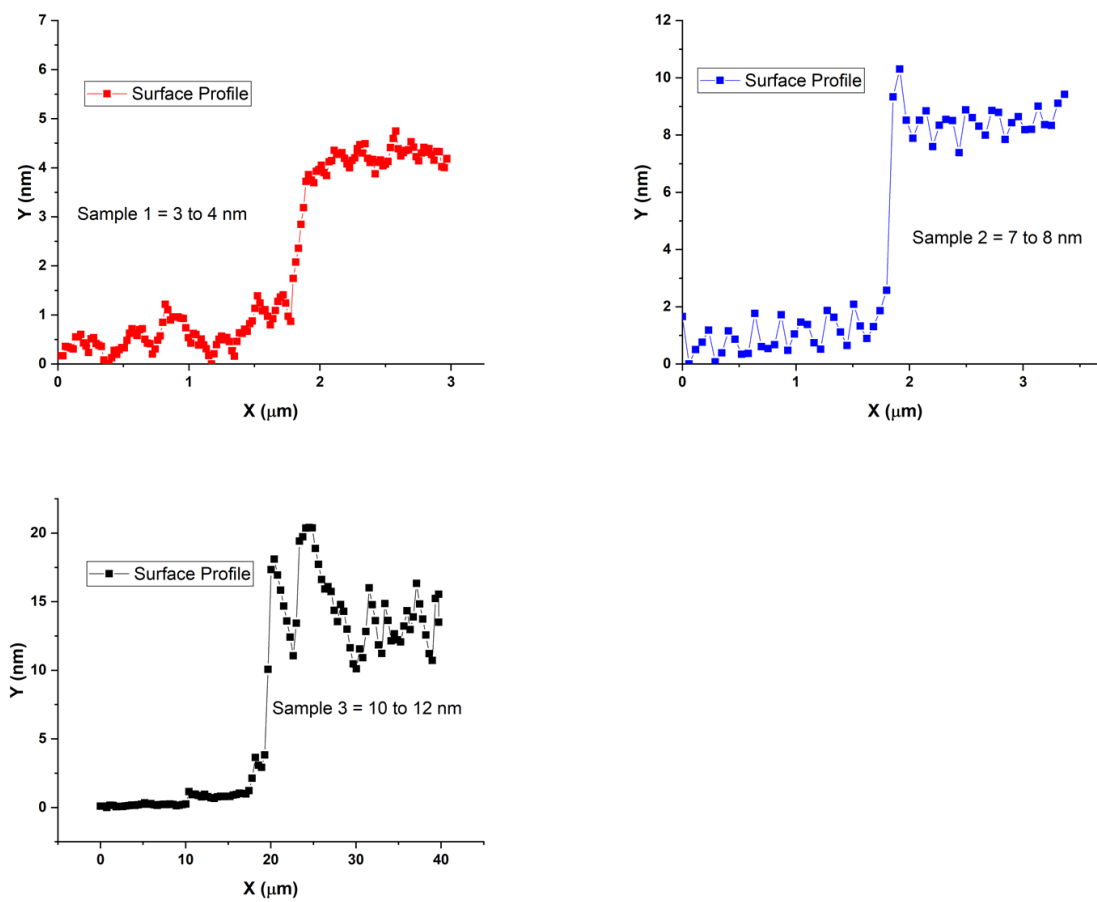
**Figure A.2:** Interaction plot of the design *effects*

An interaction plot has been drawn in Fig A.2. The interaction plot shows the dependence of the design factor temperature on the oxygen plasma. In the absence of oxygen plasma, an increased temperature creates a higher response. However, in the presence of oxygen plasma, a lower temperature creates a higher response. Based on this, the selected parameters are  $T = 40\text{ }^{\circ}\text{C}$ ,  $t = 40\text{ secs}$ , and  $O_2 = Y$  with oxygen plasma being the most significant factor.

## Appendix D – AFM Graphs (X-WSe<sub>2</sub> and PLD WSe<sub>2</sub>)

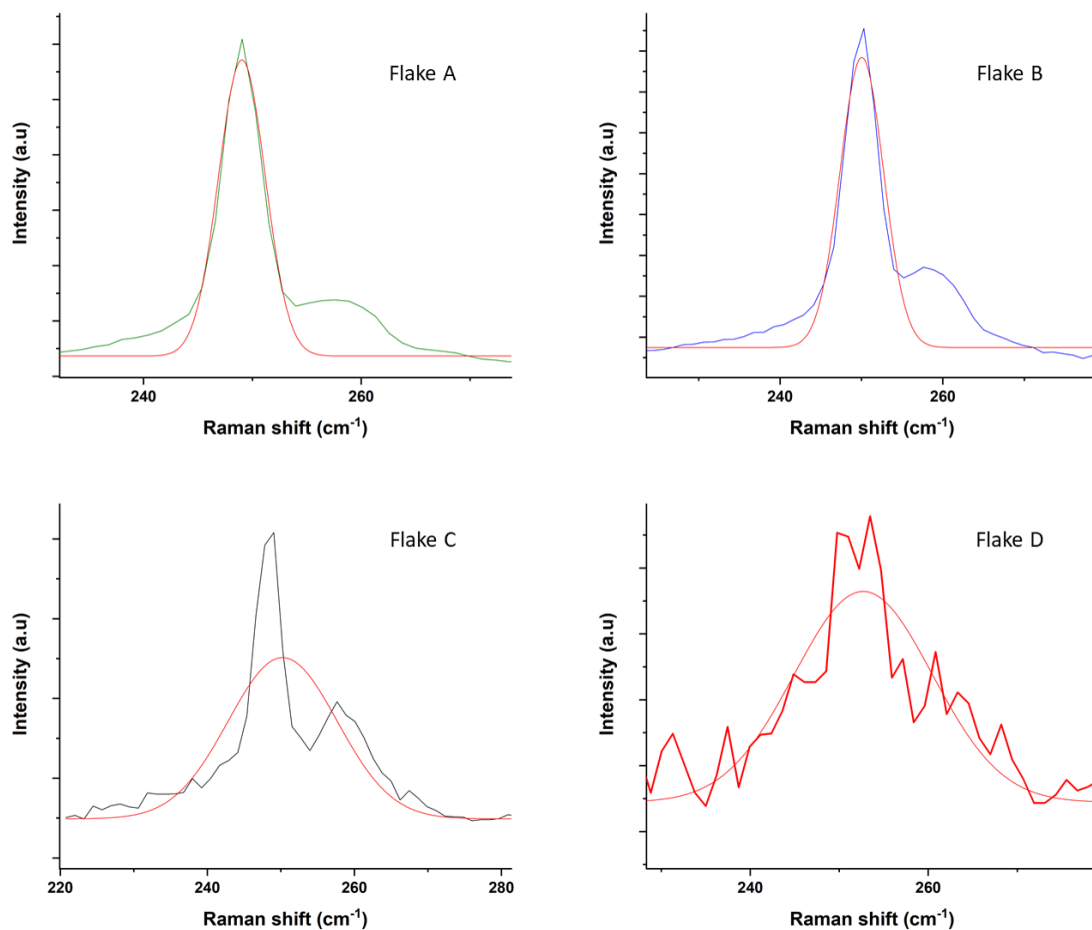


**Figure A.3:** AFM profile of exfoliated WSe<sub>2</sub> flake A, B, C and D

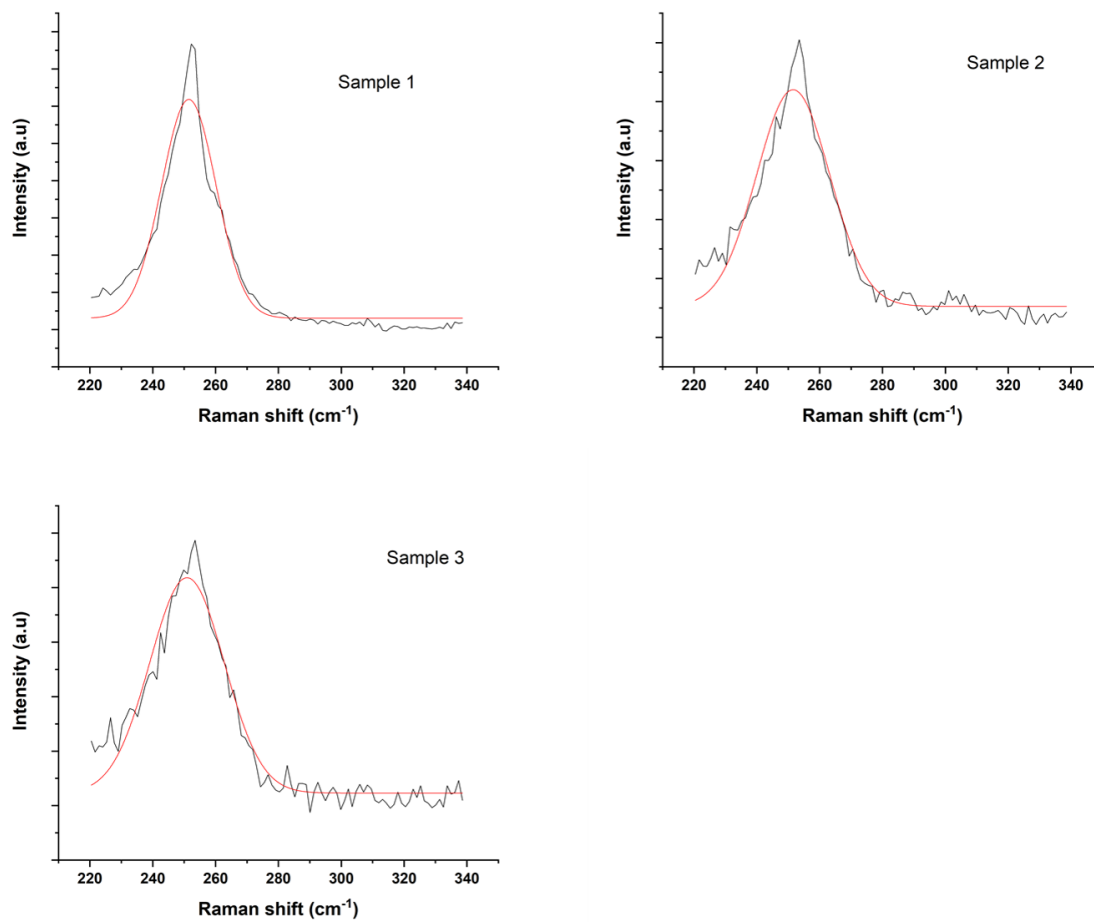


**Figure A.4:** AFM profile of PLD WSe<sub>2</sub> sample 1, 2 and 3

## Appendix E – Fits of Raman plots (X-WSe<sub>2</sub> and PLD WSe<sub>2</sub>)



**Figure A.5:** FWHM fit of Raman plots for the exfoliated WSe<sub>2</sub> flakes A, B, C and D



**Figure A.6:** FWHM fit of Raman plots for the PLD WSe<sub>2</sub> sample 1, 2 and 3