Master's Thesis

Design and Analysis of All-Digital Phase-Locked Loop for Automotive CIS Interface

차량용 CIS Interface 를 위한 All-Digital Phase-Locked Loop 의 설계 및 분석

by

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February, 2021

Department of Electrical and Computer Engineering
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Design and Analysis of All-Digital Phase-Locked Loop for Automotive CIS Interface

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Design and Analysis of All-Digital Phase-Locked Loop for Automotive CIS Interface

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Abstract

This thesis presents design techniques for All-Digital Phase-Locked Loop (AD-PLL) assisting the automotive CMOS image sensor (CIS) interface. To target Gear 3 of the automotive physical system, the proposed AD-PLL has a wide operation range, low RMS jitter, and high PVT tolerance characteristics.

Detailed analysis of the loop dynamics and the noise analysis of AD-PLL are done by using Matlab and Verilog behavioral modeling simulation before an actual design. Based on that analysis, the optimal DLF gain configurations are yielded, and also, accurate output responses and performance are predictable. The design techniques to reduce the output RMS jitter are discussed thoroughly and utilized for actual implementation.

The proposed AD-PLL is fabricated in the 40 nm CMOS process and occupies an effective area of 0.026 mm^2. The PLL output clock pulses exhibit an RMS jitter of 827 fs at 2 GHz. The power dissipation is 5.8 mW at 2 GHz, where the overall supply voltage domain is 0.9 V excluding the buffer which is 1.1 V domain.

Keywords : **All-Digital Phase-Locked Loop (AD-PLL), Time-to-Digital Converter (TDC), Digitally Controlled Oscillator (DCO), Digital Loop Filter (DLF), Delta-Sigma Modulator (DSM), Phase Noise Analysis**

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Chapter 1

Introduction

1.1 Motivation

Recently, automotive communication networks are rapidly evolving [1]. Especially for the Advanced Driver Assistance System (ADAS), a high-bandwidth transmission of high-resolution image data is crucial to utilize deep learning neural networks for complex computation. Therefore, the demand for high-resolution automotive CMOS image sensor (CIS) interface is increasing. However, there's a lot of challenges because of its harsh communication environment and the rigorous requirements on robustness and reliability. Thus, to transfer reliable data with a multi-Gb/s transmission rate, accurate clock generation for both the transmitter and the receiver is the most essential.

All-Digital Phase-Locked Loop (AD-PLL) is emerging as a solution to combat this problem. Unlike Analog PLL, AD-PLL is beneficial in terms of its small area, high process-voltage-temperature (PVT) tolerance, scalability, programmability, and testability due to its digital nature. However, one of the challenges in designing AD-PLL is minimizing the quantization noise that occurs when converting analog values into digital values. In this work, based on the theoretical analysis, design techniques; such as designing a high-performance TDC, boosting the effective resolution of DCO, and noise shaping with DSM, to overcome such problems are addressed in depth. Moreover, to satisfy the design specification of Gear 3 of the automotive physical system, whose main target data rate is 8 Gb/s with PAM-4 signaling, 8 phase 2 GHz Ring Oscillator is designed to support the half-rate signaling. Besides, to support Gear 1, 2, and to leave a margin for the possible extension toward Gear 4, the frequency range is set to be configurable from 1.5 GHz to 3 GHz. As a result, the proposed AD-PLL complies with every design requirement needed for the state of art CIS interface system and also achieves low output clock jitter. Note that the whole system is controllable and adjustable digitally.

1.2 Thesis Organization

This thesis is organized as follows. Chapter 2 starts with the background of AD-PLL in terms of its structure and its loop dynamics. Then the operations of each building block are explained and the effect of various noise sources on the output clock jitter is analyzed. Chapter 3 delves into the detailed circuit implementation of AD-PLL that has good phase noise characteristics. Specifically, it covers the design techniques to build high-resolution TDC, low jitter 4 Stage Ring Oscillator, and configurable DLF and DSM. Based on these design implementations in Chapter 3, Chapter 4 focuses on the post-layout simulation results and the analysis of the actual measurement results. Note that the automation code is utilized in the actual measurement process. The comparison table compares the performance of the proposed work with that of the other related state-of-the-art researches. Chapter 5 summarizes the proposed work and concludes this thesis.

Chapter 2

Background on All-Digital PLL

2.1 Overview

In the realm of high-speed link circuits, accurate data transmission and recovery is crucial. However, as the data rate increases, higher susceptibility to channel loss and inter-symbol-interference make low jitter clock generation and elaborate compensation technique indispensable. Phase-Locked Loop (PLL) has been widely used in many circuits for a long time to generate clock pulses for this purpose.

PLL is a circuit that adjusts the phase and frequency of the internal clock by minimizing the phase and frequency error between the external clock and the internal clock through a feedback loop. Like any feedback system, PLL consists of three main components; a Producer that generates the output, a Sensor that measures the error

between the input and the output, and a Controller that adjusts the control of the producer based on the information given by the sensor. Depending on whether or not these main constituents are made digitally or could be handled with digital equivalents, PLL is classified into Digital PLL and Analog PLL.

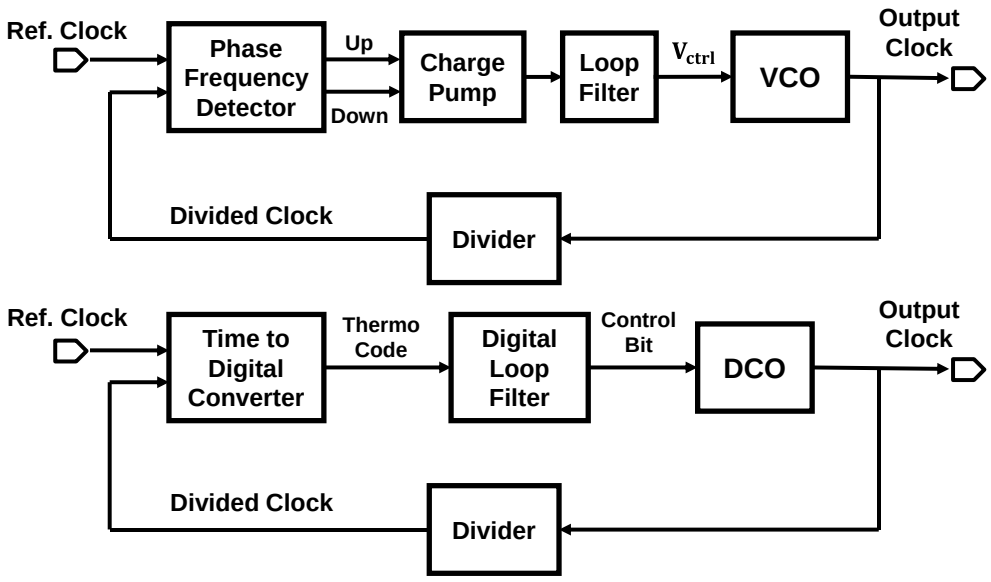


Fig. 2.1 Block Diagram of (a) Charge-Pump PLL (b) All-Digital PLL

Among various types of PLL in these two subgroups, Figure 2.1 shows the block diagram of the corresponding representatives; the Charge-Pump PLL (CP-PLL) and the All-Digital PLL (AD-PLL). Although CP-PLL has been extensively studied in the past few decades, the issues dealing with analog components such as leakage current, device mismatch, large area, and low voltage headroom are becoming more problematic as the CMOS technology scales down continuously. As a solution, AD-PLL, which is based on Digitally Controlled Oscillator (DCO) and Digital Loop Filter (DLF)

instead of their analog counterparts, is proposed and has been investigated recently. The key strengths of AD-PLL are in its high programmability, synthesizability, and PVT tolerance. In addition, since the building blocks are controlled with digital codes and there's no need for analog tuning voltages, it is suitable for deep-submicron technology with low supply voltage.

Despite these advantages, AD-PLL is prone to the quantization noise that occurs when converting analog values to digital values. Especially, the quantization noise of TDC and DCO is a critical factor in degrading the jitter performance. In the following sections, each of the building blocks will be explained in detail and the phase noise analysis to optimize overall jitter performance would be further addressed.

2.2 Building Blocks of AD-PLL

2.2.1 Time-to-Digital Converter

In AD-PLL, TDC converts the time difference between the reference clock and the divided clock into digital codewords. Figure 2.2 shows the basic operation of TDC. When START rises, TDC starts to count the time difference T_{in} with the resolution Δt_{TDC}. This count continues until STOP changes from low to high. TDC's output D_{out} can be expressed as Equation (2.1).

$$D_{out} = \frac{T_{out}}{\Delta t_{TDC}} = \frac{T_{in} - T_{err,stop} + T_{err,start}}{\Delta t_{TDC}} \quad (2.1)$$

The transfer curve of TDC is shown in Figure 2.3. Unlike an analog PFD used in the CP-PLL, TDC performs an equal function but with a quantized output value. This results in quantization noise, which degrades the PLL jitter performance. The impact of TDC quantization noise in overall phase noise performance would be dealt with in the next section.

To reduce the effect of TDC quantization noise, TDC must have a high enough resolution. However, this would reduce the detection range, whose wideness is another important metric of designing TDC. Linearity, power, area are other requirements that a TDC should satisfy.

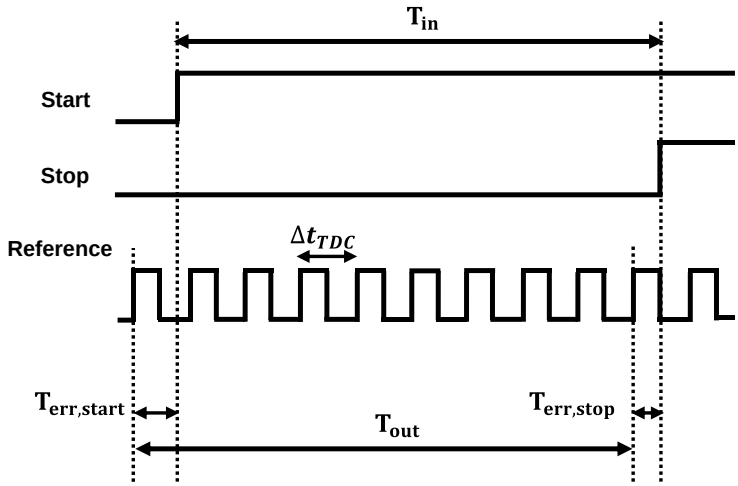


Fig. 2.2 TDC Operation

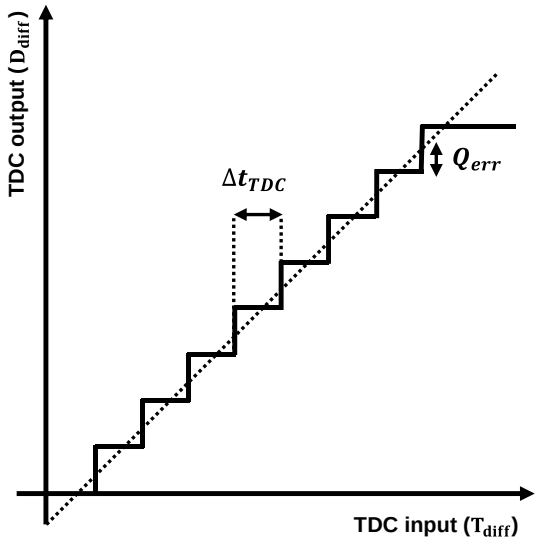


Fig. 2.3 TDC Transfer Curve

TDC can be classified into a short time interval generation TDC which utilizes fine timing signal to translate time interval to digital code; a time stretching TDC which

amplifies input time difference before feeding into the delay chain; and other un-grouped TDC, such as stochastic TDC [2], gated ring oscillator TDC [3]. Among these types, delay-line-based TDC, which belongs to the short time interval generation TDC, is the most widely used in digital PLLs.

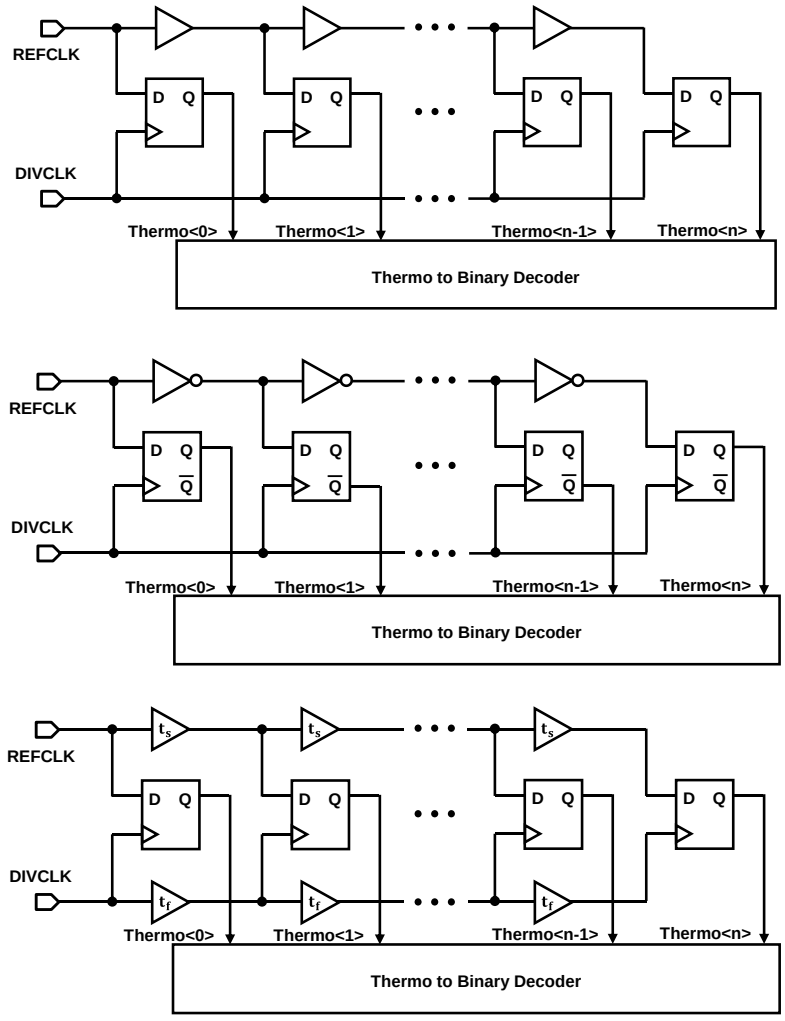


Fig. 2.4 (a) Delay Line TDC (b) Differential Delay Line TDC (c) Vernier TDC

In Figure 2.4, three basic types of delay-line based TDC is shown. As readily seen, a simple delay line TDC in Figure 2.4 (a) has resolution with two inverter delay and a differential delay line TDC in Figure 2.4 (b) has resolution with one inverter delay by using differential D-Flip Flop. However, due to the device process limit, achieving high resolution is hard with these methods. To mitigate this problem, a Vernier delay line TDC in Figure 2.4 (c) is suggested. In this structure, the resolution is equal to the difference between t_s and t_f, which makes it possible to enhance TDC resolution to sub-gate-delay, even if the actual delay of each delay line is large [4].

2.2.2 Digitally-Controlled Oscillator

DCO generates an output clock with a frequency that is proportional to the input digital code. The transfer curve of DCO is shown in Figure 2.5. Whereas an analog Voltage-Controlled Oscillator (VCO) in the CP-PLL directly controls the frequency of an output clock with the input voltage, DCO controls the corresponding value with the Frequency Control Word (FCW). Therefore, the output value is discretized and the quantization noise occurs, which also degrades the PLL jitter performance.

To reduce such a malign effect, the frequency step size must be small, but at the same time fully covering the target frequency range in all PVT variation corners. However, higher resolution and wider frequency range would increase the overall power consumption and area, so the designers have to compromise with this trade-off.

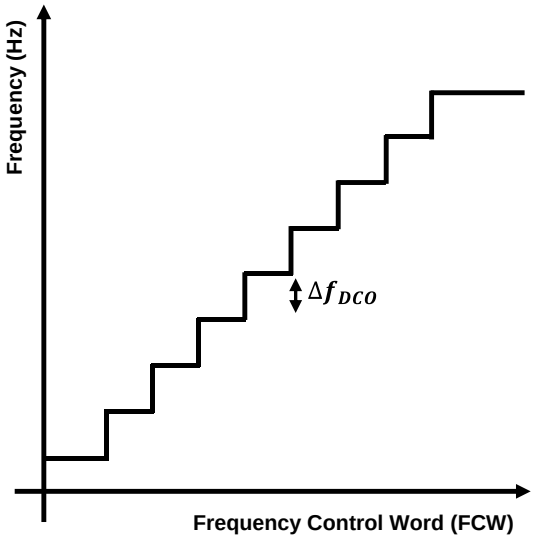


Fig. 2.5 Transfer curve of DCO

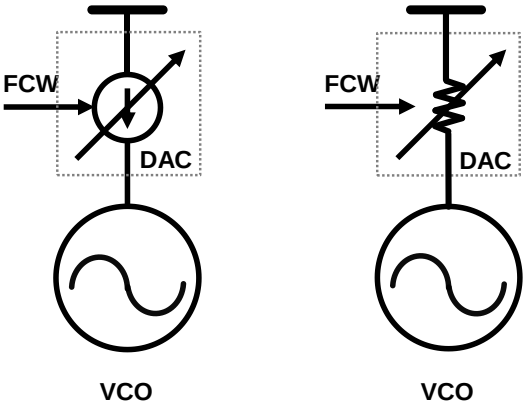


Fig. 2.6 (a) Current-Controlled DCO (b) Resistor-Controlled DCO

Since the phase noise and the power of DCO take up most of the corresponding values of the overall PLL system, meticulous efforts are needed in designing DCO. A typical way of implementing a DCO is to combine Digital-to-Analog Converter (DAC)

and analog VCO as shown in Figure 2.6. As in Figure 2.6 (a), a current-controlled DAC type controls the VCO output frequency by varying the current flowing through the VCO corresponding to the input digital code. Whereas in Figure 2.6 (b), a resistor-controlled DAC type controls the VCO output frequency by changing the resistance between the external supply voltage and the VCO supply voltage, thus changing the supply voltage of the VCO. Generally, a current-controlled DAC is better in terms of the phase noise performance but suffers more at the voltage headroom issue over a resistor-controlled DAC.

In addition, depending on the type of oscillator that DCO uses, DCO could be classified into two groups; a Ring-DCO and an LC-DCO. The former benefits from its design simplicity to generate multi-phase output clock pulses, wider frequency tuning range, and its smaller occupancy in terms of area but it is poor at phase noise characteristics and is more sensitive to PVT variations than the latter. Based on these characteristics, the choice of an appropriate type of DCO is up to designers depending on one's target application.

Besides, FCW could be implemented with a binary code or thermometer code. With N bits of code, in binary coding, the output frequency can have 2^N values, whereas, in thermometer coding, only N values are obtainable. Despite this drawback in decoding hardware cost, since the thermometer code increases monotonically, utilizing the thermometer code can make the DAC safe from glitch problems. One way to utilize the advantages of the binary coding and the thermometer coding at the same time is to use a segmented thermometer scheme, which is the combination of the two. The

detailed implementation of DAC by using the segmented thermometer coding would be addressed in detail in the next chapter.

2.2.3 Digital Loop Filter

Loop Filter is a critical block that governs the loop dynamics of the overall system. In CP-PLL, this is implemented with resistors and capacitors as shown in Figure 2.7 (a), which converts the charge pump current into the VCO control voltage V_{ctrl}. As shown in Figure 2.7 (b), DLF in AD-PLL on the other hand, takes the TDC output as an input and generates a frequency control word for DCO, and this is all built digitally. The digital nature of DLF brings many advantages. For example, since there is no capacitor in DLF, the system is free from leakage current issues. Also, a designer can adaptively configure gains of DLF to adjust the loop bandwidth of PLL without an additional cost of the area. Adaptive algorithms for fast locking or reducing jitter could be implemented also with ease. PVT tolerance is another merit of the DLF.

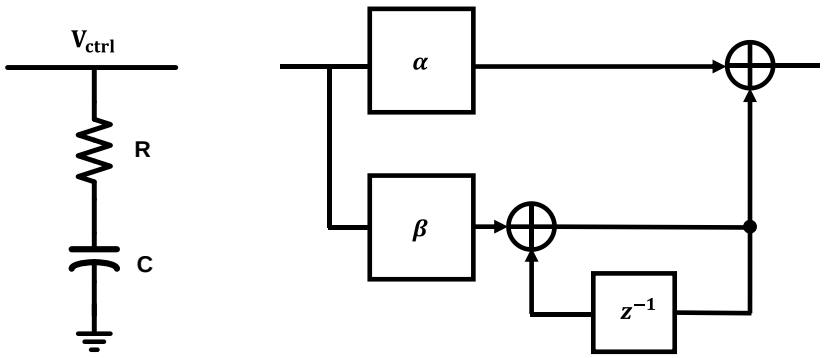


Fig. 2.7 (a) Analog Loop Filter (b) Digital Loop Filter

A Loop Filter has both a proportional term and an integral term. Take an example of a first-order analog Loop Filter in Figure 2.7 (a). The transfer function can be represented as Equation (2.2).

$$F_{LPF}(s) = \frac{V_{ctrl}(s)}{I_{CP}(s)} = R + \frac{1}{sC} \tag{2.2}$$

It can be inferred from this transfer function that the proportional term R tracks the transient phase error and the integral term $\frac{1}{sC}$ tracks the accumulating frequency error of the system. Another physical interpretation of these two terms in CP-PLL is that the capacitor sets the natural frequency w_n and the resistor sets the damping factor ζ of the whole system. This could be derived from the closed-loop transfer function of CP-PLL, which can be expressed as following Equations (2.3) to (2.5). Note that the natural frequency has a significant effect on the CP-PLL loop bandwidth w_{3dB}.

$$H_{CP-PLL}(s) = \frac{\frac{IK_{VCO}}{2\pi C}(RCs + 1)}{s^2 + \frac{IK_{VCO}R}{2\pi N}s + \frac{IK_{VCO}}{2\pi CN}} = N\frac{2\zeta w_n s + {w_n}^2}{s^2 + 2\zeta w_n s + {w_n}^2} \tag{2.3}$$

$$w_n = \sqrt{\frac{IK_{VCO}}{N2\pi C}}, \qquad \zeta = \frac{R}{2}\sqrt{\frac{ICK_{VCO}}{N2\pi}} = \frac{RC}{2}w_n \tag{2.4}$$

$$w_{3dB} = w_n[2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}\,]^{\frac{1}{2}}, \quad PM = \arctan(RC \cdot w_{3dB}) \tag{2.5}$$

Likewise, in a DLF in Figure 2.7 (b), an input signal in the proportional path is multiplied with the proportional gain α and that in the integral path is multiplied with the integral gain β. These two paths perform the equivalent behavior with their analog counterparts, holding the phase and frequency information. The transfer function of DLF is given as Equation (2.6).

$$F_{DLF}(z) = \alpha + \frac{\beta}{1 - z^{-1}} \tag{2.6}$$

Since the z-domain representation of DLF is hard to interpret its physical meaning on the bandwidth and stability of AD-PLL, it is useful to use bilinear transform to convert the discrete-time z-domain system to the continuous-time s-domain system and vice versa. Bilinear transform in Equation (2.7) is derived from a first-order approximation of the natural logarithm function that maps z-plane to s-plane.

$$z = e^{sT} \approx \frac{1 + \frac{sT}{2}}{1 - \frac{sT}{2}}, \quad s \approx \frac{2}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}}, \quad T = \text{DLF's sampling period} \tag{2.7}$$

Thus, with the help of bilinear transform, the corresponding transfer function of the analog Loop Filter in z-domain representation could be written down as Equation (2.8). Besides, by equating Equation (2.5) and (2.7) the relationship between the digital gain α, β, and analog R, C could be derived as Equation (2.9). Note that the ratio of α to β in Equation (2.10) defines the phase margin and thus the stability of the AD-PLL system [5], [6].

$$F_{LPF}(z) = \left(R - \frac{T}{2C}\right) + \left(\frac{T}{C}\right) \cdot \frac{1}{1 - z^{-1}} \tag{2.8}$$

$$\alpha = R - \frac{T}{2C}, \qquad \beta = \frac{T}{C} \tag{2.9}$$

$$\frac{\alpha}{\beta} = \frac{\tan(PM)}{T \cdot w_{3dB}} - \frac{1}{2} \tag{2.10}$$

2.2.4 Delta-Sigma Modulator

A Delta-Sigma Modulator is an optional digital block in AD-PLL, however, it is a powerful tool for noise shaping and thus reducing the quantization noise of DCO. As mentioned before, the quantization noise is inversely proportional to the quantization resolution. Yet, due to the hardware limitation and the trade-off between the operation region and the resolution, there is a limitation in increasing the quantization resolution. As a solution, a dithering technique and a DSM emerged.

A dithering technique is a way of randomizing certain periodic sequences thus reducing undesired tones. By using the dithering technique in AD-PLL, it can effectively increase the resolution of the DCO. Consider a simple example of Figure 2.8. Assume that PLL's divide ratio is 10, and the frequency error between the reference clock and the divided clock is Δf_{DCO}. Without the dithering, the phase error would accumulate as time goes by. On the contrary, if the frequency of one cycle in DCO changes from f_0 to $f_0 + \Delta f_{DCO}$ in each reference clock, the phase error would go

to zero. This makes the average frequency of DCO to $f_0 + \Delta f_{DCO}/10$, which is equivalent to a tenfold increase in the quantization resolution of DCO. In general, if the DCO frequency is f_0 in N cycles and $f_0 + \Delta f_{DCO}$ in M cycles, the average frequency would be $f_0 + \Delta f_{DCO} \cdot \frac{M}{M+N}$, making the effective resolution $\frac{M}{M+N}$ times. However, one drawback is that it can generate spurs and inject dithering noises. By using a DSM, one can compensate for this.

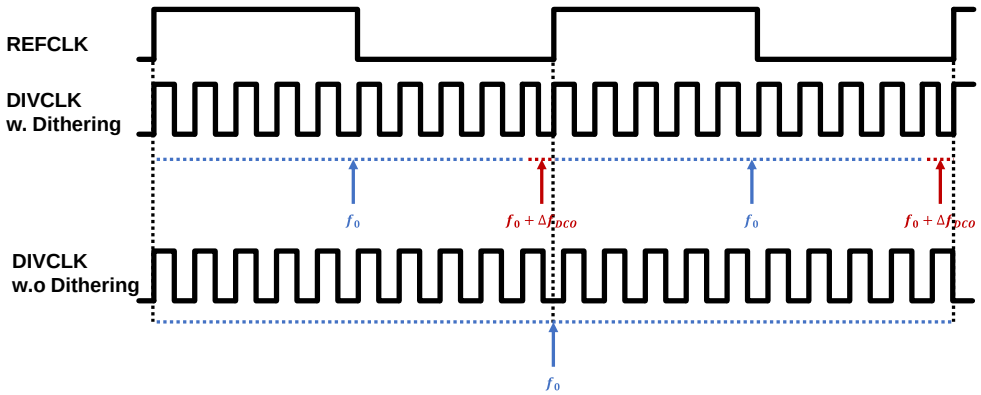


Fig. 2.8 An Example of Dithering

The concept of rudimentary DSM is simple. Basically, it oversamples the signal until the sampling points are close enough to create correlated quantization errors between the consecutive samples, then subtracts the quantization error of one sample from the next to reduce the overall quantization noise. In Figure 2.9, a typical block diagram of DSM is shown. Written down in a mathematical formation, the relationship between the input x(t), the quantization noise q(t), and the output y(t) are given as Equation (2.11). By taking the z-transform of this, Equation (2.12) could be yielded.

$$y(kT_s) = x\big((k-1)T_s\big) + q(kT_s) - q((k-1)T_s) \tag{2.11}$$

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \tag{2.12}$$

In Equation (2.12), the output is the sum of two components; the input multiplied by z^{-1}, and the quantization noise multiplied by $1 - \mathrm{z}^{-1}$. The multiplier of the former term is called a signal transfer function (STF) and the latter term is called a noise transfer function (NTF). Since the NTF $(1 - \mathrm{z}^{-1})$ exhibits a characteristic of a high pass filter, the spectrum of the quantization noise moves to a higher frequency. For higher M-th order DSMs, which are cascaded versions of the first order DSM, the NTF becomes $(1 - \mathrm{z}^{-1})^{\mathrm{M}}$ and they transfer more energy to the high-frequency region. An example of a noise shaping function is drawn in Figure 2.10. Note that the effect of reducing the quantization noise is proportional to both the order of DSM and the oversampling ratio (OSR), which is defined as $\frac{\mathrm{f_S}/2}{\mathrm{f_D}}$, where $\mathrm{f_D}$ is an input signal's bandwidth [7].

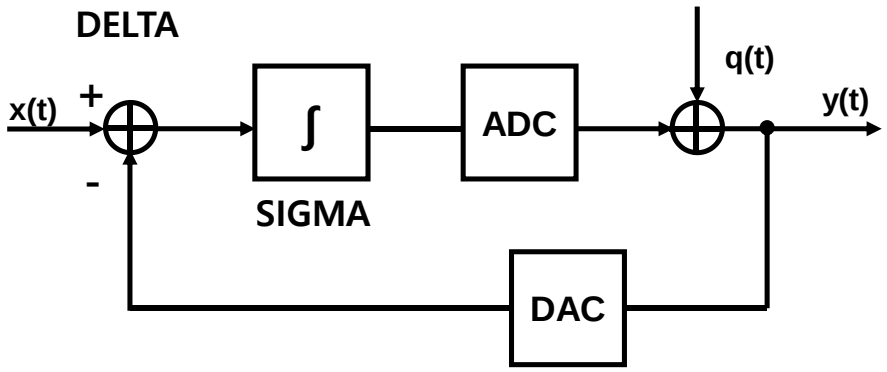


Fig. 2.9 1st-Order DSM Block Diagram

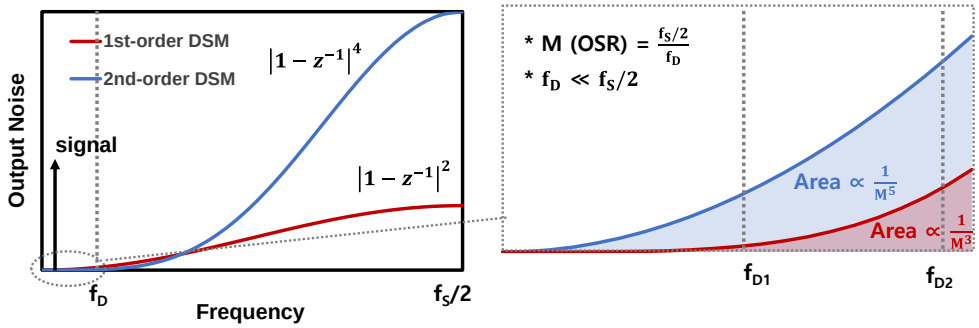


Fig. 2.10 Noise Shaping Function of the 1st and 2nd-Order DSM

2.3 Phase Noise Analysis of AD-PLL

2.3.1 Basic Assumption of Linear Analysis

PLL has four basic regions of operation which are the hold range, pull-in range, pull-out range, and lock range as depicted in Figure 2.11. Briefly explaining, the hold range denotes the frequency range that PLL can statically maintain phase tracking, the pull-in range is the range that PLL will always become locked, the pull-out range is the range that PLL can dynamically sustain phase tracking, and finally, the lock range is the range that PLL locks within a single beat note between the reference frequency and the output frequency [8].

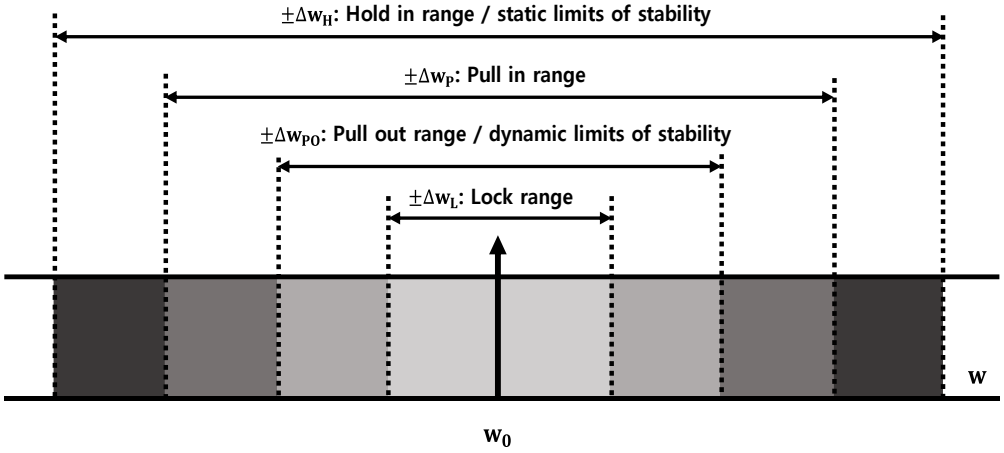


Fig. 2.11 Operation Regions of a PLL

Among these regions, if PLL is in the lock range, the behavior of the PLL can be described with a linear model analysis. In other words, the basic assumption of the linear analysis is that the frequency error of the output signal to the reference signal is zero, and the phase error between the two is a constant value. Keeping in mind this basic assumption, let's delve into the analysis of each noise source.

2.3.2 Noise Sources of AD-PLL

There are 5 internal noise sources in AD-PLL as shown in Figure 2.12; TDC Quantization Noise, DSM Dithering Noise, DCO Quantization Noise, DCO Phase Noise, and Reference Phase Noise. Each noise sources' power spectral density (PSD) can be modeled as Equation (2.13) to (2.17). Note that the open-loop and the closed-loop transfer function is given as Equation (2.18) and (2.19) respectively.

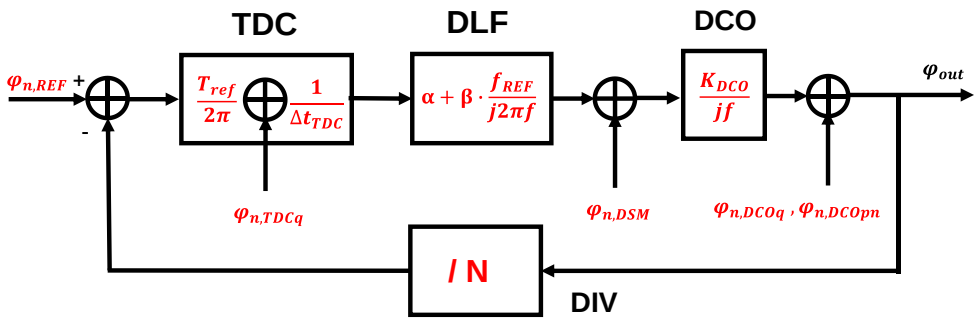


Fig. 2.12 Noise Sources of AD-PLL

$$S_{\varphi n,TDCq}(f) = \left(\frac{\Delta t_{TDC}{}^2}{12 f_{ref}}\right) \cdot \left(\frac{2\pi}{T_{ref}}\right)^2 \tag{2.13}$$

$$S_{\varphi n,DSM}(f) = \left(\frac{\Delta f_{DCO,eff}{}^2}{12 f^2 f_{DSM}}\right) \cdot \left(2\sin(\frac{\pi f}{f_{DSM}})\right)^{2n}, n = \text{ order of DSM} \tag{2.14}$$

$$S_{\varphi n,DCOq}(f) = \left(\frac{\Delta f_{DCO,eff}{}^2}{12 f^2 f_{ref}}\right) \cdot \left(\text{sinc}(\frac{f}{f_{ref}})\right)^2 \tag{2.15}$$

$$S_{\varphi n,DCOpn}(f) = \left(\frac{2FkT}{P_{DCO}}\right) \cdot (1 + \left(\frac{f_{DCO}}{2Q_{DCO} f}\right)^2) \cdot (1 + \frac{f_{f-3,DCO}}{f}) \tag{2.16}$$

$$S_{\varphi n,REF}(f) = \left(\frac{2FkT}{P_{REF}}\right) \cdot (1 + \left(\frac{f_{REF}}{2Q_{DCO} f}\right)^2) \cdot (1 + \frac{f_{f-3,REF}}{f}) \tag{2.17}$$

$$H_{op}(f) = \frac{T_{ref} K_{DCO}}{\Delta t_{TDC}(j2\pi f) N} \cdot (\alpha + \frac{\beta f_{ref}}{j2\pi f}) \tag{2.18}$$

$$G(f) = \frac{H_{op}(f)}{1 + H_{op}(f)} = \frac{T_{ref}(j2\pi f\alpha + \beta f_{ref}) K_{DCO} N}{T_{ref}(j2\pi f\alpha + \beta f_{ref}) K_{DCO} + \Delta t_{TDC}(j2\pi f)^2 N} = \frac{1}{N} \cdot H_{cl}(f) \tag{2.19}$$

Then, by using the closed-loop gain of PLL, the output PSD of each noise source after passing the linear modeling of the PLL would be reduced to Equation (2.20) to (2.24). The total phase noise is equivalent to the sum of output phase noises of each noise source, as suggested in Equation (2.25). Besides, the RMS Jitter of the output clock could be calculated through Equation (2.26) [9], [10].

$$S_{\varphi out,TDCq}(f) = S_{\varphi n,TDCq}(f) \cdot |\mathrm{N} \cdot \mathrm{G(f)}|^2 \tag{2.20}$$

$$S_{\varphi out,DSM}(f) = S_{\varphi n,\mathrm{DSM}}(f) \cdot |1 - \mathrm{G(f)}|^2 \tag{2.21}$$

$$S_{\varphi \mathrm{out},DCOq}(f) = S_{\varphi n,\mathrm{DCO}q}(f) \cdot |1 - \mathrm{G(f)}|^2 \tag{2.22}$$

$$S_{\varphi \mathrm{out},DCOpn}(f) = S_{\varphi n,\mathrm{DCOpn}}(f) \cdot |1 - \mathrm{G(f)}|^2 \tag{2.23}$$

$$S_{\varphi \mathrm{out},REF}(f) = S_{\varphi n,\mathrm{REF}}(f) \cdot |\mathrm{N} \cdot \mathrm{G(f)}|^2 \tag{2.24}$$

$$\begin{aligned} S_{\varphi out,\mathrm{total}}(f) = {} & S_{\varphi out,TDCq}(f) + S_{\varphi out,DSM}(f) + S_{\varphi \mathrm{out},DCOq}(f) \\ & + S_{\varphi \mathrm{out},DCOpn}(f) + S_{\varphi \mathrm{out},REF}(f) \end{aligned} \tag{2.25}$$

$$\mathrm{J_{RMS}} = \frac{1}{2\pi \mathrm{f_c}} \cdot \sqrt{2 \int_0^{\infty} 10^{\frac{\mathrm{L(f)}}{10}} \mathrm{df}} \ , \qquad \mathrm{L(f)} = \frac{1}{2} \cdot S_{\varphi out,\mathrm{total}}(f) \tag{2.26}$$

In general, TDC quantization noise, DCO quantization noise, and DCO phase noise are the dominant sources of noise in AD-PLL. In addition, it can be inferred from the output phase noise equations that the TDC quantization noise is low pass filtered by the overall closed-loop gain function. However, the DCO quantization noise and DCO phase noise are high-pass filtered by this function. Thus, lower the loop bandwidth reduces the TDC quantization noise more but increases the other two more. Therefore,

adjusting α and β to an optimal value, considering the dominant noise sources is crucial in noise optimization of AD-PLL.

2.3.3 Effects of Loop Delay on AD-PLL

One of the nonidealities that one must consider in designing AD-PLL, is the effects of the loop delay. Because of the digital processing time in digital blocks, this loop delay occurs and changes the transfer function and the locking behavior. As shown in Figure 2.13, with the addition of z^{-D} in the block diagram, the open-loop gain changes from Equation (2.27) to Equation (2.28). This adds additional zeros in the s-domain when converted with bilinear transformation, thus degrading the phase margin and stability.

$$H_{open,w.o,delay}(z) = K_{TDC} \cdot \left(\alpha + \beta \cdot \frac{1}{1 - z^{-1}}\right) \cdot \frac{K_{DCO}}{1 - z^{-1}} \cdot \frac{1}{N} \tag{2.27}$$

$$H_{open,w,delay}(z) = K_{TDC} \cdot \left(\alpha + \beta \cdot \frac{1}{1 - z^{-1}}\right) \cdot z^{-D} \cdot \frac{K_{DCO}}{1 - z^{-1}} \cdot \frac{1}{N} \tag{2.28}$$

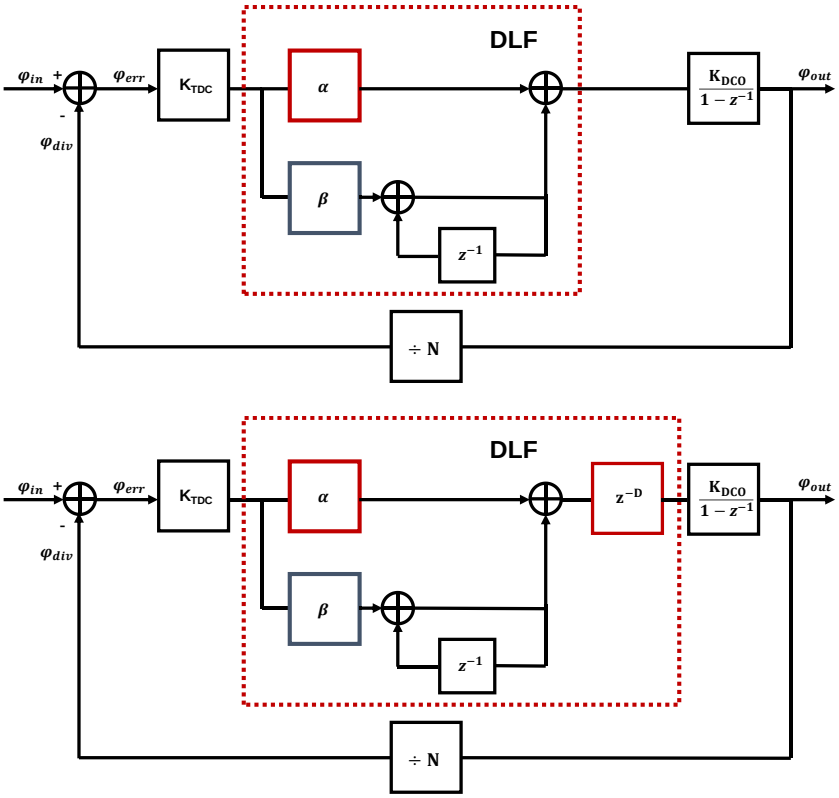


Fig. 2.13 (a) Block Diagram of AD-PLL without Loop Delay (b) with Loop Delay

To minimize such malicious effects, one needs to make an effective loop delay smaller. Other than trying to reduce the number of clock edges that are required to update the information of TDC to DCO, making the digital domain clocking faster than the reference clock is one way of doing so. For example, if the total clock edge needed is twelve, and the digital clock is ten times faster than the reference clock, then the effective loop delay becomes 1.2 cycles, not 12 cycles. Besides, another method of reducing the effective loop delay is to make a direct bypass from TDC to DCO parallel to the original DLF path, enabling the faster update of information.

2.3.4 Phase Noise Analysis of Proposed AD-PLL

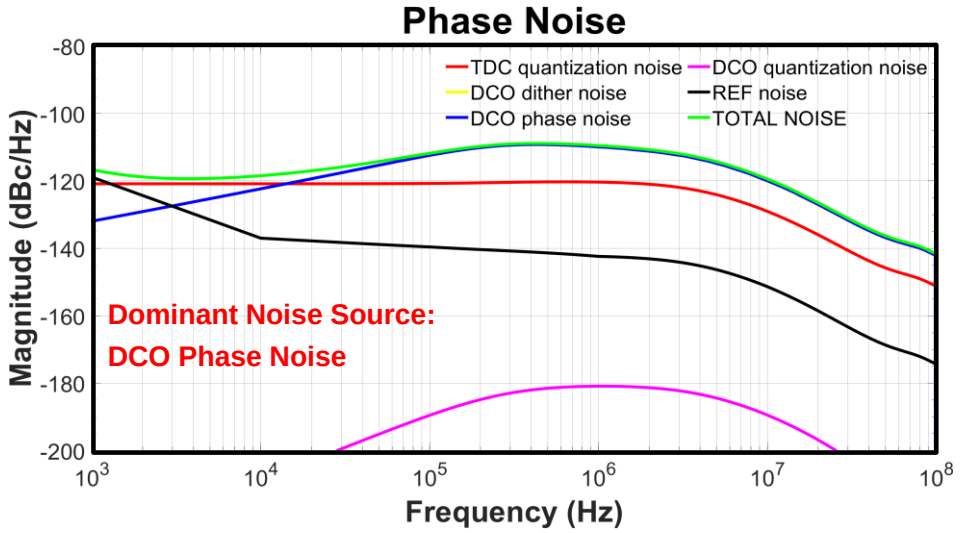


Fig. 2.14 Total Phase Noise Plot of AD-PLL ($\alpha = 2^{-5},\ \beta = 2^{-11}$)

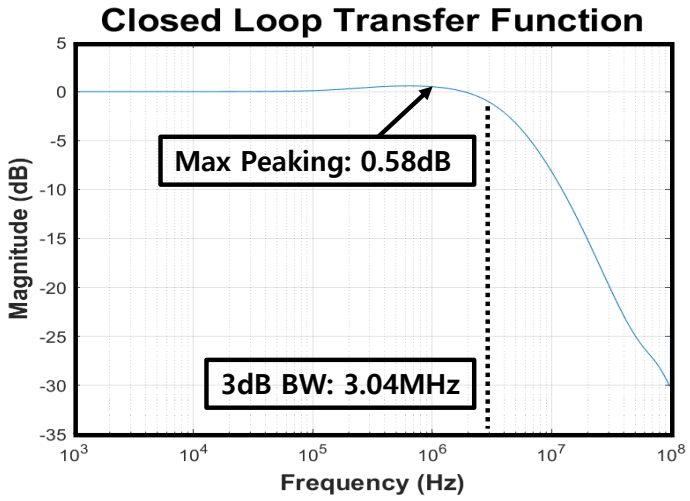


Fig. 2.15 Closed-Loop Gain Transfer Function of AD-PLL ($\alpha = 2^{-5},\ \beta = 2^{-11}$)

Based on the noise source analysis and considering the effect of loop delay and the techniques to alleviate its adverse effect dealt in the previous section, realistic phase noise analysis of the proposed AD-PLL is conducted. By using Matlab, the total phase noise plot could be drawn. Figure 2.14 shows the optimal total phase noise plot of AD-PLL based on the actual post-layout DCO phase noise and the delay modeling of implemented digital components. Specifically, -101 dBc/Hz DCO phase noise at 1 MHz offset, 100 MHz reference clock of phase noise -160 dBc/Hz, and divider factor of 20 is used. Besides, to reduce the effect of digital loop delay, the DLF frequency of 1 GHz, which is ten times faster than the reference frequency, is used. By sweeping the proportional gain and the integral gain of the loop filter, optimal values for jitter minimization are $\alpha = 2^{-5}$, $\beta = 2^{-11}$ for this simulated model. The estimated RMS jitter integrated from 10 kHz to 40 MHz is 843 fs with 0.58 dB maximum peaking at 0.63 MHz, and the PLL loop bandwidth is 3.04 MHz with a phase margin of 68.9 ◦. Note that the closed-loop transfer function of the system with this optimal gain configuration is depicted in Figure 2.15.

Chapter 3

Design of All-Digital PLL

3.1 Design Consideration

The AD-PLL proposed in this paper is designed to assist the automotive CIS interface system. The standard design specification is not firmly established yet, though, the overall requirements for this automotive physical system are discussed to be a maximum cable length of 10 m, and a channel bandwidth limit of about 2.5 GHz. Besides, compared to the other applications, the automotive physical system emphasizes more on the lower phase noise and higher robustness to PVT variations than lower power. This is because of the inherent characteristics of the automotive communication environment. Considering this and to support half-rate PAM-4 signaling of 8 Gb/s, which is the target downlink data rate of Gear 3, this paper suggests PVT tolerant, low phase noise 2 GHz AD-PLL.

Based on the phase noise analysis addressed before, PLL coefficients are set and the techniques introduced to make higher quantization resolutions are utilized for the design. For instance, the TDC resolution is set up to the physical limit to reduce the TDC quantization noise, and the digital blocks are synthesized with the highest frequency limit to improve the effective DCO resolution. Also, by using the first and the second-order DSM and the dithering technique, quantization noise shaping and boosting effective DCO resolution are possible. Furthermore, DCO is designed to cover the frequency range of 1.5 GHz to 3 GHz in every PVT corner and to generate 8-phase clock pulses with less skew to support phase interpolator-based half-rate clock and data recovery at the receiver.

3.2 Overall Architecture

The overall block diagram of the AD-PLL suggested in this paper is drawn in Figure 3.1. The building blocks are PFD-TDC, DLF, DSM, DCO, AC-coupled buffer, and Divider, respectively. With the input of 100 MHz external clock pulses, the output clock pulses of 8 phases are generated by the overall AD-PLL system and sent to the transmitter and receiver.

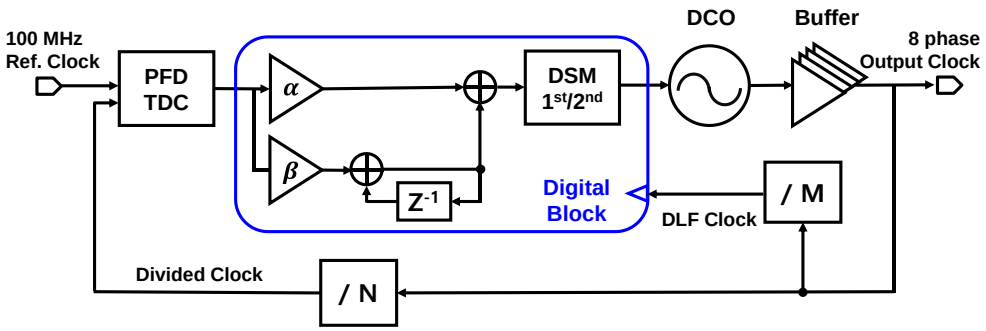


Fig. 3.1 Overall Block Diagram of AD-PLL

Whereas a TDC can detect phase errors only, the PFD-TDC block can also track frequency error information by placing PFD parallel to the TDC. Comparing the edges of the reference clock and those of the divided clock, this block generates 7-bit output thermometer codes, which are fed into the digital block through clock domain conversion. Then, in the digital block, the information from the PFD-TDC is low-pass filtered by the DLF, generating a 25-bit code consisted of 10 integer bits and 15 fractional bits. These bits are sent to the DSM, which outputs 10-bit Frequency Control

Word (FCW) that are decoded to 31-bit row code and 31-bit column code. These row and column codes control the Digitally Controlled Resistor (DCR) and the 4 stage Ring Oscillator generates the 8 phase output clock pulses with corresponding frequency. After passing AC coupled buffer to cover the full rail-to-rail swing of 1.1 V, the output clock pulses go to the other blocks of transmitter and receiver respectively. Among these output clock pulses, two clock pulses with opposite phases are selected, and this pair operates the divider to generate the divided clock and the digital clock, perpetuating the feedback loop.

3.3 Circuit Implementation

3.3.1 PFD-TDC

As stated before, a TDC converts the time difference between the reference clock and the divided clock into digital codewords. However, the conventional TDC only operates as a Phase-Detector (PD), thus additional methods for frequency tracking are needed. The PFD-TDC used in this implementation of AD-PLL uses Bang-Bang Phase-Frequency-Detector (PFD) parallel to Vernier delay line TDC to perform both phase and frequency tracking [11]. The overall architecture is presented in Figure 3.2.

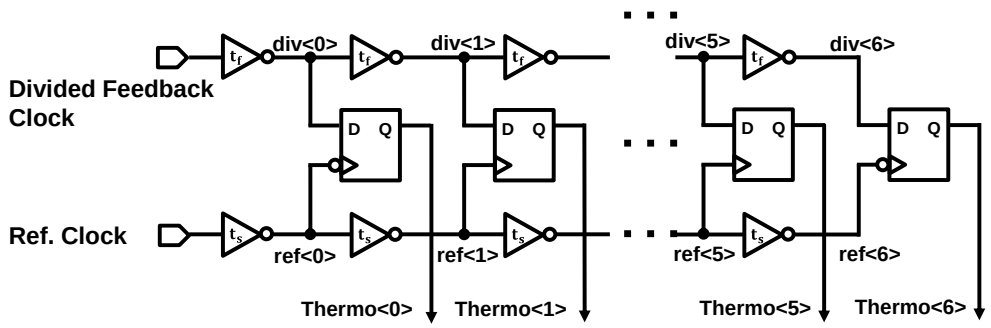


Fig. 3.2 PFD-TDC Structure

The resolution of the above PFD-TDC is equal to the difference between t_s and t_f, enhancing the TDC resolution to sub-gate-delay. To alleviate the burden of area, 7 delay cells and symmetric D-FF samplers [12] are used in total. Even and odd delay cells are separately implemented and REFCLK and REFCLKB are used for sampling

respectively. Note that the use of the symmetric sampler is beneficial because the setup time for data '1' and '0' is equal to each other. For delay cell implementation, rather than using an inverter pair, an inverter is used. This lowers the possibility of code reversion resulting from the delay variations. The 7 delay cells yield the 7-bit thermometer code, thus the detection range of phase error is equivalent to $7\cdot(t_s - t_f)$. The sizing of the delay cell is determined by the Monte-Carlo simulation and the resolution is set to 2.5 ps at TT corner (0.9V, 40°), 1.9 ps at FF corner (1.0V, -40°), 4.3 ps at SS corner (0.8V, 120°). Corresponding simulation results are shown in Figure 3.3. Note that the reversion probability is 0.006 % (3.82σ) at even delay cell and 0.002 % (4.13σ) at odd delay cell at TT corner, thus satisfying the monotonicity.

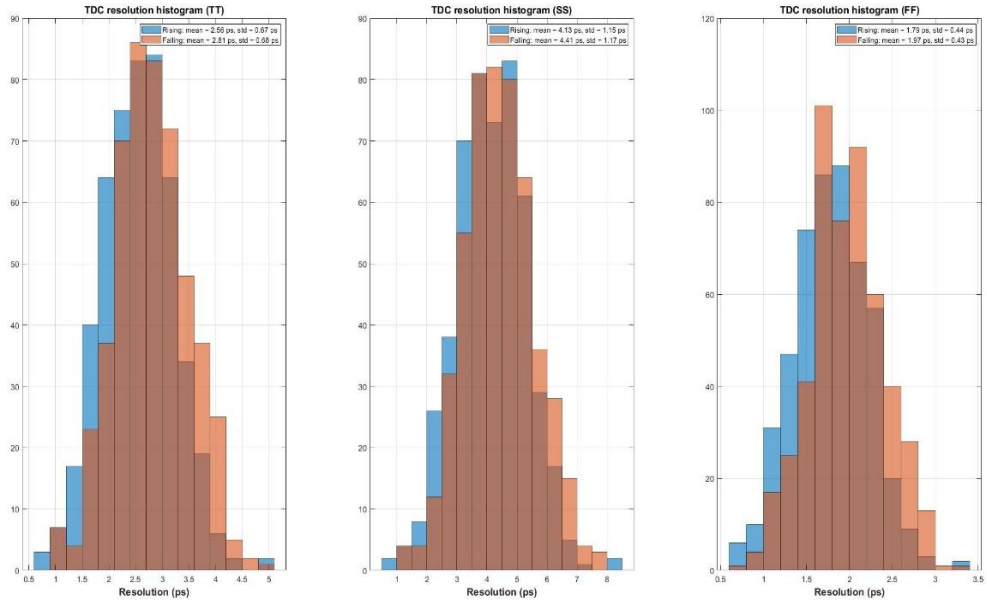


Fig. 3.3 Monte-Carlo Simulation Results of the TDC Resolution

As in Figure 3.4, BB-PFD with the input of REFCLK<3> and DIVCLK<3> is placed in parallel with the TDC for frequency tracking purposes. The sampler operates at the positive edge of REFCLK<1>, holding its value until the next signal comes in. If the phase difference of the inputs is in the TDC detection range, the PFD does not output UP, DN high signal, and for the other cases, the PFD produces UP or DN high signal according to the frequency relationship between the reference clock and the divided clock. Note that this dead zone control is done within the digital block and the total gain curve of PFD-TDC exhibits combined characteristics of PD and PFD as shown in Figure 3.5. Here, the proposed PFD-TDC has a PFD dead zone of 84 ps, and the TDC detection range of 17.5 ps.

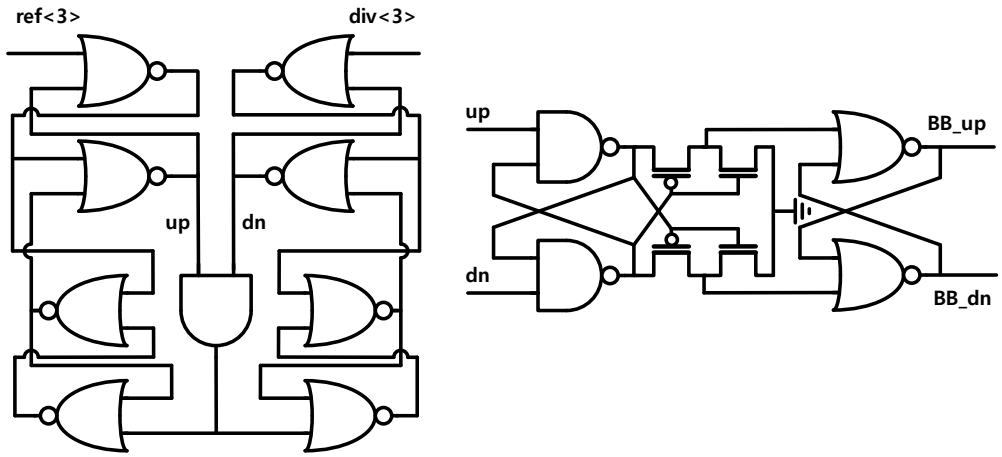


Fig. 3.4 BB-PFD Structure

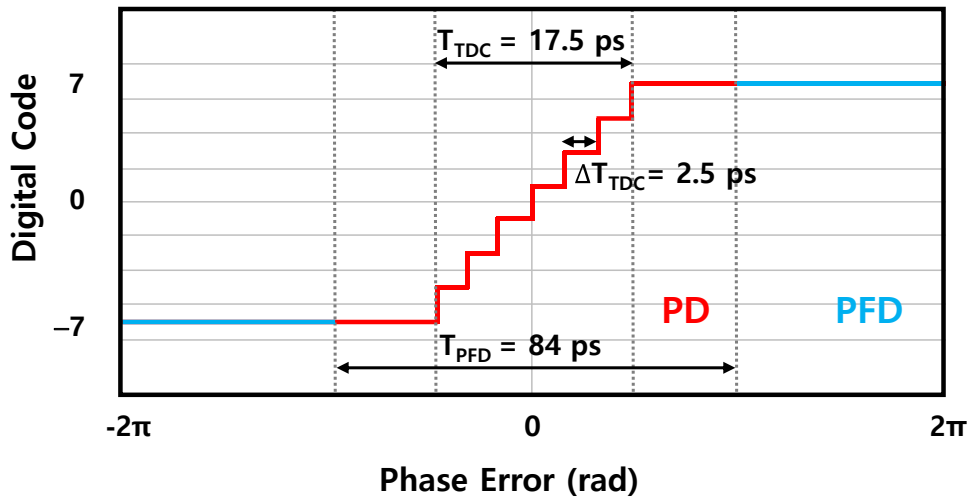


Fig. 3.5 PFD-TDC Gain Curve

The simulation results of the PFD-TDC is shown in Figure 3.6, 3.7, and 3.8. In Figure 3.6, the 100 MHz reference clock and the 100 MHz divided clock with 1.25 ps phase delay per period are used for simulation, and the corresponding output thermometer code changed by 1 bit per twice the period. Also, as shown in Figure 3.7, by shifting the initial phase of the divided clock pulses by ± 0.1π, the BB UP and DN high signals are generated respectively. Lastly, as presented in Figure 3.8, by using the 99 MHz and 101 MHz divided clock pulses, the PFD UP and DN high signals are produced properly. The total average power for the designed TDC is 0.51 mW.

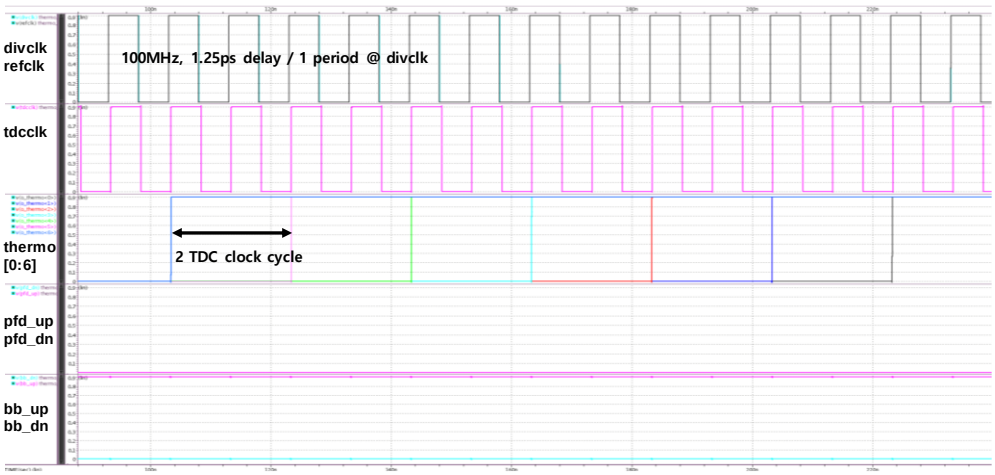


Fig. 3.6 Thermometer Code Simulation

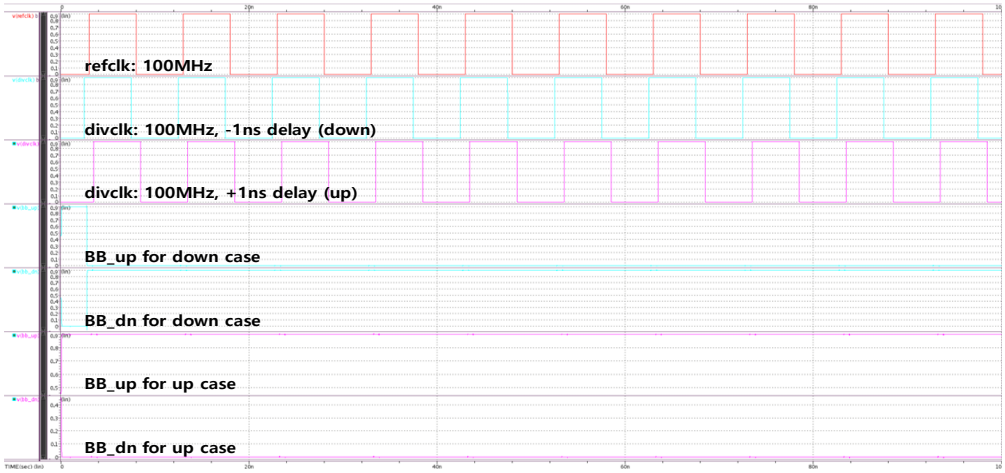


Fig. 3.7 BB Up / Down Simulation

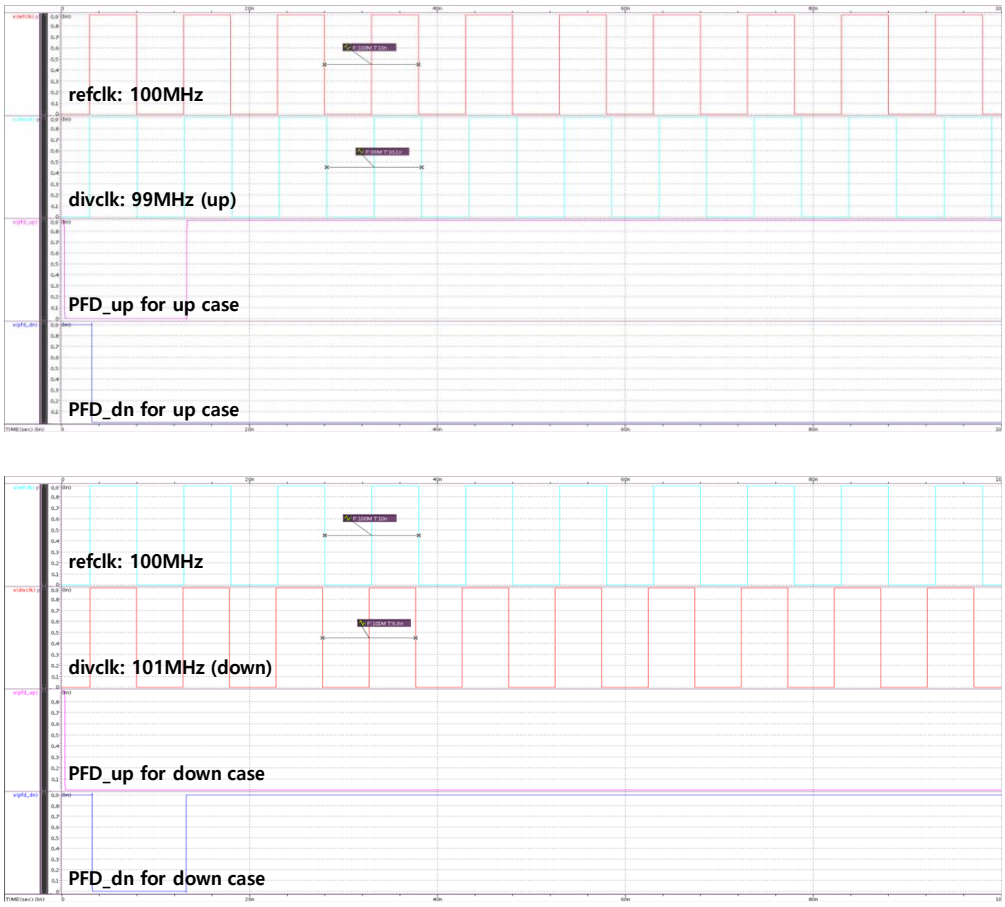


Fig. 3.8 (a) PFD Up (DIVCLK = 99 MHz) (b) PFD Down (DIVCLK = 101 MHz)

3.3.2 DCO

The DCO in this proposed AD-PLL consists of a resistor-controlled DAC [13] and a pseudo-differential four-stage ring oscillator. The former is implemented with a 32 ×32 current source array as shown in Figure 3.9. This Digitally-Controlled Resistor

(DCR), tunes the supply voltage of the subsequent ring oscillator by altering its resistance. This is done with a segmented thermometer scheme and glitch-reduction decoding, which enables the serpentine switching as shown in the arrow in Figure 3.9. It is noteworthy that only one switch is turned on and off at both column and row boundaries, thus minimizing the thermal switching noises at all possible codewords. Another benefit of using such a scheme is that the number of bits economizes, where high coding cost was the problem of a conventional thermometer coding scheme. Rather than using 2^N bits of code to represent 2^N values, it requires only $2^{N/2+1}$ bits of code by using binary to thermometer decoding. To enable such a decoding scheme, the decoding cells are divided into even and odd cells, and their implementation is presented in Figure 3.10.

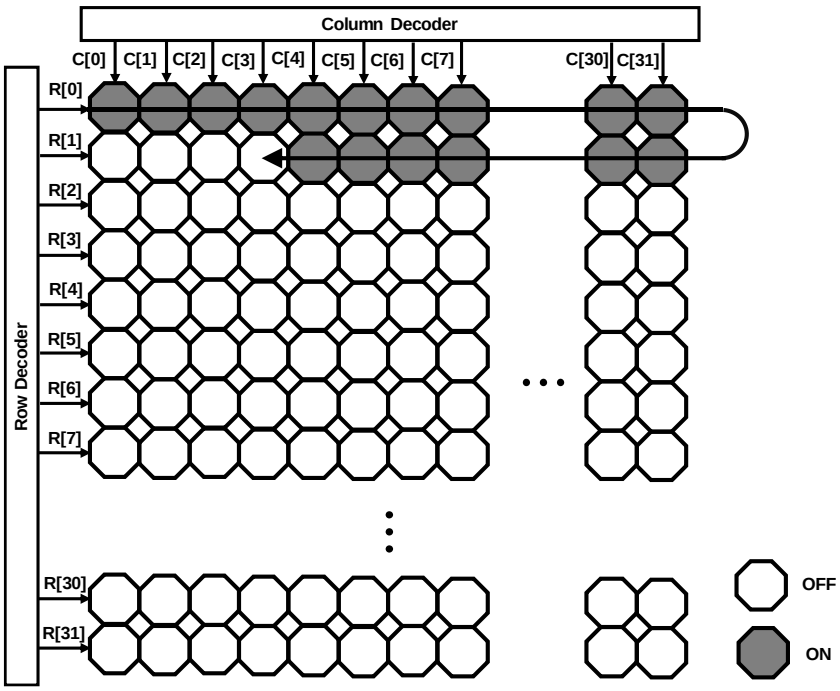


Fig. 3.9 DCR Structure in Diagram

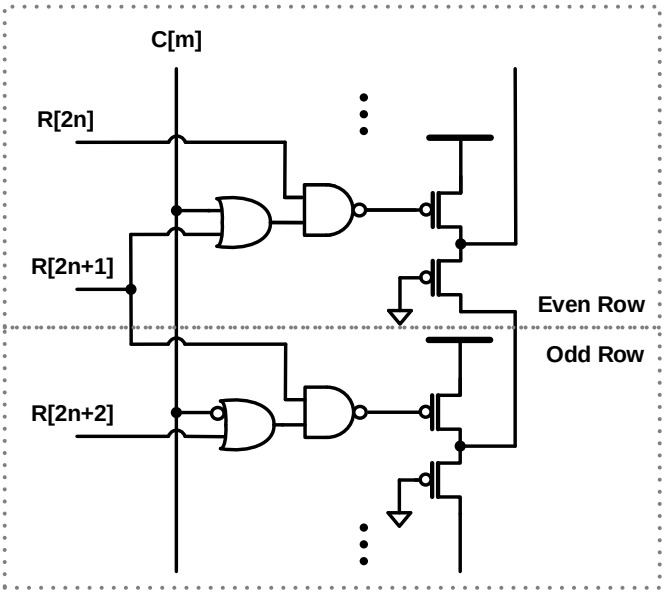


Fig. 3.10 Even and Odd Cell Structure in DCR

The detailed operation of DCR is as follows. To begin with, the 10-bit FCW ranging from 0 to 1023 in decimal is decoded as in Equation (3.1), where R denotes the number of inputs from the row decoder, and C denotes the number of inputs from the column decoder. Then the DCR turns on all the PMOS transistors in the first R rows and then turns on all the parallel C PMOS transistors in the next (R+1)-th row. By doing so, the whole PMOS transistors in the DCR act like resistances. The equivalent resistance model of DCR is given in Figure 3.11, and the total equivalent resistance is expressed as Equation (3.2). Note that if the values of series resistances in the row cells are monotonically decreasing as R increases, the approximation in Equation (3.3) holds under this assumption. Then the R_{top} term in Equation (3.2) reduces to R_{s0}, which is the series resistor of the first-row cell. Thus, to guarantee sufficient linearity

in the frequency control, the monotonicity of the series resistance in the row decoders is crucial. Besides, the typical values for parallel resistance are much higher than the series resistance and are equally sized to maintain the monotonic linear decrement of voltage drop in the DCR as the FCW decreases.

$$FCW = R \cdot 32 + C \ \ (R, C = 0{\sim}31) \tag{3.1}$$

$$R_{tot} = R_{top} || R_{p0} || \cdots || R_{pC} + \sum_{i=R+1}^{31} R_{si} \tag{3.2}$$

$$R_{top} = R_{sR} + \sum_{i=0}^{R-1} R_{si} || R_{p0} || \cdots || R_{p31} \cong R_{s0}, \ R_p \gg R_s, \ R_{s0} > \cdots R_{s31} \tag{3.3}$$

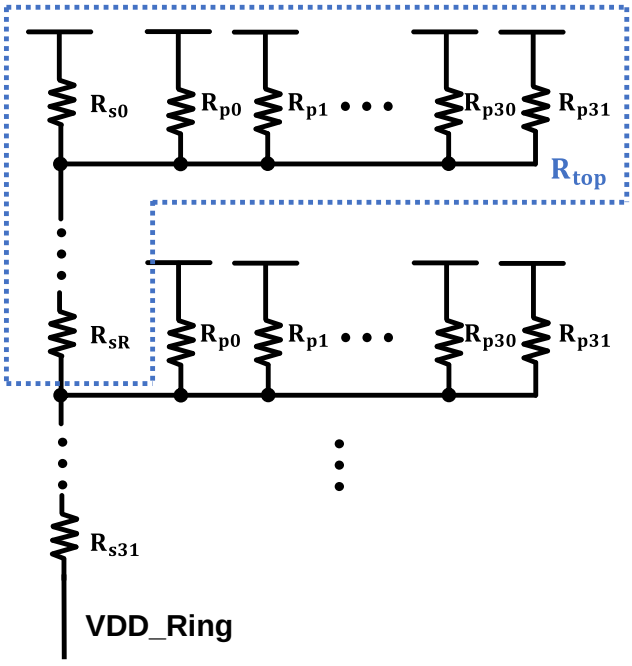


Fig. 3.11 Equivalent Resistor Model of DCR

Considering the characteristics of the target application, the oscillator core is implemented with a ring-type oscillator because of its advantages in generating wide-range and multi-phase clock pulses than an LC-type. Besides, although four-phase clock pulses are sufficient to support the half-rate clocking scheme [14], to leave room for bit-rate expandability and a margin for the phase interpolator, a four-stage ring oscillator is used instead of a two-stage ring oscillator. However, one might wonder how the oscillation starts with even numbers of delay stages because the system seems stable enough. The key to this mystery is the use of the cross-coupled inverter pairs between the main inverters, which keeps the output pseudo-differential. Since the addition of the cross-coupled inverter pairs causes an additional phase shift due to their hysteresis, the ratio between the size of the main inverter and the latched inverter should be determined with care. For implementation, the typical size of the latch for the four-stage pseudo-differential VCO, which is known to be 0.3 times that of the main inverter, is used to satisfy the Barkhausen oscillation criteria.

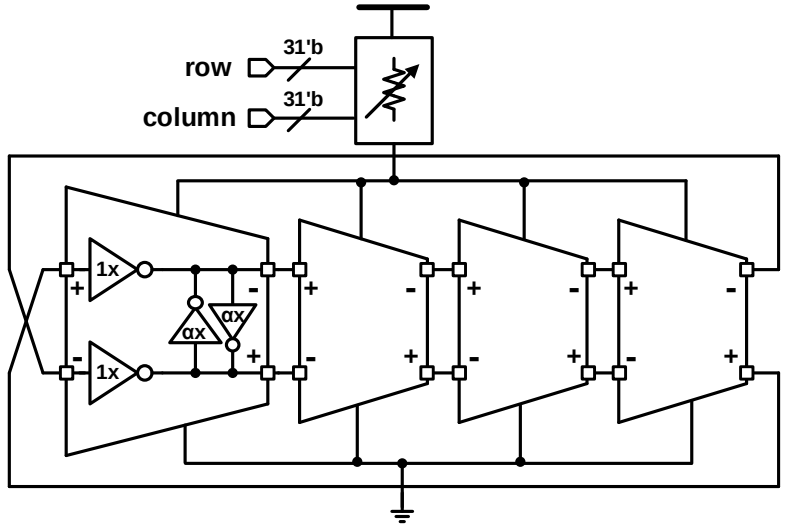


Fig. 3.12 DCO Structure

The overall DCO architecture is depicted in Figure 3.12. As the frequency control word increases, the equivalent total resistance decreases, thus the voltage drop at the supply voltage of the oscillator becomes smaller, generating output clock pulses with higher frequency. By subsequent simulations, the size of the oscillator that can cover the range from 1.5 GHz to 3 GHz in all PVT corners (TT: 0.9 V, 40 °, FF: 1.0 V, -5 °, SS: 0.8 V, 105 °) is found. Also, to improve linearity, the sizes of the series PMOS array in DCR are determined by utilizing the linear interpolation code with MATLAB. The DCR range simulation result is presented in Figure 3.13. Note that the shaded region is the 1.5 GHz to 3 GHz region, and to maintain low VCO gain at the target 2 GHz but also include that shaded region in all corners, the low code area is made deliberately lose some of its linearity. The total power for the designed DCO except buffer is 1.92 mW at 2 GHz target.

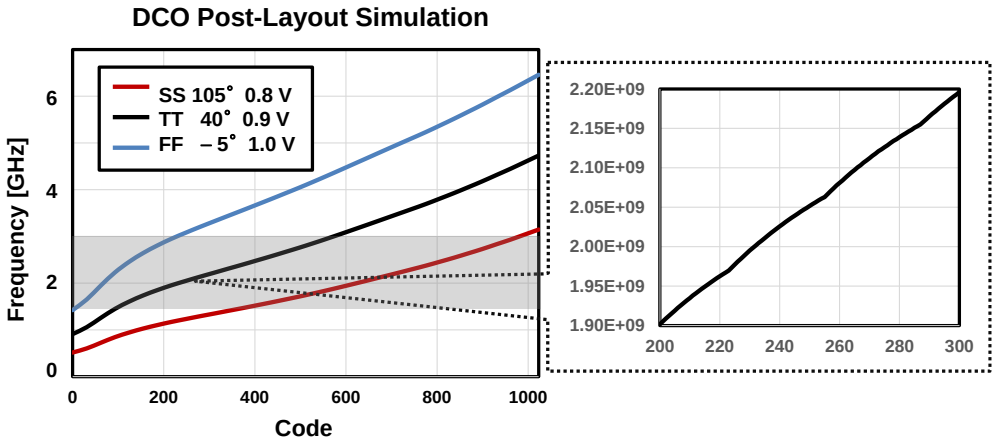


Fig. 3.13 DCO Frequency Range Post-Layout Simulation Results

3.3.3 Digital Block

Figure 3.14 shows the overall block diagram of the proposed digital block and Figure 3.15 illustrates its detailed architecture. The digital block takes inputs; which are the TDC thermometer code, TDC clock pulses, PFD up and down signals, and DLF clock pulses; then yields output 31-bit thermometer control codes of the row and column. As in Figure 3.14, the digital block first generates the internal CDCCLK by going through Clock Domain Crossing. Then with that clock pulses, it synchronizes the PFD UP/DN, and thermometer code. If PLL is frequency locked, where both of the PFD_UP and PFD_DN are zero, DLF converts 7-bit thermometer code and otherwise converts PFD_UP/DN signals into a 26-bit signed binary code. The highest bit of this signed binary code is allocated for the overflow control, and then the following lower 10 bits represent the integer bits and the next 15 bits for the fractional bits. Next, this is sent to the proportional and integral path of the DLF simultaneously, and the net outputs of the two paths are summed up. This aggregate goes through the DSM, undergoes a dithering process selectively, then outputs the 10-bit binary control code. The binary to thermometer code decoder decodes this output and produces the final 31-bit thermometer control codes of the row and column cells.

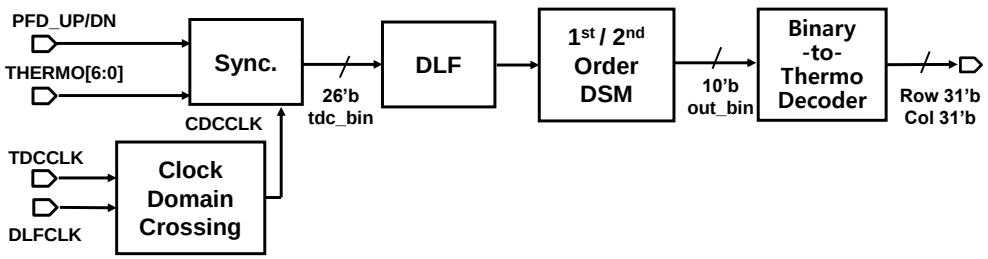


Fig. 3.14 Block Diagram of the Digital Block

Now let's take a detailed walk of the digital block through Figure 3.15. The first part of the digital block adjusts the metastability issue when the clock domain changes from one to another. Since the digital block operates based on the frequency of the DLFCLK, not that of the REFCLK, the analog TDC clock domain would be asynchronous to the digital clock domain. This traversal could cause an unreliable data transmission, thus a method to resolve such a problem must be implemented. The very simple way to solve this is to insert flip-flop chains before using the TDC clock pulses. By crossing these flip-flop chains, the TDC thermometer code is given enough time to settle before updating that code to the digital block. There's just one caveat that this process adds further loop delays, thus degrading the total jitter performance. However, this effect is leveraged by using a ten times faster digital clock than the reference clock, making the effective loop delay decrease tenfold. Besides, the number of flip-flops that the TDC clock undergoes is configurable with the CDC_CTRL signal.

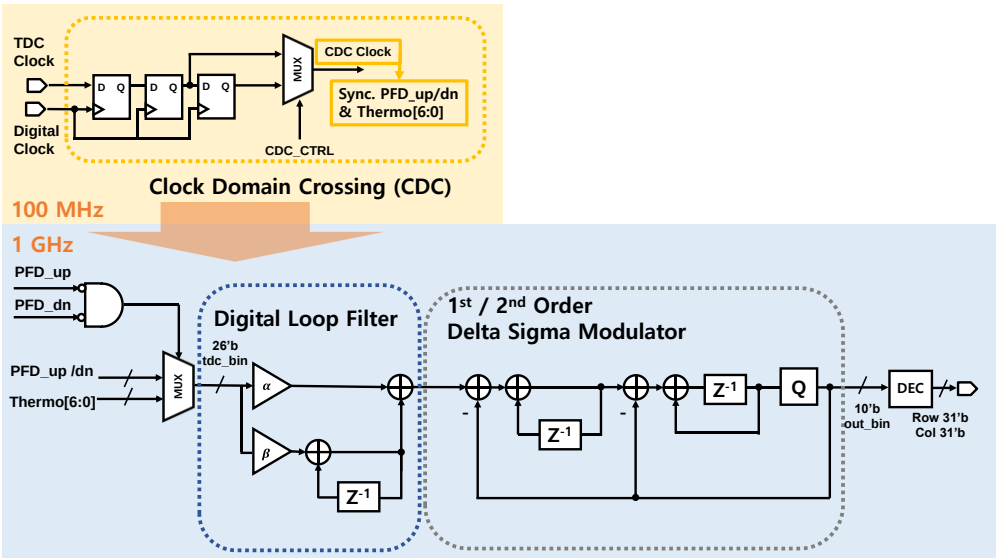


Fig. 3.15 Detailed Architecture of the Digital Block

Next, after passing Error Control Block that removes flips or bubbles in the TDC thermometer code, the DLF converts the 7-bit TDC thermometer code into 26-bit signed binary codes that correspond to the proportional gain α and the integral gain β. These gains are made configurable so that the loop bandwidth and stability of the PLL could be easily adjustable. As stated in the previous chapter, the loop bandwidth is proportional to the α, and the phase margin is proportional to the $\frac{\alpha}{\beta}$.

The last part of the digital block consists of the DSM and decoder. The DSM is designed to select between the first and second-order, where the higher the order the more randomized dithering signals are generated. By doing so, the quantization noises are effectively shaped and the in-band noise reduces. Each DSM stage is implemented with a multistage noise shaping (MASH) DSM which is a feed-forward structure. DSM gains, mode selection, and enable signals are set to be configurable from the outside to give some flexibility. Besides, the decoder takes the output 10-bit binary code and changes them to 31-bit thermometer control codes of the row and column cells. This final output controls the following DCR of the DCO. Note that the average power consumption of the digital block is 1.12 mW.

3.3.4 Level Shifting Buffer and Divider

To correct the duty cycle and to compensate for the slew rate of the output clock pulses from the oscillator, a well-designed buffer is needed. Besides, the other blocks in the transmitter and receiver that follows by the PLL are designed to have a higher

supply domain than that of the PLL, thus level shifting to 1.1 V rail-to-rail swing is also necessary. Also, note that a level shifting buffer is necessary to match the logic threshold of the subsequent inverter with the limited swing DCO output clock pulses for proper operation. For these reasons, the proposed AD-PLL utilizes the AC Coupled Resistive Feedback Inverter for buffering. Figure 3.16 shows the structure of the proposed level shifting buffer. This structure not only blocks the DC signal and changes the limited swing into a rail-to-rail swing, but also can correct the duty cycle and reduce the rise and fall time. Based on the AC simulation results, R_f = 80.4 kΩ, C_c = 104.7 fF are used for implementation and the AC gain at the target 2 GHz frequency is 34.6. Also, the inverter's PMOS to NMOS ratio is set to 2 considering the VTC curve of an inverter. The buffered output clock pulses show a phase noise of -101 dBc/Hz at 1 MHz offset and -116 dBc/Hz at 5 MHz offset. The phase noise plot is drawn in Figure 3.17. Also, at a 2 GHz locked state, the 8 phase clock pulses are distributed as Figure 3.18. They show a maximum of 1 ps phase differences and a duty cycle of 49.6 %. The power consumption of buffer at 2 GHz locked state is 1.02 mW. Note that this data is based on the post-layout simulation result at the TT condition, including dummy capacitors.

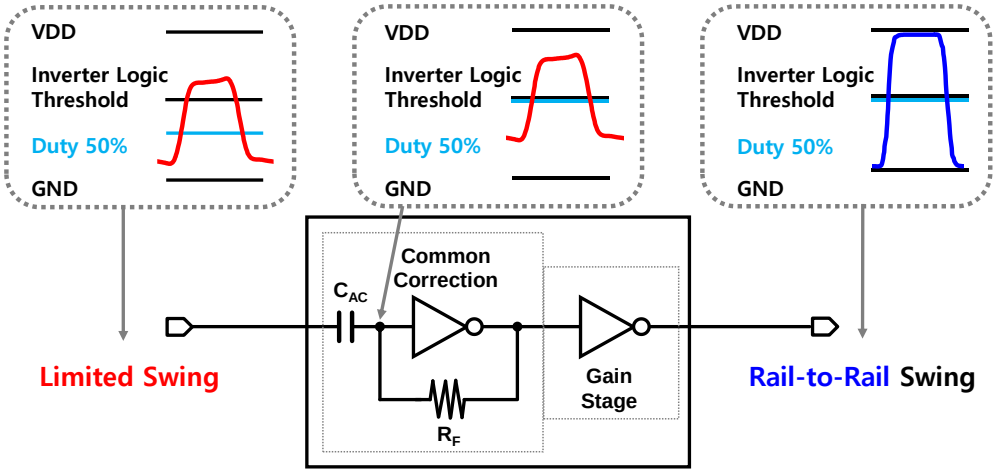


Fig. 3.16 AC Coupled Resistive Feedback Inverter Structure

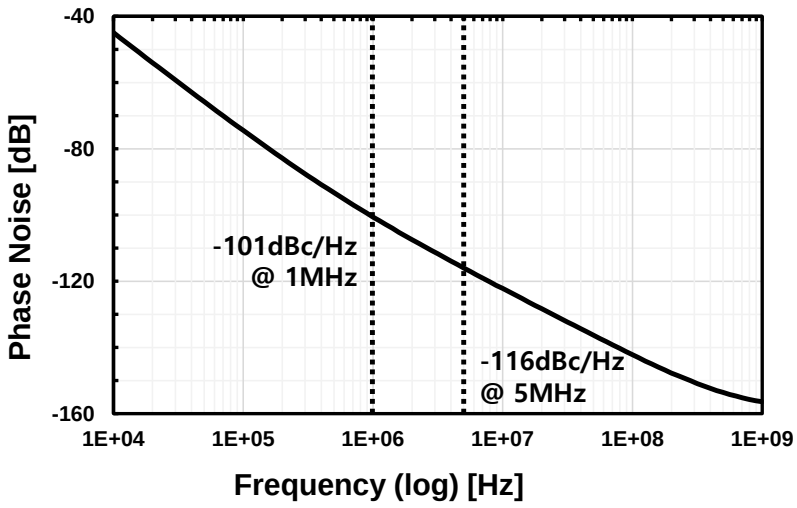


Fig. 3.17 Phase Noise Plot of the Output Clock Pulses (TT corner)

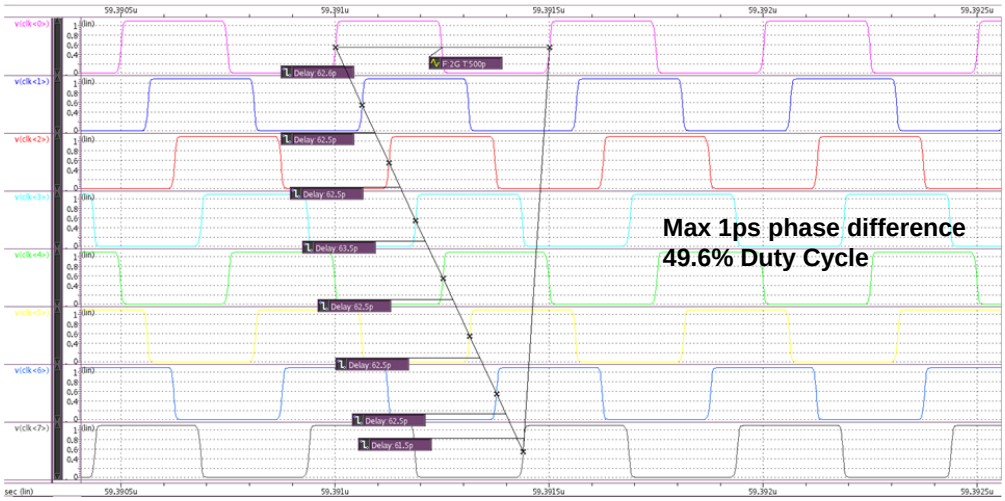


Fig. 3.18 Output Clock Pulses Skew based on the Post Simulation Results

To compare frequency and phase with the 100 MHz reference clock, the output clock has to be divided correspondingly. The divider does this function, thus generating the feedback clock of the loop. Considering the design specification of the target application, where the main target frequency output is 2 GHz, but also setting some margin from 1.5 GHz to 3 GHz, the divide ratio is set to /15, /20, /25, /30. When PLL is locked, these generate the output clock pulses of 1.5 GHz, 2 GHz, 2.5 GHz, 3 GHz respectively. Moreover, to generate a higher frequency for the DLF clock pulses, /2, /3, /4, /5 of the output clock frequency is used, producing 1 GHz, 667 MHz, 500 MHz, 400 MHz when the output clock is locked at 2 GHz. These divide ratio options are designed to be adjustable from the outside. Since a divide ratio can be represented as a product of prime numbers, the corresponding divider would be a cascaded version of the basic dividers which has a divide ratio of a prime number. Thus, the whole structure of the designed divider is represented in Figure 3.19. Note that the hold time

and set-up time violations of flip-flops are vulnerable to occur at a high frequency. Thus, to avoid a global convergence failure in the PLL, a frequency divider should be designed to cover the maximal frequency that the oscillator generates in every PVT corners. Therefore, the basic divider at the first stage should be designed with care.

By using the D-Flip-Flop based structure of Figure 3.20, the basic dividers with ratio /2, /3, /5 are designed. These basic dividers operate up to 14.5 GHz at TT corner, 8.6 GHz at SS corner, 21.6 GHz at FF corner. This operation range fully covers the frequency range of the proposed PLL with a sufficient margin. Besides, to reset the accumulated jitter due to the cascades of each stage and buffer, retiming is performed before producing the output DLFCLK and DIVCLK. The retiming options, which are DLF_RCLK, DIV_RCLK inversion selection, and retiming enable signals, are also configurable from the outside. The 2 GHz target clock generation post-layout simulation result is given in Figure 3.21. The input clock pulses fed into the divider are generated by the designed DCO and buffer. Note that the output clock pulses of the divide by 3 counter and the divide by 5 counter do not maintain the 50 % duty-cycle. However, since the designed PFD-TDC does not rely on the duty cycle, these output clock pulses do not deteriorate the whole system. The power consumption of the divider is 0.61 mW at the TT corner, including dummy capacitors.

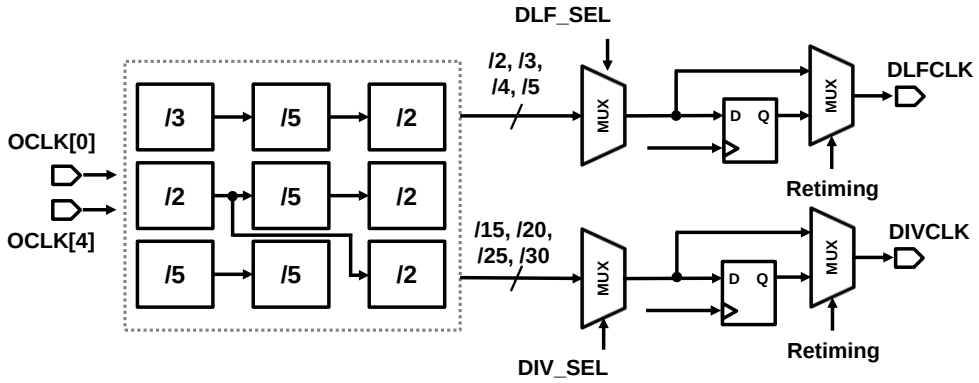


Fig. 3.19 Divider Structure

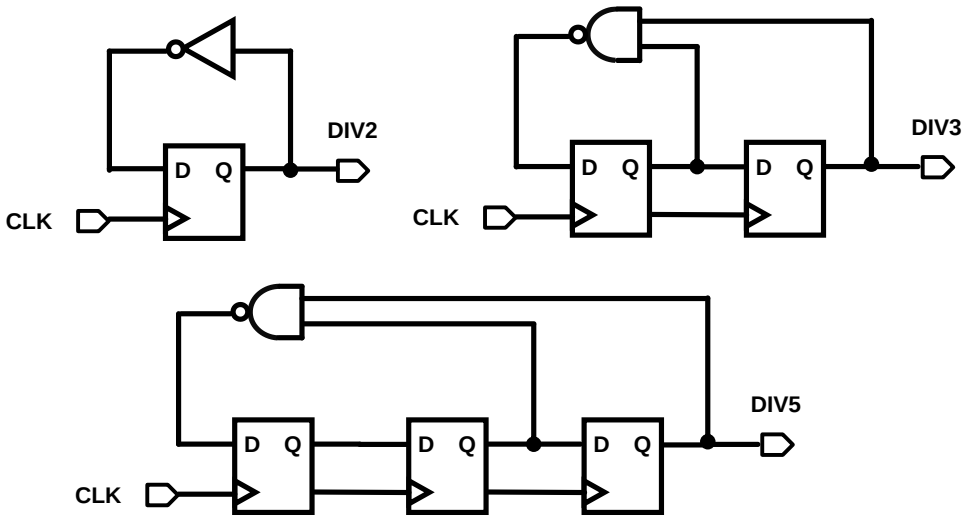


Fig. 3.20 (a) Divide by 2 (b) Divide by 3 (c) Divide by 5 Counter

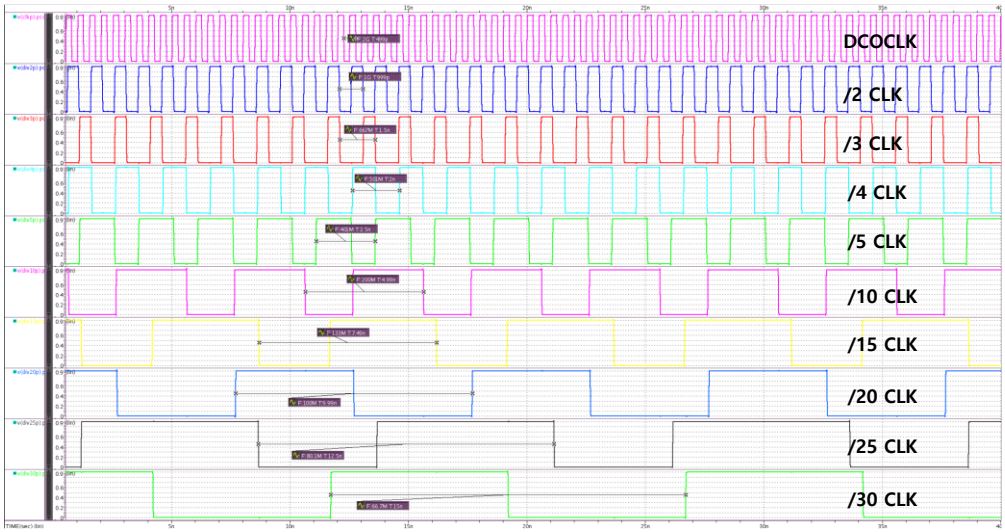


Fig. 3.21 Output Clock Pulses of the Divider based on the Post-Layout Simulation

Chapter 4

Measurement and Simulation Results

4.1 Die Photomicrograph

Figure 4.1 shows die photomicrographs of the transmitter and receiver of the automotive CIS interface and the enlarged photo of the proposed AD-PLL. The prototype chip is fabricated in a TSMC 40 nm GP CMOS process. Also, for the tape-out, the digital block written in the Verilog RTL code is synthesized and undergoes Place & Route process, and the other analog blocks are manually designed and routed. Dummy metals and decoupling capacitors (decaps) are densely placed around the blocks to reduce power supply noise and IR-drops. The total active area of the AD-PLL is 0.026 mm^2, where the DCO and the digital block occupied most of the area, taking up to

86.0 % of the total. The total power estimated by the post-layout simulation result is 5.18 mW at 2 GHz Locked state, where the power consumption of the DCO including buffer took up 56.8 % of the total and that of the digital block followed next which is 23.1 % of the total (TDC: 0.51 mW, Divider: 0.61 mW, DCO buffer: 1.02 mW, DCO except buffer: 1.92 mW, Digital block: 1.12 mW). Note that the nominal supply voltage of the DCO buffer is 1.1 V and 0.9 V for the other blocks.

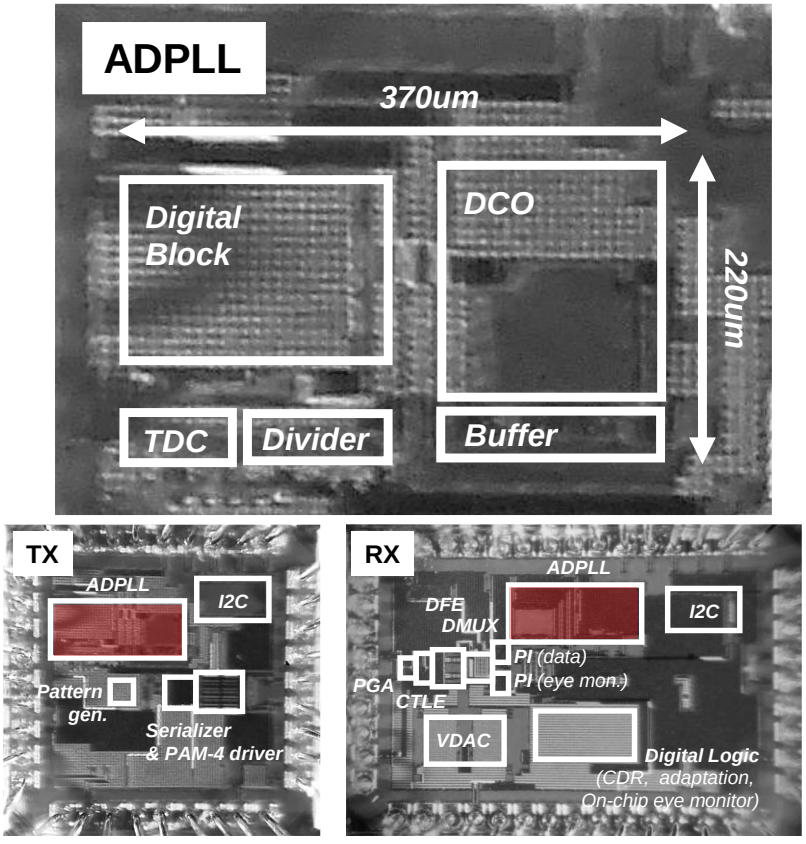


Fig. 4.1 Die Photomicrograph

4.2 Measurement Setup

The placement of proposed AD-PLL in the transmitter and receiver differs, thus the effect of different surrounding blocks, power routing schemes, and PAD arrangements would affect the performance of AD-PLL differently. Also, the PLL output clock signal passes series of repeaters and then in the transmitter, the Open-Drain Driver drives the signal to the outside, whereas in the receiver, the Current Mode Logic (CML) drives the signal to the outside. Figure 4.2 and Figure 4.3 shows the structures of the output driver of the AD-PLL clock. The main differences between the two drivers are in the 50 Ω impedance matching. CML is widely used in most high-speed data communication, because of its ease at impedance matching, thus reducing the effect of reflection. On the contrary, Open-Drain Driver has a more simple structure but more vulnerable to reflection. However, since the clock pulses are periodic, the effect of reflection is negligible. The Open-Drain Driver in the transmitter and the CML Driver in the receiver are designed to be adjustable, driving clock pulses up to about 500 mV voltage swing. Both are implemented considering the parasitic capacitance and inductance of the bonding wire.

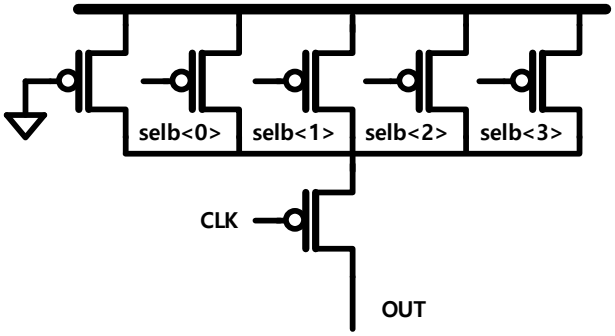


Fig. 4.2 Structure of Tx Open-Drain Driver

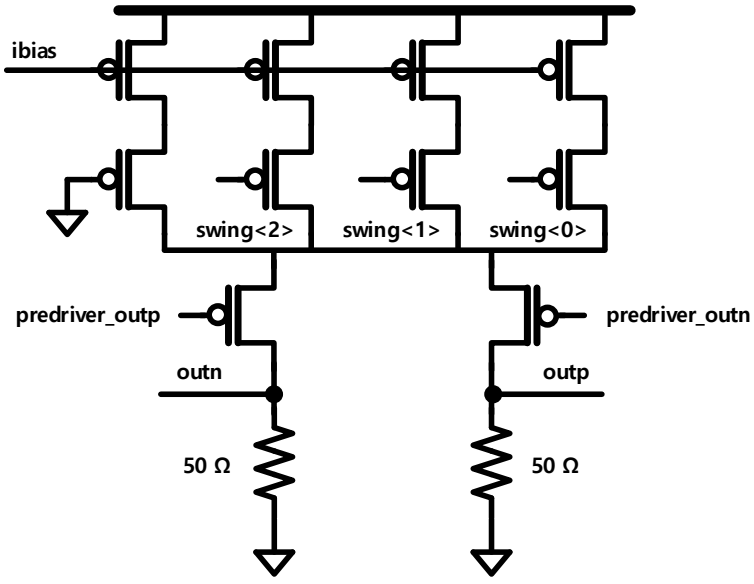


Fig. 4.3 Structure of Rx CML Driver

The equipment for the measurement is set up as in Figure 4.4. For phase noise analysis, Agilent E4440A PSA Spectrum Analyzer is used, and the 100 MHz reference clock is provided with the external crystal oscillator or by using Agilent E8267D Vector Signal Generator. Also, to measure peak-to-peak periodic jitter and to conduct

transient analysis, the Tektronix MSO 73304DX Mixed Signal Oscilloscope is utilized. To find optimal DLF gain that minimizes the RMS jitter of the proposed AD-PLL, python measurement automation code is written down and applied. By utilizing the Aardvark I2C to communicate with the chip and the LAN cable to communicate with the Spectrum Analyzer, the optimal gain and PLL options could be found without manual tuning. The measurement environment setting for the transmitter and the receiver is identical.

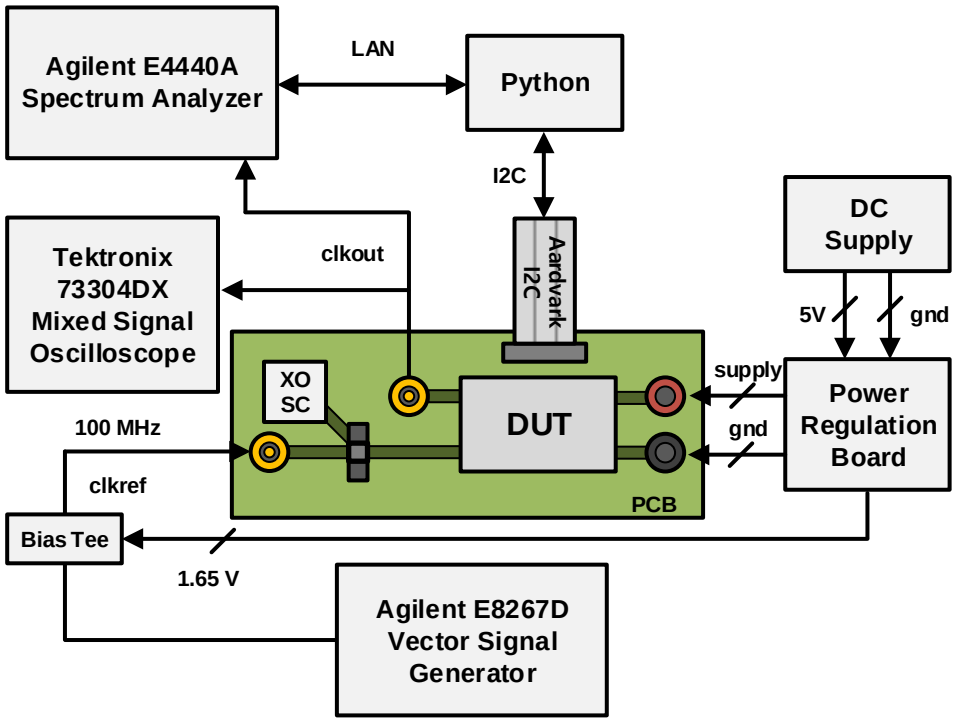
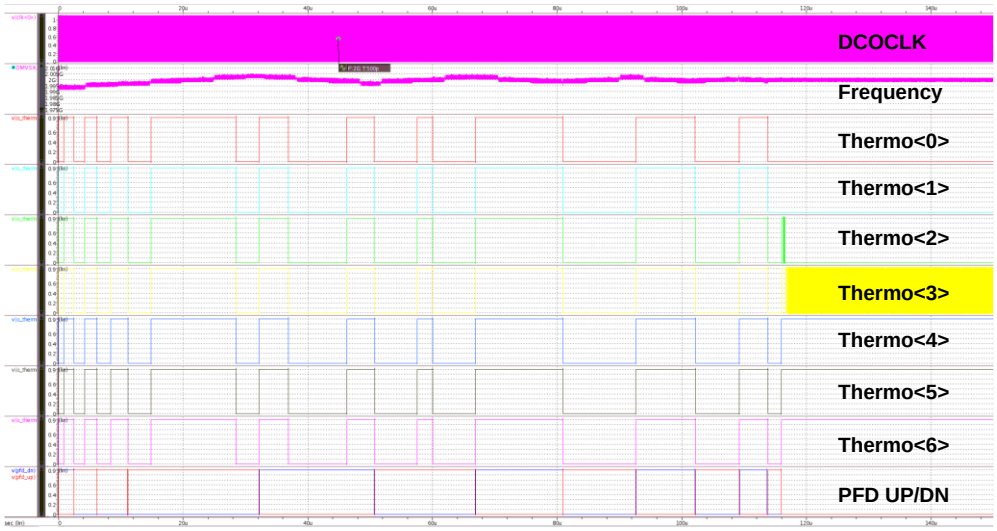


Fig. 4.4 Measurement Environment Set-up

4.3 Transient Analysis

The frequency tracking and locking behavior are simulated with FineSim, based on the post-layout data of the whole AD-PLL. Figure 4.5 (a) shows the frequency tracking behavior when the initial frequency is lower than the 2 GHz target frequency (up), and Figure 4.5 (b) shows that behavior when the initial frequency is higher than the 2 GHz target frequency (down). The DLF gain configuration in both cases is set to $\alpha = 2^{-7}$, $\beta = 2^{-13}$. As notable in Figure 4.5, the frequency is locked to target frequency within 1 bit TDC thermometer code, whose resolution is only 2.5 ps. Besides, since the PFD_up and PFD_dn signals go high alternatively in the up case, it takes more time to be locked compared with the down case. Note that there is some inaccuracy with FineSim, like some discontinuities and ripples in the simulated waveforms.



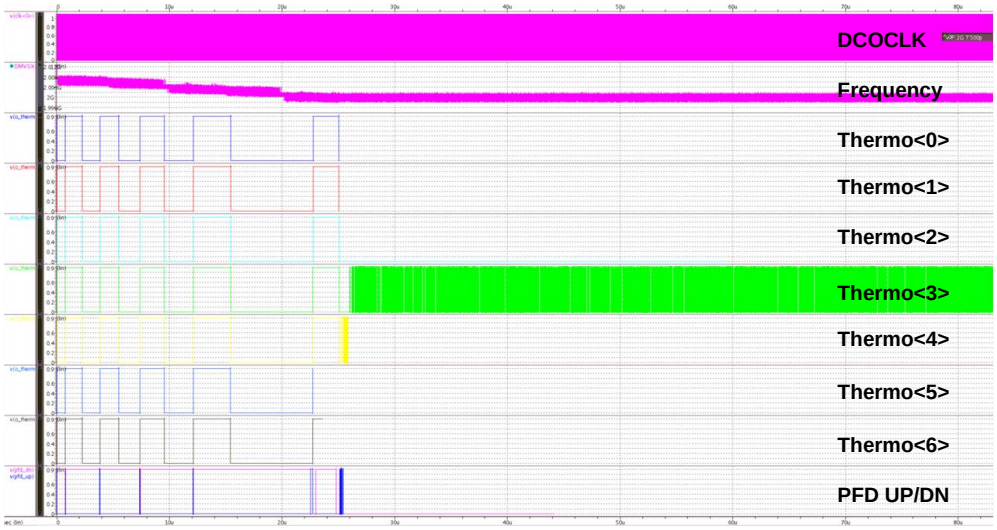


Fig. 4.5 Frequency Tracking Behavior at (a) Up (b) Down Case FineSim

4.4 Phase Noise and Spur Performance

4.4.1 Free-Running DCO

With MSO 73304DX Mixed Signal Oscilloscope, the output clock pulses of free-running DCO are measured. The frequency range of the output clock pulses at the transmitter is from 715 MHz to 3.7 GHz with an output swing of 520 mVpp, and that of the receiver is from 694 MHz to 3.5 GHz with an output swing of 320 mVpp. Compared with the post-layout simulation result at the TT corner, whose frequency range is from 909 MHz to 4.73 GHz, output clock pulses of both the transmitter and the receiver slowed down overall. The free-running output clock pulses of DCO at the transmitter and the receiver in the minimum, 2 GHz, and maximum code are presented in Figure 4.6.

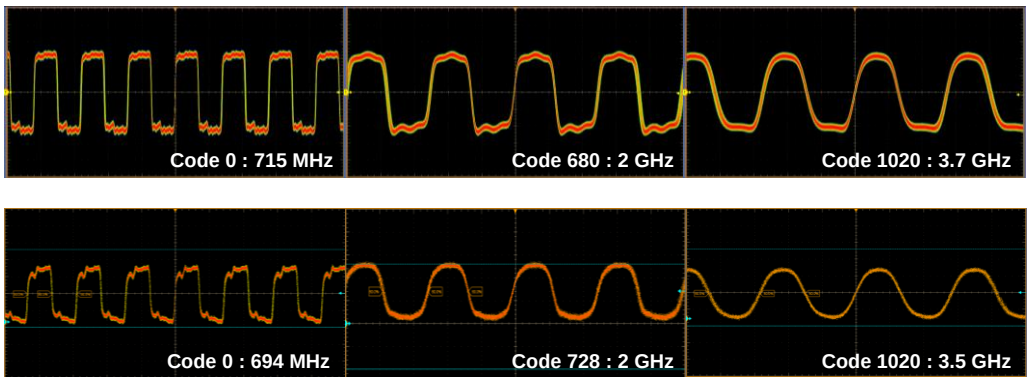


Fig. 4.6 Min/Target/Max Free-Running DCO clock pulses of (a) Tx (b) Rx

In addition, with Agilent E4440A PSA Spectrum Analyzer, the phase noise plot and the frequency spectrum plot are driven. As in Figure 4.7, the phase noise of the free-running 2 GHz output clock pulses at the transmitter is -99.74 dBc/Hz at 1MHz offset and -122.58 dBc/Hz at 10 MHz offset, and the receiver side's performance is alike. This is almost the same as the post-layout simulation result, which showed -100.56 dBc/Hz at 1 MHz offset and -122.19 dBc/Hz at 10 MHz offset. Bear in mind that the flat region at the low frequency is due to the measuring limitation of the equipment. Besides, the spectrum analysis with 400 MHz spans at the 2 GHz center frequency is as in Figure 4.8. The main spurs are at 50 MHz, 100 MHz, 200 MHz, where the 50 MHz spur disappears when the I2C clock and USB are off, and the other two remain. Note that the relative magnitude of the spur at 100 MHz is -45 dBc from the center and that at 200 MHz is – 35 dBc from the center. The situation is similar at the receiver side, having reference spur at 100 MHz harmonics.

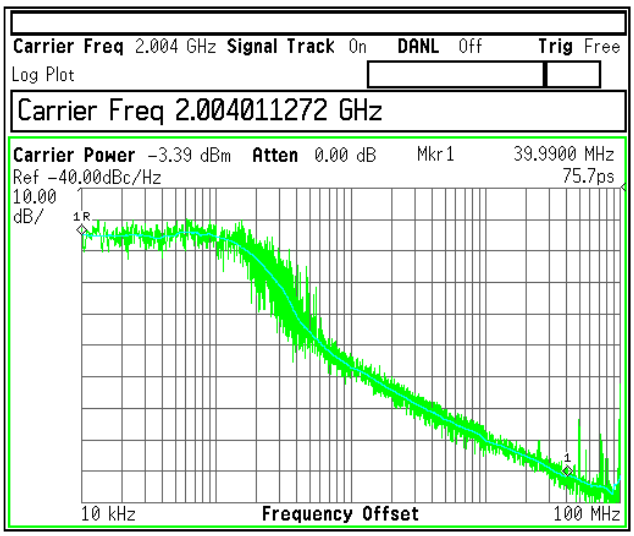


Fig. 4.7 Phase Noise Analysis of 2 GHz Free-Running Clock Pulses

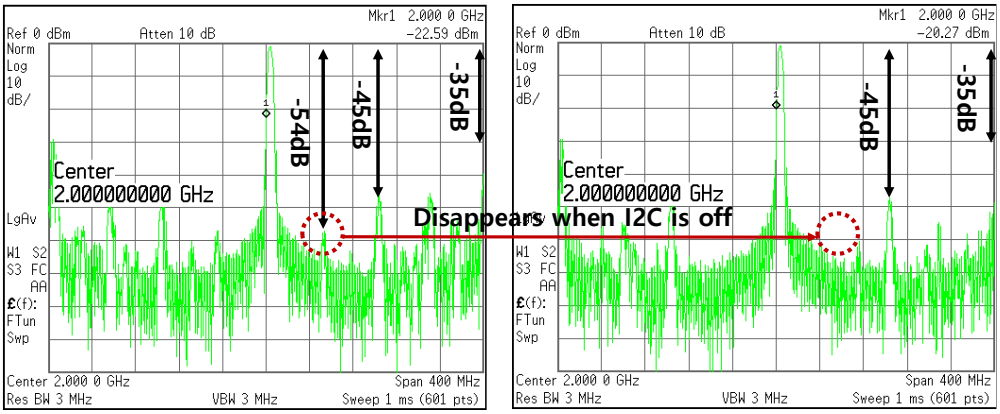


Fig. 4.8 Spectrum Analysis of 2 GHz Free-Running Clock Pulses

4.4.2 PLL Performance

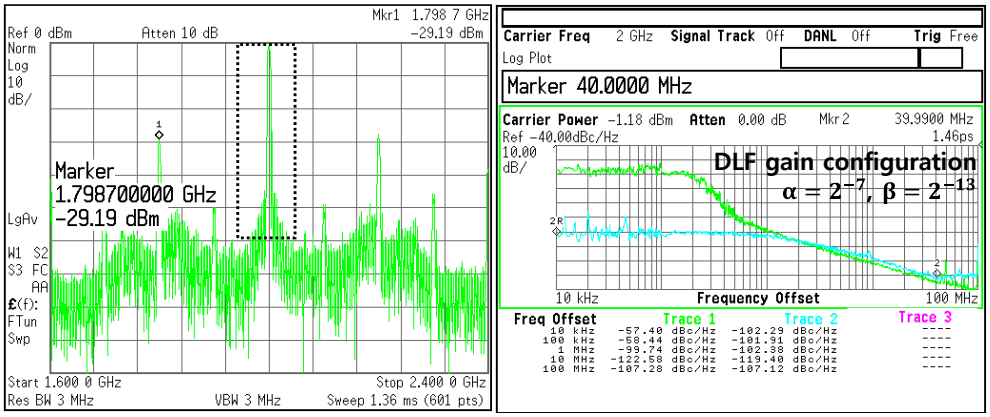


Fig. 4.9 (a) Spectrum Analysis (b) Phase Noise Analysis of 2 GHz Locked Case

When the PLL is locked to the target 2 GHz frequency, as in Figure 4.9 (a), there is a noise reduction in the vicinity of the center frequency compared to the free-running case. However, since the proposed PLL does not have an additional spur

reduction scheme, the 100 MHz reference harmonics still exist. In phase noise analysis shown in Figure 4.9 (b), there is a significant reduction of power at the frequency offset lower than the PLL bandwidth compared to the free-running case.

In terms of the integrated RMS jitter, the actual measured performance is slightly different from the optimal result of FineSim and mathematical modeling. In FineSim the integrated RMS jitter is 995 fs with the DLF gain of $\alpha = 2^{-7}$, $\beta = 2^{-13}$, whereas the actual RMS jitter integrated from 10 kHz to 40 MHz for that gain is 1.25 ps. The estimated PLL loop bandwidth is 1.05 MHz, however, as in Figure 4.10(a), it is slightly larger at the measurement. Also, as addressed in the previous chapter, the minimum RMS jitter is 843 fs and peaking is less than 1 dB with a gain of $\alpha = 2^{-5}$, $\beta = 2^{-11}$ in mathematical modeling. On the contrary, as in Figure 4.10(b), the PLL loop bandwidth, peaking, and integrated RMS jitter all increase at the measurement. These gaps are assumed to be the effect of change in DCO range, DCO phase noise, and reference noise at actual measurement.

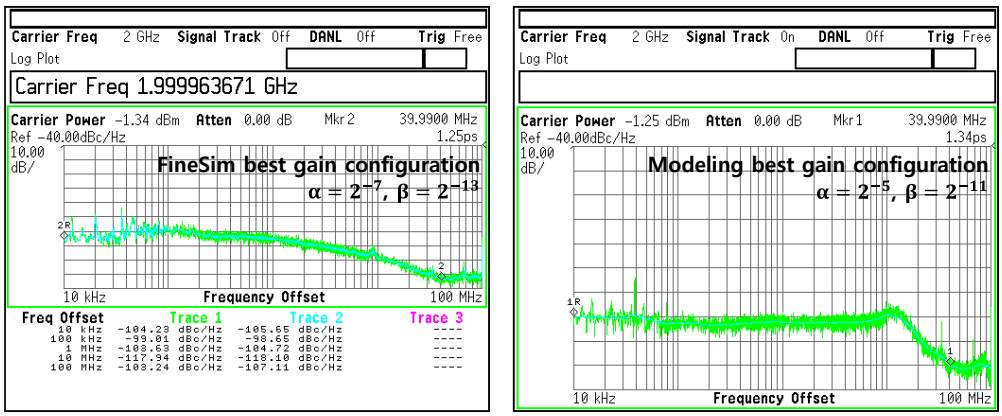


Fig. 4.10 Phase Noise Analysis with Optimal Gain (a)FineSim (b)Mathematical Modeling

Various mode configurations, such as TDC error-control mode; BB mode and gain configuration; DLF retiming and clock inversion; DSM order and gain configuration; and PCB decap variations are tested before applying python measurement automation code for finding the optimal result. Then by utilizing the measurement automation code, the optimal gain is derived. Figure 4.11 shows the two-dimensional gain sweep results in terms of the integrated RMS jitter calculated from 10kHz to 40MHz, and Figure 4.12 shows the spectrum analysis and the phase noise analysis of the optimal case ($\alpha = 2^{-6},\ \beta = 2^{-11}$). The optimal integrated RMS jitter from 10 kHz to 40 MHz is 827 fs. With MSO 73304DX Mixed Signal Oscilloscope, a detailed analysis of jitter is conducted. As shown in Figure 4.13, the peak-to-peak absolute jitter (TIE) is 22.9 ps. Here, the deterministic jitter accounts for a significant amount of the total, which is an artifact of board design. Thus, by carefully redesigning the PCB, bearing in mind to reduce power supply ripple, crosstalk, and ground bouncing, TIE would reduce significantly. Besides, note that the RMS jitter measured with the oscilloscope is higher than that of the Spectrum Analyzer. This difference accounts to be the effect of self-triggering at the oscilloscope when measuring and the error of not fully integrating the phase noise at the spectrum analyzer.

In addition, the external crystal oscillator yields lower jitter output clock pulses than with the reference clock produced by the Vector Signal Generator. Besides, the PLL's RMS integrated jitter performance is similar in both the transmitter and the receiver, but the latter is slightly better which is largely attributable to the difference in the placement and power routing schemes (higher internal power decaps).

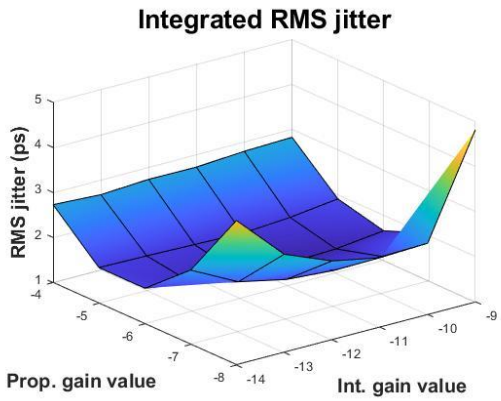


Fig. 4.11 Integrated RMS Jitter Measured by 2D DLF Gain Sweep Automation Code

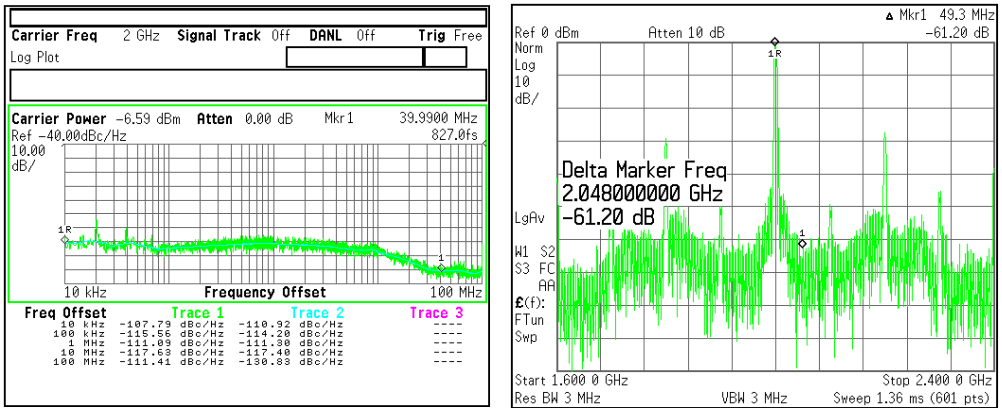


Fig. 4.12 Phase Noise Analysis and Spectrum Analysis with the Best DLF Gain

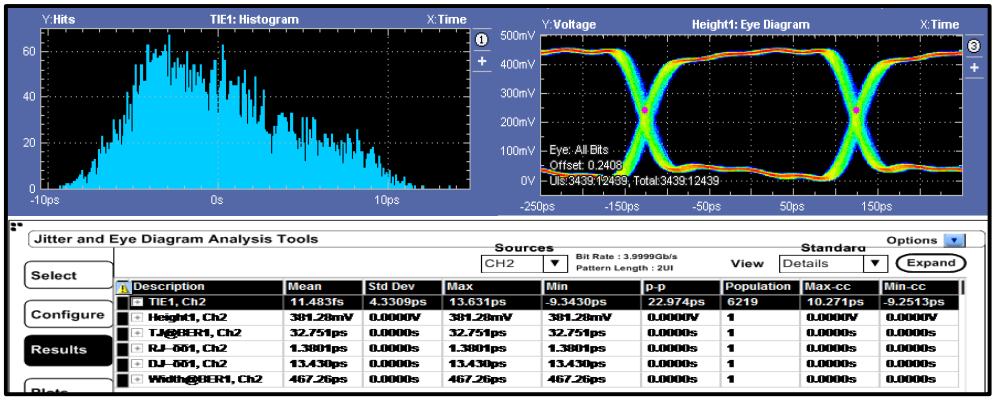


Fig. 4.13 Jitter Analysis with the Best DLF Gain

4.5 Performance Summary

The proposed AD-PLL in this thesis takes up the area of 0.026 mm^2, and the total power dissipated including the digital block is 7.35 mW, and excluding the digital block is 4.68 mW at 2 GHz locked state. Underline that digital power consumption includes the power consumption of digital blocks other than that of PLL. Thus, the total AD-PLL power consumption is estimated as 5.8 mW, summing the digital block power based on the simulation and the measured power of the analog blocks. Note that the power consumption is higher than expected (Total Post-Layout Simulation Power Consumption: 5.18mW, TDC: 0.51 mW, Divider: 0.61 mW, DCO buffer: 1.02 mW, DCO except for the buffer: 1.92 mW, Digital Block: 1.12 mW). This increase in power consumption would be attributable to the effect of process variation and the unexpected parasitic components.

Table 4.1 summarizes the performance of the proposed AD-PLL and offers a comparison with other similar works that use Ring Oscillators as a core oscillator. By using 7 stage TDC in this work, the total area and power have economized. Although the power consumption at the buffer and the divider has more than a little room for optimization, in terms of FoM, it is comparable to the other related works in Table 4.1.

Table 4.1 Performance Comparison

	JSSC'16 [14]	TCASII'14 [15]	ASSCC'15 [16]	ISSCC'14 [17]	TCASII'15 [18]	VLSI'16 [19]	**This Work**
Technology	65-nm	90-nm	40-nm	40-nm	65-nm	40-nm	**40-nm**
Type	CP-PLL	AD-PLL	AD-PLL	AD-PLL	AD-PLL	ILCM	**AD-PLL**
f_{OUT} (GHz)	10	6.0	5.0	2.4	2.5	1.4	**2.0**
f_{REF} (MHz)	625	375	250	26	25	180	**100**
Power (mW)	7.6	11.6**	3.34	6.4	5	2.8	**5.8*** **
Supply (V)	1.2	1.0	1.1	1.1	1.2	1.1	**0.9**
Area (mm^2)	0.009	0.4	0.005	N/A	0.038	0.061	**0.026**
Ref. Spur (dBc)	−58	N/A	−51	−75	N/A	−59	**−45**
$Jitter_{rms}$ (fs)	414	828	1242	3290	1720	450	**827**
FoM_{jit} (dB)*	−238.8	−231.0	−232.9	−221.6	−228.3	−242.5	**−234.0**

* $FoM_{jit}(dB)=10 \cdot \log\left[\left(\frac{jitter_{rms}}{1s}\right)^2 \cdot \left(\frac{Power}{1mW}\right)\right]$

** Excluding power for spread spectrum clock

*** Digital block power consumption of the simulation was used for calculation

Chapter 5

Conclusion

In this thesis, the design techniques for AD-PLL assisting the automotive CIS interface are proposed. To target Gear 3 of the automotive physical system, the proposed AD-PLL has a wide operation range, low RMS jitter, and high PVT tolerance characteristics.

Based on the loop dynamics and the noise analysis of AD-PLL, optimized DLF gain configurations could be found. Also, through realistic behavior modeling simulation, accurate output responses and performance are predictable. The design techniques to reduce the output RMS jitter, such as using high-resolution TDC, first and second-order DSM, and faster frequency for the digital clock domain, are utilized for implementation. The proposed AD-PLL is fabricated in the 40 nm CMOS process and occupies 0.026 mm^2. The PLL output clock pulses exhibit an RMS jitter of 827 fs. Although there's enough room for power optimization, the proposed AD-PLL displays comparable jitter performance and FoM with those of the other contemporary researches.

Bibliography

[1] G.W. den Besten, "Single-Pair Automotive PHY Solutions from 10Mb/s to 10Gb/s and Beyond," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, pp. 474-475, Feb. 2019.

[2] V. Kratyuk, P. K. Hanumolu, K. Ok, U. Moon and K. Mayaram, "A Digital PLL With a Stochastic Time-to-Digital Converter," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 8, pp. 1612-1621, Aug. 2009.

[3] M. Z. Straayer and M. H. Perrott, "A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping," IEEE Journal of Solid-State Circuits, vol. 44, no. 4, pp. 1089-1098, Apr. 2009.

[4] P. Dudek, et al., “A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line,” IEEE Journal of Solid-State Circuits, vol.35, no.2, pp. 240-247, Feb. 2000.

[5] P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of Charge-Pump Phase-Locked Loops," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

[6] V. Kratyuk, P. K. Hanumolu, U. Moon and K. Mayaram, "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-

Loop Analogy," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 3, pp. 247-251, Mar. 2007.

[7] B. Razavi, "The Delta-Sigma Modulator [A Circuit for All Seasons]," IEEE Solid-State Circuits Magazine, vol. 8, no. 2, pp. 10-15, Spring 2016.

[8] R. E. Best, "Phase-Locked Loops: Design, Simulation, and Applications," 5th Edition. McGraw-Hill, New York, NY, 2003.

[9] M. H. Perrott, M. D. Trott and C. G. Sodini, "A Modeling Approach for Σ-Δ Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis," IEEE Journal of Solid-State Circuits, vol. 37, no. 8, pp. 1028-1038, Aug. 2002.

[10] R. B. Staszewski and P. T. Balsara, "All Digital Frequency Synthesizer in Deep-Submicron CMOS, " Jon Wiley & Sons Inc., 2006.

[11] D. H. Oh, K. J. Choo and D. K. Jeong, "Phase-Frequency Detecting Time-to-Digital Converter," Electronics Letters, vol. 45, no. 4, pp. 201-202, Feb. 2009.

[12] B. Nikolic, V. Stojanovic, V. G. Oklobdzija, W. Jia, J. Chiu and M. Leung, "Sense Amplifier-Based Flip-Flop," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, San Francisco, CA, pp. 282-283, Feb. 1999.

[13] H. S. Song, D. S. Kim, D. H. Oh, S. H. Kim and D. K. Jeong, "A 1.0–4.0-Gb/s All-Digital CDR with 1.0-ps Period Resolution DCO and Adaptive Proportional Gain Control," IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp. 424-434, Feb. 2011.

[14] W. R. Bae, H. R. Ju, K. S. Park, S. Y. Cho and D. K. Jeong, "A 7.6 mW, 414 fs RMS-Jitter 10 GHz Phase-Locked Loop for a 40 Gb/s Serial Link Transmitter Based on a Two-Stage Ring Oscillator in 65 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2357-2367, Oct. 2016.

[15] J. H. Yang, J. Y. Lee, S. J. Lim and H. M. Bae, "Phase-Rotator-Based All-Digital Phase-Locked Loop for a Spread-Spectrum Clock Generator," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 11, pp. 880-884, Nov. 2014.

[16] C. Chiang, C. Huang and S. Liu, "A Digital Bang-Bang Phase-Locked Loop with Bandwidth Calibration," IEEE Asian Solid-State Circuits Conference (ASSCC), Xiamen, Nov. 2015, pp. 1-4.

[17] Y. Huang, C. Liang, H. Huang and P. Wang, "15.3 A 2.4GHz ADPLL with Digital-Regulated Supply-Noise-Insensitive and Temperature-Self-Compensated Ring DCO," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, San Francisco, CA, pp. 270-271, Feb. 2014.

[18] S. C. Jang, S. W. Kim, S. H. Chu, G. S. Jeong, Y. S. Kim and D. K. Jeong, "An Optimum Loop Gain Tracking All-Digital PLL Using Autocorrelation of

Bang–Bang Phase-Frequency Detection," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 9, pp. 836-840, Sept. 2015.

[19] Y. S. Lee, H. I. Yoon, M. Kim and J. H. Choi, "A PVT-Robust −59-dBc Reference Spur and 450-fs RMS Jitter Injection-Locked Clock Multiplier using a Voltage-Domain Period-Calibrating Loop," IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, pp. 1-2, Jun. 2016.

초 록

본 논문에서는 자동차 CMOS 이미지 센서 (CIS) 인터페이스를 지원하는 AD-PLL 을 제안한다. Automotive Physical 시스템의 Gear 3 를 지원하기 위해 제안된 AD-PLL 은 1.5 GHz 에서 3 GHz 의 동작 주파수를 가지며, 낮은 RMS Jitter 및 PVT 변화에 대한 높은 둔감성을 갖는다.

설계에 앞서서 Matlab 및 Verilog Behavioral Simulation 을 통해 Loop system 의 역학에 대한 자세한 분석 및 AD-PLL 의 Noise 분석을 수행하였고, 이 분석을 기반으로 최적의 DLF gain 과 정확한 출력 응답 및 성능을 예측할 수 있었다. 또한, 출력의 Phase Noise 와 RMS Jitter 를 줄이기 위한 설계 기법을 자세히 다루고 있으며 이를 실제 구현에 활용했다.

제안된 회로는 40 nm CMOS 공정으로 제작되었으며 Decoupling Cap 을 제외하고 0.026 mm^2 의 유효 면적을 차지한다. 측정된 출력 Clock 신호의 RMS Jitter 값은 2 GHz 에서 827 fs 이며, 총 5.8 mW 의 Power 를 소비한다. 이 때, 전체적인 공급 전압은 0.9 V 이며, Buffer 의 Power 만이 1.1 V 를 사용하였다.

주요어 : 올-디지털 위상 동기화 루프 (AD-PLL), 시간 디지털 변환기 (TDC), 디지털 제어 발진기 (DCO), 디지털 루프 필터 (DLF), 델타 시그마 변조기 (DSM), 위상 잡음 분석

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