Ph. D. DISSERTATION

Analysis on Hot Carrier Degradation (HCD) Reliability in FinFET Devices

핀펫 소자에서의 핫캐리어 신뢰성 분석

BY

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ABSTRACT

CMOS logic devices have been scaled down to improve performance. However, the operating voltage is not sufficiently reduced compared to the scale down in physical dimensions. Therefore, since the electric field and temperature of the device gradually increase, reliability is still a critical issue in logic devices. Recently, many studies on the reliability of 3D devices are being conducted, but most of the studies are related to empirical modeling. Therefore, in this study, based on the actual measurement results, the hot carrier degradation(HCD) reliability of the logic device was analyzed focusing on the physical theory using Technology computer-aided design (TCAD) simulation.

First, electron-electron scattering(EES) was applied to the TCAD simulation to improve the accuracy of the hot carrier model. Additionally, calibration between the measurement data of 14 nm node FinFET and the model was performed to confirm the consistency. The calibration process required various voltage and temperature conditions to account for all scattering mechanisms. Therefore, HCD was analyzed according to various voltage conditions, and the parameters of the HCD model were extracted by calibration process. Next, temperature dependence under various HCD conditions was analyzed. Unlike oxide traps, interface traps show different temperature dependence depending on HCD voltage conditions. Therefore, the interface traps were separated into three components and the temperature dependence was analyzed for each component. Multiple particle process (MP) and Field enhanced thermal degradation process (FP) have a constant temperature dependence regardless of voltage conditions. On the other hand, the temperature dependence of Single particle process (SP) varies depending on the voltage condition because SP is affected by scattering. In the process of temperature dependence analysis,

calibration is also performed and parameters considering various voltages and temperatures were extracted through several iterations. The improved model to which the extracted parameters were applied showed more precise prediction of degradation compared to that of the previous model. As a results, accuracy of the HCD analysis was improved by establishing the HCD simulation framework based on physical theories.

However, since the self-heating effect of the acceleration condition and the operation condition are different, the HCD mechanism that occurs in the actual CMOS circuit may also be different. Therefore, we predicted the ratio of each component under operating condition.

Finally, in 10 nm node devices, we analyzed the cause of higher HCD in pFinFETs than in nFinFETs. Self-heating effect is severe in pFinFETs because SiGe is used as the source/drain material which makes the device temperature higher than nFinFETs. Theoretically, because the lifetime of multiple particle(MP) mechanism decreases as temperature increases, degradation due to MP decreases. Therefore, it is difficult for the HCD mechanisms to occur more in pFinFETs which has higher temperature than nFinFETs. However, in pFinFETs unlike nFinFETs, reaction-diffusion (RD) mechanism can occur in which holes react with the electrons of Si-H bonds to generate interface traps. Also, since RD deteriorates more as the temperature increases, the phenomenon that more degradation occurs in pFinFET than nFinFET can be explained by the RD mechanism. Therefore, we propose an additional RD mechanism that is caused by high device temperature in pFinFETs even in HCD condition. Main components were investigated through measurements of current degradation rate in various voltage conditions, and it

was found that RD is dominant in pFinFETs. Also, RD that can occur in HCD condition was predicted through TCAD simulation. As a results, degradation due to pure hot carriers without RD occurs more in nFinFETs than in pFinFETs.

Keywords: FinFET, Hot Carrier Degradation, Bias Temperature Instability, Reaction-Diffusion(RD), Self-heating

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CONTENTS

Chapter 1
Introduction

Hot carrier degradation (HCD) is a phenomenon that degrades performances such as subthreshold swing (SS), on-current, and V_{TH} due to the generation of defects at the Si/gate dielectric interface or inside the gate dielectric material [1-3]. Therefore, HCD is one of the representative issues of reliability and has been studied for decades. In the past, measurement of HCD was based on long-channel devices and HCD was explained as follows based on measurements; carriers with energy of over 3.7 eV break the Si-H bonds and generate interface traps [4, 5]. Therefore, the maximum electric-field was considered the most significant cause of HCD. However, because HCD kept occurring in low operation voltage HCD could not be explained in short channel devices with this HCD model [6]. Therefore, further studies have described HCD at low operating voltages through a new theory, the energy driven model [7, 8]. In short-channel devices, the degradation is determined by the energy of each carrier rather than the maximum field. Therefore, carriers with low energy can contribute to HCD through energy exchange mechanisms such as scattering. Conclusively, accurate evaluation of scattering mechanisms is crucial in HCD modeling. Various studies have been conducted on HCD of short channel nMOSFETs by ViennaSHE with energy driven model by T. Grasser. As the device scaled down, however, the carrier energy-based approach became complicated and difficult. Therefore, few studies analyze HCD through fundamental physical

mechanisms, and many researches are focused on empirical modeling based on measurement [9, 10]. However, since the application of the GAA structure is expected in sub-5 nm nodes, it is crucial to understand the HCD based on physical theories in FinFETs, which is a basic 3D structure. Therefore, this study focused on analyzing HCD measurement results of actual FinFET devices using physical theory. In particular, since various scattering and various mechanisms that generate HCD must be considered, research using the simulation is essential. Therefore, we have also conducted a study to improve a framework that can analyze HCD based on physical theories in a commercial Technology computer-aided design (TCAD) simulation tool.

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Chapter 2

Hot Carrier Degradation Model

2.1 Physical theory

2.1.1 Mechanisms of Si-H bond-breakage

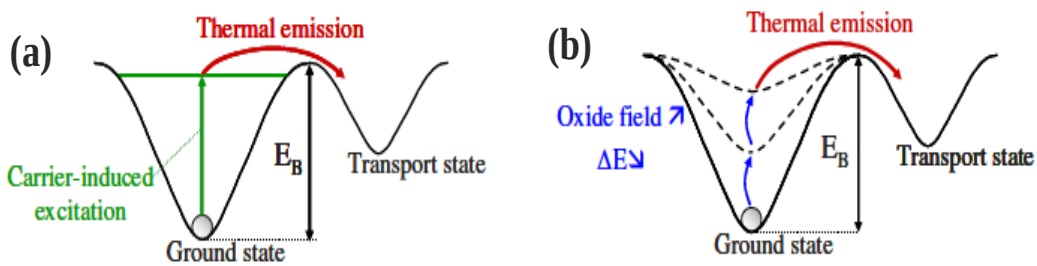

Fig. 1. (a) Transition from ground state to transport state due to carrier collision (b) Field-enhanced thermal degradation.

In the process, a defect (Silicon dangling bond) occurs at the Si/SiO2 interface, which can be solved by forming a Si-H bond through H passivation. At this time, it is expressed that the Si-H bond is in the ground state. However, when the Si-H bond receives more than a certain amount of energy (E_B), it can be transferred to the transport state through thermal emission. In this case, the Si-H bond is broken and an interface trap is formed. In general, the energy required for the transition can be obtained when a carrier collides with the Si-H bond. In addition, when the oxide field increases the energy of the ground state and reduces the energy required for the transition, the transition can occur more

easily(Field enhanced thermal degradation : FP) [1, 2]. Both cases are represented in Figure 1. The phenomenon that the Si-H bond is broken due to collision of carriers is more likely to occur as the energy of the carriers is higher, and it can be expressed as Hot Carrier Degradation (HCD) because it is mostly caused by hot carriers. From the perspective of HCD, the collision of carriers on the Si-H bond can be explained by two mechanisms: Single Particle (SP) Process and Multiple Particle (MP) Process [3, 4]. The SP process is a mechanism in which the Si-H bond is broken by one collision of high energy carriers, and the MP process is a mechanism in which the Si-H bond is broken by several collisions of low energy carriers.

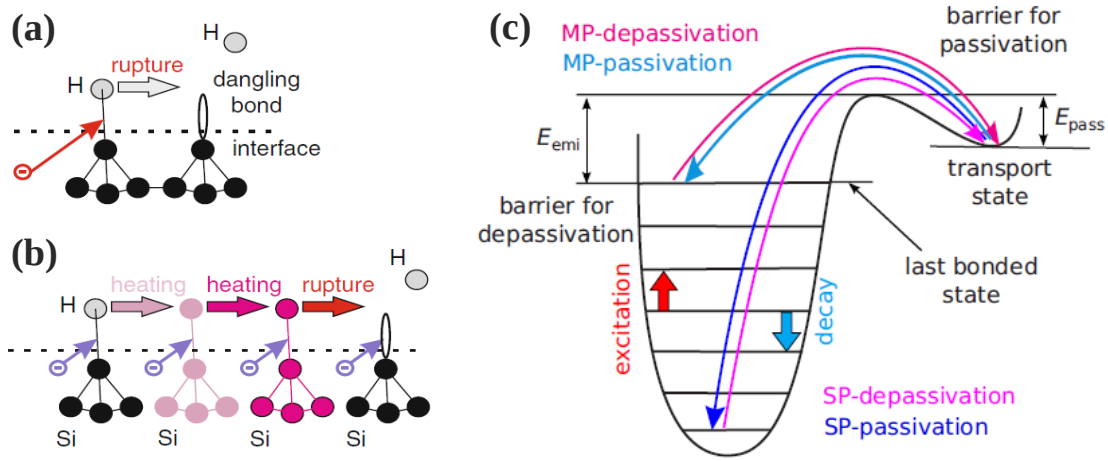

Fig. 2. (a) Single Particle(SP) Process (b) Multiple Particle(MP) Process (c) Truncated harmonic oscillator model of Si-H bond-breakage.

Figure 2(a), (b) show the SP and MP process. Both mechanisms occur simultaneously, and the Si-H bond can be expressed as a truncated harmonic oscillator with many energy levels(Figure 2(c)). In the case of the SP process, it is transferred to the transport state by one collision of carriers with high energy. In the case of the MP process, when the low energy carriers collide several times and repeat excitation and decay to reach the final level, the transport state is transferred.

2.1.2 Energy Distribution Function(EDF) / Electron-Electron scattering(EES)

In ultra-scaled devices, it can be predicted that the effect of HCD will be reduced because the operating voltage is low. However, since HCD was steadily observed, it was concluded that the energy of each carrier is more important than the voltage (field) applied to the device [5, 6]. The energy of carriers is closely related to the scattering mechanism, and the Energy Distribution Function (EDF) can be obtained through the Boltzmann Transport equation (BTE).

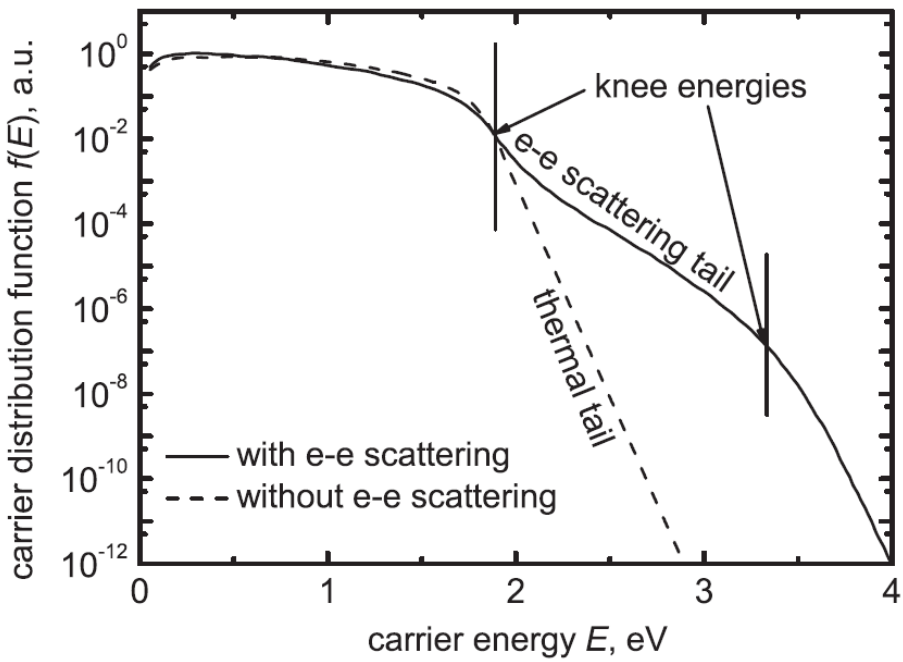

Fig. 3. Changes in Energy Distribution Function when considering Electron-Electron scattering.

Electron-electron scattering(EES) occurs when carriers collide with each other, and carriers that gain energy through multiple collisions can be classified as Hot Carriers. Therefore, as shown in Figure 3, EES worsens HCD because it increases the high-energy carrier distribution in EDF [7, 8]. EES is an important factor in HCD of short channel devices because EES can explain HCD in short channel devices with low operating voltage.

2.2 TCAD simulation

2.2.1 HCD simulation and limitations of Synopsys Sentaurus tool

In recent HCD models, since the energy of each carrier is important, it is important to accurately calculate the EDF. As explained earlier, EDF can be obtained by calculating the BTE. Monte Carlo simulation is required to accurately calculate BTE. However, since the MC method requires a very long time, it is insufficient to use it as an HCD simulation method when considering the calculation time and accuracy. Therefore, in HCD simulation, it is efficient to calculate BTE through the Spherical Harmonics Expansion (SHE) method, and the accuracy is similar to that of Monte Carlo simulation.

Sentaurus TCAD simulation provides a method of calculating BTE through the SHE method, and a system that can apply EDF obtained through calculation to HCD simulation has been established. BTE is calculated in consideration of Density of State (DOS), Scattering rate, Velocity, etc., and several parameters can be adjusted during the calculation process. As mentioned earlier, the most important parameter in HCD is the scattering mechanism. The reason why HCD occurs even in short channel devices with low operating voltage is that energy is exchanged through scattering.

Synopsys Sentaurus TCAD simulation, which is optimized for device-level analysis, was used in this study [9]. When calculating BTE through the SHE method in TCAD simulation, coulomb, impact ionization, and phonon scattering are considered.

$$\frac{1}{\tau(E)} = \frac{1}{\tau_{coulomb}(E)} + \frac{1}{\tau_{I.I.}(E)} + \frac{1}{\tau_{phonon}(E)}$$

	Phonon scattering	Coulomb scattering	Impact Ionization
Equation	$\frac{hD_{op}^2}{2\rho\varepsilon_{op}}(N_{op}+1)g(\varepsilon-\varepsilon_{op})$	$\frac{q^4\pi^2 g(\varepsilon)N_{i,eff}}{2h\varepsilon_{sem}^2[k^2(\varepsilon)+k_0^2]^2}\left[\ln(1+b)-\frac{b}{1+b}\right]$	$\left(\frac{\varepsilon-\varepsilon_{ii,1}}{1\ \mathrm{eV}}\right)^{v_{ii,1}} s_{ii,1}$

The HCD mechanism applied to TCAD simulation is as follows.

- Field-enhance thermal degradation

- Single particle process

- Multiple particle process

Field-enhanced thermal degradation			
Density	$N_{IT,FP} = N_0\left[1-\exp\left(-\kappa_{FP}t\right)\right]$	***Reaction rate***	$\kappa_{FP} = \nu_{FP}e^{-E_{FP}/kT},\ E_{FP} = E_{FP0} - pE_{OX}$
Single Particle / Multiple Particle			
Density	$N_{IT,SP} = N_0\left[1-\exp\left(-\kappa_{SP}t\right)\right],\ N_{IT,MP} = P_{MP}N_0\left[\frac{P_{emi}}{P_{pass}}\left(\frac{P_u}{P_d}\right)^N\left(1-\exp\left(-P_{emi}t\right)\right)\right]^{1/2}$		
Reaction rate	$\kappa_{SP} = \int_{E_{SP}}^{\infty} f(E)g(E)\nu(E)\sigma_{SP}(E)dE,\ \kappa_{MP} = \int_{E_{MP}}^{\infty} f(E)g(E)\nu(E)\sigma_{MP}(E)dE$		
Probability	$P_u = \kappa_{ph}e^{-E_{ph}/kT} + \kappa_{MP}(E_{MP}),\ P_d = \kappa_{ph} + \kappa_{MP}(E_{MP})$		

The most important parameter in the Si-H bond-breakage model due to SP and MP is the energy of the carrier. Depending on the energy of the carrier, the ratio of the SP and MP

process is determined, and the concentration of the interface trap (Nit) is determined. As can be seen from the above equation, SP and MP are determined by EDF (f(E)) obtained through the SHE Method. In the case of SP, the amount of Nit generated is simply determined based on Activation Energy (E_{SP}). However, in the case of MP, since the Truncated harmonics model is applied, the probability that the energy level may up or down due to a collision (P_u, P_d) is included in the equation. Therefore, the amount of Nit generated is determined through the probability of reaching the highest energy level and the probability of thermal degradation.

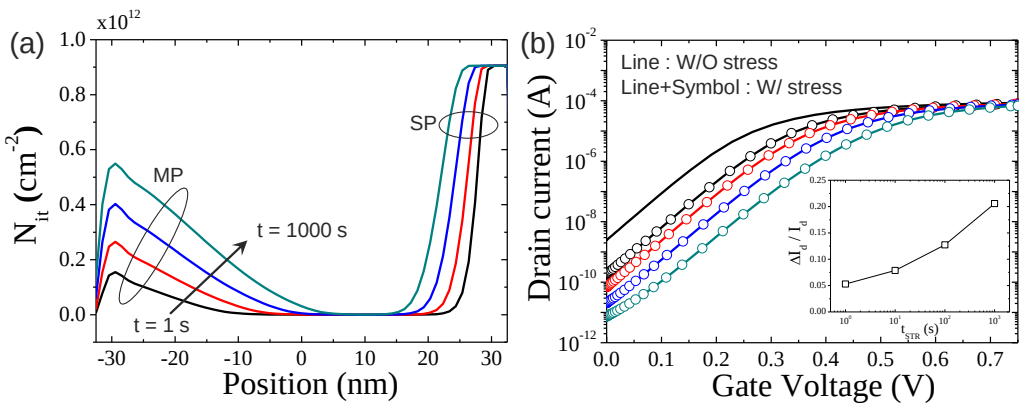

Fig. 4. (a) Interface trap (Nit) generation rate by SP, MP, and Field enhanced mechanisms (b) Extraction of drain current degradation rate according to stress time.

The concentration of Nit calculated by the above equations is showed in Figure 4(a). In the Drain region where the energy of carriers is relatively high, Nit is generated by SP. And in the source region with low energy, Nit is generated by MP. In addition, the Nit

concentration that increases with the stress time is implemented, and the influence occupied by each mechanism can be extracted. As a result, the influence of Nit calculated through each mechanism can confirm I_D-V_G characteristics, V_T change, SS and on-current change. The parameters required for the calculation of the equation are adjusted, and through this method, it is possible to fit the measured data and the simulation model.

As mentioned in the previous chapter, EES can be ignored in HCD of conventional long channel devices, but plays an important role in HCD of short channel devices. In particular, since it affects the distribution of high-energy carriers in EDF, EES is a mechanism to be accurately considered when calculating the SP mechanism. However, EES is not considered when calculating BTE with the SHE method in the current Sentaurus simulation. Therefore, it cannot be said that the HCD of the recently ultra-scaled device is accurately implemented, and even though the actual data and simulation model can be fitted, it is not physically accurate.

2.2.2 Simulation model improvement

The limitation of the current Sentaurus HCD simulation model is that Electron-electron scattering cannot be considered when calculating the energy of a carrier. Therefore, in order to consider the effect of EES, the EES rate ($1/\tau_{EES}$) was added to the total scattering rate applied to the BTE calculation.

$$\frac{1}{\tau(E)} = \frac{1}{\tau_{coulomb}(E)} + \frac{1}{\tau_{I.I.}(E)} + \frac{1}{\tau_{phonon}(E)} + \boxed{\frac{1}{\tau_{EES}(E)}}$$

The equation of the carrier-carrier scattering rate is very similar to the Coulomb scattering rate applied in the simulation. Coulomb scattering is an interaction between a charged dopant and a carrier, and Electron-electron scattering is also a physically the same mechanism because it is an interaction between charged carriers. Therefore, the difference between the two scattering is the number of interactions, and the difference can be distinguished by the concentration of the dopant and the concentration of the carrier. Therefore, $1/\tau_{EES}$ can be expressed by converting the concentration of the dopant to the concentration of the carrier in the $1/\tau_{coulomb}$ equation.

[Scattering rate] [Debye length]

$$\frac{1}{\tau_{coulomb}(E)} = \frac{2\pi q^4 N_D}{\hbar\varepsilon^2} \frac{1}{(k^2 + 1/\lambda_D^2)^2} \qquad \lambda_D^2 = \frac{\varepsilon_{si} kT}{q^2 N_D}$$

$$\frac{1}{\tau_{EES}(E)} = \frac{2\pi q^4 n}{\hbar\varepsilon^2} \frac{1}{(k^2 + 1/\lambda_D^2)^2} \qquad \lambda_D^2 = \frac{\varepsilon_{si} kT}{q^2 n}$$

When BTE is calculated by adding the above equation, it is expected that a change in EDF will occur, and the application of EES can be confirmed by conducting HCD simulation through the modified EDF.

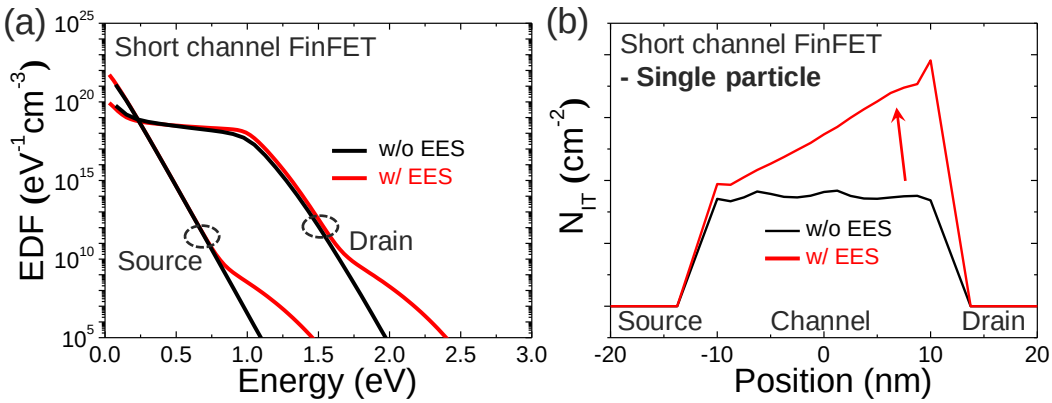

Fig. 5. (a) EDF and (b) interface trap concentration according to the application

Figure 5(a) shows EDF according to the application of EES. First, higher energy carriers increase from the source area to the drain area. In particular, when EES is applied, it can be seen that the carrier distribution in the high energy tail is increased. In addition, it can be seen that the Nit of the drain region increases due to the increased high energy carrier (Figure 5(b)). As a result, if EES is considered, the lifetime may be shorter than predicted by conventional HCD simulation model. Therefore, a more accurate HCD simulation framework was constructed by applying EES.

2.3 Calibration process

2.3.1 I-V Calibration

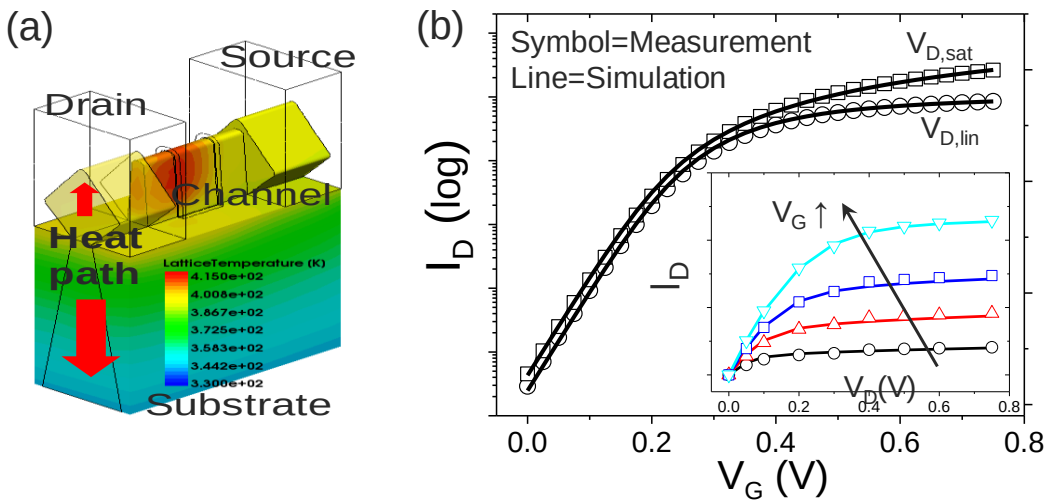

Fig. 6. (a) FinFET device designed through the TCAD simulation tool and heat generation caused by on current (b) Calibrated I-V curve.

To calibrate the HCD data, I-V calibration was conducted first. In the calibration process, accurate implementation of self-heating effect (SHE) is very important because self-heating has significant effect on the temperature dependence on HCD. SHE was considered by using the Thermodynamic model. Additionally, various thermal conductivities have been applied according to each material and thickness, and different doping concentrations and dopant materials have been considered in Si [10]. Figure 5(a) shows the FinFET structure designed by TCAD simulation and the heat generation

obtained during the I-V calibration process. It can be seen that the maximum temperature occurs in the drain region where the field is high and heat is released to the drain/source and substrate. Figure 6(b) shows the results of the I-V calibration. eQuantumPotential and BALMob models were used to consider quantum effects and ballistic transport, respectively. In the case of the BALMod model, the ballistic component was added to the original mobility term. Also, various mobility models including phonon, Coulomb, carrier, and surface scattering were considered using the Phumob, Electron-electron, and Enormal(Lombardi) models and velocity saturation was considered using the HighFieldSaturation model. Tensile stress was applied to the channel to consider strain effect due to the source/drain.

2.3.2 Parameter extraction through HCD data Calibration

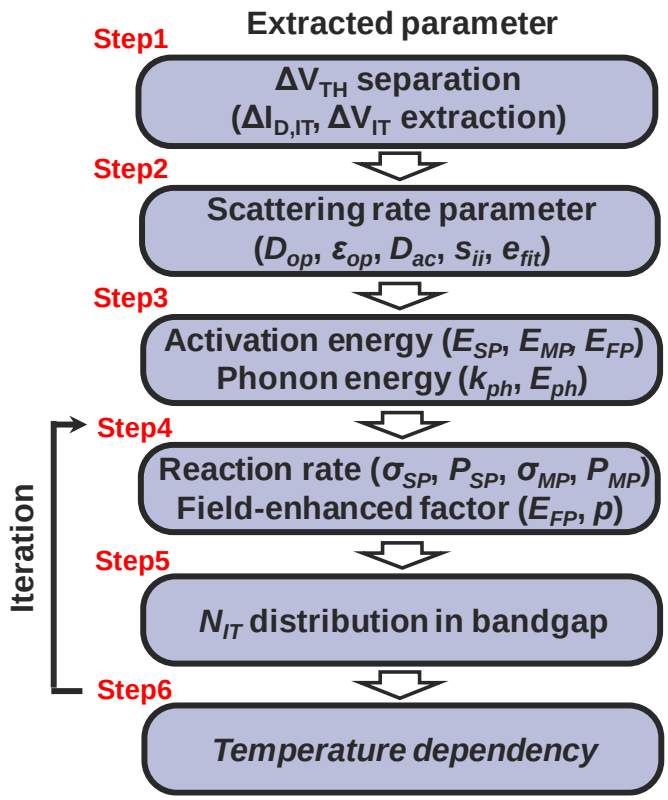

Fig. 7. Calibration process between HCD measurement data and simulation model.

Figure 7 shows the calibration process between the HCD measurements and simulation model. HCD was measured from the same device used to obtain I-V characteristics.

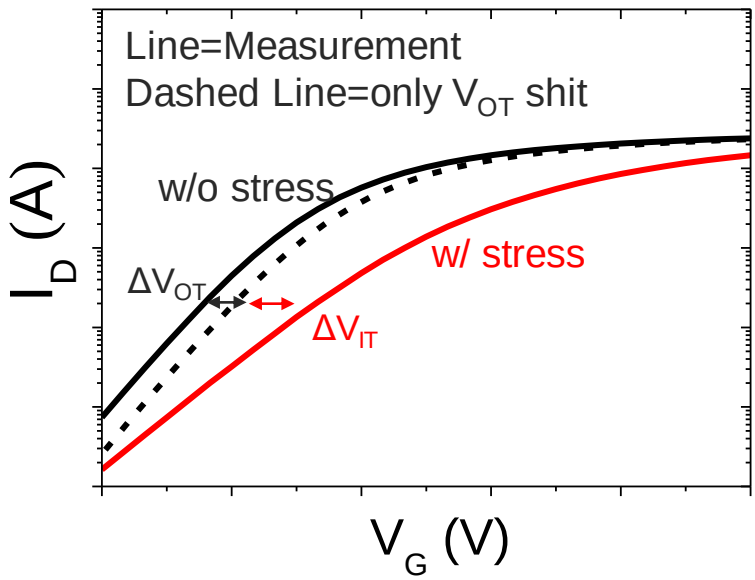

Fig. 8. ΔV_{TH} separation using SS and off-current in I-V curve of w/ and w/o stress.

First, the total V_{TH} shift includes the V_{TH} shift by the interface trap(V_{IT}) and the V_{TH} shift by the oxide trap(V_{OT}). V_{OT} can be ignored under nominal operating conditions. However, V_{OT} cannot be ignored under acceleration conditions because the device temperature or gate voltage is high. Therefore, it is necessary to extract a pure V_{IT} component because both components occur simultaneously under accelerated conditions [11]. Through the results of past experiments, it has been announced that the interface trap is concentrated above the mid-band gap. Therefore, assuming that interface traps at voltages below 0V are ignored, V_{TH} shifts accompanied by SS changes at voltages above 0V can be said to be V_{IT}. Also, the V_{TH} shift occurring at voltages below 0V is V_{OT}(Fig.8(b)).

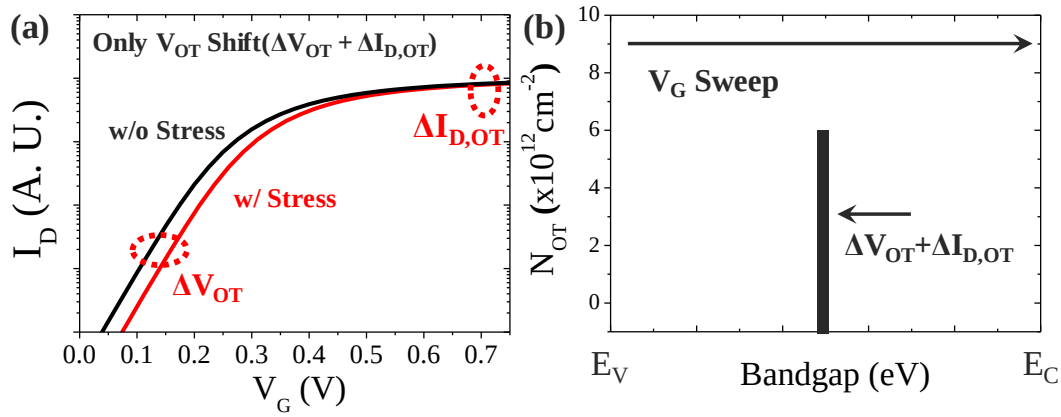

Fig. 9. (a) I-V curve shifted only by V_{OT}, (b) N_{OT} distribution within the bandgap

Figure 9(a) shows the I-V characteristics extracted through ΔV_{TH} only degraded by oxide traps. Only the V_{TH} is shifted due to oxide traps so that the on-current changes according to the shifted V_{TH}. Figure 9(b) shows the N_{OT} distribution within the bandgap which is determined through the calibration process. In addition, N_{OT} is distributed in the middle level because V_{TH} shift occurs. Iteration processes are performed until the parameter set that satisfies all the various voltage conditions because there can be several parameter sets of the N_{OT} equation that satisfy a specific voltage condition.

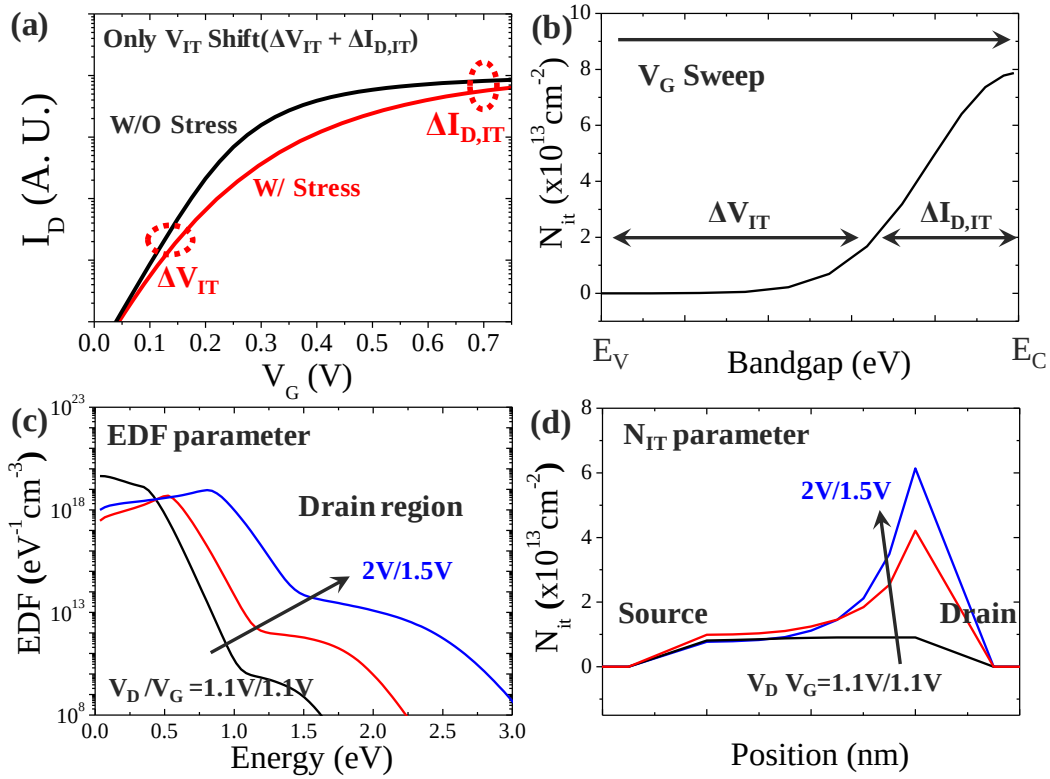

Fig. 10. (a) I-V curve shifted only by V_{IT}, (b) Nit distribution within the bandgap, and (c) calibrated EDF and (d) Nit.

The I-V characteristics only degraded by interface traps can be obtained by eliminating the effect of bulk traps from the I-V characteristics after applying the stress, as shown in Figure 10(a). ΔV_{IT} is used to calibrate the maximum Nit density (N_0) and Nit distribution within the bandgap. In the case of nMOSFETs, the Fermi level in the bandgap is swept from Ev to Ec when the gate voltage increases during the measurement. Therefore, the Nit distribution between Ev and middle level in the bandgap contributes to V_{IT} and additional Nit distribution near Ec contributes to on-current degradation. As a result, this

distribution is calibrated to a Gaussian distribution decreasing from the Ec to Ev. Finally, $\Delta I_{D,sat}$ under various stress conditions can be calibrated by adjusting EDF and degradation parameters. To perform calibration under various stress conditions, continuous iteration is required and the results are shown in Figures 10(c), (d) separately. In this process, the vibrational modes in Si-H bonds should be considered. Vibrational mode is classified into stretching and bending mode and the range of parameters was obtained through measurement. In this paper, stretching mode was used for calibration.

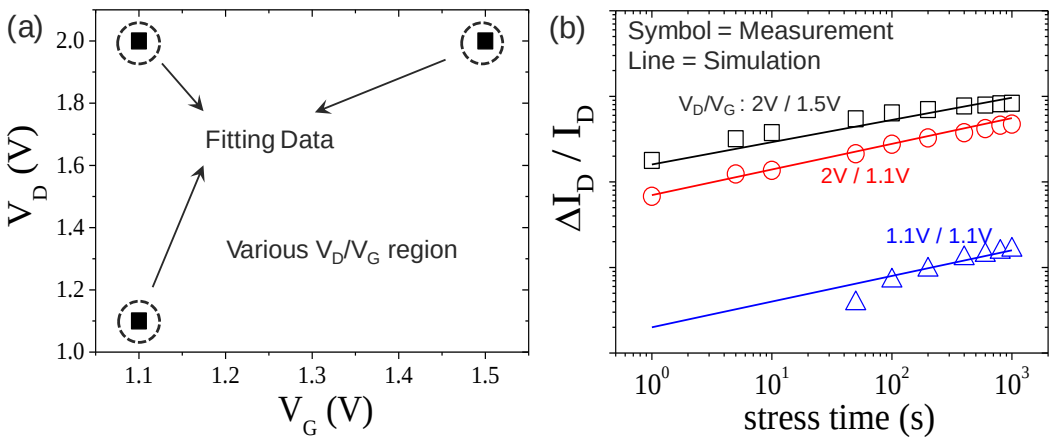

Fig. 11. Calibration between the measured data and improved simulation models.

Through the process above, calibration was conducted under various stress voltage conditions. In the case of low stress voltage(1.1V/1.1V), this condition is almost meaningless since degradation hardly occurs in short-term. ($\Delta I_{D,sat}$ < 0.5%). The three conditions with low EES effects were selected in total stress conditions ($V_D \geq V_G$).

Figure 11 shows the results of calibration between the measured data and the

simulation models. The solid line represents the improved simulation model considering interface traps with EES. It can be confirmed that the measurement result and the simulation result match well.

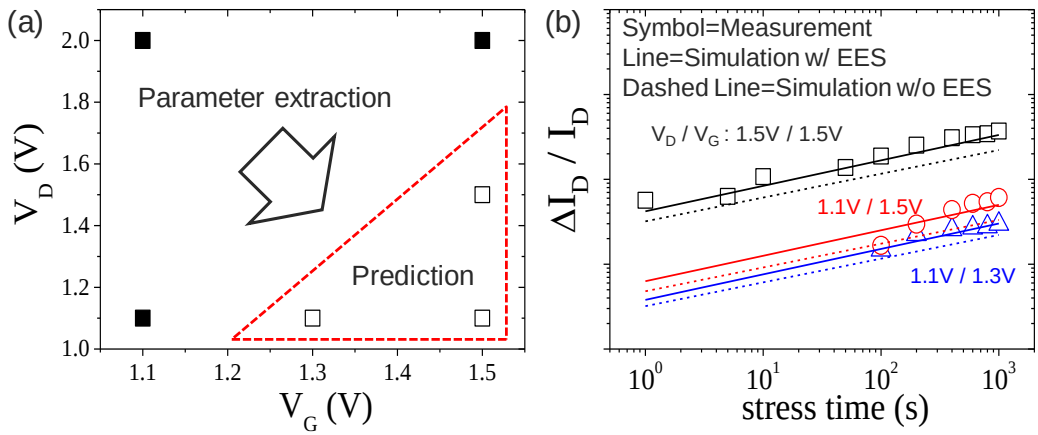

Fig. 12. Prediction of HCD under voltage stress conditions with strong oxide trap effects.

Next, degradation under conditions with strong EES ($V_D \leq V_G$) was predicted by applying parameters extracted from the previous calibration process for three conditions. When the gate voltage increases, the amount of carriers increases. However, the energy of carriers does not change much. Therefore, the previous model has the ΔNit, which is generated by increased carriers only, as the gate voltage increases. However, in the case of the improved model, there are additional ΔNit that occur as the gate voltage increases due to EES. Therefore, in Figure 12(b), the case with improved model has better agreement with the data than the previous model. In the prediction process, the average

errors are 7.08% and 14.44%, respectively.

If the HCD life-time is predicted based on the previous model, actual life-time can be greatly overestimated. However, an HCD framework can be predicted HCD life-time accurately by applying the oxide trap in the previous model.

2.4 Summary

In this study, research was conducted on a methodology that can analyze Hot Carrier Degradation under various conditions of 3D FinFET devices. In particular, for HCD analysis based on physical theory, research through simulation is essential. Therefore, the current level and limitations of the HCD model were analyzed in the Synopsys Sentaurus simulation used as a commercial tool in the study of logic devices. The problem of the simulation is that Electron-Electron scattering, which changes the carrier distribution of the energy tail, cannot be considered in calculating EDF, which is the most important in the recent HCD model. As an improvement method, when calculating the BTE, the EES equation was added in the total scattering rate, and the EES application was confirmed through the EDF extracted from the simulation. The consistency was verified using the additionally improved simulation model and actual HCD measurement data. Finally, when comparing the improved simulation model and the conventional model, it was confirmed that the accuracy of the actual data prediction was improved.

In addition, since the distribution of high-energy carriers increases due to the application of EES, the predicted lifetime of the improved model is shorter than that of the conventional model.

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Chapter 3
Analysis on Temperature Dependence of HCD in short channel FinFET

3.1 Introduction

Because HCD has a time limit, it is estimated based on the degradation under accelerated condition to predict lifetime. In particular, HCD is measured in the worst case condition to guarantee minimum lifetime. In general, HCD predict lifetime through acceleration in the worst case. In long channel device, HCD was most deteriorated under the condition of $V_G=V_D/2$ where impact ionization (I.I.) is the peak and low temperature [1]. However, as high-k layers have been applied as devices have been scaled down, pre-existing traps rapidly have been increased to show high degradation when $V_G=V_D$ and in high temperature [2]. Therefore, voltage and temperature are important factors in determining hot carrier degradation.

Recently, due to continuous scaling, the structure of the device has been developed as a 3D FinFET that can increase gate control. However, as the channel thickness decreases, the self-heating effect becomes more severe and the influence of temperature on HCD increases [3]. As mentioned above, since temperature is a factor that can determine the worst case of HCD, it is very important to study the characteristics of HCD according to temperature. Therefore, in this study, the temperature tendency of HCD was analyzed

based on physical theory in FinFET, which is a basic 3D structure. In addition, the analysis was conducted based on the measurement results under various voltage conditions to consider various mechanisms that can generate HCD.

3.2 Temperature dependence according to acceleration conditions

3.2.1 Experiment

14 nm node bulk FinFETs have been utilized in this study with high-k/metal-gate processes. The measurements have been performed in various voltage and temperature conditions. Variability is an important issue in 14 nm node devices. We have conducted 4 measurements in each HCD condition to investigate the general temperature dependency and selected the measurement result among the 4 measurements which was closest to the mean value. Also, measurements were conducted within one wafer to maximally suppress the variability between the devices and devices that showed similar VTH/on-current through I-V characteristic were used to measure the HCD. Because the variation between devices decreases as the number of Fins increases in FinFETs, 4-Fin devices with relatively low variation were used in this study [4].

3.2.2 Comparison of temperature dependence in two acceleration conditions

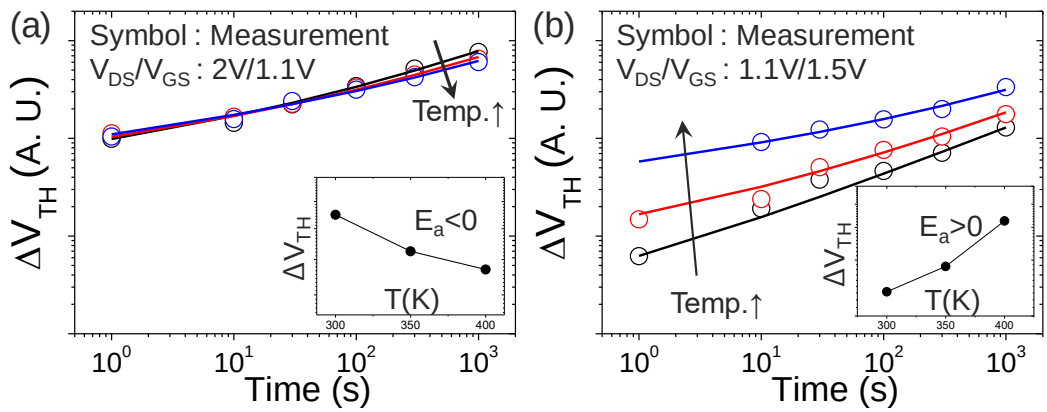

Fig. 1. Temperature dependence of HCD according to two voltage conditions (a) VDS/VGS = 2V/1.1V (b) VDS/VGS = 1.1V/1.5V.

Figure 1 shows the temperature dependence of HCD according to two voltage conditions. Measurements have been performed in temperature conditions of 300, 350, and 400K. Degradation decreases as the temperature increases in the high drain voltage condition (2V/1.1V) and degradation increases as the temperature increases in the high gate voltage condition (1.1V/1.5V). Since there are various mechanisms for generating HCD, it is necessary to understand the temperature dependence of each mechanism in order to clearly analyze these results. Generally, oxide traps (trapping) increase as temperature increases [5]. Therefore, if there is only a tendency for the interface trap to decrease with temperature, the opposite temperature dependence can be explained simply by the combination of oxide trap and interface trap that varies with voltage conditions.

Therefore, V_{TH} shift caused by oxide trap (ΔV_{OT}) and interface trap (ΔV_{IT}) was separated using Subthreshold swing (S.S.).

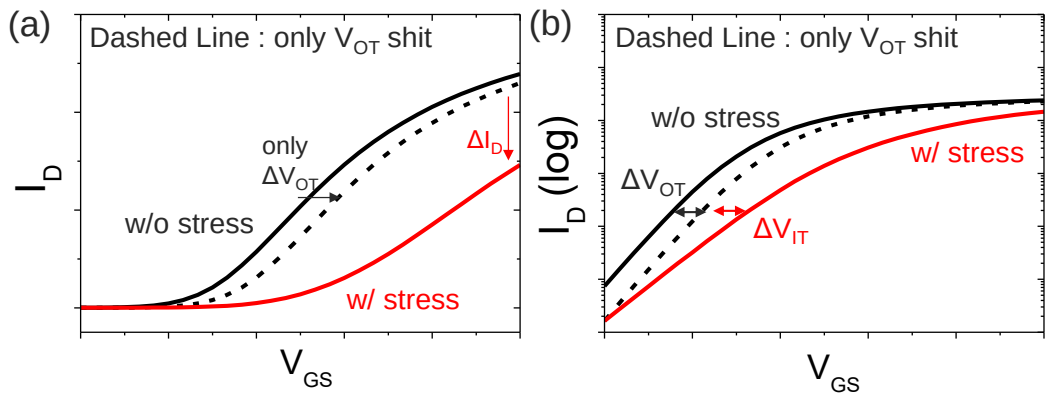

Fig. 2. (a) Additional on-current degradation (ΔID) due to interface traps (b) ΔVTH and ΔVOT component separation using total VTH shift and S.S.

Generally, interface traps are formed with specific distributions within the bandgap [6]. Therefore, as V_G increases, S.S. changes due to the increase of interface traps involved in V_{TH} shift. Also, the interface traps act as scattering centers, causing additional on-current degradation (Figure 2(a)). However, because oxide traps are generated at a constant level within the band gap, only the V_{TH} shift occurs. Therefore, the ΔV_{IT} and ΔV_{OT} components were separated based on the off current of the stressed I-V curve as shown in Figure 2(b).

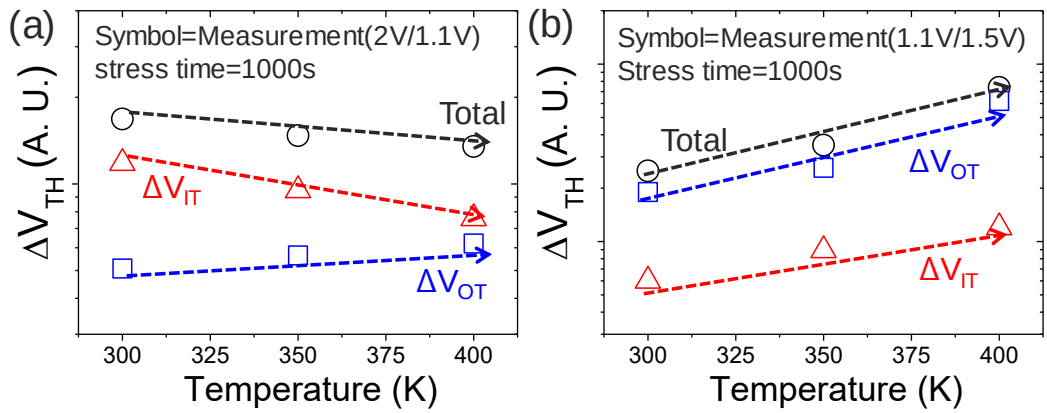

Fig. 3. Temperature dependence of ΔV_{OT} and ΔV_{IT} according to two voltage conditions (a) V_D/V_G = 2 V/1.1 V (b) V_D/V_G = 1.1 V/1.5 V.

Figure 3 shows the ΔV_{OT} and ΔV_{IT} components with temperature at each acceleration condition. As mentioned above, ΔV_{OT} increased as the temperature increased in both voltage conditions. On the other hand, ΔV_{IT} has different temperature dependences under two voltage conditions. Because these results mean that the temperature dependence of each mechanism for generating interface traps is different, additional analysis is needed to understand the overall temperature dependence. Therefore, in this paper, the interface trap was separated into three mechanisms and the temperature dependence of each mechanism was analyzed.

3.3 Calibration process

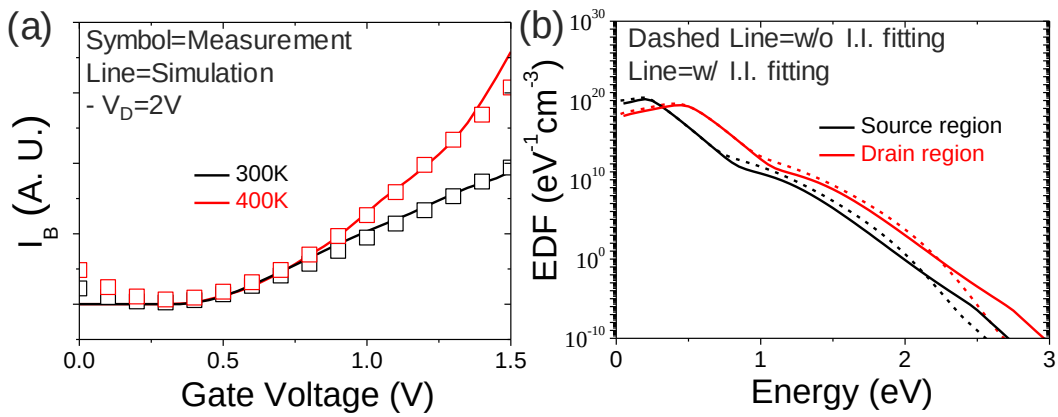

Fig. 4. (a) Calibration result of body current (I_B-V_G) according to temperature (b) EDF modified by applying the parameters of I.I.

In hot carrier conditions, a high electric field causes a large amount of impact ionization. Therefore, in order to improve the accuracy of the hot carrier simulation, the body current (I_B-V_G) was calibrated. The VanOverstraeten model, an impact ionization model, was used and the data and simulation results were found to fit well (Figure 4(a)). Carrier energy changes because the amount of I.I. changes during the calibration process. Figure 4(b) shows the change of EDF by applying the parameters of I.I. extracted during the calibration process. The SP component is most affected because the distribution of high energy carriers is different.

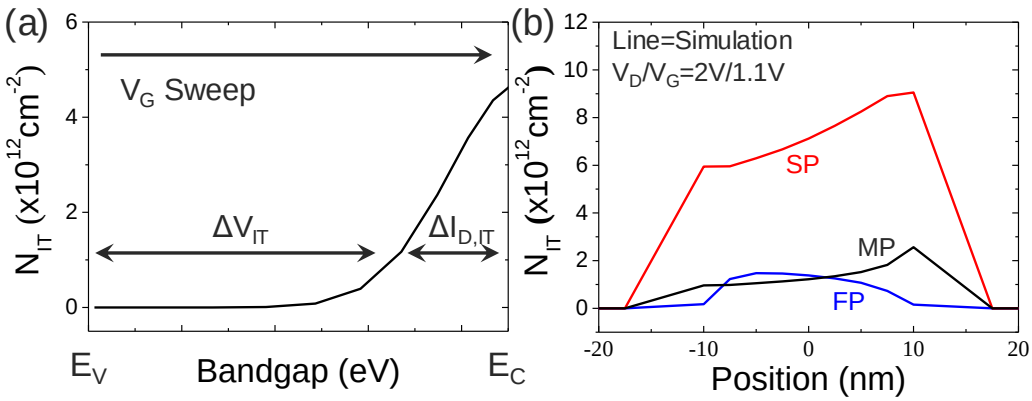

Fig. 5. (a) Nit distribution within the bandgap (b) Nit distribution in the channel

Figure 5(a) shows the Nit distribution within the bandgap which is determined through the calibration process. In the case of nMOSFETs, the Fermi level in the bandgap is swept from Ev to Ec when the gate voltage increases. Therefore, the Nit distribution between Ev and middle level in the bandgap contributes to V_{IT}. The additional Nit distribution near Ec contributes to on-current degradation. Figure 5(b) shows the Nit distribution in the channel. As mentioned above, since SP and MP are carrier energy dependent components, SP and MP occur in the drain region where the lateral field is strong. On the other hand, the FP component shows a peak in the source region where the vertical field is high because the vertical field is an important factor.

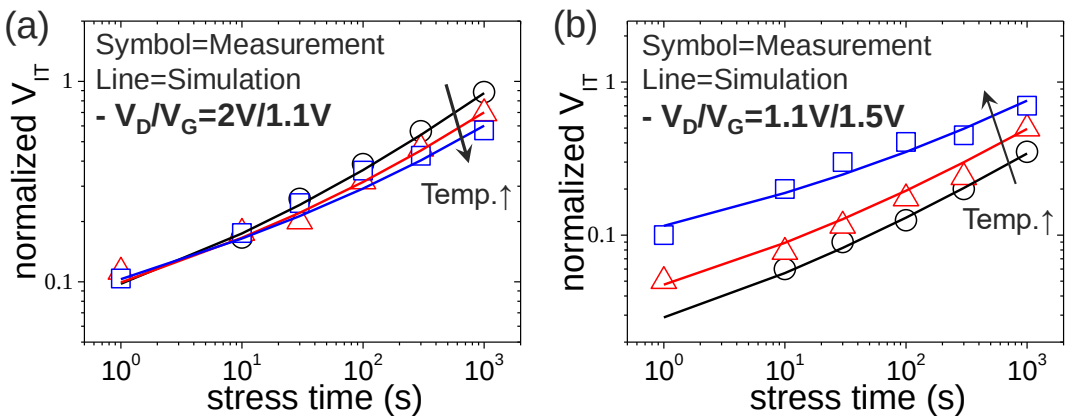

Fig. 6. (a) Calibration results between the ΔV_{IT} data and the simulation versus stress time at V_D/V_G=2V/1.1V condition (b) V_D/V_G=1.1V/1.5V.

Figure 6 shows the calibration results between the ΔV_{IT} data and the simulation versus stress time. Iteration was performed until a parameter set was obtained that satisfies all conditions, and the ΔV_{IT} was calibrated well according to temperature. Current degradation rate ($\Delta I_D/I_D$) is an important parameter in HCD. However, the current degradation rate and the interface trap density are not directly proportional because the reference current is different for each temperature. On the other hand, the ΔV_{TH} is directly proportional to the interface trap density because it is an absolute value rather than a ratio. Therefore, in this paper, we analyzed HCD temperature trend through ΔV_{TH}.

In the calibration process, carrier energy was calculated by considering Phonon, Coulomb, CarrierCarrier and I.I. scattering. In addition, the vibrational mode of Si-H bond was the bending mode and the bond dispersion and dipole moment due to activation energy (E_A) fluctuation were considered.

3.4 Mechanism separation

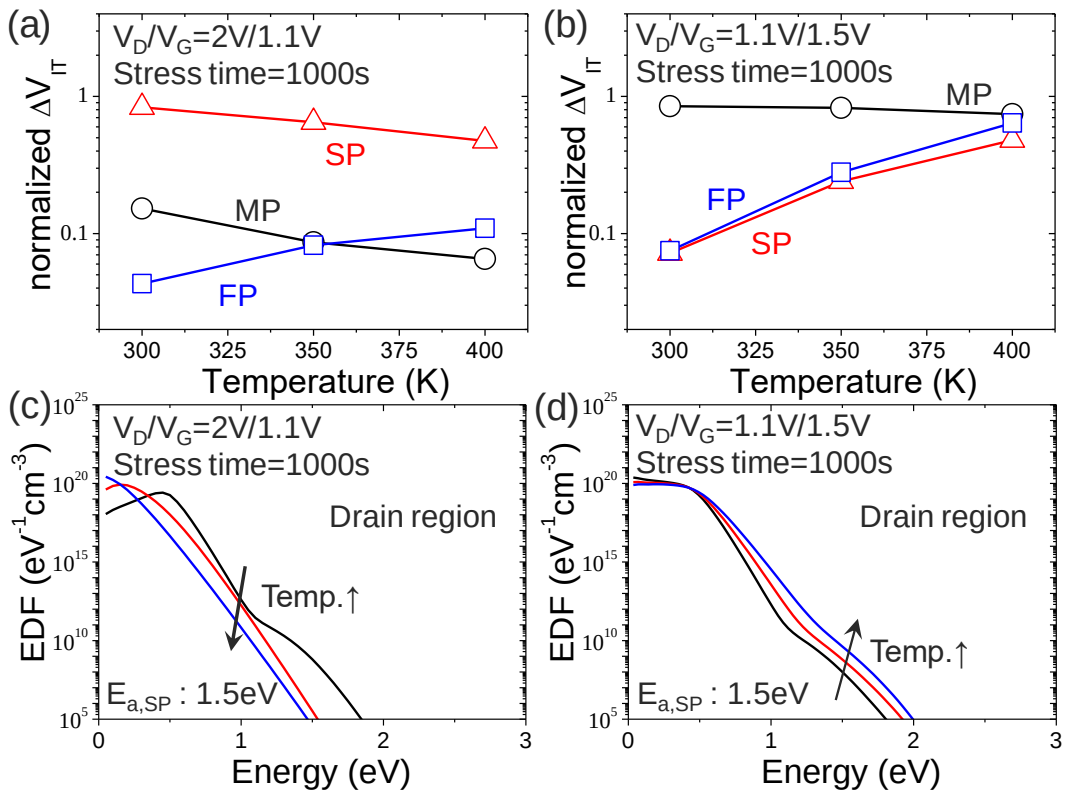

Fig. 7. (a), (b) Temperature dependence on each mechanism and (c), (d) Energy distribution function(EDF) in two voltage conditions.

Figure 7 shows the temperature dependence on each mechanism that causes interface traps. The MP is related to the number of carriers and vibration frequency of the Si-H bond. When vibration occurs, Si-H bonds tend to lose energy rather than gain energy. Although there is no significant change of the number of carriers as the temperature

increases, the vibration frequency of Si-H bond increases [7]. Therefore, the MP decreases as the temperature increases. FP is a phenomenon where Si-H bonds, which are weakened by the oxide field, break due to thermal energy. The FP accordingly increases as the temperature increases.

The SP is significantly affected by factors that change the carrier energy such as scattering, voltage, and temperature conditions because the E_A is high. When the drain voltage is high, many carriers with high energy are distributed throughout the channel. Therefore, the effect of increased carrier energy according to increasing temperature is not dominant in this case. Meanwhile, phonon scattering increases as the temperature increases which decreases the carrier energy, and decreases the SP (Figure 7(c)). On the other hand, when the drain voltage is low, most carriers have low energy. Since phonon scattering occurs under carriers with high energy majorly, carriers with low energy have low influence on phonon scattering. Therefore, SP increases since the energy of carriers increases as temperature rises (Figure 7(d)). As a result, the tendency of the SP can be considered as a significant factor that determines the temperature dependence on the total interface traps.

3.5 HCD prediction in the nominal voltage

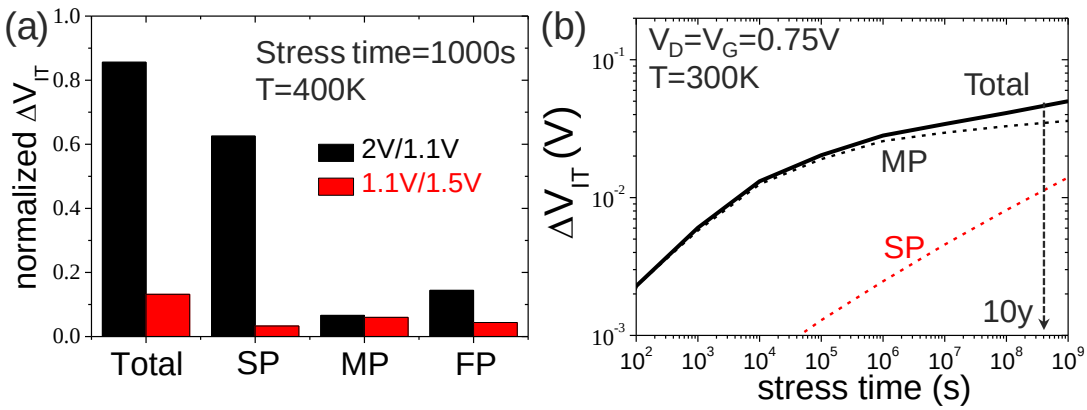

Fig. 8. (a) Comparison of the effect of each mechanism in two voltage conditions (b) ΔV_{IT} components in the nominal operating region.

Figure 8(a) shows the comparison of the effect of each mechanism in two voltage conditions. It is especially worth noting the results of the FP component. Degradation due to the FP is generally high when in strong oxide field conditions. However, FinFETs have a high self-heating effect, which can lead to high degradation even at lower oxide fields. Therefore, in nominal operating condition, the composition of mechanisms can be changed because of the lower voltage and weaker self-heating effect compared to the accelerated stress conditions.

Figure 8(b) shows the predicted degradation under nominal operating condition through simulation. The time required for deterioration is different for each component, and MP occurs first because of lowest E_A. On the other hand, FP occurs under accelerated

stress conditions, but not in the nominal operating condition. Therefore, it is possible to underestimate the actual lifetime when accelerating under the conditions of Figure 8(a). However, because the components of V_{IT} differ depending on the structure and operating voltage of the device, it is important that the acceleration conditions reflect the components in the nominal operating condition in order to accurately predict the lifetime. Therefore, researches that accurately analyze HCD using each mechanism are very important.

3.6 Summary

Temperature dependence of HCD was analyzed under two voltage conditions. In the case of oxide traps, deterioration increases as temperature increases under all conditions. However, in the case of interface traps, opposite temperature dependence was shown under two voltage conditions. In order to analyze this dependence, interface traps were separated into three components and the temperature dependence of each component was analyzed. MP and FP have a constant temperature trend depending on voltage conditions. However, SP is highly influenced by scattering and shows various temperature dependences. Due to the self-heating, FinFET has different temperatures at accelerated conditions and nominal operating condition. In the nominal operating region, FP disappears due to weak self-heating. However, the components vary depending on the

structure of the device and the nominal operating voltage. Therefore, it is necessary to consider these components when determining the acceleration condition.

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Chapter 4
Comparative Analysis of HCD in nMOS/pMOS FinFET

4.1 Introduction

In the past, interface traps caused by impact ionization (I.I.) were the main components of HCD in long-channel devices [1]. Because electrons cause higher I.I. than holes in the same voltage and temperature condition, HCD was more severe in nMOS transistors than in pMOS devices [2]. However, as high-k/metal-gate (HK/MG) processes has been applied in the scaling down of devices, more traps exist in the SiO2/HfO2 interface or HfO2 layer. Therefore, electron/hole trapping has also become a main mechanism of HCD because many carriers are trapped in these pre-existing traps even in HCD conditions [3]. Also, electrons can be trapped easier than holes because the energy barrier of electrons of the Si/SiO2 interface is lower than that of holes. Therefore, higher HCD occurs in nMOS devices than in pMOS devices regardless of the trap type. Due to the continuous scaling down of devices, the structure of devices has developed into three-dimensional (3D) FinFETs. However, unlike planar structures, higher HCD is observed in pMOS devices compared to nMOS devices in FinFETs [4]. Because this result cannot be explained with conventional theories, the HCD characteristics in FinFETs should be accurately analyzed and understood. Therefore, the HCD devices in nFinFETs and

pFinFETs are compared, and the causes are analyzed in this study.

4.2 Comparison of HCD in the long/short channel FinFET

4.2.1 Experiment

10 nm node bulk FinFETs (core, I/O) have been utilized in this study with HK/MG processes. The measurements have been performed in various voltage and temperature conditions. Variability is an important issue in 10 nm node devices. We have conducted five measurements in each voltage condition to investigate the general dependency and selected the measurement results that were closest to the mean value among the measurements. Also, measurements were conducted within one wafer to maximally suppress the variability between the devices, and devices that showed similar V_{TH}/on-current characteristics. Because the variation between devices decreases as the number of Fins increases in FinFETs, 4-Fin devices with relatively low variation were used in this study.

4.2.2 Long channel I/O device

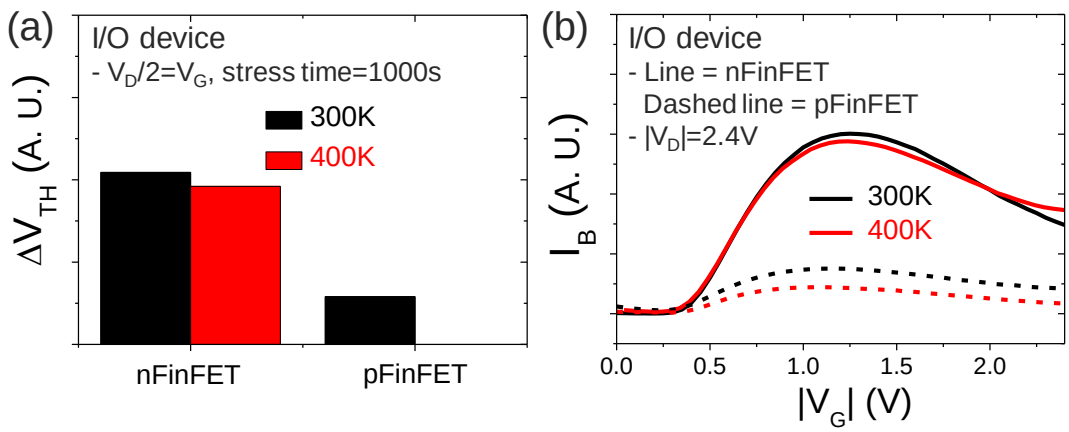

Fig. 1. (a) Comparison of ΔV_{TH} at two voltage conditions in the long channel I/O nFinFET and pFinFET and (b) body current.

Figure 1(a) shows the comparison of ΔV_{TH} in the HCD condition ($V_D/2=V_G$) in the long-channel I/O FinFET. Higher degradation was observed in the nFinFET compared to the pFinFET in the HCD condition. Also, lower degradation occurred in the nFinFET at 400K than at 300K. Holes have lower energy than electrons because the mean free path of holes is shorter. Also, the carrier energy decreases as the temperature increases because phonon scattering becomes more active. Therefore, the HCD measurements of long-channel FinFETs correspond with the trends of past studies and can be explained through physical theories [5]. The tendency of the body-current (I_B) also matches with the tendency of the temperature (Fig. 1(b)).

4.2.3 Short channel core device

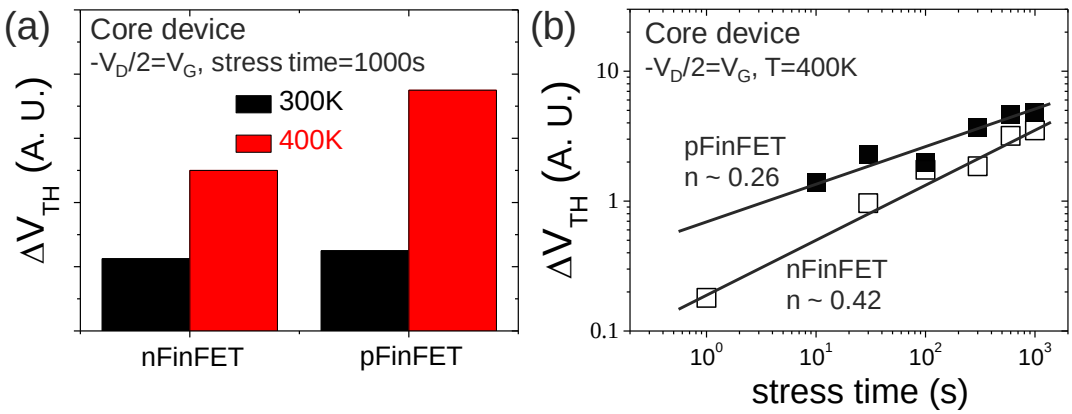

Fig. 2. (a) Comparison of ΔV_{TH} in nFinFET and pFinFET according to temperature and (b) time exponents extracted at HCD condition($V_D/2=V_G$).

Figure 2(a) shows the degradation of the short-channel core n/pFinFET under HCD condition. Degradation increased in both n/pFinFETs as temperature increased and higher degradation occurred in the pFinFET than the nFinFET. This result cannot be explained by conventional theories. Therefore, degradation was analyzed according to the stress time to investigate the cause of HCD. Generally, the time exponent (n) due to interface traps is between 0.5 and 0.6 in HCD condition and n due to oxide traps is between 0.1 and 0.2 [6]. Since both mechanisms occur at the same time, the time exponent is between 0.1 and 0.6. Therefore, it can be predicted that the interfaces are the dominant components in nFinFETs and the oxide traps are dominant in pFinFETs, as shown in Figure 2(b). Because more impact ionization can be caused with higher energy, the carrier energies of the nFinFET and pFinFET were compared through the IB. Also, there is higher

probability of carriers being trapped in the oxide traps if there are more carriers that transport from the channel to the gate. Therefore, the number of oxide traps were compared by measuring gate currents(I_G).

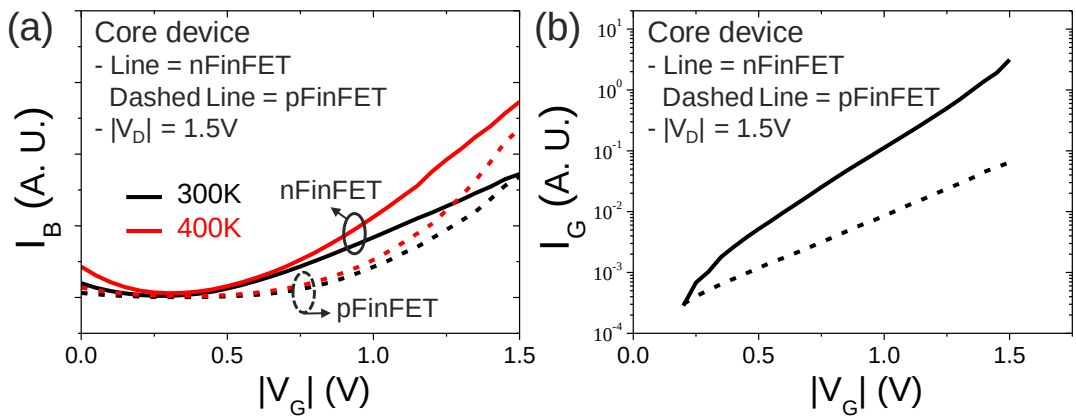

Fig. 3. (a) Body current and (b) gate current of the short channel core FinFET according to temperature.

Figure 3(a) shows the I_B of the core n/pFinFETs. The ratio of the I_B and drain current (I_D) is often used to compare the energy of electrons and holes (I_B/I_D). However, the strained pFinFET has similar I_D with that of the nFinFET in this study. Therefore, I_B was simply compared. Unlike in long-channel devices, I_B increased as the temperature increased in short-channel devices because the effect of phonon scattering decreased. Therefore, higher degradation due to increasing temperature in both devices can be explained by the increase of carrier energy. However, because the nFinFET has higher I_B than the pFinFET, we cannot explain why the pFinFET causes higher degradation than the nFinFET. Figure 3(b) shows the I_G of each device. Due to the difference of the energy

barrier height between the two devices, I_G of the nFinFET was higher than that of the pFinFET. Therefore, the probability of oxide trapping is higher in the nFinFET because there are many carriers that have moved to the oxide [7]. Also, it is difficult to consider that there are more oxide trap components in the pFinFET than in the nFinFET because the electron density is higher than the hole density, and the tunneling mass of electrons is also lower than that of holes [8]. Therefore, more interface traps or oxide traps should occur in nFinFETs than pFinFETs due to carriers with higher energy. However, the actual measurement results are the opposite. Therefore, another mechanism is needed to explain this result.

At the HCD condition, higher degradation in the nFinFET compared to the pFinFET did not occur in the planar structure, but started to occur in ultra-scaled FinFETs. Therefore, we analyzed the characteristics that can change due to the difference between the two structures using TCAD simulation.

4.3 Self-heating effect in n/pFinFET

The self-heating effect (SHE) was not a major issue in conventional planar structures because heat was easily released. However, SHE worsens in 3D FinFET structures because the heat-path decreases as the Fin thickness is reduced [9]. Especially for pFinFETs, SiGe is used for the source/drain (S/D) material to increase the current level by enhancing the hole mobility in the channel. However, alloy scattering which occurs in

SiGe reduces the thermal conductivity [10, 11]. Therefore, strained pFinFETs have higher device temperature than nFinFETs [4]. The temperature difference between pFinFETs and nFinFETs can become more severe if further scaling down is performed. Therefore, SHE is an essential factor to consider when analyzing HCD in 10 nm node FinFETs.

Because the temperature of the actual devices could not be measured, simulation was used to compare the device temperature.

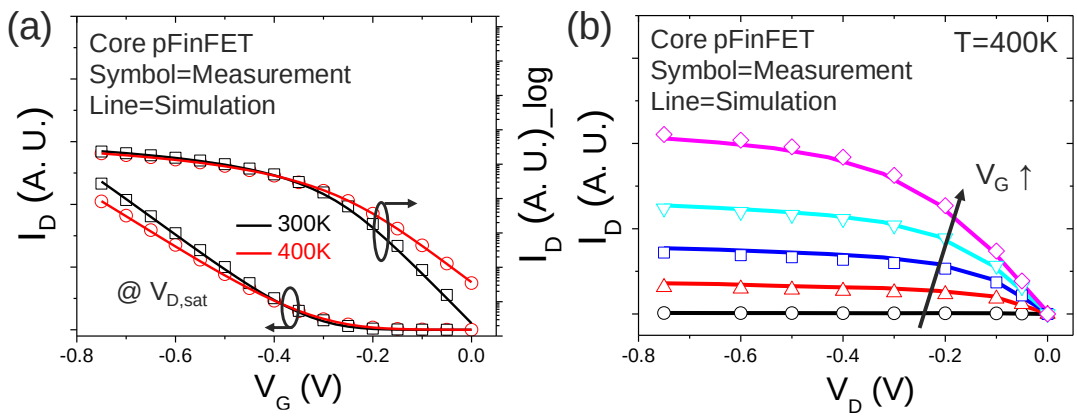

Fig. 4. (a) Calibration of the I_D-V_G and (b) I_D-V_D characteristics according to various conditions.

For accurate comparison of temperature, calibration of the I-V characteristics between simulation and measurement results is essential. In particular, I_D-V_D as well as I_D-V_G were calibrated to improve the accuracy of calibration (Figure 4(b)).

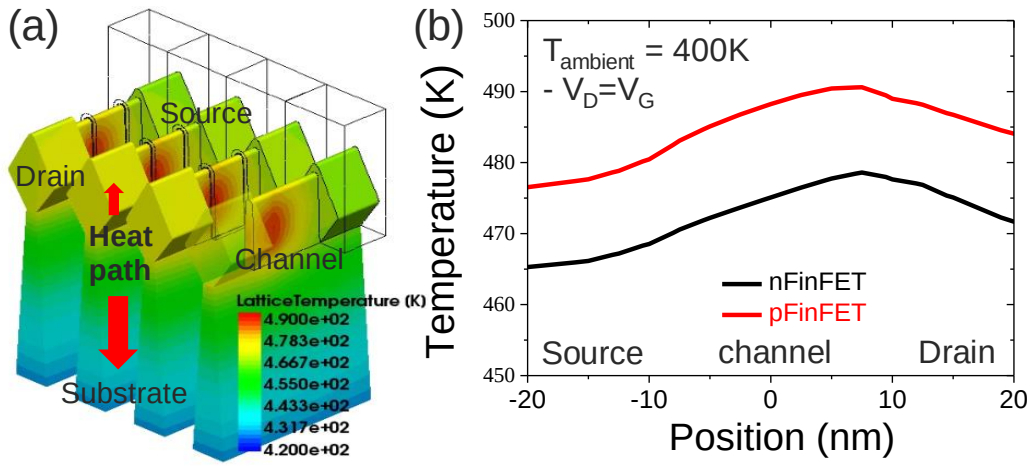

Fig. 5. (a) FinFET structure designed by TCAD simulation and the heat generation obtained during the I-V calibration (b) Device temperatures of the nFinFET and pFinFET.

Figure 5(a) shows the FinFET structure designed through TCAD simulation and the heat generation obtained during the I-V calibration process. It can be seen that the maximum temperature occurs in the drain region where the field is high, and heat is released to the S/D and substrate. SHE was considered by using the Thermodynamic model. Additionally, various thermal conductivities have been applied according to each material and thickness, and different doping concentrations and dopant materials have been considered in Si [12]. Also, due to the SiGe S/D, the thermal conductivity and strain effect which vary depending on the Ge ratio were considered. Figure 5(b) shows the device temperatures of the nFinFET and pFinFET that were extracted through simulation. Due to the low thermal conductivity of SiGe, the average device temperature of the pFinFET is high.

4.4 Bias Temperature Instability(BTI) in n/pFinFET

4.4.1 HCD simulation

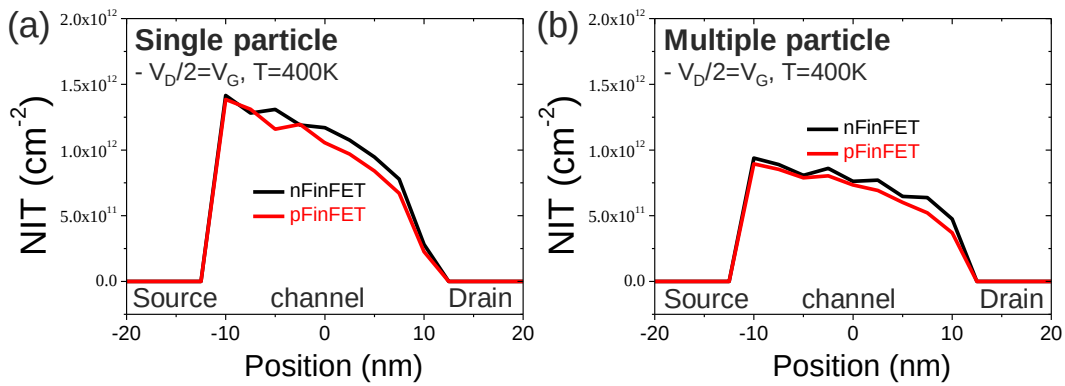

Fig. 6. Degradation of the nFinFET and pFinFET due to the (a) SP and (b) MP mechanisms.

Figure 6 shows the degradation of the two devices due to the SP and MP mechanisms. In general, the SP mechanism shows a peak in the drain region with high carrier energy. However, in this paper, the voltage condition that HCD occurs in actual logic circuits was applied ($V_D/2=V_G$). In addition, there is insufficient number of inversion carriers in the drain region because the gate voltage condition is close to the operating voltage level. Therefore, a peak appears in the source region with many inversion carriers. However, in the HCD condition used in this study, the inversion carrier of the drain region is

considerably insufficient because the gate voltage is low. Therefore, the SP mechanism peaks in the source with a large number of inversion carriers. As a result of the simulation, despite the high temperature of the pFinFET, similar SP is shown in comparison with the nFinFET. In the case of MP, carrier density is an important parameter. Electron density is higher than that of holes in the same voltage condition because electrons have larger density of state (DOS) than holes [13]. In addition, the MP mechanism decreases as the temperature increases because the life time of the Si-H bond decreases [14]. Therefore, the probability of degradation due to MP is also higher in the nFinFET. As a result, it is difficult to conclude that the HCD mechanism is the reason of the large difference of degradation between the nFinFET and pFinFET.

4.4.2 Comparison of degradation in various voltage conditions

The main mechanism of BTI varies in nFinFETs and pFinFETs. First, the main components of positive BTI (PBTI) are electrons trapped by oxide traps [15]. PBTI has especially increased due to pre-existing traps from the application of HK/MG processing. However, PBTI could be reduced by adding materials such as La or N in the processing to eliminate the trap energy levels within the high-k material [16]. Although hole trapping can also occur in the negative BTI (NBTI) condition, it is not easy for holes to move to the oxide because the energy barrier height of the Si/SiO2 interface is high and because there are barely any defect levels within the HfO2 bulk that can trap holes. Therefore, NBTI is mostly due to the interface traps generated through reaction-diffusion (RD) [17].

The holes inversed by the gate voltage react with the electrons in Si-H bonds to generate interface traps and the separated H atoms diffuse toward the gate. Therefore, this mechanism mostly occurs in pFinFETs than in nFinFETs where the inversion carriers are electrons. RD becomes more severe when the temperature and voltage conditions increase. Therefore, RD is a mechanism that can explain the high degradation of pFinFETs. Therefore, degradation was compared in high gate voltage condition to clearly observe the RD characteristics. In addition, voltage conditions with a weak drain voltage were selected to confirm the effect of self-heating on the RD.

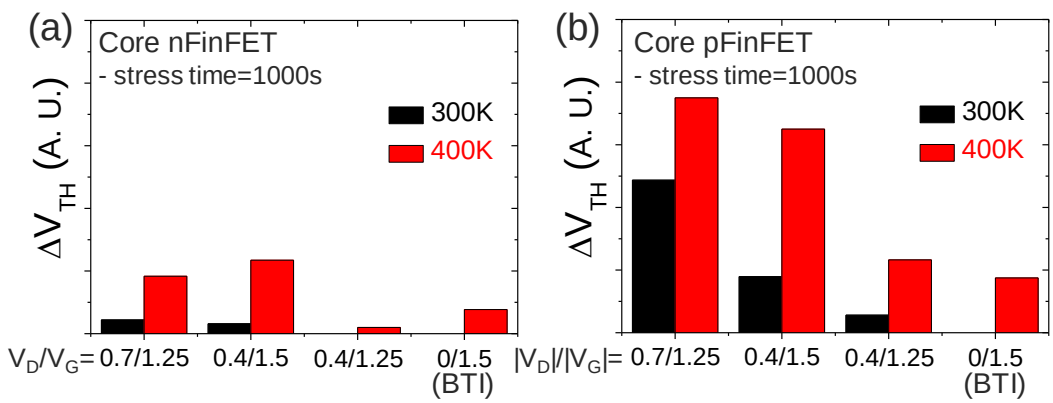

Fig. 7. Comparison of ΔV_{TH} in various voltage conditions in the (a) nFinFET and (b) pFinFET.

Figure 7 shows the comparison of ΔV_{TH} in various voltage conditions. In case of the nFinFET, degradation hardly occurred at room temperature, and degradation did not occur at 0.4V/1.25V and 0V/1.5V (PBTI). It is difficult to break Si-H bonds due to the carriers with relatively low energy because of the low drain voltage, although there are

many carriers within the channel due to the high gate voltage. (The I_B at low drain voltage (V_D = 0.7 V) is significantly smaller than the I_B at high drain voltage (V_D = 1.5 V)). However, degradation occurs in all voltage conditions in high temperature and higher degradation occurs as the gate voltage increases. Degradation in the nFinFET in high gate voltage conditions can be considered to be due to oxide traps because electron trapping becomes more active as temperature increases [18]. Also, degradation is determined by the gate voltage rather than by the drain voltage. On the other hand, higher degradation occurred in the pFinFET compared to the nFinFET in all conditions. However, the dominant mechanism cannot be confirmed as RD because there is no clear tendency according to the voltage condition. Therefore, it is necessary to confirm if the main component of degradation of the pFinFET is RD.

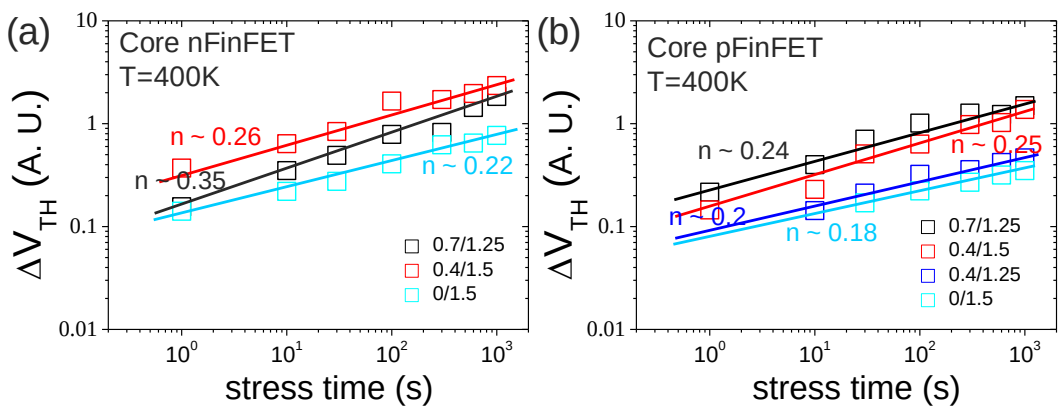

Fig. 8. Comparison of time exponents extracted in various voltage conditions in the (a) nFinFET and (b) pFinFET.

Figure 8 shows the comparison of time exponents extracted at various voltage conditions. The nFinFET shows various time exponents depending on the voltage condition. This is because oxide traps and interface traps are generated at the same time, and the time exponent decreases as the oxide trap component increases. On the other hand, in the pFinFET, n values range between 0.18 and 0.25 in all conditions, and are similar to the n values of RD reported in previous literatures [19]. Therefore, it can be considered that the interface trap due to RD is the dominant mechanism rather than due to oxide traps. However, it is difficult to determine the cause of this result as RD only with time exponents. Therefore, the on-current degradation ratio was used for additional verification.

4.4.3 On-current degradation rate

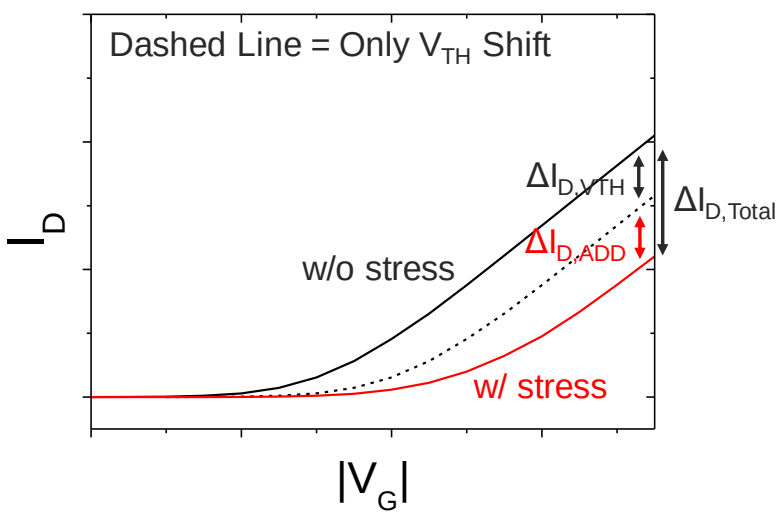

Fig. 9. Ratio between the total on-current degradation($\Delta I_{D,Total}$) and additional on-current degradation($\Delta I_{D,ADD}$).

Interface traps and oxide traps change the V_{TH}. Therefore, variation of on-current due to the changed V_{TH} is also accompanied. We defined the on-current degradation by the V_{TH} shift as $\Delta I_{D,VTH}$. However, the interface traps act as scattering centers causing additional on-current degradation. Therefore, additional on-current degradation was defined as $\Delta I_{D,ADD}$, excluding $\Delta I_{D,VTH}$ from the total on-current degradation ($\Delta I_{D,Total}$). Therefore, $\Delta I_{D,ADD}$ should occur if interface traps are generated due to RD. Thus, the on-current degradations in each condition were compared to analyze RD generation. Figure 9 shows the ratio between the total on-current degradation ($\Delta I_{D,ADD}/\Delta I_{D,Total}$). If ΔID,Total due to the interface traps does not occur, all degradation components are oxide traps and the ratio becomes zero.

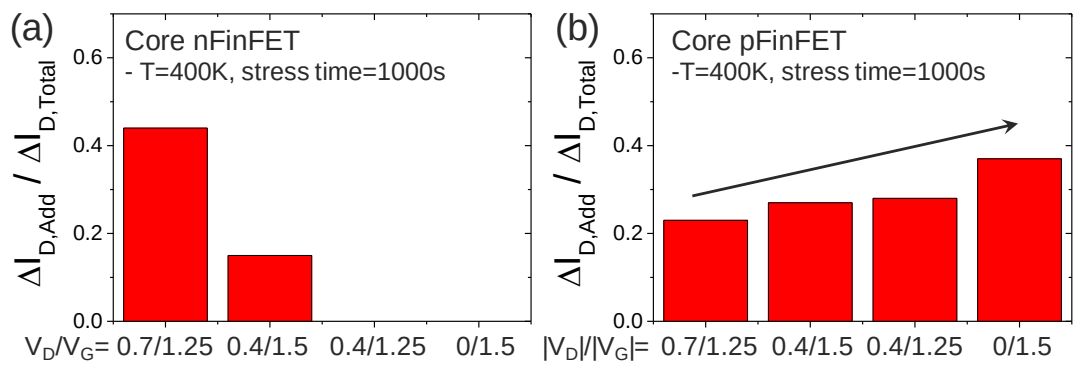

Fig. 10. Comparison of $\Delta I_{D,ADD}/\Delta I_{D,Total}$ in various voltage conditions in the (a) nFinFET and (b) pFinFET.

Figure 10 shows the comparison of $\Delta I_{D,ADD}/\Delta I_{D,Total}$ in various voltage conditions. For

the nFinFET, $\Delta I_{D,ADD}$ did not occur although the V_{TH} changed in the 0.4V/1.25V and 0V/1.5V (PBTI) conditions. Therefore, the degradation in these two conditions are solely due to oxide traps in the IL/HK interface which are far away from the channel. Also, the reason why the ratio at 0.4V/1.5V is smaller than at 0.7V/1.25V is because oxide traps increase. On the other hand, the pFinFET shows opposite tendency from the nFinFET. This is because the interface traps due to RD are mainly generated in the source region unlike hot carriers. The distribution of inversed holes increases toward the source direction because drain voltage is applied and RD occurs in proportion to the hole density. Therefore, RD is concentrated in the source region as the drain voltage increases which reduces the scattering probability of carriers passing the channel. The scattering probability is highest when the drain voltage is not applied and RD evenly occurs within the channel. Therefore, the $\Delta I_{D,ADD}/\Delta I_{D,Total}$ increases as the drain voltage decreases. It can be confirmed through these results that interface traps are generated by RD even if drain voltage is applied. Finally, simulation was used to analyze the tendencies of temperature and degradation to predict the temperature at each voltage condition.

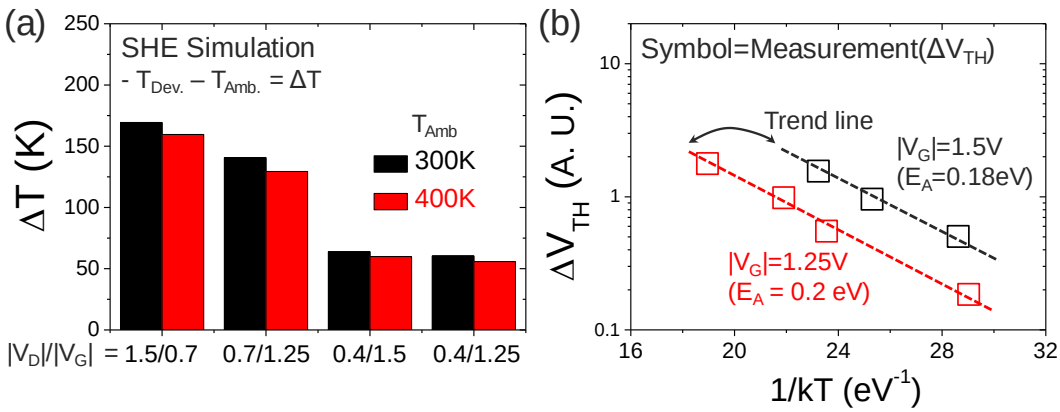

Fig. 11. (a) Temperature predicted through simulation in each voltage condition (b) Relationship between ΔV_{TH} and temperature in the pFinFET in each voltage condition.

Figure 11(a) shows the comparison of temperature in each voltage condition predicted through simulation. As mentioned above, the absolute value of the temperature predicted through the simulation does not have significant meaning because accurate device temperature cannot be measured. Therefore, the temperature increased by self-heating (ΔT) was compared by the difference between the ambient temperature (T_{Amb}) and device temperature (T_{Dev}) in each voltage condition. Even at room temperature, the device temperature can be quite high due to SHE under conditions where the drain voltage is high. High degradation may occur regardless of low gate voltage when comparing conditions at 0.7V/1.25V and 0.4V/1.5V, and this can be explained by the high temperature. Also, it was confirmed that the degradation tendency matches the temperature tendency.

Figure 11(b) shows the ΔV_{TH} in each voltage condition and the temperature tendency predicted through simulation. Degradation increases in proportion to increasing

temperature. Also, degradation increases as the gate voltage increases at similar temperature. This tendency can be determined as RD. Therefore, additional RD due to SHE was found to cause higher degradation in the pFinFET than in the nFinFET in various voltage conditions. However, RD may be the dominant mechanism in these analyzed voltage conditions because the gate voltage is relatively high. This paper focuses on analyzing the factor that causes higher degradation in the pFinFET than the nFinFET in HCD condition. Therefore, analysis was conducted on the effect of RD on the total degradation in basic HCD condition ($V_D/2=V_G$) using TCAD simulation.

4.4.4 RD simulation

RD simulation is required to investigate the degradation components in HCD condition. The largest problem of the conventional RD model is that recovery characteristics cannot be properly predicted. However, accuracy of recovery characteristics has been improved through compact modeling (transient trap occupancy model; TTOM) based on measurements [20]. Also, the improved RD model can well express the results calculated by the nonradiative multiphonon(NMP) trapping model. Therefore, the improved RD model has been used in this study. The multistate configuration (MSC)-hydrogen transport degradation model which is based on the improved RD model is applied in the Sentaurus TCAD simulation. The inversed holes enter the Si-H bonds at the Si/SiO2 interface to react with electrons and generate H atoms. The H atoms diffuse to the Si/SiO2 interface and react with other H atoms to create H2 molecules. Finally, the

generated H2 molecules diffuse to the gate.

$$\text{Si-H} + \text{h}^+ \underset{K_r}{\overset{K_f}{\rightleftharpoons}} \text{Si}^+ + \text{H}^{(1)} \qquad (1)$$

$$\text{Si-H} + \text{H}^{(1)} \underset{K_{r2}}{\overset{K_{f2}}{\rightleftharpoons}} \text{Si} + \text{H}_2 \qquad (2)$$

The equation related to interface trap generation due to RD is shown below and the fitting parameters were applied by referring to related literatures [21].

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_{IT} N_H \qquad (3)$$

$$k_F = k_{F0} e^{\frac{-E_{AkF}}{kT}}, \quad k_{F0} = c_p \sigma v_{th} p e^{\Gamma Eox} \qquad (4)$$

$$k_R = k_{R0} e^{\frac{-E_{AkR}}{kT}} \qquad (5)$$

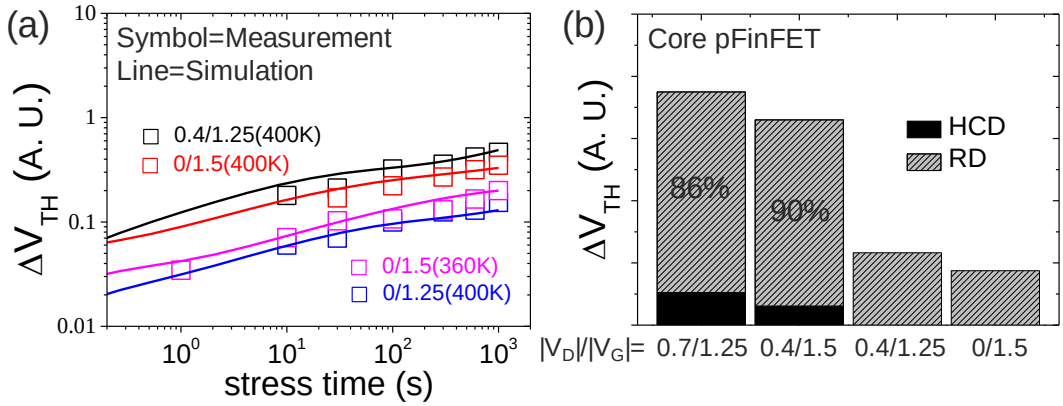

Fig. 12. (a) Calibrated ΔV_{TH} in various voltage conditions through RD simulation and (b) RD portion of degradation predicted through simulation.

Figure 12(a) shows the calibrated ΔV_{TH} in various voltage conditions through RD simulation. There should be less interface traps or oxide traps due to hot carriers in the pFinFET than in the nFinFET. Therefore, there is no degradation due to the hot carriers in the pFinFET at 0.4V/1.25V condition because degradation barely occurs in the nFinFET in this same condition (Figure 7(a)). As a result, it can be assumed that degradation in the pFinFET at 0.4V/1.25V is solely due to the RD. Therefore, calibration was performed with in three voltage conditions and two temperature conditions to confirm that the simulation results well match the measurements. RD simulation was conducted in each voltage condition by applying the parameters extracted through calibration. Figure 12(b) shows the RD predicted by simulation. The 0.4V/1.25V and 0V/1.5V conditions only showed RD and the other two conditions also showed high ratio of RD.

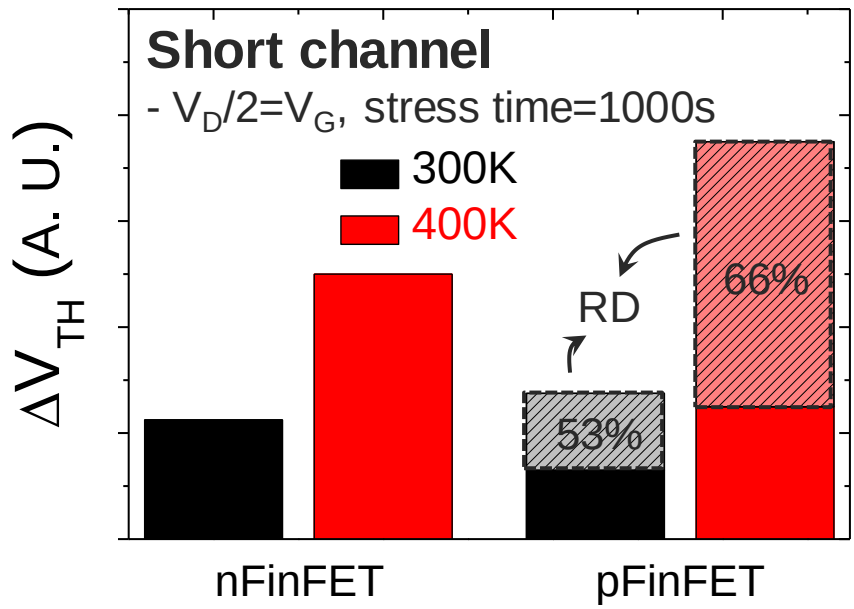

Fig. 13. RD component predicted through simulation in the HCD condition.

Figure 13 shows RD predicted through simulation in the HCD condition. As mentioned above, interface traps due to RD are not shown in the nFinFET. On the other hand, approximately 53% and 66% RD was predicted in the pFinFET at 300K and 400K, respectively. Besides the RD in the total degradation, the remaining degradation is predicted to be due to hot carriers. Therefore, degradation due to pure hot carriers occurs more in the nFinFET than in the pFinFET, and these results match with conventional theories. As a result, an additional RD occurs in short-channel pFinFETs at HCD condition due to severe SHE regardless of low gate voltage. Therefore, higher degradation is observed in the pFinFET than in the nFinFET. Also, degradation in the pFinFET at HCD condition becomes worse as devices are further scaled down.

4.5 Summary

Degradation occurs more in the 10 nm node pFinFETs than the nFinFETs at HCD condition. Therefore, degradation was measured in various voltage conditions to investigate the main degradation components in the nFinFET and pFinFET. Interface traps due to carrier collision are the dominant components in the nFinFET and oxide traps may occur due to electron trapping. On the other hand, SHE is more severe in pFinFETs than in nFinFETs because SiGe, which has low thermal conductivity, is used as the S/D in pFinFETs. Therefore, RD mechanism occurs regardless of the HCD condition because the device temperature is high. We have confirmed by using time exponents and $\Delta I_{D,ADD}/\Delta I_{D,Total}$ that RD occurs in the pFinFET. Therefore, higher degradation occurs at HCD condition in the pFinFET because additional interface traps are generated due to RD.

Finally, RD results that occurred in each condition were extracted through TCAD simulation and it was found that 60% of the degradation at the HCD condition was due to RD.

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Chapter 5
Conclusion

In this dissertation, we analyzed the hot carrier degradation of 3D FinFET based on the physical theory. In the process of research, a TCAD framework is improved to predict HCD based on physical theories precisely by applying EES in a simulation model. Moreover, consistency was confirmed through comparison between the measured data of a 14 nm node FinFET and simulation model. Calibration was performed in three stress voltage conditions. The parameters of the HCD model were extracted through the iteration. In the different stress conditions predicted by the simulation model with the extracted parameters, the results obtained from the improved model showed the better agreement with the measured data than the previous model. In addition, the temperature dependence of HCD was analyzed under two voltage conditions. In the case of oxide traps, deterioration increases as temperature increases under all conditions. However, in the case of interface traps, opposite temperature dependence was shown under two voltage conditions. In order to analyze this dependence, interface traps were separated into three components and the temperature dependence of each component was analyzed. MP and FP have a constant temperature trend depending on voltage conditions. However, SP is highly influenced by scattering and shows various temperature dependences. As a

result, based on the physical theory, a simulation model was established that considers all trends of various voltages and temperatures.

However, due to the self-heating, FinFET has different temperatures at accelerated conditions and nominal operating condition. In the nominal operating region, FP disappears due to weak self-heating. However, the components vary depending on the structure of the device and the operating voltage. Therefore, it is necessary to consider these components when determining the acceleration condition.

In the 10 nm node FinFET, degradation occurs more pFinFETs than the nFinFETs at HCD condition. Therefore, degradation was measured in various voltage conditions to investigate the main degradation components in the nFinFET and pFinFET. Interface traps due to carrier collision are the dominant components in the nFinFET and oxide traps may occur due to electron trapping. On the other hand, SHE is more severe in pFinFETs than in nFinFETs because SiGe, which has low thermal conductivity, is used as the S/D in pFinFETs. Therefore, RD mechanism occurs regardless of the HCD condition because the device temperature is high. We have confirmed by using time exponents and $\Delta I_{D,ADD}/\Delta I_{D,Total}$ that RD occurs in the pFinFET. Therefore, higher degradation occurs at HCD condition in the pFinFET because additional interface traps are generated due to RD. Finally, RD results that occurred in each condition were extracted through TCAD simulation and it was found that 60% of the degradation at the HCD condition was due to RD.

초 록

CMOS 로직 소자는 퍼포먼스를 향상시키기 위해 지속적으로 축소화 되고 있다. 하지만 구조 파라미터들의 축소화에 비해 동작 전압은 충분히 감소하지 않는다. 따라서 소자 내 수직 전계나 온도가 증가하는 추세이기 때문에 신뢰성은 계속해서 문제가 되고 있다. 최근 3D 소자의 신뢰성에 대한 연구는 많이 진행되고 있지만 empirical 모델링과 관련된 연구가 대부분이다. 따라서 본 연구에서는 실제 측정을 기반으로 시뮬레이션을 이용하여 물리적 이론 중심으로 로직 소자의 핫캐리어 신뢰성을 분석하였다.

먼저 핫캐리어 모델의 정확성을 향상시키기 위해서 TCAD 시뮬레이션에 electron-electron scattering을 적용하였다. 추가적으로 3D FinFET의 측정 데이터와 calibration을 진행하여 모델의 정합성을 확인하였다. calibration 과정에서는 모든 scattering 메커니즘을 고려하기 위해 다양한 전압과 온도 조건이 필요하다. 따라서 다양한 전압 조건에 따른 HCD를 분석하고, calibration을 진행하여 HCD 모델의 파라미터를 추출하였다. 다음으로 전압 조건에 따른 HCD의 온도 경향성을 분석하였다. oxide trap과 달리 interface trap은 전압 조건에 따라 다른 온도 경향성을 보인다. 따라서 interface trap을 3가지 성분으로 분리하여 각 성분의 온도 경향성을 분석하였다.

Multiple particle process(MP)과 field enhanced thermal degradation process(FP)는 전압 조건과 상관없이 일정한 온도 경향성을 가진다. 반면 Single particle process(SP)는 scattering의 영향을 받기 때문에 온도 경향성은 전압 조건에 따라 달라진다. 온도 경향성 분석 과정에서도 calibration을 진행하며 여러 번의 iteration을 통해 다양한 전압 및 온도가 고려된 파라미터를 추출한다. 추출된 파라미터를 적용한 시뮬레이션 모델은 기존의 모델보다 더 정확하게 HCD 측정 결과를 예측하였다. 결과적으로 물리적 이론에 근거하여 시뮬레이션 모델 구축함으로써 HCD 분석의 정확성을 향상시켰다.

하지만 가속 조건과 동작 조건의 self-heating 효과가 다르기 때문에 소자가 실제 CMOS 회로의 동작 조건에서 interface trap을 발생시키는 메커니즘은 다를 수 있다. 따라서 우리는 동작 영역에서의 각 성분의 비율까지 예측하였다. 마지막으로 우리는 10 nm node 소자에서 nFinFET에 비해 pFinFET에서 높은 열화가 발생하는 원인에 대해 분석하였다. pFinFET은 소스/드레인 물질로 SiGe를 사용하기 때문에 nFinFET에 비해 self-heating 효과가 심하여 소자 온도가 도 높다. 이론적으로 MP 메커니즘의 lifetime은 온도가 증가할수록 감소하기 때문에 MP에 의한 열화 또한 감소한다. 따라서 소자 온도가 더 높은 pFinFET에서 nFinFET에 비해 더 많은 MP가 발생하기 어렵다. 하지만 nFinFET 과 달리 pFinFET에서는

Si-H bond의 electron과 hole이 반응하여 interface trap을 생성시키는 RD가 발생할 수 있다. 또한 RD는 온도가 높을수록 더 많은 열화가 발생하기 때문에, pFinFET에서 nFinFET보다 더 많은 열화가 발생하는 현상을 설명할 수 있다. 따라서 우리는 HCD 조건이지만 소자 온도가 높은 pFinFET에서 추가적인 RD 메커니즘이 발생할 수 있다고 제안한다. 다양한 전압 조건에서의 전류 열화율을 통해 주요 열화 메커니즘을 분석하였으며 pFinFET에서는 RD가 주요함을 확인하였다. 또한 TCAD 시뮬레이션을 이용하여 HCD 조건에서 발생할 수 있는 RD를 예측하였다. 그 결과 RD를 제외한 순수 hot carrier 성분은 pFinFET보다 nFinFET에서 더 많이 발생한다.

주요어 : FinFET, Hot Carrier Degradation (HCD), Bias Temperature Instability (BTI), Reaction-Diffusion(RD), Self-heating

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