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FLEXIBLE MEMS:
A NOVEL TECHNOLOGY TO FABRICATE FLEXIBLE SENSORS AND ELECTRONICS

by

HONGEN TU

DISSERTATON

Submitted to the Graduate School

of Wayne State University,

Detroit, Michigan

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

2014

MAJOR: ELECTRICAL ENGINEERING

Approved by:

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Adviser Date

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// ACKNOWLEDGMENTS

I would like to express my sincere appreciation and thanks to my advisor Professor Yong Xu who has been a tremendous mentor for me throughout my PhD career. I would like to thank him for providing ingenious ideas and great insight on my research projects and for allowing me to grow as a research scientist. I would also like to thank my committee members, Dr. Amar S. Basu, Dr. Ming-Cheng Cheng and Dr. Jinsheng Zhang for serving as my committee members and for their support, comments and suggestions.

I would also like to thank all of the helpful staff at nFab including Bill Funk and Dan Durisin for providing critical technical support during my cleanroom fabrication. I would like to acknowledge my fellow lab mates Dr. Yuefa Li and Dr.Qinglong Zheng for guiding me through all of the important microfabrication techniques. My appreciation also goes to Yating Hu, Jessin John and Eric Kim, and everyone that has been there to support me for all of my research activities.

A special thanks goes to my family. Words cannot express how grateful I am to my parents Maozi Tu/YongZhen Gao and my sister Huan Tu for all of their love, sacrifices and unconditional support towards my career. My special thanks also go to my wife Mengying Liu for being here with me every step of the way.

Finally, I would like to thank Wayne State University for providing me with wonderful resources including a variety of classes and state of the art facilities to support all of my research activities.

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CHAPTER 1. Introduction

1.1 Motivation

MEMS (Micro Electro Mechanical System) devices and CMOS (Complementary Metal Oxide Semiconductor) circuits [1, 2] are traditionally fabricated on rigid substrates with inorganic semiconductor material such as silicon. However, it is highly desirable for functional elements like sensors, actuators or micro fluidic components to be fabricated on flexible substrates for a wide variety of applications. A number of approaches to make flexible sensors or electronics have been developed over the past two decades. The most straightforward approach is the direct fabrication of functional components on a flexible substrate, such as the widely used flexible printed circuitry technology [3] and the thin film transistor (TFT) technology [4-6] on flexible substrates. Various flexible sensors and electronics have been developed as wearable health monitoring devices and medical implants[5]. This direct fabrication of functional elements on flexible substrate has the advantages of simple fabrication process and low cost. Large area flexible sensors or electronics can be fabricated economically using this method. However, due to the flexible substrate, the process temperature is limited and the material properties are not optimized. This temperature limit makes it almost impossible to monolithically integrate CMOS circuits and many MEMS transducers to the flexible substrate.

A flexible skin technology based on silicon island structure has also been demonstrated. The basic structure of the flexible skin is arrays of silicon islands sandwiched

by two layers of polymer. The advantage of this technology is its compatibility with MEMS and CMOS since MEMS devices and CMOS circuits can be fabricated on the silicon wafer before the formation of the flexible skin. The minimum bending radius is determined by the size the of the silicon islands. Based on this technology, flexible shear stress sensor skins [7], the integration of CMOS with the flexible skin [8], and intelligent textiles [9], have been demonstrated.

Recently an innovative "transfer printing" method to make flexible electronics has also been demonstrated [10-13]. More specifically, transistors and other devices are fabricated first on SOI (Silicon-on-Insulator) wafers and then released by sacrificial etching and transferred to flexible substrates by a method similar to "printing." Many exciting applications have been demonstrated [14-16]. On the other hand, this transfer printing step is a yield-limiting step, especially when the device density increases. In addition, the releasing step is generally incompatible with commercial CMOS processes. Therefore, this method cannot fully take advantage of the mainstream CMOS technology.

In order to address the above mentioned drawbacks of existing technologies, alternative methods have been developed in our lab over the last a few years. We proposed a novel technology based on XeF_2 (xenon difluoride) isotropic silicon etching and parylene C conformal coating, which is able to monolithically incorporate high temperature materials and fluidic channels. This technology has been applied to a variety of applications which are discussed in the following chapters.

1.2 Review of flexible electronics

A common method to make flexible devices is the direct fabrication of components on flexible substrates, such as the widely used flexible printed circuit board (PCB) technology and the thin film transistor (TFT) technology on flexible substrates. Various electronics devices has been developed utilizing the aforementioned technology.

Another popular method to make electronics flexible is direct mounting of ICs (integrated Circuits) on a flexible printed circuit as demonstrated in Figure 1.1. Polyimide, PEEK or transparent conductive plastic films are a few of the materials commonly used as the flexible substrate in electronic industry. Only simple metal traces to interconnect IC components are required to be fabricated on the flexible substrate, leading to very simple fabrication process. This flexible PCB technology significantly reduced the development cost since the technology used to make rigid PCB can be directly applied to make flexible PCB such as metal etching and silver screen printing. Flexible PCB can be found everywhere in our daily lives. For example, it has been widely used in laptop computers as interconnects between motherboard and display. Unlike the conventional rigid PCB, flexible PCB allow the designer to bent and flex the PCB to a certain degree which gives us much needed freedom to integrate electronics into 3D spaces. As consumer electronic devices are getting smaller, flexible PCB becomes a necessity to establish interconnects between modules.

Figure 1.1. Flexible PCB inside an Olympus Stylus camera. From: Steve Jurvetson http://flickr.com/photos/44124348109@N01/2265519.

One drawback of the flexible PCB technology is that the bulky packaged IC significantly reduces the overall flexibility of the device. The design of the electronics is limited by the availability and form factor of the IC used. To overcome this drawback, the thin film transistor (TFT) technology has been implemented on flexible substrates. Transistors, the most fundamental elements in building ICs, are traditionally fabricated on rigid substrate like silicon wafers. In order to make transistor on flexible substrate, low temperature semiconductor material has to be developed. For example, in references [17, 18], a flexible organic transistor with extreme bending stability has been developed as demonstrated in Figure 1.2. A flexible polyimide sheet was used as the substrate for the fabrication of transistors in this case. Low process temperature material such as organic self-assembled monolayer (SAM) was chosen to be the gate dielectric layer. Note that only low

temperature material and processes are compatible with this technology. Thanks to the organic material used here, the maximum process temperature is limited to be less than 100°C

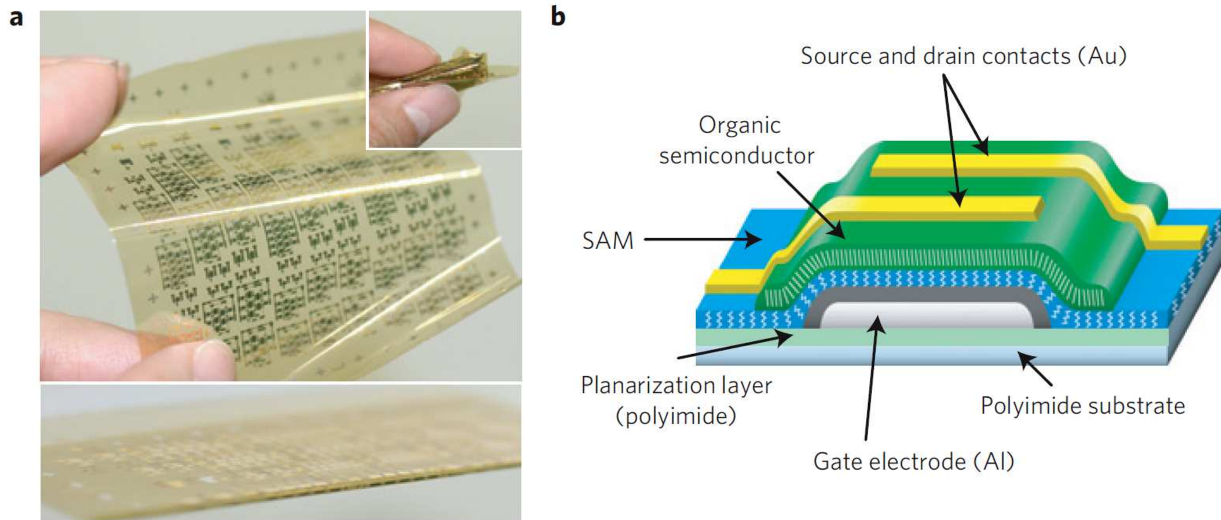


Figure 1.2 (a) Photographs of a 12.5 μm thick polyimide substrate with functional organic TFTs and organic complementary circuits[17] . The array has an area of 75x75mm^2. (b), Schematic cross-section of the TFTs.

Without the bulky ICs used in flexible PCB technology, thin film transistor (TFT) technology on flexible substrates makes the device highly flexible. As seen in Figure 1.2, successfully fabricated low-voltage organic transistors, which were placed at the neutral strain position, were folded into a bending radius as small as 100 µm without damage to the device. This technology opens a wide range of opportunities for electronic applications that require a high degree of mechanical flexibility. A lot of efforts have been dedicated in the research community to directly integrate low temperature organic materials onto flexible substrate with an intention to reduce the cost and simplify the manufacturing processes.

One drawback is that organic and low temperature materials used in TFT technology normally are not very stable and lack the performance compared with high temperature materials like silicon. Conventional silicon semiconductor devices still perform much better and are required by many applications.

There are technologies developed specifically to integrate silicon devices on flexible substrate. In reference [9], a novel intelligent textile technology based on the integration of silicon flexible skins has been reported.

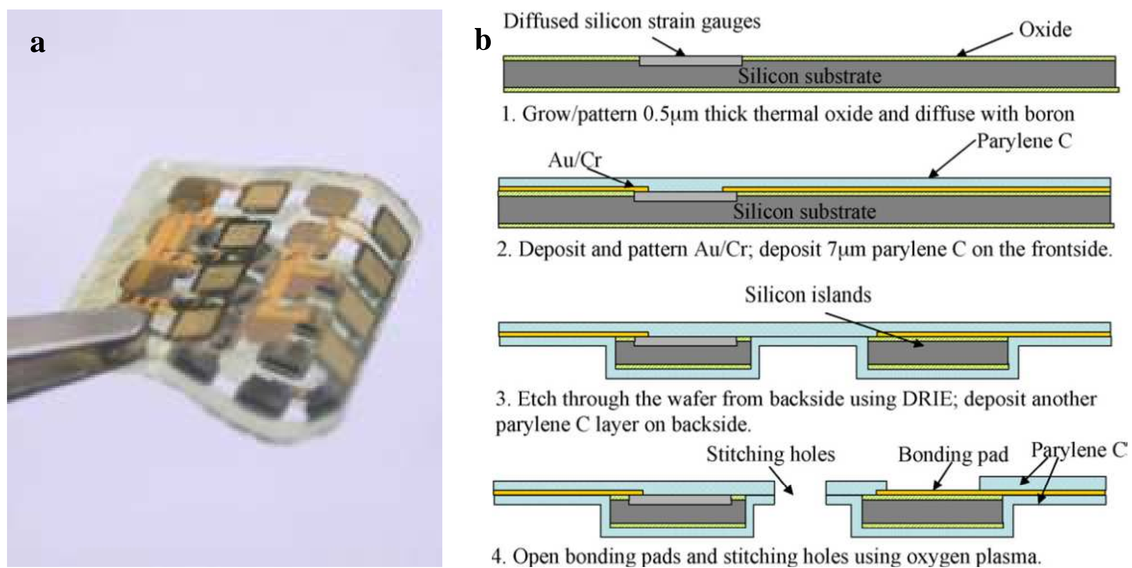


Figure 1.3. (a) Picture of a folded skin; (b) Simplified process flow of the flexible skin with integrated strain gauges [9].

As demonstrated in Figure 1.3 (b), simple strain gauges (can be replaced by MEMS devices or ICs) have already been fabricated on the silicon substrate, the first step of the skin development is the fabrication of functional electronic components on a silicon wafer. High

temperature processes are allowed since there are no polymer materials introduced at this stage. Then a polymer layer is coated on the front-side of the wafer. Afterwards, the polymer layer is patterned to expose metal pads. Then, the silicon wafer is thinned down and etched through from the back to form the arrays of silicon islands by deep reactive ion etching (DRIE). Finally, another layer of polymer is coated on the backside to encapsulate silicon islands. The basic structure of the flexible skin is arrays of rigid silicon islands sandwiched by two layers of polymer. A great advantage of this technology is the compatibility with MEMS and IC fabrications. However, due to the large silicon island used here, the minimum bending radius is limited by the size the of the silicon island. In addition, stress concentration between the flexible polymer and rigid silicon has to be addressed to make the whole system more robust.

In addition, other approaches to make flexible electronics without the compromise of high temperature materials have also been developed over the past few years. For instance, functional electronic components are first fabricated on a SOI wafer and then transferred onto a flexible substrate via a stamping method. Additional low temperature processes like the metallization of components are performed directly on the flexible substrate.

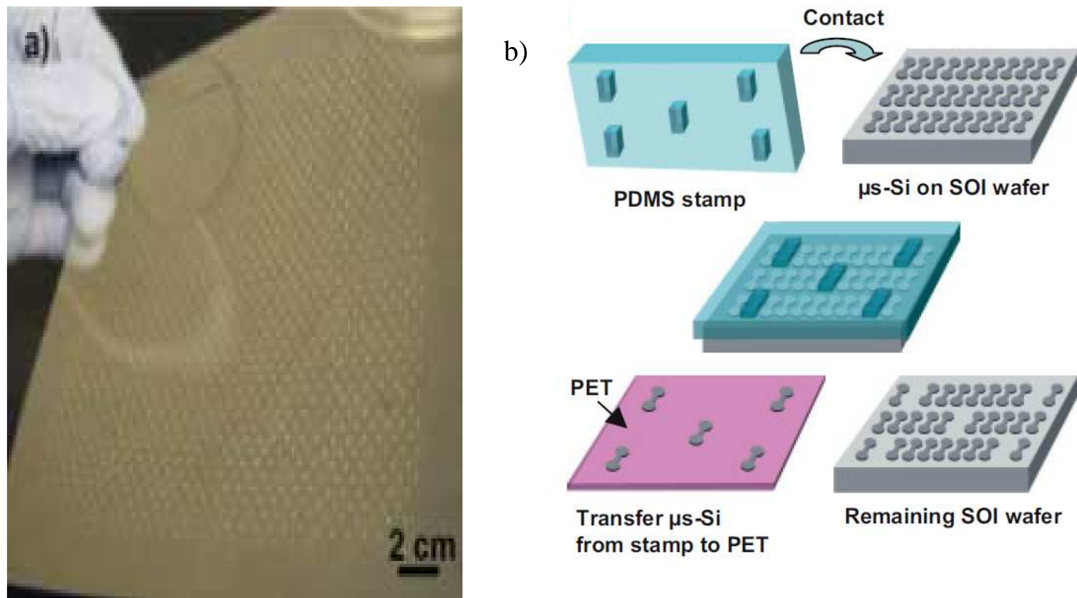


Figure 1.4. (a) Optical images of the selective transfer of μs-Si onto a PU/PET sheet; (b)Schematic illustration of selective transfer of us-Si onto PET plastic substrate using patterned hard PDMS [13].

In reference [13], a printing-based approach to make high-performance single-crystal silicon transistors on flexible substrates was reported. As demonstrated in Figure 1.4, a SOI wafer consisting of silicon device layer, buried oxide layer and handling silicon layer were used in the process. The silicon devices (μs-Si) were first fabricated on a SOI wafer by patterning the silicon device layer. A controlled oxide etch was performed to remove the majority of the underling oxide layer. Only a small portion of the oxide layer was left to temporarily hold the μs-Si in position. A specifically designed and patterned PDMS stamp was used to contact the selected μs-Si. Due to the strong adhesion between PDMS and μs-Si, μs-Si can be easily peeled off and transferred to another PET substrate.

Due to the fact that the remaining oxide layer was removed by physical forces, it will destroy part of the μs-Si. Therefore, this risky transfer printing step is a yield-limiting step, especially when the device density increases. In addition, the oxide etching solution (hydrofluoric acid) used in the releasing step makes the process incompatible with commercial CMOS processes. Therefore, this method cannot fully take advantage of the mainstream CMOS technology.

The technology developed in our lab does not suffer from the aforementioned limitations. Both transfer printing method and our method are able to integrate single crystal silicon devices. However, unlike transfer printing method, our method does not need a transfer step and thus has a higher yield. We are able to release the device layer off the handling silicon wafer by an innovative method which will be discussed and presented in the following chapters. Furthermore, our method is post SOI-CMOS compatible, which allows us to utilize commercial foundry and saves a lot of development time and cost.

1.3 Review of the key material and processes

1.3.1 Parylene C chemical vapor deposition

Parylene also known as poly(p-xylylene) is a polymer commonly used as structure material, moisture and dielectric barriers in MEMS and electronic devices[19-21]. There are many more benefits associated with the the parylene. For example, parylene film exhibits strong chemical resistance and thus is considered as a good barrier for organic and inorganic media, acids and caustic solutions and gases. In addition, parylene's biocompatibility has also been proven and been utilized in many biomedical applications [22-24].

There are three major parylene polymers referred as payrlene C, parylene N and parylene D. Parylene N provides higher dielectric strength and more stable dielectric constant. parylene D will maintain its physical strength and electrical properties at slightly higher temperatures compared with parylene C the most predominant type of parylene. Parylene C is used for almost all types of applications, including our process as well.

	Density (g/cm)	**Young's modulus (Gpa)**	**Tensile strength (Mpa)**	**Dielectric constant (at 1MHz)**
Parylene C	1.289	2.8	68.9	2.95
Polyimide	1.42	3.2	70-90	3.5

Table 1.1 Lists of selected properties of parylene C and polyimide

To better understand the physical properties of parylene C, a comparison between polyimide and parylene C used in our process is presented in Table 1.1. Both polyimide and parylene exhibit very similar mechanical properties. In many applications parylene can just simply replace polyimide. One major difference between those two materials is the coating process. Polyimide is normally dissolved in solvent and then applied to the substrate via spin coating. Thickness of the coated film is determined by the spin speed and the viscosity of the dissolved solutions. On the other hand, a process called Chemical Vapor Deposition (CVD) [25] is used to deposit parylene film on the substrate. A simplified block diagram of parylene deposition system is demonstrated in Figure 1.5

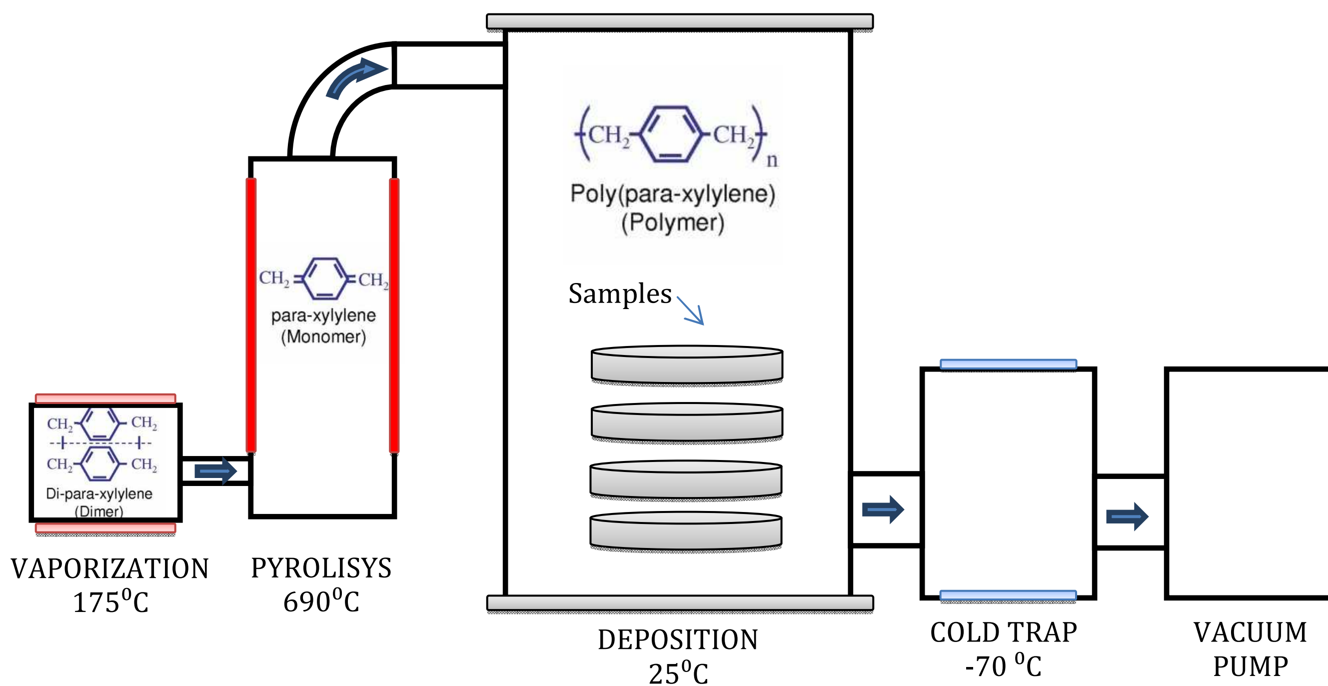


Figure 1.5. A common setup flow of chemical vapor deposition of parylene

Parylene coating is a room temperature CVD process. The parylene dimer is first loaded inside the vaporization chamber. The vacuum pump will bring the entire system under vacuum condition. Under the vacuum condition The Dimer begins to vaporize once this vaporization chamber reaches the temperature of 175 ^{o}C. The vapor passes through the pyrolysis chamber to undergo a thermal decomposition process and breaks down into a monomer at 690 ^{o}C. When the monomer reaches the sample in the deposition chamber at room temperature, it will conformally coat the entire exposed surface and cross-linke to form a parylene film. Excessive monomer will then be trapped by the cold trap to prevent damage to the vacuum pump.

A great benefit of CVD is that the deposition is highly conformal. As schematically illustrated in Figure 1.6, the coating material will get inside a feature with steps and undercut cavities to encapsulate the entire surface. This feature is not feasible using the conventional spin coating process.

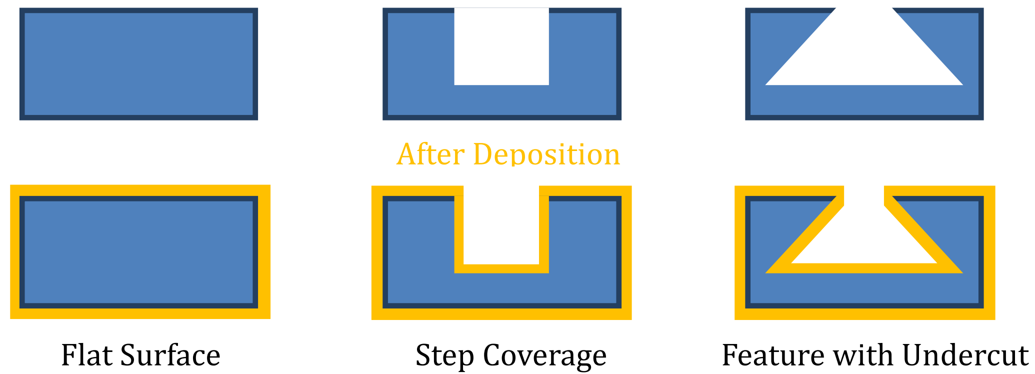
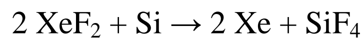


Figure 1.6. Schematic illustration of conformal CVD coating.

1.3.2 XeF_2 isotropic silicon etching

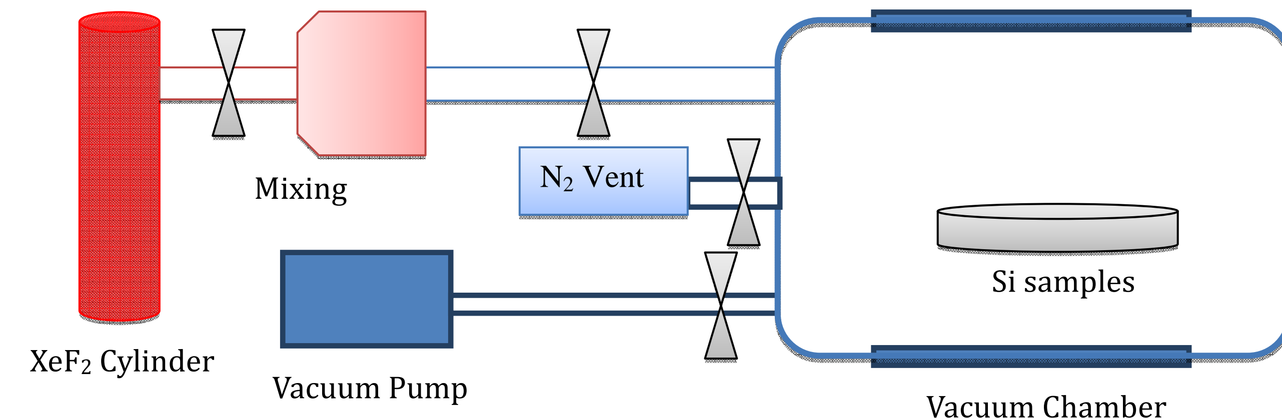
Another important etching procedure called XeF_2 (Xenon difluoride) [26] isotropic silicon etching has been utilized in our process. This isotropic gaseous etchant for silicon, has been widely used in the semiconductor industry, particularly in the production of MEMS devices [27, 28].

The etching mechanism is actually very simple and easy to implement. First, the XeF_2 molecule dissociates to xenon and fluorine when the gas reaches the surface of silicon. Fluorine then reacts with silicon and forms another gas-phase byproduct. The reaction describing the reaction process is listed below:



$$2\ XeF_2 + Si \rightarrow 2\ Xe + SiF_4$$

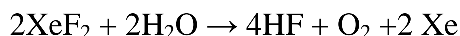
Unlike other plasma etching process, XeF2 has a relatively high etch rate and does not require ion bombardment or external energy sources to etch silicon. A simple illustration of etching apparatus is shown in Figure 1.7.



Control Valves

Figure 1.7. Schematic of XeF_2 isotropic silicon etching apparatus.

First, highly concentrated XeF_2 etching gas is contained in a pressurized container. A needle valve is placed between the gas cylinder and mixing chamber which functions as a buffer to prevent gas from coming out too fast. The sample to be etched is then placed inside a vacuum chamber and pumped down to 50 millitorr. N_2 gas is used here to purge the chamber to eliminate any residual moisture. XeF_2 is highly reactive and will react with moisture and produce highly corrosive and dangerous HF as indicated by the formula presented below.



$$2XeF_2 + 2H_2O \rightarrow 4HF + O_2 + 2\,Xe$$

After the removal of the moisture, the vacuum pump is stopped and leakage is checked before opening the valve after mixing chamber. Due to the nature of the reaction, pressure inside the vacuum chamber will rise up to around 700 millitorr in our particular setup before closure of the valve from the mixing chamber. This practice gives us better control over the

amount of the XeF_2 that gets inside the etching chamber. Vacuum chamber pressure will keep rising up to around 800 millitor before all of the XeF2 gas is consumed. A complete etching loop is complete at this point. Additional loops are repeated to control the amount of the etching.

XeF_2 silicon etching process is highly selective. A variety of material can be used as masking layer which include but are not limited to photoresist, parylene, metals and silicon dioxide. Another key characteristic of this gas phased etching process is that the process is highly isotropic. As demonstrated in Figure 1.8, huge undercut can be observed after just a few loops of XeF_2 silicon etching.

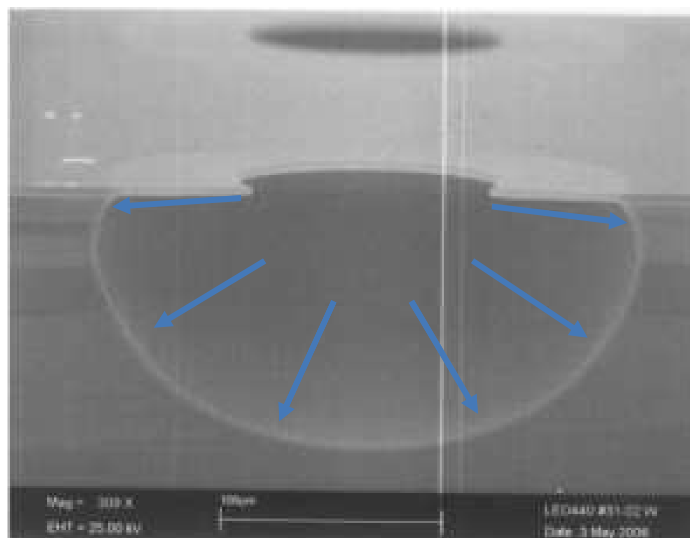


Figure 1.8. Under cut observed after few loops of XeF_2 silicon etching. A circular hole is opened in parylene C layer which functioned as a masking layer.

The amount of the XeF_2 gas that gets inside the etching chamber is fixed between etching loops. The etch rate of XeF_2 is a function of the exposed silicon area. A good way to control the etching process is to unload the sample after a few loops and observe the etching rate under microscope, and then adjust the processing time accordingly.

1.3.3 Deep reactive-ion etching

Another important MEMS fabrication process used in our technology is deep reactive-ion etching (DRIE) [29, 30]. Unlike XeF_2 silicon etching process, DRIE is a highly anisotropic plasma etching process primarily used to sculpture silicon devices. The process can create deep and steep side walled features, typically with very high aspect ratios. This technology has been heavily utilized to develop MEMS devices.

The most common method of DRIE is referred as Bosch process which is a patented process developed by Bosch Inc. Fluorine based chemistries are normally used to etch silicon. However, they all exhibit some degree of isotropy. In order to achieve anisotropic effect and etch nearly vertical walls for high aspect ratio structures, two separate steps are used in Bosch process as demonstrated in Figure 1.9.

First of all, SF_6 plasma etching is performed to isotropically etch exposed the silicon for a short period of time normally less than 10 seconds to prevent the undercut. Then SF6 gas is replaced with C4F8 which will form a Teflon-like substance in plasma and coat the entire chamber and surface. Note that The SF6 does not etch the polymer on the side walls but will attack the coating on the bottom and top surface. The previous etched sidewall is protected from the SF6 isotropic etching. The combination of both the etching step and passivation step makes a very deep vertical structure.

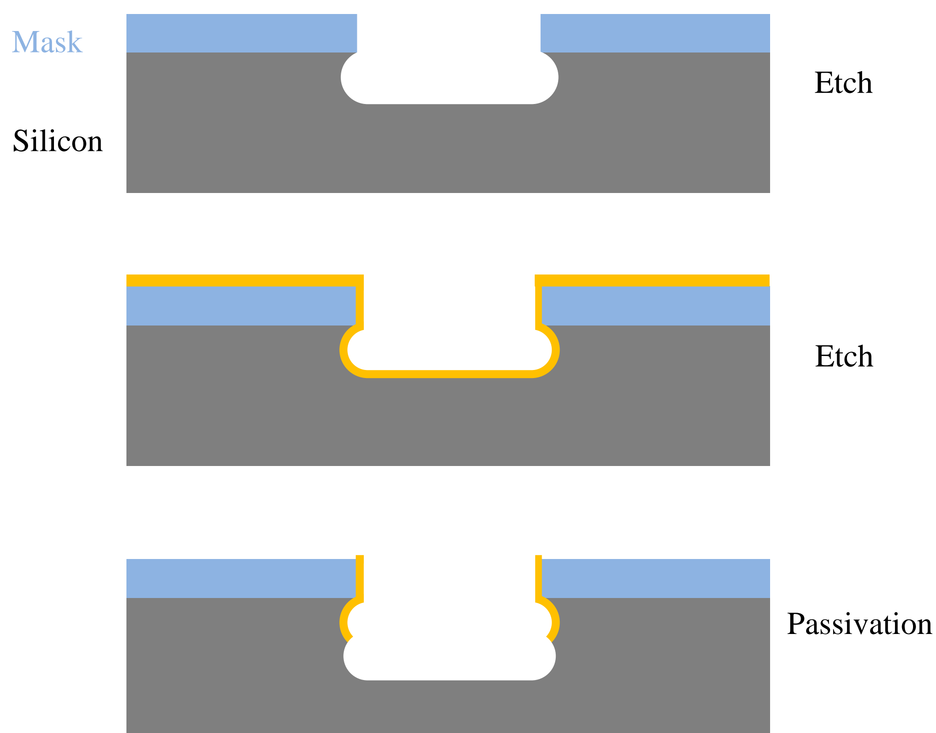


Figure 1.9. A simple demonstration of deep reactive ion etched trench using Bosch process

The figure bellow illustrates that the process will causes ripples or scallops in the side walls due to the nature of the isotropic silicon etching steps utilized.

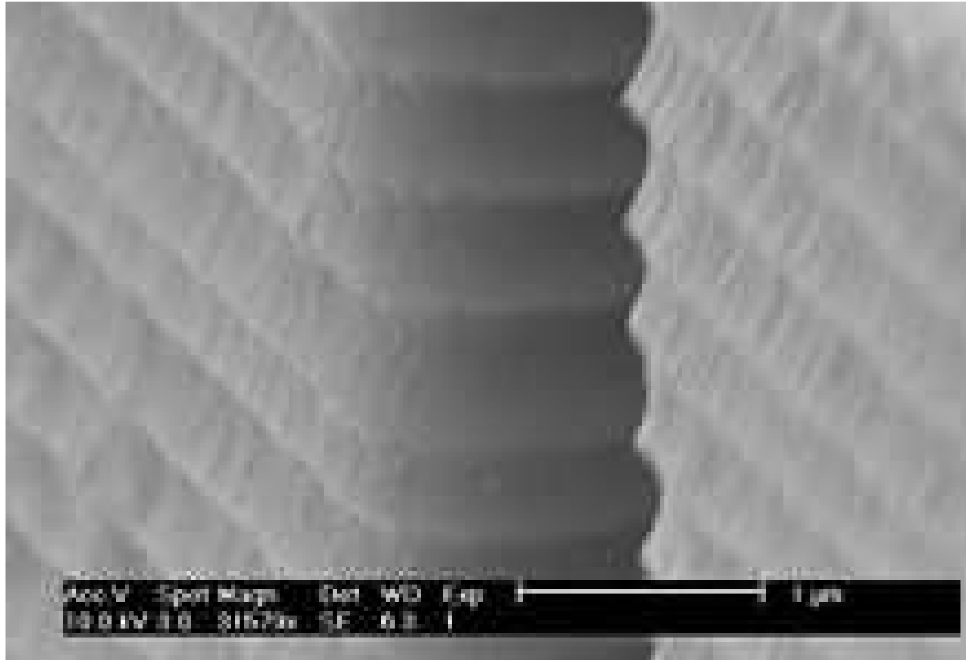


Figure 1.10. Scallops of a silicon structure created using the Bosch process. Source: Wikimedia

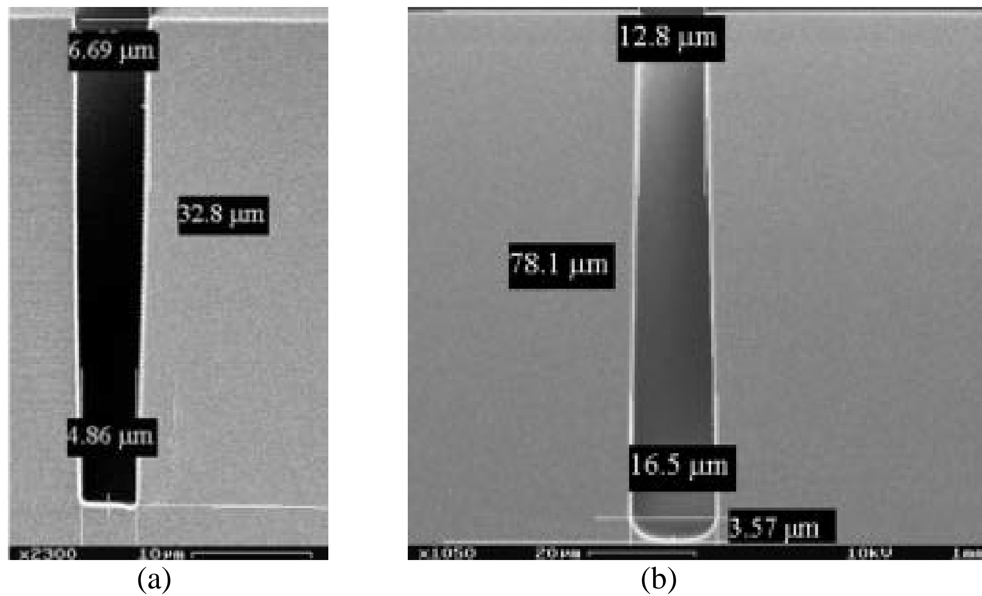


Figure 1.11. Different DRIE recipes to create different slope angles[31]. (a) Trench with a positive slope. (b) Trench with a negative slope

Another important parameter of the DRIE etching is the ratio between etching and passivation steps. By modifying the ratio between those two steps, different side wall angles can be achieved. As demonstrated in Figure 1.11, both positive and negative slopes can be created in the DRIE process. This technique is utilized in the process of developing our out-of-plane parylene microneedle device which is discussed in detail in Chapter 2.

1.4 Dissertation Organization

In Chapter 2, the technology we developed over the past few years is first implemented in the creation of flexible out-of-plane parylene microneedle arrays [32] that can be individually addressed by integrated flexible micro-channels. These devices enable the delivery of chemicals with controlled temporal and spatial patterns and allow us to study neurotransmitter-based retinal prosthesis.

In addition to the fabrication of micro-fluidic components, other great functionalities can be achieved by integrating otherwise sacrificial silicon wafers to be a part of the device. A hybrid silicon-polymer platform for self-locking and self-deploying origami [33] is demonstrated in Chapter 3.

The ability to incorporate high-temperature materials into flexible substrate is also highly desirable. The technology is further explored in Chapter 4 by adopting the conventional SOI-CMOS processes[34]. High performance and high density CMOS circuits can be first fabricated on SOI wafers, and then can be integrated into flexible substrate. Currently, the best electronics are still made by silicon based CMOS technology. Therefore, it is highly desirable to have a flexible skin technology that is compatible with both MEMS and CMOS processes. Flexible p-channel MOSFETs (Metal-Oxide-Semiconductor Field-Effect-Transistors) and high performance silicon strain gauges were successfully fabricated and tested.

In Chapter 5, the development of a smart tube[35] with integrated pressure and flow sensor is presented. The ability to monolithically incorporate electronic components and micro-fluidic structure is highly desirable. This integration is able to bring additional functionality, higher performance, simplified packaging, reduced size/weight and cost to the flexible sensors.

Finally in Chapter 6, some of the additional examples like the smart yarn device and micro pH sensor developed by this technology are presented. A few important future applications are also discussed.

CHAPTER 2. Parylene microtube arrays

2.1 Introduction

The technology discussed in this thesis is first implemented in making flexible parylene microneedle arrays with integrated micro channels for retinal prosthesis study. Many groups have been working toward the development of retinal prosthesis systems that can provide artificial vision to the blind [36-38]. An effective retinal prosthesis would improve the lives of hundreds of thousands of patients with Retinitis Pigmentosa (RP) or millions of blind patients with advanced Age-Related Macular Degeneration (ARMD), depending on its effectiveness. Designs for these prosthetic devices have been based upon the success of electrical stimulation in the cochlear implant. Prostheses based on electrical stimulation of the retina have been under development over the past two-decades as well. In fact, vision is our greatest bandwidth sensory input which requires prostheses to have a neural interface with high spatial and temporal resolution. Testing in acute human studies has demonstrated limited success in providing useful vision. Retinal implant based on electrical stimulation has limitations such as electrode corrosion, water hydrolysis, and generation of toxic radicals due to the large stimulation current. The more naturalistic chemical stimulation is able to effectively address these limitations. This chapter describes the development of parylene microneedle arrays that can be individually addressed by integrated microchannels for neurotransmitter-based retinal prosthesis.

Microneedles can be classified as in-plane or out-of-plane, and solid or hollow. For retinal prosthesis, out-of-plane hollow microneedles are required. A variety of out-of-plane hollow microneedle arrays have already been developed for drug/chemical delivery and other applications. Chun et al. developed SiO_2 microcapillary arrays for the injection of DNA into cells by growing thermal oxide in deep holes etched by DRIE [39]. Hollow silicon microneedles were also developed by Stoeber and Liepmann using a combination of DRIE and isotropic etching [40]. Gardenier et al. developed hollow silicon microneedles with sharp beveled tips using a process combining DRIE, conformal thin film deposition and anisotropic wet etching [41]. In order to address the potential problem of being clogged during the insertion of needles, Griss and Stemme developed hollow out-of-plane silicon microneedles with openings in the shaft instead of at the tip [42]. Kim et al. reported hollow metal microneedle arrays based on backside exposure of SU-8 and electroplating [43]. Hollow metal microneedles have been developed using laser-micromachined polymer mold [44]. Zhu et al. reported another method of fabricating hollow metal microneedles using PMMA molds formed by silica needle template [45]. Hollow microneedles with sharp beveled tips have also been developed using the LIGA technique by taking advantage of its capability of fabricating high-aspect ratio structures [46, 47]. Fluid access to the out-of-plane microneedles is usually made from the back of the wafer by forming a drug reservoir using a wafer bonding method. Consequently, these microneedles are not individually addressable. For retinal prosthesis, however, the microneedles have to be individually addressed due to the requirement of spatial resolution.

Individually addressable out-of -plane microneedle has been developed in our lab as described in the following section. DRIE high aspect ratio silicon etching process is used here to form the molds of the needle arrays. XeF_2 isotropic silicon etching process is employed here to form the accessing microfluidic channels to the needles. Another key process used here is conformal parylene C coating. Parylene C polymer will conformally deposit on the walls of the holes and trenches etched by DRIE and XeF2 forming hollow needles and fluidic channels.

2.2 Design and fabrication

The fabrication was carried out on double-side polished 350µm thick silicon wafers. The thickness of the wafer will determine the overall height of the microneedles. First, a 4 µm parylene C layer was deposited on the front side of wafer using SCS PDS2010 coating system. Due to the nature of parylene C coating, both side of the wafer were coated with parylene C. Back side of the wafer went through O_2 plasma to remove the deposited parylene and expose the silicon layer. Next, through-silicon vias of 35 µm in diameter were formed by DRIE from the backside of wafer as shown in Figure 2.1(a). Note that the recipe of DRIE has been modified to create a slightly slanted side wall to give the vias pointy shape. Those vias will function as a shape mold to make hollow needles. After the backside etching, 200 nm Al layer was evaporated on the frontside after treating the parylene C layer with a mild O_2 plasma to improve the adhesion. This Al layer was then patterned and subsequently used as an O_2 plasma mask to open 8-µm wide windows on the parylene layer as shown in Figure 2.1(b). In the next step, XeF_2, an isotropic gas phase silicon etchant, was used to form

trenches in the silicon substrate through the windows opened in the parylene layer. The trenches created have an undercut of approximate 25 µm from the parylene openings. Note that the trenches were connected with the through-silicon vias as seen in step (c). Then the parylene microchannels were formed and sealed by depositing another 10 µm thick parylene C layer.

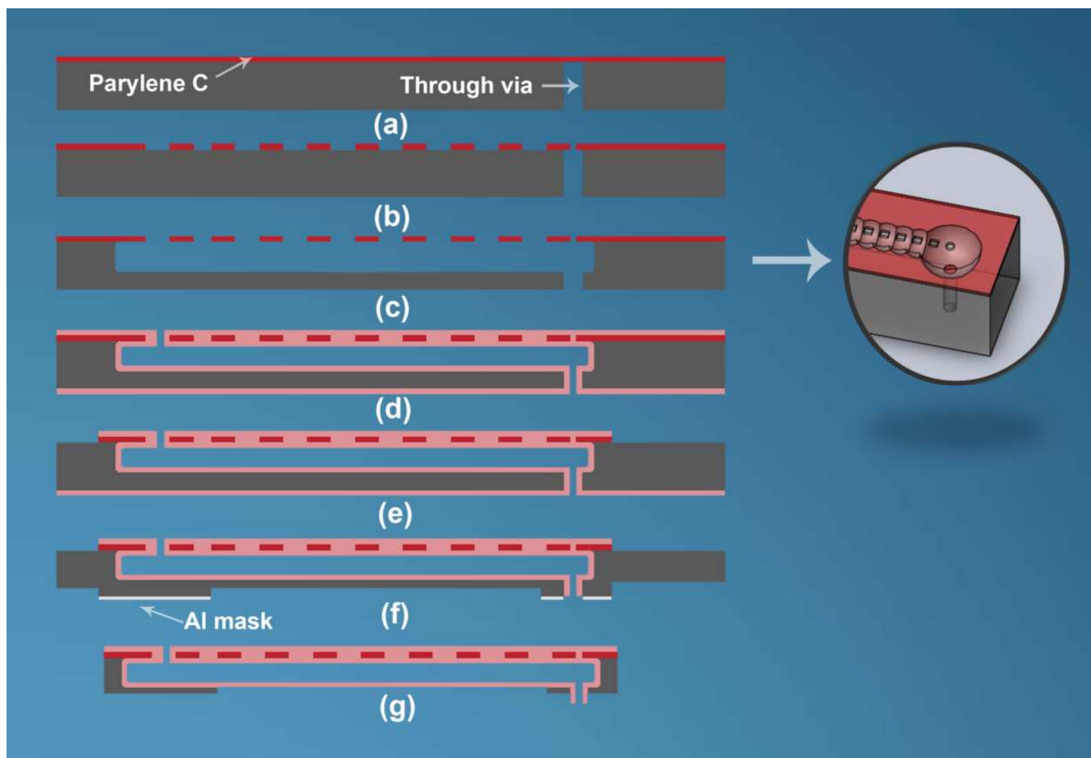


Figure 2.1. The fabrication process of the microneedles with integrated microchannels(a) deposit a parylene C layer; etch through-silicon vias from the backside of the wafer using DRIE; (b) pattern the parylene layer; (c) etch the silicon substrate using XeF_2; (d) coat a thick parylene layer to seal the channel; (e) pattern the frontside parylene; (f) DRIE from the backside of the wafer using Al mask; (g) remove Al mask and continue DRIE to release Parylene cable. Out-of-plane microneedles also emerged.

The parylene deposition is a very conformal process. Therefore, parylene layer was able to deposit on the inside surfaces of the trenches, forming sealed parylene channels [48]. The cross-sectional view of the sealed parylene channel is demonstrated in step (d). Simultaneously, hollow microneedles were formed by the parylene film deposited inside the through-silicon vias (step (c)). The frontside parylene layer is then patterned with a thick photoresist (AZ4620) mask and the parylene is etched via O_2 plasma as shown in step (e). Next, as shown in step (f), DRIE was carried out on the backside using an aluminum mask to selectively thin down the wafer. When the remaining wafer thickness reached about 100 µm, the aluminum mask was stripped away. Then DRIE continued on the backside until the parylene channels were exposed. Simultaneously, because the etch rate of payrlene in DRIE is much slower compared with that of silicon, parylene microneedles embedded in silicon emerged and protruded above the silicon surface. Note that the height of needles protruding above the silicon surface can be increased by additional DRIE etching.

2.3 Results and discussion

2.3.1 Fabricated device

Figure 2.2 (a) shows a fabricated mcironeedle device with flexible parylene cable. The overall length of this device is about 20 mm. It consists of two silicon islands connected by a flexible parylene cable embedded with microchannels. The left silicon island carries 4 slender beams which facilitate the coupling of external tubings to on-chip microchannels. Figure 2.2 (b) shows the SEM image of a microchannel inlet on the tip of the coupling beam. As shown in Figure 2.2(c), the right small silicon island hosts a 2x2 microneedle array. These parylene microneedles are about 80 µm high, and with an outer diameter of 35 µm and an inner diameter of 15 µm. It is worth noting that the height of microneedles can be adjusted by controlling the DRIE loops in step (f) and (g). The in-plane parylene microchannels are also visible in Figure 2.2(c). These channels connect to the out-of-plane microneedles at the bottom surface of the silicon island. Each microneedle can be individually addressed by the inlet ports on the left silicon island.

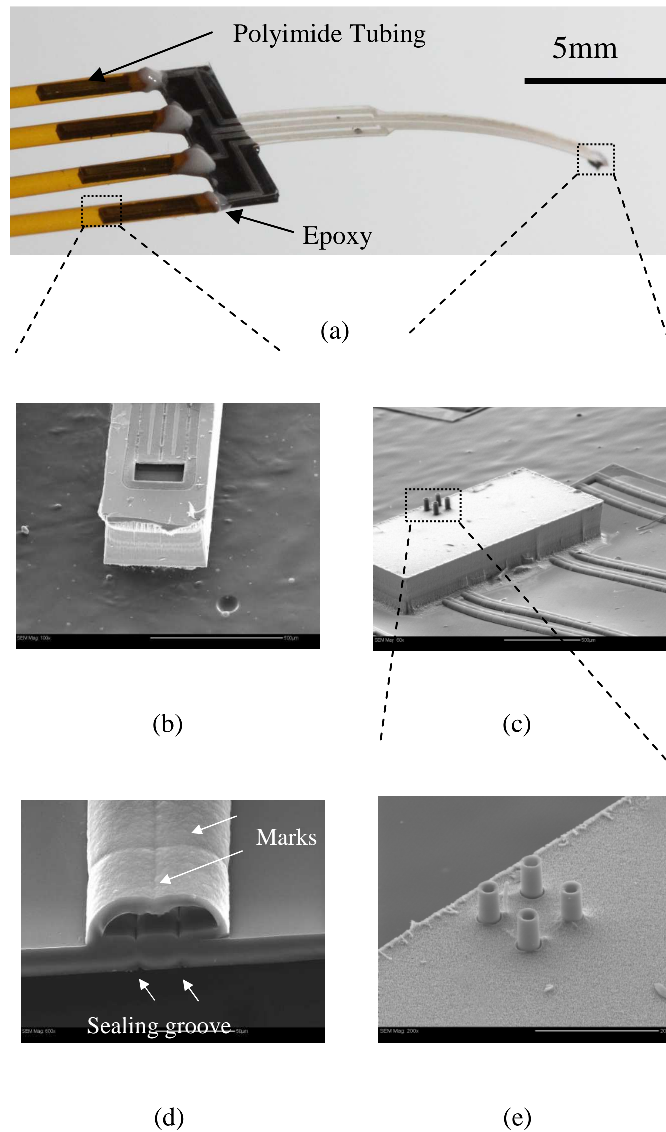
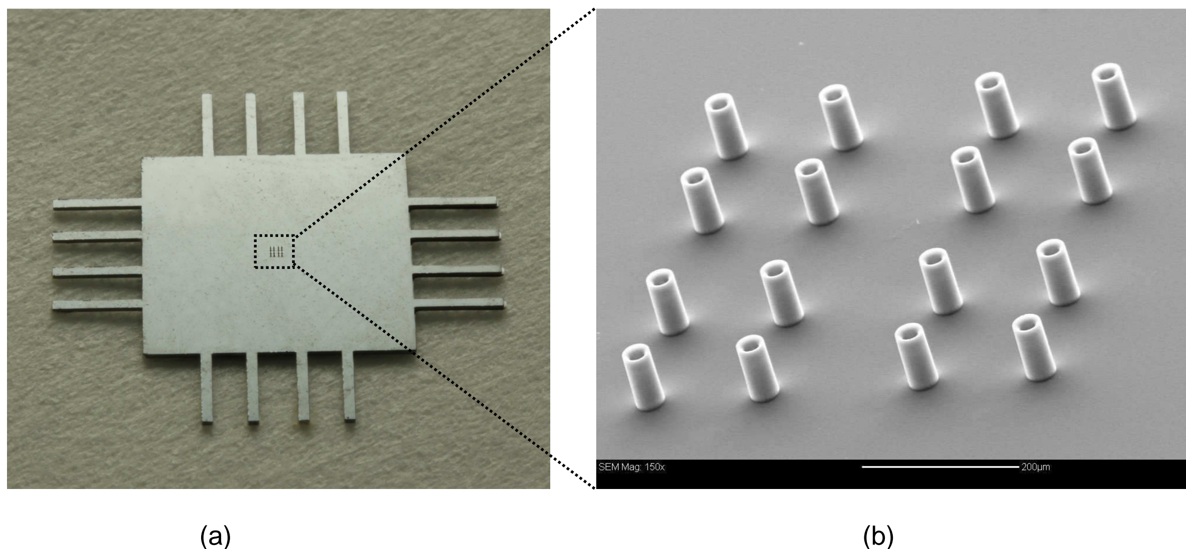


Figure 2.2. (a) A Polyimide Tubing coupled microneedle device with 1.5 cm long flexible parylene cable. Epoxy is used to seal the coupling interface; (b) SEM image of the microchannel inlet port on one coupling beam; (c) SEM image of the small silicon island on the tip of the parylene cable; (d) cross-sectional view of a micrchannel embedded in the parylene cable; (e) magnified view of the 2x2 microneedle array on the small silicon island.

The cross-sectional SEM image of a parylene channel embedded in the parylene cable is shown in Figure 2.2(d). Note that this channel was formed using two columns of openings. The groves resulting from the sealing of the two columns of openings can be clearly observed. The marks due to the isotropic XeF2 etching from adjacent openings can also be seen from the parylene channel walls. This device enables in-vivo animal study. Namely, the small silicon island containing the microneedle array can be implanted into the eye of an animal (e.g., cat or monkey). Neurotransmitters such as glutamate can be ejected to retina through the flexible parylene channels.

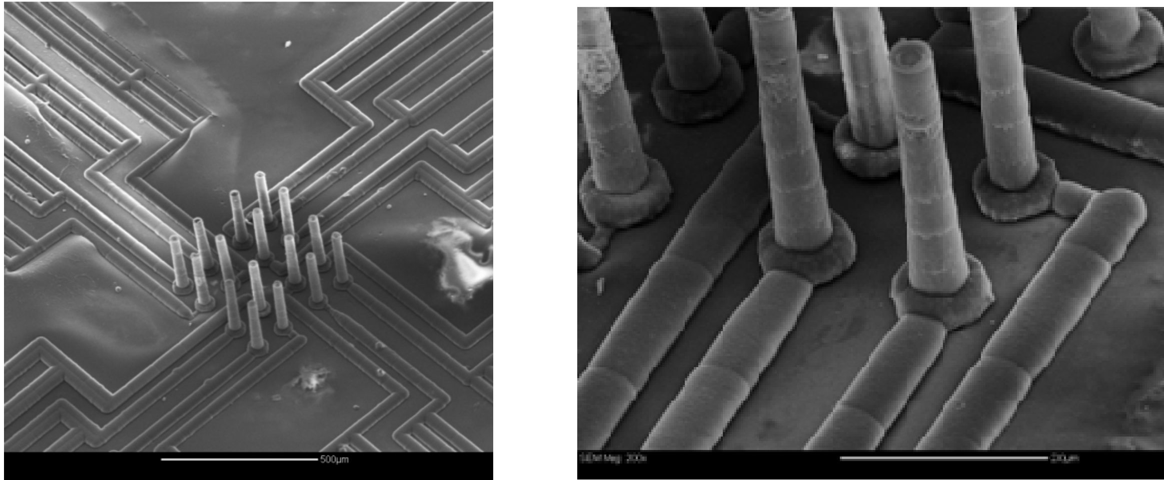
Rigid needle arrays have also been developed for in-vitro retinal stimulation study as seen in Figure 2.3. In order to improve the robustness of our device, rigid devices integrated with 4×4 microneedle arrays have been fabricated. The 4×4 microneedle array locates in the center of the device and covers an area of 500 µm × 500 µm. The dimensions of these needles are same as those on flexible devices. The 4×4 microneedles can be individually addressed by 16 microchannels whose inlets are distributed along the 4 edges of the 1.2 cm × 1.2 cm square silicon chip.



(a) (b)

Figure 2.3. (a) Photograph of a rigid microneedle device. The device carries 16 slender beams, each of which contains one microchannel inlet. (b) SEM image of the 4x4 microneedle array located in the center of the chip, which can be addressable by 16 microchannels.

To investigate the connection between the needles and channels, silicon of the rigid device was completely dissolved by TMAH (Tetramethylammonium hydroxide). It has been demonstrated previously that parylene C is not attacked by TMAH [49]. Figure 2.4 (a) shows the SEM image of the resulting pure parylene device. The tapered shape of microneedles was formed by adjusting the parameter of DRIE during the etching of through-silicon vias. The parylene microchannels previously embedded in the silicon substrate now can be clearly observed. It can also be observed how the out-of-plane parylene microneedles are connected to in-plane parylene microchannels in the magnified view shown in Figure 2.4 (b). Note that XeF_2 at step (c) also attacked through-silicon vias. However, XeF_2 only enlarged the bottom part of the vias as evidenced by the donut structures at the bottom of microneedles shown in Figure 2.4. (b).

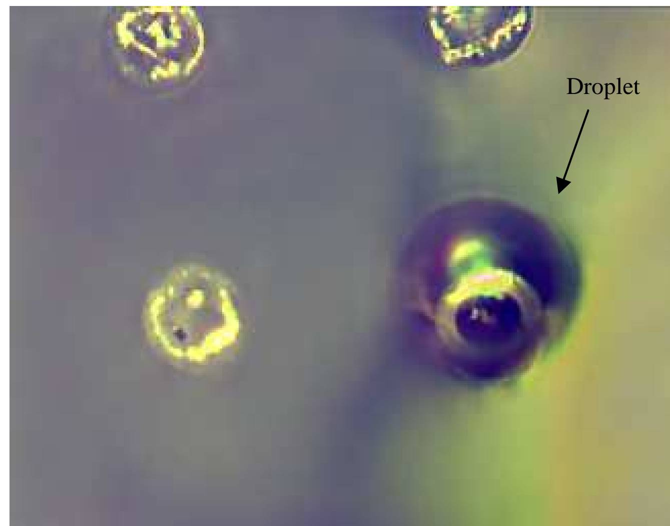


(a) (b)

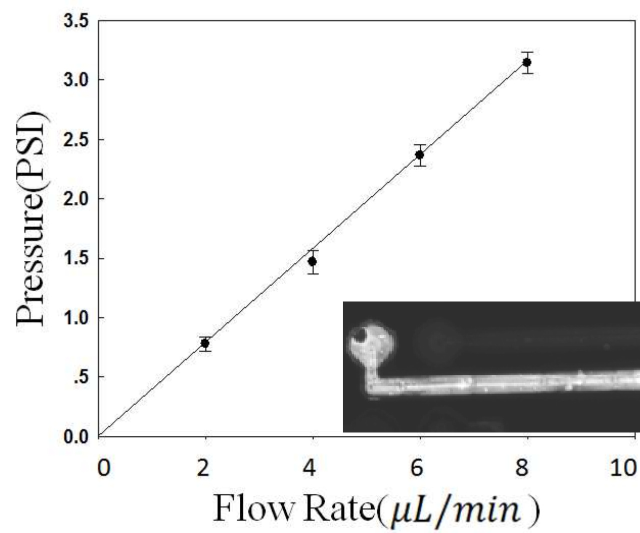
Figure 2.4. (a) SEM image of the pure parylene device by dissolving away silicon. (b) Magnified SEM image of the connection between out-of-plane microneedles and in-plane channels

2.3.2. Fluidic injection test

In order to test the connection between the microneedle and microchannel, fluorescent dyes were injected to one microchannel under a pressure up to 8 psi. The resulting fluorescent image is shown in the inset of Figure 2.5(b). The connection between the circular area, which is the bottom of the microneedle, and the in-plane microchannel can be clearly observed. The flow rate of a microchannel was measured using DI (deionized) water. Polyimide tubing (with an inner diameter of 620 microns) was coupled to the microchannel and then sealed using epoxy as demonstrated in Figure 2.2 (a). A programmable syringe pump and a pressure sensor were used for dispensing liquid and measuring pressure. The flow rate as a function of pressure applied was measured and plotted in Figure 2.5(b). Figure 2.5(a) shows the micrograph of a water droplet emerged from one of the microneedles.



(a)



(b)

Figure 2.5. (a) Optical micrograph showing a water droplet emerging from one microneedle. (b) The measured relationship between the applied pressure and flow rate. The inset is a fluorescent image of the microchannel and donut structure at the bottom of the microneedle (the channel was filled with fluorescent solution).

2.3.3. Preliminary in-vitro retina test

In addition to the fluidic tests done in our lab, the fabricated device was sent to our collaborator Dr. Paul Finlayson for a preliminary in-vitro retina test. A retina tissue was removed from a rat and cultured in a small container for testing. Then our microneedle device was placed in close contact with the retinal tissue along with a small electrode placed next to the needle outlet for neural activity monitoring. As shown in Figure 2.6., chemical based neurotransmitter was delivered to the retinal tissue via a 10 PSI pressure pulse. Retinal tissue's prompt neural response can be clearly observed in the form of electrical spikes.

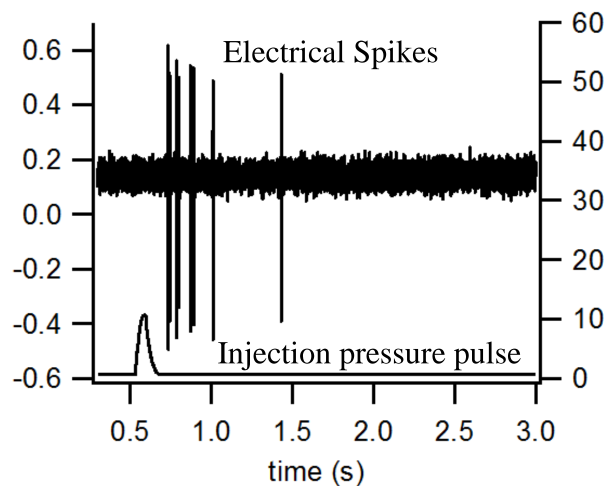


Figure 2.6. Neurotransmitter ejection pressure pulse and the resulting neural spikes. Source: Dr. Finlayson.

2.4 Summary

We demonstrated a novel microfabrication technology of out-of-plane individually addressable microneedle arrays with integrated parylene microchannels. Two different types of devices, rigid devices for in-vitro retina stimulation study and flexible devices integrated with parylene cables for in-vivo study have been developed. The fabrication takes advantage of the conformal coating of parylene. The molds of parylene, including the trenches and through-silicon vias, are formed by XeF_2 etching and DRIE, respectively. Microneedles and microchannels are formed by coating parylene conformally inside the vias and trenches. The functionality of the device has been demonstrated by ejecting water through microneedles. A simple perfusion chamber is being built on the top of the rigid chip for the in-vitro retinal stimulation study. The flexible device allows in-vivo study by implanting the small silicon island containing the microneedle array into the eye of animal (cat or monkey) and injecting neurotransmitters such as glutamate through the flexible parylene channels. Our device enables the delivery of drugs to the desired sites with high spatial resolution.

CHAPTER 3. Hybrid silicon-polymer platform for self-locking and self-deploying origami

3.1Introduction

Origami, traditionally the art of paper folding, has been applied to a variety of engineering applications based on its principle of creating three-dimensional (3D) structures from two-dimensional (2D) sheets through a high degree of folding along the creases. The applications of origami ranges from space exploration (e.g., a foldable telescope lens[50]), to automotive safety (e.g., airbags), and biomedical devices (e.g., heart stent[51]). Materials like shape memory alloy [52] in forms of coil and thick flat plates has been developed to achieve effective bending motion for origami structure. Those origami devices are fabricated by precision machining or laser micromachining [53]. More traditional microfabrication methods such as photolithography have also been used as well [54-56]. The employment of microfabrication will potentially allow the monolithic integration of electronics and MEMS sensors with origami. We developed an origami platform based on microfabricated silicon island arrays. This Silicon-polymer hybrid platform takes the advantages of the excellent rigidity of silicon substrate and combines the flexibility of polymer technology to make flexible devices. Not only it renders the whole device reasonably flexible, it also can be employed to achieve functions like actuation[57]. The technology presented in the previous chapter has been adopted to develop our origami platform. CMOS electronics and MEMS devices can be first fabricated on the silicon wafers [7, 8, 58]. Then low-temperature

processes are carried out to form silicon island arrays and the parylene balloon creases. Such an origami platform, with its capability to integrate CMOS circuits and MEMS sensors, self-lock and self-deploy, will be of great interest to the fabrication of some 3D devices.

The proposed origami device and operation principle of self-locking and self-deployment is schematically illustrated in Figure 3.1. The discrete silicon islands are connected by a parylene balloon at the creases integrated with a metal heater and filled with paraffin wax. Of cause, other materials exhibits phase change at low temperature can be used as well. Paraffin wax was chosen in this experiment. The paraffin wax can be melted by applying electric current to the heater and return to the solid state by turning off the heater. To fold the origami, the wax is melted first, making the balloon flexible. Then the device is folded by external forces. While the device is kept in the folded state, the heater is turned off. The wax solidifies and the origami is locked in the folded state. For the deployment, the heater is turned on to melt the wax to the liquid state. Thus the folded origami can return to its original flat state when the heater is on due to the elastic restoring force of the parylene balloon.

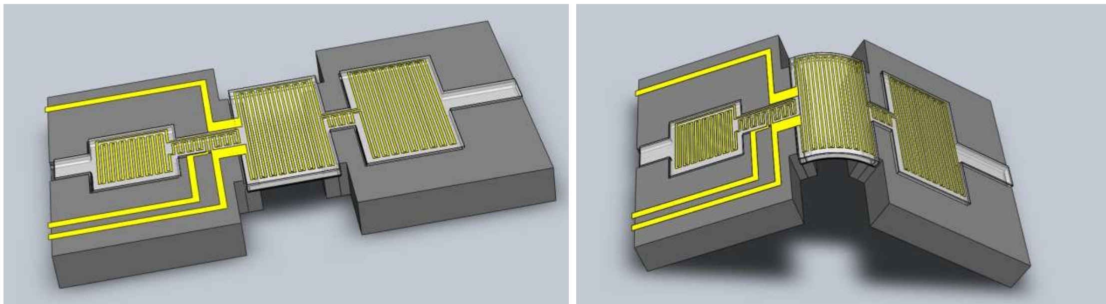


Figure 3.1. Schematic of the silicon island origami with a parylene balloon crease for self-locking and self-deploying functions.

3.2 Design and fabrication

The simplified fabrication is illustrated in Figure 3.2. A 500 μm thick silicon wafer was used for the fabrication. First the wafer was thoroughly cleaned and deposited with 3 μm thick parylene C layer as shown in Figure 3.2(a). Then as show in Figure 3.2(b), a layer of 25/200 nm Ti/Au layer was deposited and patterned to form the micro heaters, bonding pads and corresponding connection traces. Ti was used here to improve the adhesion between parylene C and Au. Next, an array of 8 μm × 20 μm parylene openings was etched via O_2 plasma. In the next step, through the parylene C windows, the silicon substrate was selectively etched by isotropic gas-phase etchant XeF_2 as illustrated in Figure 3.2(c). The depth of the undercut was measured to be 50 μm in this case. Larger depth can be achieved by increasing the exposure time to XeF_2 or using DRIE to deepen the openings before XeF2 etching. These cavities define the shape of parylene balloons. Another thicker layer of parylene C film was conformally deposited on the bottom and side walls of the cavities as shown in Figure 3.2(d). This parylene C layer simultaneously sealed the perforated top parylene C film and encapsulated the metal heaters. Oxygen plasma was then used to pattern the parylene layer to define individual devices and expose the contact pads as shown in Figure 3.2(e). Finally the backside of the wafer were patterned and etched via DRIE to form the silicon islands and release the flexible parylene balloon creases as demonstrated in Figure 3.2(f). Note that the balloons extend into the silicon islands. This actually provides cushions between the metal traces and the rigid edge of silicon islands, significantly reducing stress concentration as demonstrated in our previous work [59].

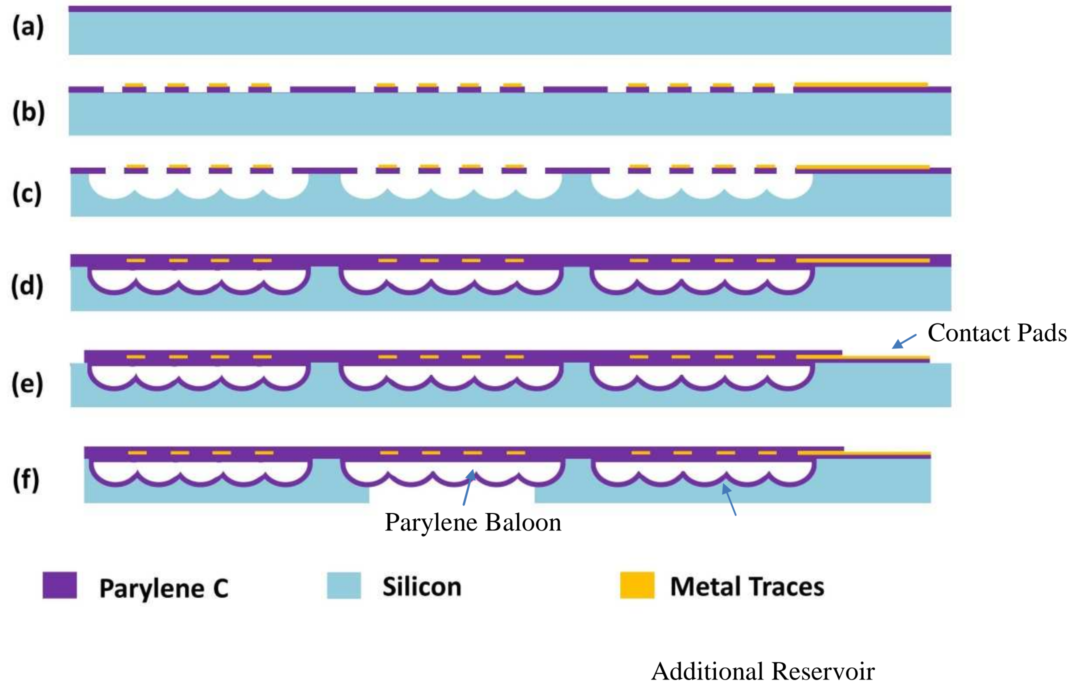
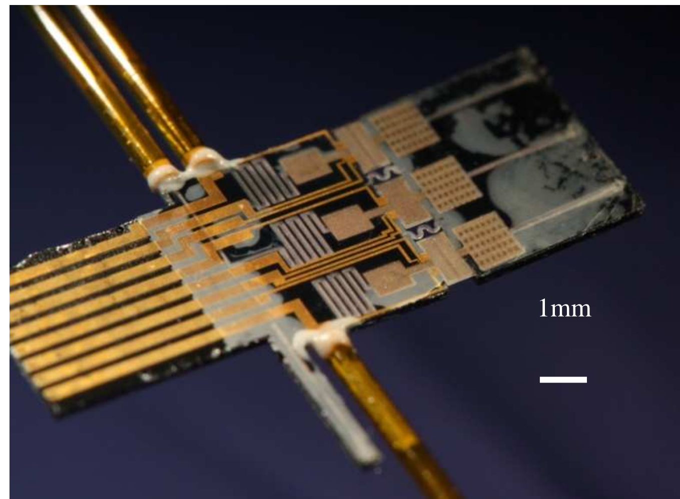
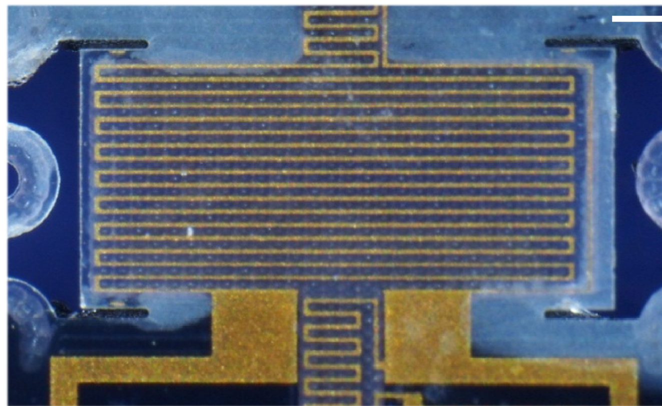


Figure 3.2. Simplified fabrication process of the Origami device.

Figure 3.3(a) is a micrograph of a fabricated device. Since the present work is to demonstrate the self-locking and self-deploying features, the testing device only contains two silicon islands that are connected by 3 parallel parylene balloons. The integrated heaters can be accessed by the bonding pads placed on the left side. Polyimide tubes were glued for the injection of melted wax. The detail of the integrated heater can be observed in Figure 3.3(b). More details of the parylene balloon can be found in the front side and back side SEM images shown in Figure 3.4. Note that the parylene balloon was cut in the middle using a razor blade in order to observe the cross section.

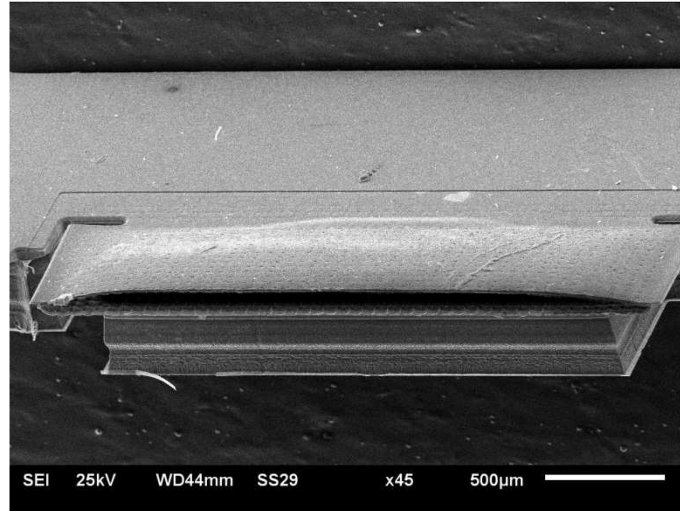


(a)

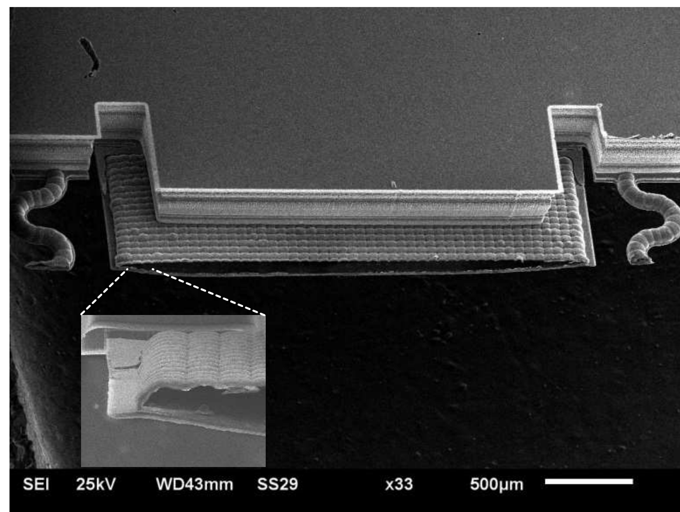


(b)

Figure 3.3. (a) Front side micrograph of an actual fabricated micro hinge structure with three individual Paraffin wax filled parylene balloon hinge; (b) micrograph of the metal heater integrated on the parylene balloon.



(a)



(b)

Figure 3.4. (a) Front side and (b) backside SEM images of a parylene balloon cut to show its cross section. The inset shows the enlarged view of the balloon.

3.3 Device testing and characterization

The balloons need to be filled with paraffin wax for the self-locking and self-deploying functions. This was achieved by placing the whole device on a hotplate with the temperature set at 60 °C, above the melting point of the paraffin wax (327212, Sigma-Aldrich). The melted wax was then simply injected via a syringe. The filling was stopped once excessive wax was observed on the outlet of the channel.

The stiffness of the parylene balloon with melted and solidified wax was measured. The test was carried out by using a needle to push against one silicon island while the other island was clamped. The distance between needle tip and the center of the balloon was about 4.3 mm. A load cell (GS0-10 from Transducer Techniques) was used here to measure the force. The displacement was controlled by a linear actuator with resolution of 5 μm in step size. In order to characterize the effect of a single parylene balloon, the other two balloons place outside were removed during the experiment. Two measurements were carried out when the heater was turned on and off, respectively. The results are plotted in Figure 3.5. It can be observed that the stiffness of the parylene balloon with solid wax is more than four times of the one with melted wax. In order to verify our experimental result, COMSOL Multiphysics 4.3b was used for a finite element simulation. Note that the Young's modulus of the paraffin wax can range from 1 to 4 GPa depending on its composition. In the simulation, in order to have 4 times increase in stiffness, a value of 1.8 GPa was used, which falls within the expected range of Young's modulus of paraffin wax. To have a large stiffness increase, a thicker parylene balloon can be used.

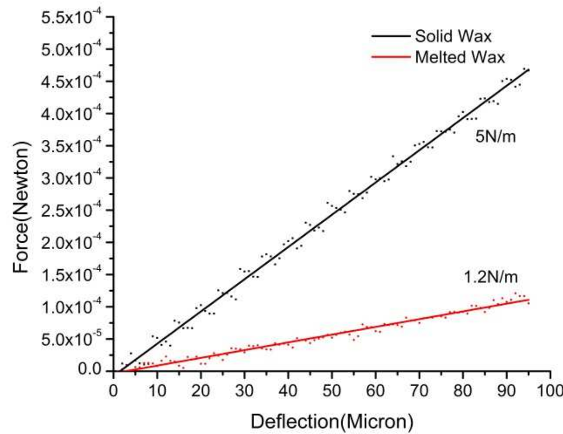


Figure 3.5. Stiffness measurements of the parylene balloon with solid and melted wax.

In order to estimate the temperature when the heater is on, the temperature coefficient of resistance (TCR) of the gold heater was characterized and found to be 0.00321(1/^{o}C). When the heater was turned on by applying a constant voltage, the resistance of the heater was simultaneously monitored. Then the temperature of the heater can be derived based on TCR.

The self-locking and self-deploying tests were carried out under a stereo microscope and recorded by a video camera. First, the heater was turned on and a micromanipulator was used to push the device into the folded state. Then the heater was turned off while the device was kept in the folded state by the micromanipulator. After about 30 seconds, which is longer than the thermal time constant of the system (about 10 seconds), the micromanipulator was removed. Since the wax was solidified, the folding state was locked as shown in the 0 second snap shot of Figure 3.6. Then the heater was turned on, melting the paraffin wax filled

inside the parylene balloon. The device returned to its original position due to the restoring force of the parylene balloon. Figure 3.6 shows a series of snap shots of the device when the heater was turned on at 0 second.

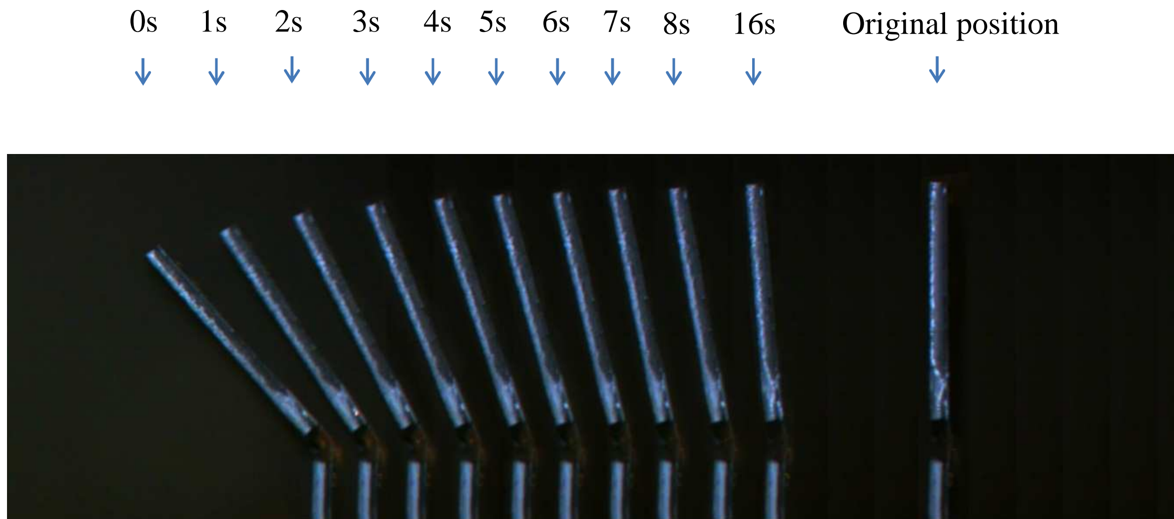


Figure 3.6. Snap shots of the device during a self-deploying process after the heater was turned on at 0 second.

For the present device, the metal heater failed when the bending angle is greater than 45°. This angle can be easily increased by using longer balloons or serpentine shape balloons. The silicon island and parylene balloon structure has another advantage of self-folding by utilizing the volume expansion of wax inside the balloon. In fact, in Fig. 1 there are additional wax reservoirs on the silicon islands. The reservoir (with heater) on the right island is used to provide additional volume expansion during actuating. The small reservoir (with heater) on the left island is actually a venting valve to control the pressure of the crease balloon. This

paper, however, focuses on the self-locking and self-deploying, and the self-folding feature will be implemented in our future work.

3.4 Summery

In conclusion, the self-locking and self-deploying features of an origami platform based on silicon island arrays and parylene balloon have been demonstrated. These features are made possible by wax filled parylene balloon creases. For proof of concept, only metal heaters are integrated to control the solid/liquid phases of the wax. Of cause, high temperature silicon devices like CMOS circuits and advanced MEMS devices can also be directly integrated as well [60] . For example, silicon strain gauge and CMOS control circuits can be directly integrated to provide feedback signal for precision control of the bending angle. The microfabrication process is post-CMOS and post-MEMS compatible, enabling the monolithic integration of electronics and sensors on the origami substrate (i.e., silicon islands). Such an origami platform will be desirable for the fabrication of 3D devices. There are still more work needs to be done in the future. For future development, the design will be optimized to achieve larger bending angles and higher structure rigidity. The self-folding mechanism will also be explored.

CHAPTER 4. SOI-CMOS compatible technology to make flexible electronics

4.1 Introduction

Flexible sensors or electronics are believed to have significant impacts on wearable health monitoring, medical implants and many other applications. In reference [4], a flexible large area position sensitive detector was developed by depositing amorphous silicon on Kapton polyimide substrate. In reference [5], a flexible multichannel sieve electrode for interfacing regenerating peripheral nerves was fabricated on polyimide film by using a silicon wafer as a support for a much better dimension control. Simple MEMS structures on plastic substrates, such as amorphous silicon air-gap resonators, have been demonstrated as well [6]. Simple process flow and low cost are two main advantages of direct fabrication on flexible substrate. Large area flexible sensors or electronics can be fabricated in this way economically. However, since the process temperature is limited due to the flexible substrate, high temperature processes are ruled out and the material properties are not optimized. Moreover, due to this temperature limit, it will be almost impossible to integrate CMOS circuits and many MEMS transducers to the flexible substrate monolithically.

The chapter discusses a simple SOI-CMOS compatible technology which can be used to fabricate flexible electronics without the limitations of the conventional techniques. The most unique part of our technology is the releasing step. All the electronic components of our device, including metal interconnects and discrete silicon islands can be fabricated right

before the final releasing step. The releasing step includes two parylene C film depositions. The first parylene layer is used as a mask to release the devices and a supporting layer for released devices. The second parylene layer functions as an encapsulation layer for the devices. XeF2 isotropic gas phase silicon etchant is used here in the releasing step to etch away the bulk silicon in the handle wafer. Parylene C is selected as the flexible substrate because parylene C deposition is a stress-free conformal process, and parylene C possesses excellent properties such as chemical inertness, biocompatibility, as well as small leakage current and low gas permeability. We have previously utilized XeF2 isotropic etching and parylene conformal deposition to fabricate microchannels and individually-addressable microtubes [32, 61]. In order to demonstrate the concept of the new flexible electronics technology, silicon strain gauges and MOSFETs were first fabricated.

4.2 Design and fabrication

The fabrication process started with a SOI wafer with a 2 μm n-type device layer and a buried oxide (BOX) layer of 0.5 μm. As shown in Figure 4.1 (a), the Si device layer was selectively doped at source and drain regions by boron diffusion (1100 ^{o}C, 15 min). Thermal oxide was used as a diffusion mask here. The resulting boron oxide layer from the diffusion was subsequently etched away by HF (Hydrofluoric Acid). The oxide diffusion mask was removed simultaneously. Next, a 0.5 μm PECVD oxide layer was deposited and patterned as the gate oxide. Then as shown in Figure 4.1(b), Si islands were patterned and the exposed BOX layer were removed sequentially. Aluminum traces and contact pads were then sputtered and patterned as shown in Figure 4.1(c). A sintering step at 450 ^{o}C was carried out to form the

ohmic contact between Al and the silicon (source and drain). It is worth noting that at this step the aluminum traces and pads were in direct contact with the handle silicon substrate, leading to short circuits. However, these short circuits were temporary since the handle silicon layer would be undercut later. It can be observed that the electronic components can be fabricated via standard CMOS process up to this point since there is no temperature limit of fabrication process.

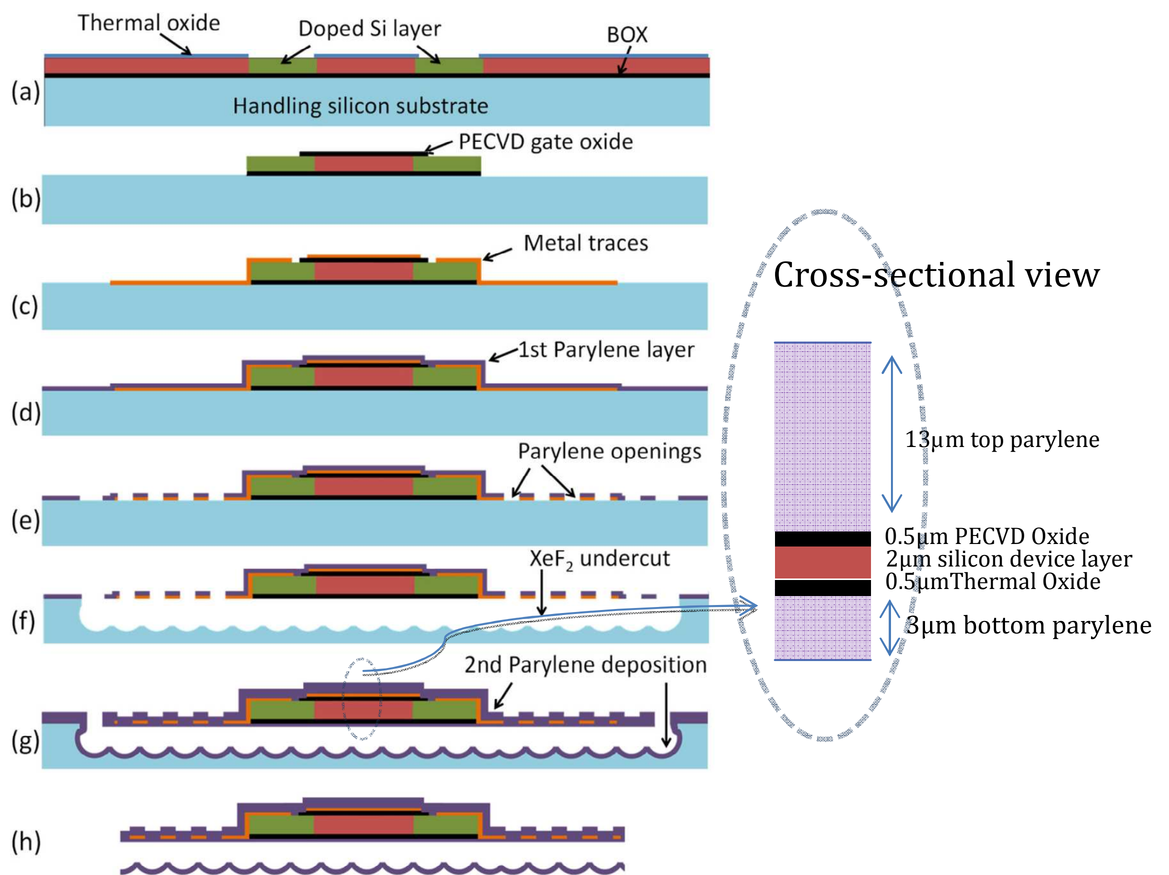


Figure 4.1. Simplified process flow: (a) Boron diffusion; (b) patterning the device layer and removing the exposed BOX layer; (c) Al deposition and patterning to form traces and pads; (d) 1st 3 µm parylene deposition; (e) patterning the parylene openings and etching away underneath metal traces; (f) XeF_2 etching to release the devices; (g) 2nd 10 µm parylene deposition; (h) patterning the parylene layer and releasing the device.

Next, a few more steps were performed to transfer devices from Si substrate into flexible parylene C substrate. First, a 3 lm thick parylene C layer was deposited as illustrated in Figure 4.1(d). Next at step (e), arrays of small windows (8 µm x 25 µm) 60 µm apart were opened in this parylene layer using O2 plasma. Note that these openings were also formed on all the wide metal traces/pads and silicon islands. Then at step (f), XeF2, an isotropic gas phase silicon etchant, was used to completely undercut the silicon underneath through the windows formed in the previous step. Note that silicon islands, including MOSFETs and strain gauges, were protected by the parylene C on the top and BOX on the bottom. At this point both functional silicon device layer and metal traces/pads were supported by a free-standing perforated parylene C membrane. Next, a second parylene C layer (10 µm) was conformally deposited to encapsulate the devices and metal traces/pads and simultaneously seal the etching windows as shown in Figure 4.1(g). Oxygen plasma was then used to open bonding pads on the front side and cut the outline of the flexible device. Finally the flexible device can be simply peeled off from the Si substrate. Note that there are two physically separated parylene C layers after step (h). Depending on the application, we can choose to either keep or remove the scalloped bottom parylene C layer by simply modifying the final parylene etching mask. Because these two parylene C layers formed an enclosed space by keeping the bottom parylene layer, we could easily integrate functional microchannels, microtubes, or diaphragms in the system. Here for the flexible MOS- FETs and strain gauges, the bottom parylene layer was removed.

A fabricated flexible device is shown in Figure 4.2 which is handled by a pair of tweezers. The flexibility of the device can be clearly observed. In order to facilitate the subsequent testing and calibration, contact pads (large square pads seen in the picture) are made fairly large about 1mm by 1mm in size. All the devices and metal traces (except contact pads) are encapsulated by con- formally coated transparent parylene C films.

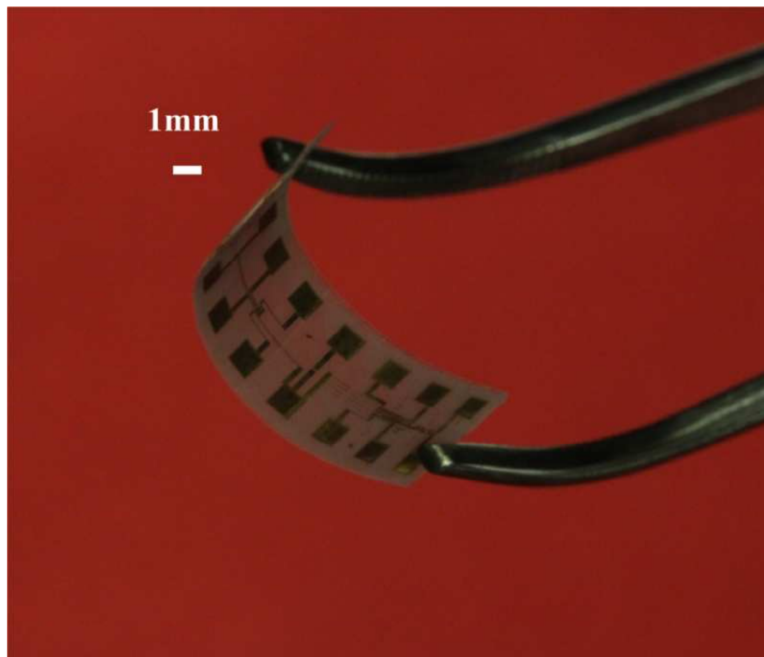


Figure 4.2. A bent flexible device held by a pair of tweezers

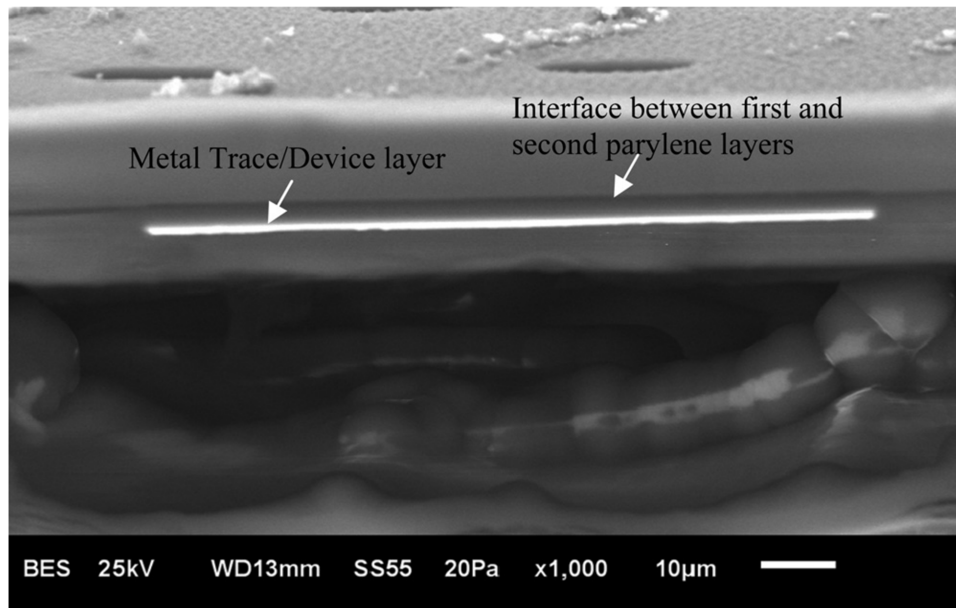


Figure 4.3. Cross sectional SEM image of the flexible device

Figure 4.3 shows the cross section of the flexible device. The relative position of the device layer in the parylene C film can be observed. As described in the process flow, there was an initial parylene film (1st parylene C layer) above the device layer. During step (g), the 2nd parylene C layer was deposited to reseal etching holes. The 2nd parylene layer was conformally deposited on the bottom side through etching holes as well and simultaneously coating the sides of the 1st parylene layer. 2nd parylene layer will stop coating the bottom side once the holes have been sealed. It estimated that around 4 μm thick parylene will be deposited on the bottom side and 10 μm parylene will be deposited on top side. Therefore, the device layer was below the middle plane of the parylene C layer. The relative position can be

easily adjusted by thinning down either top or bottom side of the parylene C film via O2 plasma after the device has been released from the substrate.

4.2.1 Fabricated MOSFETs

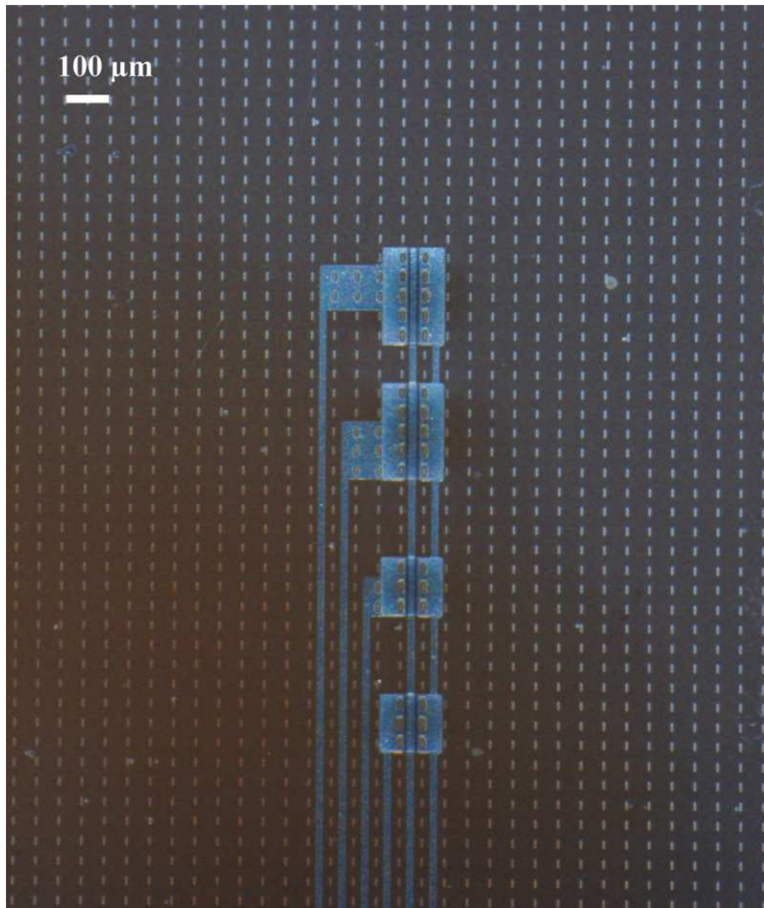


Figure 4.4. Optical micrograph of four MOSFETs with different channel widths.

Figure 4.4 is the optical micrograph showing details of four MOSFETs with different channel widths. The 2-D arrays of re-sealed etching holes can be clearly observed as well (which appears to be dotted lines). Note that the etching holes were also formed on the silicon

islands and wide metal traces. The location of the etching holes are specifically designed so that these holes facilitated the undercutting of silicon underneath without affecting the functionality of the devices.

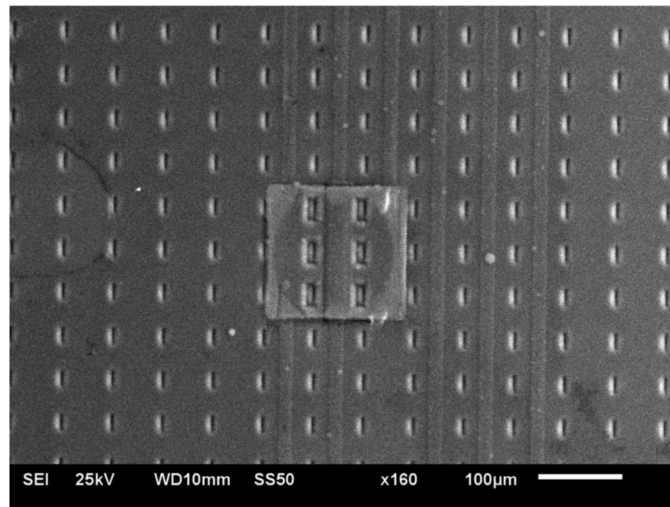


Figure 4.5. SEM image of a MOSFET integrated on the flexible substrate.

Figure 4.5 is a SEM image of a single MOSFET fabricated on the parylene flexible substrate. Note that the MOSFET and metal traces are sandwiched between parylene thin films. They can be observed in SEM because of the height variation. The sealed etching holes can be observed with more details in this SEM image. Note that the original width of the etching holes was 8 µm wide. The second 10 µm parylene C deposition was more than enough to completely seal these holes to make a complete film and enhanced the mechanical strength of the flexible substrate.

The fabricated flexible MOSFETs have been preliminarily characterized. Figure 4.6 (a) plots the Isd-Vsd curves of one PMOS device with different Vsg. It can be observed that the threshold voltage Vth of this PMOS is less than -5 V. Figure 4.6 (b) illustrates the change of the Isd-Vsd curves when the de- vice was bent with a fixed Vsg of 15 V. The increased current is due to the increase of charge carrier mobility when the MOSFET channel is strained. The strain sensitivity is mainly because the MOSFET is not at the neutral plane of the substrate. The MOSFET can actually be used as a sensitive flexible strain gauge in this case. It will become even more sensitive if we selectively thin down the bottom side of the parylene C film and thus move the device layer further away from the neutral plane. For other applications, the device layer can be positioned right on the neutral plane to minimize strains by reducing the thickness of the top parylene C layer via O2 plasma.

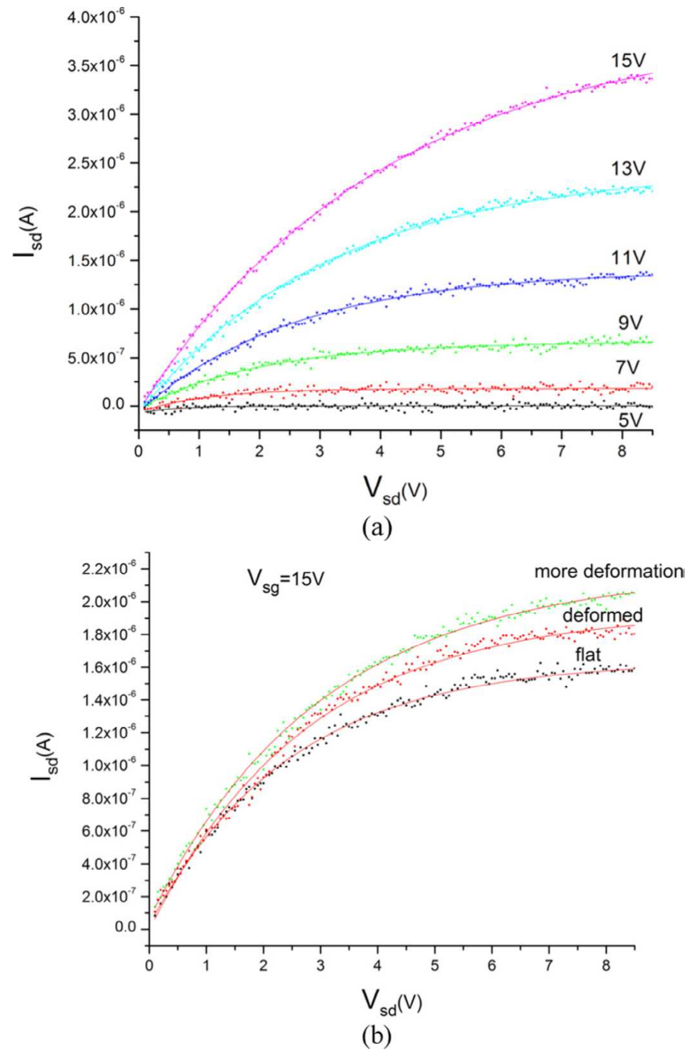


Figure 4.6. (a) Isd-Vsd curves of one PMOS device with different Vsg; (b) shift of Isd-Vsd curves of one PMOS device when the device was deformed (Vsg is fixed at 15V)

4.2.2 Fabricated Strain Gauges

The magnified view of two perpendicular strain gauges can be found in Figure 4.7. In this figure, both narrow metal traces and wide perforated metal traces can be observed. Note that metal traces or device narrower than 60 μm (the spacing between rows of etching holes) can be designed to be a complete device without etching holes embedded inside the feature.

Wide metal traces and devices wider than 60 μm will have etching holes embedded inside the feature. Wider metal traces make our device more durable and they are also required for contact pads. Note that arrays of small dimples, which are resealed parylene C windows after second parylene C deposition, can be observed on the surface as shown in Figure 4.7

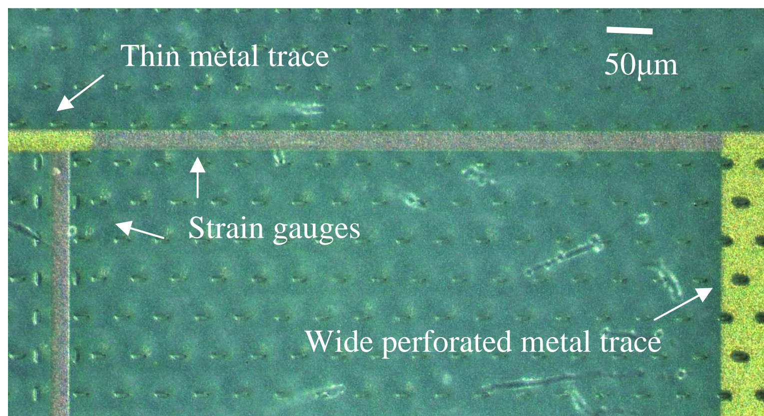


Figure 4.7. Optical micrograph of two perpendicular strain gauges.

In order to test the performance of the flexible strain gauge, conductive epoxy was used to connect the testing wires to the exposed metal contact pads. A simple experiment was carried out by pushing the flexible device in the longitudinal direction (to induce buckling) as illustrated in

Figure **4.8**. The displacement was controlled using a precision micro-manipulator. The resistance change of the strain gauge as a function of displacement was recorded. The experiments were repeated 10 times and the average data points with standard deviation are plotted in Figure 4.9. If the gauge factor is 10 (for heavily doped n-type silicon), the strain experienced by the strain gauge is 0.387% for 1mm displacement in the experiment (corresponding to a bending radius of ~3 mm). This is actually a sensitive flexible strain

gauge because the silicon device layer is not at the neutral plane. It will become even more sensitive if we selectively thin down the bottom side of the parylene C film and thus move the device layer further away from the neutral plane. For other applications, the device layer can be positioned right on the neutral plane to minimize strains by reducing the thickness of the top parylene C layer via O2 plasma.

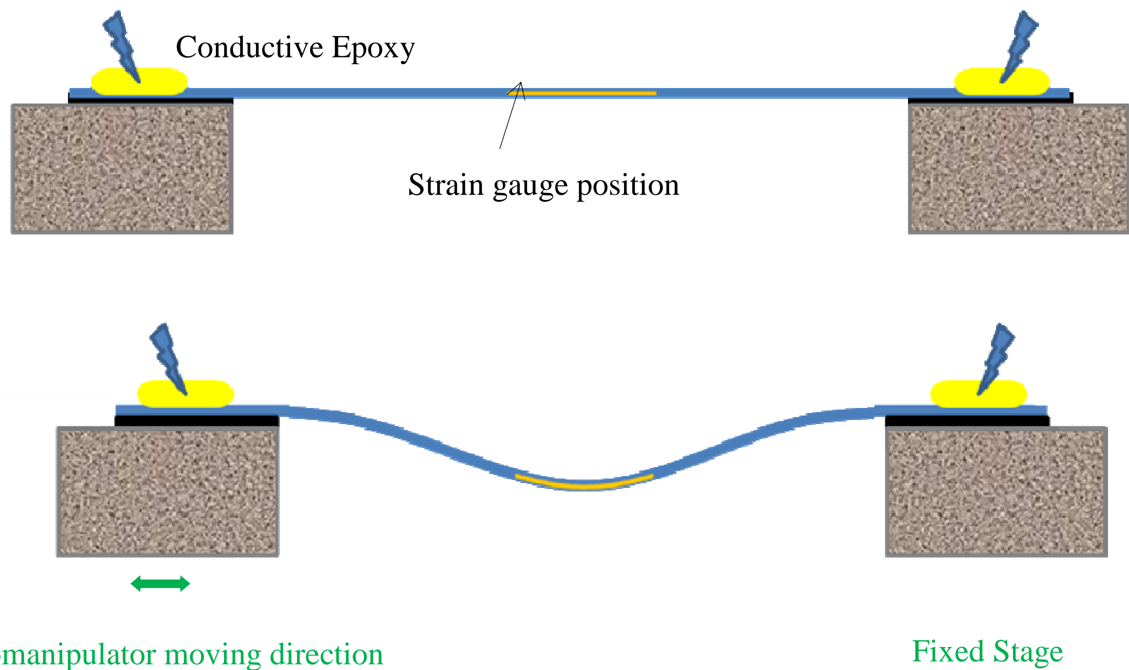


Figure 4.8. Testing setup with two moving stages to control the displacement.

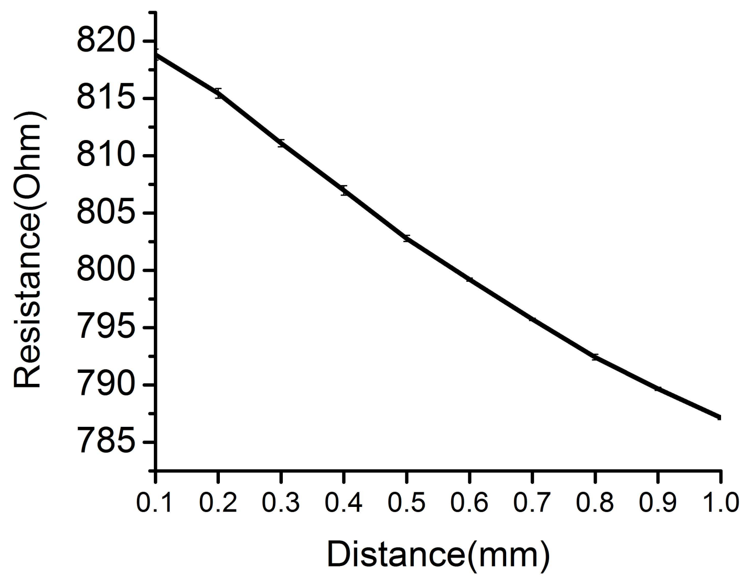


Figure 4.9. A simple experiment records the resistance change while the device bends when we applied the displacement in the longitudinal direction**.**

4.3 Summary

In conclusion, a simple SOI-CMOS compatible flexible electronics technology has been demonstrated. This technology has advantages of being simple and compatible with commercial SOI-CMOS processes. High-density and high-performance CMOS circuits can be first fabricated using SOI foundry (by slight modifying the layout rules) and readily transferred to flexible substrates. The post-CMOS process only requires two masks, one is used to form etching holes and the other to open the metal pads and shape the outline. In addition, the lamination of the electronics between parylene films offers protection against moistures from the environment. By eliminating the transfer printing process, the device density and yield can be increased significantly. Moreover, the electronics or sensors can be positioned at either neutral plane or any other selected planes by simply modifying the thickness of the top or bottom parylene C via O2 plasma, and therefore allowing more design flexibility. It is also worth noting that this technology is post-MEMS compatible in some sense and thus allows the integration of various MEMS sensors and microfluidic components on the flexible substrate.

CHAPTER 5. A parylene smart tube technology compatible with high-temperature solid-state materials

5.1 Introduction

The ability of our technology to make fluidic devices and integrate CMOS elements has been demonstrated in the previous chapters. The ability to monolithically incorporate electronic components and micro-fluidic structure is highly desirable. This chapter will discuss a smart tube device enabled by our technology.

Smart tube devices could be used in various biological and medical applications. Li et al. developed a lab-on-a-tube device targeting neuromonitoring of patients with traumatic brain injury [62]. Smart catheter flow sensor for real-time continuous cerebral blood flow monitoring has been developed as well [63]. Their devices were developed by spirally rolling a flat cable integrated with multiple sensors. Smart tube or cannula devices can be used for intraocular pressure measurement or ocular drug delivery [64, 65]. Smart tube device can also be used for 3D cell culture or tissue engineering, to measure the local parameters such as pressure, flow, pH, O2 concentration, voltage and so on [66, 67]. Neural prosthesis can be benefited from smart tubes as well, for the capability of measuring local physicochemical, mechanical and biological microenvironments [68-70]. In this chapter, we present the development of a parylene smart tube technology compatible with high-temperature solid-state materials. Namely, circuits and sensors can be first fabricated on silicon wafers using

mainstream CMOS and MEMS processes without the temperature limitation. For the purpose of proof of concept, a pressure sensor and a flow sensor are integrated.

5.2 Design and fabrication

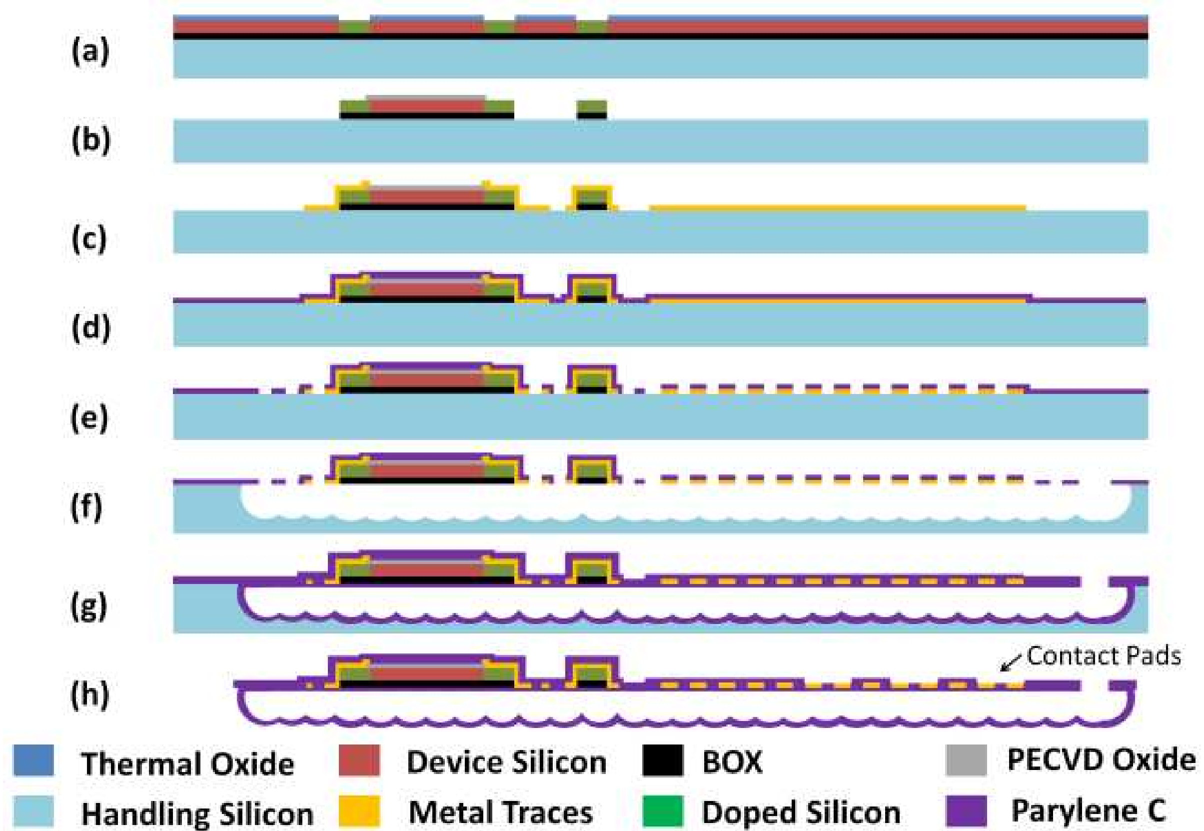


Figure 5.1. Simplified process flow: (a) Boron diffusion; (b) patterning the Si island on device layer and removing the exposed BOX layer; (c) Al deposition and patterning to form traces and pads;(d) 1st 3 µm parylene deposition; (e) patterning the parylene openings and etching away underneath metal traces; (f) XeF_2 etching to release the devices; (g) 2nd 10 µm parylene deposition; (h) patterning the parylene layer and releasing the device.

The fabrication was carried out on a SOI wafer with 2 µm n-type device layer of resistance around 1-10 ohm-cm. First, the Si device layer was selectively doped with a

diffusion mask grown and patterned prior to the doping as seen in Figure 5.1 (a). Next, Si device layer was patterned and the exposed BOX layer was also removed subsequently. Note that two silicon devices were placed perpendicular to each for better illustration of our process even though the actual fabricated devices were placed in the same direction. Then as shown in Figure 5.1 (b), a 0.5 μm PECVD oxide layer was deposited and patterned to cover both top and side wall of the Si devices except the doped regions. Aluminum (Al) traces was then sputtered and patterned to make electrical contact to the doped Si regions as shown in Figure 5.1(c). It can be observed that the electronic components and sensors can be fabricated via standard CMOS and MEMS processes up to this point since there is no temperature limit of fabrication process. Next, parylene C layer was deposited and then patterned with arrays of small windows (8 μm x 25 μm) 60 μm apart as demonstrated in step (d) and (e). Note that these openings were also formed on metal traces wider than 60 μm such as contact pads. The exposed Al traces were also etched away in this step. Then at step (f), XeF2, an isotropic gas phased silicon etchant, was used to undercut the silicon to form continuous trenches. Note that the silicon devices were not attacked since they were protected by both parylene C on the top and BOX on the bottom. At this point the devices were supported by a free-standing perforated parylene membrane. Then a second parylene C layer (10 μm) was conformally deposited to encapsulate the silicon island and metal traces/pads as shown in step (g). The parylene windows patterned previously were also sealed at this point and formed a complete parylene membrane. Finally the outline of the smart tubing device can be defined and all the devices can be simply peeled off from the substrate.

5.3 Results and discussion

Figure 5.2 (a) and (b) are optical images and SEM picture of a fabricated smart tube device. The whole device is made out of conformal coated parylene C which makes the device highly transparent. The pressure sensor is located on the larger square diaphragm, composed of four silicon piezoresistors. The flow sensor, which is based on thermal principle and is made of a silicon heater [71, 72], is placed further down to the neck region of the tube. The 2D arrays of white dots are the sealed etching holes on parylene. Total of three metal traces were used to access both sensors. The backside and cross-sectional SEM image of the device is illustrated in Figure 5.3. The scallop-shape is the result of isotropic etching of XeF2.

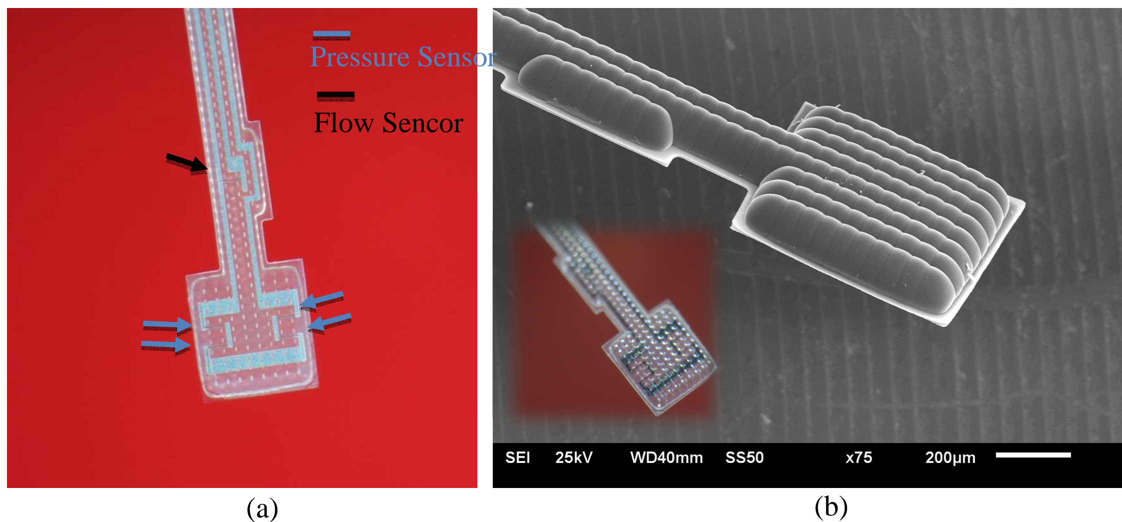


Figure 5.2. (a)Optical image of the fabricated device including both pressure sensor and flow sensor; (b) back side and SEM images of the device; the inset is the optical image of the same device where the front side sensors can be observed through transparent parylene bottom layer.

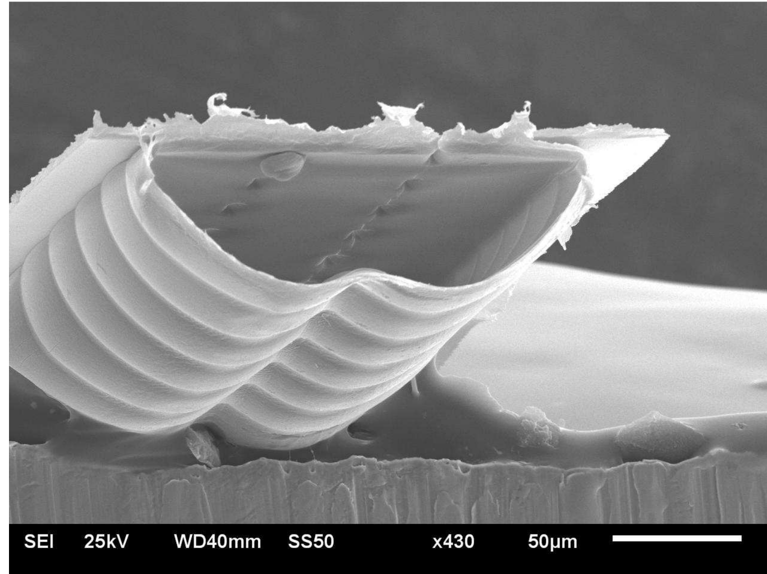


Figure 5.3. Cross-section SEM images of the tail section of the device

To better understand the operation of our pressure sensor, a white-light interferometror (ContourGT InMotion 3D Optical Microscope, Bruker Nano Inc) was used to measure the deformation of the square diaphragm under pressure as shown in Figure 5.4. The deformation of the diaphragm can be clearly observed as the tube undergoes 55kPa air pressure generated by a syringe pump. The maximum deflection of the diaphragm as a function of the differential pressure is plotted in Figure 5.5. The data shows that the deformation of the diaphragm becomes nonlinear when the pressure is large.

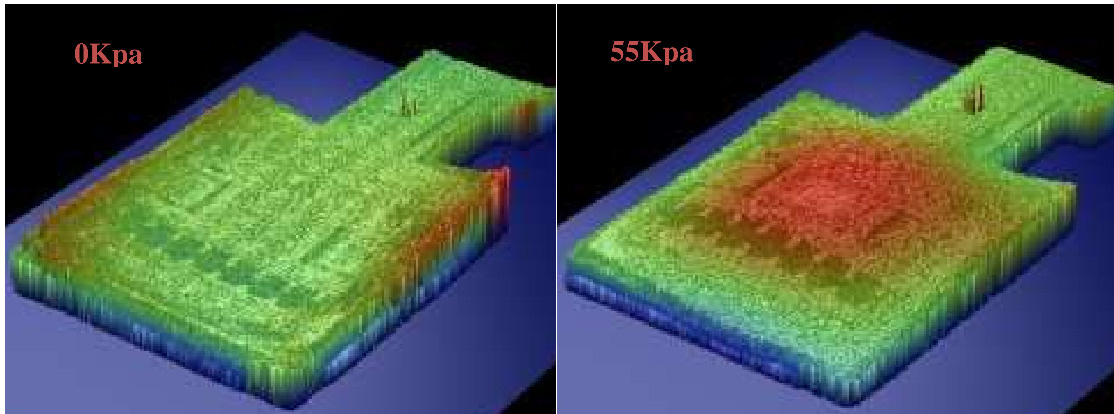


Figure 5.4. Surface profile of the diaphragm without (left) and with (right) differential pressure applied.

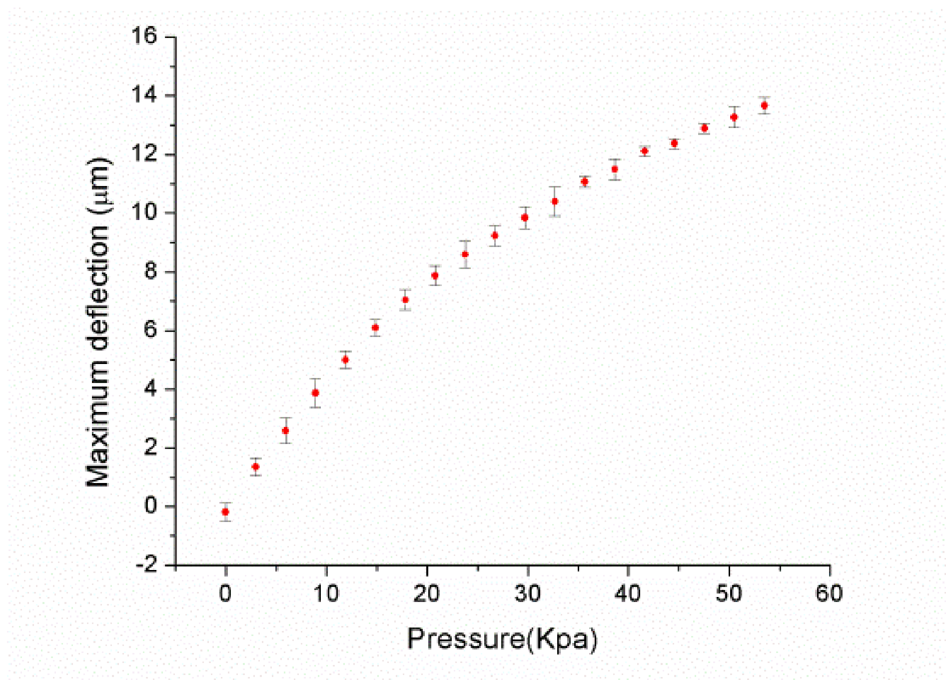


Figure 5.5. Cross-sectional surface profiles of the pressure sensor diaphragm under different pressures.

In order to calibrate the pressure sensor and flow sensor, a testing apparatus was constructed to perform the testing of the integrated pressure and flow sensors on the parylene tube in liquid environment. As schematically illustrated in Figure 5.6, the smart tube device was sealed into a chamber made out of glass slides. This chamber is accessed by two 22 gauge polyimide tubings. Note that the tip of our smart tube where sensors are located was placed inside the inlet polyimide tubing and the tail section of our smart tube was placed outside of the chamber for electrical access. Three probes were used to access the electrical contact pads located on the tail section of the smart tube. In addition, the accessing port at the tail end of the smart tube was not sealed which makes the bottom side of the pressure sensor diaphragm exposed to atmosphere.

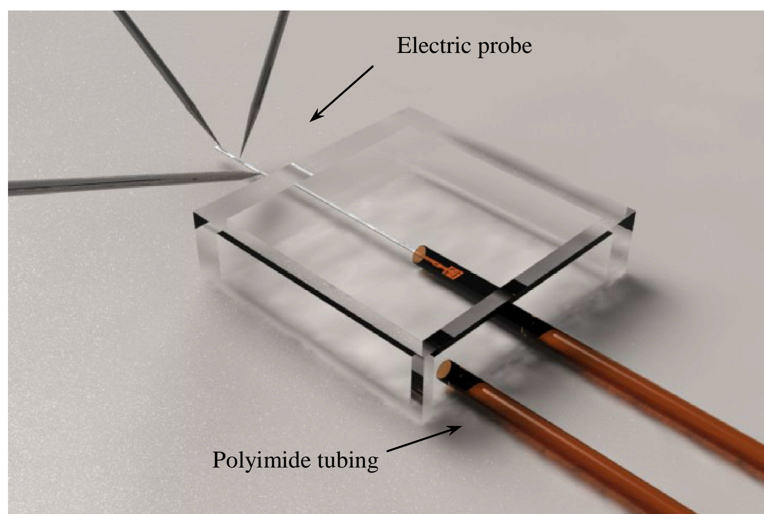


Figure 5.6. Schematics of our testing setup. The sensing tip of the smart tube device was placed inside the inlet polyimide tubing which enables us to characterize the flow sensor.

Both piezoresistors and heaters are made of silicon and are sensitive to temperature. The resistance of the sensing resistor as a function of temperature was measured. Based on the data, the temperature coefficient of resistance (TCR) was calculated to be 0.0028 (oC-1).

The pressure characterization was carried out by filling the chamber with liquid solution, IPA in this case, into the chamber via a syringe pump. A pressure sensor was also coupled in the system to measure the chamber pressure. Instead of pressurizing the smart tube device, negative chamber pressure was generated by withdrawing liquid inside the sealed testing chamber using a syringe pump from the outlet polyimide tubing. A differential pressure was generated across the diaphragm. The resistance change of the piezoresistors was measured when the differential pressure increased from zero and returned to zero, as shown in Figure 5.7. Some hysteresis was observed due to the fact that our sensor was made out of polymer material. It can be observed that the hysteresis was smaller at lower operation pressure range. When the pressure range is 0-15 KPa, the hysteresis is less than 3.8% of the full range. Nonlinearity was also observed, which is consistent with the surface displacement data measured by white light interferometer. The pressure sensitivity of the integrated flow sensor was also measured. It is observed that flow sensor exhibits a very low sensitivity to the pressure change. Therefore the pressure variation will have minimum impact on the operation of the flow sensor.

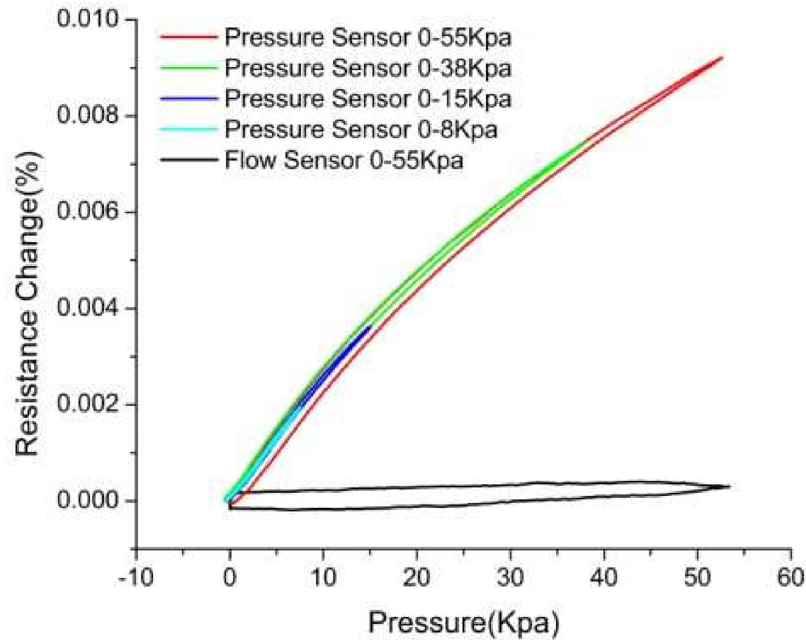


Figure 5.7. Measured relationship between differential pressure applied and resistance change at room temperature. Colored lines are measured from pressure sensor at different pressure settings which shows the hysteresis of the system. Data in black indicates the resistance change of the flow sensor under pressure.

The flow sensor was first characterized by I-V curves, from which temperature changes versus power consumption relationship was obtained. A temperature sensitivity of 0.58 ^{o}C /mW was observed. Our sensor was encapsulated by parylene C which has a melting temperature of around 290 ^{o}C. A fixed bias voltage (2.5V in this case) was applied to the sensor and current passing through the resistor was recorded when different flow rate was generated by syringe pump. Based on the TCR value, the working temperature of the thermal resistor was estimated to be around 60 ^{o}C which is a safe value for both parylene and liquid content we were measuring. The measured power consumption of the flow sensor as a

function of flow rate is shown in Figure 5.8. Note that the thermal convection around the sensor is a function of the flow rate. More heat will be dissipated at higher flow rate which in turn reduce the temperature of the thermal resistor. Consequently the resistance decreases and the power consumption increases with constant voltage mode. It is observed that the flow sensor exhibited relative large fluctuation. This is mainly because the device was suspended in the liquid and became instable when flow rate is not zero.

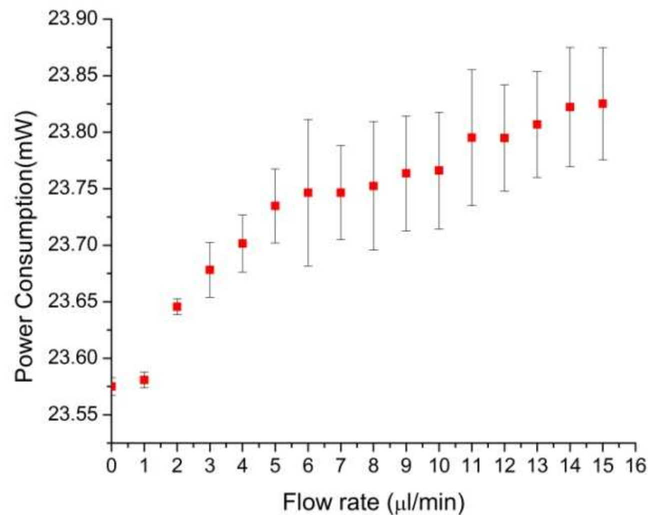


Figure 5.8. Measured power consumption with various flow speed

5.4 Summary

Smart tube devices with integrated pressure sensors and flow sensors have been demonstrated. Our new technology has the advantage of being compatible with CMOS and MEMS processes. High-temperature solid-state materials can be integrated, significantly increasing the performance and functionality of smart tube devices. By eliminating any post-fabrication bonding and packaging processes, high throughput and more reliable devices can be fabricated. The chemical resistance and biocompatibility of the parylene C makes our device suitable for a variety of biomedical applications. It is worth noting that other types of sensors and microfluidic components can be readily integrated.

CHAPTER 6. Additional applications and future work

6.1 Smart yarn devices

6.1.1 Introduction

Intelligent textiles, variously known as smart fabrics, electronic textiles, or e-textiles, have attracted considerable attentions worldwide due to their potential to bring revolutionary impacts on human life [9, 73]. Various functional yarns based on optical fibers, conductive polymer, metal filaments, or even carbon nanotubes have been developed for intelligent textile applications [74-77]. However, the aforementioned smart yarns do not have sophisticated electronics or sensors and require hybrid assembly of external circuits/sensors which render the system less flexible, and also less functionality in many cases. The ability to incorporate electronics and sensors into yarns monolithically and invisibly is highly desirable in order to reduce the complexity and increase the flexibility/functionality of the system. In addition, due to the temperature limitations, silicon-based sensors and CMOS circuits cannot be integrated. Our SOI-CMOS compatible technology to fabricate flexible electronics introduced in the previous chapters enables us to develop intelligent textiles. This compatibility allows the integration of high performance CMOS circuits by taking advantage of SOI-CMOS foundries. To prove the concept, we have demonstrated the integration of silicon strain gauges and MOSFETs.

6.1.2 Fabrication

The fabrication process our smart yarn device is compatible with the processes described in the previous chapters. CMOS compatible high temperature processes including thermal oxidation and Boron doping are performed prior to any parylene C deposition as demonstrated in Figure 6.1. All of the functional electronic components are made at this stage followed by the metallization of the interconnect traces. After the first layer of payrlene C deposition, arrays of O_2 plasma etched parylene C openings are specifically placed to avoid silicon devices and metal traces to expose the underneath silicon handling silicon layer. XeF_2 gas is then used to etch away the underneath silicon which forms the cavity at the same time based on our design. Second layer of parylene C layer is conformaly deposited to encapsulate the cavity and seals the parylene C openings at the same time to form a complete channel. As indicated in step (h), the smart yarns with integrated strain gauges and MOSFTEs were outlined and patterned along the parylene tubes via O2 plasma. Then the whole string of devices can be simply peeled off from the silicon substrate. The device at this stage was flexible and subject to kinks as it only consists of hollow parylene tube. PDMS, a silicon-based organic polymer, were simple injected from one end of the smart yarn as described in step (j). When the PDMS cures the device transforms into a solid fiber structure.

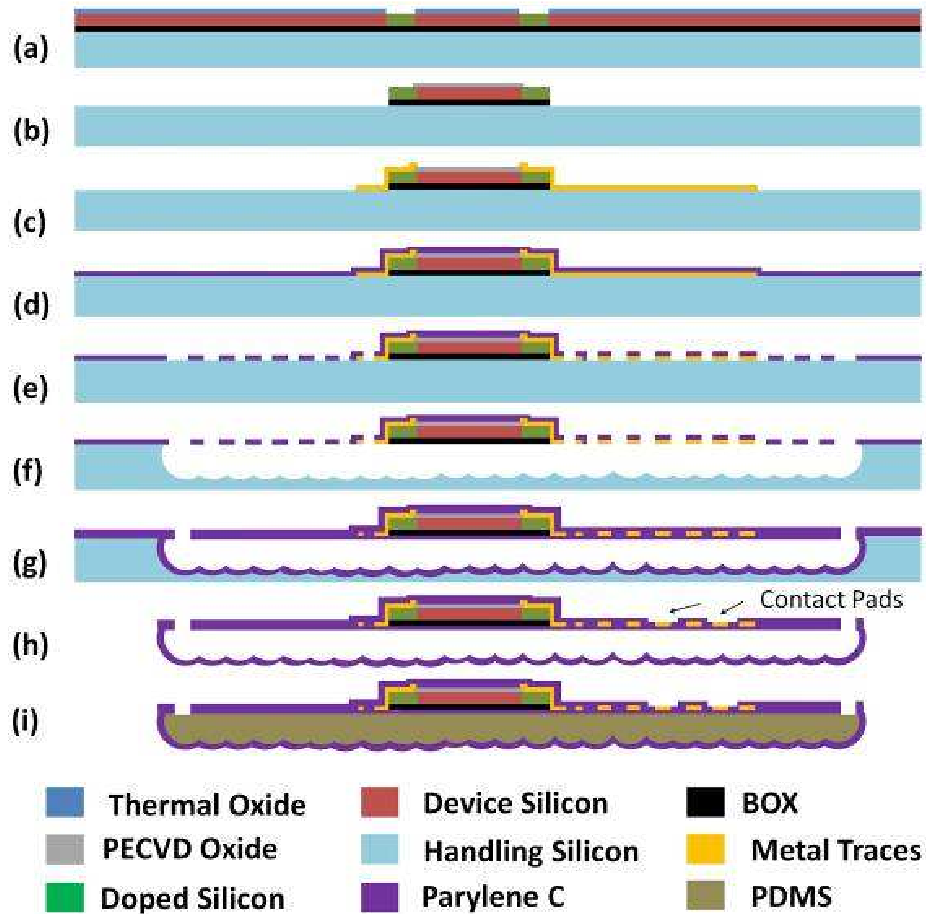


Figure 6.1. Simplified fabrication process: (a) Thermal oxide mask was used here for Boron diffusion; (b) Si island on device layer was patterned and the exposed BOX layer was removed; (c) Al deposition and patterning to form traces and pads; (d) 1st 3 µm parylene deposition; (e) patterning the parylene openings and exposed metal traces; (f) XeF_2 etching to completely undercut the handling wafer, making device free standing; (g) 2nd 10 µm parylene deposition to seal the previously opened parylene windows; (h) patterning the parylene layer, open the contact pads and releasing the device; (i) PDMS was injected as a supporting core.

6.1.3 Results and discussion

Figure 6.2 shows a fabricated parylene smart yarn which measures 7.5 cm in length and around 100 µm in diameter. The diameter of our smart yarn is comparable to that of human hairs which vary from 17 to 180 µm. Note that we are able to control the width of our device by simply modifying the number of columns of parylene etching windows and the spacing between parylene columns. In addition, overall diameter of our device can be controlled by modifying the depth of XeF_2 etching based on the number of etching loops. Excellent flexibility can also be observed and the device can be easily handled between fingers thanks to its reinforcing PDMS core. The bright reflection observed in the picture bellow is the result of metal interconnects.

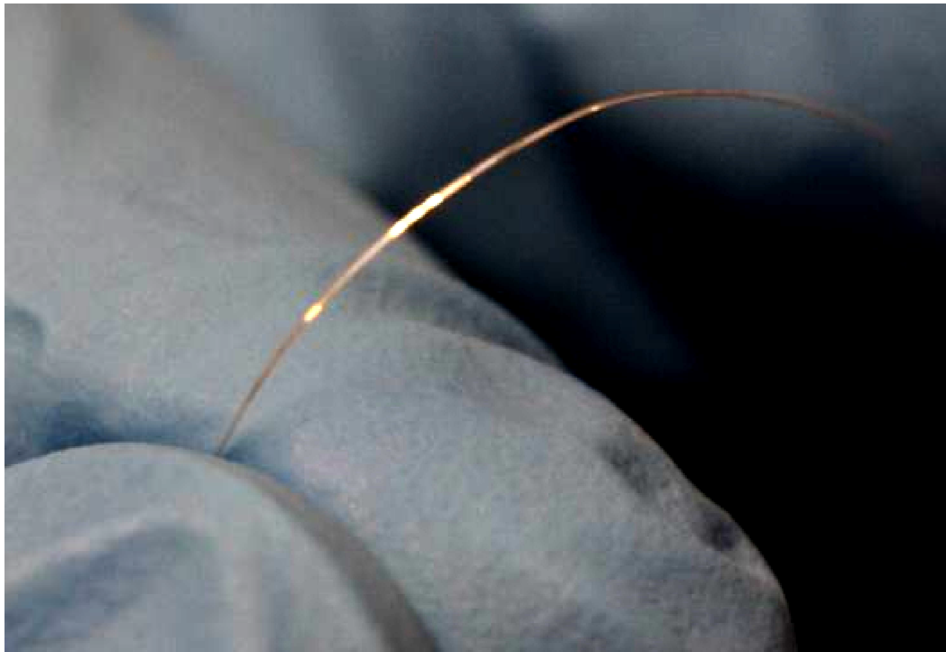


Figure 6.2. A parylene smart yarn held between fingers and bent to show its flexibility.

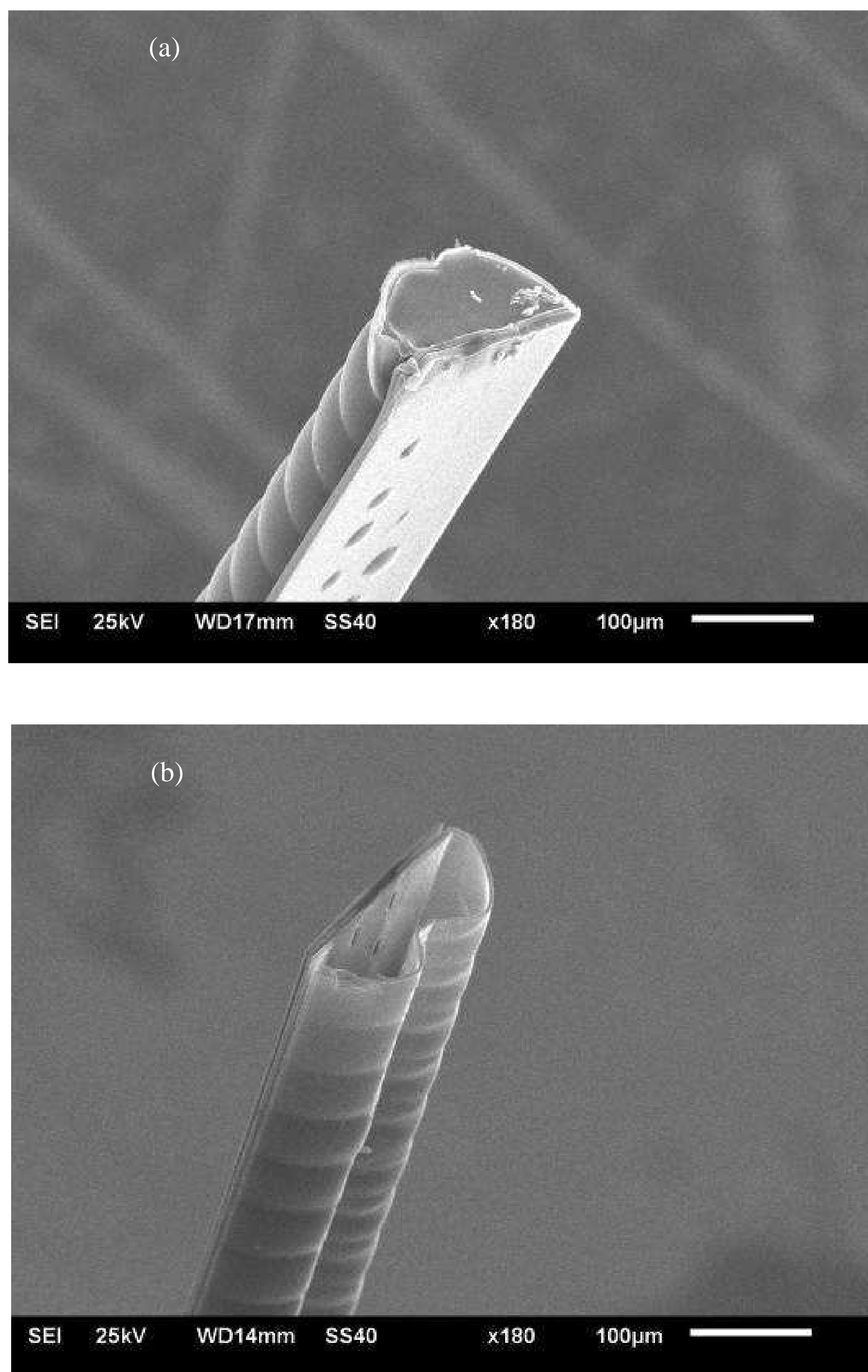


Figure 6.3. Cross-sectional SEM images of our parylene fibers. (a) Fiber filled with PDMS; (b) Hollow fiber without PDMS core.

To better understand the benefits of the reinforcing PDMS core, two devices with and without PDMS core were prepared for comparison. Cross-sectional SEM images of these two samples were shown in Figure 6.3.

It can be observed that the device on the left has more rounded profile compared with the device without PDMS. The parylene C tube remains pressurized during PDMS injection and curing process. Moreover, we have put those two samples under extreme bending test to better understand the benefit of having a reinforcing core. As shown in Figure 6.4 (a), the results clearly demonstrate that our device with PDMS core is almost kink-free under extreme deformation. A bending radius of 0.5mm has been achieved. In comparison, Figure 6.4 (b) shows the kinked device without PDMS core. Any integrated electronics/sensors will be prone to damages as extreme strain and stress will be generated at kinked regions. The PDMS core not only functions as a reinforcing layer but also helps to reduce the strain on electronic components when the smart yarn is under deformation.

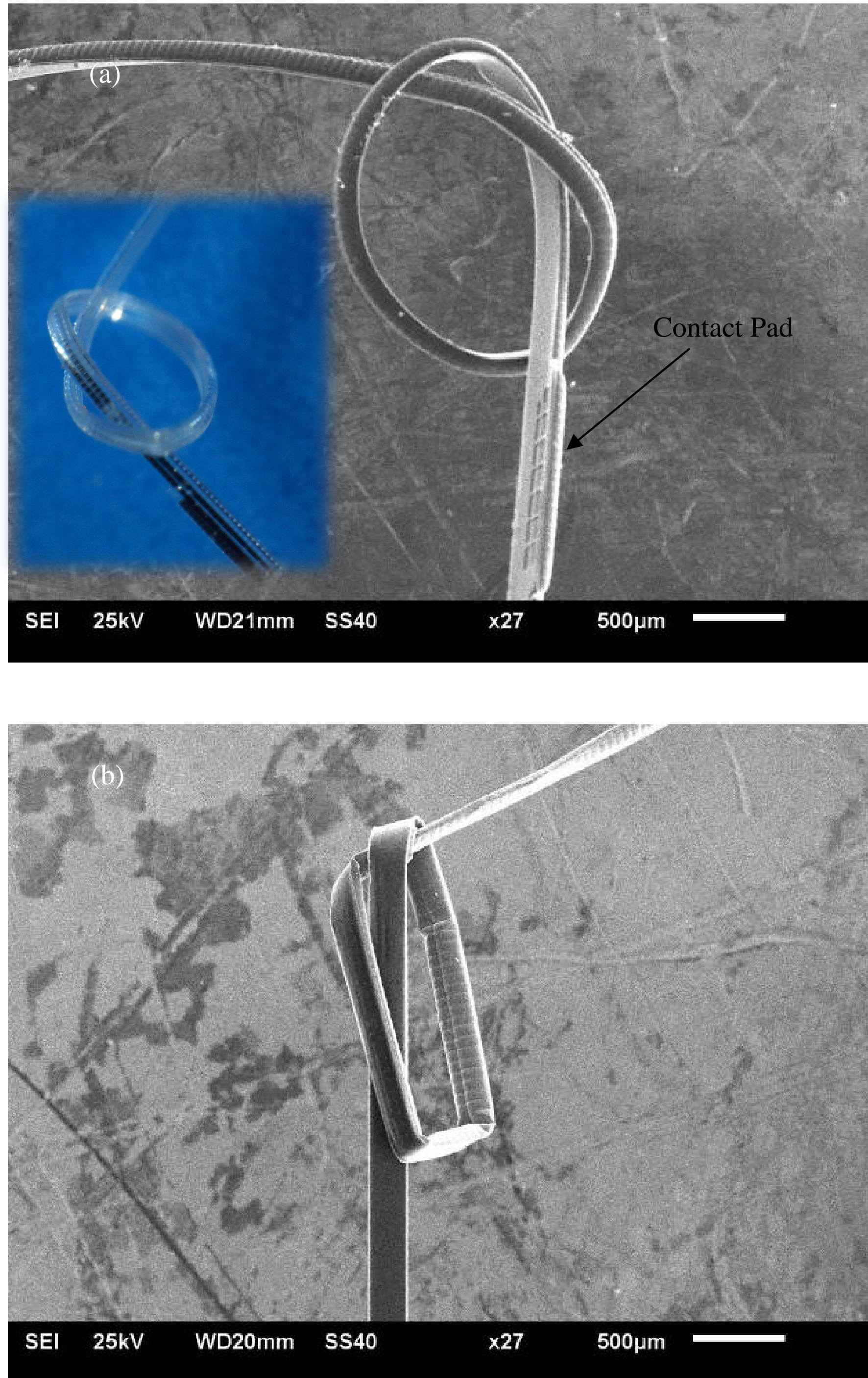


Figure 6.4. (a) SEM image of a kink-free knot made by PDMS filled yarn; the inset picture is an optical image of the actual PDMS filled yarn; (b) SEM image of a kinked knot made by parylene fiber without PDMS core.

To prove the concept, simple silicon strain gauges and MOSFETs were first integrated as seen in Figure 6.5. The whole device is highly transparent even when filled with PDMS. It allows us to visually inspect any damages caused by excessive force. In order to electrically access those devices, conductive epoxy was used to connect the exposed contact pad.

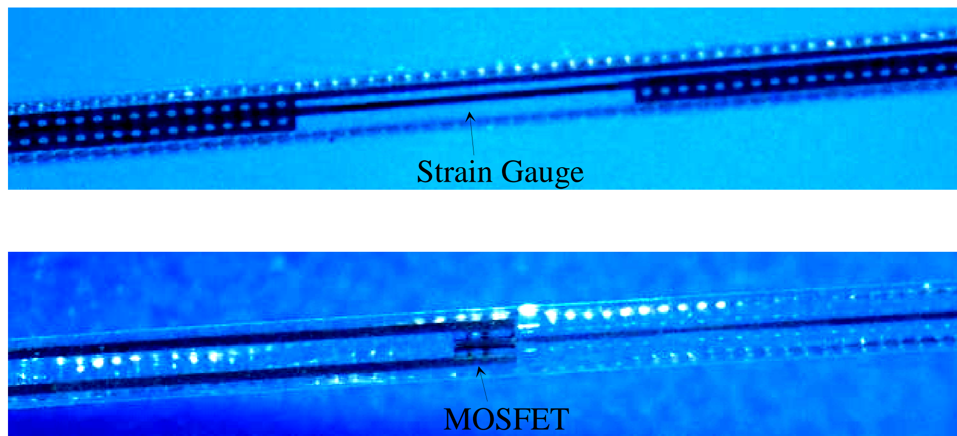


Figure 6.5. Optical images of a strain gauge and a MOSFET integrated in the parylene yarn.

6.1.3.1 Bending test of the integrated strain gauge

Silicon strain gauge of 30 μm by 1mm was embedded in the longitudinal direction of the yarn. A simple bending test was carried out to evaluate integrated strain gauge as demonstrated in Figure 6.6. The testing was performed under an enclosed chamber to eliminate ambient air flow which will cause unstable reading from the gauge. The total length of the clamped smart yarn was 21mm with the strain gauge positioned in the middle. A moving stage with a step resolution of 5 μm was used to displace one end of the smart yarn. Total displacement of 3mm was achieved during test. Note that the smart yarn in the

schematic was the actual device bent at maximum displacement. The resistance change of the strain gauge as a function of displacement was plotted in Figure 6.7 as we moved the stage forward to its max displacement and then backward to its original position. Hysteresis was observed due to the plasticity of the PDMS core and outside parylene shell during the test.

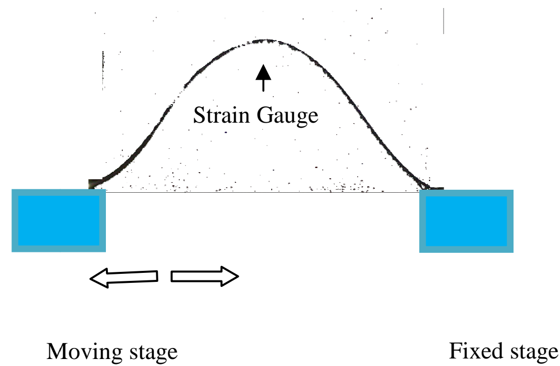


Figure 6.6. Experiment setup: the parylene fiber was secured at two stages with strain gauge positioned at the center. The parylene fiber was flat at initial position. Then the stage moved to the right to a maximum displacement of 3mm.

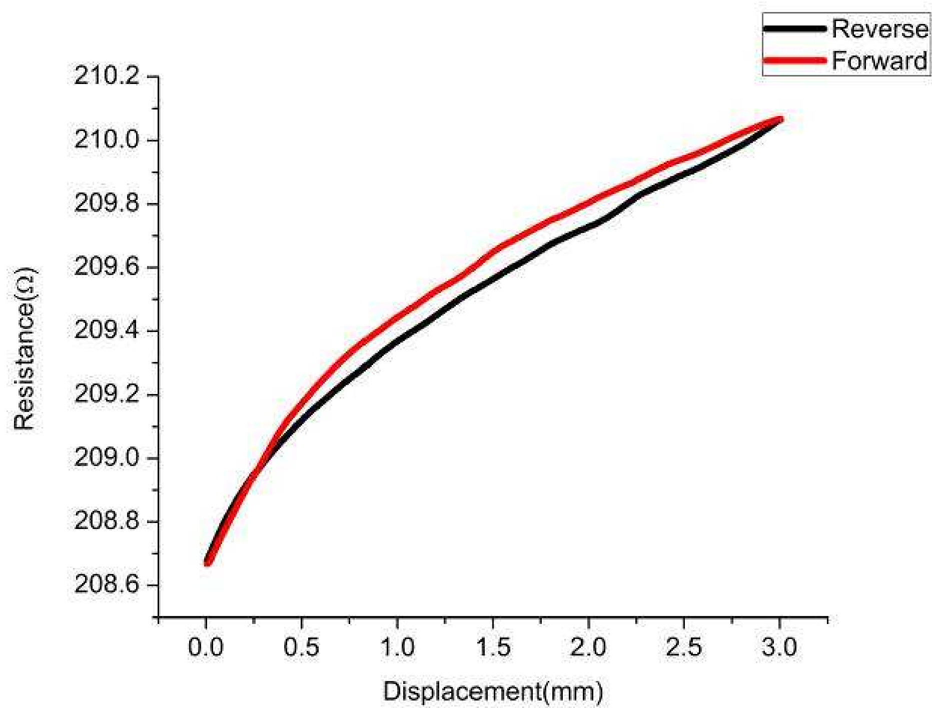


Figure 6.7. The resistance change of the strain gauge

6.1.3.2 Electrical characteristics of MOSFET

MOSFETs are building blocks for electronics which are used for amplifying or switching electronics signals. A simple p-channel MOSFET has been built into our smart yarn and also been preliminarily characterized. The I_{sd}-V_{sd} curves of the p-channel MOSFET device with different V_{sg} are plotted as seen in Figure 6.8. It can be observed that the threshold voltage V_{th} of this p-channel MOSFET is less than -10V. The fabrication process of our MOSFETs was not optimized for the performance in our prototype development. The purpose of this work was to demonstrate the ability of our technology to incorporate MOSFETs.

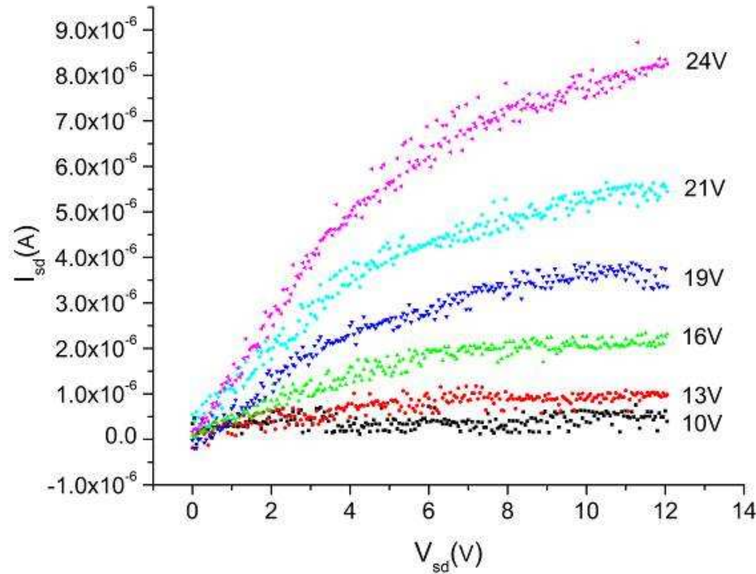


Figure 6.8. I_{sd}-V_{sd} curves of one pMOSFET device with different V_{sg}.

6.1.3.3 Implementation of the smart yard device to blood pulse measurement

The smart yard device with integrated sensors enabled by our technology will bring significantly improvements to a variety of wearable applications. For proof-of-concept purpose, we utilized the integrated strain gauge on our flexible yarn for wearable blood pulse monitoring application. The implementation of such a wearable device is very straight-forward. Our smart yarn with strain gauge was wrapped around the wrist with a slight pressure. The blood pulse correspondingly creates stress pulse on the strain gauge. As demonstrated in Figure 6.9., the stress pulse can be clearly observed in the form of measured voltage. This preliminary data proves that our method is valid and our device is capable for wearable blood pulse measurement.

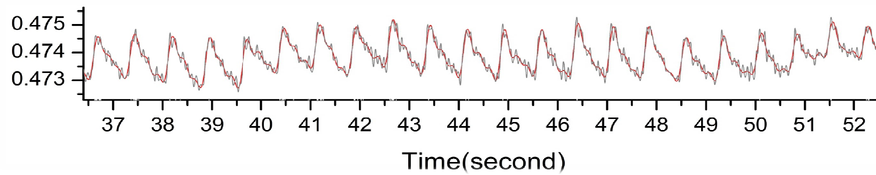


Figure 6.9. Blood pulse measurement data.

6.1.4 Conclusion

In conclusion, a SOI-CMOS compatible technology to fabricate smart yarns has been successfully demonstrated. MOSFETs and strain gauges can be first fabricated using commercial SOI-CMOS processes and readily integrated into smart yarns. Based on the amount of the undercut from XeF_2 etching, the size of the yarn is only limited by the wafer thickness. Note that the reinforcing PDMS core will significantly increase the robustness of the yarn and prevent kinks when under deformation. Depending on the applications other types of reinforcing cores are also under investigation. It is also worth noting that our technology is post-MEMS compatible which means various MEMS sensors and CMOS circuits can be integrated with slight modification of our fabrication process which will further expands the functionality of the smart yarn device. The smart yarns can be incorporated into fabrics, leading to wearable sensors or electronics. Wearable health monitoring systems based on smart yarns are highly desirable due to their convenience and non-invasive nature.

6.2. Micro PH sensors

6.2.1. Introduction

The pH sensor has served as an indispensable tool for both biology and chemistry industries. The conventional glass tube pH sensor has limitations for a wide variety of applications due to its bulky size. With the help of micro-fabrication techniques, various micro-scale pH sensors have been developed. Among various materials, IrO2 which can provide a rapid and stable response in different conditions, became a superior material for pH sensing [78]. However, most of the thin-film micro pH sensors do not have Ag/AgCl reference electrode[79-81] which significantly compromise the sensing performance and long term stability.

To overcome this draw back, we have developed a flexible liquid junction Ag/AgCl reference electrode for micro pH sensor based on our previously reported smart tube technology [35]. Specifically, the reference electrode is constructed by simply inserting a 50 μm diameter Ag/AgCl wire into a 100 μm diameter parylene tube and then sealing the open end of the tube with porous Gel. To form a complete pH sensor, IrO_2 working electrode can be directly fabricated onto the parylene tube surface.

6.2.2. Working principle of a conventional pH meter

By definition a pH meter is an electronics device used to measure the pH value of a liquid solution. The value of pH in a solution is determined by the concentration of hydrogen ion. As indicated in Figure 6., both reference electrode and measurement electrode are used in a commercial pH meter. Reference electrode used here is because a stable electrical potential is required when measuring different solutions. An Ag/AgCl electrode is commonly used as a standard reference electrode which has a relative stable potential in variety of solutions. Glass doped with lithium ions will react with hydrogen ions and potential can be measured to determine the pH value of the solution.

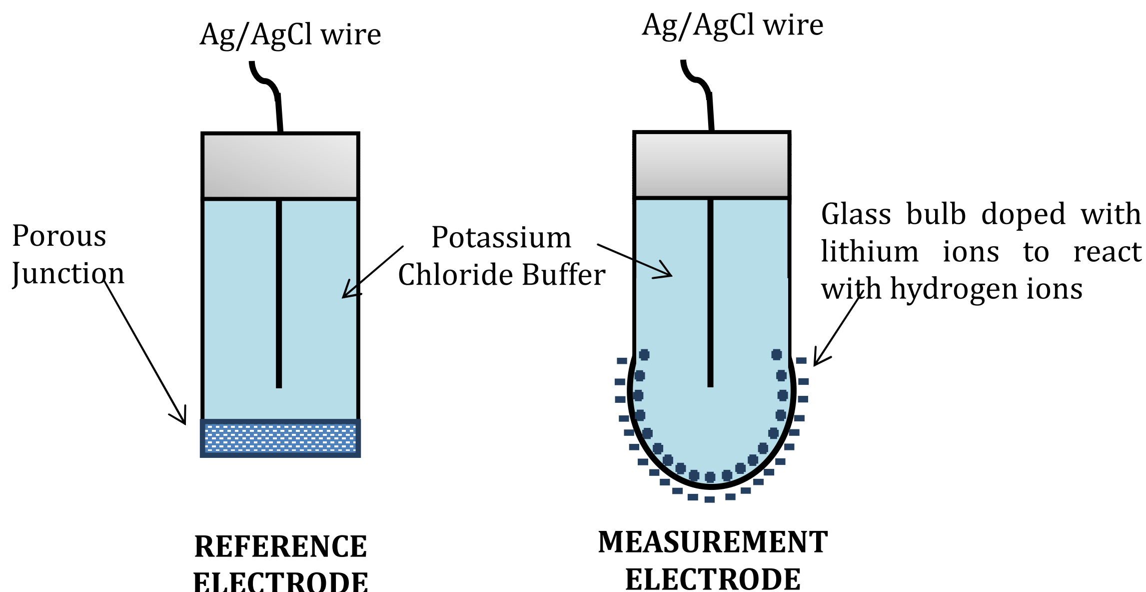


Figure 6.10. Components of a working pH meter.

A commercial pH meter which integrates both reference electrode and measuring electrode in a single package is shown in Figure 6.9. Obviously they are very bulky and require large volume of sample solution.

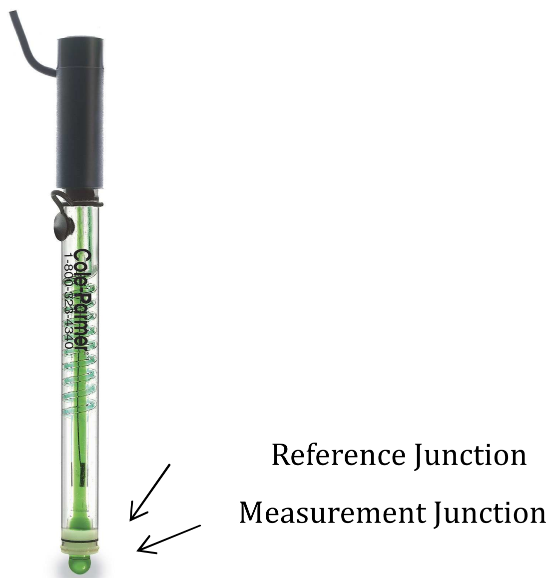


Figure 6.9. A commercial glass tube pH meter. Source: Cole-Parmer

Doped glass used in commercial pH meters are very bulky and expensive to make. Other materials have been explored to selectively measure the concentration of the hydrogen ions. IrO_2 appears to be a very good candidate to be used in pH sensing application. Our technology enables us to directly integrate the IrO_2 electrode onto our miniature reference electrode.

6.2.3. Design and fabrication

Our technology takes advantage of XeF_2 isotropic gas phase silicon etching and conformal parylene C coating.

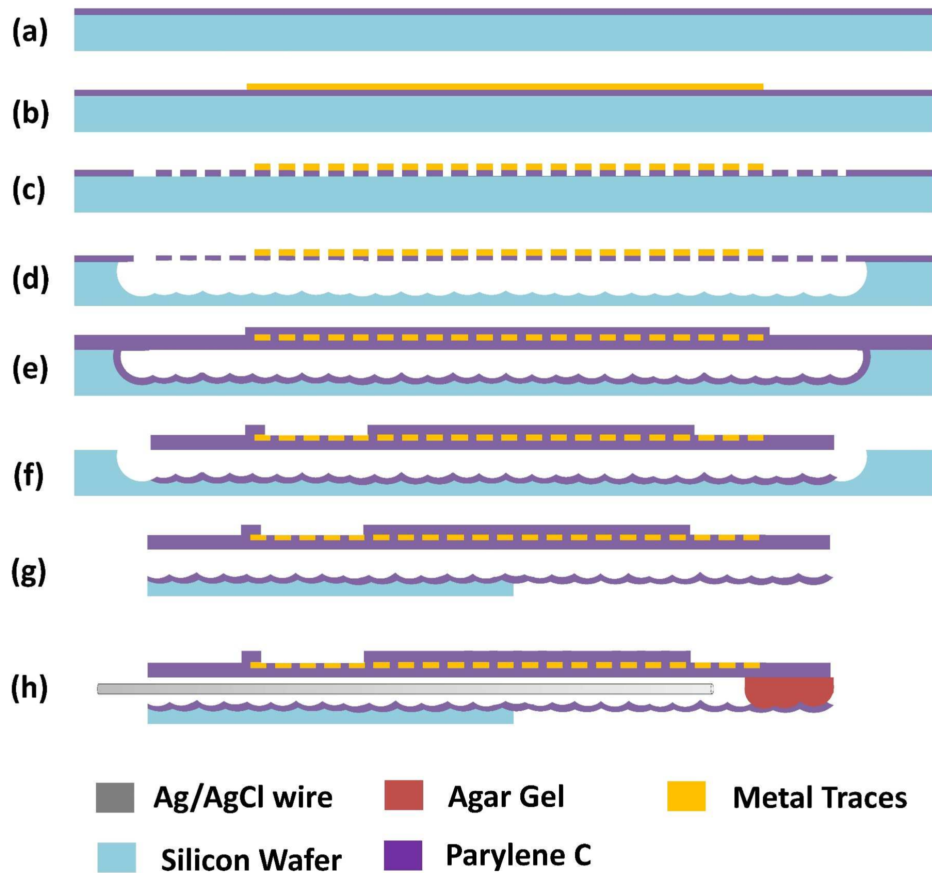


Figure 6.10. Simplified fabrication process: (a) Parylene C coating on a silicon wafer; (b) Metal deposition to form sensing and contact pads ; (c) patterning the parylene openings; (d) XeF_2 etching to completely undercut the handling wafer and forms underlying channels; (e) 2nd 10 µm parylene deposition to seal the previously opened parylene windows; (f) patterning the parylene layer, open the contact pads and exposing the device inlet and outlet; (g) Backside DRIE etching to release the device from silicon wafer; (h) Insert the Ag/AgCl wire and plug one end with Agar gel.

The process starts with depositing a 4 μm thick parylene C layer on the top surface of a silicon wafer. Then a Au layer is thermally evaporated with Ti adhesion layer. This metal layer is subsequently patterned to form the sensing and contact pads as indicated in step b. Two columns of parylene C windows are opened in step c to expose the underneath silicon. $XeFe_2$ isotropic silicon etching is used in step d to form the tubular shaped cavity as demonstrated in step d. A second layer of 10 μm parylene C is conformably coated on the entire wafer. Due to the conformal coating property of parylene C, tubular cavity will be uniformly coated and sealed by parylene C. Then O_2 plasma is used in step f to expose the metal pads and shapes the outline of the device. Backside DRIE is used in step g to etch away any unwanted silicon and release the device from the substrate. In order to make the device more robust, a portion of the silicon is left un-etched at the base of the sensor. Finally, a 50 μm Ag/AgCl wire is inserted inside the parylene tube and the tube is then capped by agar gel to form a salt bridge.

Figure 6.11 shows the schematic of the proposed PH sensor. Agar gel is used here to function as the salt bridge for our reference electrode. A 50 μm thick Ag wire is electroplated with a layer of AgCl on the surface by soaking the Ag wire in 1 Mole KCl solution and passing current through the Ag wire. As for the sensing electrode, IrO_2 is proven to be a good material to be used as pH sensor. The device is under development at the moment and IrO_2 has not been coated on the actual device. In the following section, only the part involving the reference electrode will be discussed.

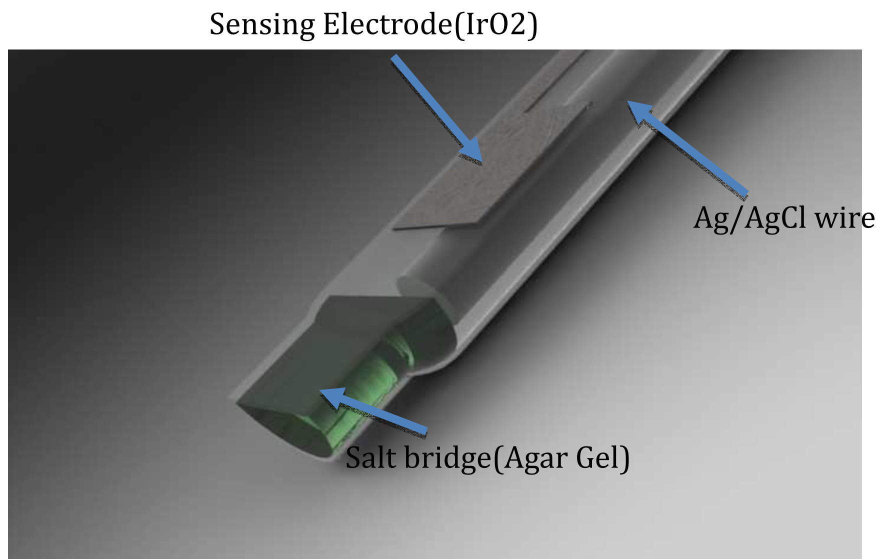


Figure 6.11. Schematic diagram of the proposed device

6.2.4. Device testing and characterization

A fabricated micro pH sensor is presented in Figure 6.12. IrO_2 has not been plated on the sensing tip. Polyimide tubing is used here to couple the silicon inlet in order to inject KCl solution. The tip of the device is narrower to prevent the gel from being pushed out of the position. This is achieved by converging two lines of parylene windows into a single row for XeF_2 etching. Figure 6.13 shows the backside SEM picture of a fabricated device.

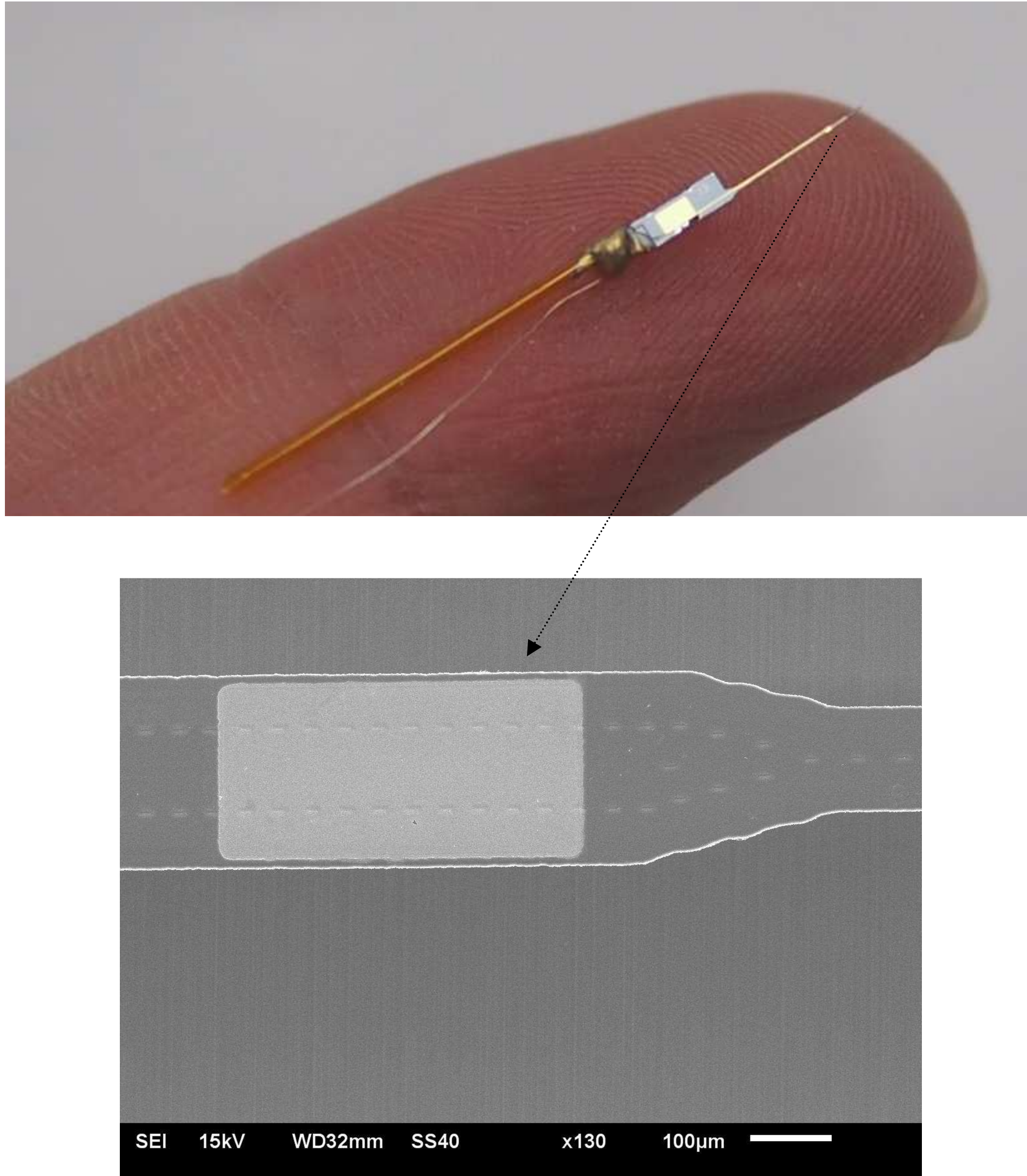


Figure 6.12. (a) Fabricated micro pH sensor place at the finger tip. (b) SEM picture of the exposed Au electrode before IrO_2 coating

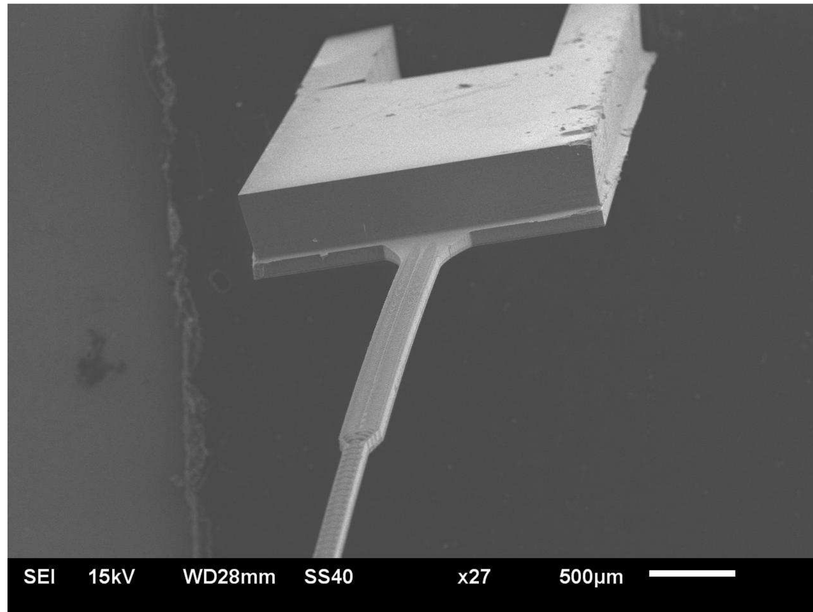


Figure 6.13. SEM picture of the micro pH sensor

In order to test the performance of our fabricated reference electrode, a commercial reference electrode is used during the testing. Both the commercial reference electrode and our device were submerged into a saturated KCl solution. The measured voltage of our device against the commercial reference electrode is plotted in Figure 6.14. The data were measured every 2 seconds. It can be observed that the potential of our electrode against commercial reference electrode is held very stable for about 5 hours. After 5 hours, the AgCl layer plated on the surface of Ag wire was consumed and subsequently our device lost its reference capability.

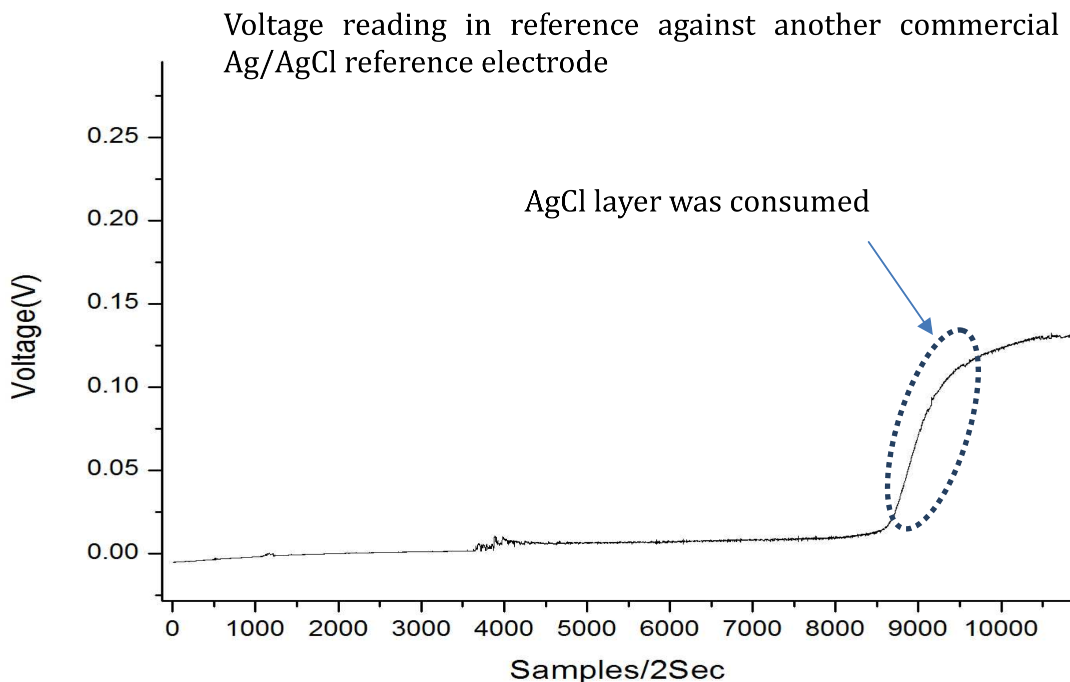


Figure 6.14. Potential measurement against another commercial Ag/AgCl electrode

6.2.5 Summary

The initial testing proves that our device can potentially serve as a stable reference electrode. However, there is still more work to be done. First, the AgCl layer electroplated on our Ag wire has to be thicker for longer period of operation. Then IrO_2 has to be coated on top of the Au sensing pad to achieve the pH sensing functionality. It is worth noting that most of the existing micro pH sensors require additional bulky reference electrode for measurement. Therefore, it is a great advantage that our technology enables the monolithic integration of both sensing electrodes and stable reference electrodes.

6.3 Conclusion and future work

This innovative technology to make flexible electronics/sensors developed in our lab during my Ph. D. research has been adopted to make a variety of useful devices. The technology was first implemented in making parylene microtube arrays [32] with integrated out-of-plan micro needles. The fact that our needle arrays can be individually addressed makes our device useful in many applications. The micro needles device has been used for retinal prosthesis study which will help to restore vision to the blind.

The ability to integrate microfluidic channels is unique to our technology. Various medical devices have been made using our technology. For example, we have developed a hybrid silicon-parylene neural probe with locally flexible regions [83]. Parylene is a highly flexible material, 3D devices are made possible with the help of the simple folding process. A multifunctional chronic 3D electrode array has been developed based on this principle.

The ability to integrate more complex electronics and transducers [34] is another key feature in our technology. For example, we demonstrated the integration of MOSFETs with flexible substrates and smart yarns [34]. We are able to integrate both pressure sensors and flow sensors into a micro parylene tube [35].

Silicon devices are still considered to be the first choice in the semiconductor industry. Our technology also relies on the processes originated to process silicon wafers. It is vital that we also make otherwise sacrificial silicon as part of our devices. We have developed a silicon-polymer platform which enables us to achieve self-locking and self-deploying

origami[33] as well as deformable silicon solar cells[60]. The integration of the silicon structures significantly improves the functionality of our flexible devices[84].

A lot of efforts have been dedicated to further expand the capability of our technology and it has been evolving over the past few years. More features and fabrication processes have been integrated into developing a variety of devices. Among various processes, XeF_2 isotropic silicon etching process, conformal parylene C coating process and deep reactive-ion etching (DRIE) are the most important techniques used in our technology. We have developed a simple two-mask process to fabricate an in-channel micro check valve[82] by only using the aforementioned techniques. Therefore, this type of check valve can be potentially integrated. Our technology is very versatile with the possibility to integrate additional MEMS fabrication processes and other materials.

This technology has inspired us to develop numerous interesting and useful devices. The potential of our technology is enormous. Many wearable and implantable devices can be developed based on this technology.

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ABSTRACT

FLEXIBLE MEMS DEVICES:
A NOVEL TECHNOLOGY TO FABRICATE FLEXIBLE ELECTRONICS

by

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December 2014

Advisor: Dr. Yong Xu

Major: Electrical Engineering

Degree: Doctor of Philosophy

This dissertation presents the design and fabrication techniques used to fabricate flexible MEMS (Micro Electro Mechanical Systems) devices.

MEMS devices and CMOS(Complementary Metal-Oxide-Semiconductor) circuits are traditionally fabricated on rigid substrates with inorganic semiconductor materials such as Silicon. However, it is highly desirable that functional elements like sensors, actuators or micro fluidic components to be fabricated on flexible substrates for a wide variety of applications. Due to the fact that flexible substrate is temperature sensitive, typically only low temperature materials, such as polymers, metals, and organic semiconductor materials, can be directly fabricated on flexible substrates. A novel technology based on XeF_2(xenon difluoride) isotropic silicon etching and parylene conformal coating, which is able to monolithically

incorporate high temperature materials and fluidic channels, was developed at Wayne State University.

The technology was first implemented in the development of out-of-plane parylene microneedle arrays that can be individually addressed by integrated flexible micro-channels. These devices enable the delivery of chemicals with controlled temporal and spatial patterns and allow us to study neurotransmitter-based retinal prosthesis.

The technology was further explored by adopting the conventional SOI-CMOS processes. High performance and high density CMOS circuits can be first fabricated on SOI wafers, and then be integrated into flexible substrates. Flexible p-channel MOSFETs (Metal-Oxide-Semiconductor Field-Effect-Transistors) were successfully integrated and tested. Integration of pressure sensors and flow sensors based on single crystal silicon has also been demonstrated. A novel smart yarn technology that enables the invisible integration of sensors and electronics into fabrics has been developed.

The most significant advantage of this technology is its post-MEMS and post-CMOS compatibility. Various high-performance MEMS devices and electronics can be integrated into flexible substrates. The potential of our technology is enormous. Many wearable and implantable devices can be developed based on this technology.

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5. **H. Tu**, H. Jiang, H. Yu and Y. Xu "Hybrid Silicon-polymer platform for self-locking and self-deploying origami" ***Appl. Phys. Lett.*** 103, 241902 (2013)

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8. E. Kim, **H. Tu**, C. Lv, H. Jiang, H. Yu and Y. Xu "A robust polymer microcable structure for flexible devices" ***Appl. Phys. Lett***. 102, 033506 (2013)

9. **H. Tu** and Y. Xu, "A Silicon-on-insulator complementary-metal-oxide-semiconductor compatible flexible electronics technology", ***Appl. Phys. Lett***., 101, 052106 (2012)

10. Y. Li, **H. Tu**, R. Iezzi, P. Finlayson and Y. Xu, "Development of Individually-Addressable Parylene Microtube Arrays", ***J. Micromech. Microeng.*** 21, 115005 (2011)

11. **H. Tu**, Q. Zheng, and Y. Xu, "Preliminary study of resonant mass sensors based on asymmetrically-gapped cantilevers", ***Sensors Journal***, IEEE 11 (5), 1107-1111 (2011)