

Power and Area Efficient Sense Amplifier Based Flip Flop with Wide Voltage and Temperature Upholding for Portable IoT Applications

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Abstract: A sense amplifier based flip-flop (SAFF) capable of operating unflinchingly at wide voltage and temperature ranges is proposed in this work. The proposed flip-flop (FF) has a single ended latch design which results in a significant improvement in power and area requirements. The modified sense amplifier along with the single ended latch design enables robust and low power operation at all variations in the input data activity. The proposed SAFF is developed in 32nm CMOS technology, and a thorough and conclusive investigation with corner case simulation for wide process, voltage and temperature (PVT) variations is carried out in order to verify the design utilization. Comprehensive comparison and analysis with previously available state-of-the-art SAFFs validate that the proposed SAFF is functional at wide voltage ranges for temperature changes of 120 °C to -40 °C while upholding better and optimal power and power delay product (PDP) results. The proposed FF, because of its power efficiency, is best suited for portable Internet of Things (IoT) devices.

Keywords: low power design; CMOS digital circuit; sense amplifier based flip-flop; single ended; IoT

Energetsko in prostorsko učinkovit senzorski ojačevalnik na osnovi flip flopa s širokim razponom napetosti in temperature za prenosne aplikacije interneta stvari

Izveček: V članku je predlagan flip-flop, ki temelji na senzorskem ojačevalniku (SAFF) in lahko deluje brezhibno v širokem razponu napetosti in temperature. Predlagan flip-flop (FF) ima enonivojski zapah, kar znatno izboljša zahteve po moči in površini. Spremenjen ojačevalnik zaznavanja skupaj z enonivojskim zapahom omogoča zanesljivo delovanje z nizko porabo energije pri vseh spremembah vhodne podatkovne aktivnosti. Predlagani SAFF je razvit v 32 nm tehnologiji CMOS, za preverjanje uporabe zasnove pa je opravljena temeljita in prepričljiva raziskava s simulacijo robnih primerov za velike spremembe procesa, napetosti in temperature (PVT). Obsežna primerjava in analiza s predhodno razpoložljivimi najsodobnejšimi SAFF potrjujeta, da je predlagani SAFF funkcionalen v širokem razponu napetosti za temperaturne spremembe od 120 °C do -40 °C, hkrati pa zagotavlja boljše in optimalne rezultate glede moči in zakasnitve moči (PDP). Predlagani FF je zaradi svoje energetske učinkovitosti najprimernejši za prenosne naprave interneta stvari (IoT).

Ključne besede: zasnova z nizko porabo energije; digitalno vezje CMOS; flip-flop, ki temelji na senzorskem ojačevalniku; enonivojsko vezje; internet stvari

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1 Introduction

Smart and IoT based technologies have advanced swiftly, creating a wide range of prospects for technological advances in many different areas of life. The main goals of IoT technologies are to improve quality of life, ensure improved system (or process) efficiency, and streamline processes across a range of industries. IoT technologies are rapidly evolving and providing a number of beneficial outcomes, but in order to prevent negative environmental effects and ensure the sensible use of limited global resources, this rapid development must be closely monitored and analyzed from an environmental point of view [1]. In the former sense, significant research is required to thoroughly examine the benefits and drawbacks of IoT technologies. For IoT applications like wearable technology and portable medical equipment, on-chip security mechanisms are essential [2]. Memory offers a physically unclonable function that can be employed in security implementation. Problems with resistive RAM memory applications stem from its stochastic switching process and the resistance's inherent unpredictability. For use in smart mote devices, biomedical implants and wireless sensor nodes, the present IoT era requires ultra-low power System on Chip (SoC) designs and architectures [3].

In modern digital circuit design, flip-flop is the critical part of most essential circuit components since they synchronize data flow and allow for local data storage [4]. A typical processor requires a lot of flip-flops, often hundreds of thousands, because this synchronization must take place across the whole clock domain [5]. Due to their high density, flip-flops consume a substantial amount of both space and power in the overall circuit architecture [6]. In light of this, minimizing the power dissipation of flip-flops has a major effect on system level power efficacy, particularly for IoT applications with constrained energy resources [7]. For IoT Integrated Circuits (IC) to maximize battery life, power consumption must be kept to a minimum. However, a significant percentage of power, specifically the dynamic power dissipation, in a synchronous system is used by flip-flops, which can change its state at every clock pulse. Due to this, numerous research projects have been carried out in an effort to create flip-flops that use less energy and are more efficient.

The overall system architecture greatly benefits from the chip area and power consumption that FFs provide. In order to satisfy varied application requirements, many FF designs have been presented [8]–[12]. One of them is the sense amplifier-based FF architecture, which comprises of a latch and a dynamic logic sense amplifier [13]. It is thought to be a superior design choice to meet both low power and high speed requirements because it has a shorter set-up time and greater

power output than standard FF. But there are two real-world issues with this FF architecture. First, switching power reduction becomes less effective at reduced or no data activity and power dissipation may be more at sense amplifier's pre-charge processes. Second, a longer clock-to-output delay results from the NAND latching stage receiving the data from the sense amplifier stage. Additionally, it has been shown that complementary FF outputs are not always required in applications.

A sense amplifier based flip flop suited for the low power domain is proposed in this study. The structure of the paper is as follows: The prior-art SAFFs are examined in Section 2, along with their advantages and disadvantages. The proposed SAFF, which is intended for reliable and low power operations, is presented in Section 3. The simulation findings and evaluations with existing SAFFs are presented in Section 4. Finally in section 5 the proposed SAFF is experimented in an actual digital circuit along with power measurements to verify its worthiness.

2 Related work

A basic sense amplifier based flip-flop consists of two stages: a sensing stage and a latching stage. The sensing stage uses a fast differential sense amplifier having two outputs (SB and RB), which is followed by a slave latch. The principle of operation of this flip-flop may be described as follows:

- The precharge state: When the clock is low, both the sensing stage's outputs, SB and RB are high. The latch stage retains the prior value.
- The evaluation state: When clock is high, one of the outputs of sensing stage is low. If the input is high, the sensing stage's SB output terminal will be low, and if the input is low, the sensing stage's RB output terminal will be low. At this point, the state of SB and RB determines how the output of the latch stage is driven. On the rising edges of the clock, for instance, if SB is low, the output is driven to a high state logic, and if RB is low, the output is driven to a low state logic.

Fig. 1 shows the prior-art SAFF, known as CBSAFF, proposed by [14]. The sensing stage in this FF uses a capacitive boosting approach. The capacitive boosters which are actually MOS transistors that are being used as capacitors amplify the data signal and provide a big enough voltage swing to trigger the latch stage from $-\beta \cdot VDD$ to $\beta \cdot 2VDD$. Here, the value of " β " (the boosting efficiency) is <1 due to parasitic capacitances. The

buffer turns on the pre-charge transistor to charge the boost capacitor to provide voltage when the clock input is '0'. This buffer is utilized to help boost the voltage to twice the value when the clock input becomes '1' and to stop the clock signal from being loaded with capacitor.

In Fig. 2, Strollo's SAFF [15] is schematically depicted. The output stage can be thought of as a combination of the N-C MOS circuit and the typical NAND based SR latch. The high-to-low output transition is accelerated using the additional transistors. In this design, removing the speed up network and condensing the sizes of few transistors significantly minimize power dissipation. As a result, the capacitive load is reduced, which permits a reduction in the size of the driving transistors at the sensing stage. In order to improve latency and power dissipation during the "1" to "0" transition a PMOS is added to the output stage, this further reduces the current (crow-bar).

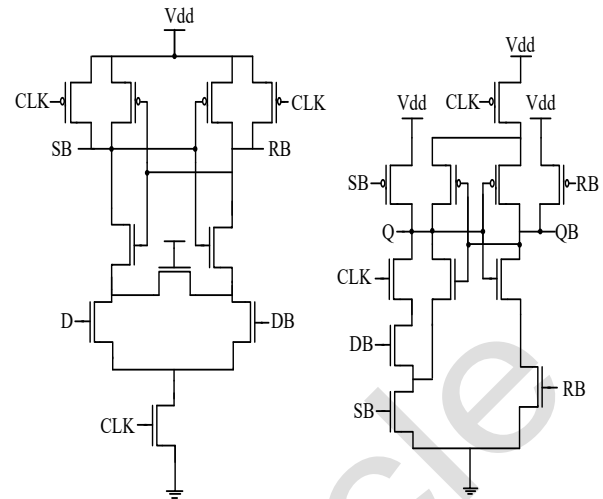


Figure 2: Architecture of Strollo's FF [15]

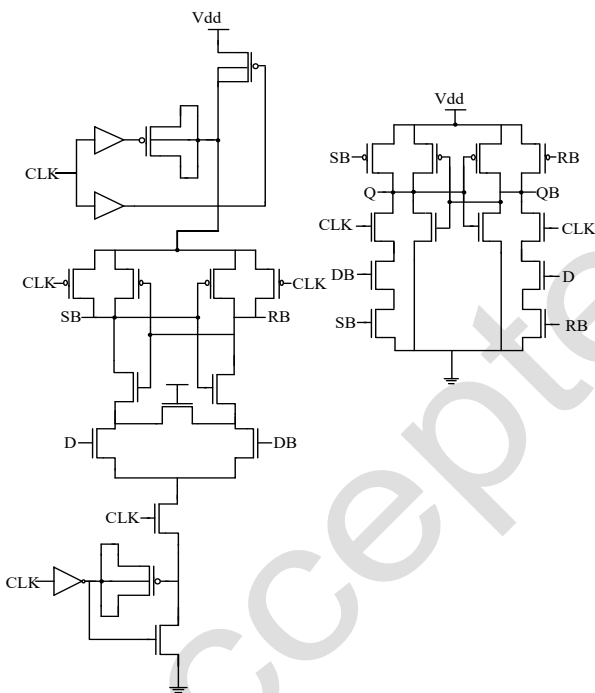


Figure 1: Architecture of CBSAFF [14]

A SAFF based on a transition complete (TC) signal was introduced by Jeong in [16] in order to address the issues with earlier SAFFs at low voltages. This SAFF-structure is depicted in Fig. 3. The sensing stage's outputs are the two inputs of a NAND gate, which produces the TC signal. Only after SET output of sensing stage is charged up, the signal TC discharges. As a result, at the clocks falling edge, both TC and SET signal are briefly high, which could result in an output glitch. However, compared to the SAFF-related issue, this hiccup is minor and far smaller. This kind of FF prevents the current conflict between latching pMOS transistors and output or compliment output pull-down pathways.

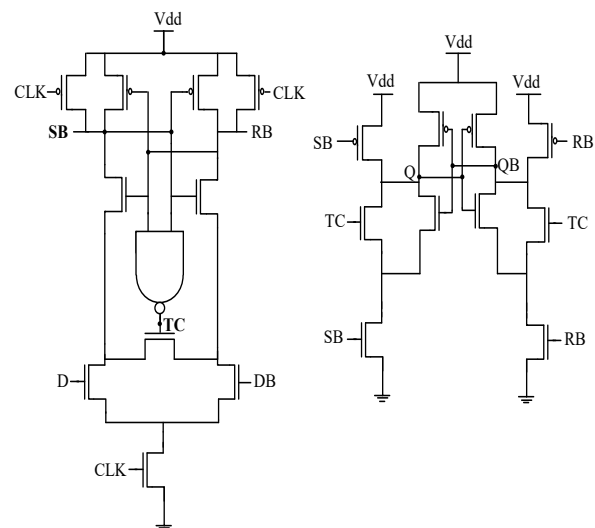


Figure 3: Architecture of Jeong's FF [16]

Another example of SAFF is the Nikolic's SAFF [17] depicted in Fig. 4. The sense amplifier is the same as that in Fig. 2. Latching stage allows for small keeper transistors because only one transistor is active in each branch when the state is changed. The slave latch has symmet-

ric true and complementary trees, which causes the delays at both outputs to be the same. The small size of the keeper transistors causes them to quickly turn off during the transition. This enables the load to be driven and the latch's status to be changed by exterior driver transistors. This characteristic makes the procedure of output transistor size optimization simple. The resistance of the output stage to crosstalk when there is a low clock pulse is the only restriction on minimizing the keeper transistors. It enables reduced clock-swing operation as well as logic integration inside the flip-flop. Additionally, just one transistor being active during the changeover improves the output stage's capacity to drive other transistors and prevents crowbar current, which lowers power consumption.

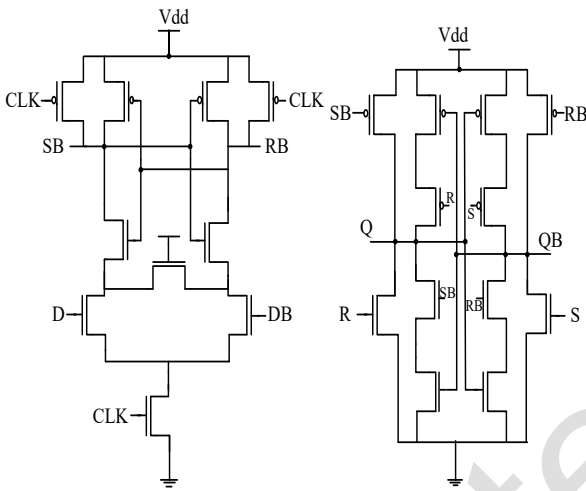


Figure 4: Architecture of Nikolic's FF [17]

Kim proposed a SAFF in [18] with updated N-C2MOS latches shown in Fig. 5. The sense amplifier is the same as it was in the conventional SAFF. Since the coupled inverters are constructed using transistors of the smallest possible size, the additional capacitive loadings they cause at the output nodes are insignificant (less than 10% of the total capacitance value). The differential output nodes are completely separated, therefore the load capacitance at the other output node does not affect the transition speed of one output node.

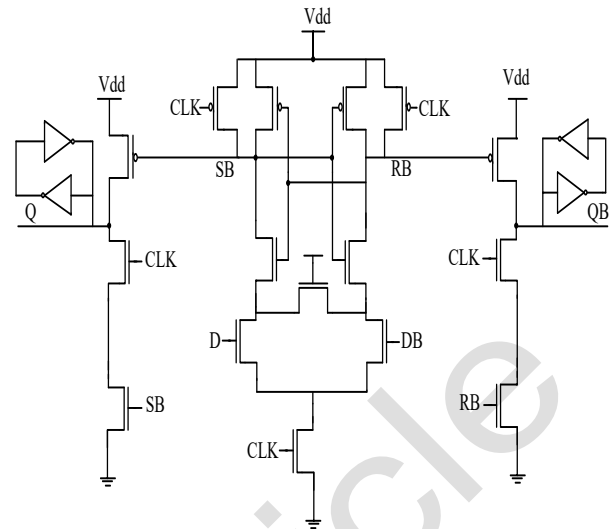


Figure 5: Architecture of Kim's FF [18]

3 Proposed SAFF

Fig. 6 shows the architecture of proposed SAFF. An input/output structure with a novel sense amplifier design and a single-ended pass transistor logic-based latch is used. This design optimization technique helps the leading sense-amplifier stage's transistor size requirement be reduced. The resulting design is more efficient than traditional designs in terms of layout and performance. A real single-ended latch is used to overcome the shortcoming of the dynamic latch. This improves the speed and power performances by significantly reducing the loading effect on the sensing amplifier. To create signal S from the output signal SB of the sense amplifier, an additional inverter INV₁ is introduced. Signal RB is in the interim removed from the latch design's list of inputs. This results in a genuine single-ended latch circuit as depicted in Fig. 6.

The operation of the FF can be realized as when clock signal is low, both the outputs of sensing stage RB and SB are precharged to logic '1', transistors N₁ and N₂ are turned ON, X stays low during the '0-1' transition of clock. During this, the latching stage maintains the state of the flip-flop. At the time when clock changes to '1', the sense amplifier stage starts the transition. One of RB or SB will drop if the shift is successful, raising X. Because of the connection between X and the transistor associated with it remains OFF during the sensing stage transition and is only turned ON when the sensing stage transition is over (i.e one of the precharged node is either brought down to low logic via by transistor N₁ or N₂ whereas the other precharged node continues to be at logic high). Therefore both the operational yield and speed loss of this transistor is not present as compared in the sense amplifiers discussed in previous sections.

Remember that as soon as the sensing stage swings, either N1 or N2 will switch off, and as a result, any further change in input will not be able to affect the state of the reset and set terminals. The transistor N7 adds better power efficiency to the FF at the cost of small delay. Nevertheless this small delay is compensated by the latching stage's single-ended structure.

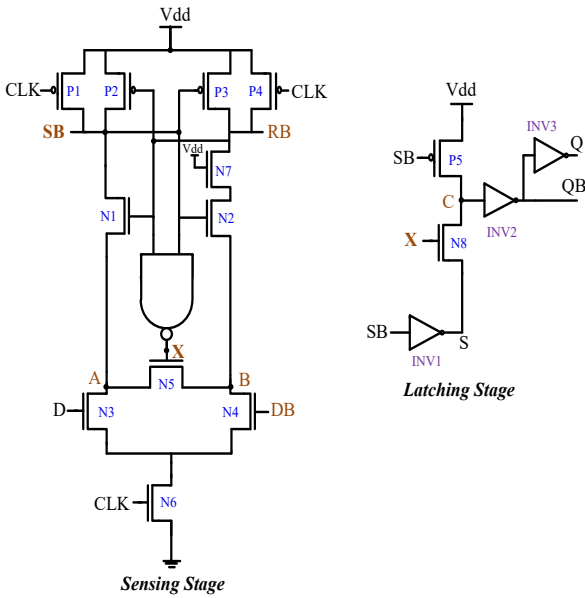


Figure 6: Proposed SAFF

When the clock is low (precharge state), the fact that two nodes A and B are not equalized is another notable aspect of this design. Also at the rising edge of clock, the voltages at the nodes A and B are the same which lessen the effect of mismatch. Conversely, the proposed design has the potential for nodes A and B to diverge at the rising edge of the clock, in turn may reduce the stability of the sensing stage. Nevertheless, the beneficial impact obtained by turning OFF the transistor while high clock outweighs the unfavorable impact of node "A" equal to "B".

For the latch of the proposed design the signal X produced in the sensing stage is applied in place of the global clock. The signal RB is not present in the latching stage since it has a single-ended form. If the input signal data D is low at the rising edges of the clock, SB will remain at operating voltage, and node C will be discharged to low through transistor N8. The transistor P5 will switch ON if the input data D is high, in a similar manner to how node SB will discharge to low if D is high. Now, transistors P5 and N8 together are pulling Node C to operating voltage. The outputs QB and Q are driven by two inverters that are coupled at node C. The operational waveforms in Fig. 7 corroborate and make clear this entire process.

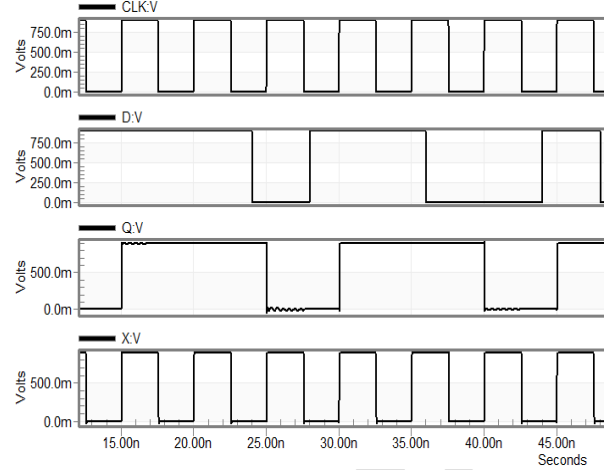


Figure 7: Transient waveform of proposed FF

The transistor size of the proposed SAFF is listed in Table 1. The sizes of N3 and N6 are selected to be larger because it controls the performance of the FF since it directly influences the pull down speed of SB. The single-ended structure of the SAFF latch stage allows transistors N2, N4, and N7 to be of minimal size. In addition, since the load on RB is "o" than that on SB, reducing the widths of the transistors N2, N4, and N7 may stabilize the pull down operations on SB. This leads in a shorter hold and setup time for the proposed SAFF. The standard sizes of the transistors are maintained at the latching stage for P5 and N8. Since the inverter's driving capabilities are unnecessary, the size of the inverter transistors can be minimized, resulting in significant power savings.

Table 1: Transistor size of proposed SAFF

Component	W (nm)	Component	W (nm)
P1-P5	320	N6	800
N1, N2, N4, N5, N7 & N8	160	P (Inv1-Inv3)	320
N3	320	N (Inv1-Inv3)	160

4 Simulation results & discussions

The proposed architecture is tested with available designs to show its competitiveness and performance. The simulations are carried out at 32 nm CMOS technology node in SPICE using PTM models [19]. The nominal working parameters are 25 °C temperature, 200 MHz frequency and 0.9 V operating voltage. A 16-bit input data is used with data activity of 50%.

The simulation results for power consumption at supply voltage variation between 0.5 V to 1.1 V and at variations in temperature from 0 °C to 100 °C are shown in

Fig. 8. This figure makes it very clear that, for all the variations considered in this paper, the proposed design consumes the least amount of power at various voltage levels and temperature changes.

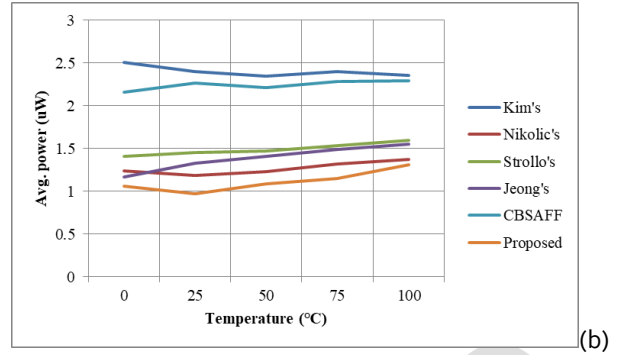
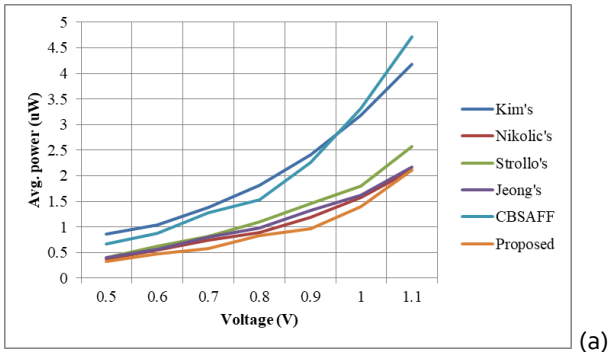


Figure 8: Average power at variations in (a) Voltage (b) Temperature

Table 2 is the detailed comparison of proposed sense amplifier based flip flop with existing FFs. It includes the layout area, the clock to Q delay and the power delay product at variations in supply voltage. It was observed that at nominal operating conditions, Jeong's FF was the fastest followed by Strollo's FF. The proposed flip flop was third fastest but nearly comparable to its rivals. When power and delay both were taken into account, the proposed flip flop showed better results. The PDP at three different voltage variations of 0.7 V, 0.8 V and 0.9 V showcases the worthiness of proposed design for portable power efficient devices.

Table 2: Performance comparison of flip-flops.

Flip Flop	Layout area (um ²)	No. of Transistors	PDP @0.7 V (uW)	PDP @0.8 V (uW)	PDP @0.9 V (uW)	C-Q delay @0.9 V (ps)
Kim's	0.352	26	62.971	66.685	72.239	30.065
Nikolic's	0.262	28	34.061	26.155	31.431	26.408
Strollo's	0.279	23	26.673	24.898	24.693	16.948
Jeong's	0.247	26	33.916	27.874	17.84	13.424
CBSAFF	0.316	38	159.698	70.594	127.457	56.22
Proposed	0.209	25	23.325	21.134	18.666	19.266

Although in terms of number of transistors the proposed design has second least count but the overall layout area of the proposed design is smaller compared to any other design. This difference and area advantage of proposed design can be seen in Fig. 9.

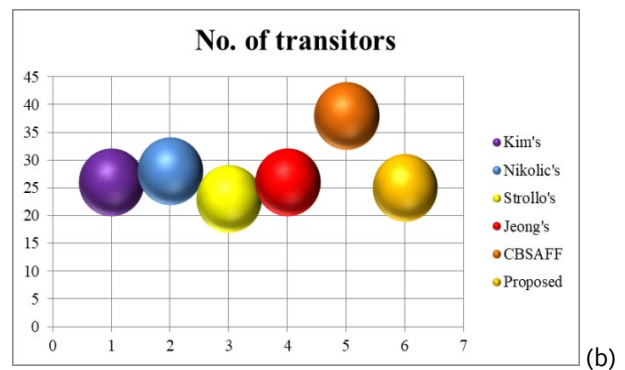
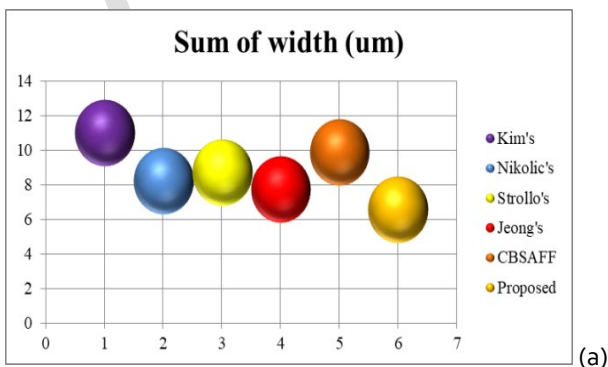


Figure 9: Area requirements (a) Sum of width (b) Number of transistors

In any VLSI design, it is important to know the effect of process, voltage and temperature variations at extreme

corners. This test was conducted with corner cases of FS 0.9 V /25 °C, SF 0.9 V /25 °C, TT 0.9 V /25 °C, SS 0.8 V /125 °C and FF 1.1 V /-40 °C. The power results of proposed design at all extreme corners were far better than its counterparts. These corner results are shown in Fig. 10.

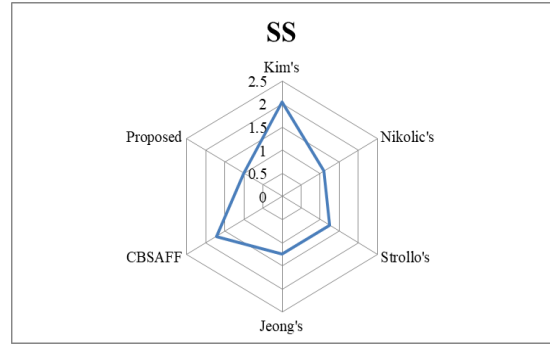
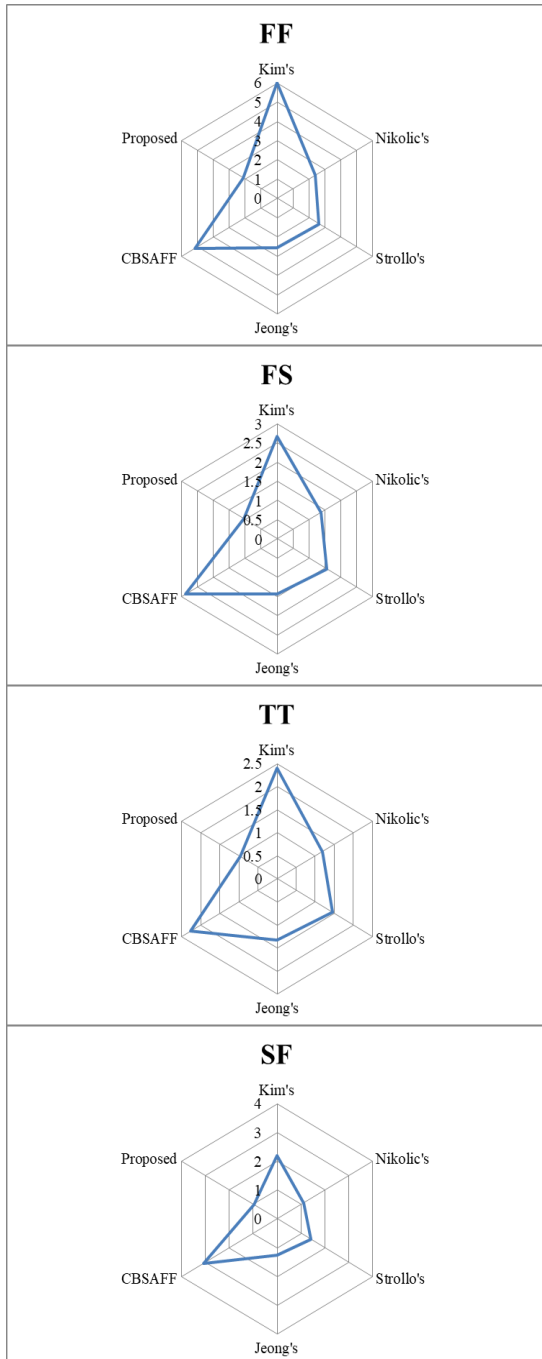


Figure 10: Corner case analysis

Fig. 11 is the power results at variations in data activity. Wide variation in input data from 0% to 100% was taken into account. For 0% both all input high and all input low were obtained. This test was conducted at two different frequencies i.e. at 100 MHz and 200 MHz. Results in Fig. 11(a) and 11(b) showcases the proposed design's superiority over other designs at all trails.

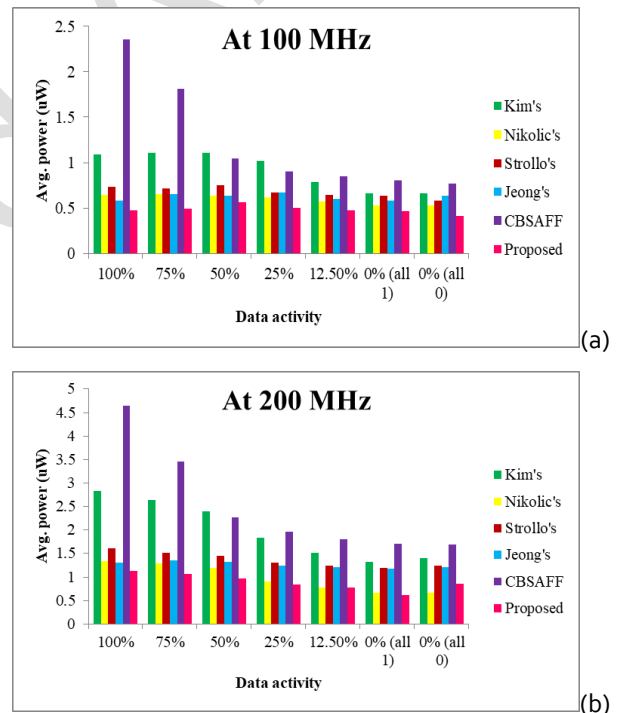


Figure 11: Average power at variation in data activity (a) at 100 MHz (b) at 200 MHz.

Simulations so far have shown that the proposed design is resilient, however, additional testing is conducted against changes in voltages for the near-threshold to sub-threshold range along with the effects of a wide range of temperatures. To test this, Monte Carlo simulations are conducted with aggressive voltage scaling across the range of 0.3 V to 0.5 V with 0.02 V increments (20 mV) and over the range of temperature with 10 °C

steps from -40 °C to 120 °C. The results of the tests performed on all of the flip-flops are shown in Figure 12. A 'pass' case test is represented by a green box, while a 'fail' case test is represented by a red box. Kim's FF was the only one to pass all of the tests, followed by CBSAFF with 2 fail instances and Strollo's FF with 6 fail cases. Notably, neither Kim's FF nor the CBSAFF performed well throughout the analysis. In addition, the proposed SAFF has also restricted functioning when subjected to sub-threshold voltage levels and temperature ranges and is therefore recommended for use at voltage levels of more than 0.34 V.

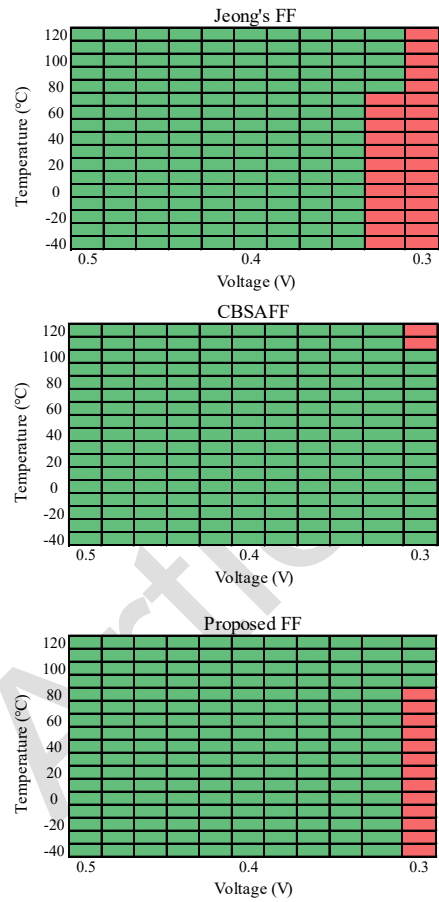
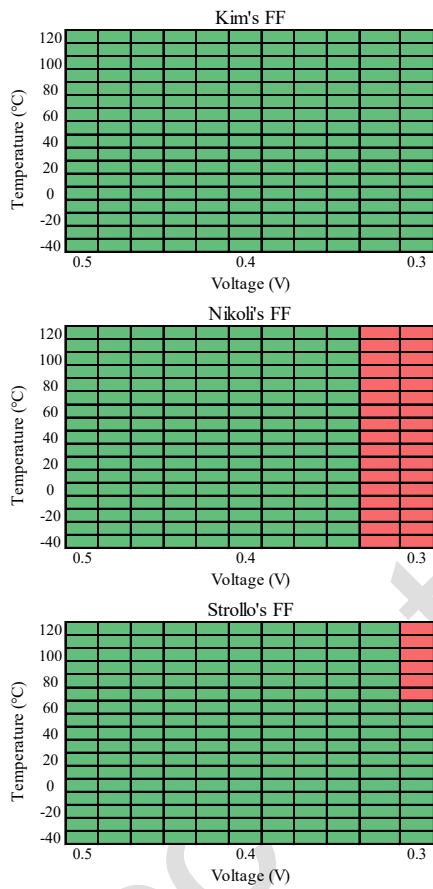


Figure 12: Results of aggressive temperature and voltage scaling (Green: Pass-case; Red: Fail-case)

5 Experimental verification

In order to illustrate and validate the correct logical operation and power performance of the proposed design, the proposed SAFF is tested for use in complex digital circuitries. The flip-flop under test (FUT) was evaluated as a four-bit shift register and a three-bit counter in simulation settings under the nominal conditions of 25 °C temperature, 0.9 V supply voltage, and 200 MHz frequency. Figure 13 are the transient waveforms of these tests thereby demonstrating the correct circuit functionality of the proposed design.

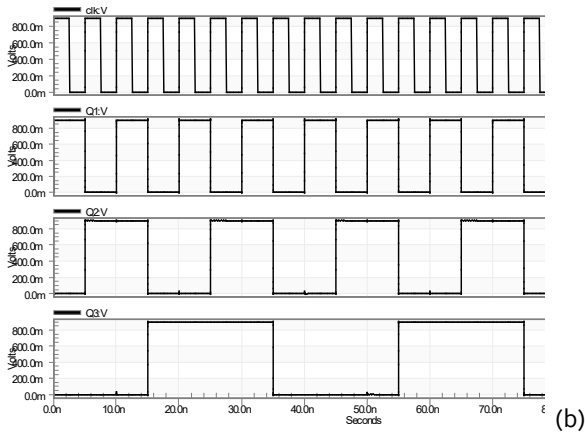
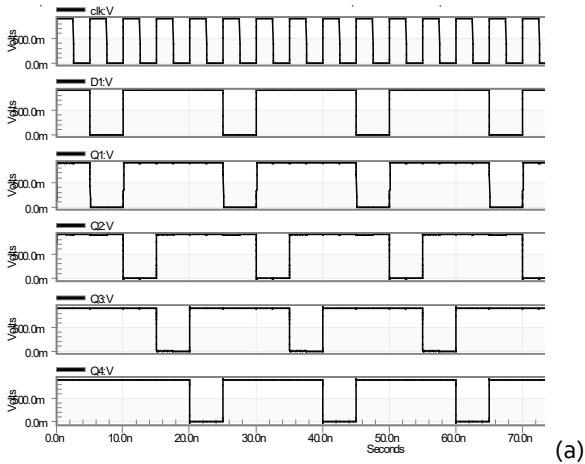


Figure 13: Transient waveform of proposed FUT as (a) 4-bit shift register (b) 3-bit counter

The test was also conducted on existing FFs to determine and compare the power performance of all the designs. The average power was determined at voltages of 0.8 V, 0.9 V and 1 V and at variations in temperature of -40 °C, 25 °C and 125 °C. Figure 14 and 15 shows the results obtained from these tests, the proposed FUT demonstrated better power performance at all conducted tests and therefore is worthy of consideration in designs requiring low power operations.

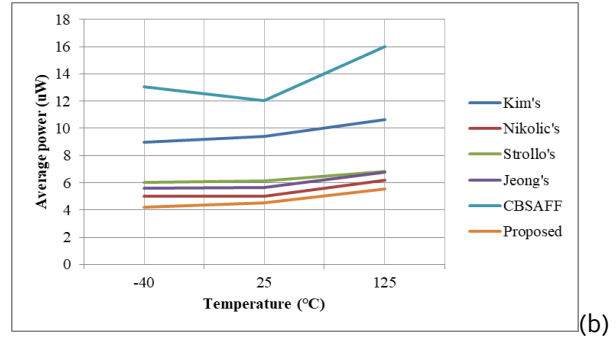
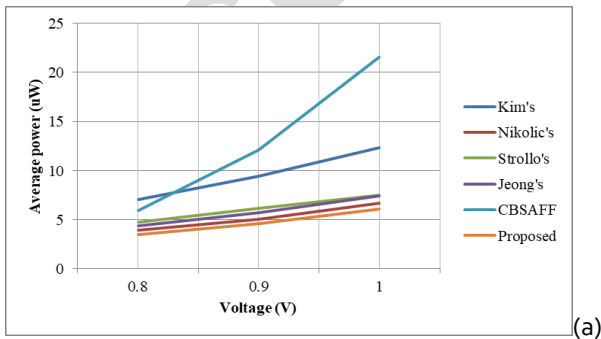


Figure 14: Power results of shift register at variation in (a) voltage (b) temperature

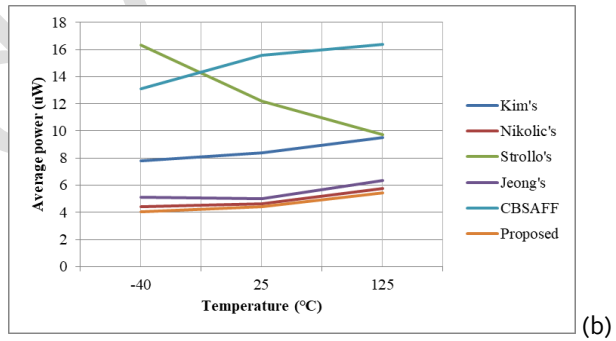
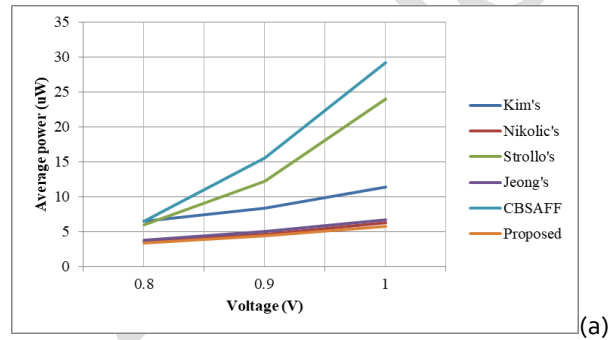


Figure 15: Power results of counter at variation in (a) voltage (b) temperature

6 Conclusion

A modified sensing stage is used to create a sense amplifier based flip flop. The major goal was to reduce power consumption so that the proposed flip flop will be a viable option for digital circuits and IoT applications. After comprehensive simulations, the proposed design excelled practically all other designs in metrics like as average power, PDP, data activity, and in especially layout area. The proposed design also upheld the voltage variation of 0.5 V to 1.1 V and corner case temperature variation of -40 °C to 120 °C. Further advantage of the novel design includes the power efficiency at input data activity variation. In addition, the proposed FF is recommended for designs with minimum voltage of 0.34 V.

7 Conflict of Interest

The authors declare no conflict of interest.

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