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New Approach in Physical Failure Analysis Based on 3D Reconstruction

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Abstract

In this work we present a new approach in physical failure analysis. Fault isolation can be done using volume diagnosis techniques. But when studying the identified defect sites by Focused Ion Beam (FIB) cross-sectioning, correct interpretation of the cross-sectional views strongly relies on choosing an appropriate cutting strategy. However, volume diagnosis techniques do not provide any information on which cutting directions and settings to choose to avoid misinterpretation of the spatial evolution of the defects. The proposed approach is to acquire FIB-SEM tomographic datasets at the defect sites to unequivocally characterize the defects in three-dimensional visualizations, independent of particular cross-sectioning strategies. In this specific case we have applied the methodology at a microcontroller for automotive applications on which a couple of floating VIAS were found. Thanks to the complete information obtained with the tomography, the defect could be assigned to a specific class of etching tools, and the root cause thus be solved

Introduction

The automotive electronics in a modern car is a network of complex systems that impact not only the entertainment activity such as multimedia player, satellite navigator, or telephone connection but also engine management, ignition, carcomputer, telematics and, highly important, all the safety systems. Most of these innovations are due to the massive use of microcontrollers. The increased automation has created a huge demand for such microcontrollers. Growing electrification along with several rules and regulations toward automotive safety and security adopted by different governments across the globe is expected to sustain the growth of the automotive microcontroller market.

The technology used in microcontrollers are designed to ensure smooth management through digital logic of various advanced components in vehicles. Unfortunately, the increase in the complexity of the devices leads to an increase in the difficulty in localizing any physical defects that may affect the operation of the device. This is an essential task not only on finished products (failure analysis) but also and above all at the production level in order to be able to catch and correct any process deviations in time (yield enhancement).

A very powerful tool to isolate the defect in the logic block is called volume diagnosis [1]. By cross-correlation of electrical tests, it can identify the potentially failing NETs. The following Physical Failure Analysis (PFA) is performed by FIB-SEM, and starts by alignment of the top surface of the sample with the CAD layout (for this reason, an initial delayering to better identify the top layer is often required). On the cells or NETs of interest, normally we proceed by progressive cross-sectioning using FIB until the defect is identified. However, because we do not know the position and the nature of the defect in the NET, we cannot determine in advance the most appropriate cutting direction to observe it. For this reason, often the resulting cross-sectional SEM images are not conclusive for identifying the defect root cause.



Figure 1 The bottom row shows SEM views of a defect cross-sectioned in two different directions indicated in the top row images a and b.

In Fig. 1, a typical example of this problem is shown. In particular, in Fig. 1a the defect is exposed in the cut direction. We can see the final part of the metal strip before the contact. Immediately after that the contact appears. In Fig. 1b the same defect is shown but cut and observed from a direction rotated 90° . From this perspective, it cannot be seen that there is actually no connection between the metal strip and the contact. It is immediately clear that a good study of the evolution of the defect is strongly related to the cross-section direction. To avoid

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this problem, in the past we have used techniques of 3D reconstructing of the area of analysis [2], achieving excellent results.

In this work we will show advanced fault isolations and FIB 3D reconstruction strategies applied to a Microcontroller based on 0.16 μ m technology platform, dedicated to Automotive Smart Power applications and build on 8-inch wafers. The wafers used showed generic failures in the logic part already from the Electrical Wafer Sort (EWS) test. In particular we have extended this complex methodology to larger volumes, and we are using a more accurate procedure to obtain 3D visualizations that unequivocally show the defect and give us information about its nature and morphology from all required perspectives.

Experimental

The Volume Diagnosis analysis was done using Synopsys Yield Explorer, Avalon and TetraMax. Based on electrical test performed with T2000 model of Advantest LSMF (52 slots).

The 3D data acquisition was done using a ZEISS Crossbeam 550L FIB-SEM instrument equipped with a Gemini 2 SEM column and Ion Sculpture Ga-FIB column. ATLAS 5 software with the Atlas 3D Software module was used to support data acquisition [3].

3D imaging reconstruction, segmentation and visualization of the data was performed using the ORS DragonFly Pro Workstation (Version 2022.1 Build 1259).

Results and Discussion

Fault Localization

Nowadays, most of SoC available on market are fabricated following the BCD concept, invented by STMicroelectronics in the mid-80s [4-6], which include in one chip Bipolar (for precise analog functions), CMOS (for dense DIGITAL design), and DMOS (for robust HIGH VOLTAGE & POWER devices). The mixed processes that allow to integrate these different transistor technologies into a single chip form a new power device class called SMART POWER devices. Since logic represents the largest part of this kind of devices, SCAN is one of the main yield detractors. For this reason, a digital logic testing methodology which uses Automated Test Pattern Generator (ATPG) is widely used for designs verification. Diagnostic results provided by Design for Testing (DFT) structures, stimulated by ATPG, allows to identify failed nets or cells causing yield losses. TetraMax by Synopsys is the most used tool for generating minimum test patterns possible with maximum test coverage for a wide range of designs. Diagnosis methodology is used to identify the root cause of the failures produced by all scan patterns:

• In volume (one or more wafers) to identify a common root cause between the various parts (systematic defects)

• On few parts (reliability, customer return) to localize a physical defect on a single part the [7].

Since volume diagnostics highlights correlation between electrical fault detected during EWS test and manufacturing design pattern, it is a very powerful tool for advanced fault isolation [1]. Volume diagnostics flow can be summarized in two important steps: a) identification of failure candidates using logical netlist, physical layout and fault simulation (stucks, bridges, transition, cell aware); b) statistical analysis of the failure candidates correlated to the critical design patterns.

At the end of the flow, a collection of candidates with no more than one or two candidates for defects and a high probability to catch physical defect are available. Focusing on these candidates, the most promising ones are selected for PFA based on length failing NET involved, fault type (stuck at is usually preferred to other fault type typically more complex) or simple component failure occurrence.

In order to reduce electrical yield losses in smart power devices, discovering failure root cause of scan fails is fundamental. Scan fails can be distributed with a particular signature on electrical wafer map that can indicate a specific manufacturing process step, or they can be randomly distributed. In this case, volume diagnostics play a key role in the identification of scan fails and their nature, potentially allowing reduction of baseline defectivity.



Figure 2 EWS map of wafer under study in which brown dice reported are SCAN fails.

The wafer under study is represented inFigure 2, where the failing devices are shown in brown. To perform volume diagnostic, Yield explorer was used. Tetramax analysis carried out a total of 16 candidates with no more than one or two candidates for defects and high probability to catch physical defect as source of scan fail. After this step, these candidates were filtered to select a few that exhibited smaller physical area and lower length failing NET involved, fault type ('stuck at' is usually preferred to other fault type typically more complex) or simple component failure occurrence. Figure 3 shows an example of one candidate for PFA. In particular, inFigure 3a the

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whole NET is shown. InFigure 3b the detail in which the suspected defect location is highlighted with a red line. InFigure 3c the structure of the previous location is illustrated.

Data acquisition

After a delayering the sample to expose the topmost metal layer visible in the FIB, the candidate NET was transferred to Avalon and aligned with the SEM image as shown in Figure 4.



Figure 3 Layout of the candidate NET used for 3D analysis. The suspected defect location is marked by a red circle.



Figure 4 Layout of the candidate area overlaid to a FIB image of the matching area on the sample.



Figure 5 starting platinum deposition step with fiducial lines on top.

A platinum layer of $10 \times 10 \times 1 \mu m^3$ was ion beam deposited on top of that area. A set of diagonal and straight lines was FIB cut into the platinum layer, as visible inFigure 5. Then it was covered by an ion beam deposited carbon layer of $10 \times 10 \times$ $1 \mu m^3$ size. A large trench was FIB milled in front of the volume of interest to make it accessible for the subsequent repeated slice milling with the FIB and imaging with the SEM (seeFigure 6).



Figure 6 Same area after preparation and before starting the data acquisition observed by ion column (a). The platinum/carbon deposition sandwich with embedded fiducial lines is visible in crosssection by SEM (b).



Figure 7 image acquired during slicing phase in which the area of interest is signed with a red rectangle (a). extraction after alignment of SE (b) and BSE images (c).

Slight slice thickness variations and lateral drifts during data acquisition are unavoidable and would eventually lead to distortions of the sample structures in the 3D visualization. Therefore, the mentioned lines serve as fiducials for measurement and dynamic correction of slice thickness during data acquisition, as well as for correction of lateral drift and for

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periodic electron beam tuning [3] (Fig. 6). A pixel size of 10nm and a slice thickness target of 10 nm were set for the data acquisition. The total acquisition time was approximately 7h. A fine alignment to remove residual image to image drifts was then made with the dataset, and it was interpolated to a constant slice thickness of exactly 10 nm using the slice thicknesses measured during acquisition. The final dataset consisted of 758 images, covering a volume of $10.9 \times 4.1 \times 7.6\mu m^3$ at $(10 nm)^3$ voxel size.

During the acquisition phase, the Atlas software simultaneously recorded secondary electron images with the in-lens SE detector, and high angle backscattered electron images with the energy-elective in-column BSE detector. Focus and astigmatism were periodically and automatically corrected. In Figure 7a, the whole picture acquired during the slicing phase is shown. At the end of the acquisition phase, the software ATLAS extracted the content of in interest area (red rectangle in Figure 7a, and performed a first rough alignment for both channel (SEFigure 7b and BSEFigure 7c). This data set was then ready for subsequent 3D reconstruction

3D Reconstruction

The 3D dataset was processed using Dragonfly Pro. A Non-Local Means filter (Kernel size 21, Smoothing 0,50) was applied to remove the noise from the input images preserving the sharpness of strong edges. The stack was aligned using an SSD registration method with a small maximum translation. Figure 8 shows a 3D visualization of this dataset in which the ILD has been faded out to display only the metal interconnects and vias. Two incomplete vias, segmented in blue, that are not landing on the interconnect underneath can be clearly discerned in the volume of interest (VOI) delimited by the red box and place in the center of the 3D model. In the conventional FA approach of cutting a single FIB cross-section, there would have been a high likelihood of already stopping the analysis once the first incomplete via had been found, thus overlooking the second one. Figure 8 shows an example for such analysis that can provide the process engineer with direct feedback on the exact nature and location of a defect. Moreover, the segmentation of every metal layer (from the bottom to the top: green, yellow, purple, red) was carried out for a three-dimensional investigation (see Fig. 10a). After the histogram-based segmentation, every region of interest (ROI) was refined manually and using a *process island* workflow. The results are reported in Fig. 10a-b where every metal layer routing can be appreciated separately in 2D/3D.



Figure 9 Two virtual horizontal slices extracted from the dataset, with the matching CAD layout section overlaid. The slice shown on the left was extracted at the height of the top quarter of the vias, the slice on the right at their bottom quarter. The vias are visible in their horizontal cross-section as bright discs.

Extracting virtual slices from the 3D dataset and overlaying them with the matching layers from the CAD layout, a more detailed comparison of the target state and the actual, defective state of the NET is possible, as shown in Fig. 9. Results carried out from this study allowed to device engineers understanding of failure mechanism and equipment which enhanced this kind of fails. In this specific case it was correlated at a specific class of etching tool that exhibit poor performances for this kind of technology. The problem was immediately solved changing the tools that perform the etching at the first level of VIAS.



Figure 8: 3D visualization of the dataset acquired, showing the metal interconnects and vias. In the center of the image, two incomplete vias are visible.

References



[1] J. C. Le Denmat, *et al.*, "Fast detection of manufacturing systematic design pattern failures causing device yield loss" *SPIE*

[2] D. Mello, *et al.*, "Advanced strategy for in-line process monitoring using FIB and TEM" *Nuclear Instruments and Methods in Physics Research B* 257 (2007) 805–809. doi: 10.1016/j.nimb.2007.01.113

[3] M.W. Phaneuf and K.G. Lagarec, "*Microscopy imaging method and system*", U.S. patent 9812290B2.

[4] Single Chip Carries Three technologies, Electronics Week, December 10, 1984

[5] C. Cini, C. Contiero, C. Diazzi, P. Galbiati, D. Rossi, "A New Bipolar, CMOS, DMOS Mixed Technology for Intelligent Power Applications", ESSDERC '85 Proceedings, Aachen (Germany), September 1985

[6] A. Andreini, C. Contiero, P. Galbiati, "A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic and DMOS Power Parts", IEEE Transactions on Electron Devices, Vol. ED-33 No.12, December 1986

[7] E. Auvray, "Evolution of navigation and simulation tools in failure analysis" Conference: ESREF (2016)



Conclusions

We are proposing to use FIB-SEM tomography as a tool for characterization of defect sites that were identified by volume diagnosis techniques. As we have shown with a practical example, this approach avoids misinterpretation of conventional cross-sectioning imaging of defect sites and provides process engineers with results they can directly interpret and compare to the target layout.

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