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# Structural advantages of rectangular-like channel cross-section on electrical characteristics of silicon nanowire field-effect transistors

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## Abstract

We have experimentally demonstrated structural advantages due to rounded corners of rectangular-like cross-section of silicon nanowire (SiNW) field-effect transistors (FETs) on on-current ( $I_{ON}$ ), inversion charge density normalized by a peripheral length of channel cross-section ( $Q_{inv}$ ) and effective carrier mobility ( $\mu_{eff}$ ). The  $I_{ON}$  was evaluated at the overdrive voltage ( $V_{OV}$ ) of 1.0 V, which is the difference between gate voltage ( $V_g$ ) and the threshold voltage ( $V_{th}$ ), and at the drain voltage of 1.0 V. The SiNW nFETs have revealed high  $I_{ON}$  of 1600  $\mu\text{A}/\mu\text{m}$  of the channel width ( $w_{NW}$ ) of 19 nm and height ( $h_{NW}$ ) of 12 nm with the gate length ( $L_g$ ) of 65 nm. We have separated the amount of on-current per wire at  $V_{OV} = 1.0$  V to a corner component and a flat surface component, and the contribution of the corners was nearly 60 % of the total  $I_{ON}$  of the SiNW nFET with  $L_g$  of 65 nm. Higher  $Q_{inv}$  at  $V_{OV} = 1.0$  V evaluated by advanced split-CV method was obtained with narrower SiNW FET, and it has been revealed the amount of inversion charge near corners occupied 50 % of all the amount of inversion charge of the SiNW FET ( $w_{NW} = 19$  nm and  $h_{NW} = 12$  nm). We also obtained high  $\mu_{eff}$  of the SiNW FETs compared with that of SOI planar nFETs. The  $\mu_{eff}$  at the corners of SiNW FET has been calculated with the separated amount of inversion charge and drain conductance. Higher  $\mu_{eff}$  around corners is obtained than the original  $\mu_{eff}$  of the SiNW nFETs. The higher  $\mu_{eff}$  and the large fractions of  $I_{ON}$  and  $Q_{inv}$  around the corners indicate that the rounded corners of rectangular-like cross-sections play important roles on the enhancement of the electrical performance of the SiNW nFETs.

37 **Key words:** silicon on insulator, silicon nanowire, rectangular-like cross-section, on-current,  
38 split-CV, inversion charge density, effective carrier mobility.

39

## 40 **1. Introduction**

41 Aggressive scaling of the planar metal-oxide-semiconductor field-effect transistors (MOSFET)  
42 has encountered difficulties with suppression of the short channel effects (SCE), which induces an  
43 increase in off-state leakage current ( $I_{OFF}$ ) to degrade the on-current/off-current ratio ( $I_{ON}/I_{OFF}$ ). A  
44 solution to suppress the SCE is an introduction of three-dimensional channel FETs for enhancement  
45 of the electrostatic controllability of the channel. Silicon nanowire (SiNW) FETs have the most  
46 effective channel controllability and nearly ideal off-characteristics have been experimentally  
47 demonstrated [1].  $I_{ON}$  enhancement of the SiNW FET has also been reported [2]. Higher  $I_{ON}$  with  
48 lower  $I_{OFF}$  is advantageous for realization of a low power supply voltage device and thus a low  
49 power consumption device application. The  $I_{ON}$  is mainly attributed to the inversion charge density  
50 ( $Q_{inv}$ ) and effective carrier mobility ( $\mu_{eff}$ ) of the SiNW channel. The  $\mu_{eff}$  of SiNW FET has been  
51 investigated in many institutes [3-5] and mainly focused on the surface orientations of the SiNW  
52 channel. We focused on structural effects of the SiNW channel on the electrical performance of  
53 SiNW FETs. In this work we fabricated the SiNW FETs with rectangular-like channel cross-section  
54 and planar SOI FETs on (100) SOI wafer simultaneously and electrically characterized, especially  
55 the  $I_{ON}$ ,  $\mu_{eff}$  and  $Q_{inv}$ . We intensively analyzed structural advantages of rectangular cross-section  
56 SiNW FET. Experimental results suggested that corners in the rectangular cross-section played  
57 important roles on the enhancement of the electrical performances of the SiNW nFETs.

58

## 59 **2. Device fabrication process**

60 A (100)-oriented silicon-on-insulator (SOI) wafer was used as a starting material with the SOI  
61 layer and the buried oxide (BOX) layer thickness of 75 and 50 nm, respectively. The mesa-type Si  
62 fin with embedded source and drain (S/D) pad region with a silicon nitride hard mask of 50 nm  
63 formed by the low-pressure chemical vapor deposition on an oxide pad layer of 7 nm atop was  
64 oxidized in dry oxygen ambient at 1000 °C for 1 hour to form narrow SiNW channel. The silicon  
65 nitride layer prevents the oxidation and the resultant reduction of the SOI layer thickness of S/D  
66 region to avoid an unexpected increase in parasitic series resistance ( $R_{SD}$ ). The sacrificial oxide was  
67 partially stripped by wet etching process and silicon nitride sidewalls were formed by deposition and  
68 etch-back process. The residual oxide was completely stripped, and the SiO<sub>2</sub> gate oxide with a  
69 thickness ( $T_{ox}$ ) of 3 nm and a non-doped poly-silicon film of 75 nm was deposited, which resulted in  
70 a trigate-like gate semi-around structure [6]. After gate ion implantation process (phosphorus for  
71 nFETs and boron for pFETs), silicon dioxide hard mask deposited by chemical-vapor deposition  
72 with tetraethoxysilane (TEOS) of 30 nm was formed. Dry ArF lithography process and dry etching

73 process with TEOS hard mask was used to form gate electrode. After the poly-Si gate electrode  
74 formation, the 1<sup>st</sup> spacer formation and the ion implantation were performed (arsenic (15 keV) for  
75 the SiNW nFET with the channel width  $w_{NW}$  of 9 nm, and phosphorus (5 keV) for the SiNW nFETs  
76 with  $w_{NW}$  of 19, 28, and 39 nm and the planar SOI nFETs, and boron (4 keV) for pFETs) at the dose  
77 of  $1 \times 10^{15} \text{ cm}^{-2}$ . The 2<sup>nd</sup> spacer formation and the deep S/D ion implantation were performed (arsenic  
78 (20 keV) for the SiNW nFET with the channel width  $w_{NW}$  of 9 nm, and phosphorus (5 keV) for the  
79 SiNW nFETs with  $w_{NW}$  of 19, 28, and 39 nm and the planar SOI nFETs, and boron (4 keV) for  
80 pFETs) at the dose of  $5 \times 10^{15} \text{ cm}^{-2}$ . After a spike rapid thermal annealing process for an activation of  
81 the implanted dopants, a self-align nickel silicidation process was performed. An excessive  
82 silicidation of SiNW channel was not observed due to optimized process conditions [7, 8]. Post  
83 metallization dielectric with the thickness of 470 nm was deposited and finally the wafer was  
84 sintered in forming gas ambience. The schematic process flow is shown in **figure 1**. A review  
85 scanning electron microscope (SEM) image of the SiNW FETs with the gate length  $L_g$  of 65 nm and  
86 cross-sectional transmission electron microscope (TEM) images of SiNW channels are shown in  
87 **figure 2**. As the SiNW channel was formed by thermal oxidation in high-temperature, the corners  
88 have rounded shape [9]. The radius of corners ( $W_c$ ) of sample A and B is 4 nm, whereas 6.5 nm of  
89 sample C based on the TEM images. The channel height ( $h_{NW}$ ) and width ( $w_{NW}$ ) in cross-section are  
90 summarized in the inset in the **figure 2**.

## 92 3. Results

### 93 3.1 Dc-characteristics of SiNW FETs

94 Typical output and transfer characteristics of the SiNW FETs ( $w_{NW}=19 \text{ nm}$  and  $h_{NW}=12 \text{ nm}$ ) with  
95 the  $L_g$  of 65 nm and the  $T_{ox}$  of 3 nm are shown in **figure 3**. A well-behaved transistor operation was  
96 confirmed for the both SiNW nFETs and pFETs. The on-current per wire of the SiNW nFET  
97 ( $w_{NW}=19 \text{ nm}$  and  $h_{NW}=12 \text{ nm}$ ) was as high as  $60 \mu\text{A}$ , whereas  $22 \mu\text{A}$  of the SiNW pFETs of the same  
98 size was obtained. Although the SiNW FETs have corners in the rectangular-like cross-sectional  
99 shape, no kink was observed in the transfer characteristics, which might be due to low-doped SiNW  
100 channel [10]. Large on-off current ratio ( $I_{on}/I_{off}$ ) of  $>10^6$  with the drain induced barrier lowering  
101 (DIBL) and the subthreshold swing (S.S.) of 62 mV/V and 70 mV/dec., for the SiNW nFETs have  
102 been obtained. We can observe saturation region clearly in output characteristics of nFETs, which  
103 suggests low  $R_{SD}$ . Sufficiently low S. S. indicates that interfacial state density ( $D_{it}$ ) of SiNW FET  
104 with rectangular-like cross-section is negligible.

### 106 3.2 On-current of SiNW FETs

107 On-currents normalized by a peripheral length, which is a total length of top and side channels of  
108 SiNW cross-section, ( $I_{ON}$ ) of SiNW nFETs with the gate length from 500 to 65 nm were measured

109 and summarized in the **figure 4(a)**. The on-current per wire was extracted at the overdrive voltage  
110  $V_{OV} = 1.0$  V, which is a difference of a gate voltage ( $V_g$ ) and a threshold voltage ( $V_{th}$ ), and drain  
111 voltage  $|V_d|=1.0$  V. As the  $w_{NW}$  increases on-current per wire was also increased. After  
112 normalization of on-current per wire by the peripheral length of channel, the largest  $I_{ON}$  of the  
113 narrowest SiNW nFET ( $w_{NW}=19$  nm and  $h_{NW}=12$  nm) was obtained. Among these, SiNW nFETs  
114 ( $w_{NW}=19$  nm and  $h_{NW}=12$  nm) showed excellent high  $I_{ON}$  of  $1600 \mu A/\mu m$ . The  $I_{ON}$  of SiNW pFETs  
115 with the gate length from 500 to 65 nm are also shown in **figure 4(b)**. The structural advantages of  
116 SiNW nFETs on the  $I_{ON}$  drivability is summarized in **figure 5**. Higher  $I_{ON}$  was obtained with smaller  
117  $w_{NW}$  in each gate length and exceeds the  $I_{ON}$  of planar SOI nFETs, which suggests that the smaller  
118  $w_{NW}$  is advantageous to  $I_{ON}$  drivability between the  $w_{NW}$  of 19 and 39 nm.

119  $I_{ON}/I_{OFF}$  characteristics of SiNW nFETs are shown in **figure 6**. The  $I_{OFF}$  was defined as the drain  
120 current normalized by the peripheral length of SiNW channel at the  $V_g-V_{th}$  of  $-0.3$  V and drain  
121 voltage ( $V_d$ ) of  $1.0$  V. The SiNW nFET with narrower  $w_{NW}$  demonstrates superior  $I_{ON}/I_{OFF}$   
122 characteristics, especially significantly improved  $I_{ON}/I_{OFF}$  in short  $L_g$  region due to electrostatic  
123 controllability of the narrow SiNW channel.

124 Parasitic series resistance of source/drain ( $R_{SD}$ ) of SiNW FETs tends to become larger than that  
125 of planar devices [11], which degrade the  $I_{ON}$ . The  $R_{SD}$  of SiNW FETs was evaluated applying a  
126 Chern's channel-resistance method (CRM) [12] to the SiNW FETs with the three different mask gate  
127 length ( $L_{mask}$ ) of 550, 450, and 350 nm. We plotted the total resistance ( $R_{tot}$ ) at the effective gate  
128 length of each device. Then, we fitted a straight line to  $R_{tot}$  of the SiNW FETs with different gate  
129 length using least square method. Finally we obtained  $R_{SD}$  at the intercept of the y-axis. Extracted  
130  $R_{SD}$  was summarized in **figure 7**. The  $R_{SD}$  of nFETs correspond to only 10 % of the total resistance  
131 ( $R_{tot}$ ) for the SiNW nFET with the  $L_g$  of 65 nm, owing to the process optimization for S/D formation.  
132 It is worth noting that arsenic implantation instead of phosphorus results in about 10 times higher  
133  $R_{SD}$ , presumably due to the damages in the S/D region as well as the difference in the Ni silicide  
134 formation [13, 14]. On the other hand, the  $R_{SD}$  of pFETs are much higher than that of nFETs. One  
135 reason of relatively low  $I_{ON}$  compared with that of the SiNW nFETs in the previous section is the  
136 large  $R_{SD}$  of the SiNW pFETs. A difference of the  $L_{mask}$  and actual gate length ( $\Delta L$ ) of SiNW pFETs  
137 obtained during the analysis using CRM was larger than  $\Delta L$  of the SiNW nFETs. We speculate the  
138 difference of  $\Delta L$  between the SiNW nFETs and the SiNW pFETs might suggest the difference of the  
139 dopant diffusion process into the SiNW channel between phosphorus and boron. The redistribution  
140 of boron during Ni silicidation process was also reported [15] and more process optimization is  
141 necessary for the SiNW pFETs.

### 143 3.3 On-current separation into a corner component and a flat surface component

144 In the previous section, the structural advantages of  $w_{NW}$  on the  $I_{ON}$  of the SiNW FET was

145 investigated. The advantages could be explained by the effects of corners in the rectangular-like  
146 cross-section. In this section, we attempt to separate on-current of corner component ( $I_{\text{corner}}$ ) and  
147 on-current along flat surface ( $I_{\text{flat}}$ ) of the SiNW nFETs for the determination of contributions of the  
148 corners in **figure 8**. The on-current along flat surface  $I_{\text{flat}}$  and the on-current of the corner component  
149  $I_{\text{corner}}$  were calculated as follows. First we subtracted the on-current per wire of the SiNW FET with  
150 smaller  $w_{\text{NW}}$  from an on-current per wire of the SiNW FET with larger  $w_{\text{NW}}$ . Then we normalized  
151 the difference of the on-current per wire with the difference of  $w_{\text{NW}}$  between each SiNW FET. We  
152 obtained the normalized on-current along flat surface of (i) 1069, (ii) 932, and (iii) 994  $\mu\text{A}/\mu\text{m}$  using  
153 the SiNW nFET with  $w_{\text{NW}}$  of (i) 19 and 28 nm, (ii) 28 and 39 nm, and (iii) 19 and 39 nm. The  
154 averaged normalized on-current along flat surface was 998  $\mu\text{A}/\mu\text{m}$ . Next, we calculated the  
155 on-current along flat surface  $I_{\text{flat}}$ . We assumed that the normalized on-current of side-surface is the  
156 same as that of the top-surface. The peripheral length of upper corners were measured based on  
157 cross-sectional TEM images and the rest of the peripheral length was that of the flat surface as  
158 mentioned in section 2. We multiplied the normalized on-current of the flat surface by the peripheral  
159 length of the flat surface and obtained the on-current along flat surface  $I_{\text{flat}}$ . The rest is the on current  
160 of corner component  $I_{\text{corner}}$ . Separated  $I_{\text{corner}}$  and  $I_{\text{flat}}$  is summarized in **figure 9** and about 60 % of  
161 the  $I_{\text{ON}}$  of the SiNW FET ( $w_{\text{NW}}=19$  nm and  $h_{\text{NW}}=12$  nm) was attributed to the corners.

162

### 163 **3.4 Inversion charge of SiNW FETs at the on-state**

164 Inversion charge density ( $Q_{\text{inv}}$ ) and effective carrier mobility ( $\mu_{\text{eff}}$ ) was experimentally extracted  
165 by advanced split-CV technique [16] applied to multi-channel SiNW FETs with a number of  
166 64 wires to facilitate the measurement accuracy. The amount of inversion charge ( $Q$ ) of SiNW  
167 channel was calculated as

$$168 \quad Q = \int (C_{\text{gc1}} - C_{\text{gc2}}) dV$$

169 , where  $C_{\text{gc1}}$  is the gate-to-channel capacitance ( $C_{\text{gc}}$ ) of multi-channel SiNW (MSiNW) FET with  
170 larger  $L_{\text{mask}}$  and  $C_{\text{gc2}}$  is the  $C_{\text{gc}}$  of the MSiNW FET with smaller  $L_{\text{mask}}$ . The inversion charge density  
171  $Q_{\text{inv}}$  at  $V_{\text{g}} - V_{\text{th}} = 1.0$  V for nFETs and  $Q_{\text{inv}}$  at  $V_{\text{g}} - V_{\text{th}} = -1.0$  V for pFETs were obtained, which is shown  
172 in **figure 10 (a)**. As the cross-sectional dimension increased, the amount of inversion charge  
173 increased. After normalization by unit channel area, largest  $Q_{\text{inv}}$  was achieved with the SiNW FETs  
174 with the smallest  $w_{\text{NW}}$ . The increase of inversion charge density was observed for both p-type and  
175 n-type SiNW FETs, which is shown in **figure 10 (b)**. The solid line in **figure 10 (b)** is calculated  
176  $Q_{\text{inv}}$  on assumptions below.

177 For an investigation of contributions of corners to the total amount of inversion charge, the  
178 amount of inversion charge was separated to the component of corners and that of flat surface. It was  
179 assumed that (i) inversion charge density of the flat surface is the same as that of planar SOI FETs

180 and that (ii) the peripheral length of upper corners was measured with cross-sectional TEM image as  
 181 in the section 3.3. The amount of inversion charge at the corner ( $Q_{\text{corner}}$ ) and the amount of inversion  
 182 charge along flat surface ( $Q_{\text{flat}}$ ) are shown in **figure 11**. As the  $w_{\text{NW}}$  decrease fraction of the amount  
 183 of inversion charge around corners increase. The solid line in **figure 10 (b)** was the calculated  
 184 inversion charge density  $Q_{\text{inv}}$  on the assumptions as follows: (i) the inversion charge at the corners  
 185 was  $4.9 \times 10^{-15}$  C with the  $W_c$  of 4 nm, which was the average of the corner component of inversion  
 186 charge shown in **figure 11 (ii)** the  $Q_{\text{inv}}$  of flat surface is the same as that of SOI planar nFETs. The  
 187  $Q_{\text{inv}}$  of the sample C is out of the line, which suggests the  $W_c$  of sample C is larger than 4 nm, which  
 188 agrees with the  $W_c$  obtained by the cross-sectional TEM image in **figure 2 (b)**.

189

### 190 **3.5 Effective carrier mobility evaluation of the SiNW FETs**

191 The  $\mu_{\text{eff}}$  of SiNW FETs was obtained using the advanced split-CV method [16] and results were  
 192 calculated using the equations

$$193 \quad \mu_{\text{eff}} = \frac{\Delta L^2 \cdot \Delta g_d}{Q}$$

194 where  $\Delta L$  is the difference of mask gate length ( $L_{\text{mask}}$ ) between two transistors used for measurement.  
 195  $\Delta g_d$  is the difference of the drain conductance, which is written as

$$196 \quad \frac{1}{\Delta g_d} = \frac{1}{g_{d1}} - \frac{1}{g_{d2}}.$$

197 , where  $g_{d1}$  is the drain conductance of the SiNW FET with larger  $L_g$  and  $g_{d2}$  is the drain  
 198 conductance of the smaller  $L_g$ . The results are shown in **figure 12**. Higher  $\mu_{\text{eff}}$  of SiNW nFET than  
 199 planar SOI nFETs were obtained from the middle-field to the high-field region, which is one reason  
 200 of the high  $I_{\text{ON}}$  of SiNW nFETs. The higher  $\mu_{\text{eff}}$  of SiNW nFETs than that of planar SOI nFETs  
 201 suggests higher  $\mu_{\text{eff}}$  could be obtained around corners. For an extraction of  $\mu_{\text{eff}}$  at the corners and  
 202 that along the flat surface of the channel,  $g_d$  was also separated to the corner component and that  
 203 along flat surface on the same assumption as in the extraction process of the inversion charge at the  
 204 corners and that of the flat surface. Finally  $\mu_{\text{eff}}$  at  $V_g - V_{\text{th}} = 1.0$  V around corners and along the flat  
 205 surface of channel were calculated, which are shown in **figure 13**. The  $\mu_{\text{eff}}$  around corners saturates  
 206 as the  $w_{\text{NW}}$  increase toward 28 nm. Higher  $\mu_{\text{eff}}$  at corners of nFETs than that of flat surface were  
 207 obtained.

208 The  $\mu_{\text{eff}}$  of pFETs were also extracted using the advanced split-CV method and shown in  
 209 **figure 12 (b)**.  $\mu_{\text{eff}}$  of the SiNW FETs were comparable with that of planar SOI pFETs and shows a  
 210 little degradation of  $\mu_{\text{eff}}$  as  $w_{\text{NW}}$  decrease.

211

## 212 **4. Discussion**

213 We obtained large  $I_{ON}$  of the SiNW nFETs due to the increase in the  $Q_{inv}$ , the enhancement of  $\mu_{eff}$   
214 and the reduced  $R_{SD}$ . Although the increase in the  $Q_{inv}$  is observed for both nFETs and pFETs, the  
215 enhancement effect in the  $\mu_{eff}$  was observed only for nFETs. The comparable  $\mu_{eff}$  of SiNW pFETs  
216 with that of planar SOI pFETs is one reason of relatively low  $I_{ON}$  of the pFETs. The extracted  $\mu_{eff}$   
217 around the corners of the SiNW nFETs are enormously large, which coincides with the experimental  
218 results of [17]. The channel surface orientation of corners is composed of various surface crystal  
219 orientations, which seems to degrade the surface carrier mobility of the corners [18]. However, the  
220 carrier mobility around corners obtained in this work is very large and even surpasses (100)-surface  
221 universal mobility [19]. The enhanced  $\mu_{eff}$  around the corners might be due to volume inversion  
222 around corners. Our two-dimensional device simulation using almost the same structure as that in  
223 this work ( $w_{NW}=19$  nm,  $h_{NW}=12$  nm and  $w_{NW}=28$  nm,  $h_{NW}=12$  nm) resulted in 2.5 times as high  
224 inversion charge density around the corners, the peak density of which is  $5.3 \times 10^{19}$  cm<sup>-3</sup>, as that along  
225 flat surface at the on-state. The high inversion charge density supports the existence of volume  
226 inversion around the corners. The  $\mu_{eff}$  enhancement due to the volume inversion has been reported  
227 [20, 21]. The effective carrier mobility  $\mu_{eff}$  of nearly 550 cm<sup>2</sup>/Vs was obtained in the double gate  
228 mode at inversion carrier density of  $10^{12}$  cm<sup>-2</sup> for [20]. The extracted  $\mu_{eff}$  of corners with the  $w_{NW}$  of  
229 19 nm is comparable with the reported experimental results. The discussion above indicates that  $\mu_{eff}$   
230 in SiNW channel is not only governed by channel surface orientation, but especially structural  
231 advantage of corners of rectangular cross-sectional shape. On the other hand, corner enhancement of  
232  $\mu_{eff}$  for the SiNW pFETs seem not to exist.

233 As a large amount of inversion charge and superior effective electron mobility was obtained  
234 around corners of rectangular cross-section, one might expect that larger  $I_{ON}$  can be obtained with  
235 smaller  $w_{NW}$  of SiNW nFETs as an extrapolation in **figure 5** toward lower  $w_{NW}$ . However we can  
236 observe that  $\mu_{eff}$  at the corners of SiNW FET degrades as the  $w_{NW}$  decrease in **figure 13**. This result  
237 suggests that  $\mu_{eff}$  degrades as the distance between each corner decreases, which is equal to a  
238 decrease of  $w_{NW}$ . Therefore we speculate that the  $I_{ON}$  of the SiNW nFET does not monotonically  
239 increase as the  $w_{NW}$  decrease. Optimized dimensions of cross-section should be studied for an  
240 enhancement of the  $I_{ON}$  with structural advantages of the SiNW nFET with the rectangular-like  
241 cross-section. We speculate an optimized cross-sectional dimension is near  $w_{NW}=19$  nm and  
242  $h_{NW}=12$  nm due to comparable  $Q_{inv}$  at  $V_g - V_{th}=1.0$  V and higher  $\mu_{eff}$  compared with those of the  
243 SiNW nFET with  $w_{NW}=9$  nm and  $h_{NW}=10$  nm.

244

## 245 5. Conclusion

246 We have investigated the structural advantage of rectangular cross-section on electrical  
247 performances, especially the  $I_{ON}$ ,  $Q_{inv}$  and  $\mu_{eff}$  of the SiNW nFETs. It is confirmed that the corners  
248 in rectangular-like cross-section play important roles on the achievement of the  $I_{on}$  as high as



249 1600  $\mu\text{A}/\mu\text{m}$  of the SiNW nFET ( $w_{\text{NW}}=19$  nm and  $h_{\text{NW}}=12$  nm) thanks to the increase of the  $Q_{\text{inv}}$   
250 and the significant enhancement of the  $\mu_{\text{eff}}$  around corners. This result suggests that current  
251 conduction is not only governed by channel surface orientation but by cross-sectional shape of  
252 channel. For pFETs, the increase of the  $Q_{\text{inv}}$  has been observed. However the enhancement of  $\mu_{\text{eff}}$  is  
253 not observed. By narrowing the SiNW channels,  $\mu_{\text{eff}}$  of corners tend to degrade, although the  $\mu_{\text{eff}}$  of  
254 the corners of narrower SiNW FET was higher than that of flat surface. Therefore we speculate that  
255 the structural advantage by the reduction of the  $w_{\text{NW}}$  is not monotonic.

256

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262

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319

320 **Figure captions**

321 Figure 1. A schematic process flow of the gate semi-around SiNW FETs. The gate semi-around  
322 SiNW FET was fabricated with conventional CMOS process facilities.

323 Figure 2. (a) A review SEM image and (b) cross-sectional TEM images of the SiNW channels and  
324 the cross-sectional dimensions. A cross-section of planar SOI FETs is also shown.

325 Figure 3. (a) The transfer and (b) output characteristics of the SiNW FETs ( $w_{NW}=19$  nm and  
326  $h_{NW}=12$  nm).

327 Figure 4. The  $I_{ON}$  dependence on gate length ( $L_g$ ) and channel width ( $w_{NW}$ ) of the SiNW FETs and  
328 planar SOI FETs.

329 Figure 5. Structural advantages of the SiNW nFETs with rectangular-like cross-section over planar  
330 SOI nFETs, which increase as the  $w_{NW}$  decrease.

331 Figure 6.  $I_{ON}/I_{OFF}$  characteristics of the SiNW nFETs ( $w_{NW}=19, 28,$  and  $39$  nm,  $h_{NW}=12$  nm) with  
332 the gate length from 65 to 500 nm.

333 Figure 7. Total resistance ( $R_{tot}$ ) of SiNW nFETs and pFETs with the different  $L_g$ . Intercepts on  
334 y-axis are extracted  $R_{SD}$ .

335 Figure 8. Assumptions for calculation and extraction of  $I_{ON}$ ,  $Q_{inv}$ , and  $\mu_{eff}$  of the fraction of corners  
336 and those of flat surface.  $W_c$  is assumed to be 4 nm considering cross-sectional TEM images in  
337 figure 2(b).

338 Figure 9. Extracted on-current of the corner component and the flat surface component of the SiNW  
339 nFETs with the  $L_g$  of 65 nm.

340 Figure 10. (a) The amount of inversion charge and (b) the inversion charge density of the SiNW  
341 FETs and planar SOI FETs (solid for pFETs and open for nFETs). The solid line in (b) is calculated  
342 on the assumptions: (i) the amount of inversion charge at the rounded corners is  $4.9 \times 10^{-15}$  C with the  
343 radius ( $W_c$ ) of 4 nm (ii) the inversion charge density along flat surface is  $9.7 \times 10^{-21}$  C/cm<sup>2</sup>.

344 Figure 11. The amount of inversion charge at the corners ( $Q_{corner}$ ) and along the flat surface ( $Q_{flat}$ ) of  
345 the SiNW nFETs with the channel width  $w_{NW}$  of 9, 19, and 28 nm.

346 Figure 12. Effective carrier mobility of the multi-channel SiNW (a) nFETs and (b) pFETs in this  
347 work extracted using the advanced split-CV method [16].

348 Figure 13. Separated  $\mu_{eff}$  of corners and that of flat surface of the SiNW nFETs ( $w_{NW}=9, 19$  and  
349 28 nm).

Figure 1.


- SiN HM deposition
  - Fin formation
  - Sacrificial oxidation & SiN removal
  - SiN removal
  - Sidewall support for SiNW
  - Oxide etching
  - Gate oxidation (3 nm) & Poly-Si deposition
  - TEOS HM deposition
  - Gate patterning
  - 1<sup>st</sup> sidewall formation & extension I/I
  - 2<sup>nd</sup> sidewall formation & deep S/D I/I
  - Rapid thermal annealing for activation
  - Ni (9 nm) / TiN deposition
  - Silicidation annealing & SPM cleaning
- 

Figure 2.

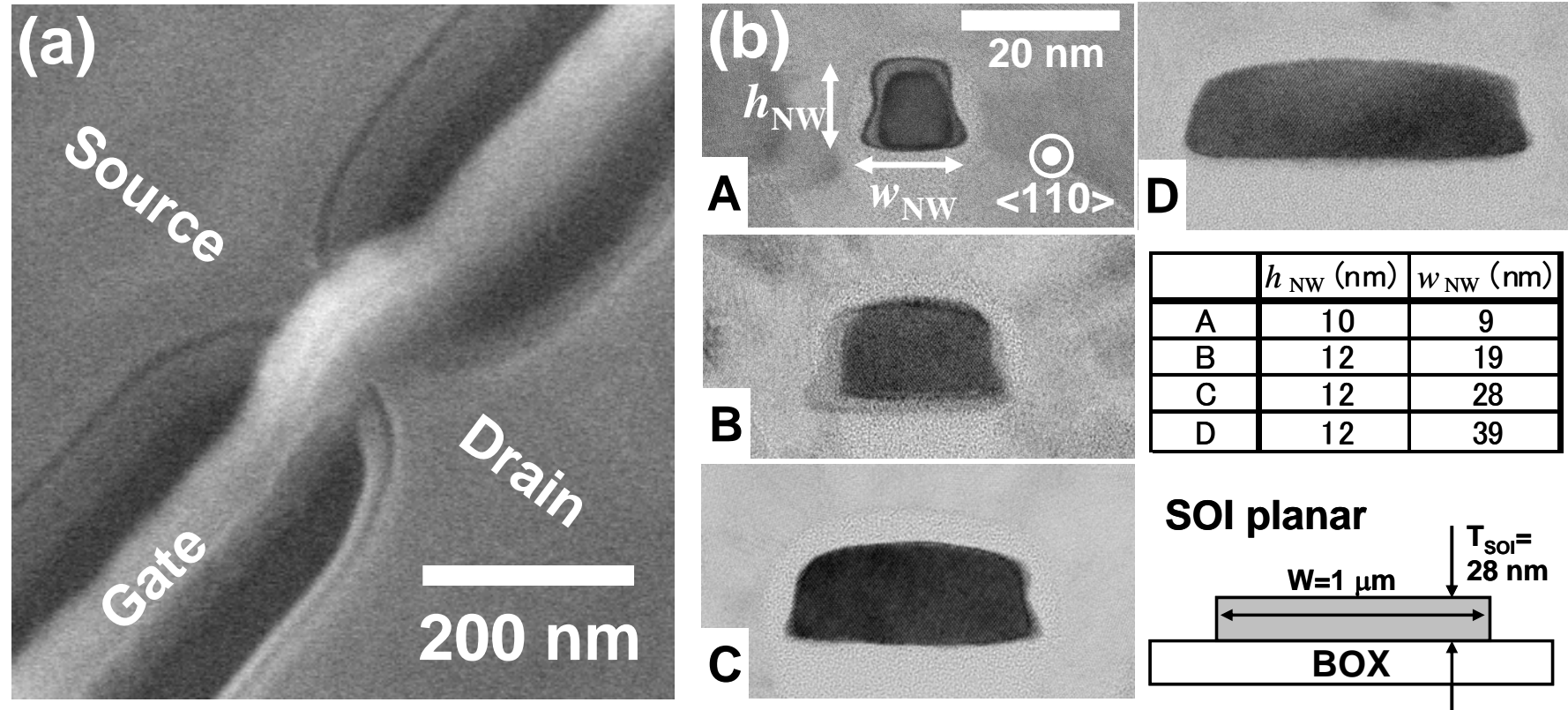


Figure 3.

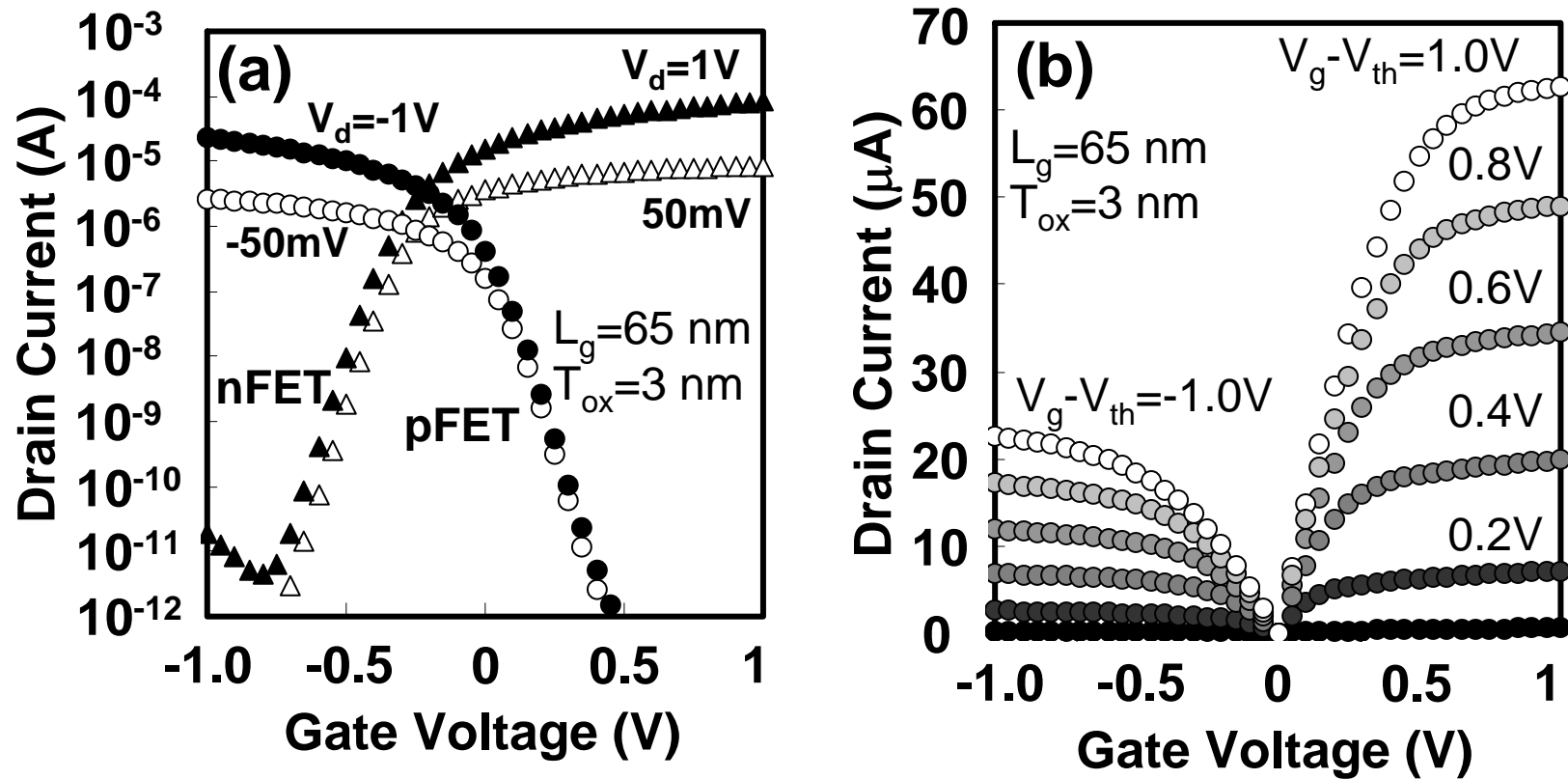


Figure 4.

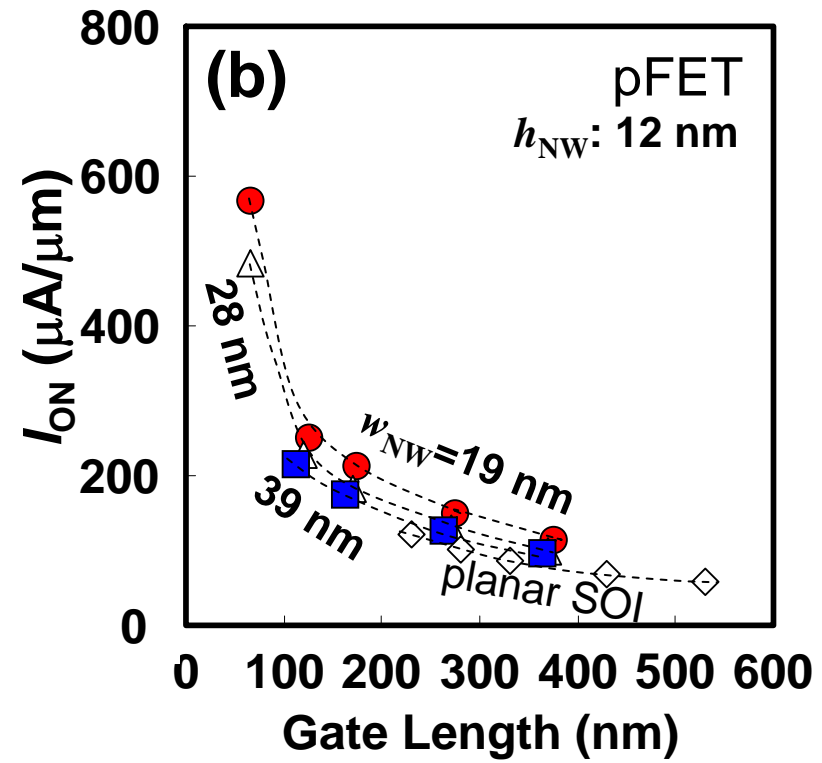
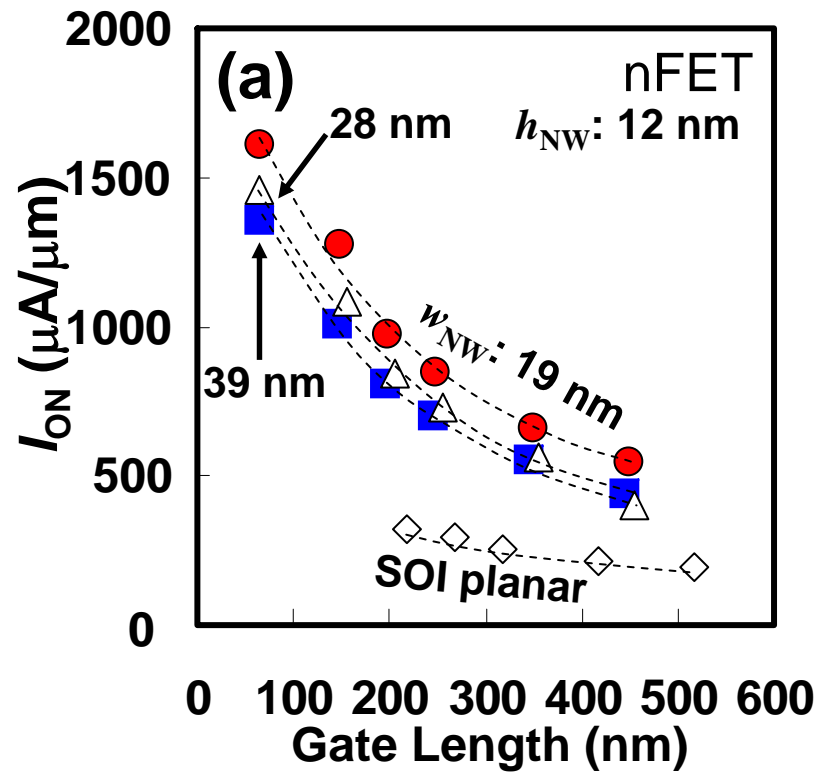


Figure 5.

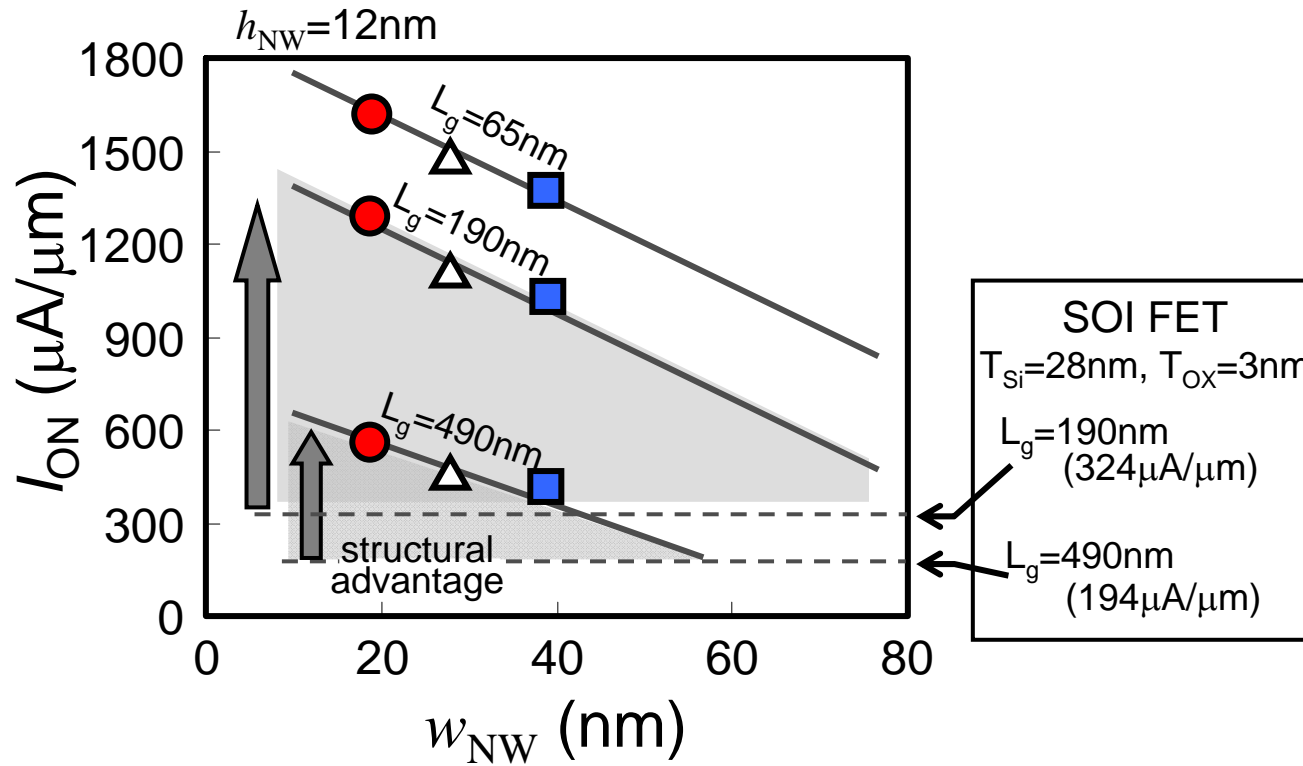




Figure 6.

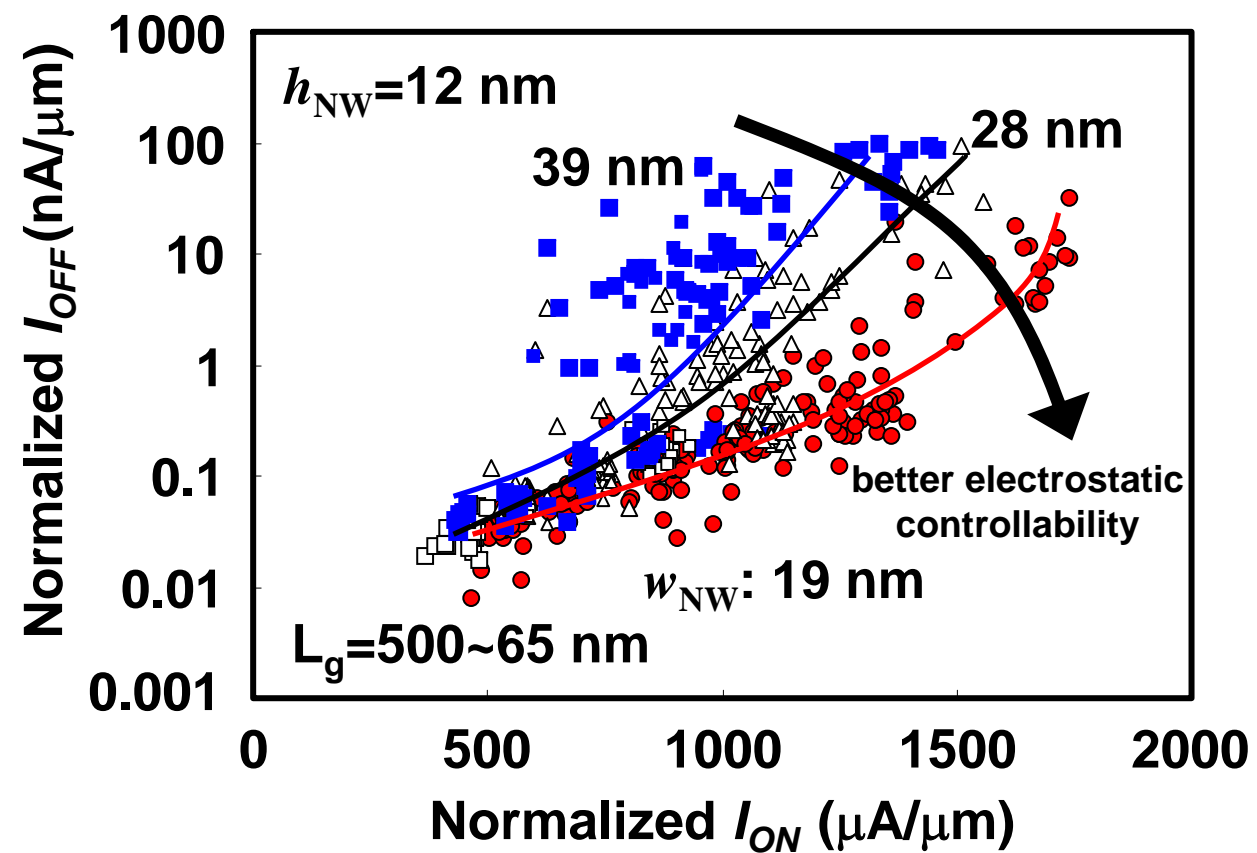
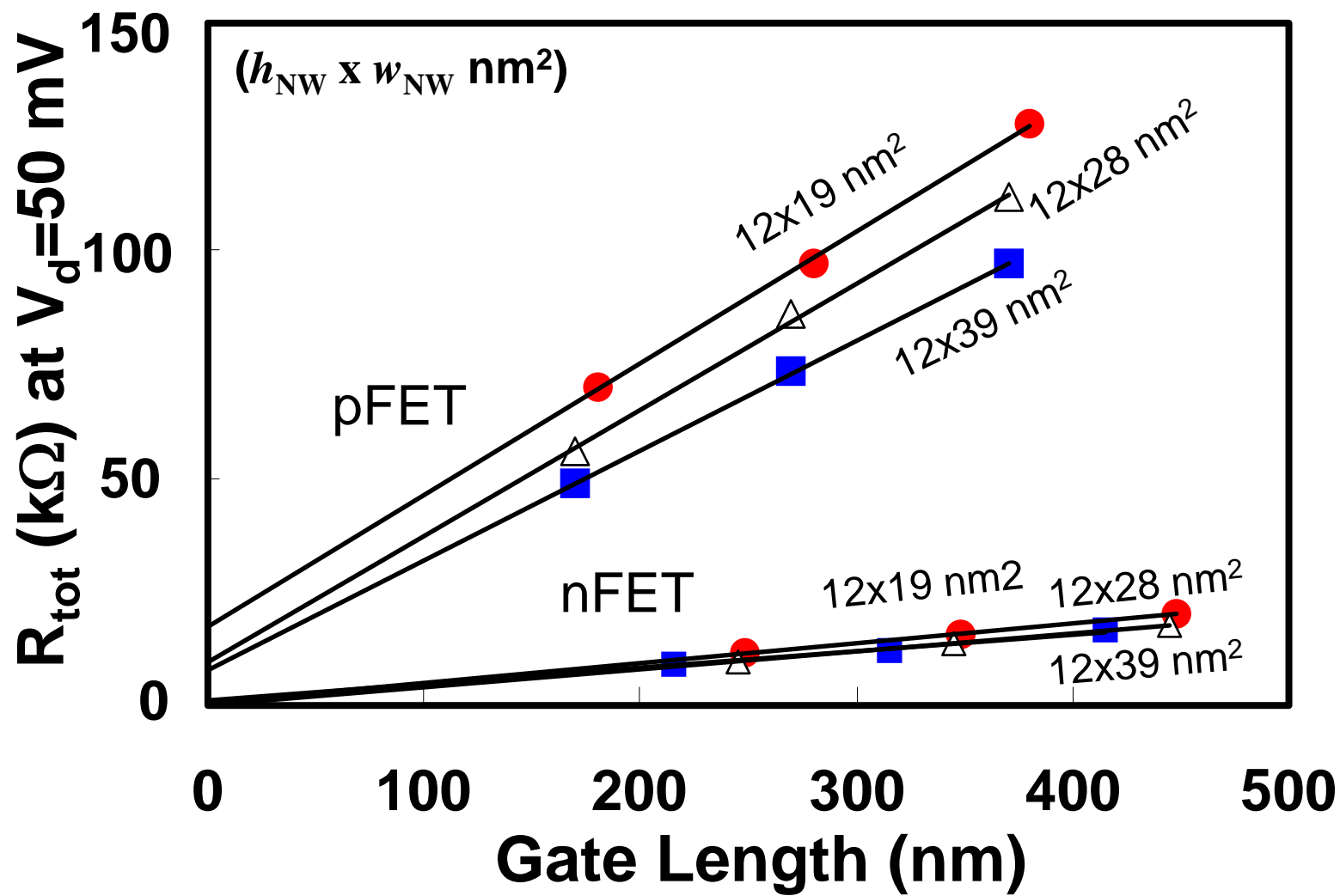


Figure 7.



**Figure 8.**

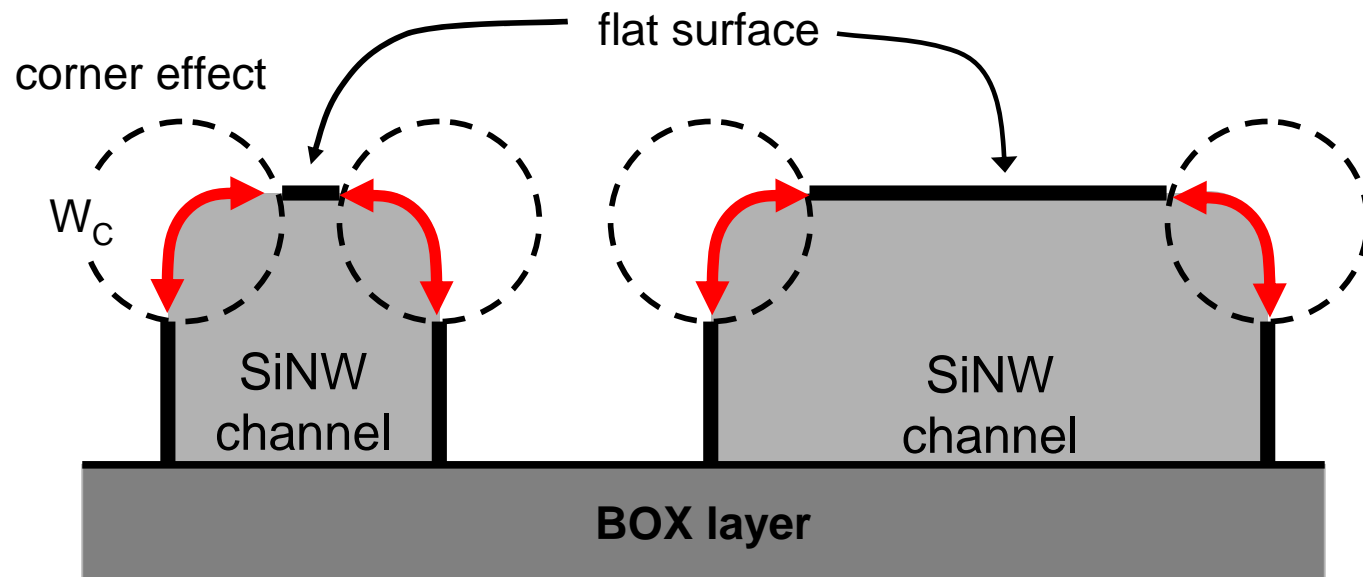


Figure 9.

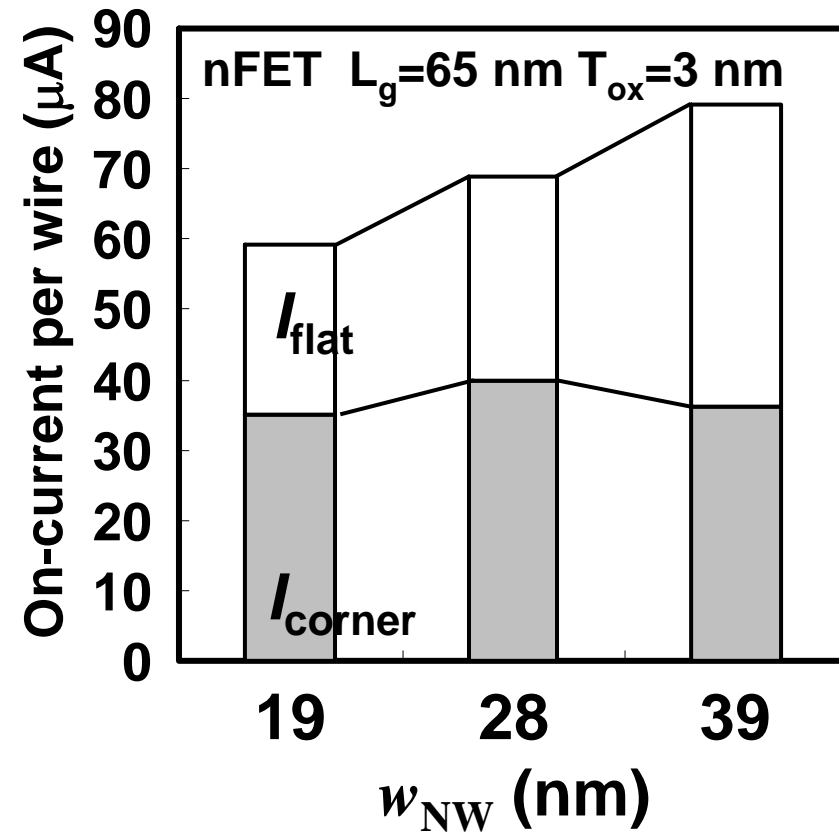


Figure 10.

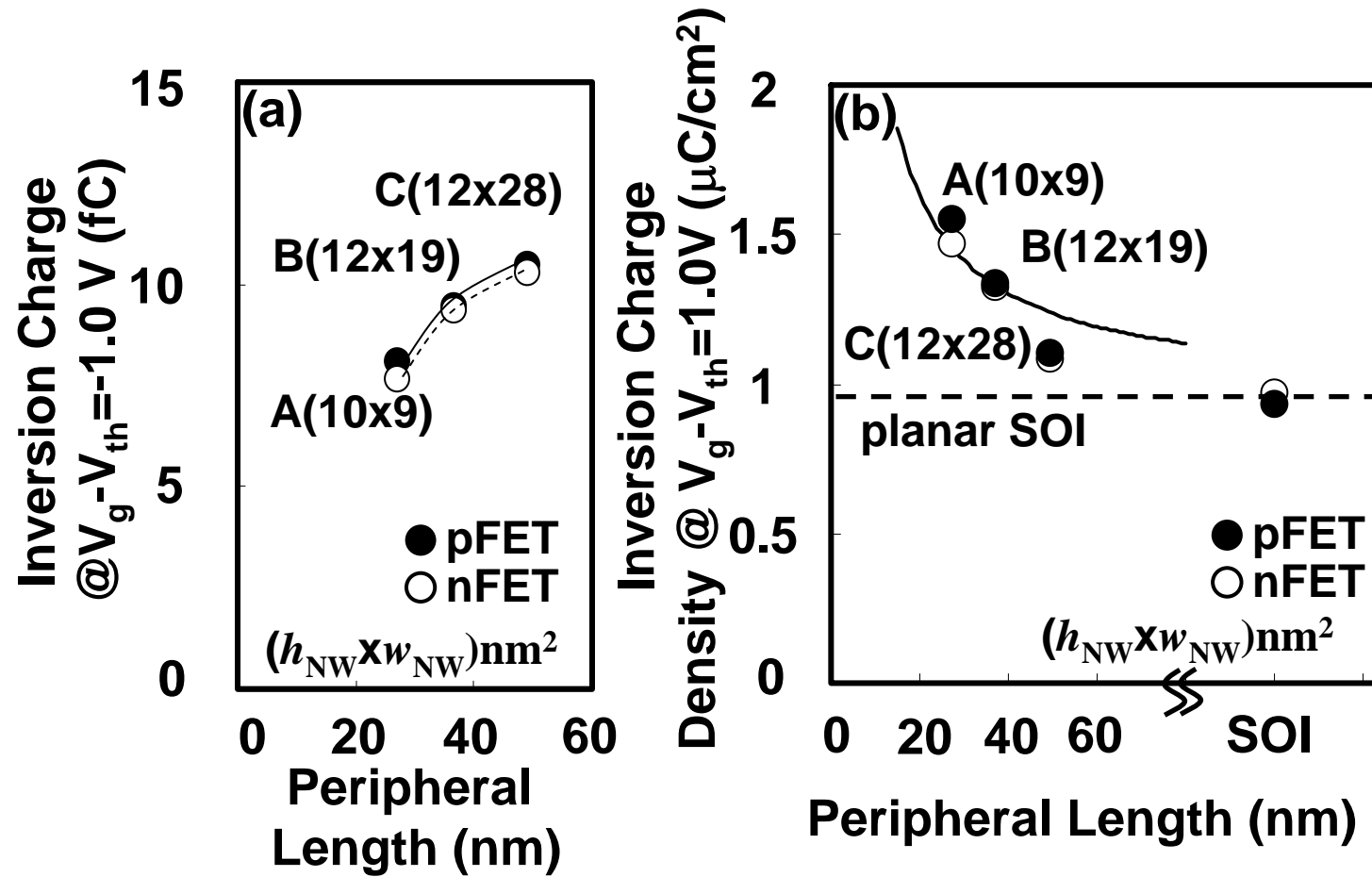


Figure 11.

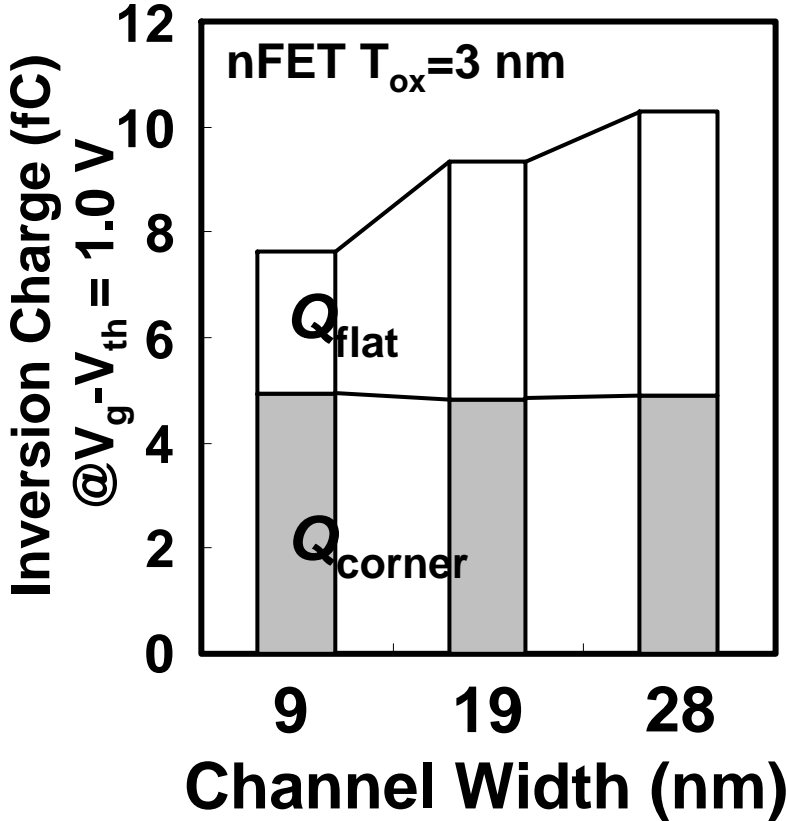


Figure 12(a).

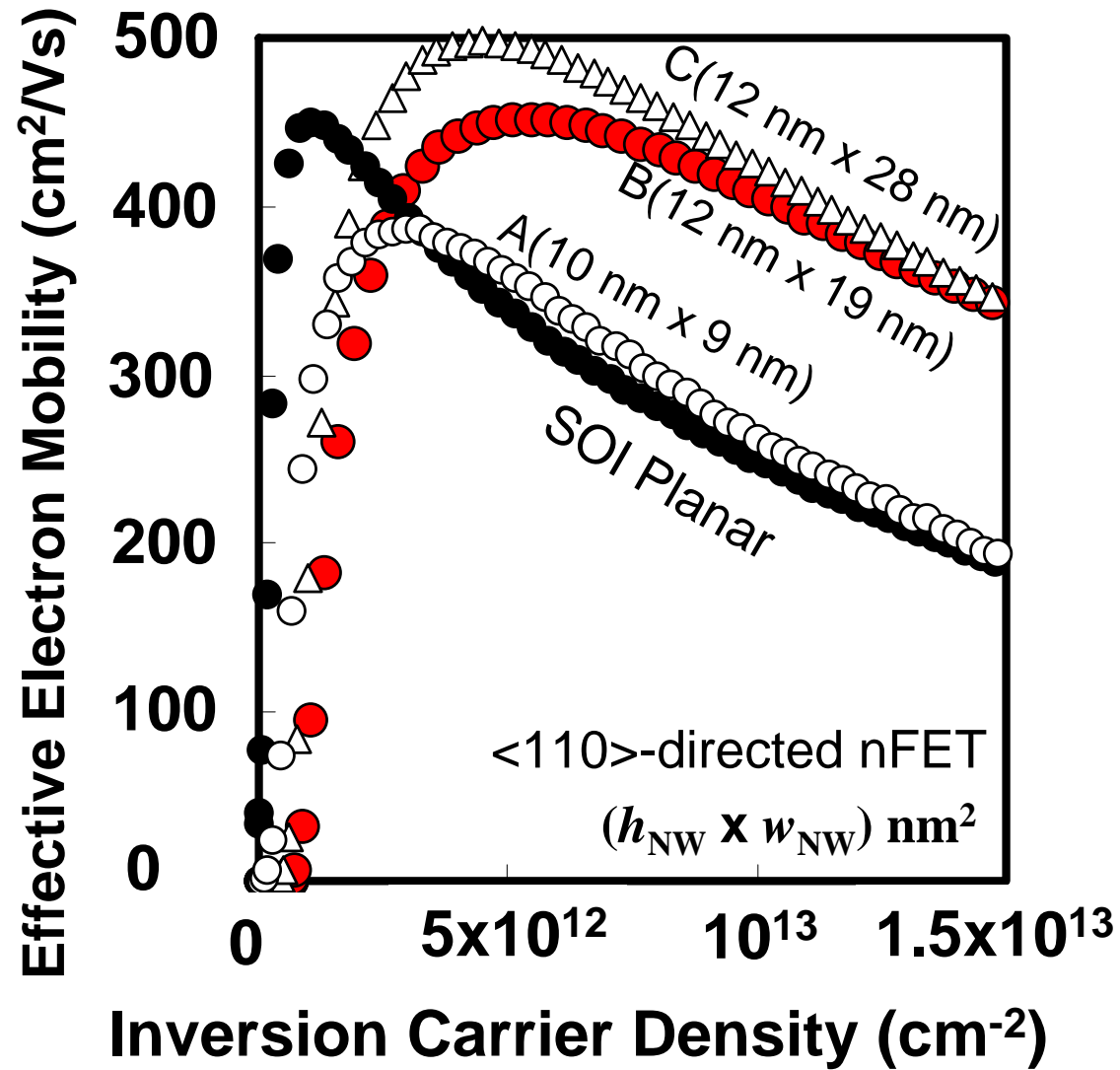


Figure 12(b).

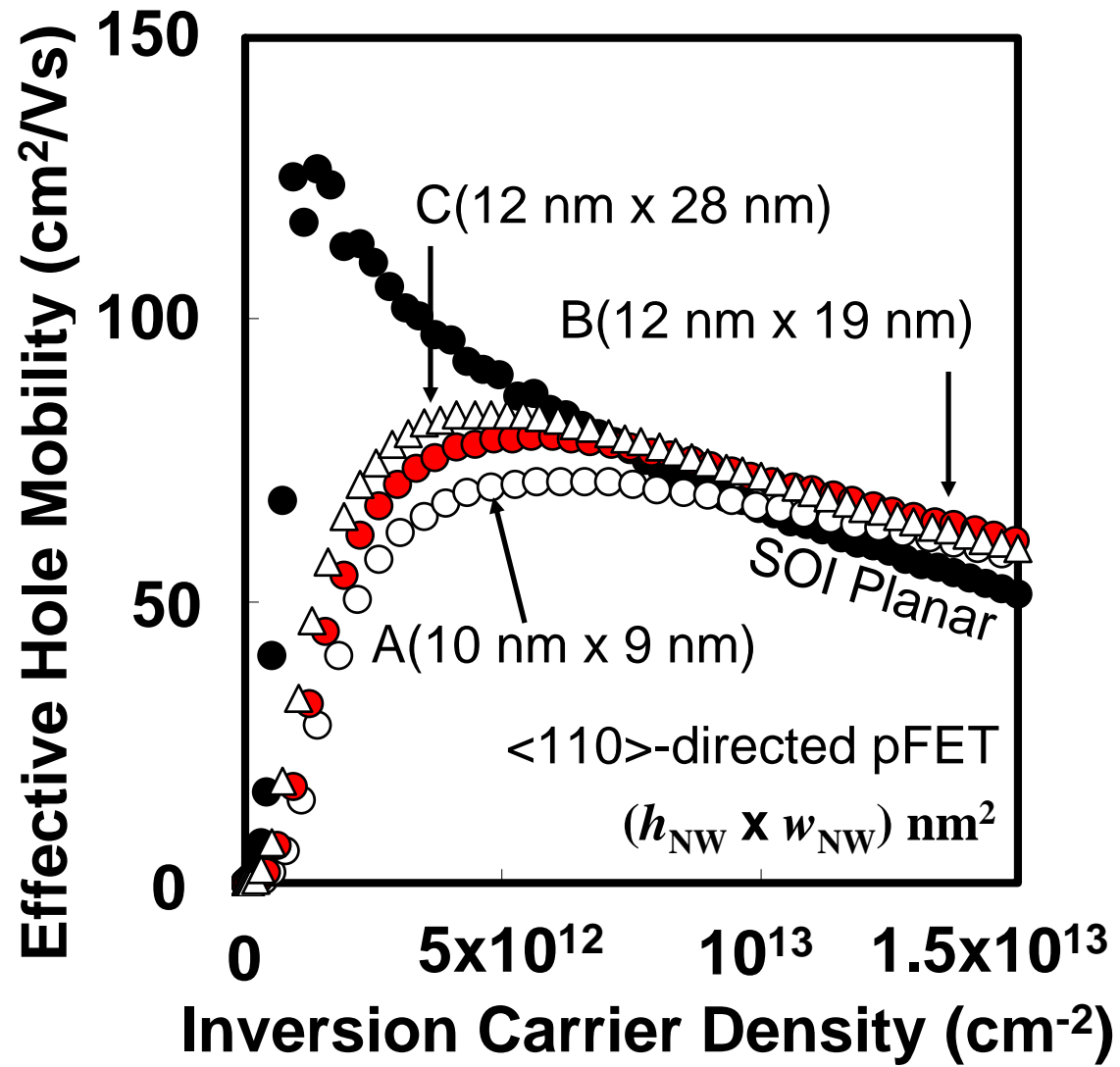




Figure 13.

