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A Broadband Doherty Power Amplifier for Sub-6 GHz 5G Applications

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ABSTRACT This paper presents a novel and accurate procedure for designing a Doherty power amplifier (DPA) for wireless systems. The method is based on a systematic approach to designing the matching networks of both Main and Auxiliary devices, which employs an optimization process to set their input impedance in the corresponding optimal regions obtained from standard load- and source-pull simulations. To import the optimum regions of each device into the optimization algorithm, mathematical expressions are derived and graphically reported on the Smith chart. Besides this, we have developed an accurate method to account for the loading effect of the Auxiliary amplifier on the Main one at back-off when designing the Main PA. As a proof of concept, a symmetric DPA is designed, fabricated, and tested. The measurements showed a working frequency band of 3.3 – 3.9 GHz (aimed at n78 band of 5G-NR), a minimum peak output power of 36 W, drain efficiency between 48 % – 53.2 % at peak and 34.6 % – 44.5 % at 6 dB back-off.

INDEX TERMS Doherty power amplifier, high-efficiency power amplifier, load-pull, optimization, source-pull, wideband matching network.

I. INTRODUCTION

MANY modern modulation schemes exhibit significant signal envelope variations, and as long as the push for higher throughput continues, the envelope variation would get more extreme. The envelope variation in a signal causes its average power to be much lower than its peak power. Nowadays, some complex signals have a peak-to-average power ratio (PAPR) of 9 dB or more. In this context, a classic power amplifier (PA) would perform poorly, especially in terms of its average efficiency. On the other hand, the ever-higher demand for green and high-efficiency tech, along with lower OpEx, has drawn significant attention to the efficiency of systems [1].

Several PA topologies have come about to answer the shortcoming of classical PAs when dealing with high PAPR signals, one of which is the Doherty PA (DPA) [2]–[4]. The DPA is based on the modulation of the load presented to an active device, namely Main, commonly working in class AB, by using a second active device, namely Auxiliary, which is biased in class C [4]. The DPA is designed in a way that for low input power levels, the Main is on, whereas the Auxiliary is off. By increasing the input power and reaching the Main's saturation, the Auxiliary turns on and modulates the load seen by the Main. By exploiting an impedance inverter network, which can be realized using a simple quarter-wave transmission line, between the two amplifiers, in ideal conditions, it is possible to keep the efficiency of the Main PA constant until the Auxiliary is saturated as well. In such a way, the DPA can provide high efficiency in a wide range of output power back-off (OBO).

On the other hand, the DPA has some shortcomings; one of them is its narrow bandwidth, mainly due to the narrow-band operation of the quarter-wave impedance inverter network [5]. The complexity of designing the matching networks (MNs) is another negative factor. It is worth mentioning that in the design procedure of a classical DPA, the intrinsic output impedance of the device needs to be known. However, for most commercial active devices, manufacturers only provide models extracted at the package planes, including both intrinsic and inherent parasitics. In order to address such issues, Akbarpour et al. in [5] proposed a modified architecture of DPA, namely transformer-less load modulated architecture wherein, at first glance, the impedance inverter is eliminated, as shown in FIGURE 1. In this architecture,

however, the output MN (OMN) of the Main PA plays the role of an impedance inverter in addition to its primary matching role. In other words, the Main amplifier's OMN transfers the modulated impedance at the load modulation point, which varies dynamically from Z'_0 at 6 dB OBO to $2 \cdot Z'_0$ at saturation, to proper impedances that the Main device needs to see at the package plane. These impedances can be straightforwardly obtained from load-pull simulations at different input power levels without the need for transistor's model at the intrinsic plane. Furthermore, thanks to the elimination of the quarter-wave transformer, a larger bandwidth with respect to the original DPA is achievable. Modifications in inverter-less DPAs were introduced in several recent works to improve the DPA's performance [6]–[13].

Usually, DPAs are designed as two separate amplifiers and connected to each other afterward. The underlying assumption in this approach is that the loading effect of one amplifier onto the other does not introduce significant variations with respect to the case of separate amplifiers. However, especially at back-off, i.e., when the Auxiliary PA is off, the reactive loading of the latter onto the Main can significantly degrade the DPA performance. Such aspect, which is usually ignored during the design phase of the Main PA, is then compensated by tuning the length of an offset line, placed at the output of the Auxiliary PA, in order to fulfill the condition in which, at back-off, the Main PA sees an open circuit at the load modulation point, looking towards the Auxiliary PA (see FIGURE 1) [5]–[8]. Alternatively, the output-matching network of the Auxiliary PA can be designed so that the output impedance of the Auxiliary PA (when the device is off), seen from the modulation point, becomes close to the open circuit point [14], [15]. However, these techniques themselves would limit the bandwidth as the PA's output impedance cannot be transformed to the open circuit in a wide frequency range. This is where this work differs from previous ones. Instead of ignoring the loading effects of the Auxiliary on the Main PA, we include the Auxiliary, or rather its extracted loading effect, while designing the OMN of the Main PA. This allows a more accurate compensation of the Auxiliary's loading effect onto the Main one.

The developed design method will be presented through the design and implementation of a 40 W DPA targeting the n78 5G band. In particular, the approach is based on a systematic procedure for designing the MNs of both Main and Auxiliary devices, which employs an optimization process to set their input impedance in the corresponding optimal regions. These optimum regions are simply related to the power and efficiency contours levels, which are the result of load- and source-pull simulations. It is worth mentioning that although it is traditionally known to consider the optimal regions for MN design, its application in an optimization-based systematic CAD requires expressing the optimal regions using mathematical expressions, which are, in turn, used to define the optimization goal. This has been the subject of some very recent works, however, mainly for a single transistor PA [6], [16]–[19].

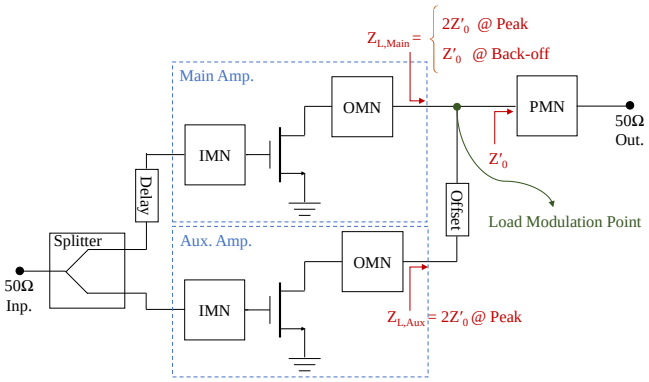


FIGURE 1: Block diagram of an inverter-less DPA with a post-MN.

II. DESIGN PROCEDURE

The proposed design strategy is explained together with the implementation of a DPA with a typical peak power of 40 W for n78 5G frequency band (i.e., 3.3 – 3.8 GHz). However, as a safe margin to account for any frequency shift in the realization, the specified bandwidth is extended to 3.2 – 4 GHz. Both Main and Auxiliary PAs use the same packaged 25 watt GaN HEMTs from Wolfspeed (CG2H40025F). The Main and Auxiliary transistors are biased in classes AB and C, respectively [4]. Moreover, to compensate for the lower gain of a class C, the drain voltage (V_{DS}) of the Auxiliary was set to a higher value with respect to the Main one [20]. Specifically, V_{DS} was set to 28 V and 33 V for the Main and Auxiliary PAs, respectively.

The overall topology uses a transformer-less load-modulated architecture [5] along with post-matching impedance transformation [6]–[10], [21], as shown in FIGURE 1. The transistor's load-pull simulations show that the optimum drain impedances for different bias conditions are in the order of a few ohms. Therefore, to simplify the design of the OMNs, the reference impedance is first set to $Z'_0 = 5\,\Omega$, and then transformed to $Z_0 = 50\,\Omega$ through the synthesis of a post MN (PMN). The value of Z'_0 is chosen to be close to the real part of the transistor's desired impedance in the frequency band of interest to simplify the design of the OMNs. The DPA implementation starts with the design of the Auxiliary PA, then the Main PA is designed, accounting for the loading effect of the Auxiliary at back-off. In the following, each step of the developed procedure is described in detail.

A. DESIGN OF THE AUXILIARY AMPLIFIER

By setting the available power from the source (Pavs) to around 33 dBm, which makes the device saturated, load- and source-pull simulations at several frequencies within the desired bandwidth (i.e., 3.2 – 4 GHz) were performed under a gate-source and a drain-source voltages of $V_{GS} = -4.6\,V$ and $V_{DS} = 33\,V$, respectively. At each frequency point, multiple contours of power added efficiency (PAE) and output power (Pout) were acquired on the smith chart.

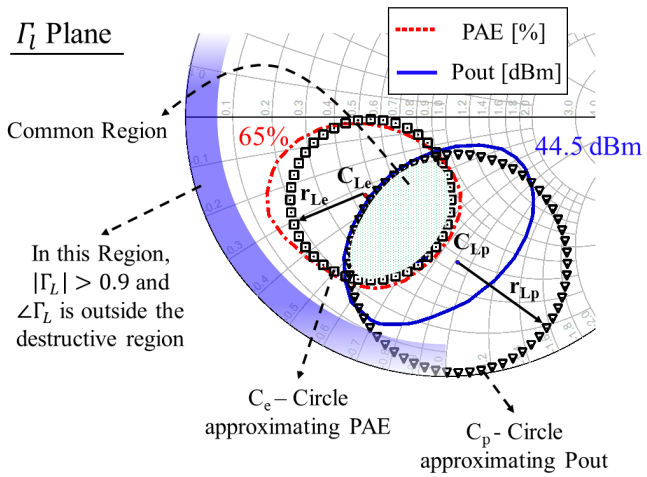


FIGURE 2: A sample of load-pull result. The chosen PAE and Pout contours (PAE = 65% and Pout = 44.5 dBm) form a common region which can be approximated with arcs from two circles. A portion of the allowed region for the second harmonic termination is also shown in blue shade.

f [GHz]	C_{Lp}	r_{Lp}	C_{Le}	r_{Le}
3.2	$0.50\angle -110^\circ$	0.48	$0.36\angle -175^\circ$	0.40
3.45	$0.55\angle -100^\circ$	0.45	$0.38\angle -158^\circ$	0.36
3.75	$0.53\angle -90^\circ$	0.42	$0.42\angle -138^\circ$	0.33
4	$0.55\angle -82^\circ$	0.40	$0.46\angle -125^\circ$	0.30

(a)

f [GHz]	C_S	r_S
3.2	$0.67\angle -110^\circ$	0.28
3.45	$0.69\angle -102^\circ$	0.26
3.75	$0.77\angle -92^\circ$	0.18
4	$0.78\angle -85^\circ$	0.15

(b)

FIGURE 3: The centers and radii of the circles defining the optimum regions for the load (a) and source (b) terminations of the auxiliary amplifier. In (a), subscripts p and e stand for Pout and PAE circles, respectively.

For PAE, the contour corresponding to 65 % (around 10 % lower the maximum efficiency), and for Pout, the contour corresponding to 44.5 dBm (around 1 dB lower the maximum Pout) were chosen, and the entire common region between these PAE and Pout contours was considered as design goals for the MNs. To synthesize a termination within this common region, we need first to define this region by a mathematical expression; then, it would be possible to consider a MN with an arbitrary topology having some tunable parameters (for example, a multi-section transmission line where the length and width of the sections can be tuned [22], [23], and apply an optimization algorithm to take the input impedance of the considered MN inside the defined region. To this end, the sections of PAE and Pout contours forming the borders of the common region were approximated by two arcs (of two circles) as shown in FIGURE 2 (black symbols) for the output

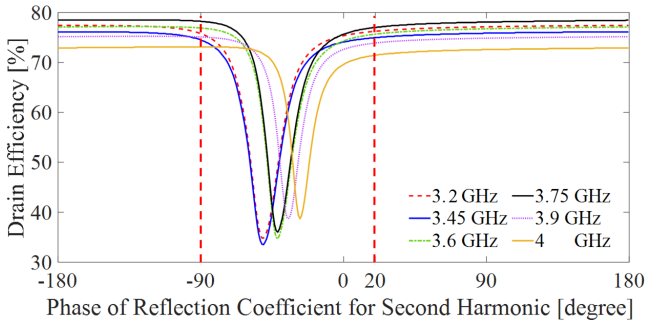


FIGURE 4: DE versus the phase of Γ_L at second harmonic (while its magnitude is fixed at 0.9) for the Auxiliary device.

plane. Then, when designing the MNs, the radius and center of these circles are used to define the design (optimization) goal as,

$$\begin{aligned} &|\Gamma(f_i) - C_p(f_i)| \le r_p(f_i) \\ &\quad \& \\ &|\Gamma(f_i) - C_e(f_i)| \le r_e(f_i), \end{aligned} \tag{1}$$

where f_i are the frequency points, Γ is the input reflection coefficient of the MN (seen from the transistor's drain or gait in the case of the OMN and input MN (IMN), respectively), C_p and r_p are the radius and center of the circle fitted to the section of the power contour forming a border of the desired region, and C_e and r_e are those of the circle fitted to the efficiency contour.

The centers and radii of the circles defining the optimum region for the load and source terminations (in other words, the IMN and OMN design spaces) are given in FIGURE 3 (a) and (b), respectively, for four frequencies. Since the PAE and Pout circles of the source termination almost completely overlap each other, only one circle was considered for defining the optimum region for the IMN synthesis.

Since the transistor's terminations at higher order and specially second harmonic can also impact the PA's performance [24]–[26], the MNs are commonly designed in a way that the reflection coefficient at higher frequency with respect to the useful bandwidth is on the border of the Smith chart with a proper phase. To investigate the effect of the second harmonic termination, we performed simulations at several frequencies in which, by keeping the fundamental source and load terminations at the center of the corresponding optimal region, the phase of the load reflection coefficient (Γ_L) at second harmonic was swept from -180 to 180 degrees, while its magnitude was fixed at 0.9. FIGURE 4 shows the variation of the drain efficiency (DE) versus the phase of the second harmonic termination, wherein a detrimental effect on efficiency is noted from -90 to 20 degrees for all fundamental frequencies, while elsewhere, the effect is minimal. We concluded that the second harmonic termination does not degrade the PA performance as long as it does not lie in this specific range of phases, which should be avoided in the design procedure. Therefore, when designing the OMN, in

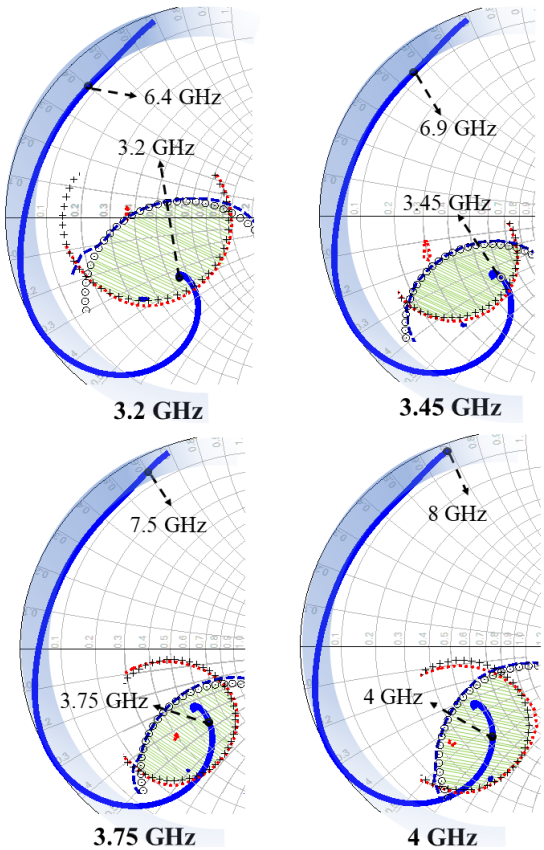


FIGURE 5: The impedance trajectory of the optimized OMN of the Auxiliary PA. The optimum regions of the load at fundamental and the suitable region for the second harmonic termination are shown by green and blue shading, respectively. The contours corresponding to Pout = 44.5 dBm and PAE = 65 % are also depicted by blue-dashed and red-dotted lines, respectively.

addition to (1), the following relations were also considered as a design (optimization) goal,

$$\begin{aligned} |\Gamma_{\mathrm{L}}(2f_i)| \geq \ & 0.9 \\ \& \qquad & \\ \angle\Gamma_{\mathrm{L}}(2f_i) \notin \ & [-90; 20] \end{aligned} \tag{2}$$

The blue ribbon on the periphery of the Smith chart of FIGURE 2 shows the allowed region for the second harmonic termination. The effect of third and higher-order harmonics on performance was observed to be too low to be of any concern.

A network composed of a multi-section transmission line (where the first section is a tapered line) with a high impedance short-circuited stub for biasing the transistor was selected to implement the OMN. Relying upon the positions of the optimum fundamental and second harmonic regions, the width and length of the transmission line sections were obtained through an optimization process setting as a goal the fulfillment of (1) and (2) starting from the impedance $2\mathrm{Z}_0' = 10\,\Omega$ (which is the impedance that the OMN of the auxiliary PA sees at the load modulated point at peak condition, as shown in FIGURE 1). FIGURE 5 shows the impedance trajectory of the realized OMN at various frequencies. It is observed that at every frequency, the fundamental falls in the optimum region, as well as the second harmonic. This concludes the design process of the OMN of the Auxiliary PA.

In a similar manner, the IMN was also designed to synthesize a source impedance inside the optimum circles of the source termination. For the source, the effect of the second harmonic termination can be ignored.

B. DESIGN OF THE MAIN AMPLIFIER

By biasing the transistor in class AB with a V_{DS}=28 V and a quiescent drain current of I_{DQ}=120 mA, load-pull simulations were performed in two conditions: peak condition wherein the transistor is saturated, and back-off condition where Pout is expected to be 3 dB lower. To achieve these conditions, in trial and error simulations, Pavs was set around 33 dBm for peak and 27.5 dBm for back-off. At peak power, similar to the Auxiliary PA, the common region between the PAE contour of 65 % and Pout contour of 44.5 dBm was considered the optimum one. For having a mathematical expression of this region, the sections of PAE and Pout contours forming the borders of the common region were approximated by arcs of two circles as shown in FIGURE 6(a), where their centers and radii are given in FIGURE 7(a) for four frequencies. At back-off, our sole goal is to maintain high efficiency since the Pout value is fixed by the selected OBO. Therefore only the PAE contour of 50 % was considered as the optimum region, which can be seen in FIGURE 6(b). This figure shows that the PAE contours can be accurately approximated by circles whose centers and radii are given in FIGURE 7(b). Source-pull simulations were performed only in the peak condition and, similar to the Auxiliary amplifier, the contours of PAE and Pout overlapped, hence only one circle is taken into account, as shown in FIGURE 7(c).

For the Main device, the destructive phases for the second harmonic termination (Γ_{L}) were also detected to be in the -90 to 20 degrees range, as shown in FIGURE 8.

Once the optimum regions for the transistor's fundamental and second harmonic terminations are defined, the IMN and OMN can be designed to synthesize a termination lies in the optimum regions. While the approach for designing the IMN is identical to that of the Auxiliary PA, the design approach for the OMN is different because a two-state matching is required in the output of the Main PA.

Referring to FIGURE 1, when the auxiliary PA is off, the OMN of the Main PA sees an impedance of Z_0' at the load modulated point. On the contrary, at peak power, when both PAs are saturated, the OMN of the Main sees a modulated impedance of $2\mathrm{Z}_0'$. Therefore, the Main PA's OMN must transfer impedances of $2\mathrm{Z}_0' = 10\Omega$ and $\mathrm{Z}_0' = 5\Omega$ to the optimum regions obtained for the peak and back-off conditions, respectively. On the other hand, for accurate modeling and design of a DPA, the loading effect of the Auxiliary on the Main PA must also be considered. At peak power

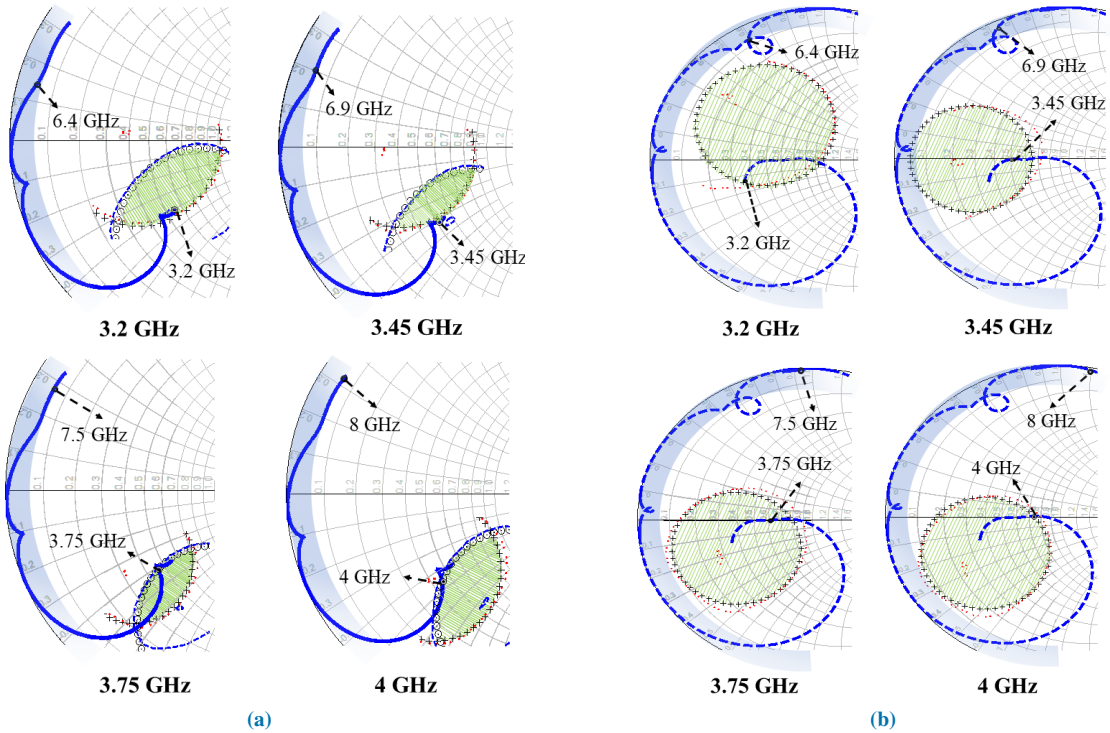


FIGURE 6: The impedance trajectory of the optimized OMN of the main PA for (a) Peak and (b) back-off conditions. The optimum regions of the fundamental load termination at four sample frequencies and the allowed region of the second harmonic load termination are also shown in green and blue shading, respectively. In (a), the contours corresponding to Pout = 44.5 dBm and PAE = 65 % are depicted by blue-dashed and red-dotted lines, respectively, while in (b), only the contours of PAE = 50 % are shown by red dots.

f [GHz]	C_{Lp}	r_{Lp}	C_{Le}	r_{Le}
3.2	$0.42\angle -95^\circ$	0.55	$0.30\angle -185^\circ$	0.40
3.45	$0.37\angle -95^\circ$	0.45	$0.33\angle -165^\circ$	0.40
3.75	$0.38\angle -88^\circ$	0.44	$0.38\angle -142^\circ$	0.35
4	$0.43\angle -78^\circ$	0.46	$0.40\angle -130^\circ$	0.34

(a)

f [GHz]	C_{Le}	r_{Le}
3.2	$0.50\angle -205^\circ$	0.35
3.45	$0.48\angle -188^\circ$	0.38
3.75	$0.50\angle -158^\circ$	0.33
4	$0.50\angle -147^\circ$	0.29

(b)

f [GHz]	C_S	r_S
3.2	$0.48\angle -104^\circ$	0.45
3.45	$0.57\angle -96^\circ$	0.37
3.75	$0.68\angle -90$	0.27
4	$0.75\angle -82^\circ$	0.19

(c)

FIGURE 7: The centers and radii of the circles defining the optimum regions for the load termination at peak (a) and back-off (b) conditions and the source termination (c) of the Main PA. Subscripts p and e stand for Pout and PAE circles, respectively.

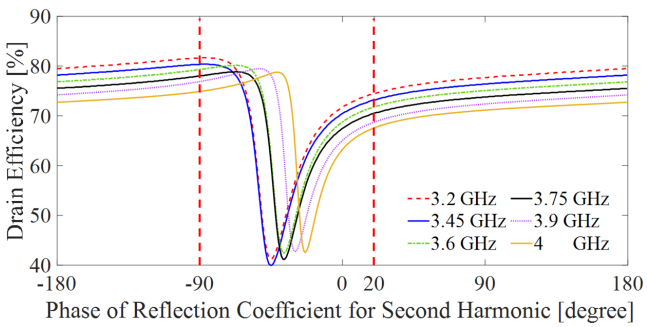


FIGURE 8: DE versus the phase of Γ_L at second harmonic (while its magnitude is fixed at 0.9) for the Main PA.

and for a symmetric DPA, both amplifiers inject almost the same current into the output load; thus, the loading effects of the amplifiers on each other can be accurately modeled by modulating the load impedance of Z_0' to $2Z_0'$. On the contrary, at back-off, the Auxiliary PA is off and plays the role of a reactive load for the Main. As shown in FIGURE 9 (a), to account for this loading effect, we have included a model of the Auxiliary (wherein the transistor is off) in the design process of the Main PA. In particular, using small-signal simulations, the output impedance of the Auxiliary PA designed in the previous stage (including its MNs) was extracted in the entire band. This extracted impedance was

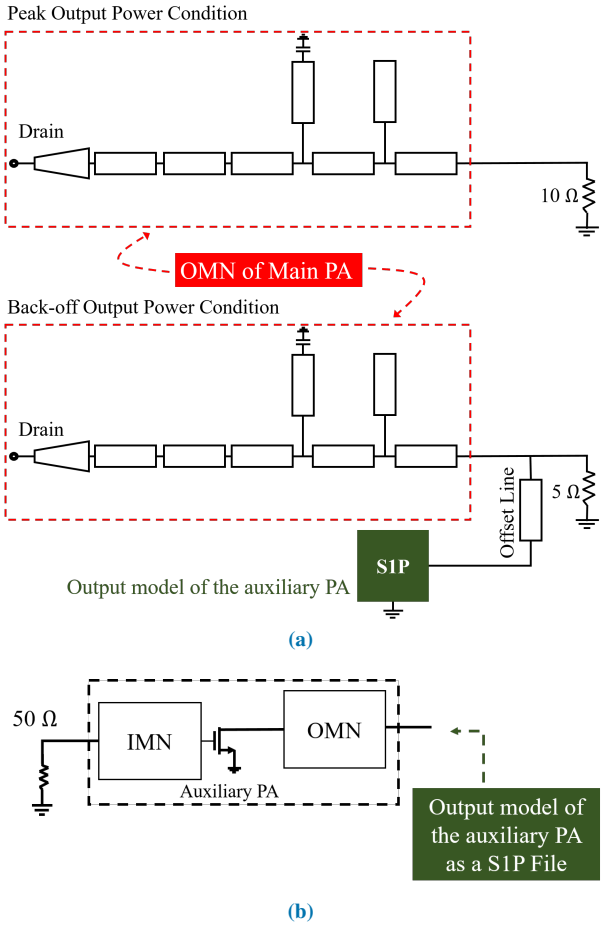


FIGURE 9: Procedure used to design the OMN of the Main PA. FIGURE 9(a) depicts a two-state matching: at peak power, the amplifier is terminated with a 10 Ω load. At back-off, the amplifier is connected to 5 Ω in parallel to an offset line which is terminated with the extracted model of the Auxiliary at back-off. This model was extracted using a simulation setup as depicted in FIGURE 9(b).

then used in the design process of the OMN of the Main in the form of a touchstone (S1P) file, as shown in FIGURE 9(b).

A multi-section transmission line network (where the first section is tapered) with a short-circuited and an open-ended stub (as shown in FIGURE 9(a)) was considered for the OMN of the Main PA. The length and width of the transmission line sections, along with the length of the offset line connecting the Auxiliary to the Main, were obtained through an optimization procedure to achieve the two-state matching conditions described previously. Also, in this case, the allowed regions for the second harmonic termination were considered as design goals. The impedance trajectory of the finalized OMN is reported in FIGURE 6. It can be seen that the trace lies in the corresponding optimum regions at both peak (see FIGURE 6(a)) and back-off (see FIGURE 6(b)) conditions. At the same time, the second harmonic in the entire band lies inside the allowed region.

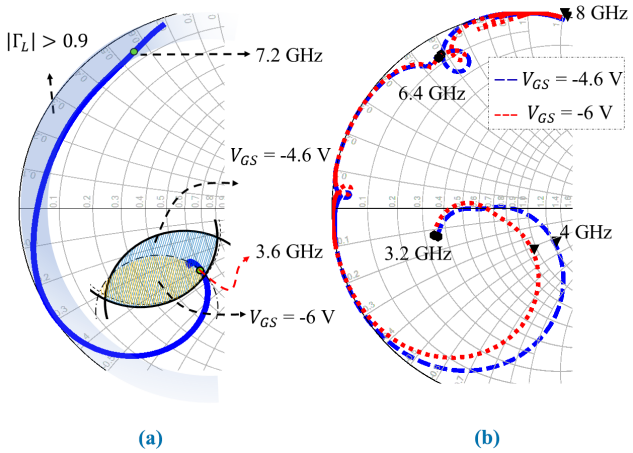


FIGURE 10: (a) Optimum load impedance region of the Auxiliary device for gate voltage from -4.6 V to -6 V. (b) Loading effect of the turned-off Auxiliary PA on the Main one at back-off for gate voltage from -4.6 V to -6 V.

C. DPA INTEGRATION

The designed Main and Auxiliary PAs were combined together, and a further investigation was carried out. In particular, being the DPA's performance significantly affected by the bias point of the Auxiliary PA, we evaluated, by performing an additional set of simulations, the effect of changing its V_{GS} on: 1) its optimum load impedances at its saturation, and 2) its loading on the Main PA when it is turned off. The results are shown in FIGURE 10 for V_{GS} within -4.6 V to -6 V. FIGURE 10(a) shows the optimum regions of Γ_L (i.e., the regions for Pout > 44.5 dBm and PAE > 65 %) at the center frequency (3.6 GHz) for V_{GS} = -4.6 V and -6 V by blue and green shading, respectively, together with the synthesized impedance across the drain of the Auxiliary device by the OMN designed in Section II-A. Notably, even if the variation of the bias point modifies the location of the optimum region, the designed OMN is flexible enough to handle such an eventual need correctly since the realized impedance at 3.6 GHz lies inside the two regions. For the same V_{GS} values, FIGURE 10(b) reports the behavior of the loading effect of the turned-off Auxiliary PA on the Main one at back-off. Clearly, different V_{GS} values lead to different touchstone models of the Auxiliary PA (see FIGURE 9(b)), which results in different impedances synthesized at the Main device's output at back-off as observed in FIGURE 10(b). However, it can be seen that this effect is not dramatic, and the impedance trajectories are not far away.

At the input, a Gysel power splitter [27] is adopted to equally split the power between the two PAs. Compared to a Wilkinson power divider, Gysel's grounded resistive terminations help with better power handling, and by keeping parasitic capacitances out of the main signal path, unlike a Wilkinson divider, the parasitics do not play a significant role here. Suitable delay lines were calculated and inserted in the input path of the amplifier branches to ensure zero loss in power combination at the output.

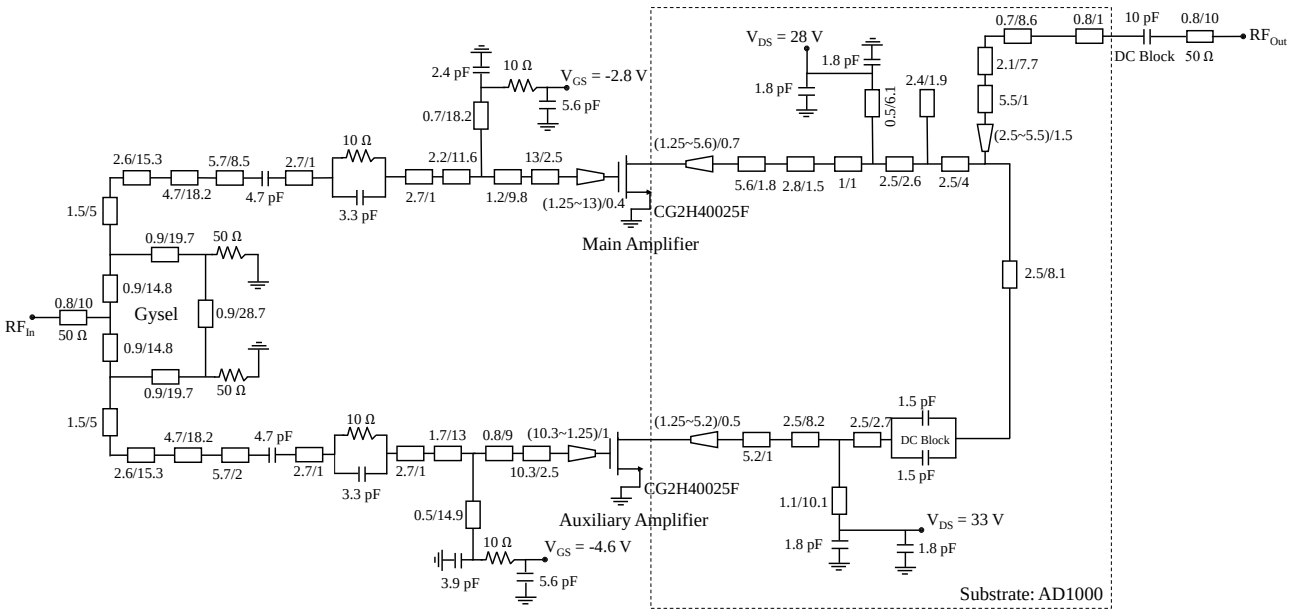


FIGURE 11: Schematic of the designed DPA. Transmission line width and length (W/L) are reported in millimeters.

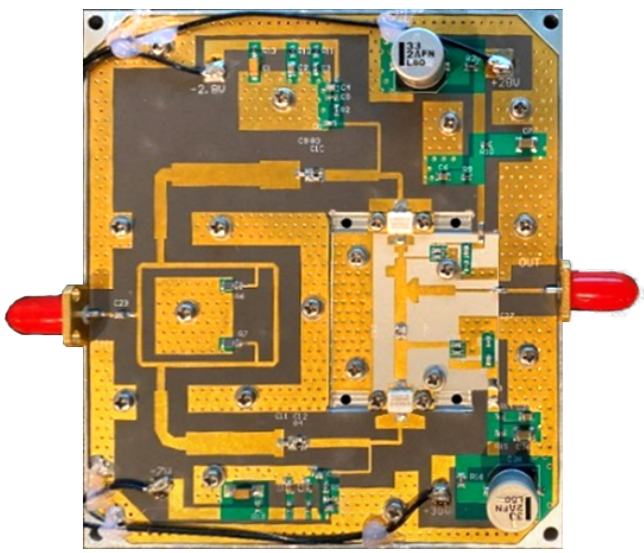


FIGURE 12: Picture of the fabricated DPA.

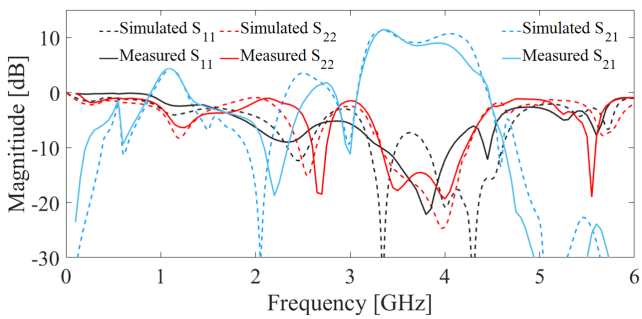


FIGURE 13: Comparison between measured and simulated S-parameters of the DPA.

The DPA was then completed with a three-section post-matching circuit that transforms $Z_0' = 5\,\Omega$ to the standard load $Z_0 = 50\,\Omega$.

A schematic of the realized DPA is reported in FIGURE 11, whereas a picture is shown in FIGURE 12. It is worth mentioning that the DPA was designed and fabricated on two different substrates. The input splitter, IMNs, DC source connections, and a small 50 Ω line at the output were fabricated on a 10-mil RT/duroid 5880 substrate. The OMNs were fabricated on a 10-mil AD1000 substrate. The difference in substrate material is because of size considerations, where the higher dielectric permittivity of AD1000 helps with the miniaturization of the OMNs, which in turn helps with arranging the whole design.

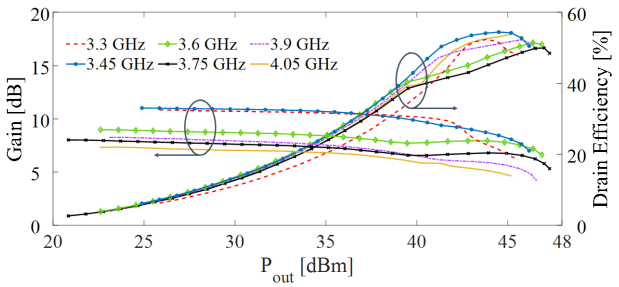
III. RESULTS

Before performing high-power tests on the fabricated amplifier, its small-signal parameters were measured and compared with the simulation results. The S-parameters measured in the biasing condition $V_{DD,Main}$=28 V and $V_{GS,Main}$=-2.6 V, $V_{DS,Aux}$=32 V and $V_{GS,Aux}$=-9 V, are reported in FIGURE 13, showing a good agreement with the simulated counterpart.

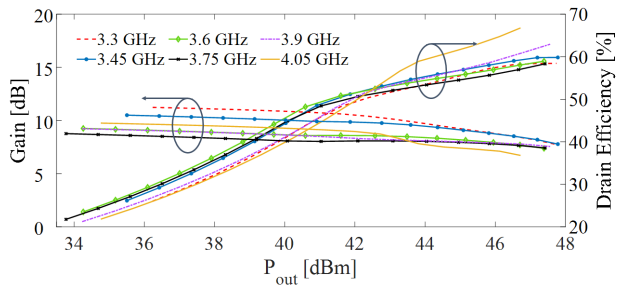
After that, the DPA was tested in continuous wave (CW) conditions. For each frequency in the band, the input power was swept from 20 dBm until the saturation was observed. FIGURE 14(a) shows the registered DE and gain as functions of the output power at various frequency points. Notably, the efficiency traces clearly show the trademark behavior associated with a DPA, signifying the fact that the Auxiliary transistor is tuned on properly and the load pulling is affecting the Main amplifier correctly. FIGURE 14(b) shows the simulation results that are reasonably in agreement with the

TABLE 1: Comparison between S-band DPAs.

Ref.	Operating Freq. [GHz]	Fractional BW [%]	Minimum saturated P_{out} [dBm]	DE @ peak [%]	DE @ back-off [%]
[28]	3.1 - 3.7	18	43.1	65 - 72	40 - 45 @ 8 dB OBO
[29]	3.05 - 3.55	15	42.3	61 - 75	51 - 65 @ 6 dB OBO
[30]	2.8 - 3.55	24	43	66 - 78	50 - 60 @ 6 dB OBO
[31]	3.4 - 3.6	6	46.6	63 - 66	47 - 49 @ 12 dB OBO
[32]	3.4 - 3.5	3	49.5	59 - 63	46 - 50 @ 6 dB OBO
[33]	2.8 - 3.6	25	43	62 - 76.5	44 - 56 @ 6 dB OBO
This Work	3.3 - 3.9	17	45.6	48 - 53.2	35 - 45 @ 6 dB OBO



(a)



(b)

FIGURE 14: Measurement (a) and simulation (b) results of the fabricated DPA. DE and gain are plotted vs output power.

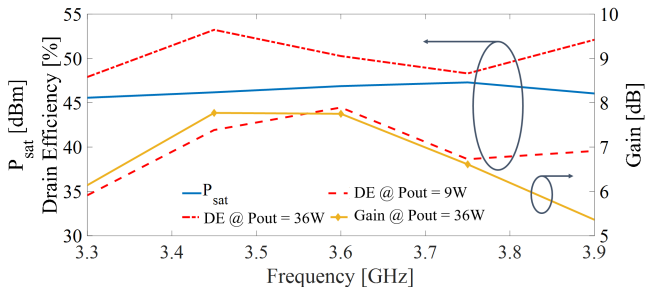


FIGURE 15: Measured saturated output power, peak and back-off efficiency, and power gain of the fabricated DPA in the entire frequency band.

measurements.

In FIGURE 15, the measured performance of the DPA are reported versus frequency. The amplifier shows a working bandwidth of 600 MHz, from 3.3 to 3.9 GHz (n78 channel of 5G-NR). In this frequency range, it delivers at least 36 W (45.6 dBm) of saturated output power. The power gain and DE at this level of Pout (i.e., 36 W) and the DE at 6 dB of back-off from this level (i.e., 9 W) are also reported in the figure. It can be seen that the DE varies between 48 – 53.2 % (PAE of 36.2 – 44.2 %) at peak (36 W) and between 35 – 45 % (PAE of 30.3 – 37.7 %) at back-off (9 W) as reported in TABLE 1. The table also compares the performance of the fabricated DPA with other S-band DPAs reported in literature. Notice that the two DPAs with a saturated Pout higher than this work have very narrow bandwidths, and the ones with comparable bandwidths have significantly lower Pout.

IV. CONCLUSION

Evolving communication standards require improved methods for designing subsystems, including power amplifiers. This paper presented the design of a quarter-wave transformer-less DPA using an improved method. By performing standard load- and source-pull simulations and considering proper target values of Pout and PAE, the optimum regions of the fundamental and second harmonic terminations of the transistor were obtained for the Auxiliary at peak power and for the Main at peak and back-off power conditions. By approximating the Pout and PAE contours by circles, mathematical expressions were derived for the optimum regions, which were then applied as optimization goals in the design process of the MNs. Furthermore, in the design process of the Main PA's OMN, for more accurate modeling of the loading effect of the Auxiliary on the Main PA at the back-off condition and hence a more precise design of the Main, a model of the output impedance of the Auxiliary amplifier (when its transistor is off) was used.

The proof of concept amplifier was designed and built for the n78 band of 5G-NR. In the frequency band from 3.3 to 3.9 GHz, which corresponds to a fractional bandwidth of 16.7 %, it achieved a minimum saturated output power of 36 W, while maintaining a DE of around 50 % at saturation (36 W) and 40 % at 6 dB output back-off.

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