Planar antenna design and channel modeling for chip-scale communications

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Abbreviations

AlN Aluminium Nitride

CEM Computational Electromagnetic Methods

Ds Delay Spread

GHz Gigahertz

mmWave Millimeter Wave

NoC Network-on-Chip

PDP Power-Delay Profile

PEC Perfect Electric Conductor

THz Terahertz

TSV Through-Silicon Via

WNoC Wireless Network-on-Chip

Abstract

The need to handle the communication demands of growing multicore processors have created a framework where Wireless Network-on-Chip (WNoC) appears as a promising complement to wired chip interconnects. In this thesis, a planar antenna design is proposed to characterize the yet largely unknown wireless channel within realistic chip packages. This work addresses the issue by modeling a flip-chip package and designing an antenna at 250 GHz, seeking it to be readily integrable in the package and the enabler of a low-loss (although probably highly reverberating) wireless channel across the package. Through simulation-based parametric studies of antenna and package configurations, and placing multiple antennas in the package, path losses and delay spread measurements are obtained to characterize the deterministic channel within a chip. We demonstrate that a wireless link around 220–230 GHz in a reverberant cavity on top of the chip package can be created with patch antennas, achieving a path loss in the range of 2–10 dB and delay spreads in the sub-nanosecond range, although time-domain results are limited in our case to computational constraints of the simulations.

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1 Introduction

"There is plenty of room at the bottom" is the name of the talk by physicist Richard Feynman, on December of 1959, where the ideas and concepts behind nanoscience and nanotechnology were born, long before the term nanotechnology was defined. A lot has been achieved since.

Recent years have witnessed promising advances in nanotechnology, which have led to rising research interest in such field from diverse backgrounds, namely environmental sciences, biomedicine, technological industry, electronics or communications [3].

In the field of semiconductors and computer engineering, nanotechnology has also had a large impact. Advances in nanotechnology have consistently led to smaller transistors, gradually increasing the transistor density and the capabilities of computer processors following the so-called Moore's law [4]. Yet such an increase in transistor density, which had traditionally led to proportional improvements in computing speed through higher operating frequency, started to give diminishing returns around in terms of efficiency around a couple decades ago.

To remedy this, the industry shifted from single-core to multicore designs where multiple processor cores were integrated on the same die [5]. Hence, instead of pushing the operation frequency, thread-level parallelism was exploited to keep increasing the computing speed of processors. This shift from single-core to multicore chip architectures, which was done to increase performance while maintaining the power consumption and complexity constant, made communication between the different processor cores of a computer very important.

To handle the communication demands of growing multicore processors, the terminology Network-on-Chip (NoC) appeared [6]. NoCs consist of a set of wired connections and on-chip routers forming a packet-switched integrated network. Despite that NoCs work well with a moderate number of cores, they can become a limiting factor in processors as the number of cores increases (which is done to theoretically keep increasing the computational speed of processors), since this translates in an increase on the average number of routers needed to reach the destination. In the end, this leads to an important raise of the latency and energy consumption across the on-chip network. This is especially critical in collective communication patterns, where a number of transmitters need to send messages to many receivers simultaneously. In the wired case, this means the transmission of multiple identical messages that flood the network [7].

The above-mentioned limitations have created a framework for research, where Wireless Network-on-Chip (WNoC) appears as a complement to the wired interconnects. An schematic of a WNoC scenario is presented in Figure 1 [1]. WNoC take advantage of a network formed by a set of antennas: the transmitter core serializes and modulates the information to be transmitted, which travels through the computing package until reaching the receiver antennas that pick up the signal, demodulate and desearialize it. Given the intrinsic absence of path infrastructure, these wireless chip-scale communications exhibit considerable promise [1, 8], as they allow to overcome pin constraints and increase versatility by offering low-latency broadcast capabilities across the computing package.

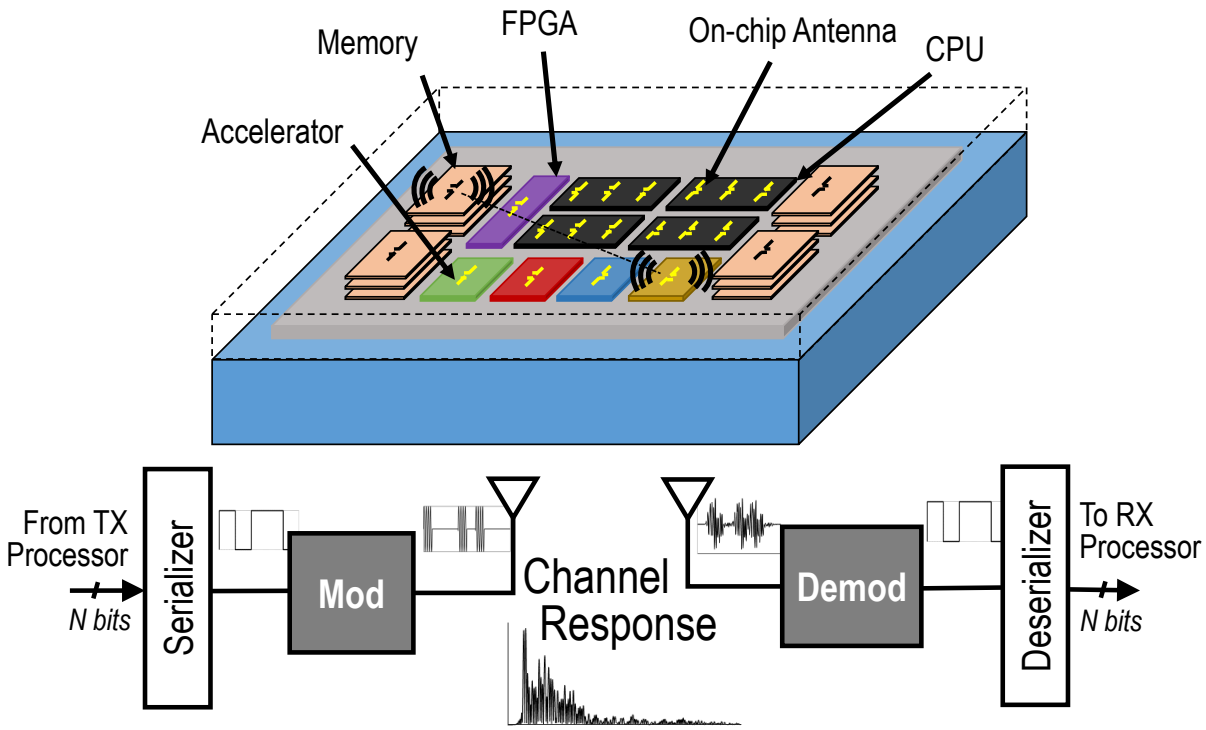


Figure 1: Schematic representation of a WNoC environment and its wireless communication process [1]

Theory on wireless on-chip communication is well studied and several works exist at different levels of abstraction, including modulations, medium access control protocols, or network architectures [8]. However, a key ingredient is missing: wireless channel characterization. In principle, WNoC would be integrated within a computing package alongside the digital processor circuits, which imposes several restrictions on the antennas and the propagation, yet only a few studies on channel characterization for WNoC include realistic chip packaging and antenna designs, as we describe in Chapter 2 [1]. As a relevant example, in [7], the authors consider standard flip-chip package with monopoles. However, due to the placement of the antennas inside the lossy bulk silicon, this option exhibits significant path losses. Instead, placing planar antennas in a micro-reverberation chamber created between the bulk silicon and the heat sink in a process compatible with commercial packages and manufacturing processes, is an alternative worthy of exploration pending a sufficient characterization of a lossy channel.

1.1 Objectives

To bridge the aforementioned gap, this thesis aims to model a low-loss channel inside of a computing package assuming realistic antennas and package configurations, in order to study low-power wireless communications between on-chip antennas. To make the model realistic, we need to consider antennas that could be integrated within the chips. In this case, the aim is to design a planar antenna that is integrated and could operate within

a computing package, to then explore the wireless communication channel within the package. The main objectives of this research project are listed below:

- To design a planar antenna that is integrable in the on-chip environment and capable of transmitting close to the terahertz band, ensuring that satisfies quality criteria of bandwidth and integration.
- To asses the impact of non-idealities and integration-related impairments on the performance of the antenna.
- To model the channel in a low-loss and highly reverberant media, as is a chip package, using the designed antenna.

Such goals are considered to be met if the requirements and specifications in Section 1.2 are accomplished.

Through the development of this research, we have been able to design an antenna that resonates at 250 GHz, which allowed us to study how it operates within a realistic flip-chip and how the size of the chip and the thickness of the heat spreader affect communication in a reverberating medium. This will be further detailed in Chapter 4. The choice of frequency is, on the one hand, motivated by the desire to increase the frequency to reduce the footprint of the antennas and limited, on the other hand, by the maximum frequencies supported by current CMOS compatible technologies around 300 GHz [9].

1.2 Requirements and specifications

The primary goals of this thesis, as previously indicated, are to characterize the communication channel between the designed planar antennas in a realistic flip-chip packaging by monitoring its delay spread and path losses.

The following requirements and specifications have been considered in that regard. Such requirements have been summarized in the following list:

- Throughout the development of this project, research should provide a planar antenna design that is readily integrable in on-chip environments and capable of transmitting at different channels at the higher end of the spectrum of the millimeter-wave band (30-300 GHz) with low loss.
- To this end, the design should consider the limitations imposed by the chip package structures, CMOS fabrication processes, or placement of the feeder circuits. Also, it should be aware of all the impairments and non-idealities related to the chip packages in terms of the presence of lossy materials and media.
- Finally, the antennas should be readily usable for the study of the wireless channel within the reberverant media where communications on-chip will take place.

Regarding the specifications, they are listed as follows:

- Return losses of the antenna at the frequency of resonance below -10 dB.

- Relative bandwidth of the antenna above 1% at -3 dB, prior to integration in the flip-chip package.
- Proof of operation at distinct frequencies between 60 GHz and 300 GHz.
- A coherence bandwidth B_{coh} of the channel above 1 GHz.
- A realistic flip-chip package of 15×15 mm^2, upon which the antenna would be implemented.

1.3 Organization of the thesis

The structure of the remainder of this thesis is as follows. Chapter 2 discusses related works and state of the art in flip-chip packages, NoC, WNoC and on-chip antenna designs. Chapter 3 describes antenna design, simulation methodology and subsequent channel modeling, whilst Chapter 4 presents the main results obtained. Finally, Chapter 5, concludes the thesis while reflecting on the objectives, requirements and specifications as well as results.

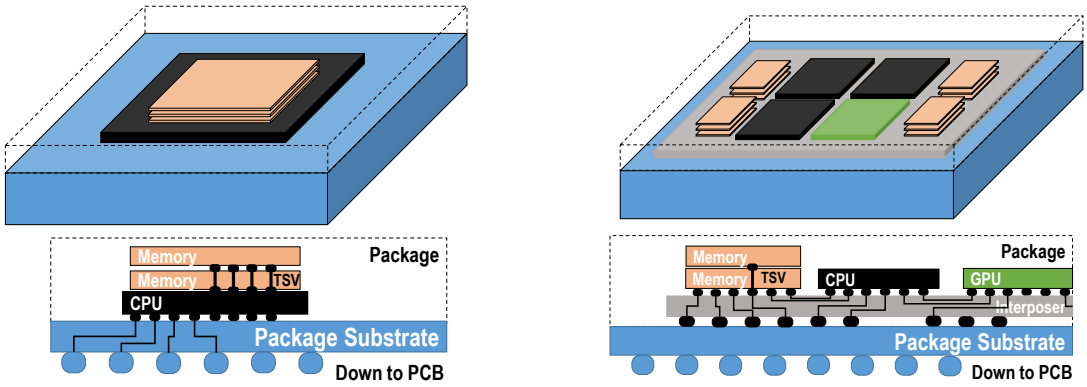
2 Background and state of the art

This chapter presents the state of the art for technologies used throughout this thesis, such as chip packaging, on-chip antennas, similar planar antenna designs in environments that are not fully integrated, and channel models previously studied.

2.1 Chip packaging

Understanding the chip environment is fundamental in the antenna design process. First, the intra-chip region, in which antenna radiation goes through chip layers, and the inter-chip region, in which electromagnetic waves that leave the intra-chip region travel to another chip, are the two places where electromagnetic propagation occurs. Based on the positioning of the antennas, frequency band and packaging selection, different materials and layers will become more relevant to propagation in the aforementioned regions [1].

At the level of the chip, comprehending packaging alternatives is critical as they are highly relevant to intra-chip propagation. Generally, flip-chip packaging and wire bonding, as well as their application-specific variants, have been the most prevalent packaging methods. Nowadays in the context of general-purpose multiprocessors, flip-chip packaging is preferable due to its lower inductance, because of shorter wired interconnections, as well as higher power and bandwidth density [10]. The fabrication process of this type of packaging consists on placing a set of solder bumps on the chip's pads and then, carefully flipconductorg it over to connect it to the system substrate or interposer, depending on whether the integration is traditional or 2.5D [1], as represented in Figures 2a and 2b, respectively.



(a) 3D chip package

(b) Interposer-based chip package

Figure 2: Schematic representation of different integrated computing packages relevant to this thesis [1]

Subsequently, the packaged flip-chip adopts the standard shape shown in 3. With the system heat sink and heat spreader, made of a material with good thermal properties and low electrical losses, on top of a silicon substrate with low resistivity to dissipate

heat away from it [1]. Below the silicon, the metallization layers are surrounded by an insulator material, usually silicon dioxide, with the solder bumps below it [11]. It is worth noting that the transistors and circuits making up the processors and transceivers are implemented in the interface between the silicon and the insulator, and hence antennas should be connected here.

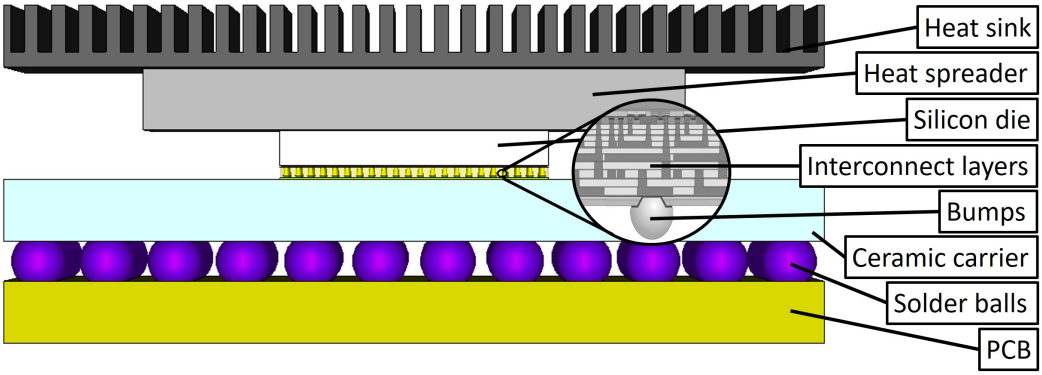


Figure 3: Schematic representation of flip-chip packaging layers [2]

As with the positioning of the antenna, the dimensions and selection of each material that makes up the chip package are crucial, as they have a direct effect on electromagnetic wave propagation. As seen in [7], the heat spreader and (most notably) the bulk silicon substrate contribute the most to propagation losses. Hence, in this thesis, we will try to avoid using the bulk silicon as propagation medium while designing an antenna that can be integrated in commercial packages with relative ease.

2.2 On-chip antennas

For structures with sub-micrometric dimensions and nanometric precision, major advancements have made it possible to overcome traditional fabrication limitations, which has enabled the miniaturization of the antennas. Working in a micrometric chip package milieu, as is the case for WNoC, necessitates the use of very high communication frequencies to enable miniaturization of antennas, which radiate when their greater dimension corresponds to half of the wave length.

The need of antennas with dimensions in the sub-micrometric range enable their integration means that, as stated in the previous paragraph, their working frequency is in the millimeter-wave band and above. Working at such high frequencies means that narrowband antenna designs namely monopoles and patch antennas, that commonly have a bandwidth approaching 1% of their resonance frequency. Hence, for millimeter-wave antennas, we can achieve an expected bandwidth of a few GHz. However, the disadvantage of its small size is that its effective area decreases quadratically with its wavelength, as a result, its capacity to convert power from an incoming wave into current during reception is substantially diminished [1].

The placement of the antenna within the package is another key design aspect worth taking into consideration. Placing them as far apart as possible from the lossy silicon, as proposed in various works, is not realistic because the antenna would be short circuited by the solder bumps. In addition, printed dipoles and patch antennas can be implemented in the metal layers closest to the silicon. However their co-planarity has been found to increase the losses, while their proximity to the solder bumps, which operate as a virtual ground plane, reduces their the efficiency.

Another antenna design that has recently been studied by fellow researchers at NaNoNetworking Center in Catalunya (N3Cat) is the use of Through-Silicon Vias (TSV) as quarter-wave monopoles. Taking into account the imaging theory, by using the solder bumps as their virtual ground plane, monopoles would radiate like half-wave dipoles and due to their vertical orientation they would radiate horizontally to the other antennas [7, 12].

The main characteristics of common on-chip antennas for free-space applications that have been proposed for its use in the inter-/intra-chip communications domain are summarized in Table 1 [1]. Note that the presence of planar patch antennas or, in general, on-chip at frequencies beyond 200 GHz is rare in the literature. In this thesis, we aim to develop an integrable patch antenna at 250 GHz.

Antenna Type	Direction	Position	Characteristics	Frequency [Ref]
Printed Dipole	Horizontal	Within insulator	Easy to manufacture, but has end-fire null	15 GHz [13], 60 GHz [14],150 GHz [15]
Meander/zig-zag	Horizontal	Within insulator	More complex, but more compact than dipole	15 GHz [16], 25 GHz [17],60 GHz [18]
Circular antenna	Horizontal	Within insulator	Better omnidirectionallity at the chip plane	60 GHz [19],100 GHz [11]
Vivaldi antenna	Horizontal	Within insulator	Broadband and directional, but also complex	180 GHz [20], 200THz (optical)[21]
Bond-wire antenna	Vertical	Off-chip	Reuses bond-wiring process, but is hard to tune	20 GHz [22], 43 GHz [23], 200 GHz [24]
Vertical monopole	Vertical	Through Silicon	Coplanar radiation, embedded in lossy silicon	60 GHz [25], 120 GHz [26]
		Through dielectric	Coplanar radiation, extra packaging steps	20 GHz [27], 150 GHz [15], 160 GHz [12]
Folded Monopole	Both	Through and on top	Uses vertical dimension to shorten the footprint	60 GHz [28], 77 GHz[29]

Table 1: Summary of integrated antennas compatible with the intra-/inter-chip communication situation

2.3 Channel models previously studied

With the emergence of mmWave integrated antennas and small transceivers, the study of wireless communication channels for WNoC has garnered the most interest in the last decade. The first measurements between antennas located within the same chip were unveiled in [13, 16, 30], which worked at the 6–18 GHz, way below the bands used nowadays in other wireless systems. These works discussed the role in communications of the dielectrics used for thermal purposes, the potential impacts of the chip package on communications and the highly lossy channel, around 50 dB for several millimeters distance, way above the expected 26.5 dB for modern mmWave transceivers.

The interest in antenna design and channel modeling for this sort of communications was not revived until the late 2000s, when advancements in integrated antennas [14] and new investigation lines in the WNoC [31] rekindled the interest. In the past few years, various paper publications have focused the majority of efforts in the more developed and familiar bands between 20 and 60 GHz [17, 19, 23, 27, 28], with a few ventures into frequencies above 100 GHz [15, 18, 12].

Frequency domain analysis has motivated the majority of research, demonstrating the significance of the path loss to the viability of chip-scale communications. Research in [32], by means of full-wave simulations of a standard flip-chip package with vertical monopoles in the silicon layer, confirmed that for a few centimeters distance, path losses could be in excess of 70 dB. While most of the attempts to reduce path loss have achieved their objective resorting to non-standard packages and layers [33, 28, 19]. In [7], Timoneda *et al.* studied the impact of silicon and thermal interface material thicknesses in TSV-based links, working as quarter-wave monopoles, within a flip-chip package, taking chip-wide losses near 30 dB. In that paper, it was also mentioned that the metallization layers within the chip or the interposer would likely block the signals due to the narrow pitch of these layers in comparison to the wavelength of the electromagnetic waves propagated. Finally, it is important to note that other factors, like as the orientation or placement of the antenna, also have an effect in ways compatible with standard packaging [34].

In contrast with path loss levels ensuring acceptable values to establish communications, very few studies have considered the time domain therefore, the dispersive nature of WNoCs is still yet to be fully characterized. Which is crucial since as higher the dispersion, the lower the coherence bandwidth, and hence more limited symbol rate [1].

Matolak et al. predicted, in their theoretical work, worst-case values of several nanoseconds when a micro-reverberation chamber model at mmWave and THz bands [35]. This is due to the model assuming full encasement and not taking into consideration dielectric losses, then increasing the importance of reflections [1]. In measurements with open chip, on the other hand, delay spread around 100 ps was achieved for frequencies between 30 GHz and 60 GHz [36].

Planar antennas design for on-chip communications and its channel is still yet to be fully characterized. Few studies have used this type of designs, and those that have been presented have a central frequency at 60 GHz [37] studied a log-planar antenna with an open chip model, while [19] used a circular patch design with a custom flip-chip package. However, Timoneda, fellow former N3Cat researcher, studied a patch design with a realistic flip-chip packaging with realistic antenna placement also at 60 GHz with monopoles [2], a recurrent problem with monopole antenna designs is that, due to the placement of the antennas inside the lossy bulk silicon, results exhibits significant path losses and low antenna gain. Instead, placing planar antennas the micro-reverberation chamber, created between the bulk silicon and the heat sink in a process compatible with commercial packages and manufacturing processes, is an alternative worthy of exploration pending a sufficient characterization of a lossy channel.

Therefore, the need to fill the research gap for planar antennas on WNoC and their channel, create a framework for this thesis which, as stated in Chapter 1, aims to design an integrable planar antenna capable of transmitting at 250 GHz, well above the typical frequencies used in studies shown in Table 1. Such an antenna would be integrated inside a standard chip package placing the antennas in a micro-reverberation chamber created between the bulk silicon and the heat sink. More than one antenna would be simulated to characterize the wireless communication channel in a reverberant medium with less losses than those studied with monopole antennas within bulk silicon [2].

3 Methodology

The methodology followed in this thesis is summarized in the block diagram shown in Figure 4, which is divided into three main parts. The first building block is research, where the essential basis for initiating the design phase is created through the study and comprehension of the state of the art. CST is the following block, where the modeling and design of the antennas, their feeding, and their simulation to assess their behavior are all performed. The outputs from the simulations done in CST are post-processed in the MATLAB block, where the communications channel is studied.

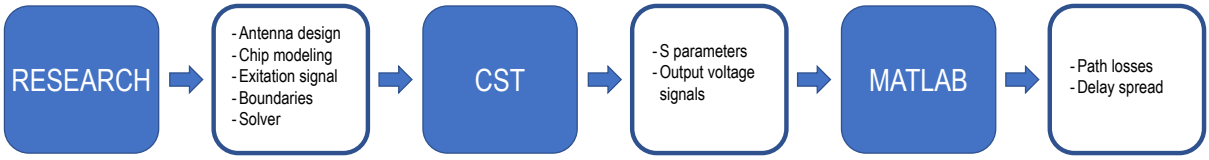


Figure 4: Block diagram of the methodology of the thesis

3.1 CST Microwave Studio

The software chosen to carry out this thesis is CST studio a full-wave electromagnetic solver, that provides an environment in which modeling, design and simulations can all be carried out. This program runs computational electromagnetic methods to solve Maxwell equations with boundary conditions for computing the electromagnetic fields in a propagation medium, divided into time-domain and frequency-domain methods, which are going to be used to obtain path losses and delay spread to characterise the channel.

With the cost of significant computing needs, full-wave simulations can be utilized to develop channel models with extremely high precision. In general, if the space in which Maxwell's equations must be solved is sampled with a resolution of around a fifth of the wavelength corresponding to the greatest frequency of interest, the solution obtained using Computational Electromagnetic Methods (CEM) from CST is accurate [1].

As we are going to be working at high frequency bands, the upper spectrum of the mm-Wave band, it is convenient to describe a given network in terms of waves rather than voltages or currents. When exposed to various steady state electrical signal stimuli, linear electrical networks exhibit certain electrical behaviors that are described by scattering parameters, also known as S-parameters. The S-parameters in this case will offer data that will be utilized to assess the antenna design, and once some of the data has been processed in Matlab, path losses will be determined.

In order to evaluate the coherence bandwidth and channel dispersion, we will provide the S-parameters to a MATLAB script, while to acquire the delay spread we will use the values from the outputs at the various ports.

3.1.1 Antenna design

The design process behind the planar antenna consisted on, firstly, having a model that

worked well at lower frequency bands and in free-space and then scale it up to the desired radiation band also in free-space, performing various parametric sweeps to optimize its behaviour. Once that was accomplished, layers of the flip-chip design were added, first silicon and then aluminium nitride, while monitoring the design parameters to ensure that it still functioned as intended. The final steps would be to simulate two of such designed antennas, with various configurations, within the whole flip-chip package to obtain data that enable us to analyze the WNoC channel in the reverberant media where the antennas are located.

The rectangular patch antenna equations from [38] were used to design the dimensions of the patch antenna. The first step is to define the wavelength of the frequency of resonance, that can be obtained by means of

$$\lambda_0 = \frac{v_0}{f_0\sqrt{\varepsilon_r}}, \tag{1}$$

where v_0 is the speed of light in the vacuum, f_0 the frequency of resonance and ε_r the electric permittivity of the substrate.

On the one hand, the patch width W is obtained using

$$W = \frac{1}{2f_r\sqrt{\mu_0\varepsilon_0}}\sqrt{\frac{2}{\varepsilon_r+1}} = \frac{v_0}{2f_r}\sqrt{\frac{2}{\varepsilon_r+1}}, \tag{2}$$

with μ_0 and ε_0 being the permeability and permittivity of vacuum.

On the other hand, the nominal value of the patch length L is:

$$L = \frac{1}{2f_r\sqrt{\varepsilon_{eff}}\sqrt{\mu_0\varepsilon_0}} - 2\Delta L, \tag{3}$$

where ε_{eff} is the effective permittivity of the substrate.

However, due to the fringing effects, electrically the patch looks larger than its physical dimensions. A widely used and accepted practical approximate relation for the extension of the length ΔL, normalized to the substrate thickness h, is:

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{eff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{eff}-0.258)\left(\frac{W}{h}+0.8\right)}. \tag{4}$$

where ε_{reff} is, for $W/h > 1$:

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[1+12\frac{h}{W}\right]^{-1/2} \tag{5}$$

Finally, the effective length L_{eff} of the patch is:

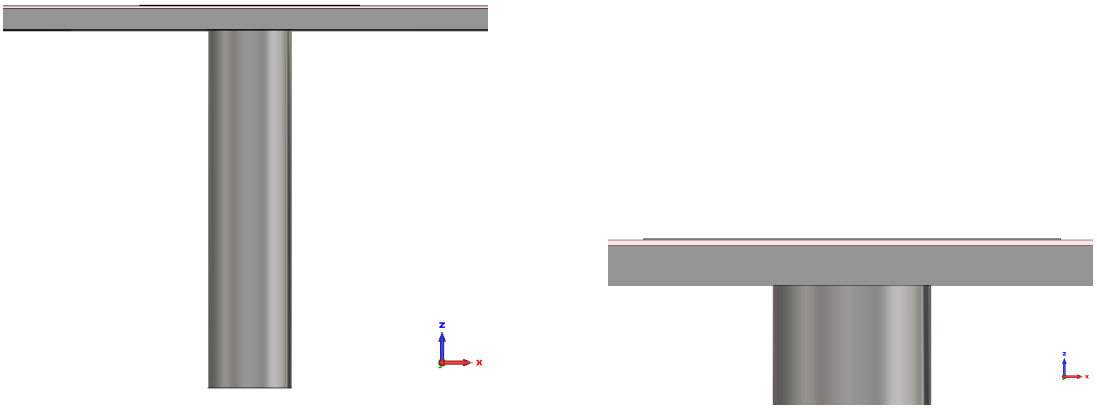
$$L_{eff} = L + 2\Delta L \tag{6}$$

For the feeding method, because of the antenna's placement, a coaxial feeding line would be the best approach, as of now. A simpler pin feed would not be effective due to the need

to traverse the lossy bulk silicon to contact the antenna with the transceiver circuits that feed the antenna. Since the antenna would be working near the THz band, due to the wavelength used, the coaxial would not be too thick. The insulator used for the coaxial feeder is the commonly used PTFE, which is very non-reactive and has a low dielectric constant, $\varepsilon_r = 2.1$. At first, the coaxial dimensions were calculated using a macro that CST provides, which takes as input the permittivity of the insulator between the two conductors and the desired working frequency, and outputs the internal and external conductor radius. However when scaling up the resonance frequency of the antenna, parametric sweeps of the internal and external radius of the coaxial, as well as the the thickness of the external conductor were performed to obtain the most suitable dimensions leading to the best antenna matching and lowest losses.

The first substrate used was FR4, a commonly used substrate for integrated circuits, with a nominal permittivity of $\varepsilon_r = 4.30$ that allows a low thickness, from 0.05 mm to 100 mm which is very relevant for this design. However, due to its poor performance in terms of losses at 250 GHz and effects in frequency displacement, FR4 was replaced by polyamide, changing relative permittivity from $\varepsilon_r = 4.30$ to $\varepsilon_r = 3.50$ and from an electric $tan\delta = 0.025$ to $tan\delta = 0.0027$, reducing return losses and improving in frequency displacement.

Figure 5 illustrates the cross section of the antenna, from top to bottom, the patch, the substrate in soft red, the ground plane in grey and and also in grey, but vertically, the coaxial feeder. Figure 5b is a close up from Figure 5a that enables to better perceive the components of the antenna mentioned.



(a) Cross section of the antenna

(b) Close up of the cross section

Figure 5: Schematic representation of the cross section the antenna

The S_{11} parameter, which is the ratio of the input signal that is reflected from the front of the connection to the input signal incident to that port, has been examined to assess the return losses and, hence, to validate the performance of the antenna throughout its iterations. In this study, a good design was defined as one with return losses below -10 dB, since if the power delivered at the port is generally 0 dB, and $S_{11} = -10$ dB, implies that

-10 dB is the reflected power, which means that 90% of the power delivered at the port is finally delivered to the antenna, whereas the remaining 10% of the power is reflected.

Figure 6 shows a 3D representation with the patch on top, the substrate in red, the ground plane below it, and the coaxial feeder in vertical position.

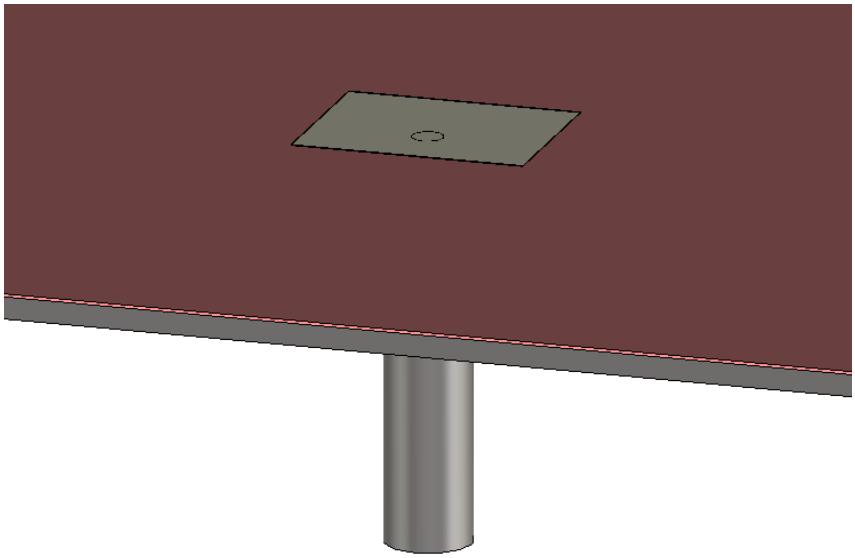


Figure 6: Schematic 3D representation of the antenna

3.1.2 Flip-chip package modeling

Prior to being able to study the propagation channel, it is necessary to model the flip-chip scenario where communication will occur.

The first step was to add a silicon layer, Si, to an scenario with two antennas and a ground plane of 4×4 mm^2, that covered the whole exposed coaxial, from the ground plane to the discrete port. By comparing the results with the model without a Si layer, we checked if the feeding coaxial was properly insulated.

As the results were satisfactory, we proceeded to add to the scenario a layer of aluminium nitride, AlN, covering the antennas. With it we first performed simulations with a ground plane of of 4×4 mm^2, like in the previous step, with different thiknesses for the AlN. In order for the chip model to be realistic, we changed the boundary condititions to perform like a perfect electric conductor where all the tangential electrical fields are 0. This boundary would act like the packaging of the chip, and it would be set for all five faces of the model except for the face that contained the excitation ports.

Then the following iteration, was to increase the dimensions of the environment to 15 $\times$ 15 mm^2 and perform simulations with different distances between antennas, these are always referred to distance from the center of one patch to another.

These last two types of simulations would provide us the data necessary, S parameters and output voltages from each antenna, to later study reverberant communication channel

thanks post-processing the data obtained using MATLAB, as presented in Section 3.2.

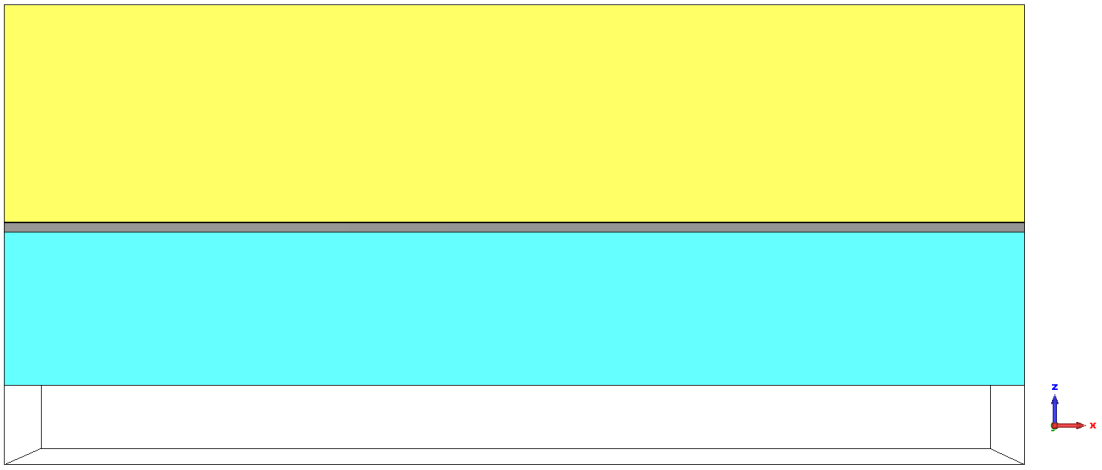


Figure 7: Schematic representation of flip-chip packaging layers modeled

Therefore, the final flip-chip package model, represented in Figure 7, has four layers modeled, plus the boundary conditions that act as the packaging of the chip, listed below, from top to bottom:

1. AlN, in yellow, serves as a heat spreader in virtue of its good thermal properties and low electrical losses [7].
2. Polyamide, the thin black layer, performs as the chip and antennas' substrate.
3. Conductor, in grey, layer that work as the ground plane for the antennas
4. Bulk silicon, in cyan, serves as the foundation of the transistors, since its low resistivity make it suitable for the operation of transistors, however not for electromagnetic propagation [39].

Due to the fact that our focus is to provide energy to the micro-reverberation chamber to be able to study its channel, nothing below the silicon, such as the insulator or solder bumps, has been added to the model.

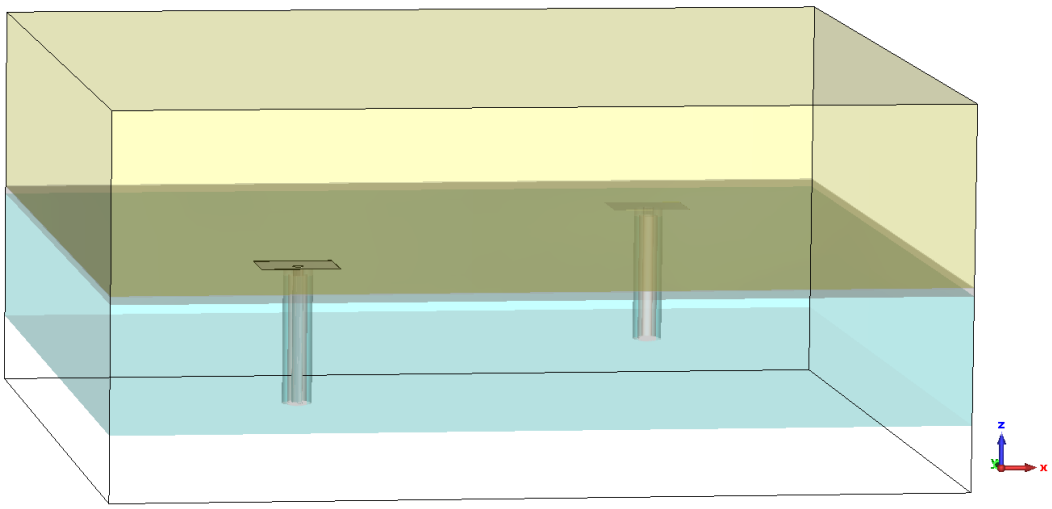


Figure 8: Schematic representation of flip-chip packaging layers modeled with two patch antennas

3.2 MATLAB

The channel model is obtained by computing the delay spread and path losses of the channel in MATLAB after the simulations have been completed, the S-parameters have been evaluated, and the antenna performance has been approved. To do so we exported text files from CST with the S-parameters data and output signals, which are going to be the input data for the scripts in MATLAB

3.2.1 Path losses

To calculate path losses we need the data from the S-parameters, when reading the text file we eliminate all the values that are not a number, NaN, then after preparing the matrices, the channel frequency response is obtained as:

$$G_i G_j |H_{ij}(f)|^2 = \frac{|S_{ji}(f)|^2}{(1 - |S_{ii}(f)|^2) \cdot (1 - |S_{jj}(f)|^2)}, \tag{7}$$

Where G_i and G_j are the gains of the transmitting and receiving antennas.

3.2.2 Delay spread

With the voltage of the transmitted signal received by the other antenna we input the data to an already existing script that calculates the delay spread with the formulas written below [40]:

$$\tau_{rms}^{(i,j)} = \sqrt{\frac{\int (\tau - \overline{\tau_{ij}})^2 P_{ij}(\tau)\, d\tau}{\int P_{ij}(\tau)\, d\tau}}, \tag{8}$$

Where $P_{ij}(\tau) = |h_{ij}(t,\tau)|^2$ is the Power-Delay Profile, or PDP, $h_{ij}(\tau)$ is the joint channel response, $\overline{\tau_{ij}}$ is the medium's mean delay and τ_{rms}^{ij} is the delay spread, D_s, between the transmitting port i and the receiving port j.

4 Experiments and results

In this chapter, the results of the full-wave EM simulations in CST, performed to satisfy the objectives from Section 1.1 as well as the requirements and specifications from Section 1.2, and their processed outputs are presented and commented.

4.1 Patch antenna design

This section takes us through the simulations and results of the design process of the antenna, following the methodology explained in Chapter 3 and the formulas presented in Section 3.1.1, in order to fulfill the required specifications for the antenna. For Figures 9–14 the boundary conditions have been set as free-space.

4.1.1 Patch antenna design and frequency scale up

The first figure presented in this chapter, Figure 9, represents the S_{11} parameters of three patch antennas designed for three different resonant frequencies, namely: 5, 100 and 250 GHz. Here, all the dimensions for each patch have been obtained using the formulas from Section 3.1.1, according to the desired central frequency.

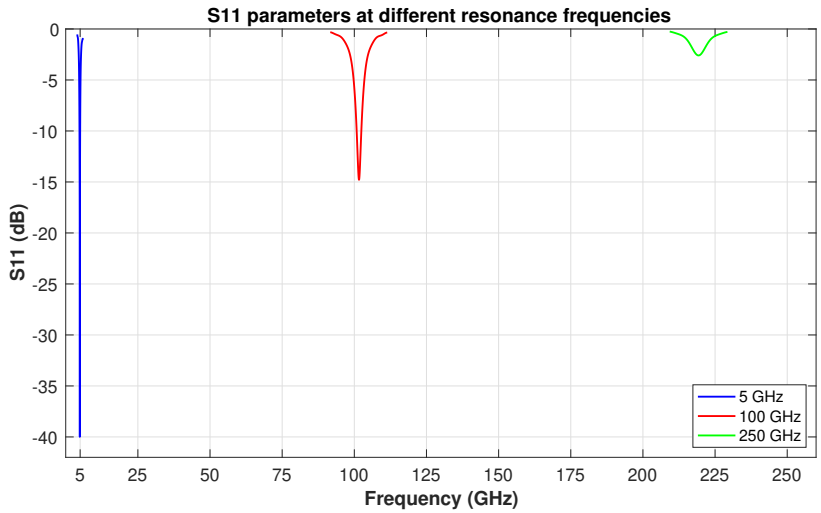


Figure 9: S_{11} parameters of patch antennas at different frequencies

The plots in Figure 9 show, as expected, that as frequency increases so do return losses. It can also be seen that the antenna designed to resonate at 250 GHz has moved down around 30 GHz which is not acceptable, as neither its S_{11} parameter values. Hence, we conclude that we cannot just rely on Balanis' formulations at high frequencies due to non-idealities of the materials and other aspects. In Section 4.1.2 changes are going to be made to deal with the results encountered.

4.1.2 Antenna optimization at the desired working frequency

In order to improve return losses at high frequencies, we made a change of substrate from FR4 to Polyamide, as mentioned in Section 3.1.1.

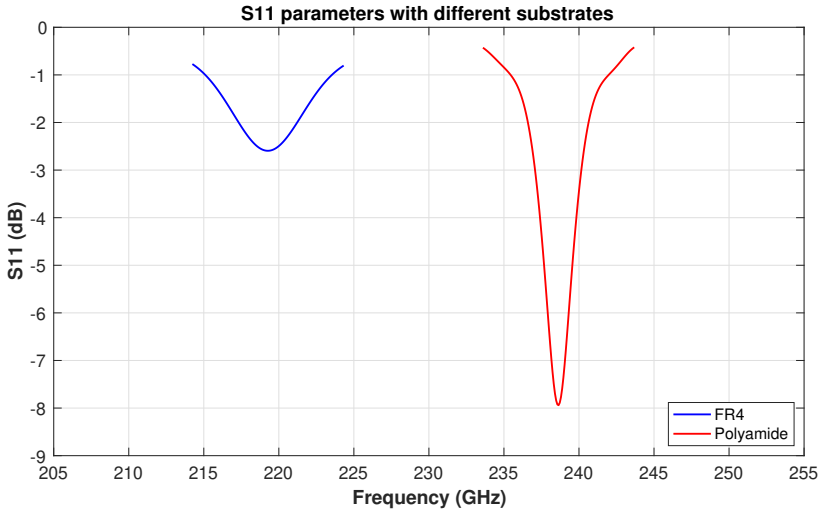


Figure 10: S_{11} parameters of patch antennas with different substrates

As can be seen, not only the S_{11} parameter improves by 5 dB, but also its central frequency displacement is now 12 GHz, instead of 30 GHz that we had with FR4 as substrate. Hence, we find that the displacement is now less than 5% of the targeted frequency of 250 GHz. Despite the improvement, the design still does not meet the requirements and specifications set at the outset of the thesis proposal.

To optimize the antenna performance, various parametric sweeps, including the radius of the inner, Figure 12, and external conductors of the coaxial feeder, the thickness of the external conductor of the coaxial, its length and thickness of the patch, Figure 13, have been made. As explained in Section 3.1.1 the metrics of the coaxial used here, prior to their optimization, had been calculated using a macro built in CST Microwave Studio.

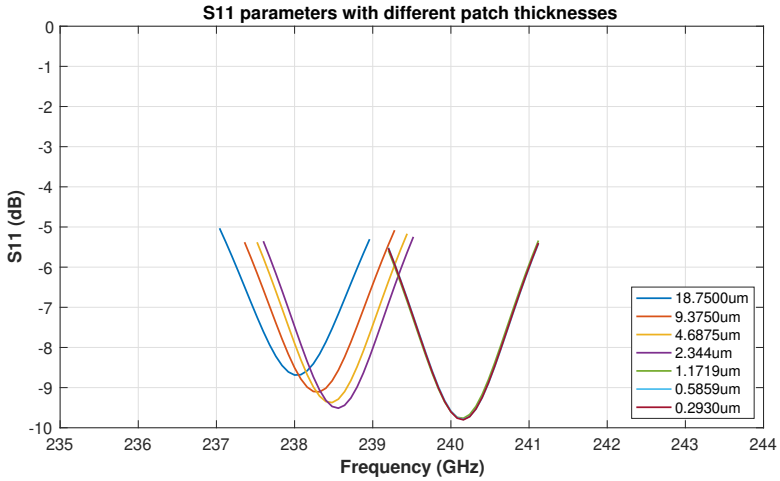


Figure 11: S_{11} for different patch thicknesses, external coaxial radius = $66.97\mu m$ and inner coaxial radius = $1.1719\mu m$

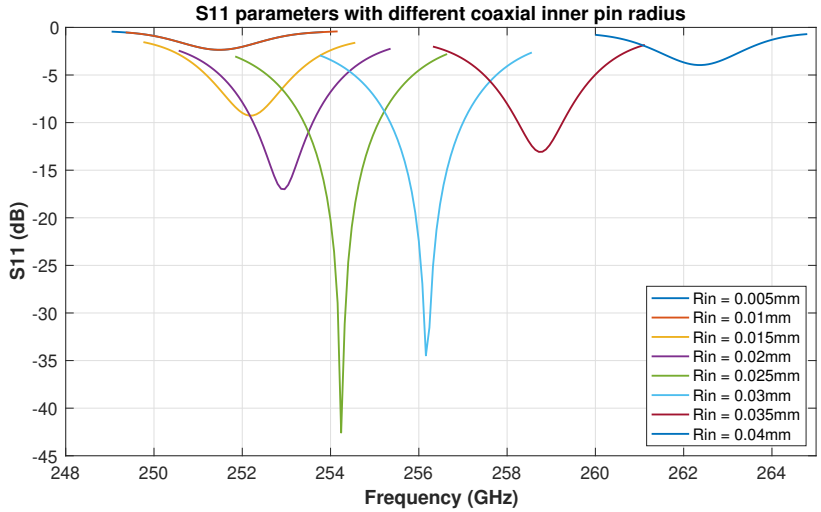


Figure 12: S_{11} for different coaxial inner conductor radius, coaxial external conductor radius = $45\mu m$ and patch thickness = $1.1719\mu m$

Figure 11 presents the S_{11} parameters as a function of frequency for different height values for the patch. The thicknesses used are the result of dividing the wave length by powers of two. As it can be seen, the three lower heights are overlapped, they have the same frequency at their minimum and the difference in terms of return losses between them is 0.04 dB, meaning that a limit for improvement has been reached here. Therefore, we have selected $h = 1.1719\mu m$ because its a good compromise between performance and fabrication complexity. It is also worth noticing that the difference in performance with the four heights represented on the left side, can be attributed to the fact that as h is smaller, $W/h \gg 1$ and hence ε_{eff} is more precise.

In Figure 12, which was made after the sweep to optimize the external conductor of the coaxial, it can be seen that having a larger space between the inner and external to prevent coupling effects increases the return losses and for tighter space between the two conductors, coupling displaces the resonance frequency and also affects the return losses. Here $R_{in} = 25\mu m$ is the best option

After performing a last sweep to find the optimal value of the thickness of the external coaxial conductor, which is $25\mu m$, a simulation with a the parameters chosen is shown in Figure 13.

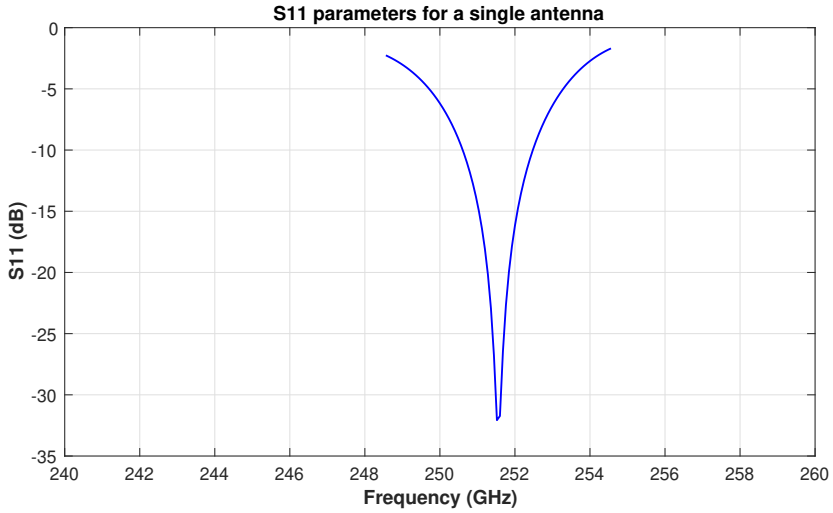


Figure 13: S_{11} parameters for the optimized antenna in free-space

The resulting design of the patch antenna has a bandwidth of approximately 2 GHz at -10 dB, while having 4.8 GHz at -3dB and a deviation from the design frequency of 0.608%. After validating the results with our requirements and specifications, we then proceed to add a second antenna to the scenario in Section 4.1.3.

4.1.3 Addition of a second antenna in the environment

Once the performance metrics of the antenna are satisfactory, we continue to place a second antenna in the scenario. Now the dimensions of the ground plane are 4×4 mm^2 to be able to place the antennas at a distance of $d = 2.83mm$ between patch centers.

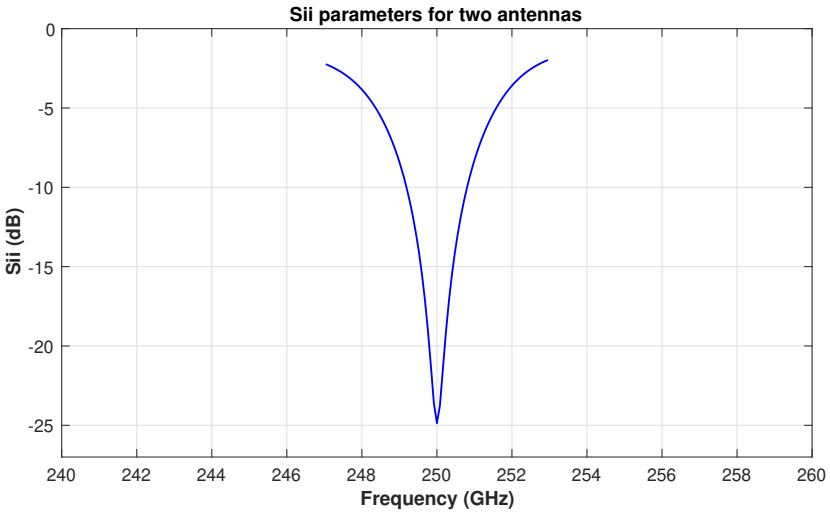


Figure 14: S_{ii} for both antennas

When placing two antennas in the environment, we can see that, due to the distance being so small, mutual coupling and impedance affect the antennas. As a result, the resonance frequency moves down with respect to the case with only one antenna, and now the resonance frequency coincides with the design frequency of the patch. We can also see an increase on S_{ii} of $7.5dB$ with respect to Figure 13. However, this has helped us having a perfectly adapted antenna a the design frequency, 250 GHz.

4.2 Addition of chip package layers

Once the design of the antenna has fulfilled our requirements and specifications, as mentioned in Section 1.2, and has proved to work in an scenario with two antennas, it is time to start adding layers of a realistic flip-chip package, bulk silicon in Section 4.2.1 and AlN in Section 4.2.2.

4.2.1 Addition of Bulk Si with two antennas

Using the same scenario as in Section 4.1.3. The first layer added is bulk silicon. This material will be located underneath the ground plane wrapping around the coaxial feeders of both antennas, similar to Figure 8 but without the AlN.

If the coaxial is well insulated, the losses caused by the bulk silicon should be low and the simulation plotted in Figure 15 should be similar to the scenario without this layer, Figure 14. We note that, here, we still have not coated the package with metallic boundaries, which is performed in Section 4.2.2.

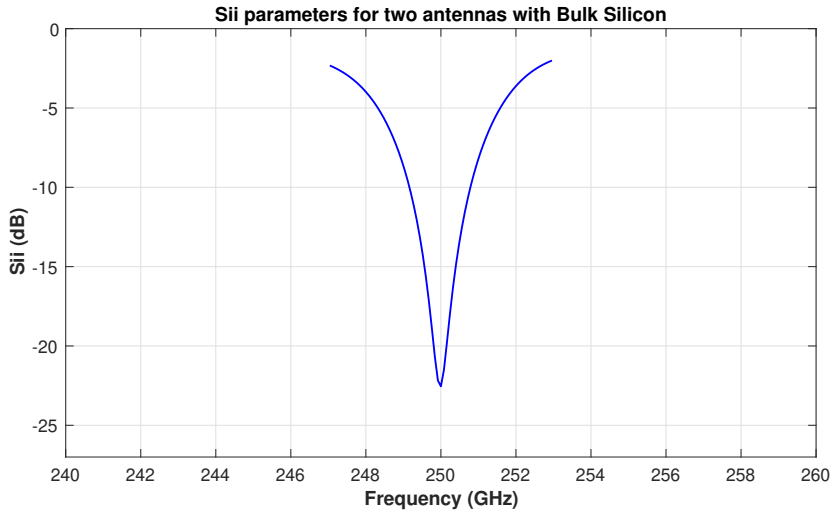


Figure 15: S_{ii} parameters of two antennas with Bulk Si wrap around the coaxial feeder

As expected, in Figure 15 resonance frequency and bandwidth remains the same, however increased the S_{11} parameters by approximately 3 dB with respect to Figure 14. Despite that, the S_{11} parameters are still well below the requirements defined in Section 1.2. The next step to be able to characterize the WNoC channel in a flip-chip is to add a layer of heat spreader (including metallic walls and ceiling) on top of the antennas.

4.2.2 Addition of AlN and metallic boundaries with two antennas

In the following, the environment modeled to perform the simulations is as in Figure 8, AlN heights and distances between antennas may vary. The boundary conditions used for chip simulations, as mentioned in Section 3.1.2, simulate PEC where all the tangential electrical fields are 0.

Different thicknesses of AlN with two antennas. Here, simulations with different thicknesses of AlN are performed to later study the effect of the heat spreader on the micro-reverberant channel. The placement of the antennas and ground plane dimensions are the same as described in Sections 4.1.3 and 4.2.1

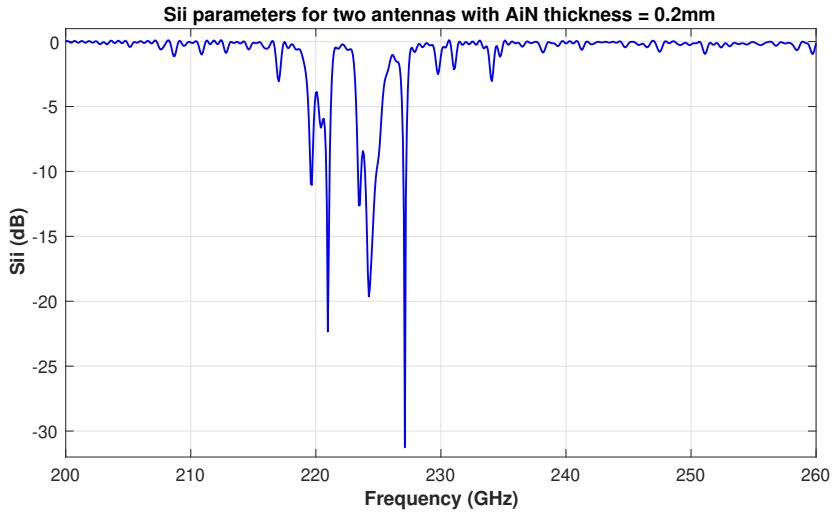


Figure 16: S_{ii} parameters of two antennas with AlN $= 0.2mm$

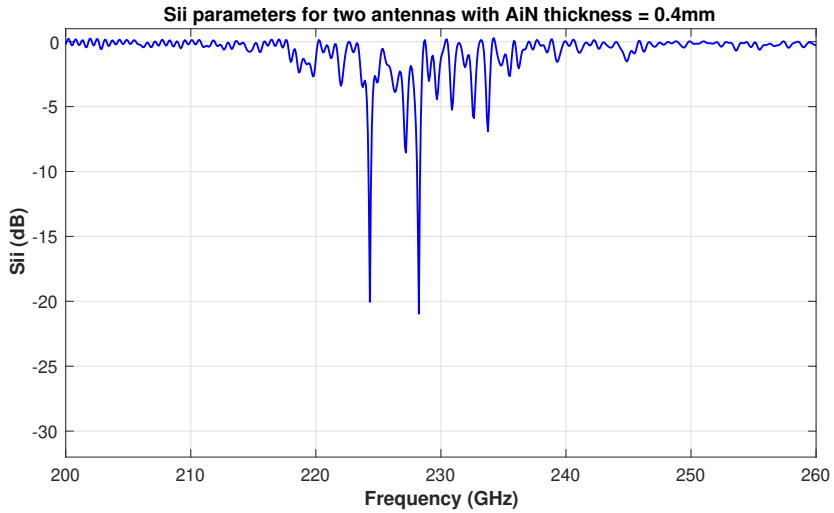


Figure 17: S_{ii} parameters of two antennas with AlN $= 0.4mm$

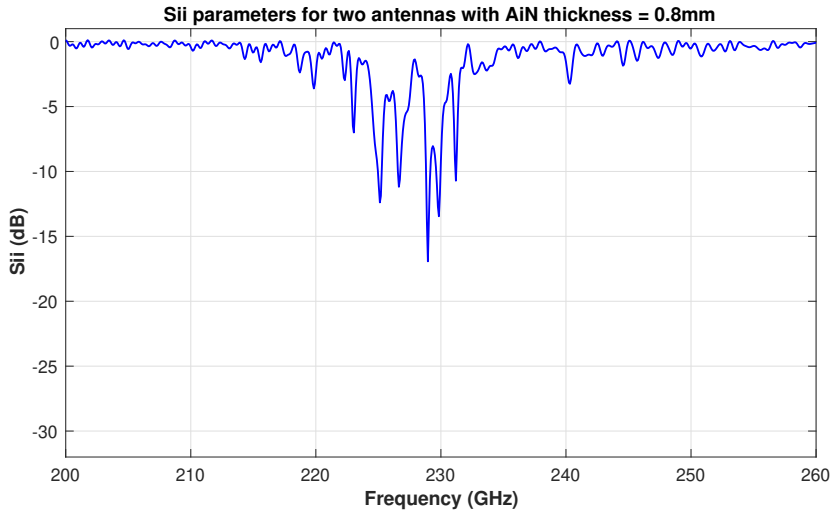


Figure 18: S_{ii} parameters of two antennas with AlN $= 0.8mm$

Simulations outputs in Figures 16, 17 and 18, prove that in a micro-reveberating media where the encasement of the chip reflects everything, and only the AlN introduces losses to the channel, the mutual coupling of the antenna changes an this affects directly on the S_{11} parameters, displacing the resonance frequency and introducing quick amplitude fluctuations throughout the spectrum.This lead to difficulties on identifying the resonance frequency and poor radiation performance.

Different distances between two antennas with AlN. Next, simulations with different distances between antennas are performed to later study its effect on the micro-reverberant channel. The environment modeled for the simulations consists on chip of 15 $\times$ 15 mm^2 with a 0.2-mm thick layer of AlN with variable distance between antennas.

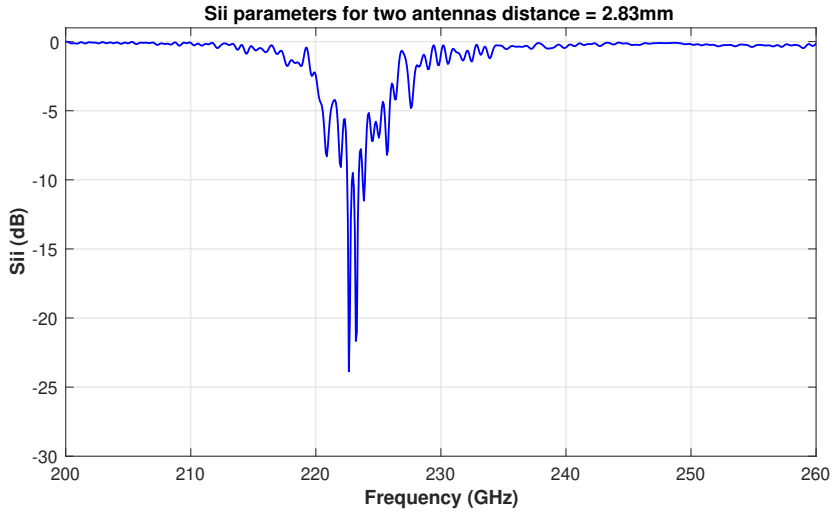


Figure 19: S_{ii} parameters of two antennas with distance $= 2.83mm$

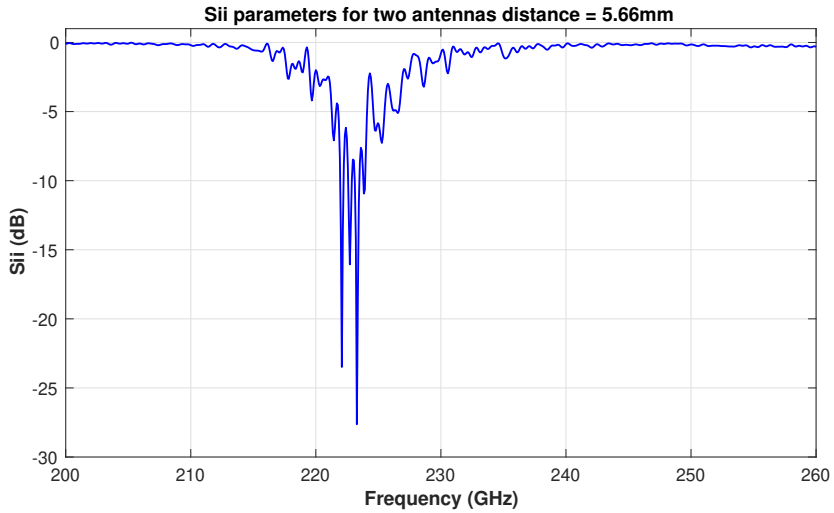


Figure 20: S_{ii} parameters of two antennas with distance = $5.66mm$

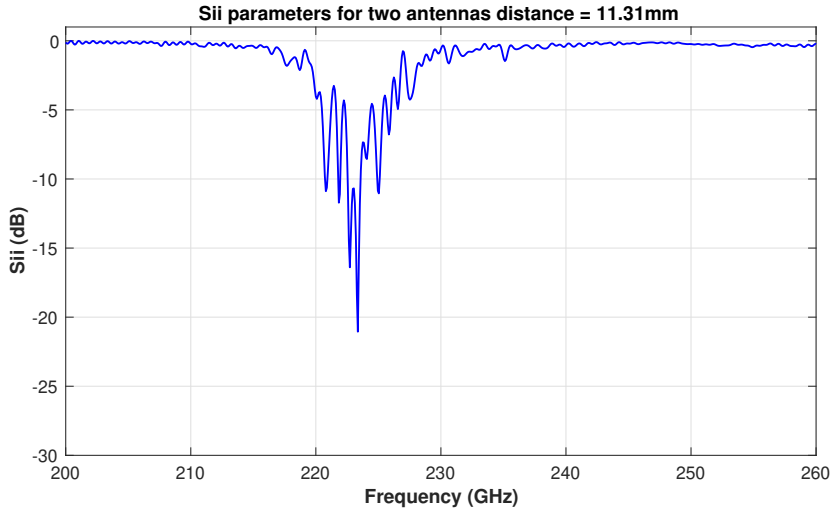


Figure 21: S_{ii} parameters of two antennas with distance = $11.31mm$

The first sight of Figures 19, 20 and 21 is that the S_{11} parameters shape can be better perceived than in Figure 16 and the resonance frequency is distinguished. Such improvement over the comparable case of Figure 16 is due to the enlargement of the model, which therefore places the reflecting walls of the chip further away. However, having a bigger micro-reverberation chamber also has its drawbacks in path losses, as will be explained in Section 4.3.1.

4.3 Channel modeling

In this section, the study of the channel is undertaken by obtaining the path losses in Section 4.3.1 and delay spread in Section 4.3.2 from the outputs obtained in the simulations

in Section 4.2.2.

4.3.1 Path losses

The path losses obtained in this section have been calculated when the antenna is better matched leading to a value of S_{ji} that is maximum. Figures 22, 23 and 24 present the S_{ji} for the three different AlN thickness values, all the antennas are at a distance of d = 2.83mm with a chip package of 4×4 mm^2

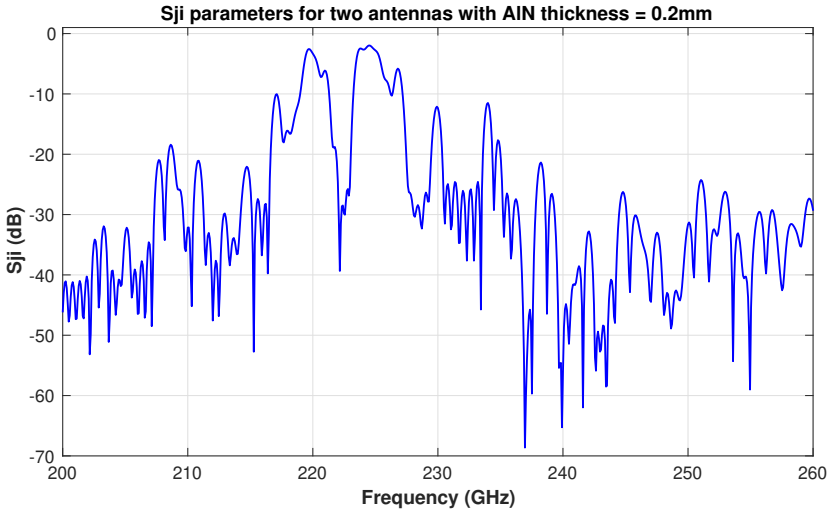


Figure 22: S_{ji} parameters of two antennas with AlN $= 0.2mm$

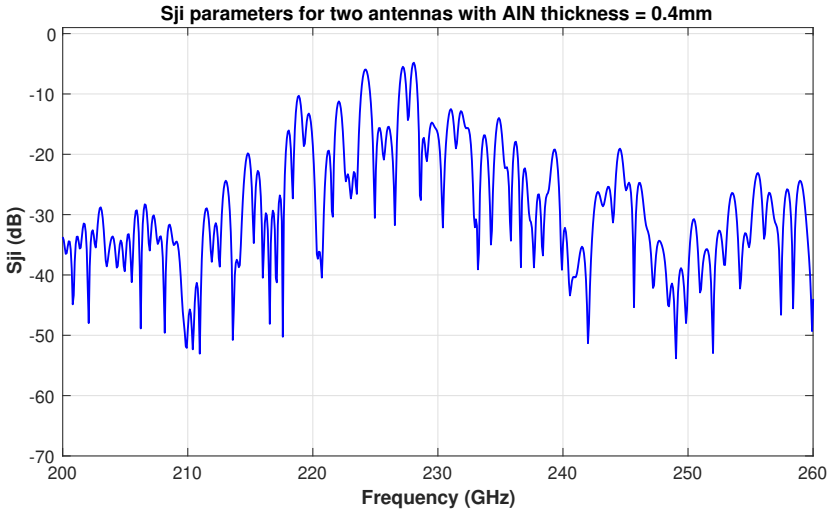


Figure 23: S_{ji} parameters of two antennas with AlN $= 0.4mm$

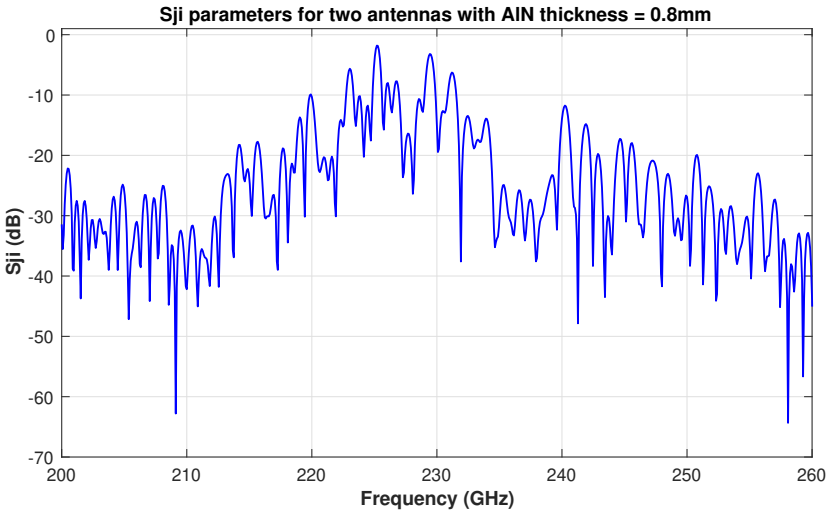


Figure 24: S_{ji} parameters of two antennas with AlN $= 0.8mm$

In the plots from Figures 22, 23 and 24 it can be seen that when the antenna resonates, the S_{ji} maximum does not go below -5 dB. The effect of the reverberant channel is reflected on the fact that S_{ji} parameters values oscillate rapidly throughout the spectrum.

Figure 25 presents the path losses calculated with the S_{ji} parameters in the points where the antenna is matched, for the three different AlN thicknesses from Figures 22, 23 and 24. As explained and seen in the reflections of Figures 16, 17 and 18, we observe in Figure 25 that we can achieve very low losses in conditions where the antenna is matched because of the reverberant environment and the low losses of the materials present in the medium. The thickness of the AlN plays a role, since the change in reflection distances does imply a variation in the shape of the antenna return losses and, as observed, could influence the S-parameter spectrum. In all cases, however, we also infer that the bandwidth achievable will be also relatively low from the notchy spectrum figures.

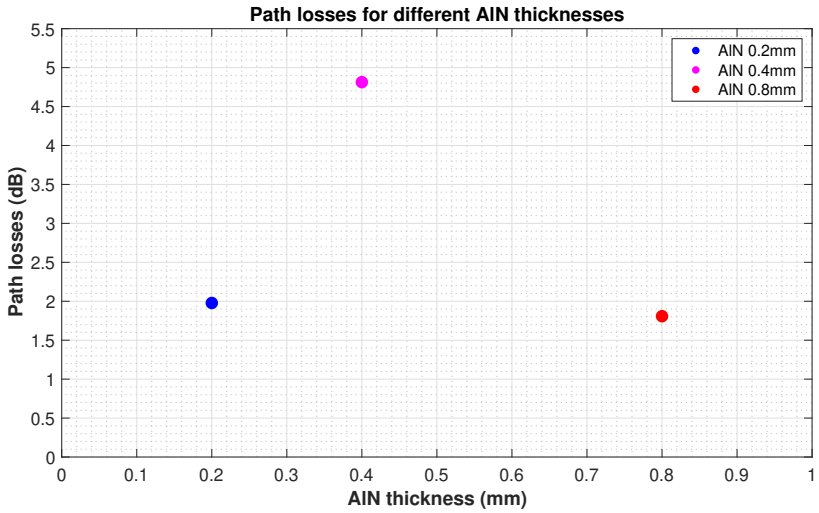


Figure 25: Path losses for different thicknesses of AlN

Figures 26, 27 and 28 present the S_{ji} for three different antenna positions leading to different distances between antennas with an AlN thickness of 0.2mm and a chip package of 15×15 mm^2.

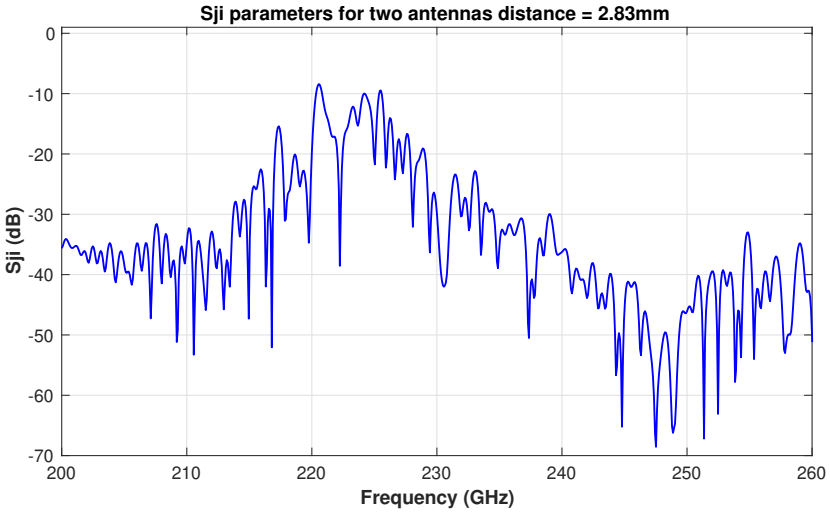


Figure 26: S_{ji} parameters of two antennas with distance $= 2.83mm$

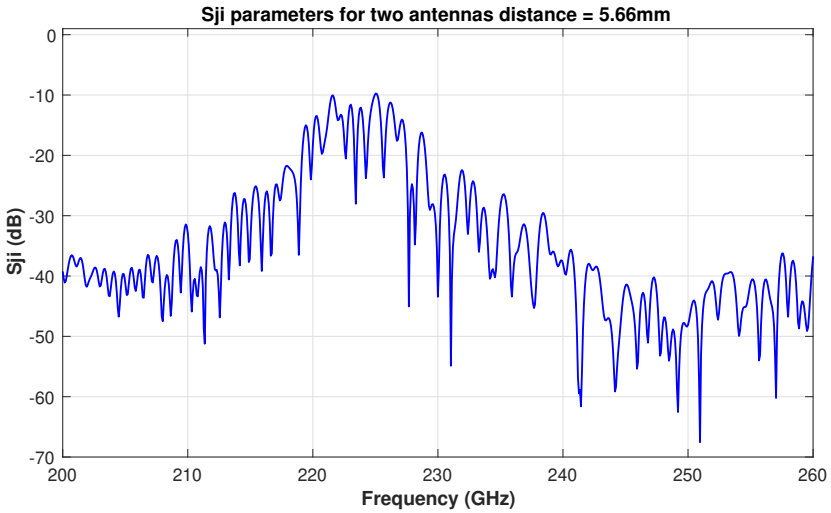


Figure 27: S_{ji} parameters of two antennas with distance $= 5.66mm$

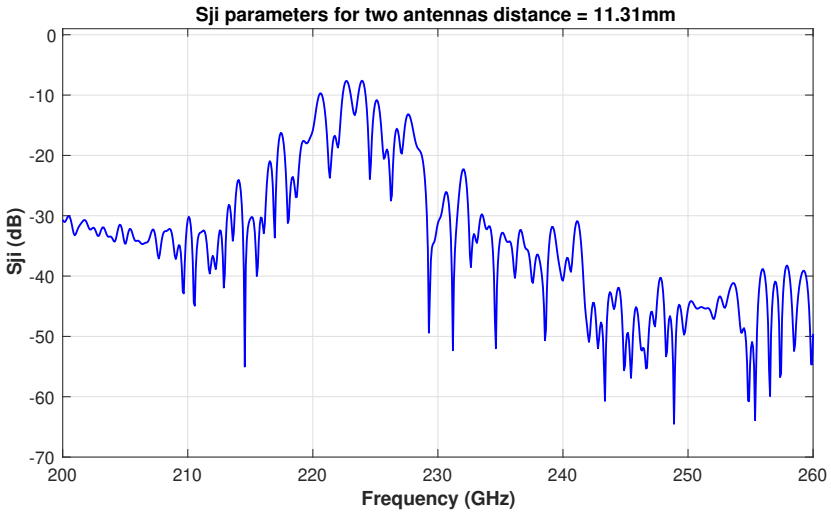


Figure 28: S_{ji} parameters of two antennas with distance $= 11.31mm$

In the plots from Figures 26, 27 and 28 it can be intuited clearer than in Figures 22, 23 and 24 but with a worse maximum S_{ji} which can be attributed to having a much larger scenario than in the simulations where we varied the AlN thickness. However, the effect of the reverberant channel can still be clearly seen in the S_{ji} parameters values oscillate rapidly throughout the spectrum.

Figure 29 presents the path losses calculated with Equation (7) using the values of S_{ji} parameters when the antenna is matched, for the three different inter-antenna distances from Figures 26 27 and 28.

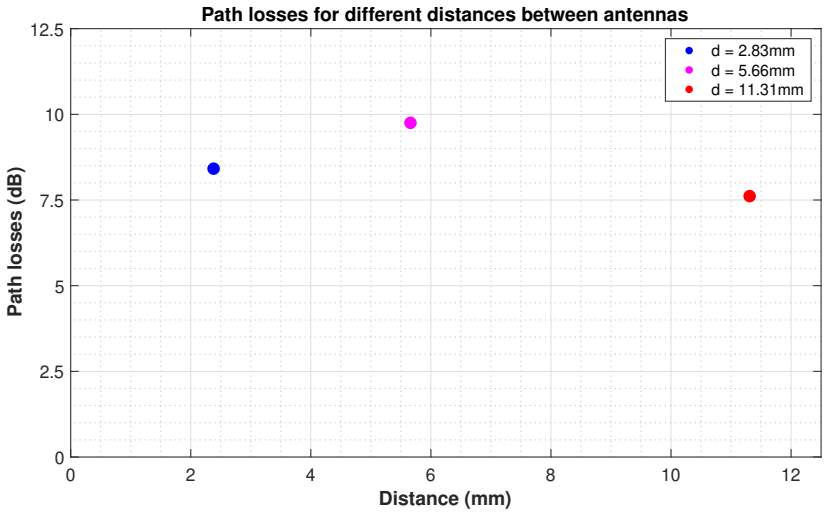


Figure 29: Path losses for different distances between antennas

In Figure 29, it is noticeable that for the same conditions in Figure 16 and 19, meaning distance between antennas equal to 2.83mm and AlN thickness of 0.2mm, having a bigger chip environment increases path losses around 6.5 dB. Figure 29 also displays that as further apart the antennas are placed lower the slope of its path losses, which can be attributed to the fact that mutual coupling is reduced when increasing distance between antennas and thus improving return losses and radiation. In free-space environments one would expect a path loss that scales with distance, yet in this completely enclosed environment, the results suggest that the energy is distributed around the entire cavity and hence the path loss does not necessarily follow a linear dependence with distance. While its true that mutual coupling reduces as distance between antennas increases, as can be seen in Figures 19, 20 and 21, constructive and destructive reflections in the micro-reverberant chamber varies when the antennas are moved, making it hard to predict what is going to happen exactly.

4.3.2 Delay spread

In this section, the delay spread results from the simulations in Section 4.2.2 are obtained by post-processing in MATLAB, as detailed in Section 3.2.2.

Figure 30 presents the delay spread of the simulations from Figures 16, 17 and 18, showing its value as a function of AlN thicknesses. It can be seen that such high values of delay spread are due to the reflections happening inside the micro-reverberant chamber. We note, however, that computational constraints have limited the temporal length of our simulations and, hence, time responses may be longer than shown here. Hence, delay spread (coherence bandwidth) values could be higher (lower) than the ones shown here. Performing the inverse of the worst Ds measures, and noting the aforementioned, we obtain that the coherence bandwidth for AlN thicknesses equal to 0.2mm is $B_{coh} < 6.76$ GHz and 0.4mm $B_{coh} < 4.76$ GHz and for an AlN thickness of to 0.8mm $B_{coh} < 4.55$ GHz.

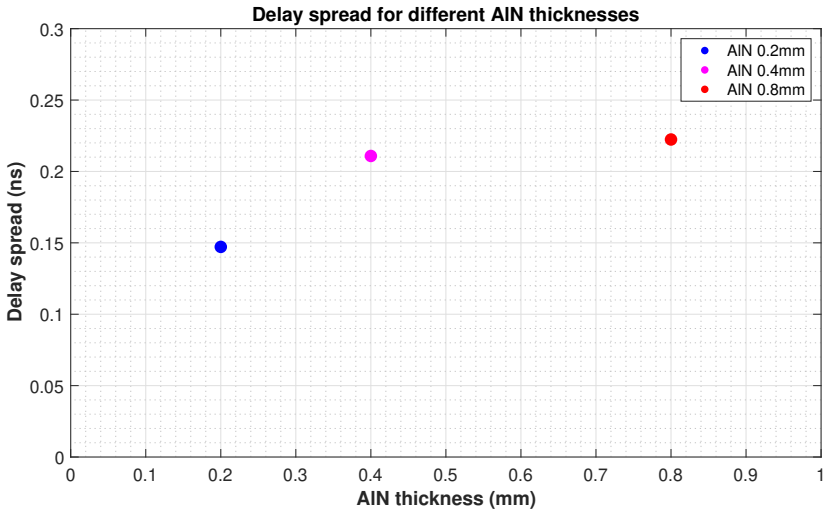


Figure 30: Delay spread over distance with different thicknesses of AlN.

Finally, Figure 31 presents the delay spread of the simulations from Figures 19, 20 and 21, showing its value as a function of distance between antennas. The plots in Figure 30 show that as the antennas are placed further apart from one another, mutual coupling decreases, and so seems to be the case for the delay spread as well. Performing the inverse of the delay spread values and considering the computational limitations of the simulations, we obtain that for a distance of 2.38 mm, $B_{coh} < 3.03$ GHz, $B_{coh} < 4.83$ GHz for d = 5.66mm and for a separation between antennas of 11.31mm $B_{coh} < 6.49$ GHz.

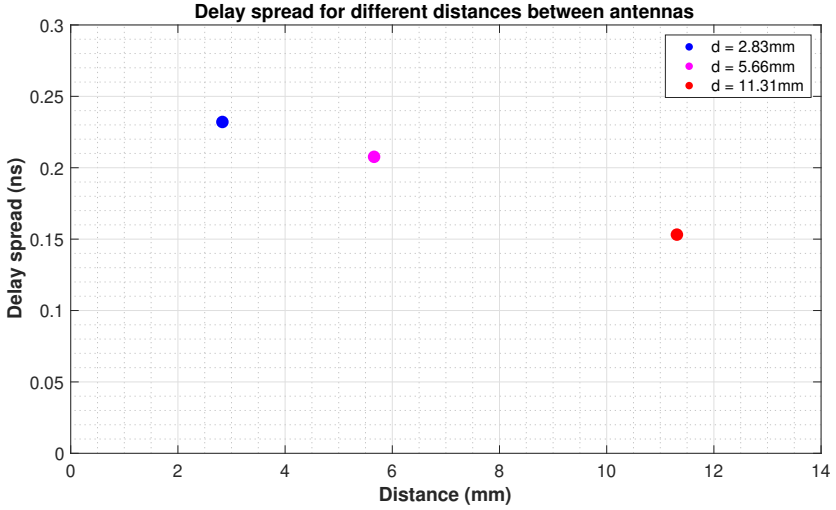


Figure 31: Delay spread over distance with different distances between antennas.

5 Conclusions

In this thesis, we have presented the design of a patch antenna compatible with on-chip integration for on-chip wireless communication purposes, and used such an antenna to study a low-loss reberverating channel created between the silicon substrate of the chip and the heat sink. Throughout the development of this thesis, the focus has been to design the antenna and study the channel following the requirements and specifications detailed in Chapter 1. After evaluating the results from the different simulations exposed in Chapter 4, we can conclude that the proposed planar antenna at 250 GHz has fulfilled its requirements and specifications in terms of return losses and bandwidth, hence being capable of providing the outputs necessary to study the WNoC channel of the micro-reverberation chamber where it is positioned. We demonstrate that a wireless link around 220–230 GHz can be created with patch antennas, achieving a path loss in the range of 2–10 dB and delay spreads in the sub-nanosecond range, although the time-domain results are limited in our case to computational constraints of the simulations.

Due to homogeneity of the ground plane and the substrate layers where the antennas are placed and the AlN where propagation occurs, there is no differentiation between the intra-chip and inter-chip regions. Therefore, the results obtained are applicable to both single-chip and multi-chip scenarios with interposers.

We emphasize the significance of package dimensions and optimization to assure the viability of the WNoC approach, as this has an effect on the decrease of path losses as well as on the return losses of the antennas. We also highlight the importance of the distance between antennas, since when placed in the micro-reverberation chamber mutual coupling increases, and has direct effect on increasing both delay spread and return losses.

6 Future Work

To continue with the study on planar antenna design and channel modeling started, the following is proposed:

- Extending the simulation campaign with bigger packages, more complete sweeps for distances between antennas, and longer simulations in time domain, as they would help to better characterize the deterministic channel especially in the time domain.
- Planar antenna arrays within the computing package for spatial multiplexing, as carried out with quarter-wave monopoles in [41] by fellow N3Cat resercher, F.Rodríguez-Galán.
- Replacing the ideal coaxial feeder with an alternative and manufacturing-friendly feeding design using a set of TSVs surrounding a core conductor as a way to emulate its behaviour.

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