



TECHNICAL UNIVERSITY OF MUNICH

CHAIR OF CIRCUIT DESIGN

MASTER THESIS

# **A 12-bit SAR ADC for a flexible tactile sensor**

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I hereby confirm that I have written the accompanying thesis by myself, without contributions from any sources other than those cited in the text and acknowledgements.  
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## Abstract

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADC) are some of the most efficient ADC topologies available, allowing excellent performance values at low power consumption across a wide range of sampling frequencies. The proposed ADC is aimed at a tactile sensor application, requiring a low-noise and low-power solution. In addition, it should have high SNDR to detect even the weakest signals with precision. This thesis presents a 12-bit 400 kS/s SAR ADC implemented in a 180 nm CMOS technology for such a task.

The designed SAR ADC uses a hybrid R-C DAC topology consisting of a charge-scaling MSB DAC and a voltage-scaling LSB DAC, allowing a good trade-off between power consumption, layout area and performance while keeping the total DAC capacitance under reasonable values. Bootstrapped switches have been implemented to preserve high-linearity during the sampling period. A double-tail dynamic comparator has been designed to obtain a low-noise measurement while ensuring suitable delay values. Finally, regarding the logic, an asynchronous implementation and the conventional switching algorithm provide a simple but effective solution to supply the digital signals of the design.

Pre-layout noise simulations with input frequencies around 200 kHz show SNDR values of 72.07 dB, corresponding to an ENOB of 11.67 bits. The total power consumption is 365  $\mu$ W while the Walden and Schreier figure-of-merit (FoM) correspond to values of 275 fJ/conversion and 160 dB, respectively.

**Keywords:** Flexible tactile sensor, Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), R-C Digital-to-Analog Converter (DAC), Low-noise ADC.

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# Acronyms

<b>ADC</b>	Analog-to-Digital Converter
<b>SAR</b>	Successive Approximation Register
<b>DAC</b>	Digital-to-Analog Converter
<b>CMOS</b>	Complementary Metal–Oxide-Semiconductor
<b>IC</b>	Integrated Circuit
<b>MSB</b>	Most Significant Bit
<b>LSB</b>	Less Significant Bit
<b>DNL</b>	Differential Non-Linearity
<b>INL</b>	Integral Non-Linearity
<b>FFT</b>	Fast Fourier Transform
<b>SNR</b>	Signal-to-Noise Ratio
<b>SFDR</b>	Spurious-Free Dynamic Range
<b>THD</b>	Total Harmonic Distortion
<b>SNDR</b>	Signal-to-Noise and Distortion Ratio
<b>ENOB</b>	Effective Number Of Bits
<b>PCM</b>	Pulse Code Modulation
<b>I2C</b>	Inter-Integrated Circuit
<b>Fm</b>	Fast Mode
<b>NMOS</b>	N-channel Metal-Oxide-Semiconductor
<b>PMOS</b>	P-channel Metal-Oxide-Semiconductor
<b>CBW</b>	Conventional Binary-Weighted array

<b>BWA</b>	Binary-Weighted Array with attenuation capacitor
<b>MIM</b>	Metal-Insulator-Metal
<b>GBW</b>	Gain-Bandwidth
<b>CDF</b>	Cumulative Distribution Function
<b>DDL</b>	Dynamic Differential Latch
<b>EoC</b>	End-of-Conversion
<b>DR</b>	Dynamic-Range
<b>ERB</b>	Effective Resolution Bandwidth
<b>FoM</b>	Figure-of-Merit

# Chapter 1

## Introduction

An Analog-to-Digital Converter (ADC) is a mixed-signal electronic circuit that converts an electrical signal from the analog to the digital domain [1]. Nevertheless, ADC are some of the most essential blocks in chip design, enabling a computer or microprocessor to form a representation of a physical world property, acting as a bridge.

Contrary to what it may seem, ADC are nothing new. The first electronic converter dates back to 1937. Until the 1950s, the existent data converters were developed for specialized applications using vacuum tube technology, making them bulky, expensive, and power-hungry, leading to no commercial use [2].

As it is introduced in [3], where an in-depth study on the history of ADC and Digital-to-Analog Converter (DAC) is conducted, during the 1960s, ADC experienced a change, and as electronic circuits shifted from vacuum tubes to transistors, new possibilities opened in design. Many of the new ADC were destined for voltmeter applications, with converters of 8-bit, 1 MS/s, as early as 1960. It should also be noted that most of the first converters used a Successive Approximation Register (SAR) topology, still relevant today. In the 1970s, the ADC and DAC market was driven by applications such as voltmeters, process control, or digital video. At the beginning of the decade, most converters used bipolar technology. However, by 1974, the first Complementary Metal–Oxide–Semiconductor (CMOS) DAC was introduced, solving most of the issues bipolar converters had. The decade of the 1980s supposed growth in the ADC industry for the Integrated Circuit (IC), hybrid, and modular converters. During this period, the emphasis of the ADC began to include dynamic performance metrics such as the Signal-to-Noise Ratio (SNR) or the Effective Number Of Bits (ENOB). Moreover, in the mentioned period, the growth of the digital video market made the companies start to develop converters with medium resolutions but high sampling frequencies, with the rise of the flash topology. In the 1990s, the demand increased even more, and trends such as single-supply voltages and low-power devices started to appear. During this time, the pipeline architecture virtually replaced the flash for most high-frequency ap-

plications. Simultaneously, the sigma-delta converter gained popularity as it became the topology of choice for audio applications, having practically unmatched resolutions.

In the last two decades, the need for ADC has increased, mainly thanks to decreasing transistor dimensions and supply voltages from which digital circuits have greatly benefited but made it harder to apply conventional analog design techniques [4]. So is the case that the flexibility and capability of developing complex functions intrinsic to the digital design blocks have made designers move as many functionalities as possible to the digital domain. However, some tasks such as amplification, are exclusive to analog circuitry, increasing the need for converter blocks.

## 1.1 Motivation

In this thesis' case, the ADC shall work for a touch sensing application, with possible implementations such as artificial skin. The general concept consists of a sensing system based on silicon, which is piezoresistive. Thus, depending on the pressure applied, the silicon will bend a certain amount, creating different resistance values, which can then be translated to an electrical magnitude such as voltage. Suppose this principle is applied to an array of sensors; then, depending on the pressure read by the different sensors of the array, the point of application could be backtracked. After the sensing, amplifying the signal received is required; in this application, the magnitudes can vary from 100 nV to a few  $\mu\text{V}$ . Thus, an amplification stage shall convert the small signals from the strain sensor array to a magnitude readable for the ADC input. At this point, the analog-to-digital conversion must be performed, in which the voltage signal obtained after the amplification stage is converted into the digital domain. Then, the bit conversion obtained by the ADC is carried to the general microcontroller of the application via a communication bus. For this design, a serial bus is the optimum choice to minimize area and power consumption.

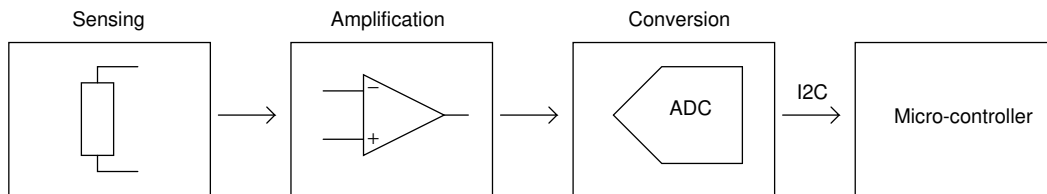


Figure 1.1: Simplified block diagram of the application.

Application-wise, there are multiple constraints, as not only does the speed of the overall system have to be considered. Noise must be small to assess the magnitude precisely, as it is essential to detect the signals as cleanly as possible to obtain a good estimation. Furthermore, power consumption is a restriction for the whole system, as



overall, there have already been compromises. Equally, the ADC will have to be minimal in both area and power consumption while prioritizing the overall performance.

Regarding ADC, there are many and multiple topologies, as introduced in Figure 1.2. Certainly, the decision on which to choose is very application dependant and is one of the most critical choices in the design process.

For example, in applications such as process control or precision temperature measurements, the sigma-delta topology tends to be favored due to their unmatched resolutions. On the other side of the spectrum, one can find oscilloscopes where high sampling rates and medium resolutions are required, making the pipeline topology the ideal candidate.

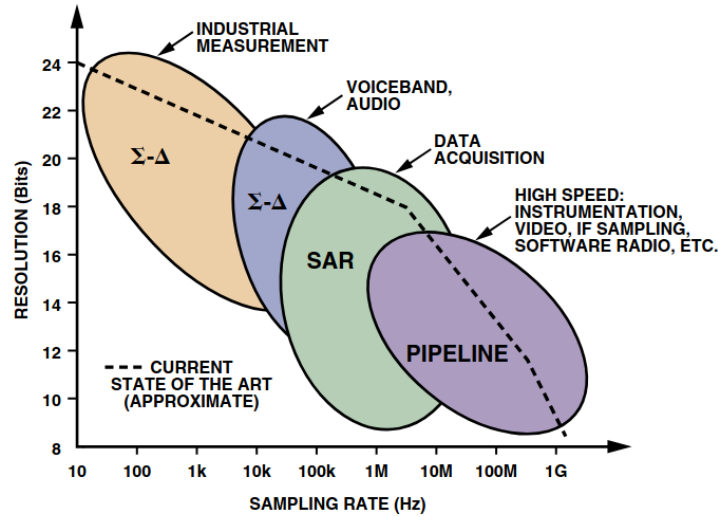


Figure 1.2: ADC topologies sorted based on sampling rate and resolution [5].

The organization of this thesis is the following:

- Chapter 2: Fundamentals of Analog-to-Digital conversion and topology selection.
- Chapter 3: Digital-to-Analog Converter.
- Chapter 4: Sample and hold.
- Chapter 5: Comparator.
- Chapter 6: ADC logic.
- Chapter 7: Verification and performance of the design.
- Chapter 8: Conclusions.

# Chapter 2

## Fundamentals of Analog-to-Digital Conversion

### 2.1 Characterization

An ADC shall produce a successful conversion after three steps: sampling, quantization, and encoding, as shown in Figure 2.1. First, samples are taken from the analog signal and held during the time required to generate the digital output. Then, the output linearly related to the input must be generated, known as quantization or the A/D conversion. Finally, the last step is encoding, which in some cases may be required to encode the output ‘1’ and ‘0’ into binary coding. Nevertheless, this process is embedded in the ADC itself for some topologies.

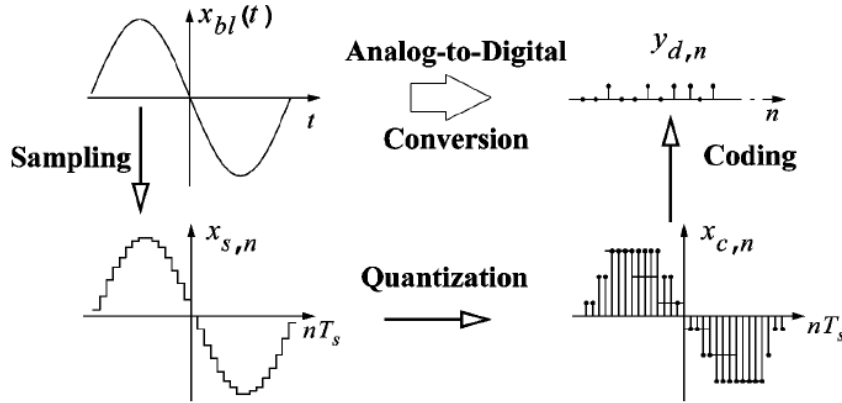


Figure 2.1: Process of converting a signal from the analog to the digital domain [6].

When designing an ADC, several non-idealities such as mismatch or noise can degrade the performance. Thus, it can be adequate to know how to assess the performance and what metrics exist to observe and quantify these non-idealities as a whole. These can be classified into two main types, static and frequency domain metrics.

### Static metrics

In the case of static metrics, it is crucial to understand the input-output transfer function of the system (Figure 2.2), as static errors can be quantified and obtained from it. In the ADC, the input is continuous. A step in the curve is defined as the difference between two analog voltages that produce two consecutive output code translations.

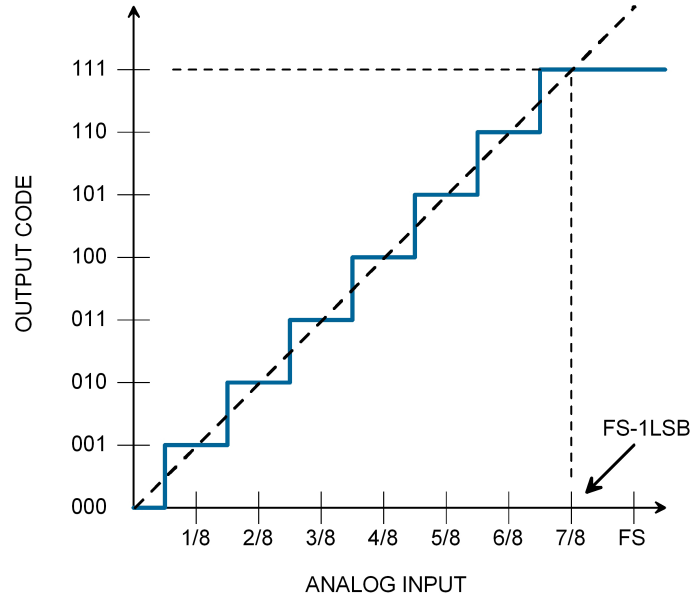


Figure 2.2: Ideal transfer function of an ADC [7].

The first error that comes up looking at the transfer function of the ADC is the offset error, which is the difference between the values that produce the first output transition. The offset point is referred to the analog input and measures a horizontal shift in the transfer curve. The ideal offset point is measured in Less Significant Bit (LSB) units and is located at  $1/2$  LSB. On the other side of the x-axis, the gain error can be found, which is the difference in the voltage that produces the last output translation, measured once the offset error has been removed. It can be interpreted as measuring the slope of the input-output transfer function and is located after the last transition  $+1/2$  LSB. Building a converter with good performance in both offset and gain errors is not trivial. Thus, it is a common practice to allow these errors to be larger than 1 LSB and remove them via calibration in post-processing [8].

While it is important to consider both offset and gain errors, as they can be removed via calibration do not affect the intrinsic performance of the converter. Thus, it is crucial to quantify the errors that hinder the performance and can not be calibrated, such as the Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL). The DNL is the difference between the actual and ideal steps (i.e., 1 LSB). Note that if the obtained step width is 1 LSB, then the correspondent DNL value is zero. The

INL is defined as the difference between the ideal and actual input values producing a code transition, which can also be interpreted as the accumulation of DNL errors, a graphical representation of both is introduced in Figure 2.3.

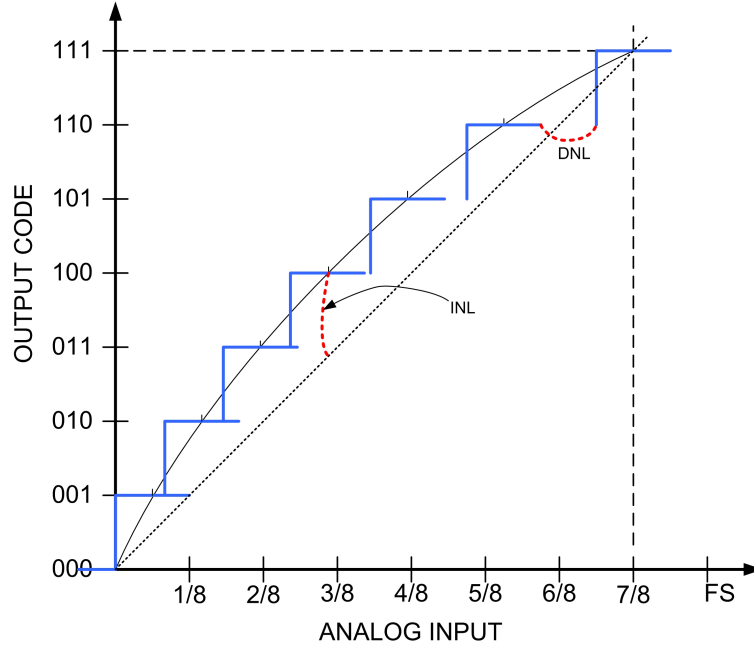


Figure 2.3: Graphical representation of the DNL and INL of an ADC [7].

To obtain the DNL and INL of a converter, one must perform a sweep in input values from zero to full-scale voltage ( $V_{FS}$ ) while observing the output code transitions. DNL and INL errors are usually identified by their maximum and minimum values.

### Frequency domain metrics

In applications with a low sampling frequency, static metrics are enough to assess the performance of the ADC. However, frequency domain metrics need to be quantified in most other cases [9]. With the aid of simulation, this can be done by using an ideal DAC and converting the ADC output back to the analog domain to obtain the spectrum representation of the output through the Fast Fourier Transform (FFT).

From the frequency domain analysis, one of the most important metrics is the SNR, which is the ratio of the power of the fundamental and the total noise power integrated over a specific frequency band, as in Equation 2.1.1.

$$SNR [dB] = 10 \log \left( \frac{\text{Signal power}}{\text{Total Noise floor Power}} \right) \quad (2.1.1)$$

A second metric that can be considered is the Spurious-Free Dynamic Range (SFDR), which is the ratio of the power of the fundamental harmonic with the power of the largest spurious within a certain frequency band, as in Equation 2.1.2.

$$SFDR [dB] = 10\log\left(\frac{\text{Signal power}}{\text{Largest Spurious Power}}\right) \quad (2.1.2)$$

The Total Harmonic Distortion (THD) is the ratio of the total harmonic distortion power in a specific frequency band and the power of the fundamental, as in Equation 2.1.3.

$$THD [dB] = 10\log\left(\frac{\text{Total Harmonics Power}}{\text{Signal Power}}\right) \quad (2.1.3)$$

In converters, it is important to define the Signal-to-Noise and Distortion Ratio (SNDR) as it determines the Effective Number Of Bits (ENOB). The SNDR is defined as the ratio of the power of the fundamental and the total noise and distortion power integrated over a certain frequency band, as in Equation 2.1.4.

$$SNDR [dB] = 10\log\left(\frac{\text{Signal power}}{\text{Total Noise floor Power} + \text{Distortion Power}}\right) \quad (2.1.4)$$

Finally, the ENOB is the measurement based on the SNDR with a full-scale sinusoidal input, as in Equation 2.1.5.

$$ENOB [bit] = \frac{SNDR - 1.76}{6.02} \quad (2.1.5)$$

## 2.2 Types of Analog-to-Digital Converters

A brief introduction to the main ADC topologies will be performed in this section to later select the structure that best suits our application's needs. But, first, a differentiation must be made between two options. Nyquist-rate converters sample at twice the maximum signal frequency and have a maximum achievable resolution of approximately 16-18 bits; while reaching conversion rates of up to Gs/s. The other type is over-sampled converters, which sample at a frequency larger than two times the maximum signal frequency, and their maximum achievable resolution is upwards of 20 bits. However, their bandwidth is quite limited [10]. In this section all of the presented but the sigma-delta are Nyquist-rate converters.

### Slope converters

If the converter topologies are introduced from lower to the higher sampling frequency, slope converters must be considered first. This group encompasses the single and dual-slope; however, only dual slope converters will be mentioned in this work because the single slope type is virtually unused. The dual-slope works as illustrated in Figure 2.4. At the initial time, the input signal is applied to an integrator. After a predetermined amount of time (T), the reference voltage is applied to the same integrator but with different polarity. When the reference is applied, the counter restarts and stops when

the integrator output reaches zero, obtaining a count value proportional to the sampled signal. This converter type can achieve high resolutions but its speed is closely tied to the resolution itself. Moreover, the precision and robustness of the ramp generator against voltage and temperature variations are critical, as it affects the overall linearity.

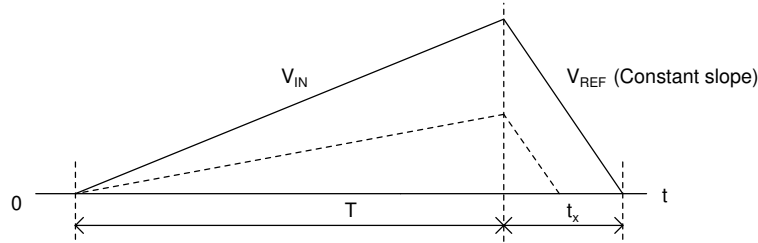


Figure 2.4: Timing diagram of a dual-slope converter [11].

### Sigma-Delta converters

Suppose higher speeds and resolutions are desired than those achievable by the slope converters. In that case, an option is to consider the sigma-delta topology, which through techniques such as oversampling and noise-shaping can obtain resolutions upwards of 20 bits.

The design of the sigma-delta consists mainly of three parts: the sigma-delta modulator (Figure 2.5), the digital filter, and the decimator. The modulator converts the analog input signal to the digital world via Pulse Code Modulation (PCM), a binary sequence containing the converter's oversampling rate. Then, the digital filter and the decimator convert the PCM stream to a higher resolution signal, filtering and sampling it down to the desired sampling rate.

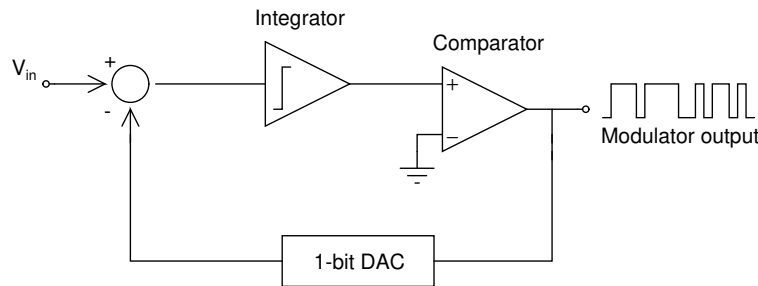


Figure 2.5: Block diagram of a sigma-delta modulator [12].

As seen in Figure 2.6, when compared to a conventional Nyquist-rate converter, oversampling decreases the amplitude of the noise floor, spreading it over a much more extensive frequency range. Suppose that the oversampling technique is combined with noise-shaping, a method inherent in the sigma-delta converter, which allows moving some of the noise to higher frequencies to then be removed via the digital low-pass

filter. Combining the two techniques is the reason why the sigma-delta converter can obtain such high resolutions. However, it comes mainly at the cost of a high-frequency clock and a large silicon area consumption by the digital part [13].

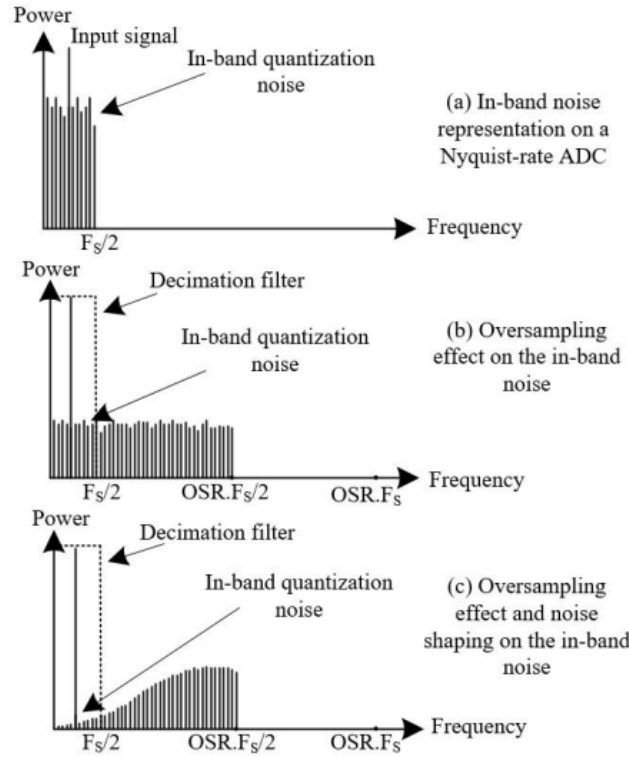
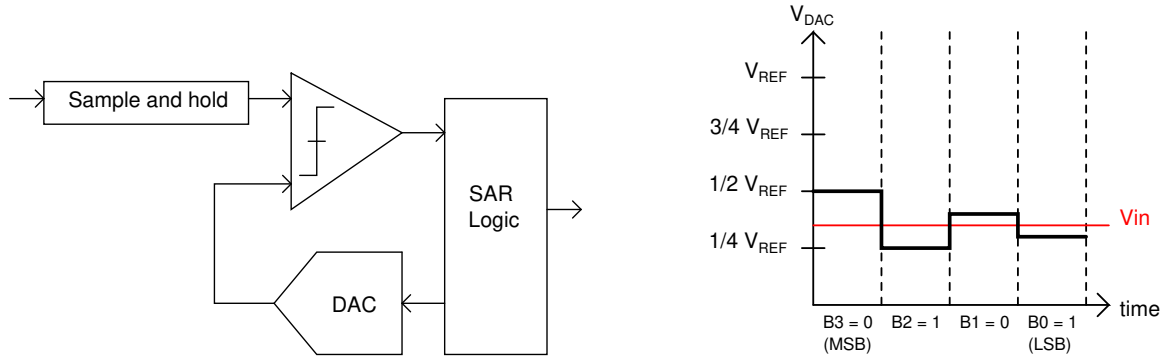


Figure 2.6: Graphical representation of the oversampling and noise-shaping techniques present in a sigma-delta converter [14].

### Successive approximation converters

If higher speeds than the sigma-delta are desired, the next in line is a serial, step-by-step converter, the SAR. The typical SAR ADC is based on the binary search algorithm and consists of four blocks (Figure 2.7a): the sample and hold circuit, where the analog value is sampled; the comparator, which compares the value sampled and the one provided by the DAC; the logic, which determines the value executed by the DAC, and the DAC itself. The principle of operation of the SAR is shown in Figure 2.7b, where the sampled input is compared iteratively to the voltage value provided by the DAC. In the first step of the process, the analog input is compared to the starting point of half the reference voltage; as the analog input is lower, the Most Significant Bit (MSB) will be set to '0', then the value at the DAC output will update and be divided by two. In the second cycle, as the input value is larger than the one provided by the DAC, bit 2 will be set to '1', and the SAR logic will adjust the DAC value. The cycle ends when all the bits have been determined, obtaining a digital word whose length is the converter's resolution.



(a) Block diagram of a SAR ADC [15].

(b) Timing diagram of a 4-bit SAR ADC [16].

Figure 2.7: Block and timing diagrams for the SAR ADC.

In summary, the SAR ADC is a low-power solution that is very attractive for medium resolutions and sampling frequencies, capable of obtaining good performance for converters around 8 to 14 bits and frequencies ranging from a few kHz to tens of MHz.

### Flash converters

The flash converter (Figure 2.8) can be found going a step further in speed. The principle of operation is to compare the input voltage against an array of threshold voltages. Unlike in the SAR topology, the flash converter compares it at once, using many comparator blocks to generate a thermometer code that can then be translated utilizing an encoder. Thus, the flash ADC's main building blocks are a bank of references, which can be created using a resistor string;  $2^N-1$  comparators; and an encoder.

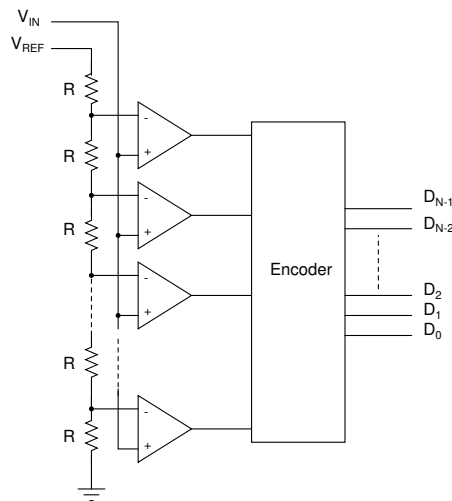


Figure 2.8: Block diagram of a flash converter [17].



In summary, the flash converter is targeted for fast speeds but low resolutions, as the number of comparators scales exponentially with the number of bits. Generally, it is also a topology with high area and power consumption. Another limiting factor of this type of converter are bubble errors, which occur when a comparator makes a wrong decision. This type of error is severe, as it produces non-monotonicity and missing codes [10].

### Pipeline converters

Reaching the top of the spectrum in terms of speed comes the pipeline converter, whose principle of operation is to perform the conversion in several steps, obtaining  $M$  bits per stage. Each stage of the pipeline serves an  $M$ -bit ADC conversion and generates a residue passed into the next stage, as shown in Figure 2.9. A simple pipeline consists of a sample and hold circuit, a comparator, and a switch.

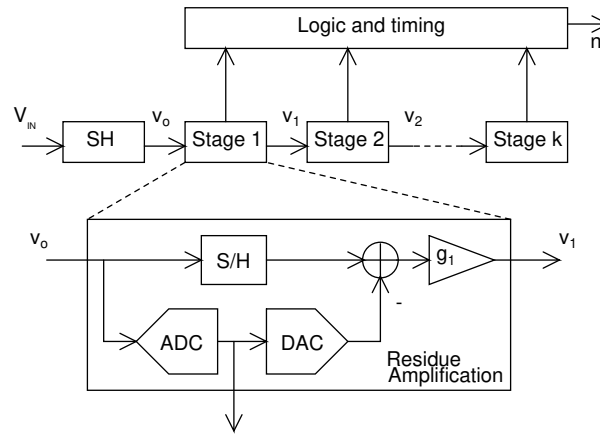


Figure 2.9: Block diagram of a pipeline converter [12].

The ADC will require  $N$  stages in a pipeline converter with a 1-bit step, linearly increasing the power consumption with every added bit. Intuitively, the conversion takes  $N$  clock cycles in the case 1-bit steps are used. The main advantage of pipeline converters is that all stages can operate concurrently. Consequently, the equivalent throughput is one conversion per clock cycle, making them suitable for high-speed frequencies with moderate resolutions. However, it should be noted that even though the converter can achieve very high speeds, latency must be considered.

## 2.3 Comparison table

Once the main converter topologies have been presented, it can be helpful to summarize the main characteristics, as in Table 2.3. The main comparison categories selected are the resolution, sampling frequency, power consumption, and the cycles it takes to obtain a conversion. Additional columns containing each category's main advantages and disadvantages are also introduced.

Type	Resolution	Sampling frequency	Power consumption	Cycles for conversion	Advantages	Issues
Slope	14-20 bits.	10-1000 S/s	Low.	$2^N$	High accuracy. Monotonic.	Slow conversion rates. Ramp errors limit linearity.
Sigma-Delta	12-24 bits	kS/s to tens of MS/s	Low.	-	Very high resolution. Very low noise.	High-frequency clock. Limited sample rate.
Successive Approximation (SAR)	8-14 bits.	0.1-100 MS/s	Very low.	Typically $N+1$ cycles	Very low power consumption. Sampling inherent of the structure.	Area influenced by minimum unit capacitance in the DAC.
Flash	6-10 bits.	Max. 1-2 GS/s	High.	1 cycle	Very fast.	Large input capacitance. Large power consumption. Bubble errors.
Pipeline	10-14 bits	100 MS/s - 2 Gs/s.	Medium. Increases with $N$ .	1 cycle	High resolution and speed.	Latency.

Table 2.1: Comparison table between the different types of ADC.

## 2.4 Topology selection

In this thesis' case, the chosen topology can be obtained via the multiple constraints introduced by the system, and depending on those constraints, the topologies shown in Table 2.3 can be discarded until the most appropriate is left.

For the first restriction, the application data output was considered, as it is known that strain sensors tend not to require speeds of MHz, and it is certain that, in this case, the conversion time for a single strain cell is not restrictive. However, multiple cells shall be placed in an array configuration, meaning that the total conversion time will be substantially larger. For example, suppose the refresh rate is 60 Hz, and it is intended to obtain a conversion for all the cells in the array in a single period. In that case, the sampling frequency will depend linearly on the number of cells. On the other side of the spectrum, the maximum sampling frequency shall be limited by the speed of the communication bus. For this application, the Fast Mode (Fm) of the Inter-Integrated Circuit (I2C) was selected, with a maximum speed of 400 kbit/s.

Furthermore, as mentioned, there have been several design choices throughout the application to minimize power consumption. Thus, low-power topologies were favored.

Moreover, a previous analysis was carried out to determine the number of bits of the design. It was identified that the converter should be able to resolve around 1 mV or less with a full-scale voltage of 1.8 V, leading to a resolution of 12 bits.

With all the information at our disposal and being mindful of the power consumption and speed restrictions, it was clear that the pipeline and flash topologies were unsuitable due to being optimized to work at higher sampling frequencies. So were slope converters, as they tend to perform better at lower frequencies than the ones desired in the application. Thus, two topologies remained, the sigma-delta and the SAR.

When choosing between the two remaining, the sigma-delta was discarded, as, even though the desired resolution and sampling speed should be achievable, the high-resolution clock made the design less attractive. Equally, SAR converters achieve lower power consumption than the sigma-delta, which made it the preferred solution.

In the end, the structure selected was a Successive Approximation Register (SAR) converter of 12 bits of resolution with a sampling frequency of 400 kS/s. This converter shall be implemented in a 180 nm topology.

## 2.5 Differential SAR ADC

Once the topology has been defined and the main constraints of the system are known, before designing each of the individual blocks, it can be helpful to present a more comprehensive analysis of the SAR ADC.

In particular, the converter designed in this thesis was a differential SAR ADC. In such converters, the DAC is generally a charge-scaling topology due to the desire to minimize the overall power consumption. Furthermore, this structure allows the merging of the sample and hold and the DAC, as the capacitors of the DAC are used for sampling. To illustrate the process, consider the 5-bit ADC in Figure 2.10. For simplicity purposes, a single-ended topology will be introduced first.

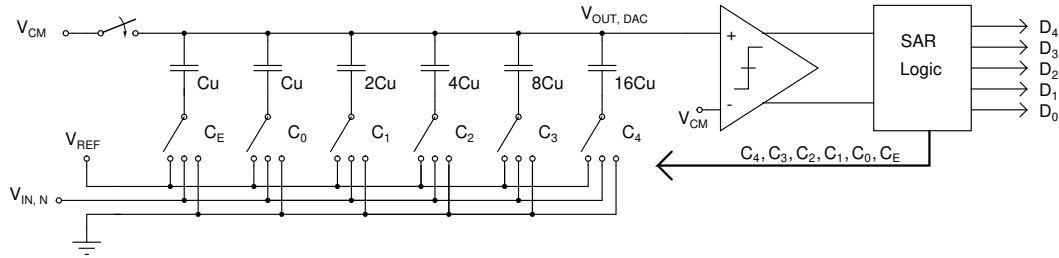


Figure 2.10: Schematic of the 5-bit single-ended SAR ADC.

The conversion procedure consists of two phases, sampling and charge redistribution. During the sampling phase, the bottom plates of the capacitor array sample the input voltage ( $V_{IN}$ ) while the top plates are set to the common-mode ( $V_{CM} = (1/2) \times V_{REF} = 0.9 \text{ V}$ ). Across the capacitors, this results in the charge shown in Equation 2.5.1.

$$Q_1 = C_{TOTAL} (V_{CM} - V_{IN}) = C_{TOTAL} \left( \frac{1}{2} V_{REF} - V_{IN} \right) \quad (2.5.1)$$

Once the sampling phase is over, the connection to the input and common-mode voltage is released. Then, the capacitances in the array are either connected to the reference voltage ( $V_{REF}$ ) or ground depending on the SAR logic, producing a voltage division. The charge across the capacitors in this phase is illustrated in Equation 2.5.2, being  $C_{EQ}$  the summed charge of the capacitances connected to  $V_{REF}$ .

$$Q_2 = C_{EQ} (V_{OUT,DAC} - V_{REF}) + (C_{TOTAL} - C_{EQ})(V_{OUT,DAC}) \quad (2.5.2)$$

As the charge has only redistributed, by combining Equations 2.5.1 and 2.5.2, one can reach Equation 2.5.3, that shows the voltage at the top plate of the DAC ( $V_{OUT,DAC}$ ).

$$V_{OUT,DAC} = \frac{1}{2} V_{REF} - V_{IN} + V_{REF} \frac{C_{EQ}}{C_{TOT}} \quad (2.5.3)$$

For the first cycle,  $C_4$  will be connected to the  $V_{REF}$  while all others to ground. The comparator will then determine  $D_4$  by comparing the values at the comparator's inputs

( $V_+ = V_{OUT,DAC}$ ,  $V_- = V_{CM}$ ). Note that for the single-ended case, if the positive input is larger, the correspondent bit will be set to ‘0’; otherwise, to ‘1’. Once the comparison has been performed, the SAR logic will update capacitor  $C_4$ , leaving connected to  $V_{REF}$  or switching it ground. In the second cycle, capacitor  $C_3$  will be connected to  $V_{REF}$  and a new comparison will start. This process is followed for the remaining bits. For  $V_{IN} = 0.3$  V and  $V_{REF} = 1.8$  V, the conversion procedure is shown in Table 2.2.

Cycle	1	2	3	4	5
<b>DAC input</b>	10000	01000	00100	00110	00101
<b>DAC output</b>	1.5 V	1.05 V	0.825 V	0.937 V	0.881 V
<b>Bit</b>	$D_4 = 0$	$D_3 = 0$	$D_2 = 1$	$D_1 = 0$	$D_0 = 1$

Table 2.2: Example of the SAR algorithm for an input voltage of 0.3 V.

Note that the LSB bits will always converge to  $V_{CM}$  for every input value. This decision significantly eases the comparator’s design, as the smaller comparisons will be made close to common-mode instead of doing so near the reference voltage or ground. This is due to connecting the top plate of the DAC to common-mode during sampling.

Following the single-ended example, a differential topology can be obtained (Figure 2.11). The bit searching procedure for the differential ADC is the same as in the single-ended topology. Once sampled the input, each array’s MSB capacitor is connected to the reference voltage and updated after the comparison. Afterwards, the binary search algorithm determines the rest of the bits. For a conversion cycle, the voltages at the top plates of the DAC can be seen in Figure 2.12. This switching scheme is called the Conventional Switching Algorithm, while not as efficient as other proposals such as the Split-Capacitor [18] or the Monotonic [19], it provides other benefits. First, it is the most simple in terms of the number of switches and clock edges [18]. Likewise, it has the advantage of using a constant common-mode voltage, converging to that value and providing the benefits mentioned in the single-ended case. Furthermore, as the voltages of the top plates of the DAC begin and converge to  $V_{CM}$  the charges across the parasitic capacitors on the top plates are the same at both time instances, making such parasitics transparent to the operation [20].

For the SAR ADC, a differential architecture was favored over a single-ended one as it allows an improvement of the overall performance and higher SNDR values. The main advantages of a differential ADC are immunity to common-mode noise and doubling the input’s dynamic range. However, this comes at the cost of power and area consumption, as well as an increase in the system’s overall complexity.

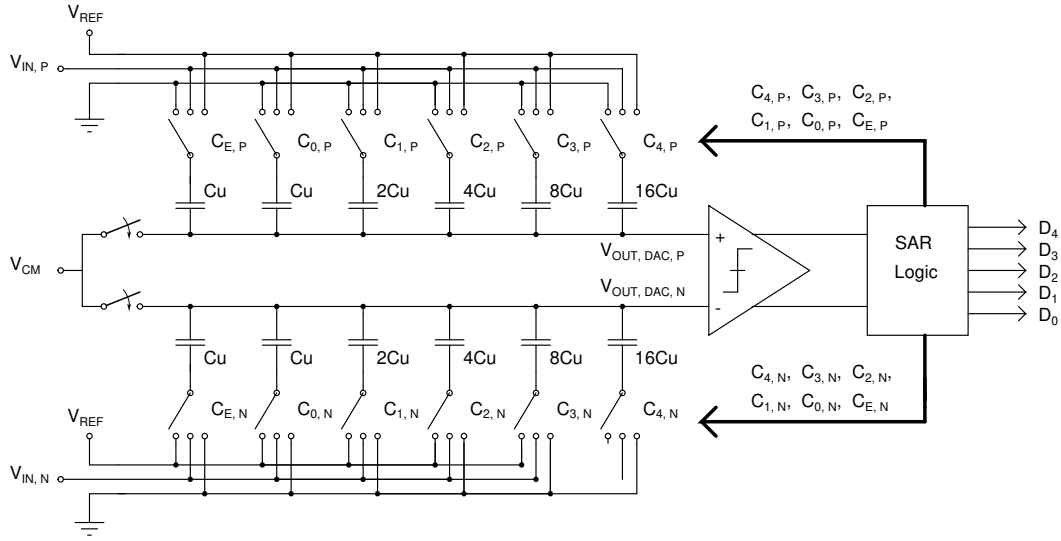
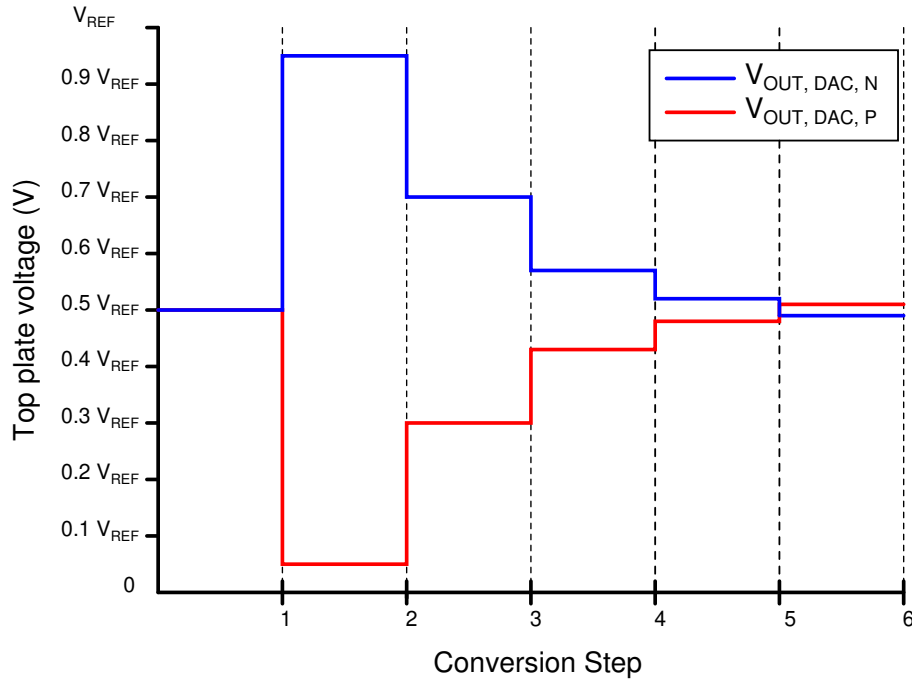


Figure 2.11: Schematic of the 5-bit differential SAR ADC.


 Figure 2.12: Top plate waveforms using the conventional switching algorithm. The inputs are  $V_{IN,P} = 0.95 V_{REF}$  and  $V_{IN,N} = 0.05 V_{REF}$ . The obtained bit sequence is 11110.

# Chapter 3

## Digital-to-Analog Converter

Once a previous study on the SAR ADC was performed, and the most important constraints were defined, it is time to look at each individual block and how it was implemented. Starting with the DAC, which was designed keeping in mind performance, power consumption, and area. It should be noted that the DAC will likely be the component with the largest footprint.

Apart from linearity, power, and area concerns, the speed of the DAC has to be taken into account. For example, the stabilization time, limited by the system's time constant, can induce issues for very high-speed converters.

### 3.1 Conventional binary-weighted array

As it was briefly mentioned, in most SAR ADCs, the topology chosen is the charge-scaling DAC, mainly due to power-saving reasons. Due to that motive, the charge-scaling Conventional Binary-Weighted array (CBW) was the first considered structure. First proposed by [21], the CBW is implemented with an array of binary-weighted capacitors. Thus, for an N-bit converter, there are N+1 capacitors and a total capacitance equal to  $2^N$  the unit capacitor value. The single-ended structure of the CBW DAC is introduced in Figure 3.1.

However, there is one main disadvantage with this topology, this being its large size. This problem is greatly accentuated for designs with resolutions larger than 10 bits. Furthermore, this size issue does not only concern the area and the system's power requirements, as the DAC is also used for sampling. Hence, increasing the size of the sampling circuitry as well. For example, in this thesis case and considering the technology available, the minimum capacitance value corresponds to a fringe capacitor of 23.9 fF. For that case, the total capacitance obtained for the single-ended array was 98 pF, making it a very power-hungry and area-consuming circuit. In such cases, an

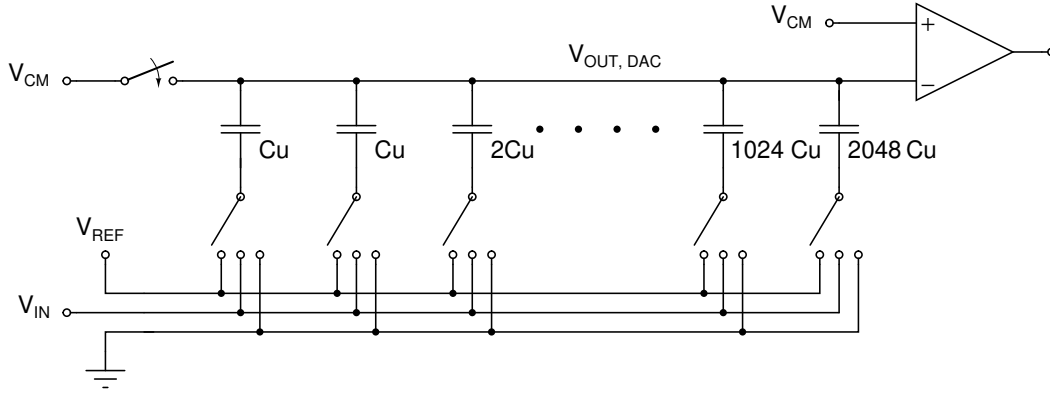


Figure 3.1: Conventional binary-weighted array DAC for a 12-bit ADC.

option to minimize the value of the DAC array could be to use capacitors in series for the LSB, as proposed in [22].

## 3.2 Binary-weighted array with attenuation capacitor

To not obtain ridiculous values of capacitance, which would increase the area and power consumption to levels above the desired, the alternative of the Binary-Weighted Array with attenuation capacitor (BWA) was considered. First proposed by [23] and depicted in its single-ended form in Figure 3.2. This structure uses an attenuation capacitor to split the DAC array in two, a MSB DAC and an LSB DAC. The idea is that the total capacitance value on LSB DAC is equivalent to the capacitance of the lowest bit in the MSB array, effectively making the two arrays have the same scaling.

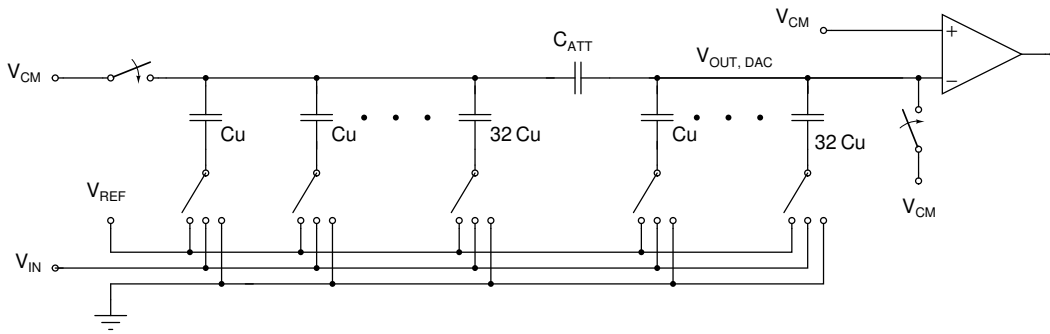


Figure 3.2: Binary-weighted array with attenuation capacitor for a 12-bit ADC using 6:6 segmentation.

One of the main issues observed for this topology was the attenuation capacitor, which tends to be a non-natural capacitor, meaning that the value will be a fractional multiple of the unit capacitor. This leads to problems in the layout phase, as fractional numbers are inaccurate due to the finite manufacturing grid [24].



As it was observed, this design tends to work quite well to minimize the size of the total capacitance; however, as proven by [25], to obtain the same performance as the CBW DAC, it would require a larger total capacitance and power consumption than the latter. Thus, it is common to use error correction mechanisms if this topology is pursued, as shown in [20] and [26].

When it comes to the array segmentation, it should be split equally to minimize the total capacitance, meaning that for a 12-bit DAC, the optimal segmentation degree is 6:6 to reduce power and area. However, other possibilities trade power for performance, such as 8:4 or 10:2 segmentation proposals, as represented in [24].

### 3.3 R-C DAC

Due to the issues observed with both the CBW and BWA DACs, other topologies were explored. One of such was the R-C DAC, which is a hybrid topology that combines a charge-scaling DAC for the most significant bits, and a voltage-scaling DAC for the less significant ones, proposed by [27] and depicted in its single-ended form in Figure 3.3.

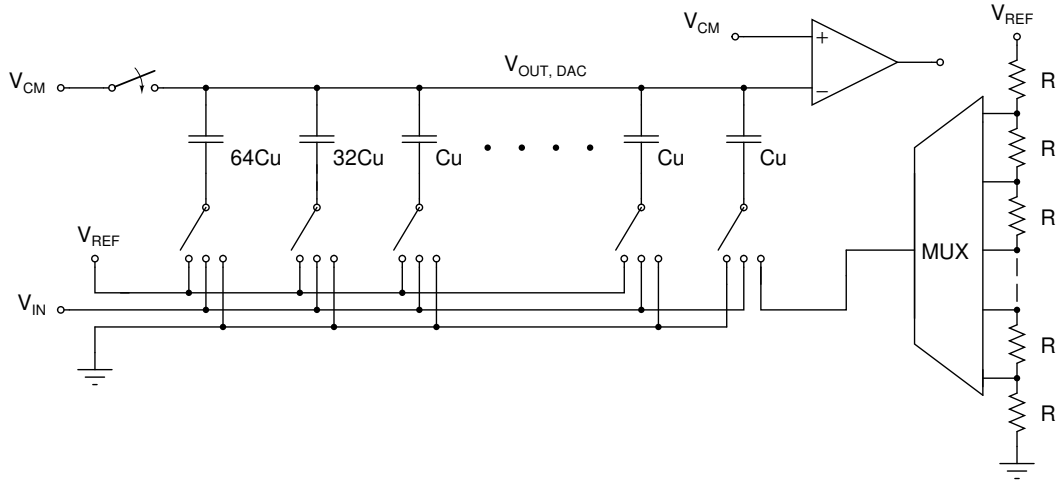


Figure 3.3: R-C DAC topology for a 12-bit ADC using 7:5 segmentation.

The voltage-scaling DAC is based on a resistor string that creates all possible output voltages with a division from the reference one. Then, a binary tree of switches is used to assign the output to the correct voltage value. The output of the voltage-scaling DAC is then divided by the C-DAC passive network, obtaining the required steps at the input of the comparator [27]. As presented in Equation 3.3.1, the voltage at the top plate of the DAC will be equal to the voltage provided by the C-DAC plus the voltage provided by the R-DAC divided by  $2^7$ .

$$V_{OUT,DAC} = V_{C-DAC} + \frac{V_{R-DAC}}{2^7} \quad (3.3.1)$$

Note that as a unary-number of components are used in the resistor string DAC, it ensures monotonicity. In this topology, the trade-off between speed and power consumption is evident. If it is desired to reduce the power consumption of the system, then the unit value of resistance in the resistor string shall be increased, enlarging the time constant of the system, which consequently limits the maximum operating frequency of the DAC. Otherwise, if it is desired to operate at larger sampling frequencies, the total resistance of the DAC shall be minimized, resulting in more significant power consumption.

This topology can reduce total capacitance and area while still obtaining good performance and reasonable power consumption values, making it an attractive solution for medium-resolution, medium-speed ADC. Furthermore, it should also be taken into account that the decision of how many bits the converter should be split is essential. As for every extra bit in the resistor string DAC, the area of both the multiplexer and the resistor string doubles, increasing the complexity.

### 3.4 Implementation

In this thesis' case, the R-C DAC topology was pursued, due to the area issues of the CBW DAC and the non-linearity concerns of the BWA structure. Regarding the segmentation degree, as proposed in [27], 7 MSB for the charge-scaling DAC for the MSB and 5 LSB voltage-scaling DAC were selected.

To quantize the DAC, the starting point was to split it into two parts, one being the charge-scaling C-DAC array and the other the voltage-scaling R-DAC array. For the first, there are three main limiting factors of unit capacitance [25]. These are:

1. KTC noise.
2. Capacitor matching.
3. Design rules.

The starting limiting factor was KTC noise, which limits the sampling capacitance of the design, Equation 3.4.1 represents it.

$$\bar{v}^2 = \frac{k_B T}{C_{TOT}} \quad (3.4.1)$$

Where  $k_B$  is the Boltzmann constant, equaling  $1.380649 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$ ,  $T$  is the temperature in Kelvin, and  $C_{TOT}$  is the total capacitance of the DAC array.

To preserve the ENOB, the thermal noise should be below the quantization noise, from which Equation 3.4.2 was obtained, giving a minimum value to the total capacitance of the DAC array.

$$C_{TOT} > 12k_B T \frac{2^{2N}}{V_{FS}^2} > 257.2 \text{ fF} \quad (3.4.2)$$

Thus, after using the mentioned equation, the minimum value of total capacitance was found to be 257.2 fF, with a minimum unit capacitance of 2 fF.

For the capacitance mismatch limit, the analysis used follows the one provided by [28]. Concerning the unit capacitance value, it was defined via the nominal value  $C_u$  and a standard deviation  $\sigma_u$ , relating to the DNL in the way Equation 3.4.3 shows. For the C-DAC design, only the DNL was considered as it is more restrictive than its INL counterpart.

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1} \frac{\sigma_u}{C_u} LSB \quad (3.4.3)$$

The capacitor mismatch in the employed 180 nm technology can be expressed as in Equation 3.4.4. While the capacitor value can be calculated as in Equation 3.4.5.

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC}{\sqrt{W \times L}} \quad (3.4.4)$$

$$C = K_C \times A \quad (3.4.5)$$

Where  $\sigma\left(\frac{\Delta C}{C}\right)$  is the standard deviation for capacitor mismatch,  $AC$  is the Pelgrom coefficient of capacitor mismatch, and  $K_C$  is the capacitor density parameter. Here, the consideration that the standard deviation of a single capacitor to the nominal value is by factor  $\sqrt{2}$  smaller than that of the difference between two capacitors was made. Thus,  $\sigma\left(\frac{\Delta C}{C}\right)$  was divided by  $\sqrt{2}$ , equaling to  $\frac{\sigma_u}{C_u}$  [28], and reaching Equation 3.4.6. Furthermore, a high yield restriction was introduced, such as that 99.7 % of the circuits shall have smaller DNL than 1/2 LSB. Combining 3  $\sigma_{DNL,MAX} = \frac{1}{2} LSB$  to the analysis.

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1} \frac{AC}{\sqrt{C_u/K_c}} LSB \quad (3.4.6)$$

For the single-ended case, the Equation obtained regarding the minimum capacitance value is shown in Equation 3.4.7.

$$C_U = 18 (2^N - 1) AC^2 K_C \quad (3.4.7)$$

As a differential topology is used, Equation 3.4.7 was divided by  $\sqrt{2}$ . This is because a differential topology doubles the signal range while only increasing  $\sqrt{2}$  times the voltage error introduced by mismatch [28], obtaining Equation 3.4.8.

$$C_U = \frac{18}{\sqrt{2}} (2^N - 1) AC^2 K_C \quad (3.4.8)$$

In this thesis, the decision to use high capacitance Metal-Insulator-Metal (MIM) capacitors was made, as they provide better mismatch and capacitance density characteristics than the lower valued fringe capacitors. For the selected capacitor in the  $0.18 \mu\text{m}$  technology employed, the value of the mismatch coefficient is equal to  $0.3 \text{ } \%/ \mu\text{m}$ , and the value of capacitor density,  $K_c$  is equal to  $2.35 \text{ fF}/\mu\text{m}^2$ . Thus, in the case of the C-DAC, the minimum value of unit capacitance obtained due to mismatch considerations was  $0.035 \text{ fF}$ , and a total value of the array of  $4.5 \text{ fF}$ .

Finally, the last restriction that was considered is the technology rules. In some cases, even though the KTC noise and mismatch limitations would point to lower unit capacitance values, the fact that the minimum capacitance value of the technology is higher limits the selection. In the employed technology's case, the minimum capacitance value for the high capacitance MIM capacitors is  $145 \text{ fF}$ . Thus, the limiting factor in the charge-scaling DAC was found to be technology rules. However, the size of the C-DAC array was decreased by half via setting the LSB in series connection, as demonstrated in [22], thus effectively obtaining a unit capacitance value of  $72.5 \text{ fF}$ .

Once the unit capacitance value was obtained, the switches connecting each capacitor's bottom plate to  $V_{REF}$  and  $GND$  could also be defined. For the connection to  $V_{REF}$ , a single P-channel Metal-Oxide-Semiconductor (PMOS) transistor was used, while for the connection to  $GND$ , a single N-channel Metal-Oxide-Semiconductor (NMOS) was employed. To have enough room for settling the value of the DAC, all switches were designed to obtain larger time constants than  $3 \text{ GHz}$ . The switches for the MSB capacitors were sized first, and the rest downsized accordingly.

The next step of the design consisted in sizing the voltage-scaling DAC. For this case, the main limitation is the mismatch between two resistor units, where a similar analysis as in the capacitive DAC was performed. In this DAC's case, the most restrictive is the INL, presented in Equation 3.4.9. This is mainly because the resistor string DAC is intrinsically monotonic. With increasing digital values, the upper nodes of the string will be selected, meaning that the DNL can never be below  $-1 \text{ LSB}$  since that would mean that between two consecutive nodes there is negative resistance [29].

$$\sigma_{INL} = \frac{\sqrt{2^N - 1}}{2} \frac{\sigma_R}{R_u} \quad (3.4.9)$$

For the poly resistors employed in this work, the mismatch can be defined as in Equation 3.4.10, while the resistance value is approximated as in Equation 3.4.11.

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{AR}{\sqrt{W \times L}} \quad (3.4.10)$$

$$R \approx K_R \times \frac{L}{W} \quad (3.4.11)$$

From the last two equations,  $\sigma(\frac{\Delta R}{R})$  is the standard deviation for resistor mismatch,  $AR$  is the Pelgrom coefficient of resistor mismatch, and  $K_R$  is the sheet resistance. As with the capacitor case, it was assumed that the standard deviation of a single resistor to the nominal value is by factor  $\sqrt{2}$  smaller than the difference between two resistors. Likewise, a yield of 99.7 % was targeted, and a differential topology was considered. With the mentioned restrictions a minimum area value for the resistor was obtained via Equation 3.4.12.

$$WL = \frac{4.5}{\sqrt{2}} \times (2^N - 1) AR^2 \quad (3.4.12)$$

Then, the width of the resistor could be fixed to a normalized value within the technology, which combined with the area restriction, defined the minimum length. Following that, by the use of Equation 3.4.11, a minimum value of unit resistance could be obtained to fulfill mismatch constraints. For the selected resistors, the value for the Pelgrom mismatch coefficient ( $AR$ ) corresponds to 4.9 %  $\mu\text{m}$ , and for the sheet resistance ( $K_R$ ), a value of 320  $\Omega/\square$  is used, leading to a minimum value of unit resistance of 20  $\Omega$ .

Nevertheless, even though the minimum resistance value was an option, it would have skyrocketed the R-DAC power consumption. Thus, in practice, the minimum resistor value was determined with the power-delay trade-off. The delay considered was estimated via the time constant created with the LSB capacitor of the C-DAC, which can be approximated as in Equation 3.4.13 [30].

$$\tau \approx 0.25 \times 2^N R C_{OUT} \quad (3.4.13)$$

In the end, the value of unit resistance value was set to 1.76 k $\Omega$ , obtaining a time constant of around 1 ns; which, having considered a sufficient settling time of multiple time constants, should be more than enough for the overall DAC operating frequency of around 10 MHz.

Equally, once it was verified that the time constant of the resistor string was not a limiting factor, it was convenient to estimate the time constant of the multiplexer. The latter being comprised of the on-resistance and parasitic capacitances introduced by the transistors, as in Equation 3.4.14 [29].

$$\tau_{mux} \approx R_{ON} C_{paras} \frac{N(N+1)}{2} \quad (3.4.14)$$

With that in mind, the multiplexer was implemented using transmission gate switches with width values of  $3.09 \mu\text{m}$  for the PMOS and  $1 \mu\text{m}$  for the NMOS, while the length was set to  $0.18 \mu\text{m}$ . By computing the on-resistance and the expected parasitic capacitance on each node, the value obtained for the time constant of the multiplexer is approximately 75 ps. With this in mind, it can be seen that the time constant and consequently the delay of the multiplexer should not be a speed concern for the DAC.

### 3.5 Performance

With all the parameters of the DAC defined, the performance was tested via simulation to ensure the correct behavior. First, the static metrics were obtained; as introduced in Chapter 2, the two most important are the DNL and INL. These were tested using a Monte Carlo simulation with 200 samples. The graphics of the standard deviation values obtained for the DNL and INL can be seen in Figure 3.4. Note that these values are obtained for a differential DAC.

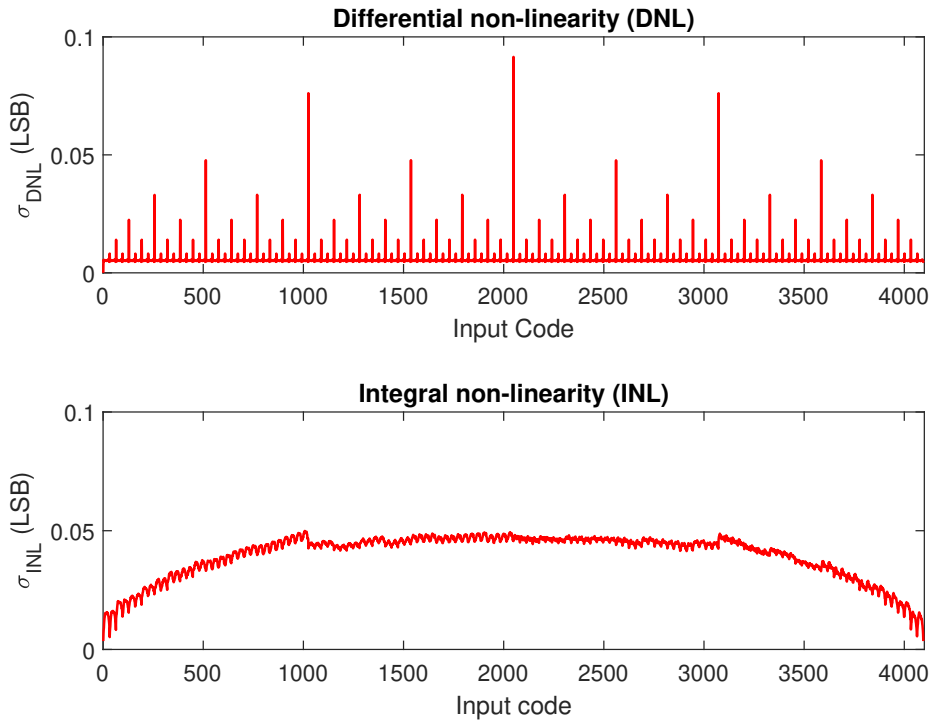


Figure 3.4: Standard deviation of the differential and integral non-linearity.

In the case of the DNL, the maximum value obtained for the standard deviation is 0.09 LSB. At the same time, the maximum and minimum values for all the runs are

0.22 LSB and -0.28 LSB, respectively. Likewise, for the case of the INL, the maximum standard deviation value is 0.05 LSB, while the maximum and minimum values are 0.21 LSB and -0.15 LSB, respectively. With these results, it is clear that the performance and the robustness obtained to mismatch are satisfactory, as the maximum and minimum values for both metrics are always under 0.5 LSB on both the positive and negative axis.

Furthermore, the dynamic metrics of the DAC were equally tested using a sinusoidal signal of full amplitude at the input and obtaining the FFT at the output. For this simulation, as was mentioned already, the approximate working frequency of the DAC is 10 MHz; thus, the simulations have been carried out at that rate. Two input frequencies were used to test the DAC, one at around 1.2 MHz and the other at around 4.8 MHz. Both simulations included transient noise with a bandwidth up to 1 GHz and the results are shown in Figure 3.5, where the lowest SNDR obtained is 73.55 dB for the largest input frequency.

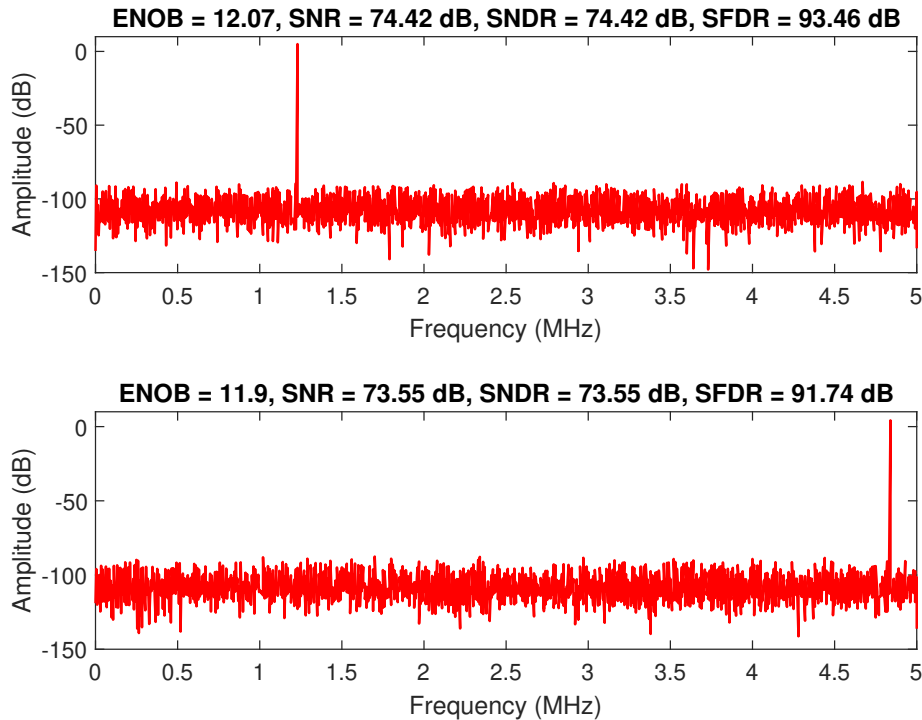


Figure 3.5: FFT of the R-C DAC output for two different sinusoidal frequencies.

When it comes to the power consumption of the DAC, it can be divided into two, the charge-scaling and the voltage-scaling, being the second more power-hungry. For the charge-scaling part, the power consumption was obtained via a simulation with the whole ADC, whereas a conversion was performed for each of the output codes,

and then the average was computed. For such a case, the power consumption obtained is  $43.05 \mu\text{W}$  (where the sampling of the input is also included). Regarding the voltage-scaling DAC, the power consumption obtained is  $107.39 \mu\text{W}$ , including both the resistor string and the multiplexer. Note that the power consumption is obtained for the DAC in differential topology. As a summary, the performance metrics for the designed DAC are shown in Table 3.1.

Metric	R-C DAC
Configuration	7 MSB charge-scaling 5 LSB resistor string
Total capacitance	9.3 pF
Total resistance	56 k $\Omega$
DNL	0.22 LSB (max) -0.28 LSB (min)
INL	0.21 LSB (max) -0.15 LSB (min)
SNDR	73.55 dB
ENOB	11.9 bits
Power Consumption	150.44 $\mu\text{W}$

Table 3.1: Performance metrics obtained for the R-C DAC.



# Chapter 4

## Sample and hold

After sizing the DAC, the sample and hold circuit could also be implemented, as both circuits' performance is closely tied. A sample and hold circuit is an intrinsic circuit in ADCs and can be found in various shapes and forms. Its most simplistic implementation consists of a series switch and a storage capacitor in parallel. The switch is clocked, defining two phases. If the switch is *ON* (shorted), the output follows the input signal, resulting in the tracking phase. Otherwise, if the switch is *OFF* (open), the capacitor's final output voltage is preserved, defining the holding phase.

In this work, as mentioned in Section 2.5, the hold capacitance is the DAC one, helping reduce both area and power consumption by not having an explicit sampling capacitor.

### 4.1 MOSFET switch

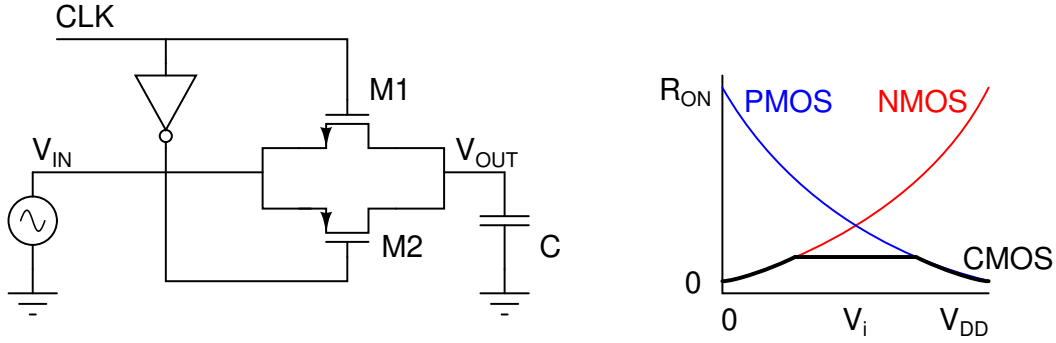
One of the main requirements that were considered when designing the sample and hold circuit was linearity. Ideally, the on-resistance of the switch should be as constant as possible not to induce distortion in the ADC. This issue is exemplified when looking at the on-resistance expression for a NMOS switch (Equation 4.1.1). Said equation is dependent on the input voltage, producing distortion and making a single NMOS switch an unsuitable candidate for the sample and hold circuit.

$$R_{on} = \frac{1}{k_N \frac{W}{L} (V_{DD} - V_{IN} - V_T)} \quad (4.1.1)$$

### 4.2 Transmission gate switch

A possible solution to minimizing the non-linearity in the switch design was to use a transmission gate (Figure 4.1a), in which the on-resistance will be composed of the parallel resistance of the NMOS and the PMOS. In said design, once the clock is high,

both the NMOS and the PMOS transistors are shorted, tracking the signal. On the counter-side, if the clock is low, both transistors are open, defining the hold state.



(a) Circuit schematic of a transmission gate switch.

(b) On-resistance of a transmission gate switch.

Figure 4.1: Schematic and on-resistance sketches of a transmission gate switch.

In theory, the parallel resistance of the transmission gate should be reasonably constant (Figure 4.1b). While it is true that this approach works much better than the single NMOS or PMOS structure, the on-resistance is not entirely invariant. For higher-resolution designs, the slight distortion introduced can cause an ENOB degradation.

### 4.3 Bootstrapped switch

The third alternative considered for the sampling switch was the bootstrapped switch. Introduced in [31], is a solution that helps preserve a linear on-resistance by providing a constant gate-source voltage for the sampling transistor,  $M_1$  in Figure 4.2. During the hold phase, when the clock is low, a capacitor is charged  $V_{REF}$  while the switch perceives 0 V at its gate, effectively disconnecting the input from the output. However, during the sampling phase, the gate-source voltage of the switch will be equal to the voltage stored in the capacitor ( $V_{REF}$ ), making it independent from the input voltage and obtaining a constant on-resistance for all input voltage values.

### 4.4 Implementation

In this thesis case, the chosen alternative was the bootstrapped switch, as while the transmission gate presented an improvement over the simple NMOS switch, the higher linearity provided by the bootstrapped switch was more desirable. The transistor-level implementation is shown in Figure 4.3.

For the circuit seen in Figure 4.3, the working procedure is the same as in the ideal bootstrapped switch. Starting with the holding period ( $CLK = 1$ ), transistors  $M_4$  and

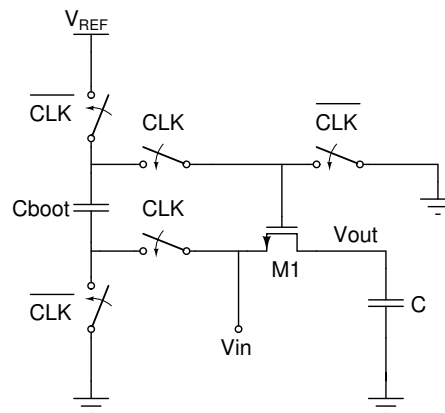


Figure 4.2: Simplified diagram of the bootstrapped sample and hold circuit.

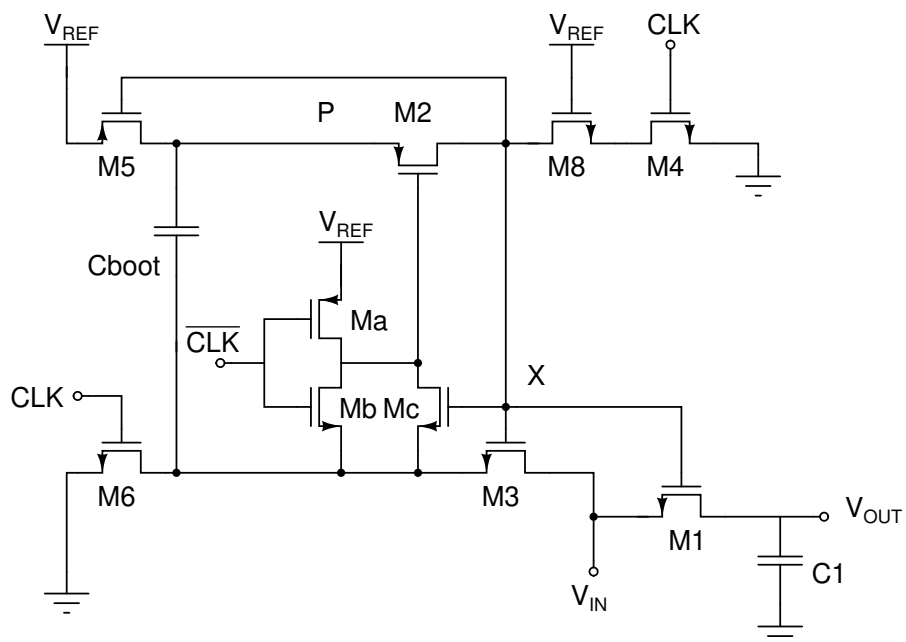


Figure 4.3: Transistor level diagram of the bootstrapped switch.

$M_8$  will bring the gate voltage of sampling transistor  $M_1$  to zero. The voltage on *node X* opens  $M_3$ , disconnecting the input from the bottom plate of the capacitor. In the meantime,  $M_5$  and  $M_6$  are closed, charging  $C_{boot}$ . Furthermore, as the clock is high, transistor  $M_a$  will be closed, setting a high voltage on the gate of  $M_2$ , disconnecting the top plate of the capacitor from the gate of  $M_1$ .

In the tracking period ( $CLK = 0$ ),  $M_4$  and  $M_6$  will be off. While  $M_2$  is turned on by  $M_c$  and  $M_b$ , the latter only being used during the start-up. Moreover, as the voltage on *node X* is equivalent to  $V_{IN} + V_{REF}$ , transistor  $M_3$  is closed. Both actions couple the gate and source of  $M_1$  to the terminals of the capacitor, introducing a  $V_{GS}$  voltage of  $V_{REF}$ . The transient waveform is depicted in Figure 4.4, where the tracking period has been set to 50% of the holding one.

In this design, note that transistor  $M_8$  was placed to protect  $M_4$  from device stress issues, as during the tracking period, without  $M_8$ ,  $M_4$  would experience a drain-source voltage equal to  $V_{REF} + V_{IN}$ . Moreover, the need for  $M_c$  is exhibited during the sampling phase, as if only  $M_b$  was placed, when  $V_{IN}$  approached values closer to  $V_{REF}$ , said transistor would turn off, disconnecting the gate of  $M_2$ . Nevertheless, this does not occur for  $M_c$  since the gate of said transistor is bootstrapped [32].

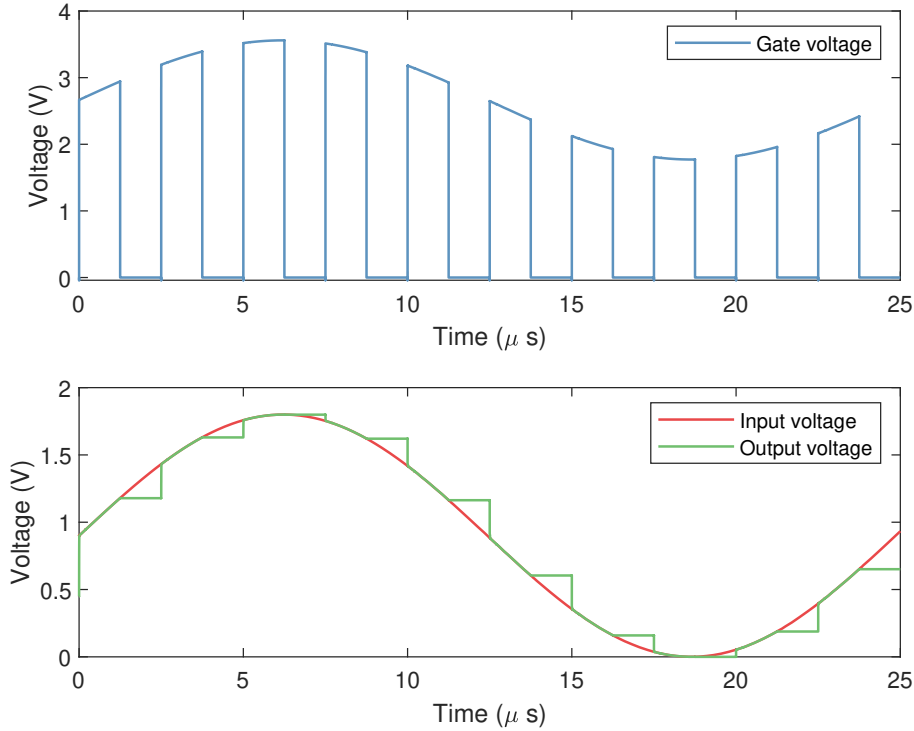


Figure 4.4: Transient waveform of the bootstrapped switch.

To size a sample and hold circuit, there are a few limitations that were taken into account. The first was already verified in Chapter 3, as the KTC noise was considered (Equations 4.4.1 and 4.4.2). Where it was seen that with an array capacitance of 9.8 pF the KTC noise introduced in the system should not be an issue.

$$\bar{v}^2 = \frac{k_B T}{C_s} \quad (4.4.1)$$

$$C_s > 12k_B T \frac{1}{\Delta} = 12k_B T \frac{2^{2N}}{V_{FS}^2} \quad (4.4.2)$$

The second restriction that was accounted for is regarding the acquisition time. Where the sampling circuit needs to allow the output to settle to less than 1/2 LSB. For an ideal switch, the acquisition time would be zero; however, real switches have on-resistance. This on-resistance forms an RC circuit with the capacitor setting a limit on the sampling time. For example, if the sampling time considered is 50% of the total time), the expression shown in Equation 4.4.5 can be reached [33].

$$\Delta v_{out}(t) = \Delta V_{in}(1 - e^{\frac{-t}{RC}}) \quad (4.4.3)$$

$$\Delta v_{out}(t = \frac{T_s}{2}) = V_{FE}(1 - e^{\frac{-T_s}{2RC}}) = V_{FE}(1 - \frac{1}{2^N}) \quad (4.4.4)$$

$$f_s < \frac{1}{2 R_{on} C_s (N + 1) \ln 2} \quad (4.4.5)$$

Thus, the size of the sample and hold switch was obtained using the restriction introduced by Equation 4.4.5, dictating the maximum switch on-resistance.

Nevertheless, another limitation that was taken into account is the jitter, which can be defined as the deviation from true periodicity [34] and can be especially important for the clock signal of the sample and hold switch. And while the jitter constraint can be quite important when it comes to high-speed, high-resolution designs, in our case, with a sampling frequency of 400 kS/s, it was deemed nonrestrictive.

Before introducing the sizing procedure, it should be noted that in this ADC, the configuration employed for the bottom-plate switches is the one in Figure 4.5. Thus, each capacitor has its own bootstrapped switch. Note that the other switches supplying the reference voltage and ground were already discussed in Chapter 3. Additionally, to ensure linearity during the sampling process, the switch connecting the top-plate of the DAC to the common-mode voltage was bootstrapped as well.

Starting with the sampling transistor, this was sized using Equation 4.4.5 (adapting the equation keeping in mind the relation between the tracking and holding period

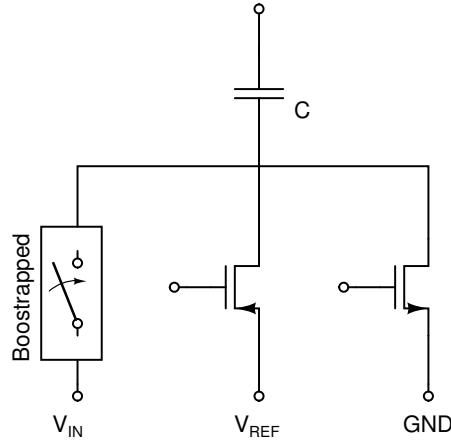


Figure 4.5: Configuration of the bottom plate switches.

of the ADC). For example, with the MSB capacitor (4.64 pF), the maximum on-resistance is 2.1 k $\Omega$ , making quite feasible to size the transistor to low-width values. With all this in mind, to be safe, a width of 1.5  $\mu\text{m}$  was selected for the sampling transistor of the MSB capacitor. The rest of the switches were scaled down in order to preserve the time constants of the system.

To size the rest of the design, the approach proposed by [32] was followed, which provides a guide on obtaining the dimensions of all the transistors in the bootstrapped design. After the sampling switch, the next transistors to be sized were  $M_2$  and  $M_4$ . The first was sized considering the RC constant formed with the parasitic capacitance at the *node X* of Figure 4.3, requiring to provide a bandwidth larger than 10 MHz. For said purpose, the width selected for  $M_2$  was 1  $\mu\text{m}$ . For the latter, it must pull down the voltage at *node X* with a high slew rate to rapidly turn off  $M_1$ ; for said purpose, the width selected was 2  $\mu\text{m}$ . The next transistor was  $M_3$ , which according to the design guide, its on-resistance should be similar to  $M_2$ ; thus, for this purpose, the size selected was 0.5  $\mu\text{m}$ . The next transistor group were  $M_5$ ,  $M_6$ , and the capacitor  $C_B$ . Starting with the capacitor, its size is dictated by the charge sharing with the parasitics of *node X*. Thus, a size of 300 fF was deemed enough to be able to ignore the parasitic capacitances tied to it. The two transistors connected to the capacitor were sized taking into account the time constant created by the three, which should be less than half the time period, which for lower sampling frequencies, should not be a big constraint. For it, both  $M_5$  and  $M_6$  were set to a size of 0.5  $\mu\text{m}$ . Due to stress issues,  $M_8$  was required, being set to the same width as  $M_4$  (2  $\mu\text{m}$ ). To preserve  $M_2$  closed during the sampling phase, transistor  $M_c$  was required. In conjunction to  $M_a$  and  $M_b$ , these three were set to 1  $\mu\text{m}$ , 1.5  $\mu\text{m}$  and 0.54  $\mu\text{m}$ , respectively. A summary of the transistor sizes is shown in Table 4.1.

Element	Width [ $\mu m$ ]	Length [ $\mu m$ ]
$M_1$	1.5	0.18
$M_2$	1	0.18
$M_3$	0.5	0.18
$M_4$	2	0.18
$M_5$	0.5	0.18
$M_6$	0.5	0.18
$M_8$	2	0.18
$M_a$	1.5	0.18
$M_b$	0.54	0.18
$M_c$	1	0.18

Table 4.1: Transistor sizes for the bootstrapped circuit shown in Figure 4.3.

## 4.5 Performance

A significant limitation that should be accounted for in terms of the sampling switch is the charge injection, as the charge injection introduced into the circuit by the sampling switch depends on the input voltage. The effect of the charge injection was verified by obtaining the introduced DNL and INL of the switch via a Monte Carlo simulation with 200 samples. The results are shown in Figure 4.6. From there, it is clear that both the mean and the standard deviation are quite small. From all the ran iterations, the maximum and minimum DNL values obtained were of 0.0174 LSB and -0.0174 LSB, respectively. While for the INL, the maximum was 0.025 LSB and the minimum - 0.022 LSB. Non-linearity values significantly smaller than the ones introduced by the DAC.

Moreover, the linearity of the sample and hold circuit was tested using a sinusoidal signal to measure the FFT at the output node of the DAC and obtain the dynamic metrics of the overall sampling system. The results are shown in Table 4.2 for the system including all the switches. Nevertheless, it should be noted that apart from the global result, all the switches were equally tested individually and all obtained similar results as the ones shown in the table.

Frequency	SNDR	ENOB
40.23 kHz	74.85 dB	12.14 bits
198.82 kHz	73.35 dB	11.89 bits

Table 4.2: SNDR and ENOB values for the bootstrapped switch configuration.

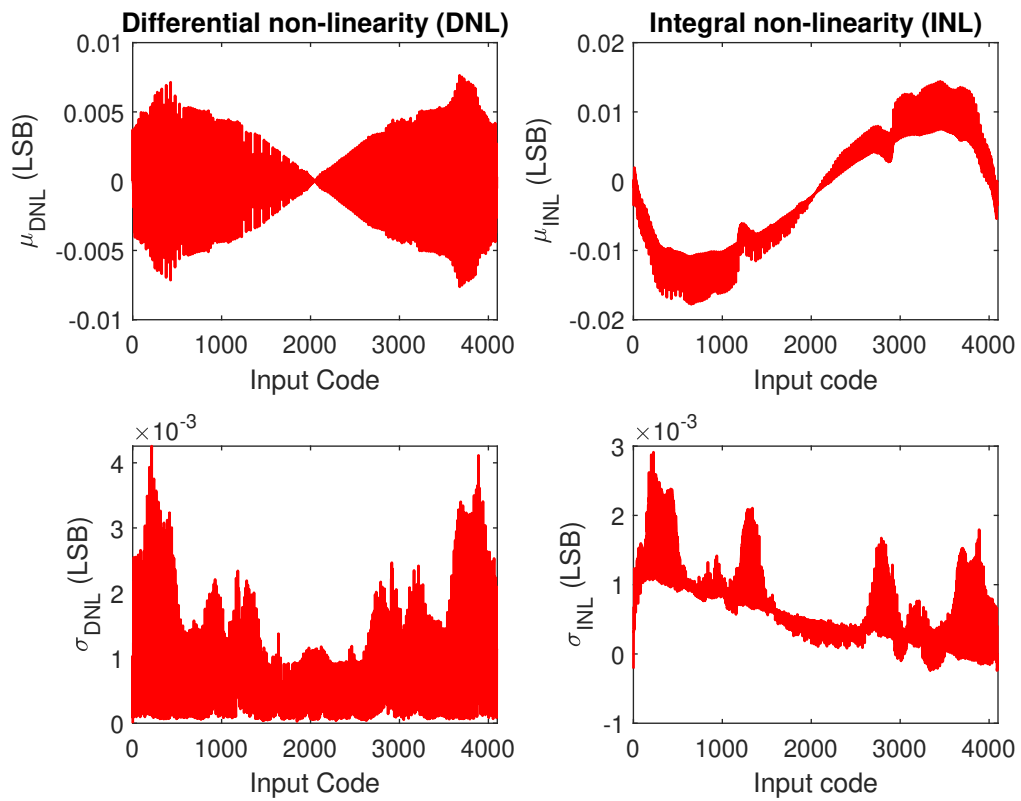


Figure 4.6: Mean and standard deviation of the DNL and INL introduced by the switches.



The power consumption of the sample and hold switch and the driving circuitry was simulated through a sweep of input voltage values, and the mean value obtained was  $1.12 \mu\text{W}$  per conversion for all the switches required in the ADC design. A summary of the performance metrics obtained is shown in Table 4.3.

Metric	Sampling switches
DNL	0.0174 LSB (max) -0.0174 LSB (min)
INL	0.025 LSB (max) -0.022 LSB (min)
SNDR	73.35 dB
ENOB	11.89 bits
Power Consumption	$1.12 \mu\text{W}$

Table 4.3: Performance metrics obtained for the sampling switches.

# Chapter 5

## Comparator

Besides the DAC, the comparator is one of the most critical pieces in the ADC. It obtains a logical output value depending on the voltage difference between the input values.

There are several options for building a comparator circuit; perhaps the most intuitive one is a high-gain amplifier. High-gain amplifiers could be considered continuous comparators, as they monitor the inputs continuously and update the output as suddenly as the inputs suffer from a change. However, ADC with larger resolutions might require extensive gain parameters, which will restrict the Gain-Bandwidth (GBW), thus making them unsuitable for most designs. Another issue related to continuous comparators is power consumption, as measuring the output continuously increases the power consumption of the whole system. Due to these limitations, most of the comparators used for ADC design are clocked latches.

The clocked latch is a circuit where the main idea is to introduce a slight imbalance depending on the difference between the input voltage values; this imbalance then will force the output to evolve to one state or another.

Most latched comparators consist of two stages, the first one a pre-amplifier and the second one the latch itself. The first generates the slight imbalance in function of the input difference, while the second decides on which state to evolve.

Regarding latched comparators, the two main types were considered. The first are static latched comparators, which obtain good kickback noise values due to having the switches being placed in the second stage instead of the first. However, the trade-off is with power consumption, as the comparator consumes DC current. The other option is the dynamic latched comparator, with the advantage of higher speed and lower power consumption at the cost of higher kickback noise [35]. In this thesis, the dynamic latch implementation was pursued due to the desire to minimize power consumption.

## 5.1 Double-tail dynamic latch

Even within the dynamic latch family, there are multiple topologies available. In this thesis, the double-tail one was chosen due to its ability of being able to set two different tail currents in an attempt to obtain a very customizable delay-power consumption trade-off. The transistor-level schematic of the double-tail dynamic latch used in this work is shown in Figure 5.1, and it was introduced in [19].

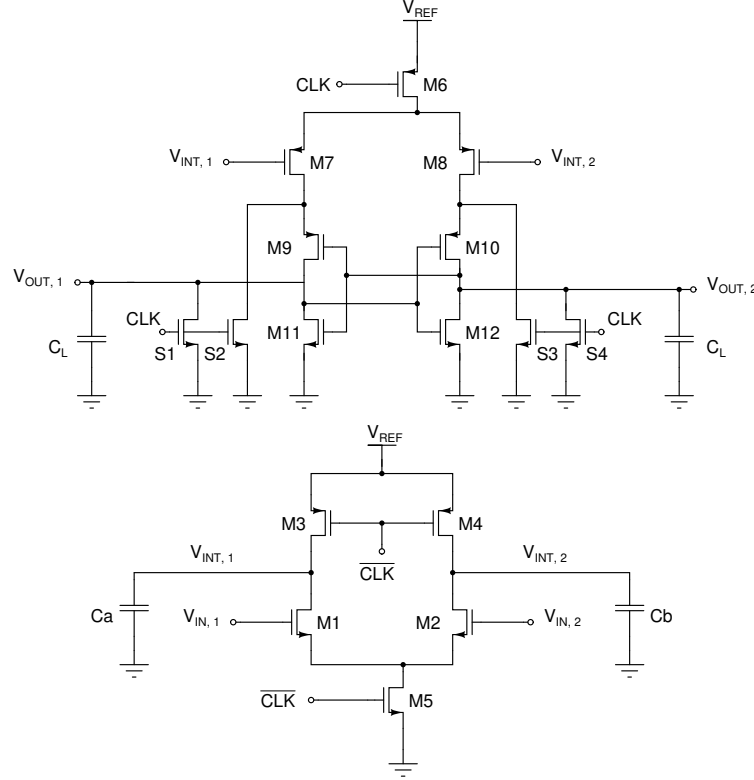


Figure 5.1: Transistor level diagram of the double-tail dynamic latch, based on [19].

The clock signal ( $CLK$ ) governs the operation of the design; when it is high, tail transistors  $M_5$  and  $M_6$  are off; thus, no current flows through the input transistors of either stage ( $M_1, M_2, M_7, M_8$ ). During this period, note that the voltages at the intermediate nodes ( $V_{INT,1}, V_{INT,2}$ ) are set to  $V_{REF}$ , pre-charging the capacitances  $C_a$  and  $C_b$ . In the second stage, the output nodes are discharged to ground by transistors  $S_1$  and  $S_4$ , giving a low value for both outputs. On the counter side, when the clock signal is low, the comparison phase starts,  $M_5$  and  $M_6$  are turned on, allowing current flow through input transistors  $M_1$  and  $M_2$ . Consequently discharging the parasitic capacitances  $C_a$  and  $C_b$  at the intermediate nodes at different speeds, depending on the difference between the input voltages,  $V_{IN,1}$  and  $V_{IN,2}$ . Once the output voltages of the first stage reach the threshold voltage of the second stage input transistors, the latch amplifies the signal until the positive feedback takes over, pulling one output to a high value and the other to low, providing rail-to-rail differential output [19]. This is exemplified in Figure 5.2, where it is clear that for a positive differential input

( $V_{IN,1} > V_{IN,2}$ ), the positive output ( $V_{OUT,1}$ ) will evolve to  $V_{REF} = 1.8$  V, but for a negative differential input ( $V_{IN,1} < V_{IN,2}$ ), the contrary occurs. Note that transistors  $S_2$  and  $S_3$  have been included to completely reset the latch during the reset phase.

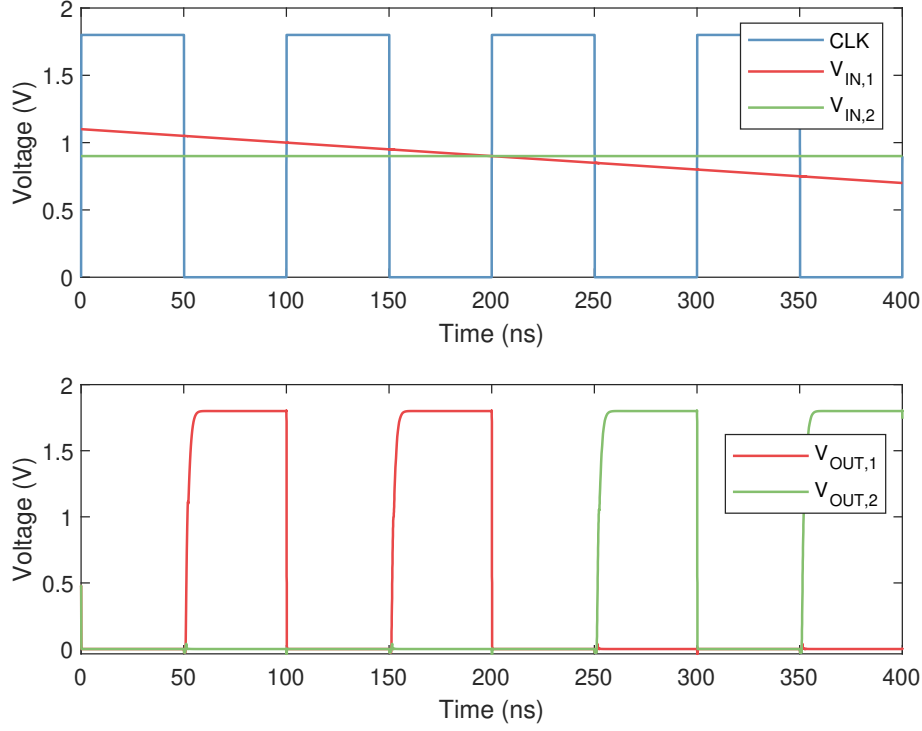


Figure 5.2: Transient simulation for the double-tail comparator shown in Figure 5.1.

## 5.2 Implementation

Noise considerations were used to size the double-tail dynamic latch. The analysis followed is based on previous studies by [19] and [36]. In those analysis, the noise and offset introduced by the second stage was not considered due to the amplification provided by the first stage. Moreover, it is argued that the efficiency will largely depend on the first stage.

When considering noise, it should be noted that the significant voltage variations on the regeneration nodes are coupled through the parasitic capacitances of the transistors to the input, originating kickback noise [37]. Such noise can result in non-linearities during the conversion process. Ideally, to reduce the kickback noise, the dimension of the input pair should be small. Nevertheless, this conflicts with the input-referred noise and timing constraints. In this work, the size of the input transistors was obtained considering input-referred noise requirements. However, once sized, it was verified that

kickback noise did not significantly reduce the comparator's performance.

The starting point of the input-referred noise analysis was to estimate the noise of the input stage. This was done based on the consideration of the thermal noise of a single MOS transistor with an equivalent noise resistor at its gate:

$$R_{n,MOS} \approx \frac{\gamma}{g_{m,MOS}} \quad (5.2.1)$$

Being  $\gamma$ , the noise excess factor with a value close to 1. In the dynamic latch, the pre-amplifier integrates the input signal and the noise from the equivalent noise resistor, the latter being estimated by Equation 5.2.2, [36].

$$\sigma_v = \sqrt{4 k T 2 R_{n,MOS} NBW} = \sqrt{4 k T \frac{2}{g_{m,MOS}} NBW} \quad (5.2.2)$$

The noise bandwidth (NBW) introduced in Equation 5.2.2 concerns the noise integrated over the integration time, which can be defined as in Equation 5.2.3.

$$NBW = \frac{1}{2 T_{int}} \quad (5.2.3)$$

The latched stage samples the output voltage of the first stage when the voltage on the intermediate nodes have changed by approximately the threshold value of the input pair of that second stage. The current through each input transistor of the first stage is then integrated into the parasitic capacitances at the intermediate nodes ( $C_a$ ,  $C_b$ ) [36]:

$$T_{int} \approx \frac{V_{th} C_a}{I_{CM}} \approx \frac{V_{th} C_b}{I_{CM}} \quad (5.2.4)$$

Combining Equations 5.2.2 and 5.2.3 and 5.2.4, allowed obtaining Equation 5.2.5. From which the parasitic capacitances were isolated, as shown in Equation 5.2.6.

$$\sigma_v = \sqrt{4 k T \frac{1}{V_{th} C_a} \frac{I_{CM}}{g_{m,MOS}}} \quad (5.2.5)$$

$$C_a = \frac{4 k T}{\sigma_v^2 V_{th}} \frac{I_{CM}}{g_{m,MOS}} \quad (5.2.6)$$

Once the operating region of the input transistors is defined, Equation 5.2.6 can be resolved, dictating the minimum parasitic capacitance values for the intermediate nodes. The minimum values obtained for the intermediate capacitances are around 20 fF. When computing the values of Equation 5.2.6 it is important to note that the threshold voltage is the one for the input of the second stage transistors [36].

Once the capacitances at the intermediate nodes were known, the minimum common-mode current could be obtained using Equation 5.2.4. In this case, the period considered was 5 ns, obtaining a minimum value of common mode current of  $1.4 \mu\text{A}$ .

With the analysis performed, the transistor width and lengths of the first stage can be obtained. Starting with the input pair, which is generally the main contributor to input-referred noise and offset voltage, was sized with a width of  $10 \mu\text{m}$  and a length of  $0.3 \mu\text{m}$ . For the PMOS transistors of the first stage, a width and a length of  $2.5 \mu\text{m}$  and  $0.18 \mu\text{m}$  were selected, respectively. Finally, for the tail transistor, a width of  $0.22 \mu\text{m}$  and a length of  $0.18 \mu\text{m}$  were deemed enough to provide the desired current.

For the second stage, the components were sized to contribute the minimum possible to the first stage's noise while trying to obtain reasonable delay values. A value of  $5 \mu\text{m}/0.18 \mu\text{m}$  was used for the second stage input transistors. Regarding the timing constraints, the tail transistor of the second stage was sized  $0.22 \mu\text{m}/0.18 \mu\text{m}$ , trying to minimize the power consumption of said stage. For the size of the latched transistors, it was opted for  $2.5 \mu\text{m}/0.18 \mu\text{m}$  for the NMOS and  $2.5 \mu\text{m}/0.18 \mu\text{m}$  for the PMOS. Finally, when it comes to the switches, they were sized to be able to bring down the voltages at their respective nodes in less than 1 ns, for which a value of  $1 \mu\text{m}/0.18 \mu\text{m}$  was sufficient. A summary of the sizes for the transistors in the dynamic comparator can be seen in Table 5.1. After simulating the comparator, the gain of the first stage before the second stage takes over is of 4.

Transistor	Width [ $\mu\text{m}$ ]	Length [ $\mu\text{m}$ ]	Nº of fingers
$M_1, M_2$	10	0.3	5
$M_3, M_4$	2.5	0.18	1
$M_5$	0.22	0.18	1
$M_6$	0.22	0.18	1
$M_7 M_8$	5	0.18	5
$M_9 M_{10}$	2.5	0.18	1
$M_{11} M_{12}$	2.5	0.18	1
$S_1, S_2, S_3, S_4$	1	0.18	1

Table 5.1: Transistor sizes for the double-tail latch in Figure 5.1.

### 5.3 Performance

Multiple parameters were looked at to assess the correct behavior and performance of the comparator. These were input-referred noise, delay, offset, and power consumption.

The first was the input-referred noise. Note that the comparator does not operate continuously; thus, a particular noise analysis was performed. Here the one presented in [38] and [39] was followed.

The starting point considers a normal distribution of variable  $x$  based around a mean value ( $\mu$ ) and a standard deviation ( $\sigma$ ). For a random variable  $M$ , the Cumulative Distribution Function (CDF) can be seen in Equation 5.3.1

$$F_M(x) = \int_{-\infty}^x f_M(a) da \quad (5.3.1)$$

While the probability of obtaining  $M < x$  is:

$$F(x) = \frac{1}{2} \left( 1 + \operatorname{erf} \left( \frac{x - \mu}{\sigma \sqrt{2}} \right) \right) \quad (5.3.2)$$

The same principle was applied to the comparator. Instead of the probability of  $x$ , the analysis considered the probability of obtaining a logic ‘1’ at the output depending on the value of the differential input voltage. Thus, if that is the case, Equation 5.3.2 can be remodeled into 5.3.3 [39].

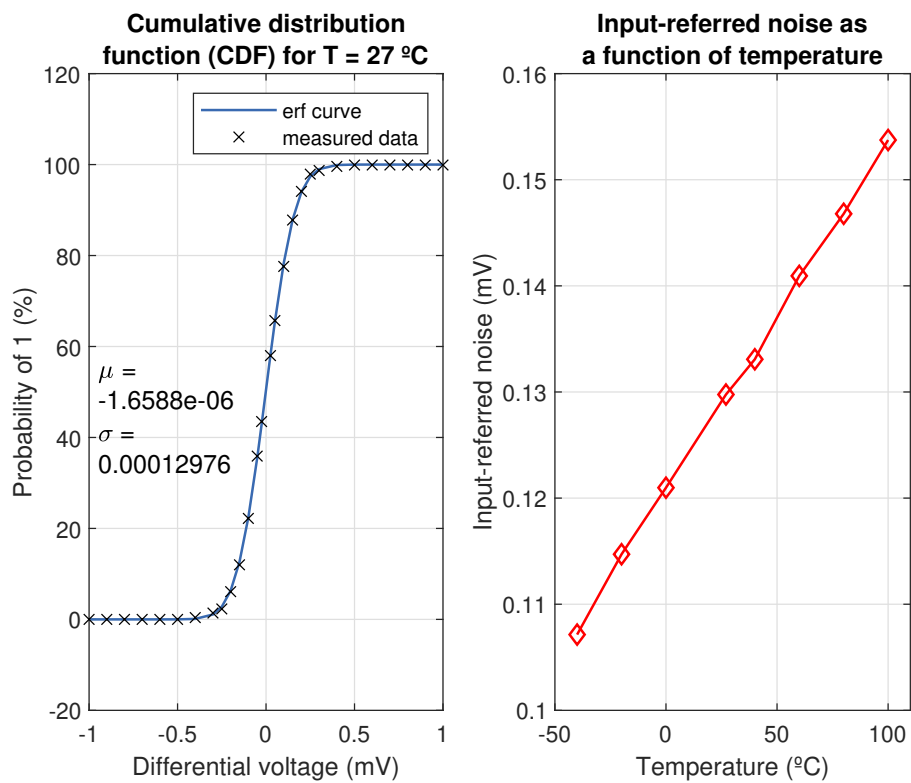
$$F(v_{diff}) = \frac{n_1}{N_{tot}} = \frac{1}{2} \left[ 1 + \operatorname{erf} \left( \frac{v_{diff} - \mu}{\sigma \sqrt{2}} \right) \right] \quad (5.3.3)$$

Being  $n_1$  the number of 1s and  $N_{tot}$  the total number of samples for the simulation. In this case, 1000 samples were obtained for each differential voltage value while the noise bandwidth used for the simulation was set to 10 GHz. The data obtained for the double-tail dynamic latch working at 27 °C can be seen in Figure 5.3a, where both the measured data and the fitted curve are shown. From the said figure, it is clear that the obtained standard deviation of the input-referred noise (Table 5.2) corresponds to a value safely below the quantization noise and should not excessively degrade the SNDR. Moreover, it is known that the noise should increase with temperature; thus, said the effect was also tested by introducing a sweep from -40°C to 100°C (Figure 5.3b). As the results show, even though the noise increases for the largest temperature value, it is still under suitable values.

Regarding the delay of the comparator, a parametric analysis was performed for different values of differential input voltage, ranging from 1 nV to 0.1 V; this sweep was performed for all four corners of the system. As can be seen in Figure 5.4a, the delay obtained for the double-tail latch is always under 6 ns even at the worst corner, which

Metric	Double-tail
Mean value	-1.66 $\mu\text{V}$
Standard deviation	129.76 $\mu\text{V}$

Table 5.2: Mean and standard deviation values of input-referred noise obtained for the double-tail dynamic latch at 27 °C.

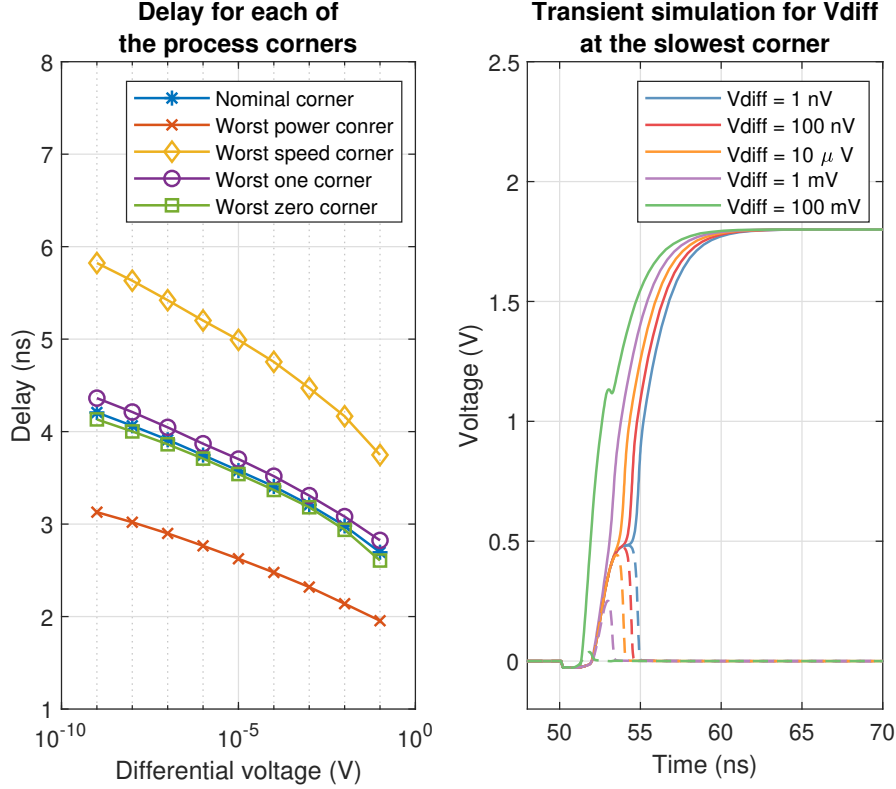


(a) CDF of the input-referred noise at 27 °C. (b) Standard deviation values of input-referred noise for different temperatures.

Figure 5.3: Input-referred noise simulations against different temperature values.



is satisfactory considering the reset cycle available. That means there will always be a stabilized output before the clock is pulled up again, around 50 ns after the comparison is requested.



(a) Delay obtained at the corners of the system for a sweep of input voltages. (b) Transient simulation of the delay at the slowest corner.

Figure 5.4: Corner simulation of the delay in the latch against a sweep of input voltages.

A Monte Carlo simulation with 200 samples was performed to compute the offset, obtaining the distribution seen in Figure 5.5.

Regarding the offset of the dynamic comparator, it arises from mainly three factors. The threshold voltage offset of the differential pair ( $\Delta V_T$ ), the effective voltage of the input pair ( $V_{GS} - V_T$ ), and the conductivity mismatch ( $\Delta\beta$ ). It should be noted that the threshold voltage offset depends mainly on the size of the input transistors, while the second is the overall conductivity mismatch between the input transistors. The first term is a static offset and thus does not degrade the linearity of the ADC [19]; its Equation can be seen in 5.3.5 [40], where the term  $A_{V,TH}$  is a constant related to the technology called *Pelgrom coefficient voltage threshold mismatch*. The second varies with the input signal common-mode voltage [19] and affects the system's linearity. In this thesis's case, as introduced in Section 2.5, the switching algorithm employed

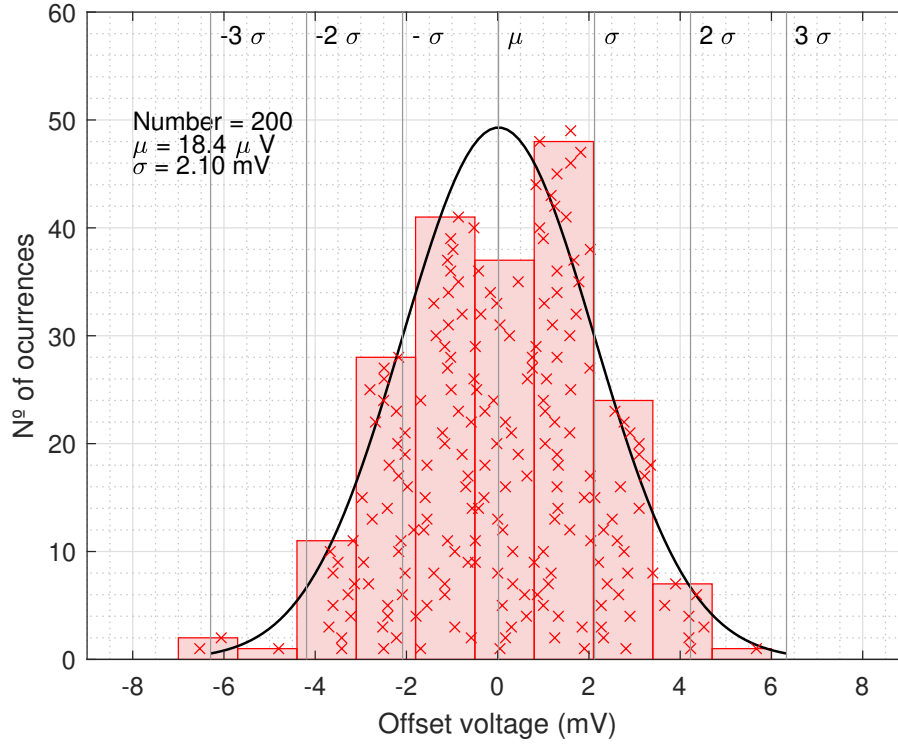


Figure 5.5: Monte Carlo simulation of the offset in the double-tail dynamic latch.

uses a constant common-mode voltage, thus limiting the contribution of the second term. Consequently, it will be assumed that the offset will be mainly produced by the threshold voltage offset contribution, causing only a static error.

$$V_{os} \approx \Delta V_T + \frac{V_{GS} - V_T}{2} \frac{\Delta\beta}{\beta} \quad (5.3.4)$$

$$\Delta V_T = \frac{A_{V,TH}}{\sqrt{WL}} \quad (5.3.5)$$

Nevertheless, in some applications, there is the desire to minimize the offset. The easiest option would be to increase the size of the input pair. However, that would produce an area and power consumption overhead. Even so, it can be noted that there are multiple options to reduce the offset values to a few hundreds of  $\mu V$  without increasing the input pair transistors to undesirable sizes. Some of these techniques propose cancellation by adding additional input transistors [41], [42], [43] or by even tuning the bulk voltages of the input pair [44]. However, these methods decrease the offset by adding significant area or/and power consumption, as they require extra circuitry. Some even require additional comparison cycles to reduce the offset, increasing the timing restrictions in the other components of the ADC as well.

Furthermore, the comparator's approximate SNDR can be computed via Equation 5.3.6

[39], where both the quantization and input-referred noise are taken into account. Using said equation, the SNDR computed is approximately 73 dB.

$$SNDR [dB] = 10 \log \left( \frac{A^2/2}{\sigma_q^2 + \sigma_{comp}^2} \right) \quad (5.3.6)$$

Regarding power consumption, the value was obtained at a frequency of 10 MHz, which is the frequency at which the comparator shall operate. To compute the power consumption, the tail currents were looked at, where a value of 7.25  $\mu\text{W}$  per comparison was obtained.

The metrics obtained for the comparator can be seen in Table 5.3.

<b>Metric</b>	<b>Double-tail</b>
Input-referred noise	129.76 $\mu\text{V}$
SNDR	73 dB
Delay	4.2 ns to 2.6 ns (mean corner)
Offset	2.10 mV
Power consumption	7.25 $\mu\text{W}$ /comparison

Table 5.3: Metrics obtained for the double-tail latch.

# Chapter 6

## ADC Logic

The logic of the ADC is in charge of providing the digital signals to set the DAC output to one voltage or another depending on the comparator output. When considering what logic to use for an ADC, two main routes were explored, synchronous and asynchronous. However, for both, the general idea is the same; after the sampling phase, a train of pulses must be generated to trigger a comparison. Each pulse will set the bit to one or zero, depending on the comparator's decision.

Generally, most designs take  $N+1$  or  $N+2$  cycles to complete the cycle, leaving one for the sampling and the rest for the comparison process. This means that if a synchronous approach is pursued in higher speed designs, a clock with frequency values of hundreds of MHz or a few GHz must be provided, dissipating a lot of power consumption and making the jitter quite restrictive.

Even though the frequency of a synchronous clock should not be an issue when considering the sampling rate for the implemented ADC. The asynchronous approach was preferred due to the desire only to use one clock signal, as only the sample signal has to be provided to the design.

### 6.1 Asynchronous logic

The general idea for the logic is to carry a positive edge via a shift register which will then trigger the selected bit to '1' or '0'. Nevertheless, in an asynchronous design, other tasks, such as generating the reset signal for the comparator, have to be performed as well. The implementation in this thesis is an adaptation on the one proposed by [45].

In this design, the generation of the reset signal for the comparator is triggered by the circuit shown in Figure 6.1, while its waveform is shown in Figure 6.2. During the sampling state, signals *Valid*, *Start* and *EoC* are at logic value '0', while *Sample* and

*Reset* signals are at logic ‘1’. Thus, when the sampling period ends, and the *Sample* signal becomes a logic ‘0’, the *Reset* signal is pulled down, generating a comparison. After this first comparison, and almost simultaneously, the *Start* and *Valid* signals are pulled up, the first being triggered and kept to logic ‘1’ after the first successful comparison. The second is pulled up every time the comparator output evolves into one state. Once both are high, the reset cycle starts; the TDL block is the logic temporizer, which function is to enable the comparator, wait for the decision, and then reset it for a long time to ensure the DAC settling [45]. In this thesis case, it has already been seen that the comparator shall take around 6 ns to generate an output for the worst corners. While the *Reset* signal is a square wave with a set period of 100 ns, giving the logic and the DAC at least 94 ns to settle before a new comparison is performed. The temporizer cycle occurs for every comparison until all the bits have been determined. Afterward, the End-of-Conversion (EoC) will be pulled up, indicating that the conversion has been finalized.

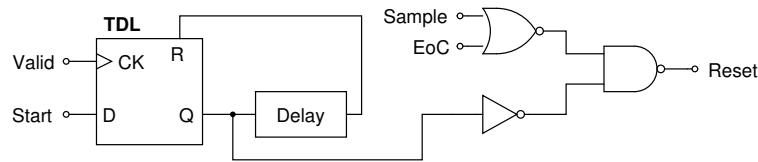


Figure 6.1: Generation of the reset signal for the comparator [45].

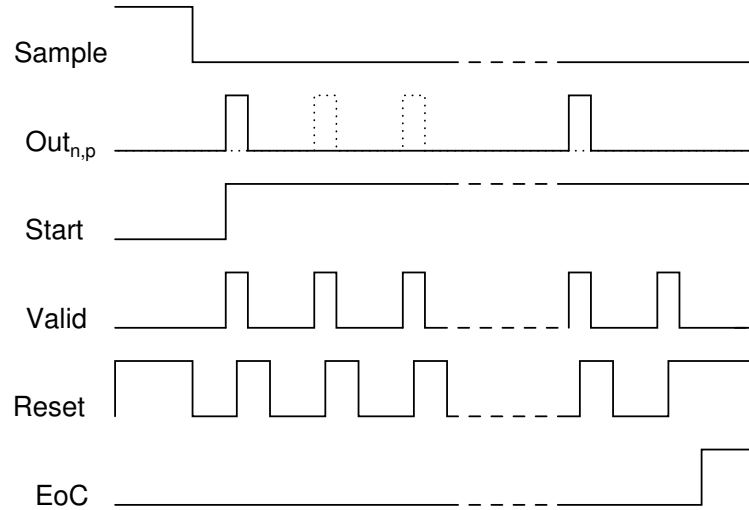


Figure 6.2: Simplified waveform of the asynchronous logic implementation [45].

Once it is clear how to obtain a new comparison from the reset generation circuit, the overall logic circuit can be looked at. As mentioned earlier, this will consist of a shift register stage that will generate a positive edge to initiate a bit determination stage that will change the value of the DAC depending on the comparison value. The block

diagram for both stages is shown in Figure 6.3.

For the shift register stage, D flip-flops were used. For these, the *Sample* signal was determined to be the used to reset them, while the *Valid* signal is the asynchronous clock; thus, every time there is a new comparison, the positive edge will move from one flip-flop to the next.

A row of Dynamic Differential Latch (DDL) was pursued for the bit determination part, being the output of the DFF the comparator's clock. While inactive, the output of the logic comparators will be at logic '1'; and depending on the result of said comparison, the output will be updated to '0' or '1'.

In this thesis case, the first shift register positive's edge and the first logic comparator are used to set the DAC to the binary word 100..00 after sampling. After this transition period, on the next pulse, the first "true" comparison is performed. Thus, completing the comparison in  $N + 1$  cycles without taking into account the sampling phase.

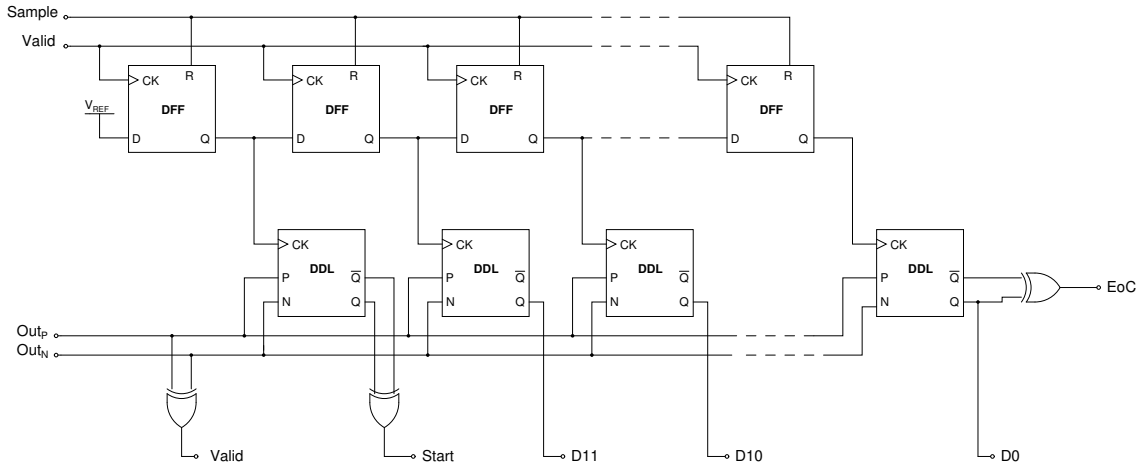


Figure 6.3: Simplified diagram of the logic implementation [45].

## 6.2 Implementation

Starting with the temporizer, the block responsible for the reset generation cycle, it was implemented using a dynamic latch with a feedback loop. The transistor-level diagram can be seen in Figure 6.4a. For the dimensions, all NMOS were sized with a width of 220 nm and a length of 180 nm. While to maintain similar rise and fall times, all PMOS transistors were sized around three times larger at a width of 680 nm and a length of 180 nm.

The transistor-level diagram of the D flip-flop is shown in Figure 6.4b, this block was implemented following a  $C^2MOS$  structure and an asynchronous reset. The NMOS transistors were sized with a width of 220 nm and a length of 180 nm. While the PMOS transistors were sized with a width of 680 nm and a length of 180 nm.

The DDL block is shown in Figure 6.4c. Note that this latch does not require any analysis in terms of offset or noise, as it will have to compare two signals already coming out of the comparator, so one will have a value of 1.8 V and the other of 0 V, making the comparison decision extremely easy. As in the previous cases, the NMOS transistors of the latch were sized at a width of 220 nm and a length of 180 nm. While the PMOS were sized with a width of 680 nm and a length of 180 nm.

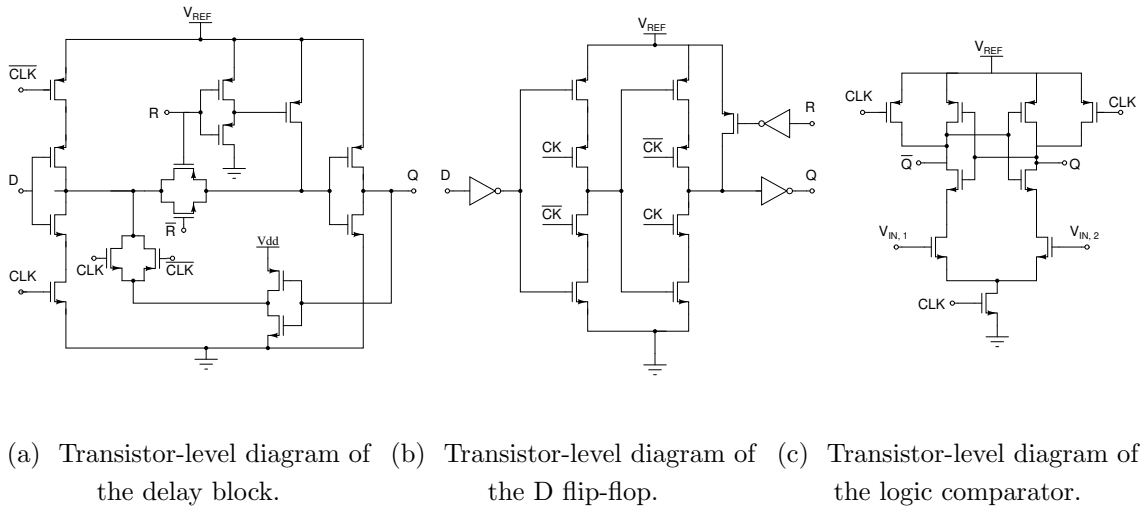


Figure 6.4: Transistor-level diagrams of the blocks of the logic design [45].

Next, note that before each DDL is activated, the output will always be at logic ‘1’, evolving into the desired final state after its corresponding clock cycle. However, it is not desirable in the case of the implemented switching algorithm. Take a possible DAC third cycle, where the word introduced should be ‘0010..00’. Instead, all the logic comparators that have yet to determine a value will have a logic ‘1’ at the output. Thus, XOR gates were introduced to set a logic value of ‘0’ for the logic comparators that have yet to determine their bit.

The only block remaining is the delay line, which will determine the speed of the overall ADC. As already mentioned, in this ADC case, the delay line has to delay the signal around 50 ns in order to generate a period for the *Reset* signal of around 100 ns. Note that this clock was sized faster than it would generally be required. This was mainly to account for process variation and to fulfill even the slowest corners of the design. For the generation of the delay itself, an inverter chain was used; which, while a robust solution, lacks the tunability and power efficiency of other designs.

### 6.3 Performance

First, a simulation of how the control signals are generated can be seen in Figure 6.5, where after the sample signal goes down, there is a first comparison which triggers the *Start* and *Valid* signals and sets both DAC arrays to half point for the first comparison. Then, after this first transition period, the comparator is reset again, being this first comparison used to obtain the first bit. After the fixed delay of around 100 ns, the comparator is reset again, giving a new comparison and receiving the second bit. This procedure continues until all the bits are determined and the EoC signal is pulled up, ending the cycle until the next *Sample* pulse arrives. Thus, it can be seen that in our case, the conversion takes  $N+1$  cycles (without considering the sampling itself) as the first cycle is used to set the DAC for the first cycle.

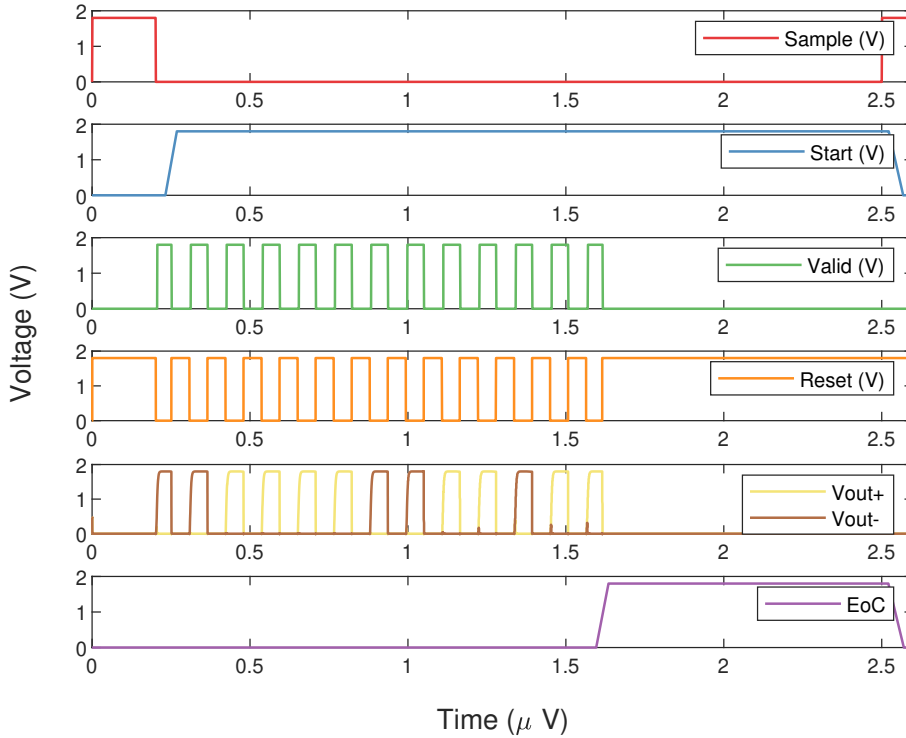


Figure 6.5: Waveform of the asynchronous implementation.

Once it was clear that the reset generation was performed correctly, the output bits were tested as well. For this task, instead of simulating just with a test-bench, the previously designed blocks of the ADC were introduced, as the voltages at the top plates of the DAC are closely related to the output bits. The waveforms obtained are shown in Figure 6.6 and Figure 6.7. From the first one, it is clear that the top plates of the DAC follow the switching procedure introduced, gradually converging to the common-mode voltage established, and obtaining a successful conversion. Moreover,



there is a zoom-in also presenting some of the LSBs. The second refers to how the output bits evolve for the waveform shown in Figure 6.6. There it is clear how each bit is set to logic ‘1’ before the comparison, and once it is obtained, the corresponding bit is maintained at ‘1’, like bits 11 or 6, or it is pulled down to ‘0’ like bits 10 or 9. With this simulation, it can be seen that the transient working procedure has been verified. As all of the individual blocks correctly perform their function when joined.

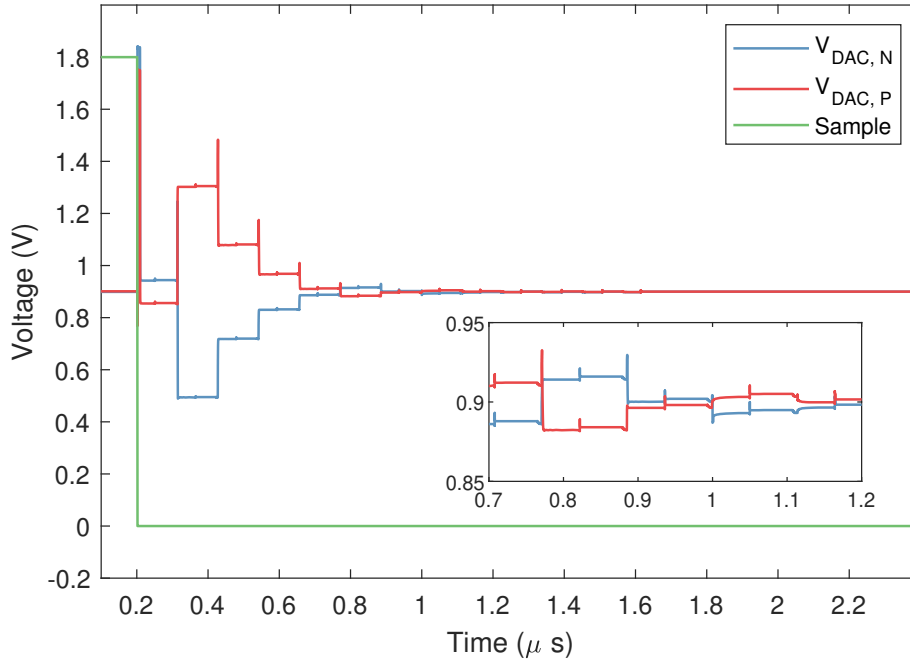


Figure 6.6: Waveform of the DAC top plates, exemplifying the switching algorithm employed.

The power consumption of the digital logic was simulated during one complete cycle, and the value obtained was  $119.74 \mu\text{W}$ . From the said simulation, it was noted that the generation of the delay was the most power-consuming block of the logic system.

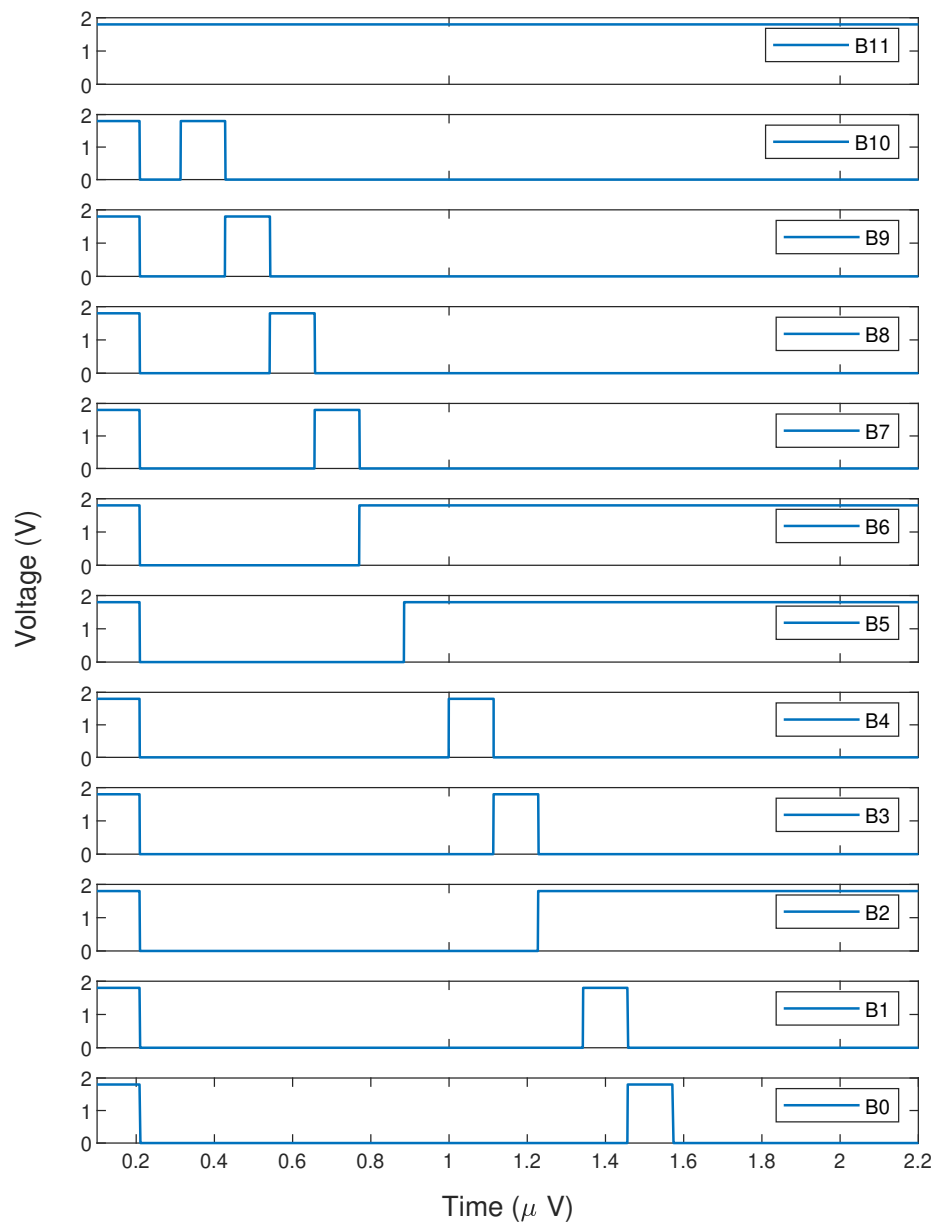


Figure 6.7: Waveform of the output bits for the conversion depicted in Figure 6.6.

# Chapter 7

## Verification

In this chapter the performance metrics and robustness of the complete ADC are assessed. Note that the transient working procedure was already verified in the last chapter, and it was seen that when merged together all the individual blocks performed correctly.

To obtain the dynamic metrics of the system, the FFT was computed using an ideal DAC introduced in the ADC output, converting the binary code back to the analog domain, exemplified in Figure 7.1.

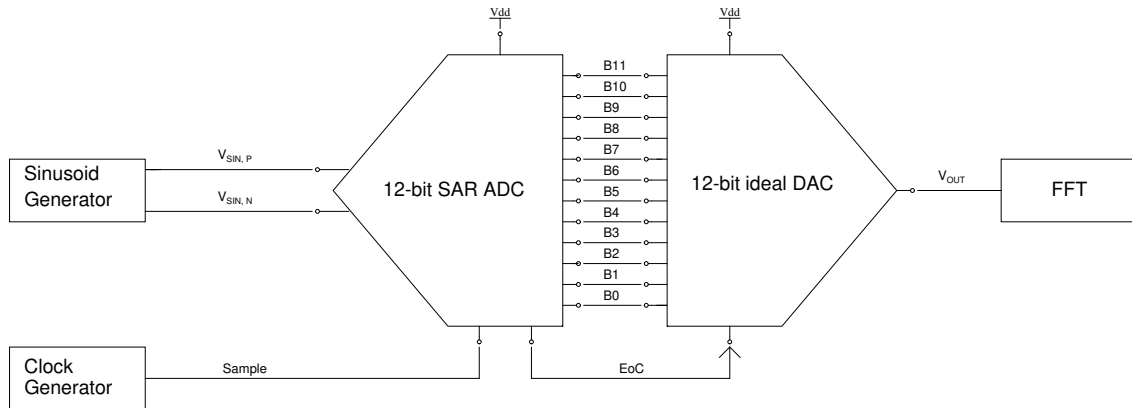


Figure 7.1: Block diagram of the measurement setup used.

### 7.1 Schematic of the design

The simplified schematic of the complete application employed for testing can be seen in Figure 7.2.

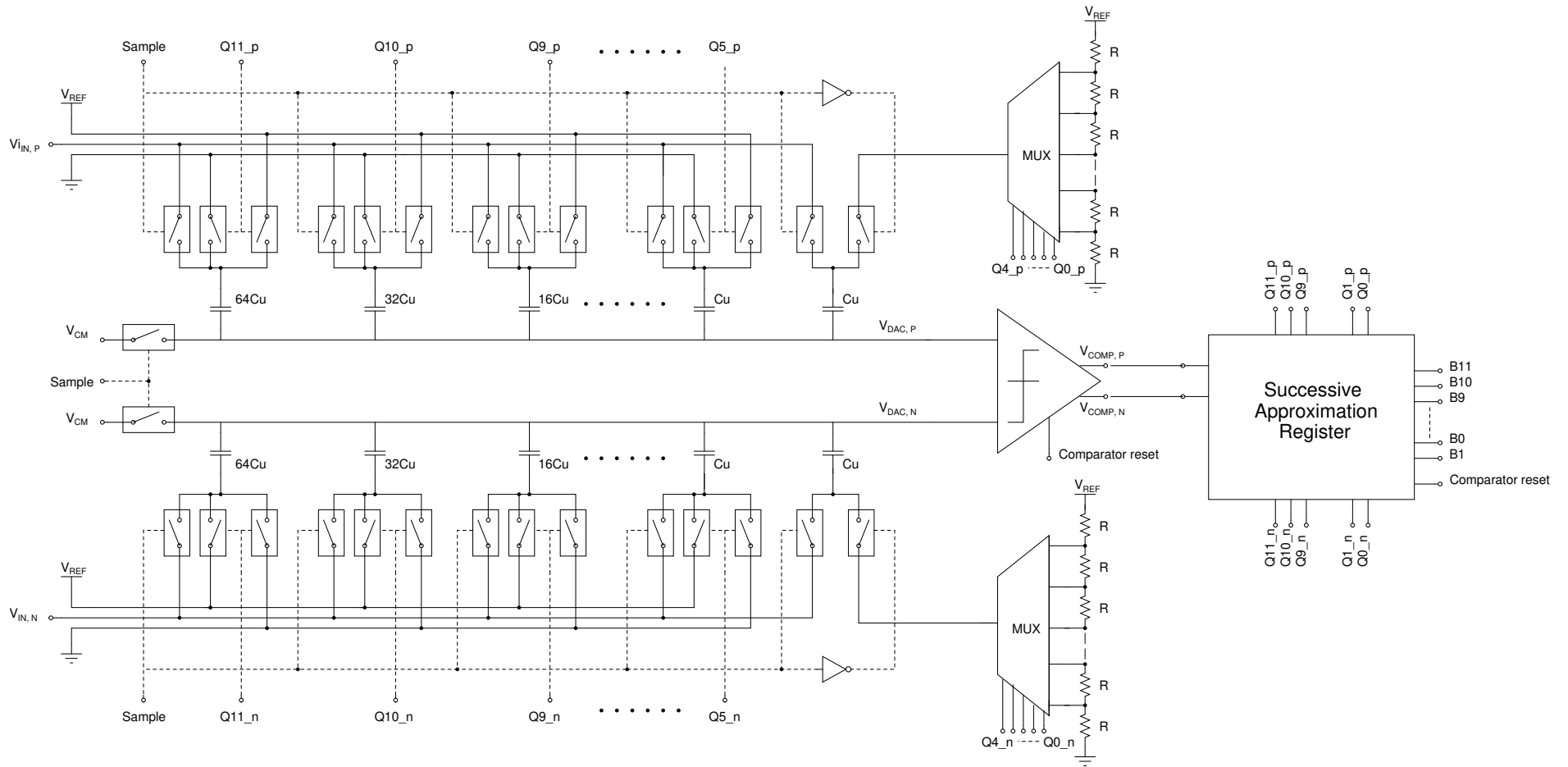


Figure 7.2: Simplified schematic of the 12-bit SAR ADC.

## 7.2 Transient noise simulation

The dynamic metrics of the ADC were verified utilizing a transient noise simulation, with a noise frequency bandwidth up to 500 MHz. Figure 7.3 shows the simulated output spectrum with an FFT of 2048 points for input frequencies of 45 kHz and 200 kHz. The achieved SNR in both waveforms is around 72 dB, translating to an ENOB of around 11.7 bits.

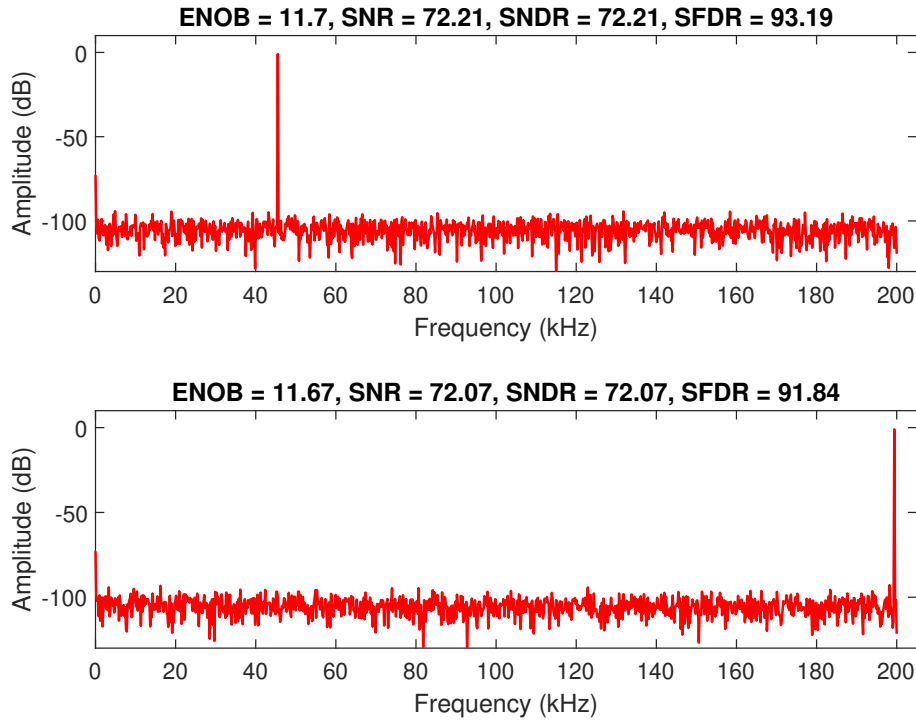


Figure 7.3: FFT of the SAR ADC obtained with a transient noise simulation.

## 7.3 Monte Carlo simulation

A Monte Carlo analysis with 200 samples was performed to assess the variations due to process mismatch. The resulting distribution is shown in Figure 7.4, in which it can be seen that there exists degradation when mismatch is introduced. Nevertheless, the mean value obtained of SNDR is 71.84 dB while the standard deviation is 1.30 dB. Anyhow, except for two outlying values, the obtained SNDR is always larger than 69 dB. The results obtained from the simulation provide with the understanding that the system should be robust against mismatch variations.

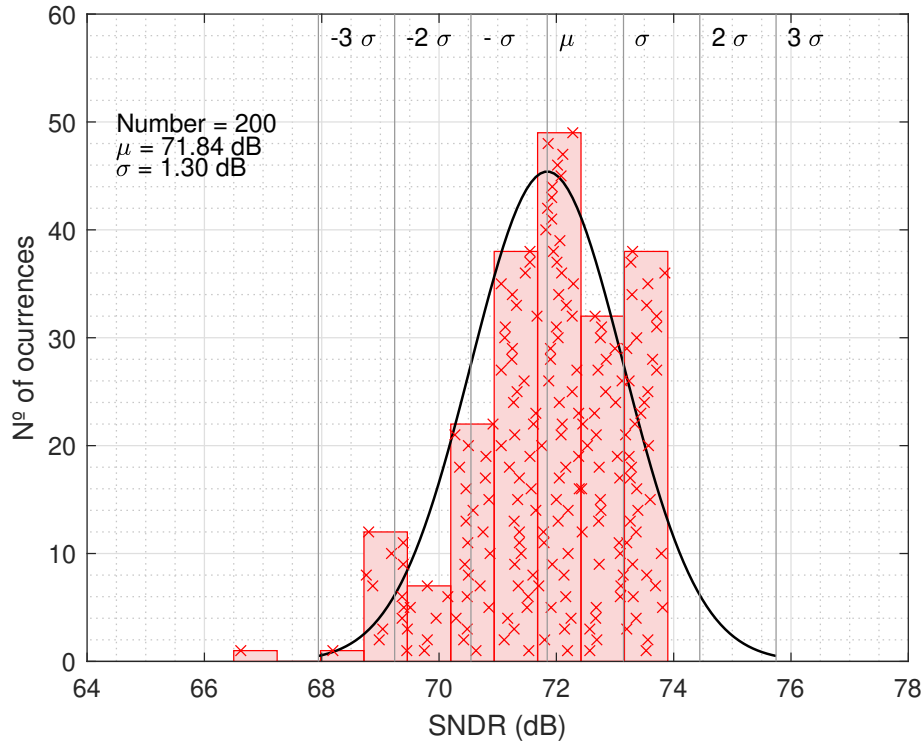


Figure 7.4: Monte Carlo simulation of the SNDR of the SAR ADC.

## 7.4 Robustness

To further examine the ADC and determine where its performance limitations lie, it was not enough to test for mismatch or noise simulations, as other variations also required to be checked.

### 7.4.1 Process corners

This simulation tested power supply and temperature variations alongside the corners of the system. Thus, for each of the four process corners, the supply voltage and temperature were swept from 1.62 V and 1.98 V and  $-40^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ , respectively. Obtaining a total of 25 points for each corner.

From Figure 7.5, it can be seen that when it comes to the worst one (wo), zero (wz), and worst power (wp), the corner performance remains relatively unaffected, always obtaining values larger than 71 dB. However, one main drop-off in performance can be seen for the worst speed corner (ws) at the lowest temperature values, in which the system becomes so slow that it does not give enough time to the converter to determine all the bits within the specified time. Nevertheless, even in that corner, the performance obtained is always above 60 dB or 9.6 ENOB. Regarding the overall performance after the corner analysis, it can be said that 90% of the tests obtain better

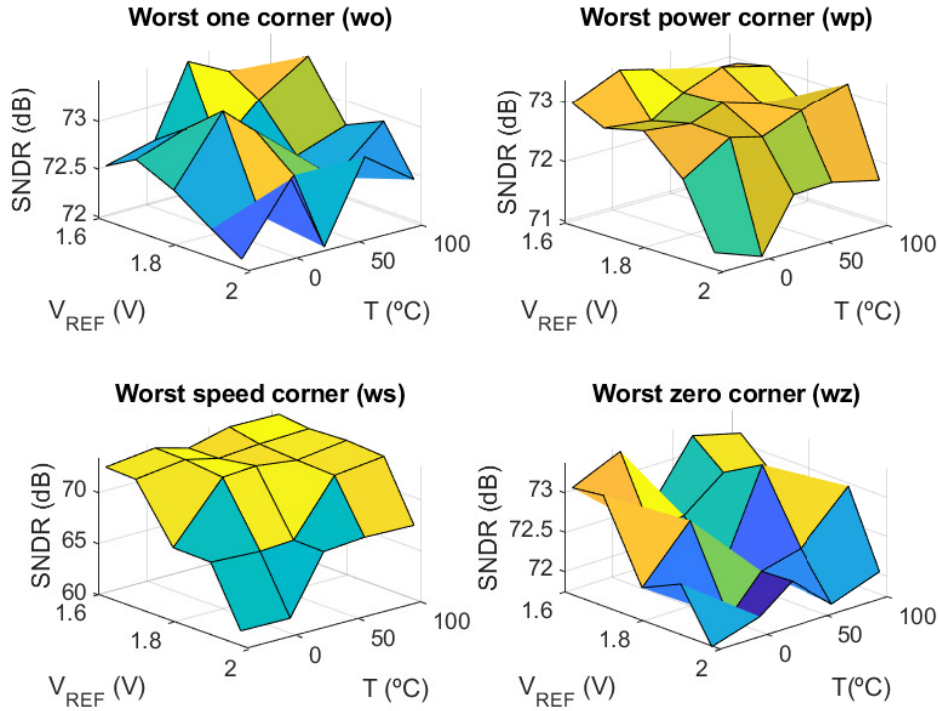


Figure 7.5: Surface plot of the SNDR for each of the four process corners.

SNDR values than 71 dB or 11 ENOB. While 98% of the corners obtain better SNDR values than 62 dB or 10 ENOB. Being the remaining 2% above 60 dB.

### 7.4.2 Common-mode voltage variations

Apart from temperature and supply variations, it can be helpful to assess the system's performance when the common-mode changes. Modifying the common-mode voltage of the ADC means that, for example, if the common-mode voltage is set to 0.8 V, the system will converge to 1.0 V, being that the end-value of the top-plates of the DAC.

For this test, the common-mode voltage was swept from 0.75 V to 1.05 V, and the results obtained can be seen in Table 7.1, in which it is clear that the ADC is robust except when it comes to variations out of the ordinary, as illustrated for the common-mode value of 0.75 V.

## 7.5 Input signal variations

In practice, the SNDR can also be used to obtain the Dynamic-Range (DR), which can be defined as the range from full-scale voltage to the smallest detectable signal [8]. The DR of the design can be seen in the top graphic of Figure 7.6 and is equal to

$V_{cm}$ (V)	$SNDR$ (dB)
0.75 V	69.70 dB
0.8 V	71.98 dB
0.85 V	72.03 dB
0.9 V	72.07 dB
0.95 V	71.98 dB
1.0 V	72.01 dB
1.05 V	71.93 dB

Table 7.1: SNDR in function of the common-mode voltage.

approximately 72 dB. Likewise, it can be interesting to perform a sweep in input frequency values to obtain the Effective Resolution Bandwidth (ERB), which is the maximum signal bandwidth that can be handled and should be well above the Nyquist frequency. This metric can be obtained when the SNDR drops 3 dB, and in this converter case, that occurs at around 1.1 MHz, as exemplified in the bottom graph of Figure 7.6.

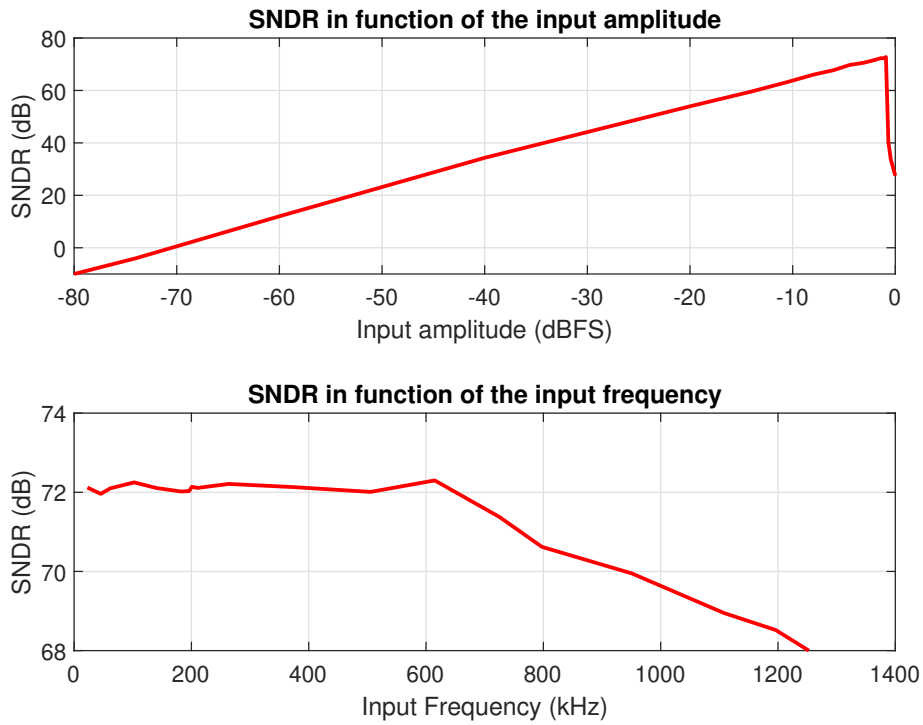


Figure 7.6: SNDR in function of input amplitude and frequency.



## 7.6 Stress variations

The ADC proposed is targeted for a tactile sensing application; consequently, the circuit will undergo some amount of stress. Thus, it was a must to test the system against multiple directions and magnitudes of stress. The main target of this test was the worst overall stress element, the resistor. And while it was already chosen to be of poly-silicon due to the said type being less dependent on stress variations, it is still essential to assess its robustness. The resistor is the key element in the R-DAC, and significant variations in the voltage divider could translate to an increase in the overall DNL and INL of the system.

Nevertheless, one should note that the resistors are placed in a string configuration, meaning that as long as they are all laid out with the same reference and crystalline directions, all should suffer similar stress distortions. Consequently, inducing a minimal change in the voltage division they produce, only causing an effect in the current through the string. This is verified in Figure 7.7, where for different stress magnitudes and directions, the variation of the current across the DAC is observed. But, it should be noted that the value obtained is always in between  $31 \mu\text{A}$  and  $32 \mu\text{A}$ , meaning that the introduced distortion due to stress should be insignificant.

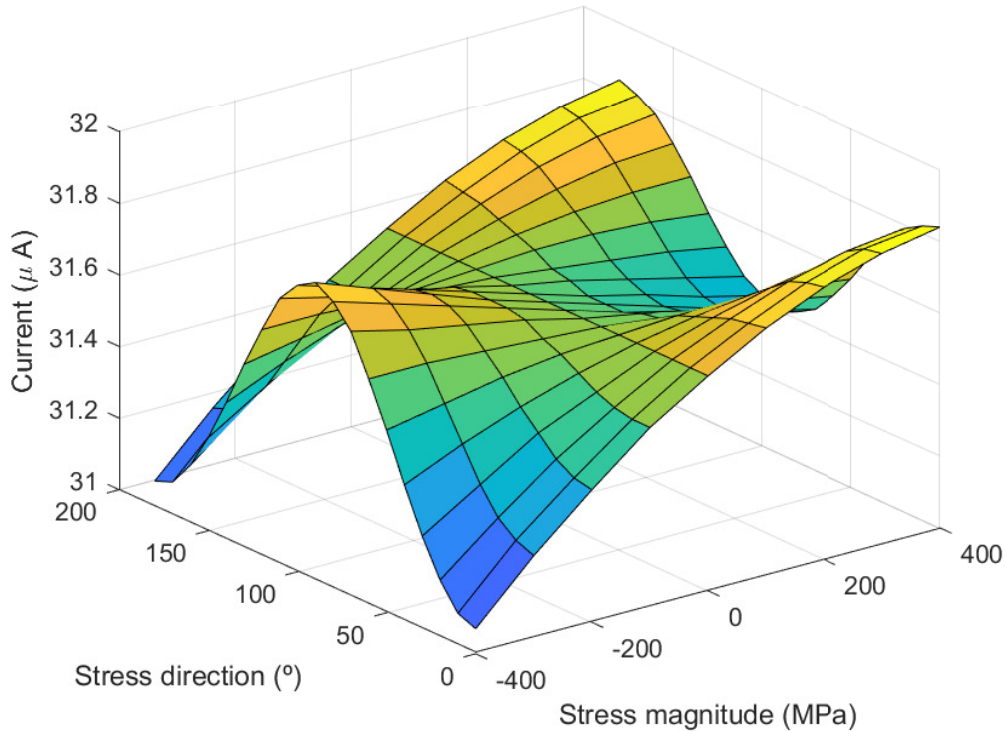


Figure 7.7: Current through the resistor string depending on the magnitude and direction of the stress.

This change in current does not hinder the performance of the DAC nor the ADC, always maintaining a constant SNDR of both across the applied magnitudes and directions. Additionally, the stress dependence of the DAC was tested via a Monte Carlo simulation across multiple stress directions and magnitudes. From those simulations, it was verified that the stress variations applied did not induce significant changes in the DAC, obtaining DNL and INL variations in the maximum and minimum values of less than 0.02 LSB in all tested cases. Thus, it could be said that the stress robustness of the system is satisfactory and should not affect the overall performance.

## 7.7 Power consumption

The design's power consumption was already briefly discussed in the implementation of each block. In summary, the total power consumption and final values for each of the four main blocks are shown in Table 7.2. From the obtained values, it is quite interesting to see the power consumption obtained by the logic, which in this thesis case, around 75% of it is caused by the delay line.

Sub-block	Power consumption
DAC	150.44 $\mu\text{W}$
Comparator	94.25 $\mu\text{W}$
Switches	1.12 $\mu\text{W}$
Digital logic	119.74 $\mu\text{W}$
<b>Total</b>	365.55 $\mu\text{W}$

Table 7.2: Power consumption of the SAR ADC.

## 7.8 Circuit area

After the verification of each of the blocks and the total ADC, the layout of the whole circuit can be done. The entire area obtained is of 0.50 mm<sup>2</sup>. A word of caution here with the area of the DAC, in which by the time of this report was finished, the layout of this block was not completed; thus, it is only an estimation. This also applies to the total area of the layout.

## 7.9 Comparison with state-of-the-art ADC

Once all the simulations and the power and area have been obtained, it can be interesting to compare the proposed ADC to other designs via a Figure-of-Merit (FoM). There are two main ones, the Walden and the Schreier (Equations 7.9.1 and 7.9.2).

Sub-block	Area
DAC	0.20 mm <sup>2</sup> *
Comparator	0.9 x 10 <sup>-3</sup> mm <sup>2</sup>
Switches	0.02 mm <sup>2</sup>
Digital logic	0.20 mm <sup>2</sup>
<b>Total</b>	0.50 mm <sup>2</sup> *

Table 7.3: Area allocation of the SAR ADC.

$$FOM_{Walden} = \frac{Power}{f_s \times 2^{ENOB}} \left[ \frac{J}{conversion} \right] \quad (7.9.1)$$

$$FOM_{Schreier} = SNDR + 10 \log \frac{f_s}{2 \times Power} [dB] \quad (7.9.2)$$

The results obtained for both metrics are 275 fJ/conversion and 160 dB, respectively.

The simulated performance of the ADC is summarized and compared to other similar SAR ADC designed in recent years, Table 7.4. In the introduced table, it is clear that the design is in line with recent ADC designed with similar technologies. Nevertheless, it is obvious that other ADC proposals obtain much better FoM results, mainly due to their low power consumption. However, it should also be mentioned that most designs use smaller technologies and power supplies, which can help achieving better FoM results.

Metric	Muratore [27]	Shen [46]	Hung [47]	Yang [48]	This work
Architecture	SAR	SAR	SAR	SAR	SAR
Technology	65 nm	40 nm	180 nm	65 nm	180 nm
Year	2017	2018	2021	2022	2022
Resolution (bits)	12	12	12	10	12
Sampling rate (MS/s)	8	1	0.001	0.02	0.4
SNDR (dB)	69	66	57.7	60.15	72.07
Power (μW)	200	31	0.204	5.32	365
Area (mm <sup>2</sup> )	0.04	0.073	0.05	-	0.6 *
$FOM_W$ (fJ/conv)	9.9	15	323	307.5	275
$FOM_S$ (dB)	172	168	151	153	160

Table 7.4: Comparison against other ADC.

## 7.10 Overall discussion

From the results obtained, it is clear that the converter designed obtains good performance values. Achieving resolutions upwards of 71 dB with transient noise simulations and a remarkable robustness to a number of disturbances.

Moreover, besides the parasitic extraction, most of the effects present in an actual circuit were included, such as thermal noise or process variations.

Regarding possible improvements for future iterations of the SAR ADC presented in this thesis. The first that should be mentioned is to decrease the overall power consumption. A couple of these upgrades could be targeted at the comparator and the delay generator. For the comparator, some trade-offs could be explored, such as trying to minimize the power consumption at the expense of the delay. The main power-consuming block for the logic is the delay generator, currently implemented via an inverter chain. Other possible designs could include a control voltage to adjust the delay, allowing the converter to operate at different sampling frequencies. Likewise, in this thesis, the selected switching algorithm was the conventional approach; however, in recent times, there have been multiple switching proposals to help improve the efficiency that could be pursued in future iterations [20].

As mentioned, the parasitic extraction could not be performed in this design due to not having the complete layout ready at the time of submission. Thus, the performance of the ADC with parasitic remains unknown. However, while some performance drop is expected, the SNDR and ENOB should remain above over 65 dB and 10.5 bits, respectively.

Metric	Result
Technology	180 nm
Resolution	12 bits
Sampling rate	400 kS/s
Supply voltage	1.8 V
SNDR	72.07 dB
ENOB	11.67 dB
Power	365 $\mu$ W
Area	0.5 mm <sup>2</sup>
$FOM_W$	275 fJ/conv
$FOM_S$	160 dB

Table 7.5: Final specifications of the designed ADC.

# Chapter 8

## Conclusions

A 12-bit 400 kSps Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) has been successfully designed and implemented. Pre-layout simulations show that the design consumes  $365\ \mu\text{W}$  while achieving SNDR values of 72.07 dB for a 200 MHz input frequency, which corresponds to an ENOB of 11.67 bits. The converter obtains values of 275 fJ/conversion and 160 dB in the Walden and Schreier figure-of-merit, which aligns with recent converters designed for similar technologies. Moreover, the robustness of the design was tested against multiple disturbances, remaining reliable across all the tests, and most notably against the stress disturbances that should be present in the application.

In this thesis, the hybrid R-C DAC proved a suitable alternative to the conventional binary-weighted array employed in most DAC, achieving excellent performance values with suitable layout area and power consumption. When it comes to the overall noise of the system, the comparator is the main contributor. About said block, its design allows obtaining satisfactory noise values across a wide range of temperatures. Less power consumption in the comparator could be allowed at the cost of permitting larger noise values.

The next step in this thesis should focus on improving the system's power consumption without decreasing the performance. These improvements should focus mainly on the comparator and the delay generator, which are some of the system's most power-consuming blocks. Likewise, the power consumption of the DAC could be reduced by introducing a new switching algorithm or by trying to optimize the power-delay trade-off.

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