Evaluation of Single Event Upset Susceptibility of FinFET-based SRAMs with Weak Resistive Defects

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Abstract

Fin Field-Effect Transistor (FinFET) technology enables the continuous downscaling of Integrated Circuits (ICs), using the Complementary Metal-Oxide Semiconductor (CMOS) technology in accordance with the More Moore domain. Despite demonstrating improvements on short channel effect and overcoming the growing leakage problem of planar CMOS technology, the continuity of feature size miniaturization tends to increase sensitivity to Single Event Upsets (SEUs) caused by ionizing particles, especially in blocks with higher transistor densities such as Static Random-Access Memories (SRAMs). Variation during the manufacturing process has introduced different types of defects that directly affect the SRAM's reliability, such as weak resistive defects. As some of these defects may cause dynamic faults, which require more than one consecutive operation to sensitize the fault at the logic level, traditional test approaches may fail to detect them, and test escapes may occur. These undetected faults, associated with weak resistive defects, may affect the FinFET-based SRAM reliability during its lifetime. In this context, this paper proposes to investigate the impact of ionizing particles on the reliability of FinFET-based SRAMs in the presence of weak resistive defects. Firstly, a TCAD model of a FinFET-based SRAM cell is proposed allowing the evaluation of the ionizing particle's impact. Then, SPICE simulations are performed considering the current pulse parameters obtained with TCAD. In this step, weak resistive defects are injected into the FinFET-based SRAM cell. Results show that weak defects can positively or negatively influence the cell reliability against SEUs caused by ionizing particles.

Keywords SRAMs · FinFET · Resistive defects · TCAD · SEU · Reliability · Single event transient modeling

1 Introduction

Fin Field-Effect Transistor (FinFET)-based Static Random-Access Memories (SRAMs) represent one of the current state-of-the-art technologies for integrated systems as they are designed with high density and produced at the limit of the fabrication process. Furthermore, as FinFET is a recent technology, there is a need to evaluate and model its behavior concerning defects and failures [1].

One major reliability issue in nanometer technologies is radiation-induced Single Event Effects (SEE), i.e., soft

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errors caused by ionizing particles [2]. In SRAM cells, a soft error may generate a bit-flip, called Single Event Upset (SEU). This faulty behavior occurs when an ionizing particle strikes a reverse-biased PN junction (usually an off-state transistor's drain) initially generating a transient current pulse in a given circuit node. If the affected transistor belongs to a cell's storage node, this transient current pulse may propagate through the feedback of the cross-coupled inverter, generating a bit-flip [3].

Another essential reliability issue in FinFET memory technology is related to weak resistive defects [1] caused by variability in the manufacturing process. These defects can be classified either as resistive-opens or resistive-bridge defects [4]. They can be classified as "weak" [5] if they are hard to detect, especially using traditional memory tests such as March tests [5]. Therefore, they may lead to test escapes, which might affect the FinFET device's susceptibility to single events due to ionizing particle strikes in the field, as discussed in this paper.

It is known from the literature that radiation can lead to soft errors in FinFETs even at ground level [2, 6]. Several works performed a comparative analysis regarding SEEs between FinFET and other technologies (conventional bulk CMOS and SOI) [2]. Also, in [2], an analysis of FinFET-based SRAMs at different altitude levels was performed. Analysis of weak resistive defects has already been carried out for both planar SRAM cells [4] and FinFET-based SRAM cells [7]. Further, an analysis of the radiation susceptibility of conventional CMOS SRAM cells in the presence of weak resistive defects is presented in [8]. Considering the previously published work, we propose to analyze the influence of weak resistive defects on the FinFET-based SRAM robustness under single event effects. Because the FinFET structure is physically more complex than the planar CMOS, a more precise and realistic simulation tool is necessary. Thus, a FinFET-based SRAM cell was modeled using a Technology Computer-Aided Design (TCAD) tool, and simulations of ionizing particle impacts were performed at the physical level. Further, the transient current generated by such an event was modeled at the electrical level.

Hence, the main contributions of this paper are: 1) obtain, by physical simulation, the minimum value of Linear Energy Transfer (LET) of an incident particle that results in a bit-flip (LET_{th}, or threshold LET) for FinFET SRAM cells designed in a technology equivalent to a 14 nm node; 2) propose a SPICE model for the obtained current curves; 3) investigate the impact of SEUs on the reliability of FinFET-based SRAMs with weak resistive defects. Note that the first step towards these goals was presented in [9]. Thus, this publication extends the explanations regarding the proposed simulation flow during experiments, improves the development of the transistor's electrical characteristics, and enhances the SRAM cell's analysis with respect to regions far from the critical node. The results obtained in this work may help researchers working on SRAM reliability by providing a feasible simulation flow and important insights of the possible impacts of test escapes, considering non-critical resistive defects, in SRAM field applications susceptible to ion strikes.

2 Background

FinFETs are composed of thin vertical slices of silicon (known as fins) that are wrapped by the gate structure and built on top of a silicon substrate [1]. These fins comprise the channel region of the transistor. Note that this work considers the bulk FinFET model, in which the fins are directly connected to the substrate, and the oxide is used to isolate each fin from the others.

A schematic view of a standard 6 T-SRAM cell is illustrated in Fig. 1. For sake of conciseness, this figure also shows the equivalent resistive defects and the transient current model (Q_{crit}) that will be described in Section III. This cell is composed of six transistors: two cross-coupled inverters (M_1 & M_2 and M_3 & M_4) that store the digital information in nodes Q and its counterpart $\overline{Q}$, and the other two nFET transistors acting as Pass Gates (PG) (M_5 and M_6), responsible for isolating the cell during hold phase, and open the cell during read and write operations. The Word Line (WL) signal controls the two PGs that are connected to the bit lines (BL and $\overline{BL}$) [4].

One of the main causes of test escapes in new technologies based on FinFETs is related to the presence of weak defects, which make the cell more prone to dynamic faults than conventional planar CMOS-based SRAM [1]. Weak resistive defects are defects with resistive characteristics that cause small device's electrical parameter deviations [10]. In SRAM cells, such defects can generate dynamic faults, which require more than one consecutive read operations to propagate a fault at logic level [10–12]. A resistive-open is modeled as a resistor between two nodes that share a connection, and a resistive-bridge is modeled as a resistor between two nodes that not should be connected [4], as illustrated in Fig. 1.

The memory testing methodology for the detection of dynamic faults, used for FinFET and CMOS, caused by resistive defects can be done by performing n consecutive read operations (stress condition) [13]. The number of consecutive operations is related to the defect size, which means that weak defects could require a prohibitive number of consecutive read operations during manufacturing testing. Thus, when considering FinFET technology, the presence of weak defects and the fact that they did not necessarily propagate any fault at the logic level, causing an electrical deviation only, is considered a great source

Fig. 1 FinFET-based SRAM cell with injected defects and transient current
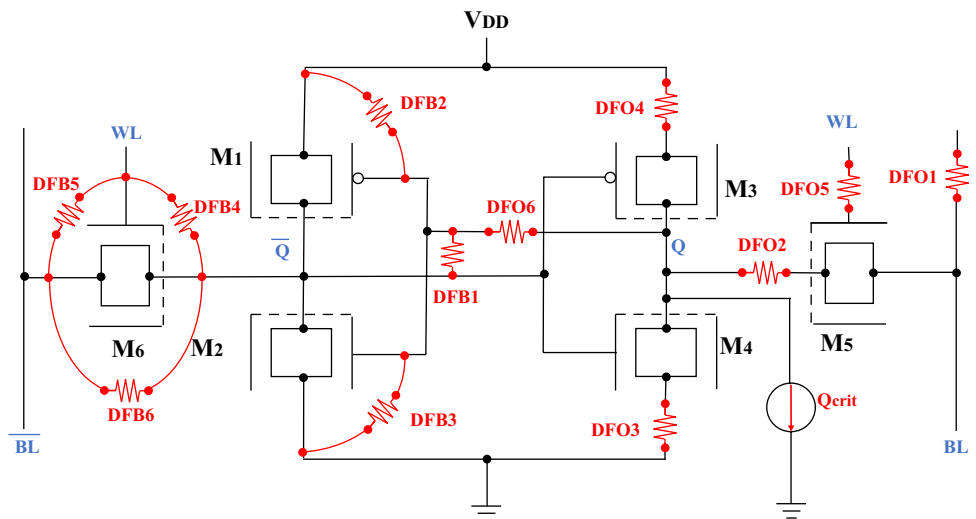
of test scape [1]. In this context, a memory including cells with very weak defects can be classified as fault-free. However, the presence of these very weak defects can exacerbate the memory susceptibility to SEUs, justifying the proposed methodology and analysis.

In [14], a comparison of SEEs between a 16 nm bulk FinFET and a 28 nm bulk planar technology was carried out. This study shows that low-LET particles may cause transients in FinFETs when hitting the fin region. Therefore, FinFET technology has a very strong dependence on the ion strike location, unlike planar CMOS, which demonstrates less dependence on the position of impact. The same study reported that a strike between two fins produces a very small transient voltage. This effect happens in FinFETs due to their low charge collection efficiency, which means that a small fraction of the generated electron–hole pairs is collected at the FinFET drain during the silicon ionization, resulting in lower current pulses [2].

However, with the proximity of connections and the reduced supply voltage, FinFET-based SRAMs are becoming more susceptible to SEUs, even at ground level [6]. Traditionally, the major sources of radiation-induced soft errors at ground level or flight altitudes are: (1) alpha particles originated by the radioactive contamination existing in the packaging [15, 16]; (2) the high-energy neutrons from cosmic radiation (generating secondary reactions); and (3) the interaction of cosmic ray thermal neutrons with devices containing borophosphosilicate glass [16]. The work presented in [2] has shown that for SRAMs, protons, and muons are also among the particles able to generate SEUs at ground level in bulk FinFET technologies.

The work presented in [17] describes an empiric experiment of two 128 Mb FinFET-based SRAMs using two different configurations: High-Density (HD), and High Performance (HP), both being exposed to alpha particles, thermal neutrons, and high energy neutrons. The experiments show that the HP cell is more sensitive than the HD cell due to its advanced geometric isolation from the substrate. It is interesting to note, that the method used for computing the critical charge differs from the method used in this work. In [17] the critical charge is obtained from the equation given in [18], resulting in a higher critical charge for HP when compared to HD cells. However, as is described throughout this paper, it has to be assumed that the critical charge's definition is not so trivial.

3 Methodology

In order to evaluate the transient effects caused by ion strikes, a layout of a 14 nm FinFET-based SRAM cell was designed and modeled in Sentaurus™ TCAD tool. This technology node was chosen due to its current use by memory manufacturing companies. This section also describes the methodology carried out to simulate ionizing particle strikes at the physical level as well as the SPICE modeling of resistive defects.

3.1 Modeling a FinFET-SRAM Cell in TCAD

To study the effects of SEUs, an initial FinFET SRAM 3D model was developed using Sentaurus™ TCAD. In comparison to SPICE simulations, this tool allows larger flexibility while controlling the device physics aspects, including the impact location of ionizing particles and its associated LET. This study considers three models of FinFET-based SRAM cells: High-Density (HD), High Performance (HP), and Low Voltage (LV). Because of the discrete nature of fins, it is not possible to tune the transistor parameters to obtain an ideal robustness/area ratio as it would be feasible in planar
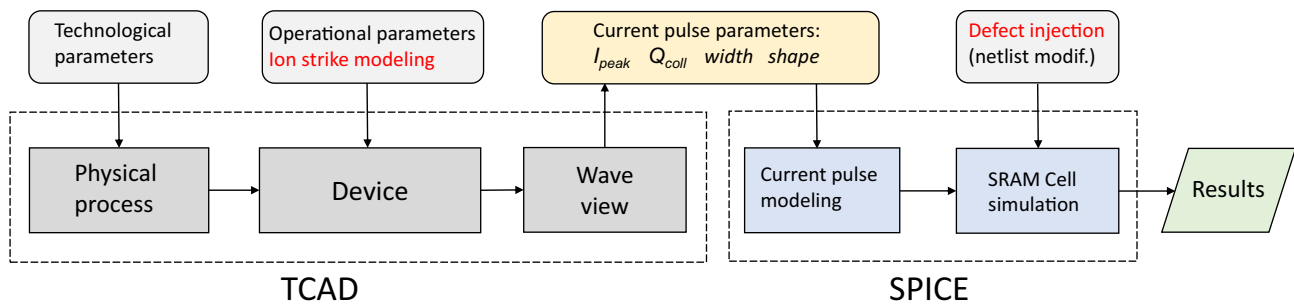
Fig. 2 Adopted simulation flow

CMOS. Therefore, each model has its configuration with a different distribution of fins in the cell's transistors. The SRAM cell structure is divided into three parts with their proper notation (PU:PG:PD), meaning respectively: Pull Up, Pass Gate and Pull Down [18]. As an example, the HD configuration adopts a (1:1:1) configuration, meaning that all the cell transistors are composed of a single fin.

Figure 2 shows the simulation flow adopted in the Synopsys Sentaurus™ environment [20]. Firstly, the physical process of cells was developed, using the Sentaurus™ Process (S_Process) tool. The transistors designed with the Sentaurus™ tool were calibrated using the physical characteristics described by the 2015 International Technology Roadmap for Semiconductors (ITRS) [21], summarized in Table 1. The mesh grid configured in these simulations was generated given special attention to the active zones such as channel, source, and drain.

Using the Sentaurus Device (S_Device), the operational parameters of the circuit are implemented, allowing its validation. The curve of Static Noise Margin (SNM) was also collected at this stage in order to properly evaluate the reliability of the circuit with respect to noise fluctuations. After these steps, the injected ionizing particle is modeled, using the same tool. The tool Sentaurus Visual (S_Visual) was used to analyze the electrical behavior, by wave verification. Finally, the Inspect tool was used to verify the transient operations while simulating the ion impact.

Table 1 Adopted Physical Parameters for FinFETs

Physical Parameters	Values [nm]
Physical Gate Length	26
Fin Width	8
Fin Height	42
Fin Pitch	42
Poly Pitch	90
Effective Width	92
Metal Pitch	56

3.2 Modeling Ion Strike

The heavy-ion injection in TCAD simulation follows the methodology presented in [14], considering a Gaussian charge distribution with a track radius of 10 nm. To model the worst-case scenario of such particle strike, the charge track length should be longer than the fin height, with normal incidence over the drain of the sensitive transistor (off-state transistor). The sensitive transistor is the pull-down transistor when the node (inverter output) is charged with a logic '1', or the pull-up transistor when the node is '0'.

In the simulation setup, the input parameters for heavy ions are given in charge per track length (pC/µm). To convert this value into the LET parameter the relation of 1 pC/µm is equivalent to a 97 MeV-cm^2/mg LET in silicon [15]. For example, the alpha particles due to radioactive contamination in the packaging material can result in 0.015 pC/µm, which approximates 1.5 MeV-cm^2/mg [15]. This analysis aims to find the threshold LET that causes a bit-flip in the cell. Considering this LET, the drain current in the affected transistor is evaluated, obtaining important parameters, such as the collected charge (Q_{coll}), current peak (I_{peak}), pulse width, and general shape, which is then compared with the traditional double exponential. The obtained current shape is modeled in SPICE to allow transient injections and resistive defect modeling at the same time. This analysis is carried out in SPICE since TCAD simulations would demand a huge computational effort. The overall simulation flow, including the resistive defects modeling in SPICE, is depicted in Fig. 2.

3.3 Injecting Resistive Defects

The electrical simulations to evaluate the robustness of a FinFET-based SRAM cell in the presence of weak defects are performed using Hspice™ from Synopsys. The Fin-FET-based SRAM was designed using the Arizona State University's 14 nm FinFET Predictive Technology Model

Table 2 Number of fins and area considering different SRAM cells

Configuration	(PU:PG:PD)	Area (um^2)
HD	(1:1:1)	0.0558
LV	(1:1:2)	0.07092
HP	(1:2:2)	0.07092

(PTM) [22]. For this purpose, the injected charge to simulate single events in SPICE is set with a value lower than the excess charge observed when simulating a particle strike with LET = LET$_{th}$, while simultaneously injecting resistive defects. In this case, the defect resistance values are varied using an automated tool that interacts with the SPICE simulator. Note that the critical resistance (R$_{crit}$) is the defect resistance threshold that results in a bit-flip when injecting the ionizing particle. The methodology for resistive defects injection, according to the model shown in Fig. 1, is the same used in [7] and [22]. This effort is necessary to observe if resistive defects may change the cell's robustness to SEUs. The opposite situation was also verified, simulating an event depositing the critical charge (Q$_{crit}$) at the same time that resistive defects are injected, in order to determine if SEEs are attenuated due to the presence of a given defect.

4 Results and Discussion

This section presents the results divided into three subsections: A) the FinFET-based SRAM cell model and validate using TCAD; B) TCAD-based SEE injection results and comparison with SPICE injections; C) the influence of resistive defects on cell reliability when considering single events.

4.1 SRAM Cell Modeling and Validation

As previously mentioned, a FinFET-based SRAM cell was implemented based on the physical parameters described on the 2015 ITRS [21], and as presented in [19]. Three different models were adopted, whose configurations (number of fins of the transistors), along with the corresponding area, are shown in Table 2. As an example, Fig. 3 shows an LV SRAM cell modeled in 3D-TCAD. Different from this exemplary cell, the HD configuration, the most compact, would not possess a fin column on each side of the cell, and the HP configuration would show two fins in the PG. To reproduce industrial devices, only HD and LV cells use source and drain regions with a polyhedron of silicon over the fin [19]. Note that these structures do not cause a considerable current variation in the transistor when compared with the HP cell. Electrically, the LV model has a more robust SNM for a read operation, and the HP model is faster during reading and writing operations [19].

To validate the device's electrical operation is compatible with the 14 nm node used as target technology, the electrical behavior was compared to the drain current/gate voltage data from the Arizona State University's Predictive Technology Model (PTM) [22]. To observe the *Id* x *Vg* behavior, Fig. 4 presents the drain current (*Id*) comparison, for both *p* and *n* FinFETs considering two drain voltages, 0.05 V and 0.8 V. Table 3 shows the *off* and saturation currents (I$_{off}$ and I$_{sat}$), as well as the percentage difference between the PTM model and the TCAD modeled device for each reported parameter. The I$_{off}$ is obtained with 0.8 V as drain voltage and the I$_{sat}$ with the highest possible voltage value. The normalized currents are the currents divided by the fin pitch in μm, thereby 0.042 for the developed transistor and 0.023 for PTM. Note that the difference between them is calculated using normalized values. Despite observing a significant difference between the saturation currents, the PTM model was used as a behavioral reference model only. The physical parameters of the PTM model are different from the parameters used in the TCAD model, consequently, the behavior is not expected to be exactly the same.

Table 4 summarizes the hold, read and write SNM values for the three different FinFET-SRAM cells developed using TCAD as well as for the circuit modeled according to PTM parameters in SPICE. Comparing the data, it is verified that
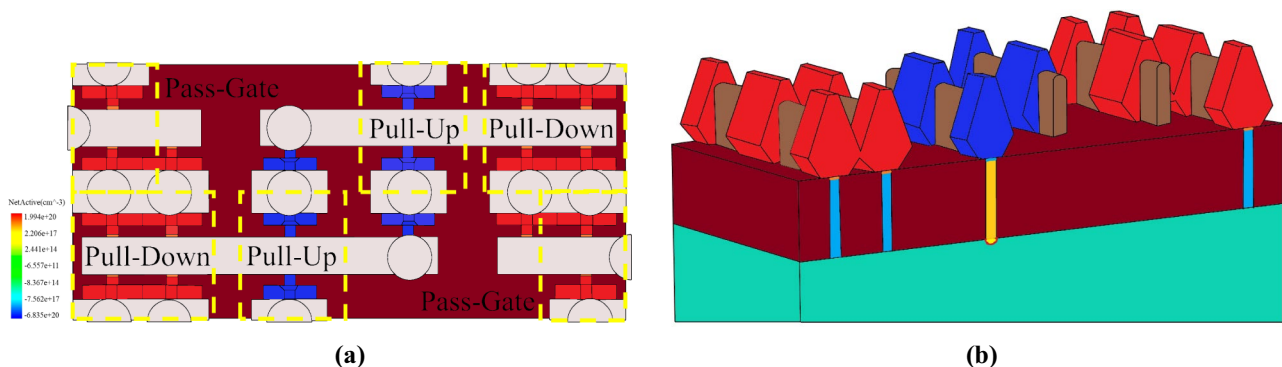

Fig. 3 FinFET LV SRAM cell implemented in this work: (**a**) top view; (**b**) 3D view without gate and metals
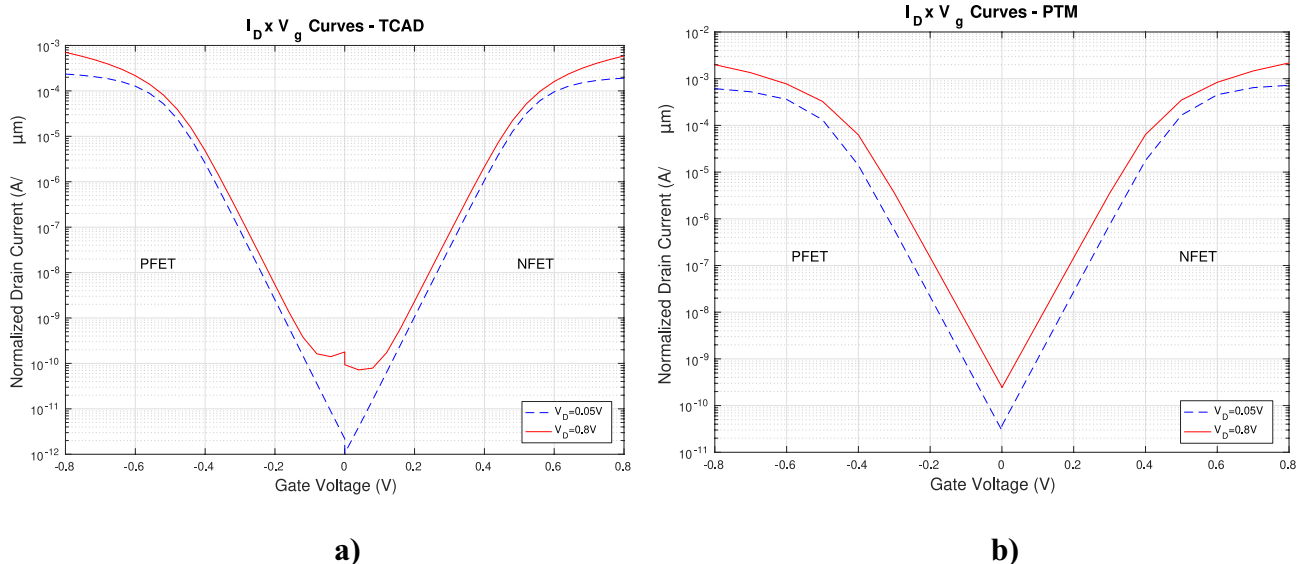
Fig. 4 Drain Current vs Gate Voltage for the transistors modeled in: a) TCAD, with physical parameter x b) SPICE, with PTM

the behavior of the circuit modeled in the TCAD simulator is correct, being even more robust than the PTM version. Finally, Fig. 5 shows the hold SNM butterfly curve of the FinFET-SRAM cell modeled using TCAD.

4.2 Simulating Single Event Transient using TCAD

The heavy-ion simulation considers the particle strike in the corresponding time of 10 ps and the ion track according to the parameters presented in Section III. Considering that the

Table 3 Electrical Characteristics—comparative between the Fin-FETs modeled in TCAD and SPICE (PTM)

Electrical Characteristics		TCAD	PTM	Δ
NFET	Ioff	3.920 pA	5.589 pA	-29,86%
	Ioff_norm	93.33 pA/μm	243.0 pA/μm	-61.59%
	Isat	24.69 μA	50.00 uA	-50.62%
	Isat_norm	587.9 μA/μm	2174 uA/μm	-72.96%
PFET	Ioff	7.505 pA	5.732 pA	30.93%
	Ioff_norm	178.7 pA/μm	249.2 pA/μm	-28.29%
	Isat	29.63 μA	45.91 uA	-35.46%
	Isat_norm	705.6 μA/μm	1996 uA/μm	-64.65%

cells were designed with a depth of 1 μm, the deep length for the ion track was set as 0.9 μm. Figure 6 depicts the cells' behavior when an SEU is observed. In more detail, Fig. 6(a) presents the bit-flip caused by ionizing particles with the lower LETs (threshold LET, or LET_{th}) in the different designed cells, or, in other words, when Q_{crit} is achieved. However, according to [3], the definition of Q_{crit} in SRAMs is not as intuitive as for logic circuits, where it is associated exclusively with the charge stored in the node and the drive strength of the restoration transistors. In SRAMs, the feedback plays an important role, collaborating with the behavior of the transient current pulse. Two ways of defining Q_{crit} can be found in the literature. The first one considers the value of deposited or collected charge able to start bit-flips. The second definition considers the value of the charge flowing in excess during the transient current in the affected node, which considers also the charge flow due to the circuit dynamics (hence not merely the collected charge) [3]. Moreover, Fig. 6(b) shows the drain current observed for particles (with $LET = LET_{th}$) injected at one of the inverters' nFET. One can notice a plateau region on the current pulses, corresponding to the occurrence of the feedback action. The feedback action tends to activate the nFET, which is nominally *off* before the transient. As can
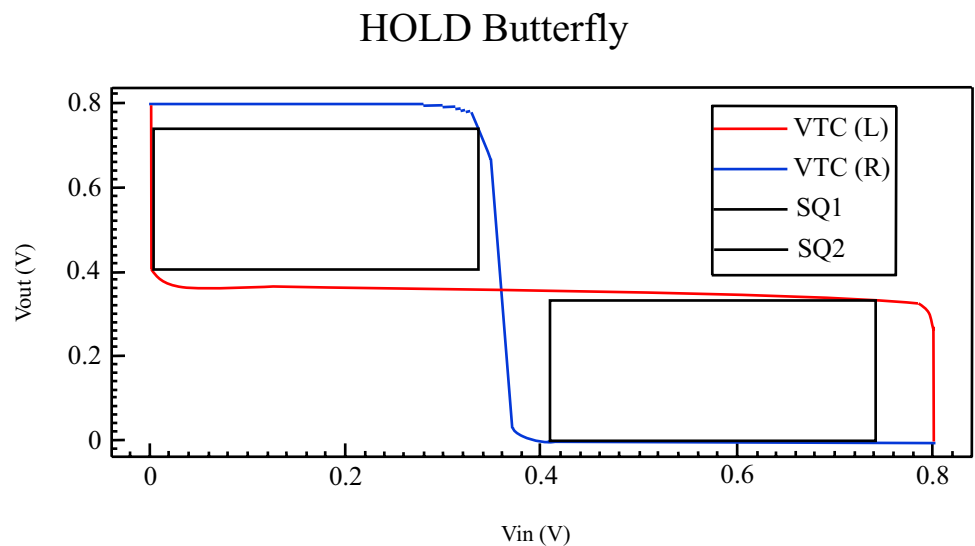
Table 4 Comparison of the SNM values considering the FinFET-SRAM cell modeled in TCAD and in SPICE (PTM)

Cell	Hold_SNM		Read_SNM		Write_SNM	
	TCAD	*PTM*	*TCAD*	*PTM*	*TCAD*	*PTM*
HD	0.33	0.30	0.15	0.13	0.39	0.30
LV	0.34	0.30	0.18	0.16	0.38	0.30
HP	0.33	0.30	0.15	0.13	0.39	0.30

Fig. 5 Hold SNM butterfly curve

HOLD Butterfly

be observed from Fig. 6(a), the plateau happens while both transistors are simultaneously in a conduction state (near the inverter trip point). Since the *n* devices of LV and HP cells are built with two fins, the current on this plateau is higher, which facilitates the inversion of the bit stored in the cell. Thus, it can be expected that the LET_{th} for these two models is similar.

The data presented in Table 5 demonstrates that the HD cell is the most robust when considering transients injected in pull-down transistors; the LET_{th} obtained with TCAD simulations is higher. The table's remaining columns show the charge that is injected to simulate the heavy-ion (Q_{dep}) and the excess charge (Q_{exc}), which is the charge disturbance on the affected node (integral of the transient current). Despite the lower LET_{th}, one may notice that Q_{exc} is higher for LV and HP cells due to circuit dynamics. Another point that deserves attention is that not all the deposited charge is collected, as already discussed by [3]. Indeed, related works often consider the quantity denominated Q_{exc} as the Q_{crit}

in SPICE-based injection campaigns. However, it is clear that this may lead to an erroneous evaluation regarding the circuit reliability, especially for SRAMs, as can be observed in Table 5. According to [24], Q_{crit} values computed from currents of 3D device simulation are approximately 3 times smaller than those found using current models. Therefore, this paper uses the value of LET_{th}, based on the values obtained with TCAD, for reliability comparison purposes. Additionally, for SPICE simulations, we adopted the quantity Q_{exc}, which is the charge disturbance on the circuit due to the impact of a particle with LET = LET_{th} on the drain of the sensitive transistor. From here on, this work avoids using the term critical charge during its analysis, since smaller LET values and deposited charges may result in a higher amount of excess charge, as observed during TCAD simulations, and in Table 5.

The distance of the ion impact from the transistor drain and the track length also plays an important role. Figure 7 shows the drain current that results from the impact of a

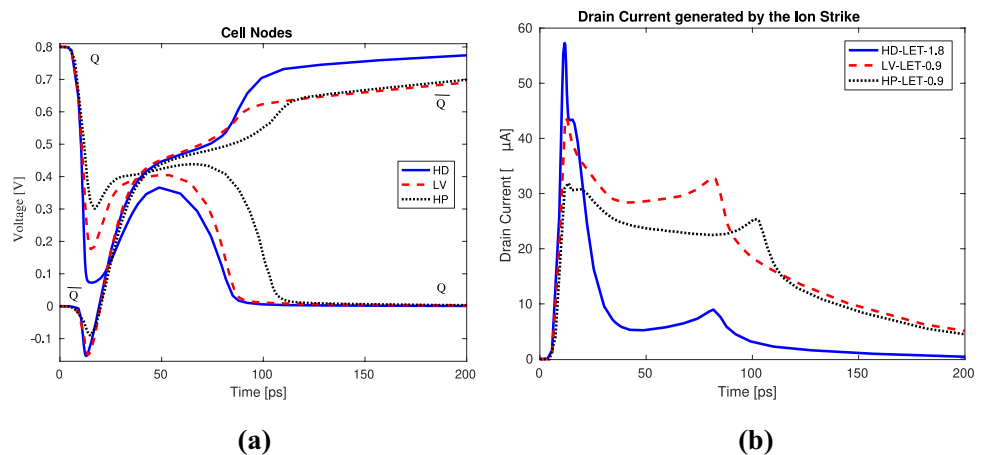**Fig. 6** (**a**) Bit-flip in the cell; (**b**) Current generated by the ion strike

(a)

(b)

Table 5 Threshold LET and Deposited Charges (TCAD)

Cell	LET$_{th}$ (MeV-cm^2/mg)	Q_{dep} (fC)	Q_{exc} (fC)
HD	1.8	16.7	1.24
LV	0.9	8.34	3.79
HP	0.9	8.34	3.55

particle with LET $= 80$ MeV-cm^2 /mg occurring 112 nm from the drain region's center of the pFET in the HD cell. The current difference observed in this figure is only caused by the variation of the charge track length from 150 to 200 nm. Integrating the results, one obtains a charge of 9.0 fC and 11 fC, respectively. It is possible to see that a much higher LET is needed to produce a similar amount of charge collection, able to generate a bit-flip if the impact occurs far from the drain.

The observed current curves in TCAD simulations were then modeled as current sources in SPICE. The well-established Messenger's double exponential model [25] is still being applied in related works to simulate SEEs due to its simplicity, even for recent FinFET technologies [6]. However, in some cases, this model may not accurately represent the current behavior. For instance, in this work, the double exponential is suitable to model a particle with LET $=$ LET$_{th}$ striking the pull-down transistor of the HD cell because the current from the plateau has a low effect in the bit-flip, while the same is not true to the LV and HP cell (Fig. 6(b)). A previous work that investigated single events in FinFETs [6] considered the following values using the double exponential time constants for the execution of SPICE simulations: $\tau_1 = 2$ ps and $\tau_2 = 20$ ps (time constants of rising and falling exponentials, respectively). However, TCAD simulations in the present work showed that, for strikes on nFET of the HD configuration, the rising and fall times are similar, resulting

in $\tau_1 = 6$ ps, $\tau_2 = 9$ ps, and $(t_{d2} - t_{d1}) = 7$ ps (t_{d1} and t_{d2} are the initial times of both exponentials). Therefore, the double exponential curve is shown in Fig. 8(a) was used to perform transient injections on HD cells in SPICE, though varying the current peak according to the desired injected charge. Both curves (TCAD and SPICE modeled double exponential) are shown in Fig. 8(a).

However, the pulse shapes observed for the LV and HP configurations are significantly different from the double exponential. Hence, following the methodology proposed by [26], a combination of three exponential sources in SPICE is proposed to represent the behavior. The first is the double exponential with $\tau_1 = 6$ ps, $\tau_2 = 8$ ps, and $(t_{d2} - t_{d1}) = 7$ ps with a short peak, the second source is a long double exponential with $\tau_1 = 6$ ps, $\tau_2 = 100$ ps, and $(t_{d2} - t_{d1}) = 80$ ps. Finally, an exponential curve with a slow rising time constant completes the modeling, whit $\tau_1 = 85$ ps, $\tau_2 = 8$ ps, and $(t_{d2} - t_{d1}) = 80$ ps. Figure 8(b) depicts these curves.

Although these three source models fit the observed transients very well, a further simplification may be executed. Figure 8(c) shows a comparison of curves with different particle LETs for LV cells, including a simulation in which no bit-flip has occurred. Based on these and other performed simulations, it was verified that besides the current's peak value, the plateau amplitude and duration are the main parameters of the curve related to bit-flips. Therefore, the component of the later peak from the proposed curve can be removed to simplify the model, though keeping the plateau as shown in Fig. 8(b).

4.3 Influence of Resistive Defects on SEU Reliability

In order to evaluate the impact of SEUs on the reliability of the FinFET-SRAMs in the presence of resistive defects, simulations using Hspice™ were performed. A FinFET-SRAM cell adopting a 14 nm PTM technology was designed

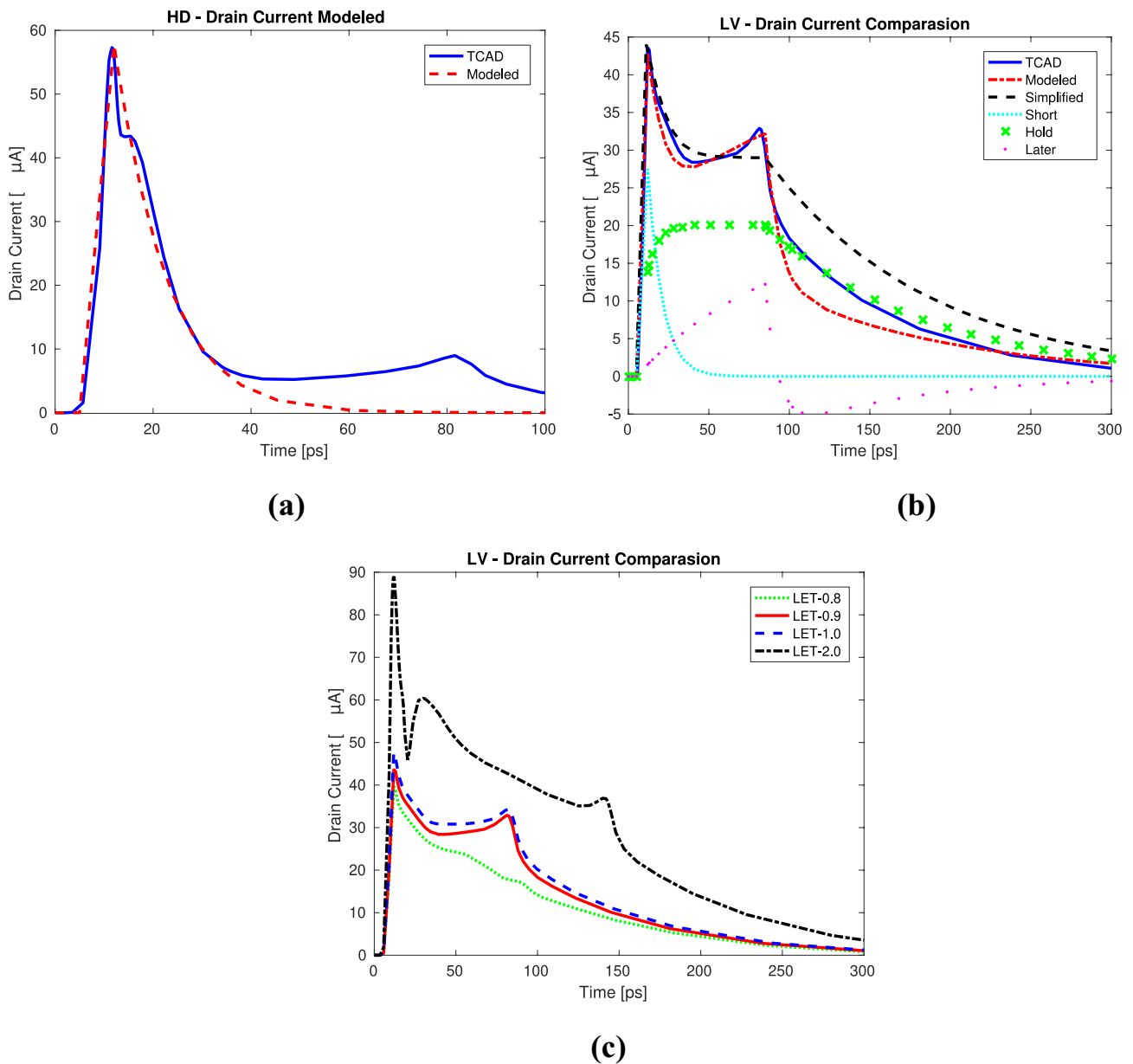**Fig. 7** Drain current with different charge track lengths implemented with ion far from the drain
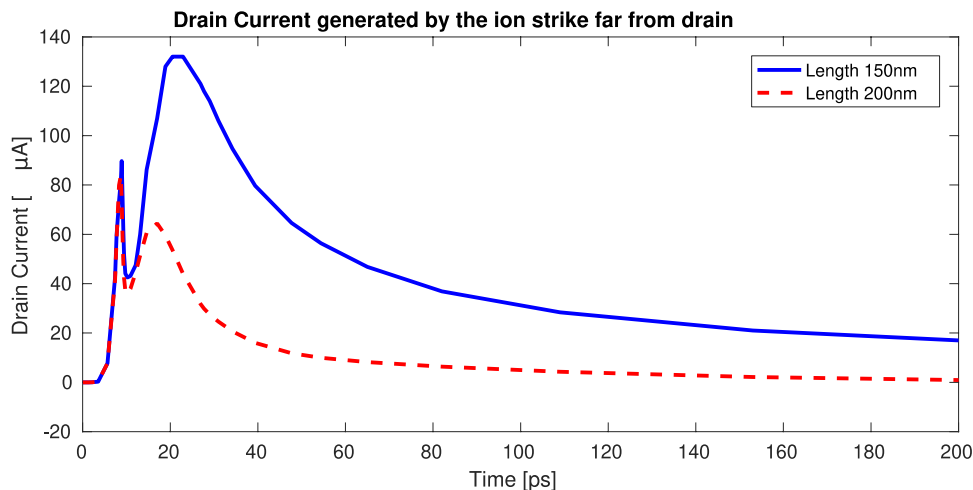
Fig. 8 Transient current modeled in spice for (**a**) HD cell and (**b**) LV cell and (**c**) comparison of curves with different particle LETs for LV cell (TCAD)

for simulating the ionizing particle as a current source in the pull-down transistor according to the models presented in the previous Section. The values of Q_{exc} corresponding to the transient effects (Q_{exc_nom}), the peak current (I_{peak}), and the plateau current ($I_{plateau}$) are summarized in Table 6. Note that the values of Q_{exc_nom} were obtained by integrating the current pulse, considering the lower values of I_{peak} that resulted in bit-flips in the SPICE model, and modeling the same value of plateaus observed in TCAD. This way, some variations in Q_{exc_nom} were observed when compared to the TCAD model. This difference is observed due to the fact that

different technological parameters for the TCAD model and the SPICE PTM model are applied.

Table 7 shows the observed values of R_{crit}, along with the values of simulated Q_{exc} and the correspondent I_{peak} and $I_{plateau}$. The value of Q_{exc_alt} was reduced from Q_{exc_nom} by 10% to verify if weak defects can reduce the amount of charge needed to cause a bit-flip. For resistive open defects, the critical resistance is the lowest value that results in a bit-flip, considering the reduced value of Q_{exc_nom}. For resistive bridges, the R_{crit} are the highest values that render the cell susceptible to SEUs. The defects marked with '*' indicate

Table 6 Excess Charge Configuration

Cell	Q_{exc_nom} (fC)	I_{peak} (µA)	$I_{plateau}$ (µA)
HD	1.01	63.5	-
LV	5.28	47.0	31.0
HP	5.46	47.9	32.1

Table 8 Weak resistive defects that prevent bit-flips, considering the critical excess charge (spice)

Cell	Q_{exc_nom} (fC)	R_{crit} (Ω)
HD	1.01	DFO2* = 2429
		DFO3 = 5623
		DFO4 = 1603
		DFO6 = 2715
		DFB2 = 645.1 k
		DFB3&4* = 11.30 k
		DFB6* = 645.1 k
LV	5.28	DFO2* = 7052
		DFO3 = 2044
		DFO4 = 4128
		DFO6* = 664
		DFB2 = 1.322 M
		DFB3&4* = 168.3 k
		DFB6* = 1.322 M
HP	5.46	DFO2* = 310
		DFO3 = 132
		DFO4 = 4803
		DFO5 = 157
		DFO6 = 351
		DFB2 = 5.122 M
		DFB3*&4* = 5.036 M
		DFB6* = 5.122 M

that this defect was injected into a different cell's inverter than the transient was injected into.

Looking at Table 8, it is possible to observe that weak resistive defects may indeed modify the cell robustness. DFO2 and DFO4, which are low resistance open defects, as well as DFB2 and DFB6, which represent high resistances for bridge defects, represent this situation where the cell robustness is reduced. Note that the defect sizes adopted represent weak defects, which means that may not be detectable by manufacturing tests, even those able to detect dynamic faults, according to the results in [23].

This paper also investigated what is the nominal value of excess charge necessary for causing a bit-flip in a healthy cell. It was possible to observe that some defects may turn the cell more robust to the SEUs, as shown in Table 8. It is interesting to notice that some defects may have distinct impacts when occurring in the inverter that is affected by the SEU or during their occurrence in the opposite inverter. For example, if DFO2 occurs in the inverter hit by the ion, the bit-flip occurrence is facilitated, while, if it occurs in the opposite inverter, a higher collected charge is needed to turn the event into an SEU.

5 Final Considerations

This work analyzed the impact of SEUs on the reliability of defective FinFET-based SRAM cells. To accomplish this, three variants of 14 nm FinFET SRAM cells were modeled using TCAD. In a subsequent step, ion strikes were simulated and injected into the modeled cells. As a contribution, the obtained current shapes and the corresponding excess charges for the different design variants (HD, LV, and HP) were modeled.

This work also remarks that physical simulations (TCAD) should be performed if the goal is to evaluate, by simulation, the design sensitivity to a given energy spectrum of incident particles. This phenomenon happens due to a specific SRAM circuit dynamic: a particle with lower LET can result in a higher value of excess charge depending on the layout configuration, as demonstrated in this work. Therefore, SPICE simulations that consider this value as a comparison parameter or as a critical charge (classic simulation method) do not accurately represent the actual memory reliability concerning single events in real radiation environments.

In this work, considering the TCAD simulation data, the HD cell demonstrated to be more robust than HP and LV cells since a higher LET was necessary to trigger a

Table 7 Weak resistive defects that increase the SEU sensitivity of the studied SRAM cells

Cell	Q_{exc_alt} (fC)	I_{peak} (µA)	$I_{plateau}$ (µA)	R_{crit} (Ω)
HD	0.909	56.0	-	DFO2 = 2839
				DFO4* = 509
				DFB1 = 1.524 M
				DFB2* = 1.680 M
				DFB3&4 = 710.6 k
				DFB6 = 1.680 M
LV	4.77	41.6	28.0	DFO2 = 4351
				DFO4* = 920
				DFB1 = 209.5 k
				DFB2* = 1.145 M
				DFB3&4 = 106.8 k
				DFB6 = 145.0 k
HP	4.94	43.6	29.1	DFO2 = 3480
				DFO4* = 708
				DFB1 = 638.7 k
				DFB2* = 348.3 k
				DFB3&4 = 163.1 k
				DFB6 = 348.4 k

bit-flip. After discussing the suitability of applying the double exponential model to simulate SEE in this technology, the obtained current shapes observed in TCAD were modeled in SPICE. For specific cell configurations and particle energy conditions, the double exponential is still a satisfyingly accurate model, while for other cases, different current models had to be proposed.

Finally, this paper showed that weak resistive defects might indeed affect the behavior of the cell under single events. In fact, some weak defects may turn the cell more prone to SEUs. However, some defects may prevent bit-flips from occurring, considering the LET_{th} observed for a defect-free cell, making a higher particle LET necessary to generate an SEU. This ambiguous behavior is explained by the fact that the amount of excess charge due to a single event in SRAMs is highly dependent on the circuit's dynamic response, which indeed may be significantly modified by the occurrence of resistive defects. As future work, we identify that it would be interesting to calibrate the proposed models with empiric experimental data.

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