# Impact of the variation of capacitance, inductance, and resistive load on the behavior of buck converter

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**Abstract.** This paper deals with the structure of the buck converter circuit and the influence of the inappropriate values of its electrical components on the trend of its output voltage. In this perspective, a further study is established on the variation of the inductance, the capacity and the load. As a result, an observation of their impacts on the behavior of the converter is performed. Therefore, when the inductance value is low and the capacitance value is defined as large, the system tends to be more stable and faster. The optimal values of these two components have been considered within the converter circuit in order to closely observe the output response. Indeed, the obtained response has been the most stable and the faster. In this context, a comparison has been made between the calculated values and those obtained during the simulation on Matlab/Simulink. A small difference is observed between the both. On the other hand, the variation of the load resistance only influences the stability of the system, seen clearly for important values.

## 1 Introduction

The electronic conversion of electrical energy is essential to adapt the input voltage to the need of the load in terms of electrical current and voltage. In the literature, several devices of static conversion are used, namely: transformers, rectifiers, choppers and inverters [1-3]. In this work, we deal with a chopper converter that transforms DC energy from a fixed value to another larger or smaller one. In this context, two types of converters are distinguished: Boost and Buck [4-6]. This paper analyzes the buck chopper converter which involves stepping down the source voltage in DC-DC mode. Basically, a buck chopper is made up of a MOSFET transistor, a normal diode, an inductor and a capacitance. The chopper is controlled at the gate of the MOSFET transistor by a square wave signal called "Pulse Width Modulation" (PWM) with a variable duty cycle [7]. The optimization of the output voltage and current at the terminals of the load strongly depends of the optimum value of the duty cycle.

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We closely study the behavior of the buck static converter according to different values of inductance, capacitance and load. A comparative study is established to conclude the correct value to be used in the equivalent electrical circuit. In addition, automatic notions are put in place to interpret the resulting curves for each studied value of each electrical component. From the obtained outcomes, a low value of the inductance and a large value of the capacitance lead to a faster and more stable conversion with damped oscillations.
This paper is organized as follows: Section 1 deals with the introduction. Section 2 describes the equivalent circuit of the DC-DC static buck converter. Section 3 presents the dimensioning of the studied converter. Section 4 reveals in detail the different obtained results as well as their interpretations. Section 5 presents the conclusion of the paper.

## 2 Buck converter modeling

A DC-DC converter is a static device intended to reduce the input power according to the output load needs. The conversion process can be controlled by a duty cycle that drives the gate of a MOSFET transistor. It is however ensured by using a combination of electrical components namely: Inductance, capacitance and semiconductor diode. Through designing a buck converter circuit, the analysis begins with the assumption that the circuit is operating in a steady state, the inductance current is in DC mode and the output voltage is held constant at voltage V0. The circuit of the buck converter is shown in Figure 1.

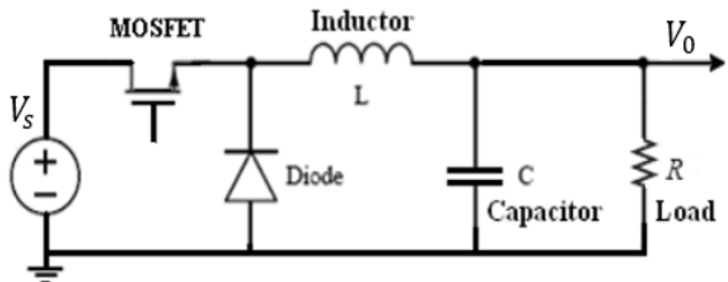


**Fig. 1.** Buck Converter circuit

When the MOSFET transistor is on, the current flows from the DC source through the inductance toward the load [8]. The energy stored in the inductance increases until the transistor turns off. At this point, the diode polarized in reverses and blocks the current path:

$$V_L = V_S - V_0 \quad (1)$$

However, when the MOSFET turns on, the diode becomes forward polarized and the inductance acts as a source allowing the current to continue to flow through the resistive load. The current passes through the inductance, the resistive load and the diode:

$$V_L = -V_0 \quad (2)$$

As a result, the energy stored in the inductance decreases and its current decreases. The voltage output $V_0$ is expressed as follows:

$$V_0 = V_S \times D \quad (3)$$

In steady state, the average current in the capacitance must be zero so that the average current in the inductance will be the same as the average current in the load resistance:

$$I_L = I_0 = \frac{V_0}{R} \tag{4}$$

When operating in DC mode, the inductance current varies between a minimum inductance current ($I_{\min}$ ) and a maximum inductance current ( $I_{max}$) the inductance current is assumed to evolve linearly. The minimum and maximum inductance currents are calculated as follows:

$$I_{min} = V_0\left(\frac{1}{R} - \frac{1-D}{2Lf}\right) \tag{5}$$
$$I_{max} = V_0\left(\frac{1}{R} + \frac{1-D}{2Lf}\right) \tag{6}$$

Using Eqs. 5 and 6, the peak-to-peak inductance current ripple is defined:

$$\Delta I_L = I_{max} - I_{min} \tag{7}$$

If the desired switching frequency is established, the minimum inductance ($L_{min}$) is required for DC mode [9]. In experience, an inductance value greater than ($L_{max}$) is suitable to ensure a continuous current. Some designers select an inductance value around 25 - 40% higher than $L_{min}$.

$$L_{min} = \frac{(1-D)R}{2f} \tag{8}$$

The capacitance withstands a sudden change in the voltage across it. In this study, the capacitance was used to filter the output voltage and to reduce the output voltage ripple. The latter depends on the source voltage, duty cycle, frequency, filter inductance value and the capacitance value [10], from which comes the expression allowing the calculation of the capacitance:

$$C = \frac{1-D}{8f\left(\frac{\Delta V_0}{V_0}\right)f^2} \tag{9}$$

## 3 Designing the buck converter

The buck converter circuit is designed for a switching frequency of 100 kHz, an input voltage around 30V, a duty cycle fixed at 90% and with a resistive load value 50 Ω. The minimum size of the inductor $L_{min}$ is determined to ensure the operation of the circuit in direct current mode using Eq.8:

$$L_{min} = \frac{(1-D)R}{2f} \tag{10}$$

An inductance value 25% higher than $L_{min}$ is considered:

$$L_{min} = \left(\frac{25}{100} \times L_{min}\right) + L_{min} = 40\mu\text{H} \tag{11}$$

The ripple of the output voltage of the buck converter is taken less than 1% almost 0.03% of the output voltage in this study. On the other hand, the value of the capacitance has been calculated to be around 100 µF. The capacitance value is selected using Eq. 9:

$$C = \frac{1-D}{8f\left(\frac{\Delta V_0}{V_0}\right)f^2} = 100\mu\text{F} \tag{12}$$

# 4 Results and discussions

In this paper, the simulation of the designed circuit of the buck converter is performed under MATLAB/Simulink software. In this context, a further study has been adopted. Indeed, we calculated the theoretical optimal values of the maximum current, minimum current, the current ripple, the voltage ripple and the output voltage and compared them with the corresponding values found through the simulation. In another part we studied and closely observed the influence of the variation of the inductance and the variation of the capacitance on the stability of the response of the converter. A study of the load variation was also taken into account.

## 4.1 The buck converter circuit

The circuit shown in Fig. 1 was carefully plotted on MATLAB/Simulink as shown in Fig. 2 by adding blocks allowing to display the curves of the voltage $V_S$ according to the various parameters defining the circuit.

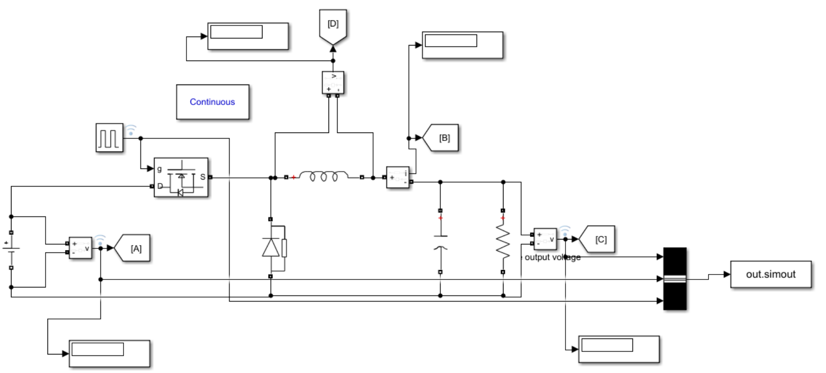


**Fig. 2.** Buck Converter circuit under Matlab/Simulink.

We attacked this circuit with the following parameters:

- A supply voltage of 30V,
- A frequency of 100 kHz,
- A duty cycle fixed at 0.9.

In this work, the Buck converter designed and studied for a low output voltage ripple (0.02% $V_0$) with an output voltage of 27 volts.

## 4.2 Influence of the dynamic variation of the inductance on the output voltage

The capacitance value and the buck converter load are kept constant around 100 µF and 50 Ω respectively, while the inductance value varies between three values (30, 60 and 100 µH). The results of the simulation can be seen at Fig. 3.

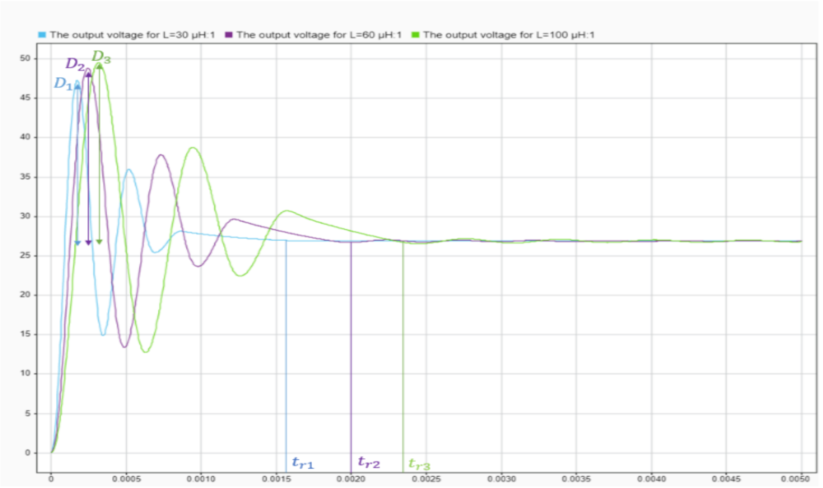


**Fig. 3.** Evolution of the converter output voltage according to the variable inductance L.

**Table 1.** Variation of overshoot and response time according to inductance value.

| **Inductance L (µH)** | 30 | 60 | 100 |
|---|---|---|---|
| **Overshoot D (%)** | 43.08 | 44.92 | 45.81 |
| **Response time $t_r$ (ms)** | 1.49 | 1.99 | 2.5 |

- ***L= 100 µH***: The output voltage of the converter includes three clearly visible oscillations such that the maximum overshoot is defined by D = 45.81%. The response of the converter don't stabilize in its steady state and is always seen with weakly damped oscillations from $t_{r3}$ = 2.5ms.

- ***L= 60 µH***: The output response includes three oscillations with a maximum overshoot D = 44.92% more or less low compared to the first case. The converter considers itself faster and more stable. Indeed, it begins to provide a fixed voltage at $t_{r2}$= 1.99ms once the steady state is established.

- ***L= 30 µH***: The response of the converter is the fastest $t_{r1}$ = 1.49ms compared to the two previous cases. The output voltage is marked by two oscillations, with the lowest maximum overshoot D = 43.08%.

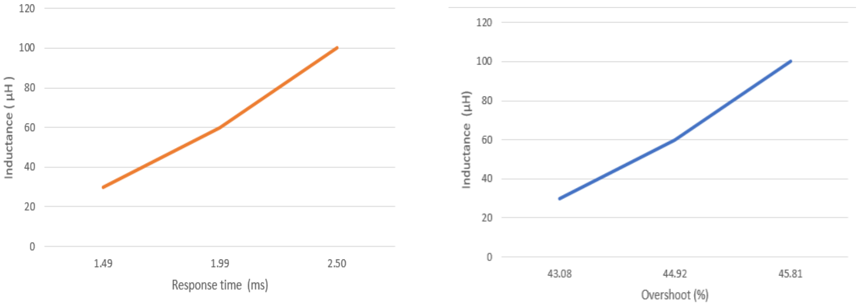


**Fig. 4.** Evolution of the overshoot and response time according to the inductance variation.

*When the inductance decreases the converter becomes more stable and faster*

### 4.3 Influence of the dynamique capacitance variation on the output voltage

In this second simulation, the inductance value and the output load are fixed at 30 µH and 50 Ω respectively. The values of the capacitance vary according to three different values. Fig. 5 shows the trend of the voltage for each considered value of the capacitance.


**Fig. 5.** Evolution of the output voltage of the converter according to the variable capacitance C.

**Table 2.** Variation of overshoot and response time according to inductance value.

| **Capacitance C (µF)** | 10 | 50 | 100 |
|---|---|---|---|
| **Overshoot D (%)** | 46.77 | 44.92 | 43.10 |
| **Response time $t_r$ (ms)** | 0.34 | 1.14 | 1.37 |

- **C = 10 µF**: The converter is oscillated (not stable) but fast with important maximum overshoot D = 46.77% and a low response time ($t_{r1}$ = 0.34ms).
- ***C = 50 µF***: The response is slower ($t_{r2}$= 1.14ms) than the case of C = 10µF. The oscillations are characterized with a maximum overshoot D = 44.92% lower than the previous case.
- ***C= 100 µF***: The converter is stable but slow. Indeed, the oscillations have the lowest overshoot D = 43.1% and an important response time ($t_{r3}$= 1.37ms).

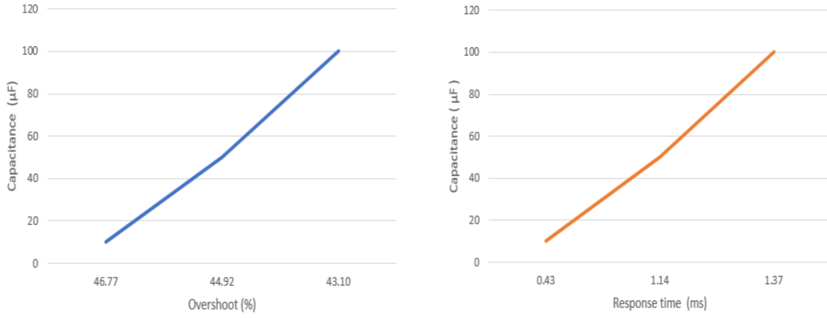


**Fig. 6.** Evolution of the overshoot and response time according to the capacitance variation.

*As the capacitance increases the converter becomes more stable but slow to generate its response.*

### 4.4 The dynamique varaition of the load

In this third simulation, the capacitance and inductance values are considered constant at 100 µF and 30 µH respectively. The variable term in this study is load. The variation of the latter is performed on three values 10Ω, 25Ω and 50Ω as shown in Fig. 7.

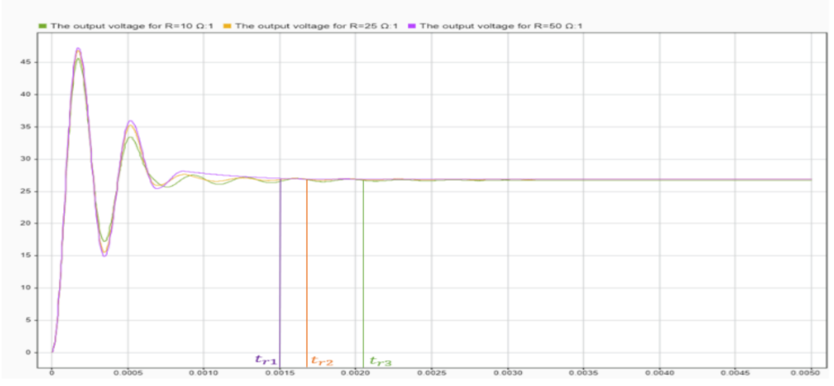


**Fig. 7.** Evolution of the output voltage of the converter according to the variable load R.

- ***R= 10 Ω***: The converter oscillates too much with $t_{r1}$ = 1.45 ms.
- ***R= 25 Ω***: The output voltage includes almost five oscillations, such that $t_{r2}$ = 1.36 ms.
- ***R= 50 Ω*** : the response is characterized by three oscillations and shows that the converter is stable, $t_{r3}$ = 1.3 ms.

### 4.5 Study of the dimensioned step-down converter

The value of the inductance and of the capacitance are found in the previous sections, namely L = 30µH and C = 100µF are used in this simulation. In this context, we made the theoretical calculation of some parameters and we carried out a comparative study with the simulation. As result, we obtained the curve shown in Fig. 8 that shows the optimum output voltage.

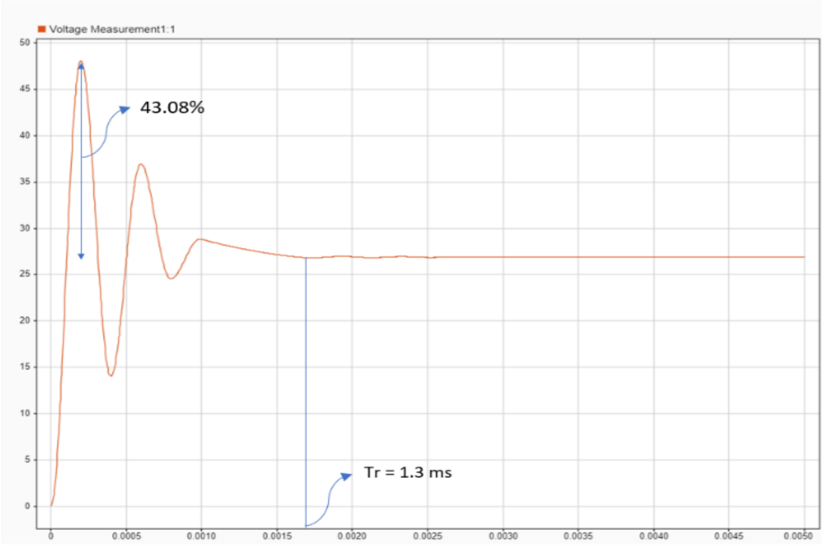


**Fig. 8.** Trend of the output voltage.

After simulating the circuit of Fig. 2, we deduced the measured values and compared them with those calculated theoretically. Table 3. clearly shows the obtained outcomes

**Table 3.** Comparison of calculated and simulated parameters.

| Item | Theoretical calculation | Simulation results |
|---|---|---|
| $I_L$ | 0.54A | 0.50A |
| $I_{max}$ | 0.87A | 0.88A |
| $I_{min}$ | 0.20A | 0.19A |
| $\Delta I_L$ | 0.67A | 0.73A |
| $V_0$ | 27V | 0.68V |
| $\frac{\Delta V_0}{V_0}$ | 0.03% | 0.02% |

The results of simulation and those calculated seem to be matched with a low difference between the both.

## 5 Conclusion

In this paper the impact of the variation of the inductance, the capacitance and the load on the output voltage of the buck converter. The lower the inductance and the greater the capacitance are the more stable and faster the converter is. On the other hand, the variation of the load is also carried out in order to observe its effect on the output response.

Consequently, the variation of the load acts directly on the stability of the converter without any influence on its rapidity. Indeed, the greater the load is the faster the converter is too. A comparative study is established between the theoretical calculation and the simulated measurements for some specific parameters of the converter, showing then a compatibility between the both.

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