Development and Validation of an optimized syndromes block for reed solomon decoder

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Abstract. Reed Solomon decoder plays an indispensable role in many applications involving data transmission, storage applications and Video broadcasting DVB-T and DVB-S2. In this work we propose a new optimized parallel syndrome block [67] for the Reed Solomon RS code (15,11) used in digital Video broadcasting DVB-T. Therefore, this proposed parallel block is compared to the serial syndrome block existing. On the basis of this technique a new architecture based on three syndromes in parallel is developed. This technique reduces both the energy consumption and the number of iterations. The RS code (15, 11) is composed of 255 symbols that are multiples of 3. The symbols are entered in parallel in the syndrome block.
These decoding algorithms developed in this work are compared with the existing algorithms, and they are evaluated through a simulation using the hardware description language VHDL, then they are implemented on a Xilinx Spartan type FPGA card using the XILINX software.
Keywords—RS codes, DVB-T and DVB-S2 transmission chains, Galois field, syndrome block. VHDL, FPGA.

1 Introduction

Error correcting codes [1][2][3]are tools aimed at improving the reliability of information transmission[4][5][6] on a noisy channel. The method they use is to send over the channel more data than the amount of information to be transmitted. A redundancy (symbols added to the data by the correction circuit) is thus introduced, it is then possible to correct any errors introduced by this channel, and it is possible, despite the noise, to find information transmitted at the start (i.e) the message received is indeed the message sent). However, to make this communication[6][7] more reliable, these codes use decoding algorithms which use circuits comprising more numbers of iterations, which minimizes their performance, in particular its transmission capacity and its gain[8][[9].

The objective of this work is to develop a new method using the new architectures for RS codes in order to reduce both the complexity and the number of iterations in the syndrome

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Block using a three Parallelization Syndrome Block. The rest of the paper is organized as follows: an overview of Reed Solomon code calculator is provided in section 2. Section 3 discusses the proposed the new syndrome used a three parallelization syndrome .Finally comparison of basic and the modified circuit for different RS codes section 4 followed by a conclusion.

2 REED-SOLOMON THEORY

The RS encoder [10][11][12]works by adding redundancy (parity check symbols) to the input data before the data transmission. The coded data consisting of errors is decoded to recover the data without error. Redundancy symbols are added to allow the RS decoder to detect locations of corrupted data and to fix errors appear in the data. The number of errors can be corrected the RS code depends on the number of parity checks added symbols.

A typical RS code consists of data symbols (message) and parity symbols (redundancy). RS code also known as a systematic code because the data. RS code consists in coded parity symbols that are used to decode the original message with fewer errors.

A general RS code [13 [14] is represented by RS (n, k, t).

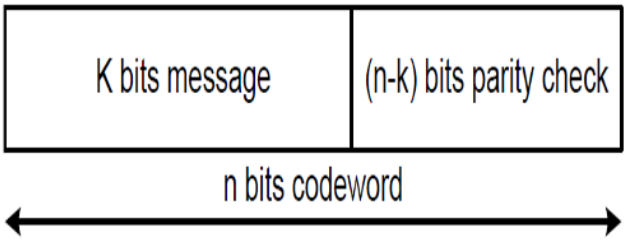

Fig. 1. Systematic form of a codeword of RS code

For a (15, 11) RS code, the encoded code word is 15symbols and the data symbol is 15 symbols. Also, the error correct capability t = 2, where t = (n-k)/2. The parameters used in this study for the RS (15, 11, 2) code are as follow:

- Number of bits per symbols: m = 4 bits
- Number of data being encoded (message): k = 11
- Number of code word in encoded block: n = 15
- Number of parity check symbols (redundancy): 2t =4 symbols
- Maximum number of correctable symbol errors: t = (n-k)/2 = 2 symbols

The symbol width (m) defines the field generator polynomial.

2.1 primitive polynomial

For the field GF [15][16]the corresponding primitive polynomial[17][18] is the following in the table 1.

Table 1. Primitive polynomials in GF (2^m)

m	Polynomial Primitive
3	$1+X+X^3$
4	$\mathbf{1+X+X^4}$
5	$1+X^2+X^5$
6	$1+X+X^6$
7	$1+X^3+X^7$
8	$1+X+X^3+X^4+X^8$
9	$1+X^4+X^9$
10	$1+X^3+X^{10}$
11	$1+X^2+X^{11}$
12	$1+X+X^4+X^6+X^{12}$

The minimum [19] RS code defines the number of symbols distance between two RS code words:

$$d_{min} = n - k + 1 \quad (1)$$

The capability [20] of the RS code is:

$$t=(d_{min}- 1)/2 = (n- k)/2 \quad (2)$$

2.2 RS parameterization for DVB norm

The Table 2 summarizes RS parameters :

Table 2. RS parameters for DVB

Parameter	Symbol	DVB
Field Polynomial	P(x)	$1+X+X^4$
Generator polynomial	G(x)	$g(x) = (x+\alpha^0)\ (x+\alpha^1)\ (x+\alpha^2)\ (x+\alpha^3)$
Bits number/Symbol	M	4
Code length	N	11
Message length	K	15
Parity Symbols	2t	4

3 Proposed optimization and existing algorithm

The optimization algorithm [21] for syndrome block proposed in this paper is easy to compute and provide a simple and scalable approach. There will be 2t syndromes which can be corrected by the decoder.
This syndrome block has 16 iterations using the existing method while just 6 iterations using the modified method.
This optimization algorithm is based on the use of syndrome blocks in parallel in order to reduce the number of iterations.

3.1 Existing algorithm

The existing algorithm used the serial syndrome computation block [22] is implemented by following equation 3.

$$S_i = R(i) = r^{14}(\alpha i)^{14} + r^{13}(\alpha i)^{13} + r^1(\alpha^i) + r^0 \quad (3)$$

Where i = 1, 2, . . ., 2t.

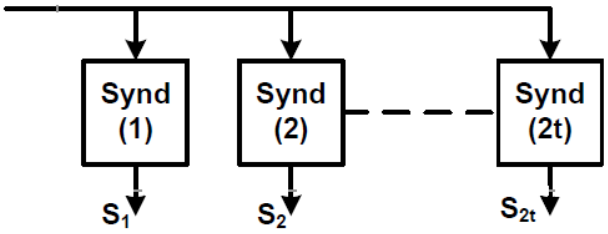

Fig. 2. Serial Syndrome Block Diagram

3.1.1 Case of the basic circuit

The basic circuit of the syndrome computation block for RS (15, 11) is expressed by the equation 4.

$$S_i = R(i) = r^{14}(\alpha i)^{14} + r^{13}(\alpha i)^{13} + r^1(\alpha^i) + r^0 \quad (4)$$

In the equation 4, the circuit corresponding shown in the figure3:

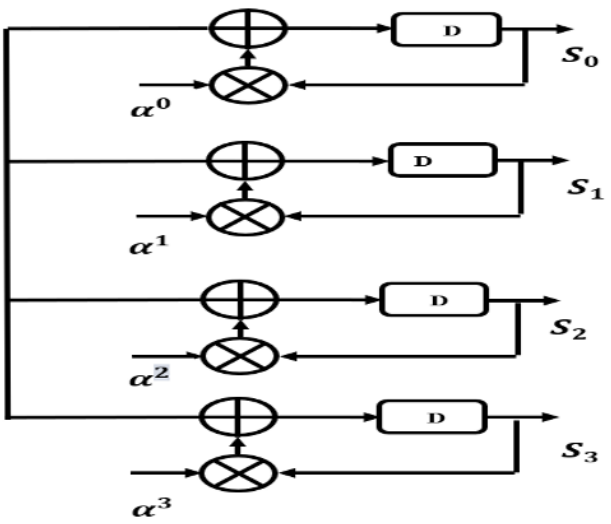

Fig. 3. Basic syndrome block

3.2 Proposed optimization algorithm

In this method, another form of Syndrome computation block circuit is designed that minimizes large number of iterations.

3.2.1 Case of the proposed circuit:

The proposed Syndrome computation Block [24] can be expressed by the equation presented in equation. 5:

$$Si=R(\alpha i)=(((r_{14}(\alpha i)^2+r_{13}(\alpha i)^1+r_{12})(\alpha i)^3+r_{11}(\alpha i)^2+r_{10}(\alpha i)^1+r_9)(\alpha i)^3+..)(\alpha i)^3+r_2(\alpha i)^2+r1(\alpha i)^1 +r0) \quad (5)$$

The first clock, the mot received in parallel is (r14, r13, r12).

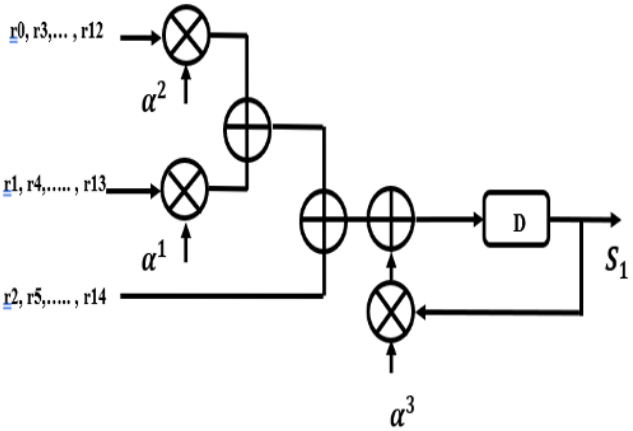

Fig. 4. Modified Syndrome Block

4 SIMULATION RESULTS

The simulation of the basic and proposed syndrome block using the hardware description language VHDL [25] [26] for the RS and BCH decoders are presented in this party.

4.1 Simulation the basic circuit of RS code

The Simulation result of RS code using the equation:
$S_i = R(i) = r^{14}(\alpha i)^{14} + r^{13}(\alpha i)^{13} + r^{1}(\alpha^{i}) + r^{0}$ shown in the figure 5.

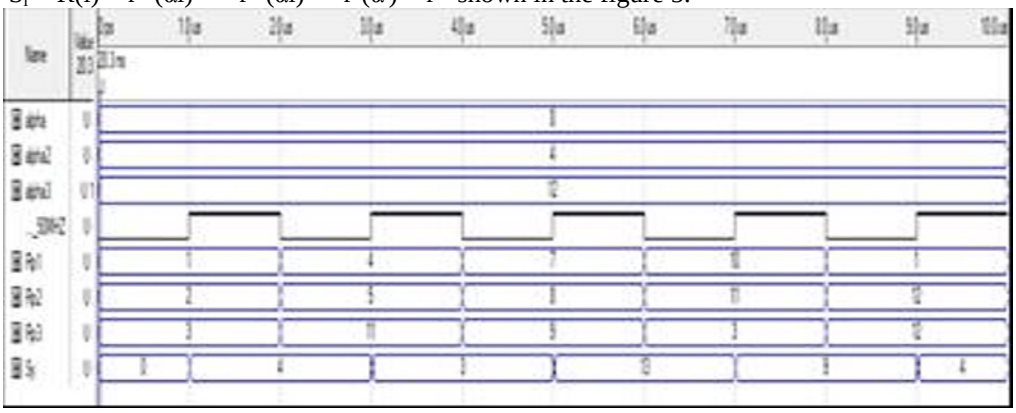

Fig. 5. Simulation result of the basic RS code

4.2 Simulation the proposed circuit of RS code

The Simulation result of the modified RS code using the equation:
$Si=R(\alpha i)=(((r_{14}(\alpha i)^{2}+r_{13}(\alpha i)^{1}+r_{12})(\alpha i)^{3}+r_{11}(\alpha i)^{2}+r_{10}(\alpha i)^{1}+r_{9})(\alpha i)^{3}+..)(\alpha i)^{3}+r_{2}(\alpha i)^{2}+r1(\alpha i)^{1}$ +r0) shown in the figure 6

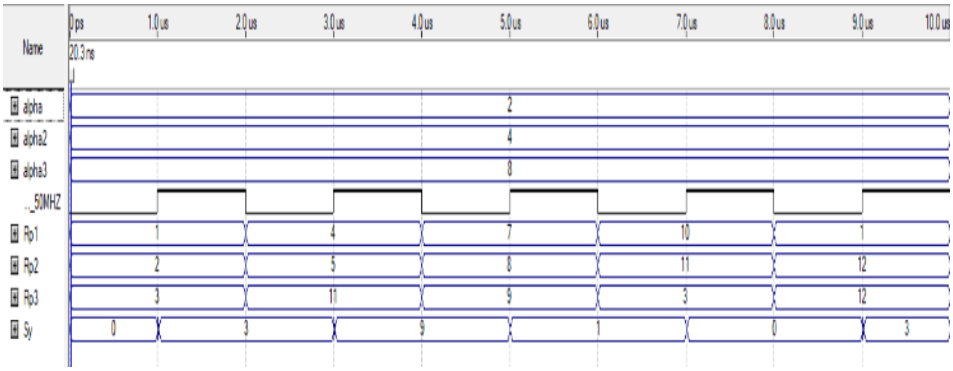

Fig. 6. Simulation result of the modified RS code

The simulation of the developed and basic decoder is presented in this part for the RS code. Thus, simulation results on the tested scenario show that the proposed system is very effective and achieves high performance in the minimization.

5 Design and implementation of RS code

5.1 Syndrome Block

The implementation of the proposed algorithms of Syndrome Block on FPGA consists of programming the circuit using the hardware description language VHDL. We will describe the circuit as a VHDL algorithm. The second step is to perform a simulation using the QUARTUS II [27] software.

The circuit scheme of the implemented program is shown in Figure 7.

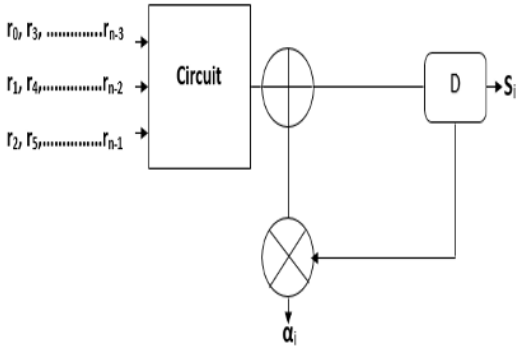

Fig. 7. Block diagram of Syndrome Bloc

The proposed Syndrome Block consists of a global 'Clk' and Three Parallel Inputs initiate the calculating Syndrome Block process, the 'result' can be obtained immediately after entering inputs.

5.2 Implementation of RS code

The proposed algorithm has been implemented on a FPGA Card using Xilinx Spartan 3E-500 to verify the test setup which presented in figure 8.

Fig. 8. Validation of new RS decoder on FPGA card

For the case of RS (15, 11), we have four coefficients of syndrome Block (S0, S1, S2, S3). In Fig.7, the value is equal to 15 (S0 =15) in decimal, (1111) in binary, so we can get the same result with only 5 iterations in comparison with the basic circuit.

6 Conclusion

In this contribution, a new Reed Solomon decoder is developed based an efficient algorithm of syndrome block. This algorithm offers a new syndrome computation block with a view to minimize the number of iterations. The proposed corresponding circuit has been developed, synthesized, simulated, implemented on the FPGA card and compared to the existed one to demonstrate the difference between the two circuits and the number of reduced iterations, the comparison between circuits in table 1 proves that the RS code (15, 11) has 256 iterations using the modified method while, 86 iterations using the basic method.

Finally, Simulation and Experimental results show that the performances of the now Reed Solomon decoder based parallel syndrome block are superior to the performances of traditional Reed Solomon decoders based serial syndrome block.

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