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"Nous sommes comme des nains juchés sur des épaules de géants, de telle sorte que nous puissions voir plus de choses et de plus éloignées que n'en voyaient ces derniers. Et cela, non point parce que notre vue serait plus puissante ou notre taille avantageuse, mais parce que nous sommes portés et exhaussés par la haute stature des géants."

Bernard de Chartres

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Abstract

Electric motor-driven systems represent the largest total global electricity consumption worldwide with medium-voltage motors consuming around 10 percent of the world's energy. On the other hand, the energy cost is increasing, and energy consumption must be reduced for economic and environmental reasons. Therefore, medium-voltage (MV) motors are a clear target for energy improvement ; not just to limit energy bills but also to comply with tightening regulations. Nevertheless, today only a small amount of installed medium-voltage motors are controlled by variable speed drives, opening the door for introducing efficient adjustable speed drives in a wide range of industrial applications. This technology will help the industry around the world to save energy use without compromising performance or production efficiency. Therefore, the medium-voltage drive market is expected to grow significantly during the next decade. This thesis introduces and studies a three-phase multilevel converter topology based on the multiplexed concept which is especially intended for medium-voltage drives. The main targets are four-quadrant 4.16 kV and 6.6 kV power drives. Chapter I presents the context and the state of the art of the MV power drives: their applications, their potential to reduce the energy consumption in the industry, the market expectations, and a description of the aim of this study. The state of the art presents the classical and advanced multilevel topologies that have been implemented as standard products for MV industrial drives and the performance and cost limitation of the HV semiconductors used in these topologies. Chapter II presents the multiplexed family of converters and proposes different structures that could meet the cost and performance requirements of this study by minimizing the number of HV semiconductors. Additionally, the proposed structures are compared in terms of semiconductors cost with two well-established solutions in the market. Chapter III presents the working principle of this topology and two different modulations schemes that have been developed for the structures proposed previously. A carried-based modulation and a space vector modulation have been developed to reduce the switching efforts of the HV semiconductors. Moreover, the two modulation schemes have been compared in terms of waveform quality. Finally, chapter IV presents the experimental results that validated some particular technical aspects of the multiplexed structure and some assumptions made during this work. Three different test benches (one being a complete inverter) have been used to validate the series connection of 1.7 kV and 4.5 kV IGBTs, to measure the switching energies of HV semiconductors under reduced voltage and measure the stray inductances of the inverter. These results have been used to estimate the efficiency of the proposed structure, study the distribution of semiconductors losses, and compare the performances of the two developed modulation schemes.

Keywords: Medium-voltage power drives, multilevel topologies, multiplexed topology, space vector modulation, power semiconductors characterization, IGBTs series connection.

Resumé

Les systèmes entraînés par des moteurs électriques représentent la plus grande consommation totale d'électricité dans le monde, les moteurs à moyenne tension consommant environ dix pour cent de l'énergie mondiale. D'autre part, le coût de l'énergie augmente, et la consommation d'énergie devient de plus en plus importante pour des raisons économiques et environnementales. Par conséquent, les moteurs moyenne tension (MT) sont une cible évidente pour les mesures d'amélioration énergétique, non seulement pour limiter les factures d'énergie, mais aussi pour se conformer à des réglementations plus strictes. Néanmoins, seule une petite partie des moteurs MT actuellement installés sont contrôlés par des variateurs de vitesse, ce qui ouvre la porte à l'introduction de variateurs de vitesse efficaces dans un large éventail d'applications industrielles. Cette technologie aidera l'industrie du monde entier à économiser de l'énergie sans compromettre les performances ou l'efficacité de la production. Par conséquent, le marché des variateurs MT devrait connaître une croissance solide au cours de la prochaine décennie. Ce travail de thèse étudie et propose une topologie de convertisseur multiniveau triphasé basée sur le concept multiplexé qui est spécialement destinée aux applications variateurs de vitesse moyenne tension. Les principales applications potentielles sont les variateurs de vitesse quatre quadrants de $4,16\,kV$ et $6,6\,kV$. Le chapitre I présente le contexte et l'état de l'art des variateurs de vitesse MT. Le contexte couvre leurs applications, leur potentiel pour réduire la consommation d'énergie dans l'industrie, les attentes du marché, et les objectifs de cette étude. L'état de l'art présente les topologies multi-niveaux classiques et avancées qui ont été implémentées en tant que produits standards pour les variateurs industriels MT, ainsi que les limites de performance et de coût des semi-conducteurs HT utilisés dans ces topologies. Le chapitre II présente la famille des convertisseurs multiplexés et propose différentes structures adaptées aux objectifs de coût et de performance de cette étude en minimisant le nombre de semi-conducteurs HT. De plus, les structures proposées sont comparées en termes de coût des semi-conducteurs avec deux solutions bien établies sur le marché. Le chapitre III présente le principe de fonctionnement de la topologie et deux schémas de modulation différents qui ont été développés pour les structures proposées précédemment. Une modulation basée sur le transport et une modulation vectorielle ont été développées pour, en association avec le principe de fonctionnement, réduire les efforts de commutation des semi-conducteurs HT. De plus, les deux schémas de modulation ont été comparés en termes de qualité de forme d'onde. Enfin, le chapitre IV présente les résultats expérimentaux qui ont validé certains aspects techniques particuliers de la structure multiplexée et certaines hypothèses formulées au cours de ce travail. Trois bancs d'essai différents (l'un étant un onduleur complet) ont été utilisés pour valider la connexion en série des IGBT de $1,7\,kV$ et $4,5\,kV$, pour mesurer les énergies de commutation des semi-conducteurs HT sous tension réduite et pour mesurer les inductances parasites de la structure de l'onduleur. Ces résultats ont été utilisés pour estimer l'efficacité de la structure proposée, étudier la distribution des pertes des semi-conducteurs, et comparer les performances des deux schémas de modulation développés.

Mots clés : Variateurs de vitesse moyenne tension, topologies multiniveaux, topologie multiplexée, modulation vectorielle, caractérisation des semi-conducteurs de puissance, connexion en série des IGBTs.

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Chapter 1

General Introduction

1.1 Medium-voltage power drives

Variable speed drives are classified as medium voltage (MV) when their operating voltage is typically between 2.3 and 13.8 kV. These drives have found widespread applications such as compressors, pumps, fans, grinding and rolling mills, conveyors, crushers, blast furnace blowers and gas turbine starters, to name a few. Thus, finding applications in a wide range of industries, such as oil and gas, petrochemical, mining, water, waste treatment, paper pulp, cement, chemical, power generation, metal production and processes, traction, and marine drive sectors [1–9].

Concerning the worldwide situation, it is estimated in [10] that electric motor-driven systems (EMDSs) represent 43% to 46% of the total global electricity consumption. This represents more than twice the second largest consumption, which is lighting (19%) [11]. From this percentage, 64% of the energy consumption by motor-driven systems comes from the industry sector [12]. Therefore, electrical motors in industry represent 28 % of the total worldwide consumption [13]. These data can be analyzed by another perspective: the industry represents 40% of the world's energy consumption [13] and around 70% of the total electrical energy consumed by industry is used by the millions of electrical motors installed worldwide [14]. Large electric motors, with more than 375 kW, are usually medium voltage motors and they represent just 0.03% of the electric motor stock in terms of numbers. However, they account for about 23% of motor power consumption, representing a significant fraction of global power with about 10.4% [10].

Additionally, the energy cost is increasing and energy consumption is becoming ever-more important for economic and environmental reasons. Therefore, with medium-voltage (MV) motors consuming around 10% of the world's energy, they are a clear target for energy improvement measures not just to limit energy bills but also to comply with tightening regulations [13].

On the other hand, only a small amount of currently installed medium-voltage motors are controlled by variable speed drives (VSD) [3, 7]. This opens the door for introducing efficient adjustable speed drives in industrial applications. This technology will help the industry around the world save energy without compromising performance or production efficiency. [13] shows that variable speed drives, by precisely matching speed and torque to the requirement can offer significant savings even though the speed reduction is often quite small. For example, a pump's power consumption can be cut in half with a 20% reduction in speed.

Therefore, the medium voltage variable speed drives market is mainly driven by increasing energy costs and by the energy-saving potential offered by variable speed drives. The growing focus towards industry 4.0 also drives the market for industrial motors and VSDs [14]. Industrial automation is a crucial instrument for improving the production efficiency in the manufacturing sector, which is expected to show a solid growth during the next five years. In 2021, the medium voltage drive market was valued at more than USD 1.5 billion, would reach USD 1.95 billion in 2028, and is expected to grow at a compound annual growth rate of around 3.8% between 2022 and 2032 [15].

1.2 Considered application and specifications

This section will specify the application and specifications studied in the context of this doctoral thesis in accordance with the market strategy of Schneider Electric. The main application relates to the supply of medium voltage electric motors of 4.16 kV and 6.6 kV. These power supplies (power drives) are intended to generate an amplitude voltage and a variable frequency at the terminals of the machine using an inverter. The inverter is supplied by a MV grid and generally of the same voltage as the machine itself. As part of this study, an active front end (AFE) is connected to the network to supply the inverter. In this configuration, the machine operation is possible in all four quadrants and the amplitude of the input and output voltages are, generally, close.

The powers considered will range from 500 kW to several MW depending on the motor voltages and the semiconductors available. The targeted market segment is high-performance drives, with output frequencies up to typically 50 or 60 Hz depending on the geographic location, but certain applications may require even higher output frequencies.

1.3 State of the art of converter topologies

The need for energy savings and the increase of raw materials market results in an increased demand for medium voltage drives over a wide range of powers and voltages, tipically 0.3 to 32 MVA and 2.3 to 13.8 kV [4]. Nevertheless, most of the installed MV drives are in the power range of 1 to 4 MW with voltage ratings from 3.3 to 6.6 kV [1].

Therefore, multilevel converters have found great interest and have been widely studied in industry and academia during the last decades. Multilevel topologies development associated to the growth of voltage and current ratings of fast power semiconductors, such as IGBT (Insulated Gate Bipolar Transistor), have allowed the evolution of medium-voltage and high-power solutions. The cost of semiconductor devices, the reliability, the power density and the efficiency are the main criteria used for MV drives [1–9].

Figure 1.1 presents a simplified classification of the converter families used in medium and high-power applications [5]. In the scope of this doctoral thesis, the presentation of the topologies state of the art will be limited to the multilevel voltage source converters (VSC).

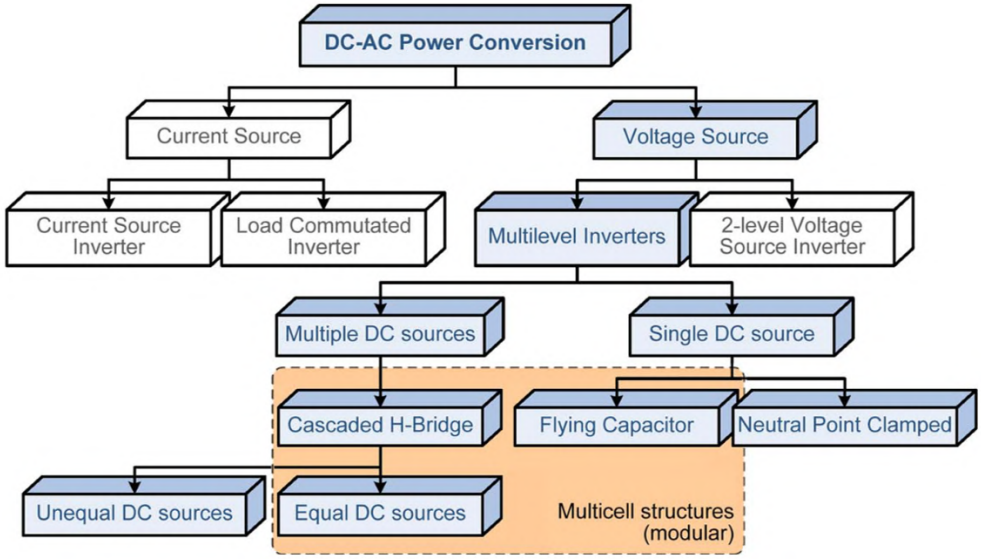


FIGURE 1.1: Classification of converters for medium and high-power drives [5].

1.3.1 Classic multilevel topologies

Multilevel voltage source converters topologies can be divided into classical and advanced topologies. This section will focus in the classical topologies, i.e., the 3-level neutral-point clamped (3L-NPC), the 4-level flying capacitor (4L-FC) and the cascaded H-bridge (CHB) (Figure 1.2).

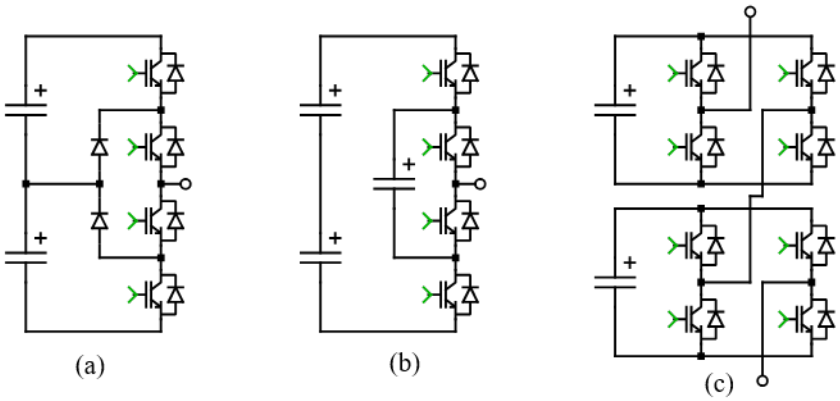


FIGURE 1.2: Classic multilevel topologies: (a) 3L-NPC; (b) 3L-FC; (c) CHB.

The CHB converters are multilevel structures formed by the series connection of two or more power conversion cells [3–5]. By associating a higher number of cells in series, it is possible to increase the voltage level, the power level and, remarkably, the quality of the waveforms thanks to the interleaving of the controls. In addition, the different cells of a CHB converter can be supplied with different voltages which reduces the number of redundant switching states but increases the number of voltage levels generated by the converter. The main advantages of the CHB converter are the modularity and the possibility to use low voltage semiconductors (cheap and very efficient) to obtain high output voltages. However, the main disadvantage is the need for a complicated and bulky transformer. This transformer can account for 30 to 50% of the system's size and 50 to 70% of its weight; so it increases the cost of raw material and can be a source of significant losses [1].

The NPC converter was first introduced in the early 1980s [16, 17], offering a simple solution to extend the voltage and power ranges of existing 2-level voltage source converters, limited by the blocking voltage of the power semiconductors [4]. Therefore, this topology found special interest for MV drive applications. This topology added the third level (zero level) to the voltage output waveform helping to reduce its harmonic content. This concept can, to some extent, be scaled to any number of levels increasing the number of bus capacitors and clamping diodes [3]. Nevertheless, due to the increasing difficulty of voltage balancing and a dramatic increase in the number of clamping diodes needed to share the voltage, the NPC inverter is in the industry almost exclusively limited to three levels only [5]. This topology uses 6.5 kV semiconductors for the 4.16 kV inverter and series-connected 4.5 kV semiconductors for the 6.6 kV inverter.

The FC topology (also known as capacitor-clamped inverter) was first introduced in the early 1990s [3, 4, 18, 19]. This topology has some of the characteristics of the NPC topology presented earlier, except that flying capacitors are used to guarantee the voltage distribution. In the 3-level FC topology, the intermediate voltage level is produced by connecting the load to the positive or negative bar through the flying capacitor; without ever connecting to the midpoint of the DC bus. This eliminates the need for DC bus voltage balancing of the NPC topology. On the other hand, voltage balancing of the flying capacitor must be guaranteed, which has been addressed in various ways in the literature [20–25]. The main advantages of the FC over the NPC are its modularity (topology and control can easily be derived for more voltage levels and higher power ratings), symmetrical loss distribution, and the ability to handle unidirectional currents [2]. The main drawback of the FC converter is the size of the flying capacitors, which increases in the inverse proportion to the switching frequency. Therefore, the high cost and volume of the flying capacitors make this topology unusable at low and medium switching frequencies [3]. This topology uses 6.5 kV semiconductors for a 3L-FC 4.16 kV inverter and 6.5 kV semiconductors for a 4L-FC 6.6 kV inverter.

1.3.2 Advanced topologies

Numerous new topologies have been proposed in the literature. Nevertheless, the majority of them are variations or a hybridization of the three classic topologies previously presented [5]. Among the recent topologies, the following topologies have found practical application and are commercialized by manufacturers. The 3-level active NPC (3L-ANPC), the 5-level active NPC (5L-ANPC), the 4-level nested NPC (4L-NNPC), the 4-level T-type NPC (4L-TNPC) and the 5-level multipoint clamped (5L-MPC) (Figure 1.3).

The 3L-ANPC topology is an improvement of the presented 3-level NPC to face the unequal share of losses between each converter leg's inner and outer switches [2]. It can actively control the loss distribution between the switches replacing the neutral clamping diodes with clamping switches. However, due to the replacement of the diodes by active switches, this topology presents a higher number of semiconductors devices compared to the 3L-NPC. Therefore, this topology increases the cost and complexity of the structure for the same number of output levels. Like the 3L-NPC, this topology uses 6.5 kV semiconductors for the 4.16 kV inverter and series-connected 4.5 kV semiconductors for the 6.6 kV inverter.

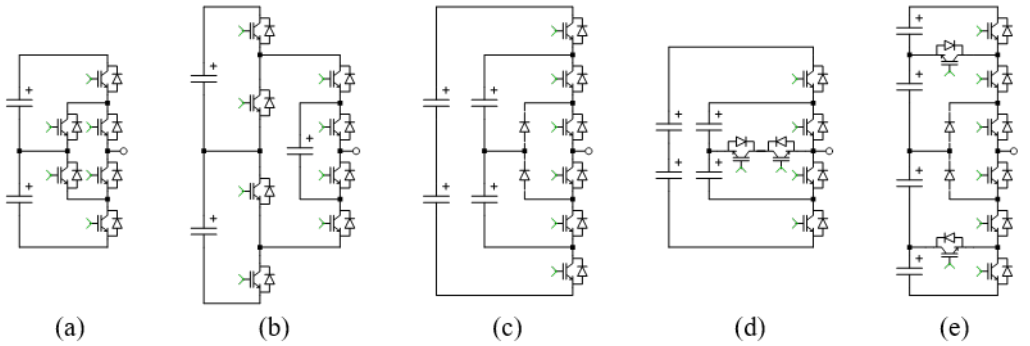


FIGURE 1.3: Advanced topologies: (a) 3L-ANPC; (b) 5L-ANPC; (c) 4L-NNPC; (d) 4L-TNPC; (e) 5L-MPC.

Afterwards, a variation of the ANPC concept was proposed combining a 3L-ANPC leg and a 3L-FC power cell between its inner switching devices, generating the 5L-ANPC [2, 26, 27]. The addition of the FC cell increases the number of output levels to 5. The flying capacitor of this topology is controlled to $V_{DC}/4$. The main drawback of the 5L-ANPC topology is using different voltage ratings for the outer and inner devices. The outer devices need two times the rated voltage compared to the inner ones. [26] uses 3.3 kV semiconductors for the 4.16 kV inverter and 4.5 kV semiconductors for the 6.6 kV inverter. The outer switches use two series-connected devices.

A 4L-NNPC is a combination of the NPC topology with the FC topology [28]. The flying capacitors are controlled to one-third of the dc-link voltage. The advantage of this topology compared to other 4-level topologies, such as a 4L-NPC and a 4L-FC, is the reduction in the number of semiconductors devices. The main drawback of this topology is the control of the flying capacitor voltage that can only be performed at the output frequency, increasing the FC size. This topology uses 4.5 kV semiconductors for the 4.16 kV inverter and 6.5 kV semiconductors for the 6.6 kV inverter.

The 4L-TNPC topology used the same concept as the previously presented topology; however, it combines the T-Type (TNPC) and the FC topology [29]. Likewise, in the previous topology, the FCs are charged to one-third of the dc bus voltage. The main drawback remains the control of the flying capacitor voltage performed at the output frequency. This topology uses 6.5 kV semiconductors for the 4.16 kV inverter and series-connected 4.5 kV semiconductors for the 6.6 kV inverter. Therefore, this topology does not always represent an advantage in the number of used semiconductors when compared with the 4L-NNPC.

The 5L-MPC is an evolution of the 3L-NPC to output 5 levels using a reduced number of semiconductors compared to the 5L-NPC [30]. The main drawback of this topology is the complexity of the balance of the dc-link capacitors. Some strategy has been proposed by [30], but it depends on a high capacitor value in the LCL filter to ensure the dc bus capacitors' balance. This topology uses 3.3 kV semiconductors for the 4.16 kV inverter and 4.5 kV semiconductors for the 6.6 kV inverter (some devices are series-connected).

1.4 HV semiconductors

The previous topologies that have been presented, except for the CHB, are based on high voltage (HV) semiconductors, sometimes series-connected, to withstand the necessary DC bus voltage. Moreover, due to the working principles of these topologies, most or even all the semiconductors switch continuously at a high frequency.

However, one of the main problems of high voltage (HV) semiconductors (IGBTs and diodes), rated between 3.3 kV and 6.5 kV, is still the limited switching performance. Figure 1.4 shows, in blue, the switching energy evolution for the same current (here 450 A) with the semiconductors rated voltage using 1.7 kV IGBTs as reference. By multiplying the rated voltage by two, i.e., for a 3.3 kV, the switching energy is multiplied by a factor of four. The switching energy can be multiplied by eight, comparing the reference IGBT with a 6.5 kV one.

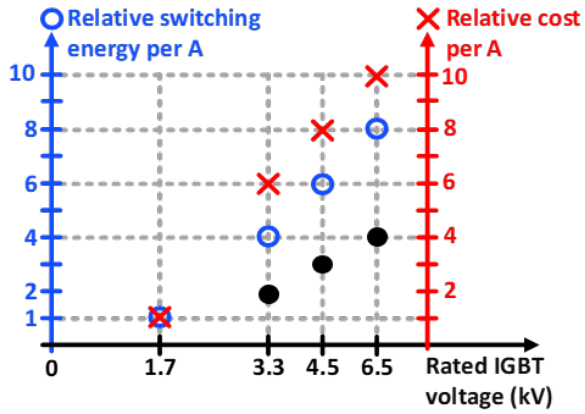


FIGURE 1.4: Evolution of the switching energy and cost of IGBTs as a function of their nominal voltage. The losses and cost for the series connection of 1.7kV IGBTs is represented by the black dots, .

Multiplying the high switching energies of the HV semiconductors and the high switching frequencies, the switching losses of the HV semiconductors devices are responsible for the major portion of the device losses [6]. The direct consequence is a severe switching frequency limitation or a low efficiency if the application requires a high output frequency to drive the machine [6, 31].

Figure 1.4 shows, in red, the evolution of the price (red cross) and switching energies (blue circles) of semiconductor versus their voltage rating. The price (resp. switching energy) of a module is divided by its current rating and by the price per Ampere (resp. switching energy) of the 1.7 kV device. On the same graph, the black dots represent the evolution of both the price and switching energies of 1.7 kV devices in series. It can be seen that 1.7 kV devices in series allow a significant reduction of switching energy, and the advantage in terms of cost is even bigger showing their non-linearity with the increase of the rated voltage .

As cost, efficiency and power density are essential characteristics targeted for MV drives [1–6] and to get around the limited switching performance of HV semiconductors, architectures/topologies that reduce the number and the stress of high voltage semiconductors devices need to be studied.

1.5 Multiplexed topology

Some topologies using the mutualization of some elements have been proposed in the literature to limit the number of semiconductors [32, 33]. These topologies share only the outer cell of the 3-Level Flying capacitor within the three phases (Figure 1.5). Consequently, this approach needs a dedicated leg for each phase that still has to generate the entire full voltage. Therefore, it can be considered a variant inside the multiplexed converters family.

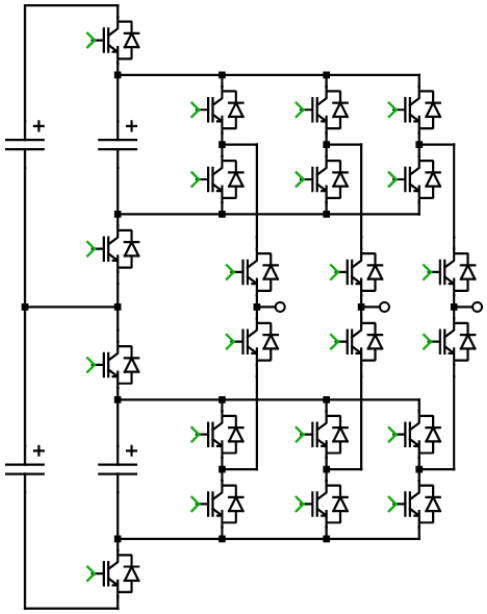


FIGURE 1.5: A five-level converter with common flying capacitors.

A hybrid 2/3 level converter (Figure 1.6) has been proposed by [34] and may be considered the first appearance of a converter of the multiplexed family. This converter is composed of two 2-level choppers and a 2-level output inverter. This topology produces an output waveform that can vary between 2 and 3 levels, hence its name, and therefore cannot be considered a classical 3-level converter. Some improvements have been realized in the carrier-based modulation for this topology [35], reducing the calculation effort of the algorithm for generating the same results. This topology is also referred in the literature as a sparse neutral point clamped inverter [36]. An extensive study has been realized recently on the space vector modulation and the performances of this topology applied for industrial variable speed drives [36].

The authors in [37] have improved this concept by proposing a so-called "multiplexed" configuration. The term multiplexed refers to the operating principle of the introduced topology. The common stage composed of three choppers (DC-DC converters) produces the maximum, intermediate and minimum voltage of the three phases. The independent stage (DC-AC converter) acts as a multiplexer connecting the voltages generated by the choppers to each of the three phases. Hence the name of the converter: multiplexed choppers. The authors have described several variants of the proposed structure.

The main advantage of this topology applied to high power drives, compared to

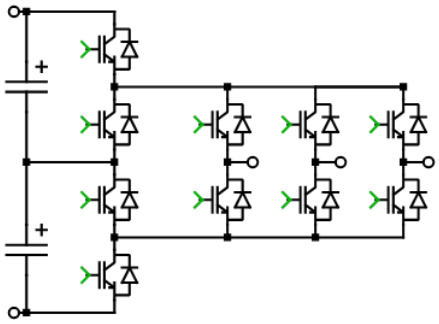


FIGURE 1.6: A hybrid 2/3 level converter (sparse neutral point clamped inverter).

the more standard multilevel topologies, is the reduction of the amount of high-frequency and high voltage semiconductors having the potential to reduce the total cost of the converter. On the other hand, the proposed converters need the use of bus balancer circuits, increasing the complexity and penalizing the solution's cost and efficiency.

Furthermore, a variation of this topology has been studied at Schneider Electric [38, 39]. It has been shown that this topology allows reducing the stresses on some semiconductors; switching is mainly realized by the chopper stage which uses components with a reduced voltage rating, so losses and cost are reduced. This advantage can be decisive in MV applications.

1.6 Objectives

This doctoral thesis focuses on new topologies of variable speed drives and their control system to offer more efficient systems. The limited dynamic performance of MV semiconductors (between 3.3 kV and 6.5 kV), greatly limits the switching frequency and thus the quality of the waveforms.

To avoid this problem, Figure 1.7 represents a new architecture of the multiplexed family of converters for the inverter stage that has been patented during previous studies [40]. This stage can be bidirectional in power and the study will focus on the rectifier and the inverter, which will have a similar structure but different constraints. Cost, performance and power density are key features targeted for these products that need to fit the previously presented specifications.

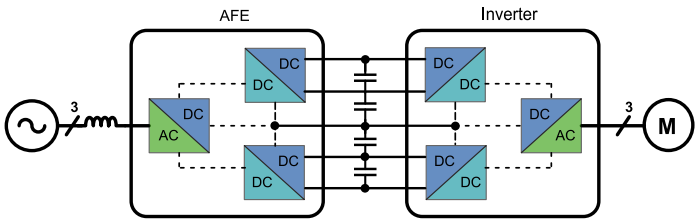


FIGURE 1.7: Power drive application conversion architecture (active front end + inverter) patented by Schneider Electric.

The objective of the thesis is to study and validate the topology with the aim of an industrial realization, to study all the of operation and to explore the various control laws associated with the converter for variable speed drives. Finally, a number of

key technological points will be studied in order to validate the concept experimentally. The two key points are the series connection of power semiconductor devices and the layout of the structure.

Chapter 2

Multiplexed Topology

2.1 Introduction

The objective of this chapter is to introduce the family of multiplexed choppers converter topologies. First, the general architecture of this family of converters will be presented with its evolution with time and different applications. Secondly, different structures for 4.16 kV and 6.6 kV power drives will be studied in order to fulfill the application requirements. Finally, the proposed structures will be compared with the better-established topologies, the 5-level ANPC and the 3-level NPC.

Later in this work, the working principle and the modulations strategies will be explained.

2.2 Multiplexed topology

Since the arrival of the first multilevel converter structures and with the past two decades of relevant development and advances, many attempts have been made to derive new structures adapted for high-power drives. These attempts improved the overall performance of these solutions with a better waveform quality, reduced power losses, improved efficiency, power density, and reduced number of semiconductors [1, 3–5, 41].

Despite all these advances in modern topologies, the number of employed power semiconductors remains high, increasing the cost, the power losses, and limiting the reliability [37].

Some topologies that employ common parts, i.e., that share some components such as semiconductors or flying capacitors, have been proposed to overcome this problem. However, these topologies still have independent elements per phase (legs) that are needed to generate the entire phase voltage [37].

To extend this concept [37] presented the multiplexed choppers family of topologies to reduce the number of semiconductors switching at high-frequency and allow the use of cheap semiconductors for those switching at a lower frequency, thus leading to a reduction of the total cost of the converter. The proposed family of converters is composed of two main elements: a common stage (shared by the three phases) composed of high-frequency semiconductors that generate the three sinusoidal voltages and three independent stages (one per phase) composed only of semiconductors commutating at the fundamental frequency.

Figure 2.1 shows the architecture and the scheme of the multiplexed converter proposed by [37]. Although the common stages allow the reduction of the high-frequency semiconductors, [37] proposed replacing the semiconductors of the independent stage (that may seem numerous) by thyristors reducing their cost and hence the total converter cost.

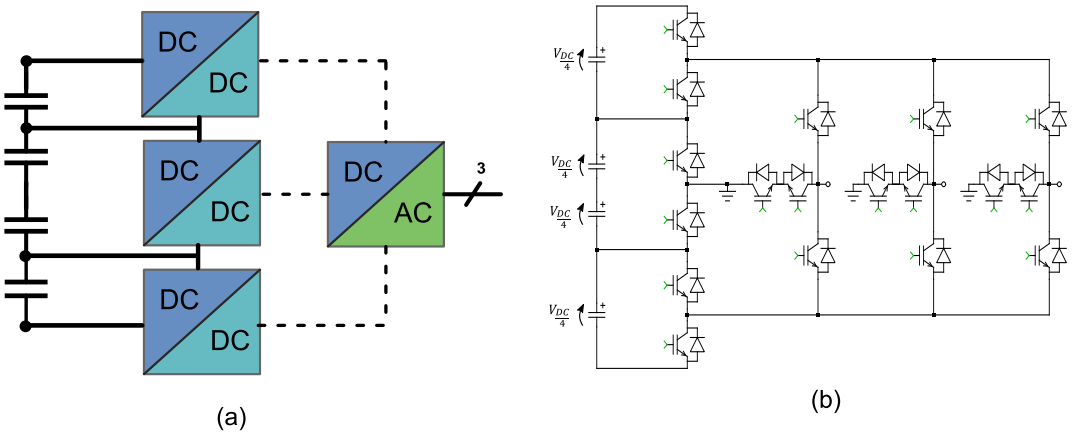


FIGURE 2.1: First proposed multiplexed choppers converter. (a) Architecture; (b) scheme.

However, the use of thyristors requires a finer commutation with the crossing of the choppers output voltage to turn on and turn off properly. To do such a voltage crossing a common stage with two independent branches has been proposed by [37].

Later [38] proposes a different inverter architecture based on the multiplexed choppers (i.e. "xPlexed") that face the limitation imposed by the thyristors. The intended inverter architecture for Uninterruptible power supply/Battery energy storage system (UPS/BESS) application is composed of two DC/DC converters that feed a DC/AC converter. Figure 2.2 shows the most generic concept of this architecture where the DC/DC converters are not directly connected to the common point of the DC bus. Some DC voltage source can be introduced between them, reducing the voltage that the chopper (consequently their semiconductors) need to withstand. This DC voltage will be referred to as a dead voltage during this work. The dead voltage can vary from zero (nonexistent) to a certain fraction of the whole bus voltage, depending on the bus voltage, the requirements of the application, the chopper topology and desired static voltage of its semiconductors. Finally, [39] proposed another different architecture for its four-quadrant applications where the common stage is common to the inverter and rectifier side. This was possible due to the close operation points of each side, which is not the case in power drive applications. Thus, the first architecture proposed by [38] will be adopted in this work due to its main advantages that fulfill the requirements of this medium voltage power drive application.

The following sections will show how the architecture has been selected to address the requirements of the targeted application.

2.2.1 Dead Voltage

The general working principle of the topology depends on the value of the dead voltage and the intersection of the output voltage of the three phases. If the dead voltage is superior to this intersection value the working principle is affected. The choppers are no longer able to produce, completely, neither the maximum nor the

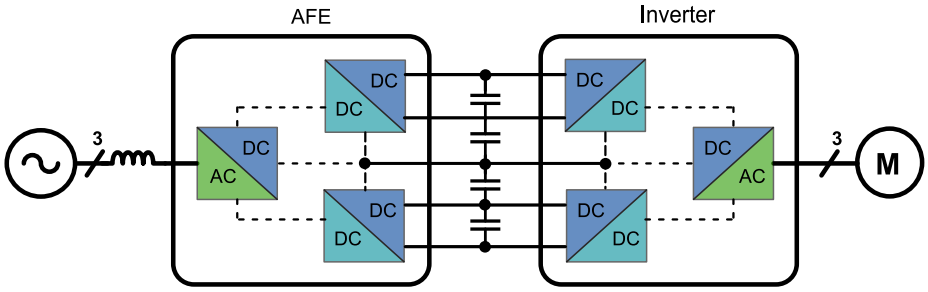


FIGURE 2.2: Power drive application conversion architecture (active front end + inverter) using multiplexed topology with dead voltage.

minimum voltage of the three phases. Thus, the inverter needs to produce, besides the intermediate voltage, at least a part of the maximum and minimum voltage. Consequently, the inverter arms switch more than one-third of the time, increasing their efforts and switching losses.

In function of the bus voltage, the dead voltage ratio and the output voltage three different working zones can be defined (Figure 2.3). The first one (in green) represents the zone where the output voltage intersection is higher than the dead voltage (Figure 2.4), so the original working principle is valid and the inverter switches one-third of the time. The second zone (in yellow) corresponds to an output voltage intersection inferior to the dead voltage but to a voltage amplitude superior to the dead voltage. In this zone, the working principle is changed. The choppers produce only part of the maximum and minimum voltage. The inverter needs to produce the intermediate voltage and the remaining of the maximum and minimum voltage. This zone reduces the efforts of the choppers because they do not switch all the time but increases the efforts of the inverter legs that need to switch more than one-third of the period. The third zone (in red) corresponds to an output voltage with an amplitude lower than the dead voltage. In this zone the choppers are saturated to zero, not switching anymore. However, the inverter switches all the time being responsible for producing the whole output voltage from the dead voltage.

Comparing Figure2.3 (a) and (b), one can observe, besides the 15% gain in the modulation depth, the influence of the third harmonic injection (THIPWM) in the operation zones compared to the sinusoidal pulse width modulation (SPWM). The THIPWM slightly increases the red area, i.e., for a given output voltage, the SPWM can have a higher dead voltage than the THIPWM and stay in the yellow zone. On the other hand, the THIPWM reduces the yellow zone and increases the green one, increasing the voltage range in which one inverter switches one leg at a time. Figure 2.4 shows an example of the zones as a function of the phase output voltage evolution for a dead voltage (black) of 33%.

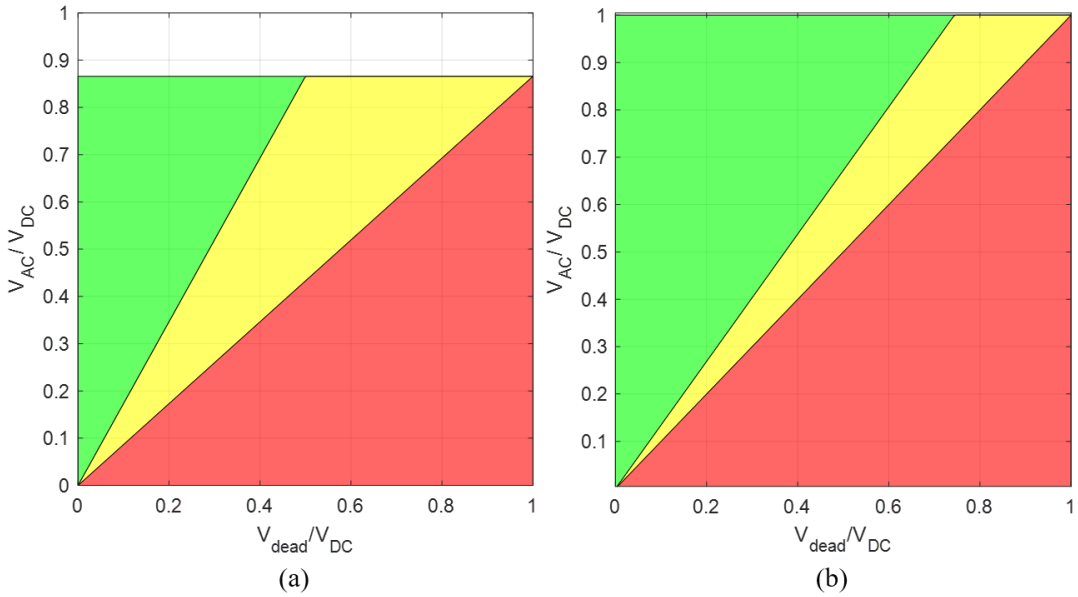


FIGURE 2.3: Operation zones for different output voltage as a function of the dead voltage and bus voltage ratio. Green: one inverter legs switches at a time. Red: Three inverter legs switching at the same time. Yellow: more than one legs switches at a time. (a) Sinusoidal PWM; (b) third harmonic injection PWM.

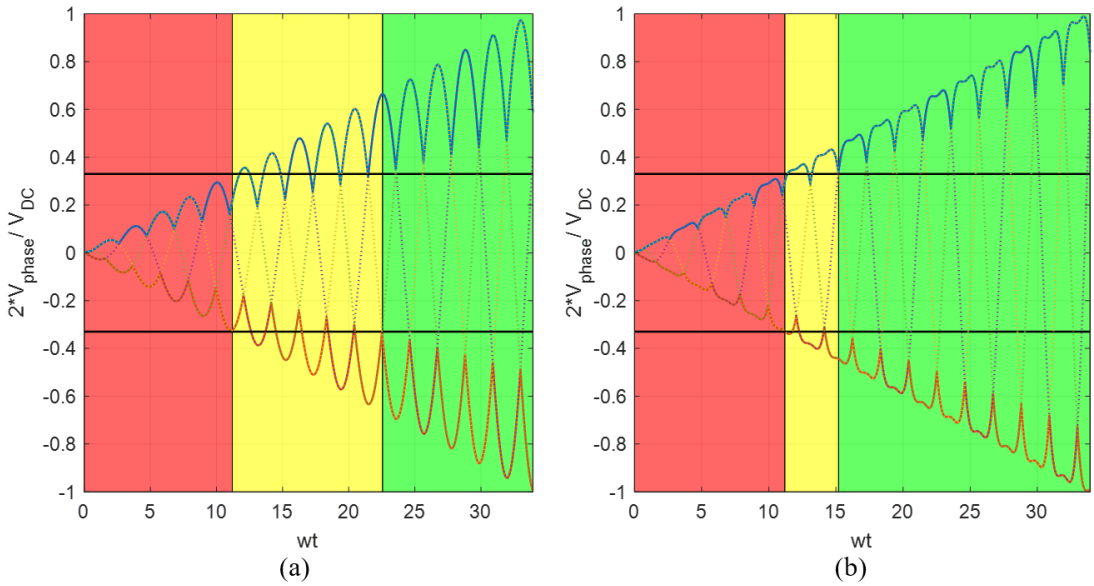


FIGURE 2.4: Operation zones as a function of the phase voltage for a 33% dead voltage. Green: one inverter legs switches at a time. Red: Three inverter legs switching at the same time. Yellow: more than one legs switches at a time. (a) Sinusoidal PWM; (b) third harmonic injection PWM.

The use of a dead voltage is mainly interesting because it allows to use less semiconductors and/or to reduce the rated voltage and the switched voltage of the semiconductors of the chopper stage. Consequently, reducing the cost and the losses of this stage. The higher the dead voltage, the more significant these advantages. As will

be seen later in this work, the chopper stage always conducts current values that are close to the amplitude of the output current, and reducing the voltage rating of the chopper semiconductors will contribute to reduce the conduction losses of this stage

However, the use of a dead voltage has some drawbacks in the inverter stage. The first one is linked to the different working zones and concerns mainly the machine side, in which the output voltage can vary from zero to the nominal value. Depending on the operation point (lower modulation depth) and the dead voltage, the inverter will operate in a zone where the inverter legs switch more than one-third of the time and possibly all the time. This will significantly increase the inverter losses because it is composed of high voltage semiconductors. Besides that, because the inverter switches an already switched voltage, for low modulation depth, the inverter can switch the minimum voltage that the chopper can deliver: the dead voltage. Therefore, at low modulation depth, the dead voltage increases the switched voltage and consequently the switching losses.

Finally, the main drawback of the use of a dead voltage is the creation of floating points that will need DC bus balancers circuits. Considering a back-to-back configuration (AFE + inverter) and the important amplitude of points that the inverter can operate, the balancer circuit needs to conduct currents comparable to the converter ones. Section 2.2.3.2 will show the unbalance current the bus balancers need to face and some possible balancer circuits.

2.2.2 Structures for 4.16 kV inverter

The structure for a 4.16 kV inverter needs a bus voltage of 6.5 kV. The bus voltage is given by equation 2.1 considering third harmonic injection to minimize the bus voltage (gain of 15% [42]) and considering a grid voltage variation of $\pm 10\%$.

$$V_{DC} = 1.1 \cdot \sqrt{2} V_{AC} \tag{2.1}$$

V_{DC} and V_{AC} denotes the bus voltage and the nominal grid/motor voltage, respectively.

The main objective in defining the topologies that will be used for the inverter legs is to minimize the number of high-voltage semiconductors (minimizing the cost and the switching losses). The inverter legs will use 3-level topologies to improve waveform quality without significant addition of semiconductors. For this bus voltage, a 3L-NPC leg requires only two diodes in addition to the semiconductors of a 2-level leg.

For the inverter, three different 3-level topologies have been analyzed: a 3-level neutral point clamped (3L-NPC), a 3-level T-type neutral point clamped (3L-TNPC) and a 3-level active neutral point clamped (3L-ANPC) (Figure 2.5). Considering the bus voltage and the recommended static voltage for these components [43, 44], these inverters will be composed of 6.5 kV semiconductors. The use of 3.3 kV semiconductors connected in series is not interesting because it does not bring a reduction of switching losses or cost (Figure 1.4). For the NPC and the ANPC inverter, each semiconductor needs to withstand half the bus voltage, i.e., a single 6.5 kV is enough. The same voltage is applied to the semiconductors of the clamping leg to the TNPC inverter. However, the vertical(outer) leg of the TNPC inverter needs to withstand the whole bus voltage; thus, 6.5 kV semiconductors need to be series-connected.

Table 2.1 compares the number of semiconductors, IGBTs and diodes, for a single leg of each of the three inverters. It is important to know that in terms of cost two diodes will be considered equivalent to one IGBT during this work.

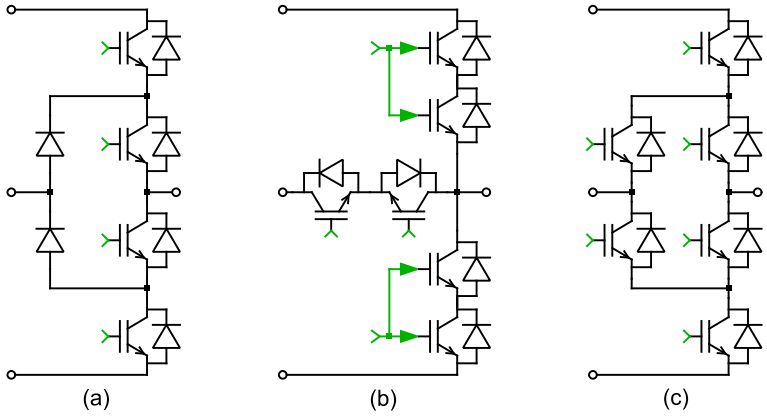


FIGURE 2.5: 3-level inverter topologies. (a) 3L-NPC; (b) 3L-TNPC; (c) 3L-ANPC.

A 3-level flying capacitor (3L-FC) inverter is not considered because the chopper stage supplies the inverter stage with a chopped and non-filtered voltage which is incompatible with the flying capacitor voltage balance and, consequently, this topology.

Table 2.1 shows that the NPC solution uses fewer semiconductors than the other two. Due to the series connection in the TNPC it loses some of its advantages [45] compared to the NPC having equivalent conduction losses and representing a higher semiconductors cost. Therefore, the chosen topology for the inverter stage will be the NPC.

TABLE 2.1: Number of semiconductors per inverter leg (diode counts as half an IGBT due to their price ratio).

Topology	IGBT	Diode	Total
3L-NPC	4	2	5
3L-TNPC	6	0	6
3L-ANPC	6	0	6

For the chopper stage it is interesting to compare a 2-level converter and multilevel converters of maximum 3 levels to limit the complexity and the number of semiconductors used. A 2-level chopper demands the use of 6.5 kV semiconductors or 3.3 kV series-connected semiconductors to withstand half the bus voltage (3.25 kV). However, the chopper stage is subject to high switching efforts: the chopper switches permanently (differently from the inverter stage) at a frequency equal to the inverter one, and the current switched by the chopper presents during most of the time a value equal to the sum of the current of two phases. And, as seen before, neither the 3.3 kV semiconductors nor the 6.5 kV are well adapted for such high switching frequency and efforts. Moreover, even though the 3.3 kV semiconductors in series are better adapted to higher switch frequency than the 6.5 kV ones, this solution is not economically attractive either.

To use well-adapted semiconductors the solution is to use a multilevel topology for the chopper stage, more precisely, a 3-level one. The three topologies compared

for the inverter stage (NPC, ANPC, T-NPC) and the 3-level flying capacitor can be compared to find a suitable solution for the chopper. Nevertheless, the first three topologies create an intermediate point in the DC bus for the clamping. This intermediate point will produce some unbalance between the two parts of the bus [4, 5], considering that the output current most of the time keeps the same signal. This unbalance cannot be compensated by the other chopper that will be back-to-back (in a 4-quadrant solution) because they can have very different operation points between the rectifier and the inverter side.

Furthermore, it has been proven that in these current conditions the NPC and the T-type chopper are not able to balance the bus voltage [46], so they are discarded. On the other hand, the ANPC can balance the bus voltage but needs an extra LC network, adding extra components aside from the extra transistors. Finally, the flying capacitor does not need this intermediate bus point eliminating the bus balance problem and uses less semiconductors than the previous solutions but adds extra capacitors. The flying capacitors size is directly linked and inversely proportional to the switching frequency. Using an adequate switching frequency they are less bulky, complex, and expensive than the needed LC network for the ANPC, turning out to be a more interesting solution.

Using a 3-level flying capacitor topology two voltage ratings of semiconductors are interesting: 3.3 kV or 1.7 kV series-connected semiconductors. The 3.3 kV, however, are limited in terms of switching frequency, even though they benefit from the FC property and can switch at half of the switching frequency for the same output frequency [18, 22, 47] as the 2-level topology. Moreover, there is no gain in cost using a 3.3 kV semiconductors-based 3-level chopper compared to a two-level chopper. On the other hand, comparing the switching energies, the 1.7 kV is much more suitable for higher switching frequencies required to reduce the size of the flying capacitors. Later in this work, one can observe that they switch at the same frequency as the inverter legs, resulting in a reduced volume of capacitors. Moreover, regarding the cost comparison between them (Figure 1.4), a series connection of lower-rated voltage semiconductors (1.7 kV) is also, economically, more interesting than using a single 3.3 kV one. Finally, a multilevel chopper switching at such a frequency will help to increase the waveform quality and reduce the filter size on the grid side.

To conclude, regarding the results of this comparison, the most interesting variation of this multiplexed structure for the 4.16 kV is a 3-level NPC inverter supplied by two 3-level flying capacitors choppers. Figure 2.6 shows the schematic for this power drive.

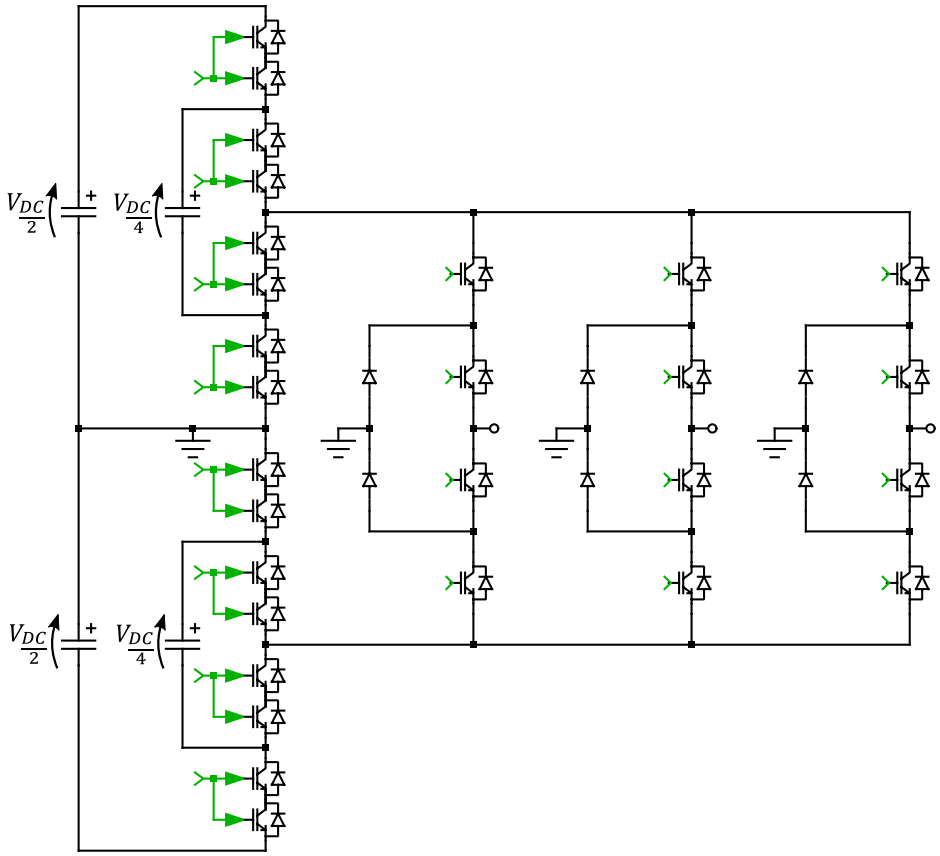


FIGURE 2.6: Proposed multiplexed DC-AC inverter with 3-level flying capacitor chopper topology and 3-level NPC inverter topology for 4.16 kV power drive. Chopper is composed of 1.7 kV semiconductors series-connected and the inverter is composed of 6.5 kV semiconductors.

2.2.3 Structures for 6.6 kV inverter

Using third harmonic injection and considering a grid voltage variation of $\pm 10\%$ a bus voltage of 10.3 kV (Eq. 2.1) is needed for the 6.6 kV structure. The inverter topology for this structure will be the same as the previous one, a 3-level NPC. The main conclusions from the 4.16 kV NPC inverter are still valid in this case. The difference is the need of series-connected 4.5 kV semiconductors all over the inverter. For example, if a T-NPC had been chosen, four 4.5 kV semiconductors needed to be series-connected in the vertical arm and two sets of two semiconductors back-to-back connected for the clamping arm.

One advantage of this topology that makes it easier when using series-connected semiconductors in the inverter stage is the capability to switch at reduced voltage, which gives some margin if the voltage balance is not perfect. This property will be explained in the next chapter.

For the chopper stage, however, there are more possibilities that need to be evaluated than for the previous structure: it is also interesting to analyze the possibility of adoption of the dead voltage. A two-level chopper will be avoided due to the previously discussed drawbacks compared to the 3-level one. Considering the conclusions from the first studied structure, the remaining solution is a 3-level flying

capacitor chopper combined with a given value of dead-voltage or a 4-level flying capacitor without dead-voltage.

2.2.3.1 Structure with dead voltage

Considering the adoption of a dead-voltage (Figure 2.7), two main options will be analyzed: a dead-voltage of resp. 33% and 50% of the bus voltage. With a dead-voltage of 33% the voltage that each chopper needs to withstand is 3.45 kV, i.e., nearly the same voltage that for the 4.16 kV inverter. Therefore, the chopper used in this case will be the same, a 3-level flying capacitor with 1.7 kV semiconductors in series. For the 50% dead voltage each chopper will withstand around 2.6 kV. Thus, the use of 1.2 kV semiconductors in series is possible, giving some gain in terms of the chopper losses and the cost of the semiconductors. Moreover, a bigger dead-voltage also means that the flying capacitor voltage will be reduced, reducing the stored energy. On the other hand, it represents a reduction of the operation zone in which there are benefits for the inverter side.

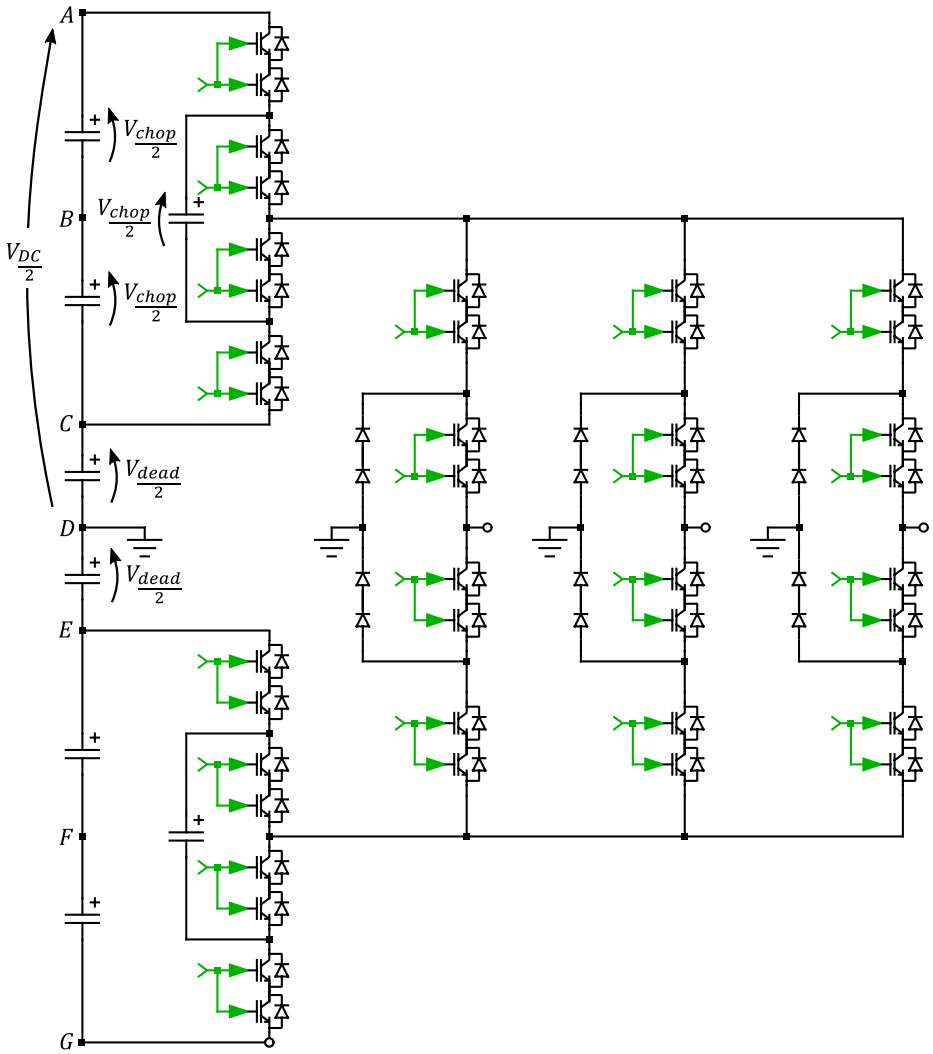


FIGURE 2.7: Proposed multiplexed DC-AC inverter with 3-level flying capacitor chopper topology, 3-level NPC inverter topology and dead voltage for 6.6 kV power drive. Chopper and inverter are composed of 1.7 kV and 4.5 kV semiconductors series-connected, respectively.

Moreover, as discussed before, adopting a dead voltage also needs bus balancer circuits. This bus balancer needs to compensate the current unbalance in between the different parts of the DC bus to balance the bus voltage. To size this bus balancer in a four-quadrant structure some simulations need to be done to measure the difference between the current injected by the rectifier and the current supplied to the inverter in the floating-point of the dead voltage (node C and E of Figure 2.7). This simulation is done with the inverter being supplied with the same power that the grid is supplying the rectifier, i.e., an average power of the bus equal to zero. Besides that, it is also essential to find the worst-case scenario that will size the bus balancer. For that, the simulation has been done with the inverter side supplying the motor with nominal current and the output voltage and frequency varying at a constant ratio from zero to the nominal value.

Figure 2.8 shows the average unbalance current at the floating-point in function of the output voltage/frequency for a 6.6 kV/2 MVA inverter. One can observe that the maximum average unbalance current is close to the nominal current of the converter (175 A_{RMS}) and occurs at an output voltage close to the dead voltage. This maximum current is the current that the bus balancer needs to supply the intermediate point of the bus.

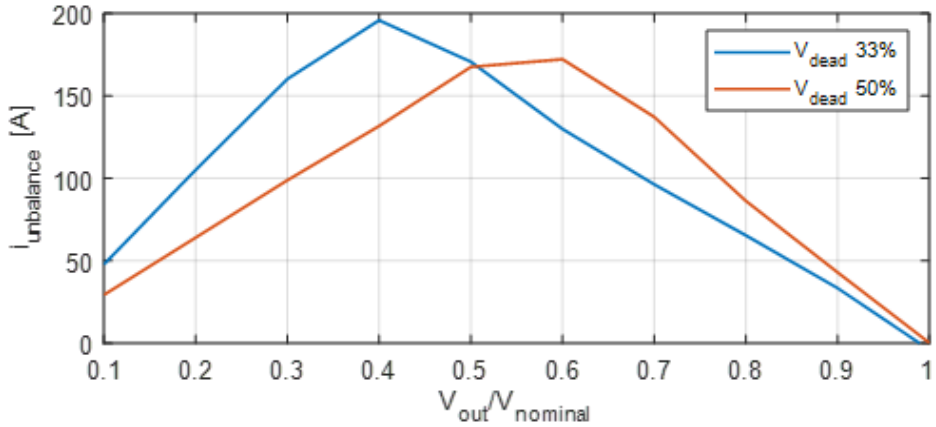


FIGURE 2.8: Unbalance current as a function of the output voltage for a 33% and 50% dead voltage in a 6.6 kV/2 MVA inverter. Unbalance current averaged at the output period.

2.2.3.2 Bus balancer circuits

In order to reduce the comparison perimeter, a simulation has been done, using Plecs software, regarding the inverter and the whole converter losses for a 6.6 kV and 2 MVA structure with a dead voltage of 33% and 50%. Table 2.4 shows the semiconductors used for this simulation. The semiconductor's electrical and thermal parameters and models used for this simulation have been taken from the component's datasheet. The heatsink temperature is fixed to 75°C, and the junction temperature evolves in function of the semiconductors losses updating their conduction and switching losses parameters. Figure 2.9 shows the losses of a single inverter arm and the whole converter for an output voltage variation from 10% to 100% of the output value, nominal current and a switching frequency of 1950 Hz.

TABLE 2.2: Power semiconductors selected for dead voltage losses influence simulation.

Power switch	V_{rated}	i_{rated}	**Manufacturer**	**Reference**
Chopper IGBT	3.3 kV	450 A	Infineon	FF450R33T3E3-DS
Inverter IGBT	4.5 kV	600 A	Mitsubishi Electric	CM600HG-90H
Inverter diode	4.5 kV	800 A	Infineon	DD800S45KL3-B5

One can see that the inverter losses are primarily influenced by the converter's dead voltage. There is a big step in the inverter arm losses when the operation point crosses the threshold corresponding to the dead voltage. I.e., there is a big switching losses step when passing from the zone where the three legs switch continuously to the zone where each leg switches one-third of the time. This step is more important for a 50% dead voltage than a 33% one, a consequence of a higher switched voltage when switching the three legs simultaneously. When operating in the zone where one leg switches at a time, the inverter losses for both the dead voltage values are close.

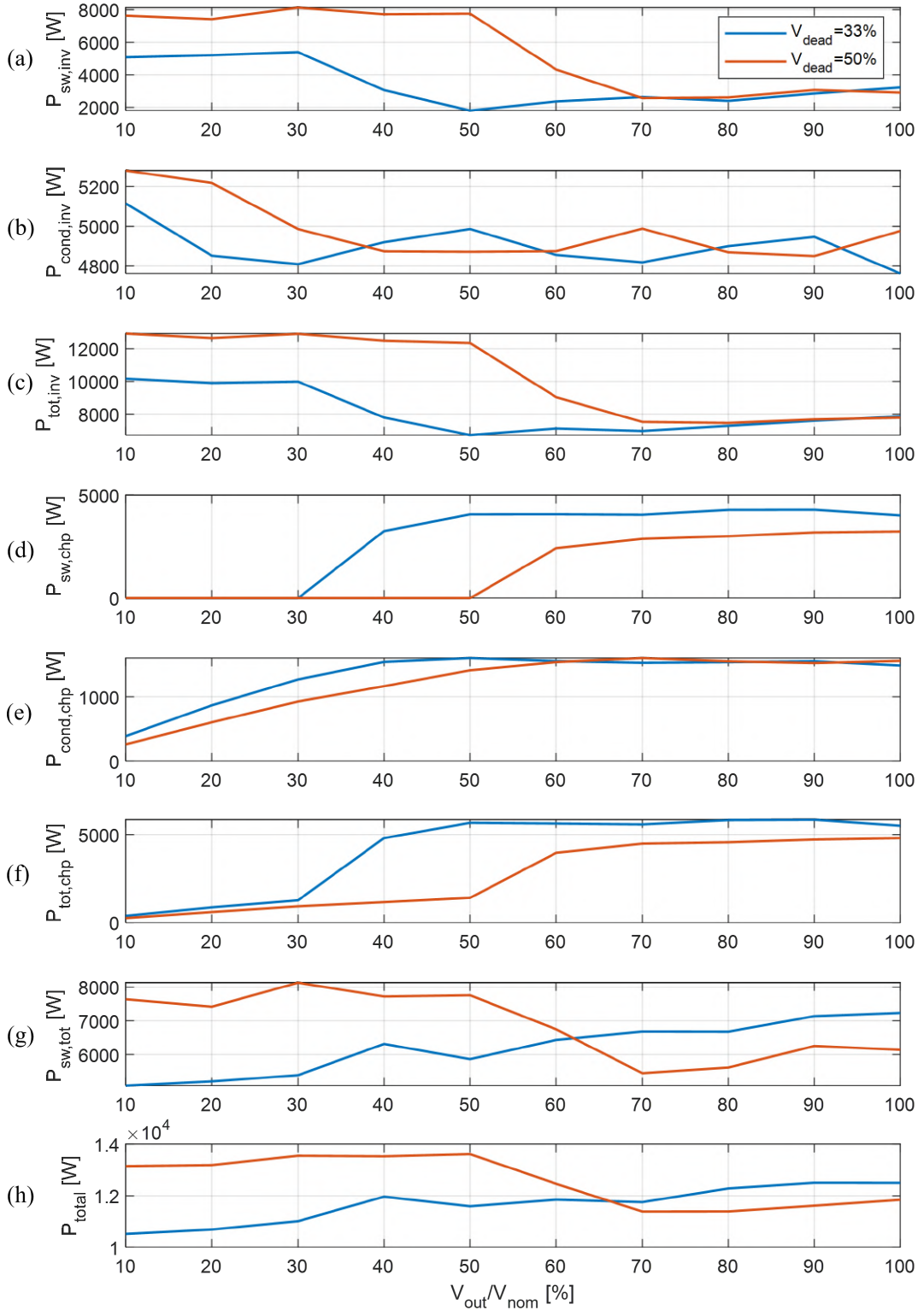


FIGURE 2.9: Simulation loss distribution of the 6.6 $kV/2$ MVA multiplexed inverter for a 33% (blue) and 50% (orange) dead voltage as a function of the output voltage. (a) Inverter switching losses; (b) inverter conduction losses; (c) inverter total losses; (d) choppers switching losses; (e) choppers conduction losses; (f) choppers total losses; (g) multiplexed inverter switching losses; (h) multiplexed inverter total losses.

This losses step is also strongly present in the total converter losses. Even though

the chopper starts to switch when the output voltage is higher than the dead voltage, the inverter losses are predominant over the chopper losses. Moreover, the inverter losses are predominant over a not optimized chopper, using 3.3 kV IGBTs and not 1.7 kV one series-connected.

Consequently, with 50% dead voltage high inverter switching losses occur for modulation depths less than 50% which is a large portion of the operating area, so this option will no longer be considered. The 33% dead voltage option is maintained because inverter switching losses at low output voltages are not so high and they occur in a narrower output voltage range.

Figure 2.10 shows two examples of circuits that can be used to balance the bus voltages of a structure with a dead voltage equal to 33%. The capacitors inside the blue rectangles represent the DC bus capacitors of Figure 2.7. The first one (Figure 2.10(a)) consists of a 4-level flying capacitor chopper connected to each half of the bus and supplying the nodes C and E with the unbalance current through the inductor L. These choppers work with a fixed duty cycle of 33% to maintain the bus voltage balanced.

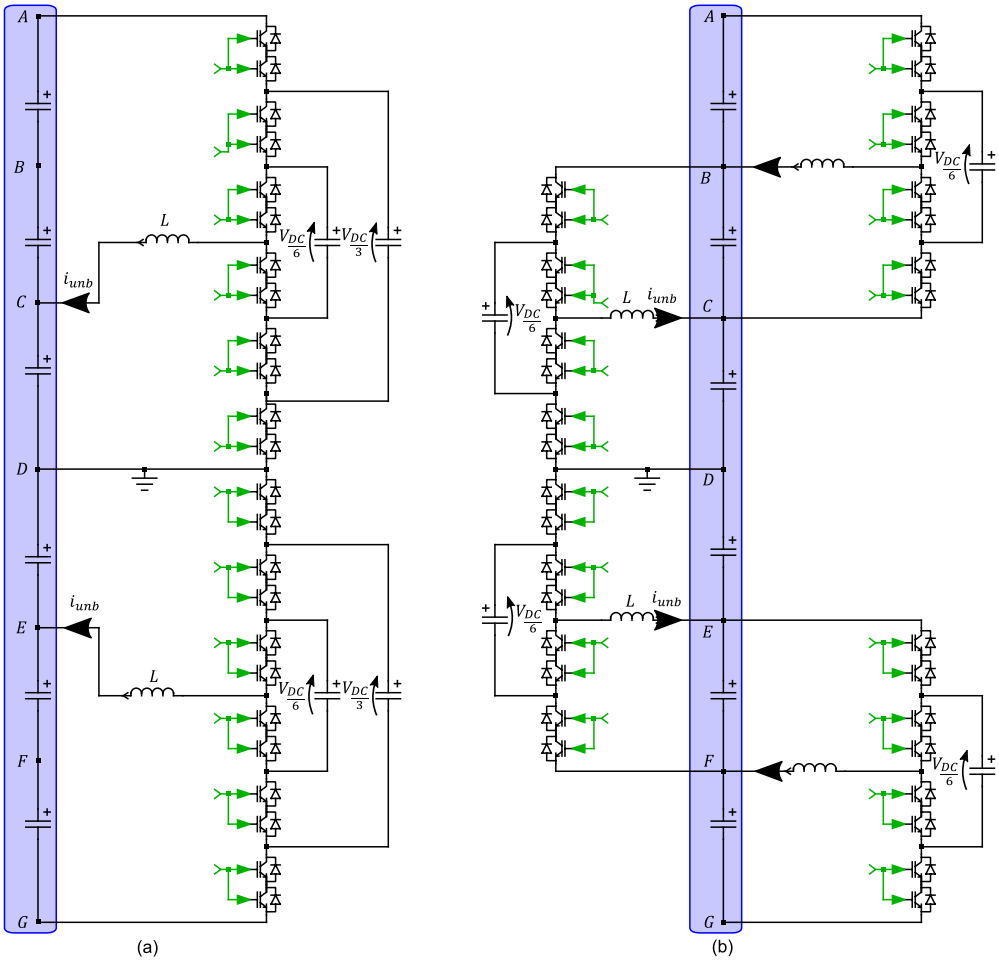


FIGURE 2.10: DC bus balancer circuits for a 33% dead voltage. Both circuits use 1.7 kV series-connected IGBTs. (a) 4-level flying capacitor based circuit; (b) 3-level flying capacitor based circuit.

The second circuit (Figure 2.10(b)) consists of an association of two 3-level flying capacitors for each half of the bus that will also supply the nodes C and E with the

unbalance current through the inductor L. In this case, each chopper works with a fixed duty cycle of 50%.

It should be noted that in both cases, the duty cycle is constant and corresponds to a minimum current ripple, which means that the inductance is theoretically not needed and can have in practice a very low value (basically designed with respect to the voltage ripple).

Since the voltage and current that these bus balancers need to withstand are the same as the choppers and they use flying capacitors, it is also interesting to use 1.7 kV semiconductors series-connected all over them.

Other bus balancer structures are presented in the literature [48–52]. However, regarding the number of extra components and the complexity they add, the comparisons will only consider the previously presented circuits.

2.2.3.3 Structure without dead voltage

Finally, if no dead voltage is adopted, a 4-level flying capacitor chopper can be used (Figure 2.11). Each chopper needs to withstand around 5.15 kV, therefore it will be composed of 1.7 kV semiconductors in series. As previously explained, the use of single 3.3 kV semiconductors is not interesting since each chopper includes two flying capacitors of which volume and stored energy should be minimized.

The comparison between the different solutions proposed here and the most common solutions of the market will be developed in the next section.

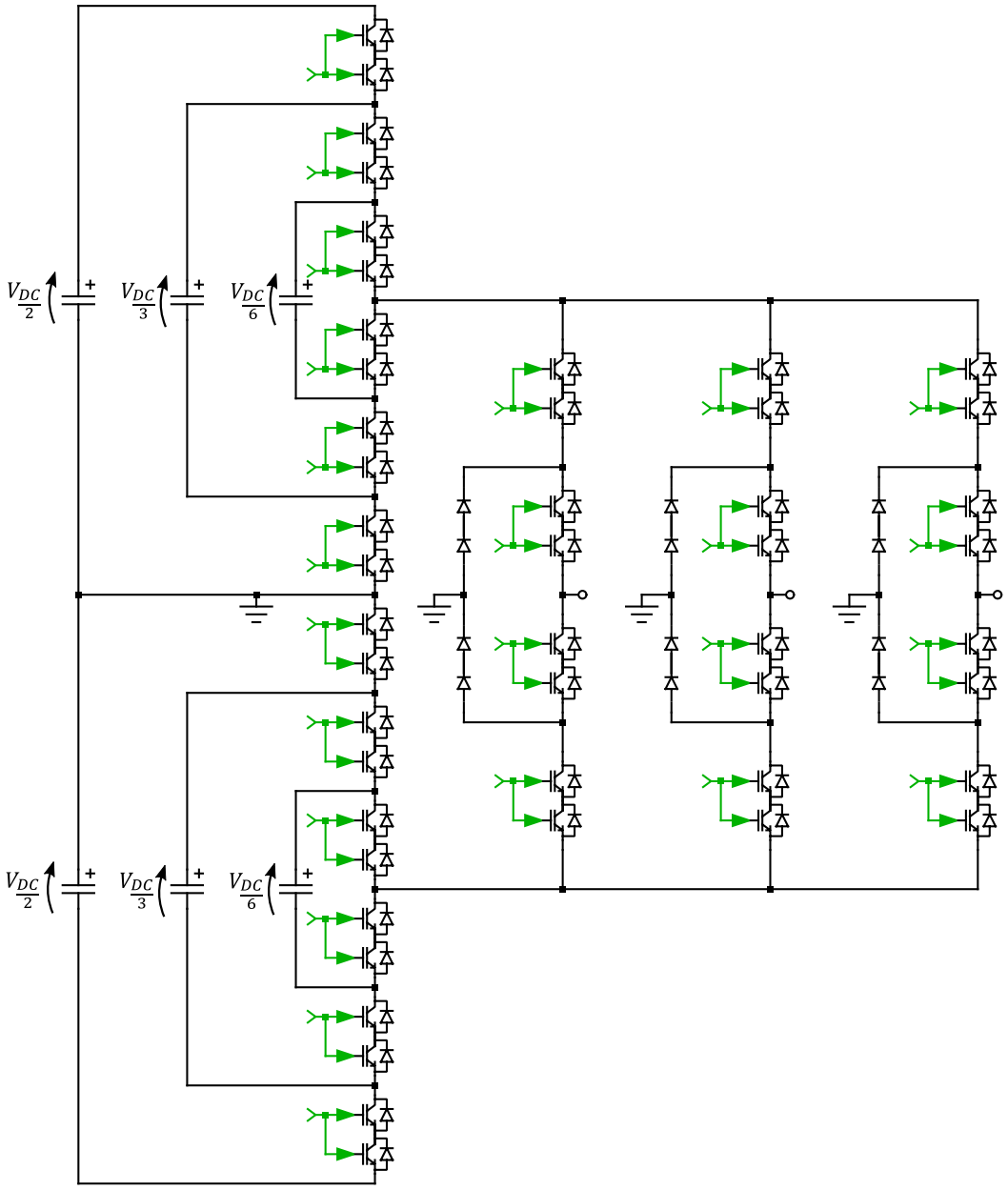


FIGURE 2.11: Proposed multiplexed DC-AC inverter with 4-level flying capacitor chopper topology and 3-level NPC inverter topology for 6.6 kV power drive. Chopper and inverter are composed of 1.7 kV and 4.5 kV semiconductors series-connected, respectively.

2.3 Comparison

The two remaining structures that have been previously presented and two of the market's leading solutions (3L-NPC and 5L-ANPC) will be compared in terms of the numbers of semiconductors, but principally, in terms of the total semiconductors cost. For this comparison, the semiconductors will have a reference current given by I and the relative cost given by Figure 1.4. The relative costs are based on actual prices provided by suppliers that are confidential to Schneider Electric. The energy ratio has also been taken from Figure 1.4. Additionally, the linearity of the cost with the current is assumed based on Schneider Electric's supplier information.

To compensate the unbalanced effort and losses of the different semiconductors of the converters and have a more homogeneous utilization factor of these components, the switches that switch continuously will have a rated current two times bigger ($2I$) than those that switch only part of the time, at a reduced voltage or at the output frequency. This choice has been made based on the results of [31, 53] that show that the switching losses of the semiconductors that switch continuously in the 3-level NPC and in the 5-level ANPC (external switches and flying capacitor switches, respectively) are roughly equal to their conduction losses or the losses of the switches that switch at the output frequency (inner switches of the 3L-NPC and outer switches of the 5L-ANPC). In other words, the semiconductors that switch permanently have around twice the losses of those that switch at low (output) frequency. Figure 2.12 shows the schematic of the 3L-NPC and 5L-ANPC inverters presenting a parallel connection when the semiconductor has a rated current $2I$.

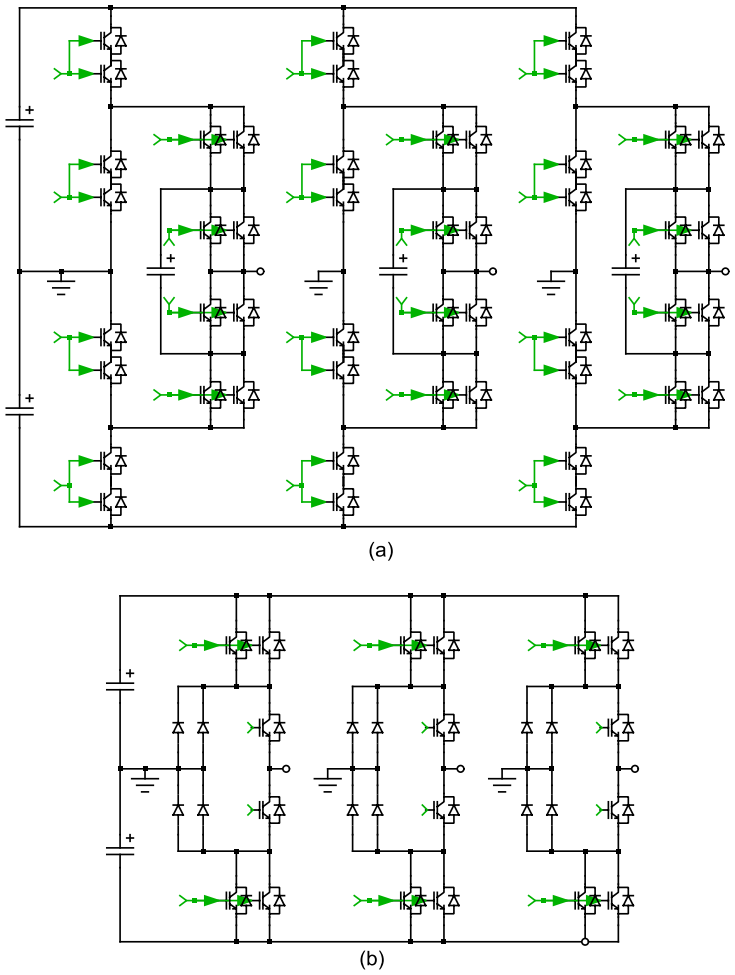


FIGURE 2.12: Two market leading solutions for comparison with multiplexed topology. (a) 5L-ANPC; (b) 3L-NPC.

To keep a fair comparison with the multiplexed topology, the chopper semiconductors, that switch all the time and at high values of current, will also use a current rating $2I$. In contrast, the inverter semiconductors that switch only a fraction of the time at reduced voltage and lower current values will use a rated current equal to I. Moreover, the bus balancer semiconductors will also use a $2I$ rated current value, considering they must withstand roughly the same current values as the choppers.

Table 2.3 shows the number of semiconductors used and corresponding cost as well as the total cost for each solution (chopper + inverter) which has been kept in the previous sections.

TABLE 2.3: Number of semiconductors and cost for the 4.16 kV and 6.6 kV multiplexed inverters.

Topology	Rated voltage	No. of SCs.	Cost/unit	Total cost
4.16 kV **xPlexed**	1.7 kV	32	1	32
	6.5 kV	15	10	150
6.6 kV **xPlexed 3L**	1.7 kV	32	1	32
	4.5 kV	30	8	240
6.6 kV **xPlexed 4L**	1.7 kV	48	1	48
	4.5 kV	30	8	240

Regarding the table, the solution that uses a 3-level chopper associated with a dead voltage is less expensive when compared to the one that uses a 4-level one. Nevertheless, this comparison is not complete without considering the semiconductors from the bus balancer that the 3-level solutions needs. Thus, Table 2.4 shows the number of semiconductors used with their associated cost and the total cost for each bus balancer.

TABLE 2.4: Number of semiconductors and cost for the bus balancers.

Topology	Rated voltage	No. of semiconductors	Cost/unit	Total cost
4-level	1.7 kV	48	1	48
3-level	1.7 kV	64	1	64

Table 2.5 presents the semiconductors used in the 3L-NPC and 5L-ANPC. The 3L-NPC is composed of 6.5 kV semiconductors in the 4.16 kV inverter and 4.5 kV semiconductors series-connected in the 6.6 kV inverter. The 5L-ANPC is composed of 3.3 kV and 4.5 kV semiconductors, respectively.

TABLE 2.5: Number of semiconductors and cost for the 3L-NPC and the 5L-ANPC for a 4.16 kV and a 6.6 kV inverter.

Topology	Rated voltage	No. of semiconductors	Cost per unit	Total cost
4.16 kV **3L-NPC**	6.5 kV	24	10	240
4.16 kV **5L-ANPC**	1.7 kV	48	6	288
6.6 kV **3L-NPC**	1.7 kV	48	8	384
6.6 kV **3L-ANPC**	1.7 kV	48	8	384

Finally, a comparison between the proposed solutions (with a bus balancer when necessary) and the leading solutions is presented in Table 2.6. Table 2.6 compares two leading solutions, the 3-level chopper multiplexed converter with bus balancer and the 4-level chopper multiplexed converter.

TABLE 2.6: Number of semiconductors and total cost for each structure for two inverter voltages.

Nominal voltage	Topology	No. of semiconductors	Total cost
4.16 kV	**xPlexed**	47	182
	3L-NPC	24	240
	5L-ANPC	48	288
6.6 kV	**xPlexed 3L-FC (1)**	110	320
	xPlexed 3L-FC (2)	126	336
	xPlexed 4L-FC	78	288
	3L-NPC	48	384
	5L-ANPC	48	384

Table 2.6 shows that the total cost of the semiconductors for all the proposed solutions based on the multiplexed topology are inferior to the compared leading solutions. Moreover, the solution for a 6.6 kV motor that does not use a dead voltage has an even more significant advantage in terms of semiconductors cost compared to the reference solutions, being the chosen one. This significant reduction in the total cost of the semiconductors shows the interest of this topology for a medium voltage power drive application. Moreover, this advantage demonstrates the validity of this concept with the common stage for the phases reducing the number of semiconductors needed in the independent stage.

Regarding the number of semiconductors of each structure, it may seem to be a big drawback for this topology, principally for the 6.6 kV inverter. However, a semiconductor with a rated current $2I$ counts as two semiconductors in these numbers. If one considers that each used semiconductor has an adapted rated current, i.e., a $2I$ semiconductor counts as only one component, the scenario changes. For the 4.16 kV inverter the multiplexed, the 3L-NPC and the 5L-ANPC have, respectively, 31, 15 and 36 semiconductors. The corresponding 6.6 kV inverters have resp. 51, 27 and 36 semiconductors. As a summary, the multiplexed inverter uses more components than the 3L NPC for both the output voltages and less components than the 5L-ANPC for the 4.16 kV inverter.

2.4 Conclusion

The main variants of multiplexed choppers have been presented and discussed. More specifically, solutions satisfying the requirements of power drives of 4.16 kV and 6.6 kV have been identified and compared, with a special focus on the reduction of cost of semiconductor by using less high-voltage semiconductors. Finally, a comparison has been made with the two better-established transformerless solutions.

Regarding the results of the comparisons, it has been demonstrated that the use of 1.7 kV IGBTs in series in the chopper stage is a crucial factor in the competitiveness of this architecture for both the 4.16 kV and 6.6 kV power drives. First of all, they represent a substantial reduction in the total semiconductor cost when compared with solutions using 3.3 kV IGBTs. Secondly, they also represent a reduction in the chopper stage switching energy, enabling a higher switching frequency and, consequently, reducing the size and volume of the flying capacitors, line-side filter and overall volume and cost.

The comparison also shows that the 3-level choppers with dead voltage for the 6.6 kV inverter are competitive compared to the target solutions in terms of semiconductors cost. However, they add extra complexity to balance the DC bus voltage, needing extra converters with extra passive components (capacitors and inductors). Additionally, the bus balancer circuits need to handle currents of the same order as the nominal current of the inverter due to the significant difference in operation points that the inverter and rectifier sides can have. Finally, another big drawback of the dead voltage for this application is the penalization (in terms of switching efforts) of the inverter stage at low modulation depth. The increase of the switching losses of the inverter legs at low modulation depth goes in the opposite direction of the objectives of this application.Therefore, these solutions are not interesting for this application, but they can find a place in different applications where there is not such a big difference between both sides operation points, such as static synchronous compensators for example.

Consequently, due to the dead voltage's significant drawbacks, using a 4-level chopper-based solution is much more interesting. It eliminates the drawbacks associated to the dead voltage and reduces the cost of the semiconductors compared to the 3-level one. Moreover, the low voltage semiconductors that allow a higher switching frequency helps to compensate the extra stored energy due to an extra flying capacitor in each chopper. Last but not least, this extra flying capacitor chopper level increases the chopper's output frequency helping to improve the waveform quality.

Finally, looking at the comparison results, the multiplexed topology with the proposed structures represents a competitive solution in terms of overall semiconductors cost. The multiplexed topology represents a significant reduction in semiconductors cost for the medium-voltage power drives compared with the better-established solutions from the market. The advantages of the multiplexed topology come from its particular configuration and working principle that mutualizes a switching stage involving low voltage semiconductors thus reducing the stress of the high voltage semiconductors in the inverter stage.

Chapter 3

Modulation

3.1 Introduction

This chapter will present two different modulations strategies for the multiplexed topology: the carrier-based modulation and the space vector modulation. A carrier-based modulation scheme has been developed for the five-level multiplexed converter by [38, 39], but for a different application, with different objectives and constraints. Consequently, new modulation schemes, adapted to the requirements of this medium voltage power drive application, have been developed.

The main objective of the developed modulations follows the main objective of the topology itself: reduce the switching efforts in the high voltage (HV) semiconductors, reduce the number of commutations and the switched voltage. The main reduction of the semiconductor stress comes from the working principle of the topology that at any time only one inverter leg switches (switching only one third of the time), thus dividing by three the number of commutations when compared to a classical inverter topology at the same frequency. Moreover, the inverter stage is in series with the chopper stage switching an already switched voltage. This allows the inverter legs to switch the square voltage waveform generated by the chopper stage and, assuming an appropriate synchronization, the inverter can switch the lower voltage of this square wave. The reduced switched voltage reduces the switching energy and also helps to reduce the voltage spike seen by each semiconductor when turning off, thus reducing the cosmic ray failure rate [43, 44]. This is especially interesting for the 6.6 kV solution where the inverter semiconductors are series connected because it reduces the maximum voltage seen by these components and gives some extra margin in case the voltage balance is not ideal. More details of the working principle of the topology and how it reduces the semiconductor stress will be explained in the following sections. Next sections will also detail the different carrier-based modulation and space vector modulation schemes.

3.2 Control strategy for xPlexed Converters

In the multiplexed topology the output voltage results of the combined action of the two conversion stages that are interconnected but need to be controlled separately. The top and bottom choppers generate, respectively, the highest (in green) (Figure 3.1(a)) and lowest (in blue) voltages of the three-phase reference and the corresponding inverter legs are saturated to respectively 100 % and 0 % duty cycles, which means they are not switching. The remaining inverter leg will generate the

intermediate voltage (in red) by switching the square voltage produced by the chopper.

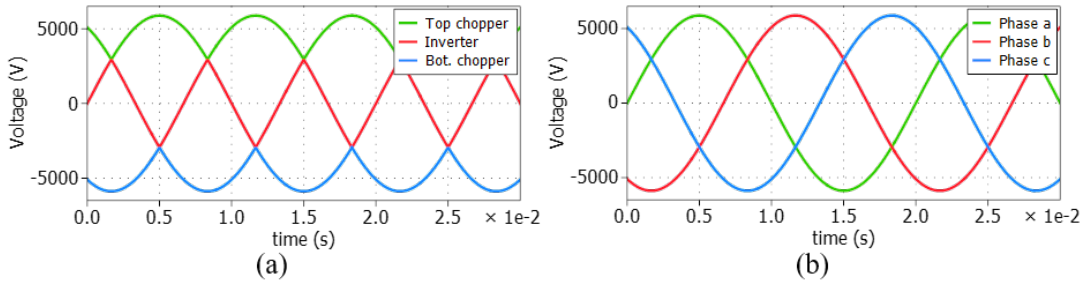


FIGURE 3.1: Three-phase voltage reference signals for: (a) multiplexed inverter; (b) conventional inverter.

Consequently, unlike conventional three-phase topologies, this topology does not have independent phase legs [38] (Figure 3.1(b)).

3.3 Carrier based modulation

Authors in [38, 39] worked on the carrier-based modulation for a five-level multiplexed converter applied to Uninterruptible Power Supply (UPS), solar or Battery Storage System (BSS) applications. This work had a different application and a major difference that prevents to use its scheme in this power drive application: it is a step-down application with an important voltage ratio between the DC bus ($V_{DC} = 1500\ V$) and the AC output ($V_{AC} = 400\ V$). Besides that, due to the application and the voltage ratio the major objective was to reduce the static voltage seen by the inverter switches in order to reduce their rated voltage and, consequently, reduce the overall losses and cost. Therefore, in this application it was possible to use inverter switches that do not need to withstand the whole bus voltage.

In the medium voltage power drive application is not the same case because the voltage ratio between the bus and the output voltage can be close to the unit depending on the operation point. Consequently, it is not possible to change the static voltage seen by the inverter switches via the choppers; the inverter switches need to withstand the whole bus voltage. Therefore, the objective is to keep the working principle of one phase switching at a time (thus reducing the number of switchings per second) and the reduction of the voltage switched by the inverter (thus reducing the switching energy, the voltage overshoots and the failure rate).

Due to its working principle (and the topology configuration used in this application) the carried based modulation applied to the multiplexed topology presents some degrees of freedom that can be explored in function of the objectives of the application. The degrees of freedom of this topology are the nature of the chopper and inverter carriers (triangular, sawtooth or inverted sawtooth), the phase between the carriers of the different conversion stages (chopper-chopper and chopper-inverter) and the ratio between the switching frequency of chopper and the inverter.

Two examples of utilization of the degrees of freedom will be presented here. These two examples fit the main criteria for the modulation for this application that is reduce the switched voltage by the inverter switches. Other combinations such as the modulation developed by [38, 39] for example can be used, but they do not match

the application criteria/requirements, or they add extra complexity when compared to these two examples we selected. The principle that will be presented here can be applied for the two topologies that have been chosen in the previous chapter, i.e., two 3-level or 4-level flying capacitor choppers with a 3-level NPC inverter.

For this topology configuration, where the inverter stage is composed by a 3L NPC (Figure 3.2), the positive and negative sides of the converter can be decoupled. In other words, the converter can be simplified to two decoupled converters where each one is, respectively, responsible to produce a positive and negative average output voltage. These two converters are symmetric so the analysis that will be done for the positive average voltage is valid for the negative one.

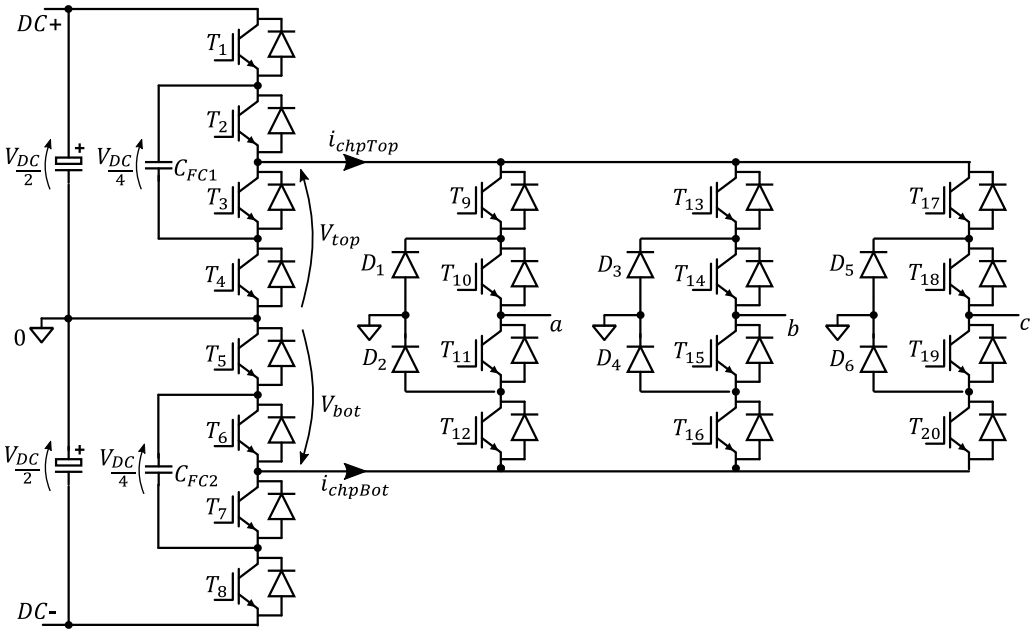


FIGURE 3.2: Detailed electrical schematic diagram of the 5-Level three-phase DC-AC Multiplexed Power Converter. The chopper stage consists of two 3-level-Flying Capacitor and the inverter stage consists of three-phase 3-level NPC converters.

For both the positive and negative average output voltages, the structure can be simplified, symmetrically, as a half bridge supplied by a chopper. To reduce complexity and notation changes of this simplified schematic the flying capacitor will be referenced as chopper and the half bridge as inverter. Figure 3.3 shows the simplified schematic that allows an easier definition of the average output voltage.

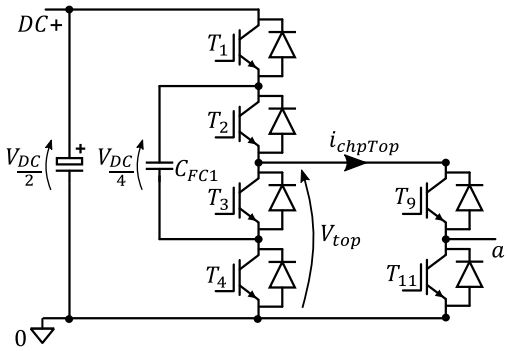


FIGURE 3.3: Simplified electrical schematic to represent the positive side of phase *a* with a 3-level-Flying Capacitor chopper supplying a half bridge.

Figure 3.4 (a) and (b) shows combinations of sawtooth carriers for the chopper and, respectively, a sawtooth and an inverted sawtooth carrier for the inverter. For this case the equivalent frequency of the chopper and the switching frequency of the inverter are the same. The flying capacitor chopper switching frequency is equal to its equivalent frequency divided by the number of switching cells [18, 22]. In these two combinations it is possible to see that the chopper carriers are slightly delayed with respect to those of the inverter. This delay is used to ensure that either the rising edge of the inverter commutation (case a) or the falling edge of the inverter commutation (case b) will occur at a low chopper voltage. The voltage in which the other commutation edge occurs depends on the inverter duty cycle.

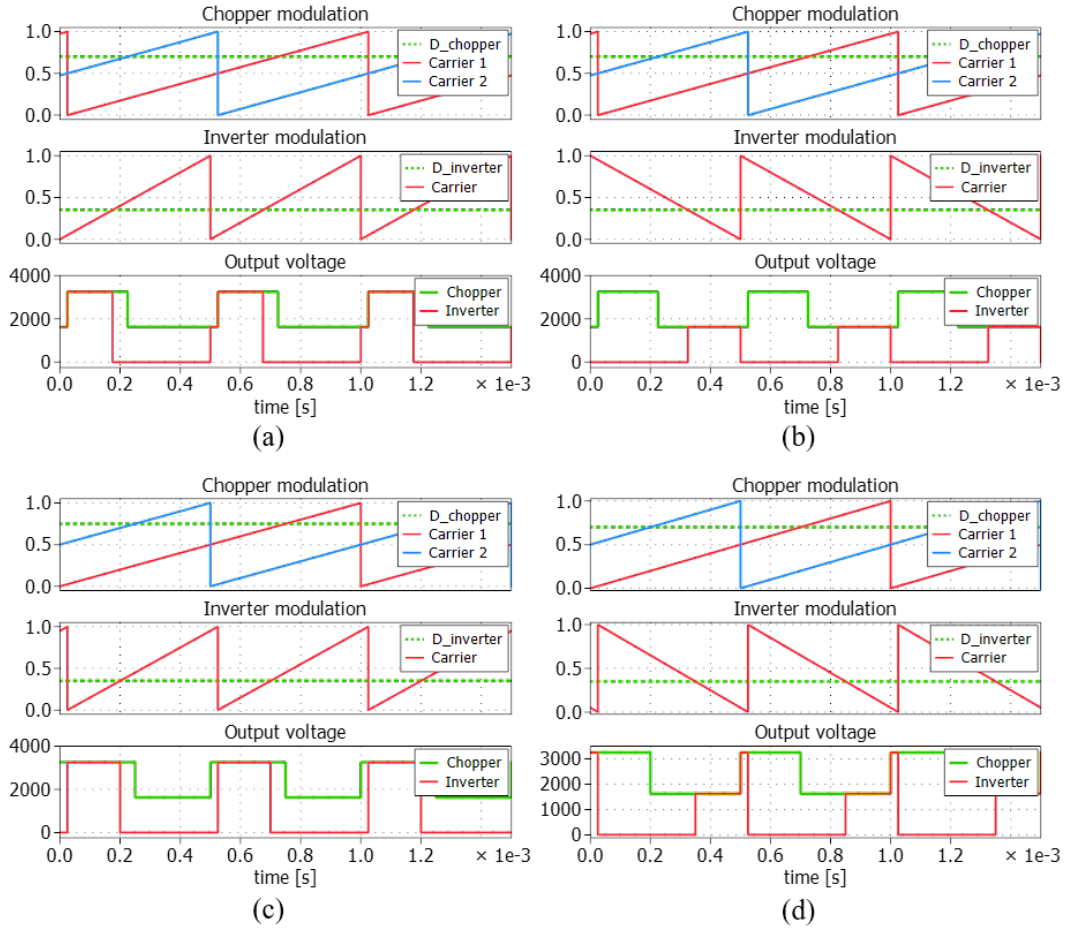


FIGURE 3.4: Proposed carrier-based modulation combining sawtooth carriers for the chopper with: (a) advanced sawtooth carrier for the inverter; (b) advanced inverted sawtooth carrier for the inverter; (c) delayed sawtooth carrier for the inverter; (d) delayed inverted sawtooth carrier for the inverter.

The delay needs to be just bigger than the switching time of the inverter switches to ensure that when the chopper starts to switch the inverter switching is finished. In other words, this delay should be equal to the inverter dead-time.

If these delays where in the opposite direction, i.e., the inverter carrier delayed with respect to those of the chopper (Figure 3.4 (c) and (d)), these commutations would always occur at a high chopper voltage.

Figure 3.5 (a) and (b) presents shows a combination of a triangular carrier for the

chopper and, respectively, a sawtooth and an inverted sawtooth carrier for the inverter, but now with the chopper switching at the same frequency as the inverter. These combinations are more interesting than the previous one (Figure 3.4), considering the use of 1.7kV IGBTs in series for the chopper. They allow a reduction of the capacitance of the flying capacitors for a given voltage ripple or/and a reduction of the voltage ripple for a given capacitance in comparison with the previous solution. This increase in the chopper switching frequency also contributes to the current waveform quality, reducing the current ripple in the grid and inverter side. Later, on Chapter 4 it will be possible to see that this increase in the chopper switching frequency does not have an important effect in the chopper overall losses. More details in the chopper and inverter modulation of this combination will be presented hereafter.

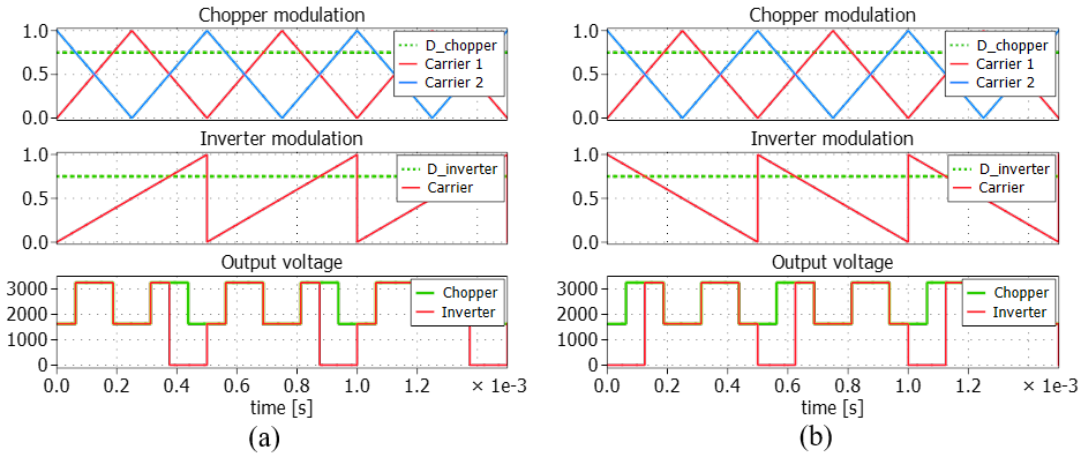


FIGURE 3.5: Proposed carrier-based modulation combining triangular carriers for the chopper with: (a) sawtooth carrier for the inverter; (b) inverted sawtooth carrier for the inverter.

3.3.1 Chopper modulation

The main purpose of the control of the DC-DC choppers is to generate the highest and lowest voltages of the three-phase reference. In addition, it must also balance the voltage of the flying capacitors maintaining the average current in the flying capacitors at zero [22, 38, 39].

Unlike proposed by [38], where the chopper switches at half of the frequency of the inverter, in this case the chopper switches at the same frequency as the inverter.

This choice of switching frequency is possible because the switching energies of the $1.7kV$ devices are almost negligible compared to those of the inverter legs, and it contributes to reduce the flying capacitors size and voltage ripple. Consequently, stored energy, volume and even cost can be reduced.

The current supplied by the top (resp. bottom) chopper can take two values: can be equal to the current in the phase with the highest (resp. lowest) of the three voltages or to this current plus the current in the phase with the mid voltage as shown by Equation 3.1. Consequently, the current supplied by the chopper has a switched shape with a frequency equal to that of the inverter (Figure 3.13(b) and Figure 3.15(c)). If a frequency ratio like the one described by [38] was used, an almost zero current in each flying capacitor would be guaranteed because the charging and discharging phases of the flying capacitor would occur with almost the same

value. So, it would be possible to take advantage of FCs self-balancing property using Phase Shifted (PS) modulation [20].

$$i_{chop} = i_{high} + k \cdot i_{mid} \tag{3.1}$$

i_{high} and i_{mid} denotes the current of the highest and intermediate voltage phases; k stands for the switching state of the intermediate voltage phase (1 if connected to the top chopper and 0 if not).

However, using the same switching frequency for the chopper and inverter, the charge and discharge current of the flying capacitors is no longer symmetrical, because the charge and discharge occur within the same period of the inverter. Therefore, the chopper modulation chosen is based on Phase Disposition (PD) by means of state machines [22, 47] giving the necessary degree of freedom to balance FC voltages even though this may cost some extra commutations.

Next section will explain how the inverter modulation is done respecting the unitary switching frequency ratio between chopper and inverter

3.3.2 Inverter modulation

For this topology, where the inverter stage is composed by a 3L NPC (Figure 3.2), each phase can be seen as two decoupled blocks where each one is responsible to produce, respectively, a positive and negative average output voltage. For example, the positive part of the voltage in phase a will be built by the top chopper and the top NPC switching cell (T_9 and T_{11}). These two blocks are symmetric so the analysis that will be done below is valid for the positive and negative average voltage.

In order to reduce the inverter switched voltage, the maximum voltage and the switching energy, one of the inverter switching edges will be aligned to the middle of the lower voltage level produced by the chopper. Figure 3.5(a) shows in red how the inverter re-chops the square voltage generated by the chopper for a rising sawtooth carrier. In this case, the inverter rising edge will be always aligned with the beginning of the first period of chopper voltage and the corresponding inverter commutation is guaranteed to occur at lowest voltage; on the other hand, depending on the value of the inverter duty cycle, the falling edge will create a commutation of the inverter at a voltage that can be low or high. Figure 3.5(b) shows a similar analysis for a falling sawtooth. As a conclusion of these two figures, a rising (resp. falling) sawtooth carrier can guarantee that the rising edge (resp. falling edge) of the inverter voltage occurs when the chopper voltage is low; concerning the falling edge (resp. rising edge) of the inverter voltage, it may occur at low or high chopper voltage depending on the inverter duty cycle. However, it should be noted that the sign of the current is needed to determine whether an edge of the inverter voltage involves a turn-on or a turn-off of the inverter IGBTs.

The mathematical development of the inverter duty cycle calculation will be done in the Appendix A. The waveform simulation results and the conclusions for the carrier-based modulation are presented in Section 3.5.

3.4 Space Vector Modulation

This section will present the development of a space vector modulation (SVM) scheme dedicated to the multiplexed inverter applied to medium voltage power drives. The

SVM scheme for a five-level multiplexed inverter will be detailed and the scheme for the seven-level will also be presented.

3.4.1 Five-level multiplexed inverter

3.4.1.1 Modulation triangle identification

The modulation triangle identification of the space vector modulation (SVM) for this topology is an application of the scheme that has been developed by [54]. This scheme has been used to find the vertex as will be described hereafter and some particular strategies have been developed to adapt to the special features this topology.

The reference vector (Figure3.6(a)) for a three-phase SVM is given by:

$$V_{ref}^{*} = (n-1)(V_a^{*} + V_b^{*} \cdot e^{j\frac{2}{3}\pi} + V_c^{*} \cdot e^{j\frac{4}{3}\pi}) \tag{3.2}$$

where V_a^{*}, V_b^{*} and V_c^{*} are, respectively, the reference voltages of phases *a*,*b* and *c*; and n the number of output levels of the converter. In order to simplify the identification of the triangle and, mostly, the switching sequence definition the reference vector will be shifted to the first sector (sextant). This way, the next steps will be addressed only on the first sector and, at the end, a rotation table (Table 3.2) will be used to apply the switching sequence in the original sector.

The sector of the reference vector is given by:

$$sector = 1 + floor\left(\frac{\theta}{\frac{2\pi}{3}}\right) \tag{3.3}$$

$\theta \in [0, 2\pi]$ denotes the angle of the reference vector V_{ref}^{*}; $floor(\gamma)$ stands for the corresponding integer part of γ.

The rotated reference vector V_{ref} is given by:

$$V_{ref} = |V_{ref}^{*}| \cdot e^{j(\theta-(sector-1)\cdot\frac{2}{3}\pi)} \tag{3.4}$$

where $|V_{ref}^{*}|$ stands for the module on the reference vector V_{ref}^{*}.

To be able to identify the three closest states to the rotated reference vector that compose the modulation triangle, this reference vector will be decomposed into orthogonal coordinates using the real V_x and imaginary V_y unit-vectors (Figure3.6(a)) defined as [54]:

$$\begin{bmatrix} V_x \\ Vy \end{bmatrix} = V_{DC} \cdot \begin{bmatrix} 1 \\ j\sqrt{3} \end{bmatrix} \tag{3.5}$$

where V_{DC} is the DC bus voltage.

According to the previously defined orthogonal vectors the real and imaginary coordinates of the rotated reference vector [54] are given by:

$$x = \frac{V_{ref}(x)}{V_{dc}}, \quad y = \frac{V_{ref}(y)}{\sqrt{3}V_{dc}} \tag{3.6}$$

$V_{ref}(x)$ and $V_{ref}(y)$ are the real and imaginary components of the vector, respectively.

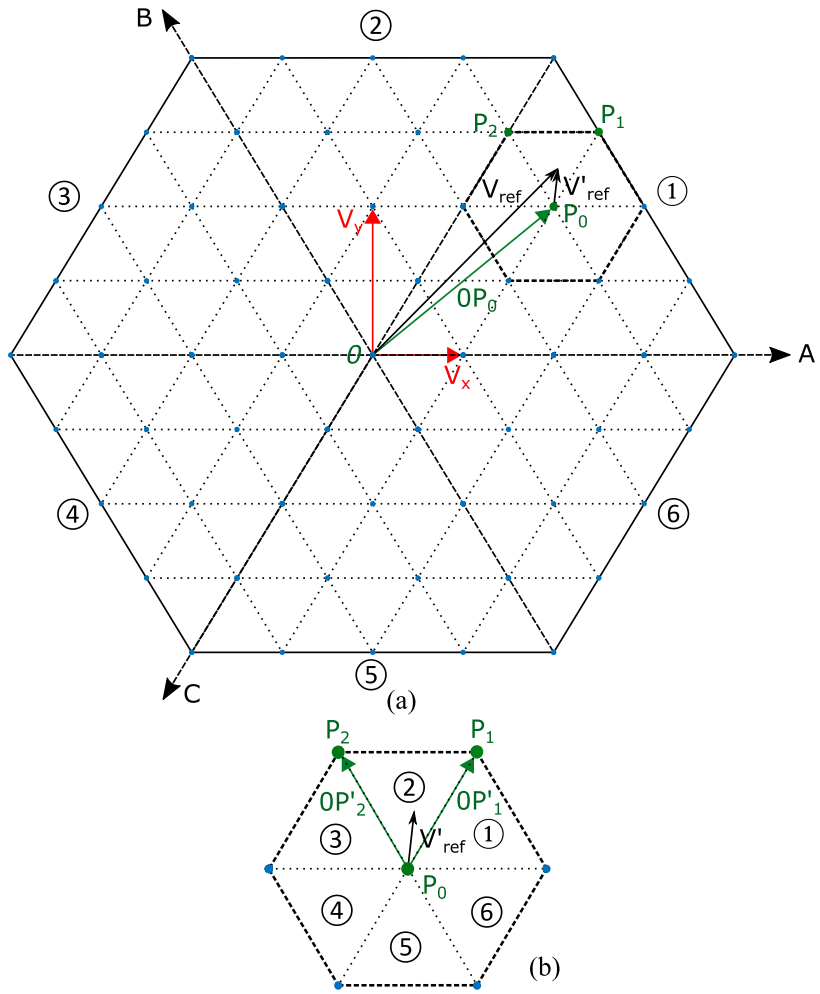


FIGURE 3.6: Proposed SVM scheme: (a) vertex identification on a 5-level diagram; (b) remainder vector in the local two level state space diagram.

Having those components of the vector it is possible to find the vertex of the modulation triangle $\Delta P_0P_1P_2$: the vector part of the modulation triangle closest to the origin O of the state space diagram. Equation 3.7 gives a candidate switching state for the vertex.

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = floor\left(\begin{bmatrix} x - min(x,y,-y) \\ y - min(x,y,-y) \\ -y - min(x,y,-y) \end{bmatrix}\right) - \frac{n-1}{2} \tag{3.7}$$

$min(x,y,-y)$ corresponds to the minimum value among x, y, and $-y$; $floor(\gamma)$ denotes the corresponding integer parts of all the elements in an array γ; $\frac{n-1}{2}$ ensures that the switching states of the vector are comprised in the interval $[-2,2]$ for a five level converter.

This switching state does not necessarily correspond to a switching state that can be directly synthesized by this topology. But, the problem of selecting a control vector for a given point will be addressed in a later step.

Corresponding to equation 3.2, an output space vector that represents the switching states of all three phases is defined for a n-level converter as:

$$V_{out} = V_{dc} \cdot (S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi}) \tag{3.8}$$

Once the vertex of the modulation triangle is detected, the origin of the rotated reference vector V_{ref} is shifted to the detected vertex (Equation 3.9). This new vector will be called remainder vector V'_{ref} [54]. The remainder vector is located inside a local two-level state space diagram as can be seen on Figure 3.6(b).

$$V'_{ref} = V_{ref} - OP_0 \tag{3.9}$$

OP_0 is the vertex of the modulation triangle $\Delta P_0 P_1 P_2$.

The next step is to find the other two vectors of the modulation triangle. This can be done using the angle of the remainder vector to find in which sector of the local two level state space diagram the modulation triangle is located. Equation 3.10 gives the sector $sector'$ of the remainder vector in the local two-level state space. Once the modulation triangle is located, the other two vectors of the modulation triangles are easily known.

$$sector' = 1 + floor\left(\frac{\theta'}{\frac{2\pi}{3}}\right) \tag{3.10}$$

θ' denotes the angle of the remainder vector V'_{ref}; $floor(\gamma)$ stands for the corresponding integer part of γ.

The scheme previously described would be enough to find all the modulation triangles of a classical multilevel topology. However, the multiplexed topology, due to its particular configuration and working principle, does not have all the vectors and states of an equivalent classical topology with the same number of levels. Figure 3.7(a) presents the state space diagram of a five-level multiplexed converter. The red dots represent the vectors/states that are available in a classical five-level inverter but not all of them can be acessed by the five-level multiplexed. The red dotted lines represent, in the first sector, the unavailable transitions of the five-level multiplexed inverter. The green dashed trapeziums that outline the areas A_1 and A_2 represent, in the first sector, the areas where this topology cannot use regular modulation triangles due to the absence of a vector. To cover these trapezoidal areas there are three possibilities that will depend on the reference vector as shows Figure 3.7(b,c,d): the two isosceles modulation triangles T_{11} and T_{12} or the modulation trapezium T_{13} for A_1 and, respectively, T_{14}, T_{15} and T_{16} for A_2.

The choice between the two different triangles and the trapezium depends on the duty cycle calculation that will be explained hereafter.

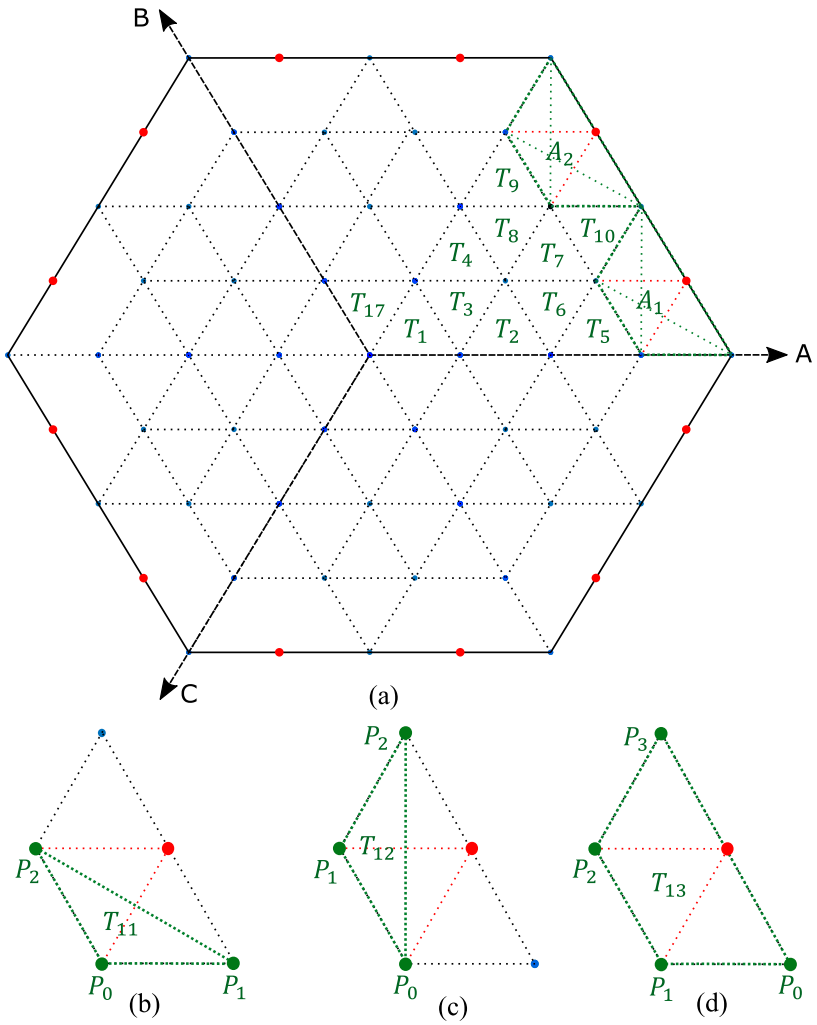


FIGURE 3.7: State space diagram: (a) 5-level multiplexed converter with modulation triangle/trapezium identification; (b), (c) modulation triangles and (d) trapezium of the trapezoidal areas.

3.4.1.2 Duty cycle

The next step is to calculate the duty cycle of each vector of the modulation triangle or the modulation trapezium, i.e, the amount of a period that each vector of the modulation triangle/trapezium will stay active. There are more straightforward ways to calculate the duty cycle that have been presented by [55–58], but they are not compatible with the different modulation triangles and trapezium that can be found on this topology. Thus, the duty cycle calculation will be explained first for the different triangles and after will be extended to the trapezium.

The duty cycle of each vector from the modulation triangle can be obtained solving the following equation:

$$V_{ref} = d_0 \cdot OP_0 + d_1 \cdot OP_1 + d_2 \cdot OP_2 \tag{3.11}$$

$d_x (x = 0, 1, 2)$ are the duty cycles for the vectors OP_x $(x = 0, 1, 2)$, respectively. OP_x is the vector that goes from the origin O to the state $P_x (x = 0, 1, 2)$. Once we have already the vertex for the given rotated reference voltage V_{ref}, the remainder

vector V'_{ref} is inside the local two level state space diagram and the problem can be simplified to the equation 3.12.

$$V'_{ref} = d_1 \cdot OP'_1 + d_2 \cdot OP'_2 \tag{3.12}$$

d_1 and d_2 are, respectively, the duty cycles of the vectors P_1 and P_2; OP'_x is defined as:

$$OP'_x = OP_x - OP_0 \tag{3.13}$$

The vectors OP'_x ($x = 1, 2$) correspond to the other two vectors of the modulation triangle shifted to the detected vertex. Knowing the duty cycles d_1 and d_2, the duty cycle of the vertex d_0 is given by:

$$d_0 = 1 - d_1 - d_2 \tag{3.14}$$

Regarding the trapezoidal areas on the first sector represented, for example, by A_1 on Figure 3.7 there are three different possibilities to produce the output voltage: using the modulation triangles T_{11} or T_{12} and the trapezium T_{13}. When the reference voltage is located inside the triangle T_{11} it is used as the modulation triangle. When the reference voltage is outside the triangle T_{11} and inside T_{12} it becomes the modulation triangle. Otherwise, when the reference is located in the trapezoidal area but outside both the triangles, the trapezium T_{13} is used. In this case we do not have a modulation triangle anymore, but a modulation trapezium.

The duty cycle calculation for these isosceles triangles located in the trapezoidal areas is realized in the same way as for the other modulation triangles (Equation 3.12) using one of its vertices as vertex. When using the modulation trapezium, in order to use the same equations, a triangle shown on Figure 3.8 that will be referred at as simplex is used. This simplex triangle is composed by the two states furthermost from the origin and a third point P'_0 located between the two states from the trapezium closest to the origin. This fictitious state will be the P_0 state on the duty cycle calculation (i.e., it works as the vertex of the simplex). After that, its duty cycle is divided equally between the two states of the trapezium closest to the origin. The other two duty cycles from the simplex triangle will be affected to the corresponding states on the trapezium.

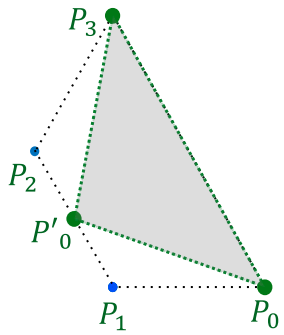


FIGURE 3.8: Simplex triangle used to determine the duty cycle of the trapezium states.

To choose between the three existing options in the trapezoidal area the duty cycle is calculated for both the three ones. After, the duty cycle of each vector from both the modulation triangles is verified to be between 0 and 1. The modulation triangles

which all the duty cycles fulfill this condition are able to be used. If both fulfill the conditions the priority is given to T_{11} as we have seen before. On the other side, if none of the triangles fulfill the condition (i.e., the reference is out of the two triangles) the trapezium is used.

3.4.1.3 Switching sequence

As explained before, the multiplexed topology presents some limitations in terms of the vectors that it can output (i.e., some nonexistent states) (Figure 3.7) and some limitations on the number of states redundancies.

To take advantage of the topology biggest benefit (i.e., to reduce the HV semiconductors constraints), to reduce the total switching losses and to limit the degrees of freedom in the modulation strategy definition, we will only consider sequences that:

- have two inverter legs locked to the top and bottom chopper, respectively;
- avoid the inverter switching half the bus voltage;
- allow the inverter doing no more than one turn-on and turn-off per period;
- have a single switching function change per state transition;
- have an inverter leg switching function that starts at zero;
- have an unitary switching function change per flying capacitor transition.

When it is impossible to find a complete switching sequence (that does the three transitions of the modulation triangle or the four transitions of the trapezium) that respects those criteria, this transition is avoided.

One more requirement that has been used in this work to choose the sequences, but is not mandatory and has a lower priority than the previous ones, is to start the switching sequence with the lowest levels of the flying capacitors. This will reduce the flying capacitors commutations when transiting between two triangles.

The switching sequences are determined by choosing the possible switching states of each vector of the modulation triangle/trapezium that allows to determine a transition sequence in between them that respects the criteria previously defined. Table 3.1 presents the switching sequences S1 to S4 for each triangle and trapezium of the first sector. The State line corresponds to the switching state of the converter, Tc Bc corresponds to the switching state of the top and bottom choppers, respectively, and Inv(phase) corresponds to the state of the inverter leg of the phase that is switching. In the first sector the inverter leg of phase b switches, phase a is saturated to 1 (to the top chopper) and phase c is saturated to -1 (to the bottom chopper).

Most of the triangles sequences of Table 3.1 have 4 states (S1 to S4), but T7 and T10 and the ones located inside the trapezoidal area have only 3 states (S1 to S3). When the sequence goes from S1 to S4, S4 been a redundant state of S1, we have a complete turn around the triangle in one direction and another turn in the opposite direction during the period as one can see on Figure 3.10(a). When the triangle sequence goes from S1 to S3 it is due to an undesired transition, i.e., a transition that does not respect the previous described criteria. Figure 3.10(b) shows that this sequence does an incomplete tour around the triangle in one direction and then returns to the first one in the opposite direction (i.e., S1 or its redundancies are only accessible at the beginning and the end of the sequence). One can also observe that the modulation

trapeziums T13 and T16 have only four vectors in the sequence (S1 to S4). Like the three vector sequence triangle, on the trapeziums the transition between S4 and S1 is not allowed and the sequence does an incomplete turn and returns as can be seen on Figure 3.10(c).

Figure 3.9 shows in the state space diagram the existing vectors and the allowed transitions from the previous requirements and the switching sequence table.

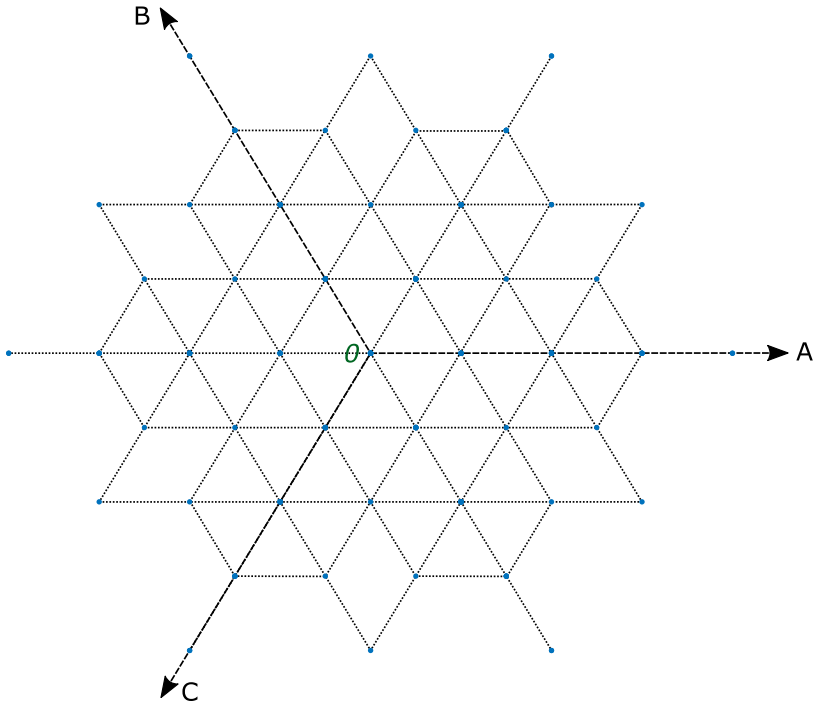


FIGURE 3.9: State space diagram with allowed transitions of the five-level multiplexed converter.

On Table 3.1 it is possible to observe that the triangle T17 has a defined sequence even though it belongs to the sector two. Furthermore, its sequence is not the sequence of T1 rotated to the second sector. This choice has been done because the switching sequence of T1 changes the switching function of the top chopper but not from the bottom chopper. Thus, the switching sequence of T17 only changes the switching function of the bottom chopper. The result of these two different sequences is the balance of the switching efforts of the bottom and top chopper at low modulation depth. This effort equalization is important for normal operation at low modulation depth and can become even more important to manage a critical operation point like a short circuit.

Once the duty cycles are calculated and the switching sequence defined for a given modulation triangle/trapezium, each duty cycle need to be related to its correspondent switching state. This needs to be done because, as seen before, the switching candidate that has been used to the duty cycle calculation does not necessarily correspond to an existing switching state of the topology. Besides that, the vertex and the other vectors from the modulation triangle/trapezium order may not correspond exactly to the final switching sequence (i.e., P_0, P_1 and P_2 may not correspond to S_1, S_2 and S_3, respectively).

To relate a possible switching state with the used one Equation 3.15 gives all the

TABLE 3.1: Proposed switching sequence for the 5-level multiplexed topology SVM.

Triangle		**S1**	**S2**	**S3**	**S4**
T1	State	0 0 0	1 0 0	1 1 0	0 0 0
	Tc Bc	0 0	1 0	1 0	0 0
	Inv(b)	0	0	1	1
T2	State	1 0 0	1 0 -1	1 -1 -1	1 0 0
	Tc Bc	1 0	1 -1	1 -1	1 0
	Inv(b)	0	0	-1	-1
T3	State	1 0 0	1 0 -1	0 0 -1	0 -1 -1
	Tc Bc	1 0	1 -1	0 -1	0 -1
	Inv(b)	0	0	0	-1
T4	State	0 0 -1	1 0 -1	1 1 -1	1 1 0
	Tc Bc	0 -1	1 -1	1 -1	1 0
	Inv(b)	0	0	1	1
T5	State	2 0 0	2 0 -1	2 -1 -1	1 -1 -1
	Tc Bc	2 0	2 -1	2 -1	1 -1
	Inv(b)	0	0	-1	-1
T6	State	2 0 0	2 0 -1	1 0 -1	1 -1 -1
	Tc Bc	2 0	2 -1	1 -1	1 -1
	Inv(b)	0	0	0	-1
T7	State	2 0 -1	1 0 -1	1 0 -2	- - -
	Tc Bc	2 -1	1 -1	1 -2	- -
	Inv(b)	0	0	0	-
T8	State	0 0 -2	1 0 -2	1 0 -1	1 1 -1
	Tc Bc	0 -2	1 -2	1 -1	1 -1
	Inv(b)	0	0	0	1
T9	State	0 0 -2	1 0 -2	1 1 -2	1 1 -1
	Tc Bc	0 -2	1 -2	1 -2	1 -1
	Inv(b)	0	0	1	1
T10	State	2 0 -1	2 0 -2	1 0 -2	- - -
	Tc Bc	2 -1	2 -2	1 -2	- -
	Inv(b)	0	0	0	-
T11	State	2 0 -1	2 -1 -1	2 -2 -2	- - -
	Tc Bc	2 -1	2 -1	2 -2	- -
	Inv(b)	0	-1	-1	-
T12	State	2 0 -2	2 0 -1	2 -1 -1	- - -
	Tc Bc	2 -2	2 -1	2 -1	- -
	Inv(b)	0	0	-1	-
T13	State	2 0 -2	2 0 -1	2 -1 -1	2 -2 -2
	Tc Bc	2 -2	2 -1	2 -1	2 -2
	Inv(b)	0	0	-1	-1
T14	State	2 0 -2	1 0 -2	1 1 -2	- - -
	Tc Bc	2 -2	1 -2	1 -2	- -
	Inv(b)	0	0	1	-
T15	State	1 0 -2	1 1 -2	2 2 -2	- - -
	Tc Bc	1 -2	1 -2	2 -2	- -
	Inv(b)	0	1	1	-
T16	State	2 0 -2	1 0 -2	1 1 -2	2 2 -2
	Tc Bc	2 -2	1 -2	1 -2	2 -2
	Inv(b)	0	0	1	1
T17	State	0 0 0	0 0 -1	-1 0 -1	0 0 0
	Tc Bc	0 0	0 -1	0 -1	0 0
	Inv(a)	0	0	-1	-1

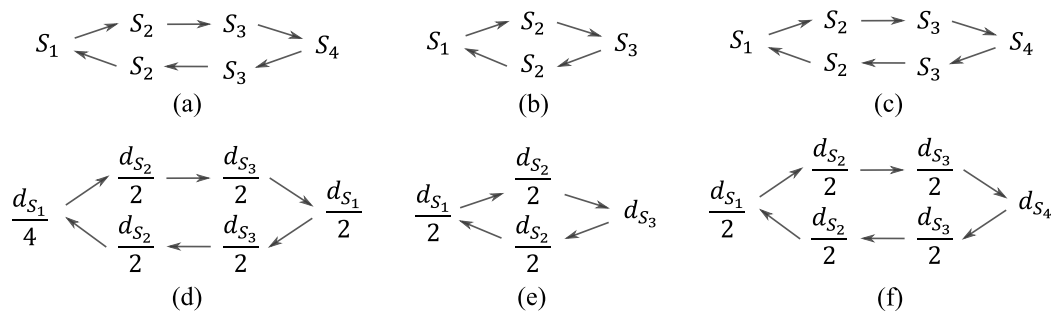


FIGURE 3.10: Switching sequences and duty cycle distribution: (a),(d) complete turn around the triangle (4 states sequence); (b),(e) incomplete turn around the triangle (3 states sequence); (c),(f) an incomplete turn around the trapezium (4 states sequence).

possible redundancies, i.e., all the switching states that correspond to the same vector. Having all the redundancies it is possible to relate the switching state of the sequence with its correspondent duty cycle. Figure 3.10 (d)-(f) shows how the duty cycle calculated previouly are distributed during the period for the different modulation triangles/trapezium. $d_{Sx}(x = [0,4])$ are the duty cycles for the states S_x $(x = [0,4])$, respectively. This sequence has been defined in order to reduce the harmonics using the scheme proposed by [7] and adapted to the triangle with 3 states sequence and the trapezium with 4 states sequence.

$$V_{ref} = [N + S_a, N + S_b, N + S_c] \tag{3.15}$$

where N is an integer $\in [0, \frac{n-1}{2} - max(S_a, S_b, S_c)]$, $max(S_a, S_b, S_c)$ is the maximum value along S_a, S_b and S_c.

Finally, the switching sequence being defined for the reference vector rotated to the first sector, a rotation table can be applied in order to apply this sequence in the original sector of the reference vector [55]. Table 3.2 presents the rotation between the three phases that needs to be realized to convert a vector in the first sector to the other ones. This rotation table is valid also for the switching sequence of the triangles T1 and T17. The only exception is that if the reference is located in an odd sector the sequence of T1 is used and if the vector is located in an even sector the sequence of the T7 is used. It is important to note that the rotation between the phases corresponds only to the rotation between the switching states of the inverter legs. The chopper switching states stay the same independently of the sector, exception made for the triangle T17.

TABLE 3.2: Rotation of the output states depending on the sector in which the reference vector is located.

1st Sector	**2nd Sector**	**3rd Sector**	**4th Sector**	**5th Sector**	**6th Sector**
a	a→b	a→b	a→c	a→c	a
b	b→a	b→c	b	b→a	b→c
c	c	c→a	c→a	c→b	c→b

Looking deeply in all the switching sequences of the Table 3.1 it is possible to observe that the number of switching functions changes for the top and the bottom chopper are the same. Moreover, for similar modulation depths this balance still

present helping on a good equalisation of the losses between the two stages, independently of the operation point. Looking at the inverter side it is possible to see that the inverter switching function changes, at most, only 2 times per modulation triangle/trapezium keeping the characteristics of the frequency multiplicity between the chopper and the inverter and low inverter efforts seen in the carrier-based modulation.

Once the switching sequences defined, these sequences need to be translated to the real state of each switch of the converter. The switching states of the choppers represent their output level, but not how they are produced; the same applies for the inverter legs. In the case of the choppers the strategy used to translate the output levels in the switches states is directly linked with the flying capacitor voltage balancing strategy. The objective is to keep the average value of the flying capacitors voltage at its reference and limit the voltage ripple under some limits.

Flying capacitors converters in conventional applications have the property of natural balance under load. This is possible having an output current that can be considered constant in the switching period window and using one redundant state of the intermediate level at a time when commuting between levels ensuring a capacitor average current equal to zero. This voltage balance is possible using phase-shifted carriers or a finite state machine (FSM). Some strategies to accelerate the voltage balance of the flying capacitors have been studied in the literature [21, 22, 47, 59–63].

However, on this topology the current that feeds the auxiliary bus, i.e, that outputs the chopper, cannot be considered constant in the switching frequency window (as it would be in a conventional application) and the natural balance is not possible for all operation points. To face this voltage unbalance, resulting from a non-zero average current on the flying capacitors, a particular strategy needs to be used. Differently of the conventional strategies, where the redundancies of the intermediate level are alternated, is this strategy the flying capacitor voltage and the output current are watched to choose the redundancy. When commuting to the intermediate level the flying capacitor voltage is compared to its reference: if it is lower the redundancy that increases the voltage is chosen and if it is higher the redundancy that decreases the voltage is chosen. This choice depends on the flying capacitor output current sign, because the state that increases the voltage for one current sign decreases for the opposite one.

This strategy would be enough if each chopper switched continuously. However due to the used switching sequences both the top and bottom chopper can stay saturated to a given level during part of the voltage period for some operation points. If they stay saturated to the intermediate level, that is the level that varies the flying capacitor voltage, the method previously presented is not able to regulate the voltage. Being saturated to the intermediate level means a state that will charge or discharge the capacitor permanently, thus diverging from the reference voltage. If the voltage is diverging from the desired value due to a saturation to a given state, the strategy needs to be able to switch to the other redundant state that will force the voltage to evolve in the other direction. This direct switch between redundant states is controlled by two threshold values: a maximum and a minimum value of the flying capacitor voltage. When the maximum or minimum level is reached a commutation between redundancies is done in order to force the voltage ripple in the other direction. Once the flying capacitor converter is switching between levels the first explained strategy will be enough.

Figure 3.11 shows the finite state machine that is responsible of balance the flying capacitors voltage and executes the strategy that has been described. The variable lvl controls the transitions between the different levels, i_{FC} has the information about the sign of the output current, ΔV_{FC} the variation of the flying capacitor voltage compared to the origin and $actBal$ the information that the voltage reached one of the threshold voltages. Inside each state we have the state of the flying capacitors switches. T_1 and T_2 correspond to the top chopper switches from Figure 3.2 that are complementary to T_4 and T_3, respectively. The same reasoning can be used to the bottom chopper to the switches T_8 and T_7, respectively.

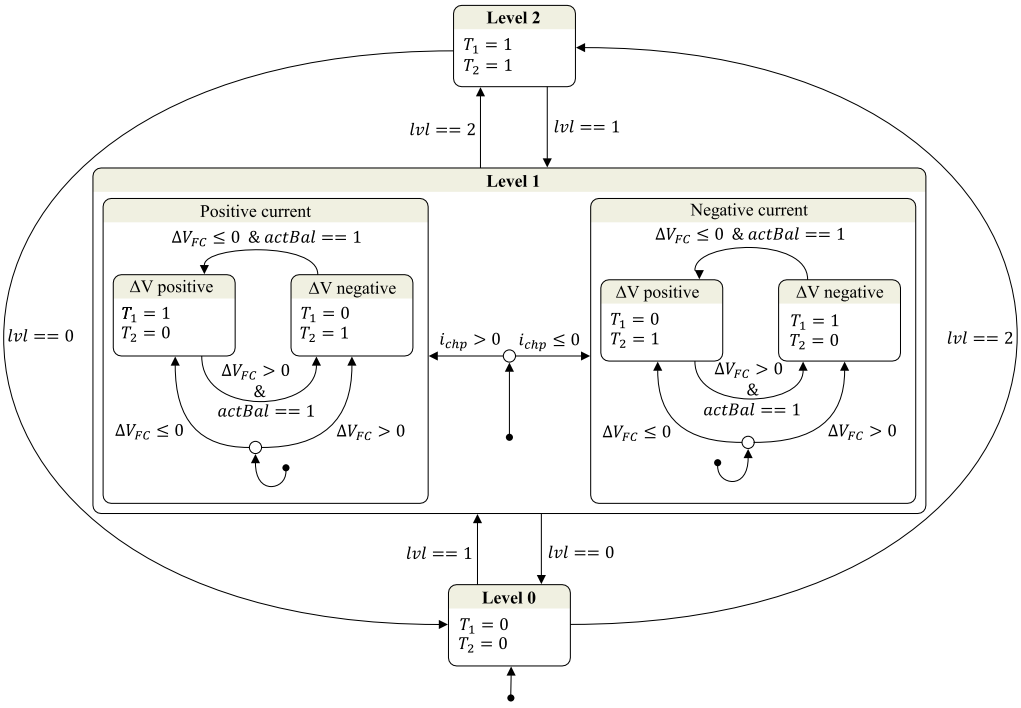


FIGURE 3.11: Finite state machine that controls the flying capacitors voltage and switches states.

For the inverter Table 3.3 shows how each level is translated to the switches states.

TABLE 3.3: Inverter leg switches states in function of is correspondent leg output level from the SVM.

Level	T_9,T_{13},T_{17}	T_{10},T_{14},T_{18}	T_{11},T_{15},T_{19}	T_{12},T_{16},T_{20}
-1	0	0	1	1
0	0	1	1	0
1	1	1	0	0

3.4.2 Seven-level multiplexed converter

This section presents the space vector modulation for the seven-level multiplexed inverter, composed by two 4-level flying capacitor choppers and a 3-level NPC inverter. Figure 3.12 presents the state space diagram of a 7-level multiplexed converter. The red dots in the first sextant represent the states that are available in a classical 7-level topology but not on the 7-level multiplexed one. The green dashed trapeziums that outline the areas A_1 and A_2 represent, in the first sector, where

this topology cannot use regular modulation triangles due to the absence of the red states. To cover those trapezoidal areas, like for the 5-level converter, the possibility is to use asymmetrical triangles or trapezoidal areas. In this case, as there are more non-existent states, there are more possible combinations than in the 5-level one.

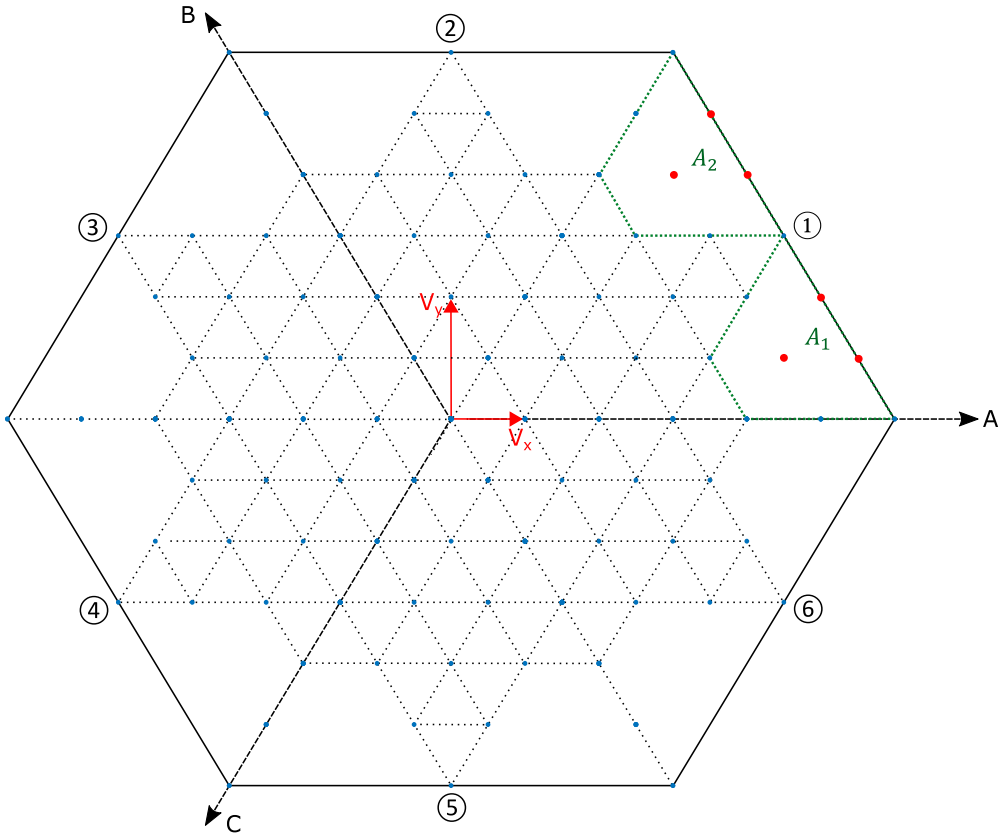


FIGURE 3.12: State space diagram of a 7-level multiplexed converter: existing states in blue and non-existing states compared to a convectional 7-level topology in red.

The SVM for this configuration has not been studied in depth as for the 5-level configuration, but because of the similarity between the two cases the principle of the SVM for this configuration still the same as for the five-level one. The strategy previously adopted for the identification of triangle/trapezium and modulation is still valid for this configuration and so is the duty cycle calculation. Some adaptation may be necessary to cover the bigger trapezoidal areas with different triangles and trapeziums, but always with a similar strategy.

To take advantage of the biggest benefit of this topology (reducing the HV semiconductors constraints and the total switching losses) and to limit the degrees of freedom in the modulation switching sequence definition, the same conditions used for the 5-level can be adopted for the 7-level. One more condition that needs to be defined in this case is which fraction of the bus voltage the inverter can switch. The four-level chopper can output 0, 1/3, 2/3 and 1 of the half bus voltage, consequently the limitation of the maximum voltage switched by the inverter will limit the modulation triangles/trapeziums and the switching sequences.

3.5 Simulation Results

This section will present the simulation results of the carrier-based modulation and the space vector modulation applied to the 4.16 kV fivel-level multiplexed inverter. A comparison of the waveform quality between the two modulation schemes will also be done. Furthermore, a comparison of the semiconductors losses between both schemes will be done on Chapter 4.

Table 3.4 presents the parameters of the 4.16 kV 5-level multiplexed inverter that have been used in the following simulations. The inverter load for these simulations is a RLE load. In order to minimize the bus voltage, third-harmonic injection has been used following Equation 3.16.

$$V_{x,3th} = V_x - \frac{1}{2}(max(V_a, V_b, V_c) + min(V_a, V_b, V_c)) \tag{3.16}$$

where $V_{x,3th}$ $(x = a, b, c)$ is the reference with third harmonic injection, $max(V_a, V_b, V_c)$ and $min(V_a, V_b, V_c)]$ is the maximum and minimum value along the references V_a, V_b and V_c.

TABLE 3.4: Converter parameters used for the simulations.

Parameter	Symbol	Value
Nominal Power	$P_{nominal}$	670 kVA
Nominal Current	$i_{nominal}$	93 A
DC bus voltage	V_{DC}	6500 V
Load voltage	V_{load}	4160 V
Output frequency	f_{AC}	50 Hz
Switching frequency	f_{sw}	1950 Hz
Motor inductance	L_{load}	0.15 $p.u.$
Motor resistance	R_{load}	0.01 $p.u.$

3.5.1 Carrier Based Modulation

Figure 3.13 presents the result of the carrier-based modulation when a falling sawtooth carrier is used (Figure 3.5(b)). One can observe that the falling edge of switch T_9 always occurs at a reduced voltage. It is also possible to observe that the current supplied by the chopper has a switched shape, as indicated by Equation 3.1, with a frequency equal to that of the inverter. In this waveform the top chopper output current i_{chpTop} assumes the values of the output current of the phase a i_a or c i_c or the sum of both.

In the same way, Figure 3.14 shows the waveforms of the output voltage of the top chopper and the voltage of the switches T_9 and D_1 for output voltages lower than the nominal one. On Figure 3.14(a) and (b) that have output voltages equal to 25% and 50%, respectively, of the nominal voltage it is possible to see that the chopper produces a chopped voltage that assumes two different values: 0 and $V_{DC}/4$. Moreover, the falling edge of the switch T_9 always occurs at zero voltage. On Figure 3.14(c), with an output voltage of 75%, it is possible to observe that for some inverter duty cycles the rising and the falling edge of T_9 occurs at the lower voltage supplied by the chopper.

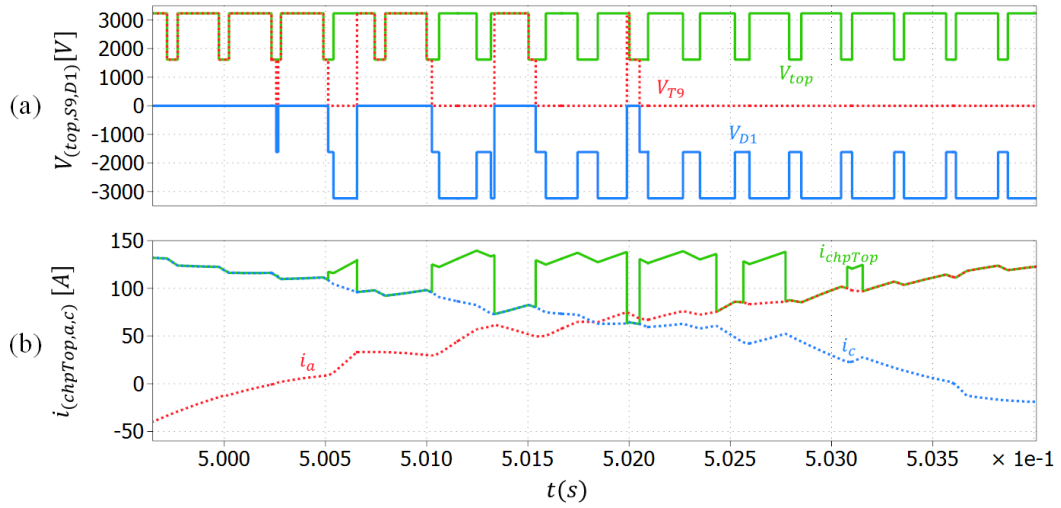


FIGURE 3.13: Simulation waveforms at nominal conditions. (a) Chopper output voltages, V_{top} in green, S_9 and D_1 voltages in red and blue; (b) Top chopper output current i_{chpTop} in green, and phases a and c output current i_a and i_c in red and blue, respectively;

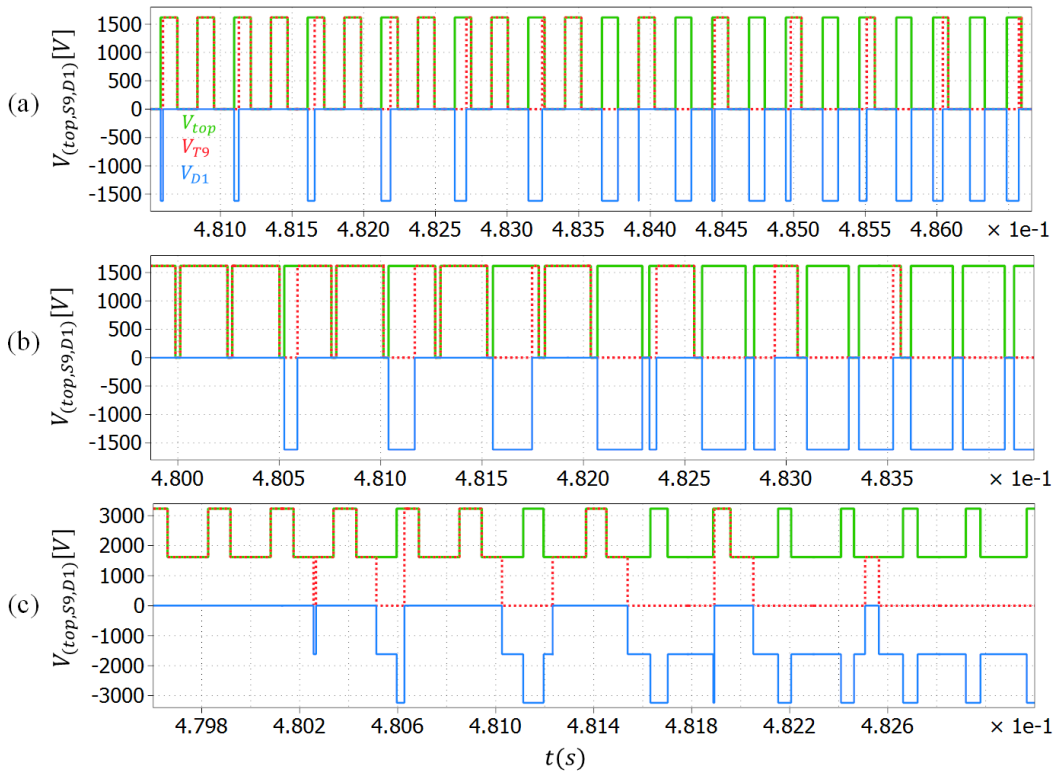


FIGURE 3.14: Simulation waveforms of the top chopper output voltage, V_{top} in green, S_9 and D_1 voltages in red and blue for different percentages of the nominal voltage and frequency: (a) 25%; (b) 50%; (c) 75%.

The fact that those inverter legs switch an already switched voltage allows the inverter legs to switch a reduced voltage or even at zero voltage. This contributes to the reduction of the losses at low output voltage and, besides that, contributes to reduce the efforts in the inner switches from the inverter legs. Those inner switches, in a normal 3-level NPC inverter, have to withstand higher efforts than the outer

switches because of the important difference in the duty cycle between them. Moreover, in the machine side it is common that the inverter needs to supply nominal current at low voltage, which results in important efforts of the inner semiconductors [64, 65].

Figure 3.15 presents an overview of the waveforms of the multiplexed topology using carrier-based modulation at the nominal operation point. Figure 3.15(g) shows the current switched by the semiconductors T_9, T_{11}, and D_1 that switch only one sixth of the time, fallowing the working principle of the topology. Additionally, it is possible to observe that these semiconductors switch current values from the sinusoidal current that are near to zero when the converter works with a power factor close to the unit. This is an important advantage of this topology because, besides the fact that the inverter legs switch only one third of the time, and mostly at reduced voltage, it is able to reduce the HV semiconductors switching losses switching low values of current.

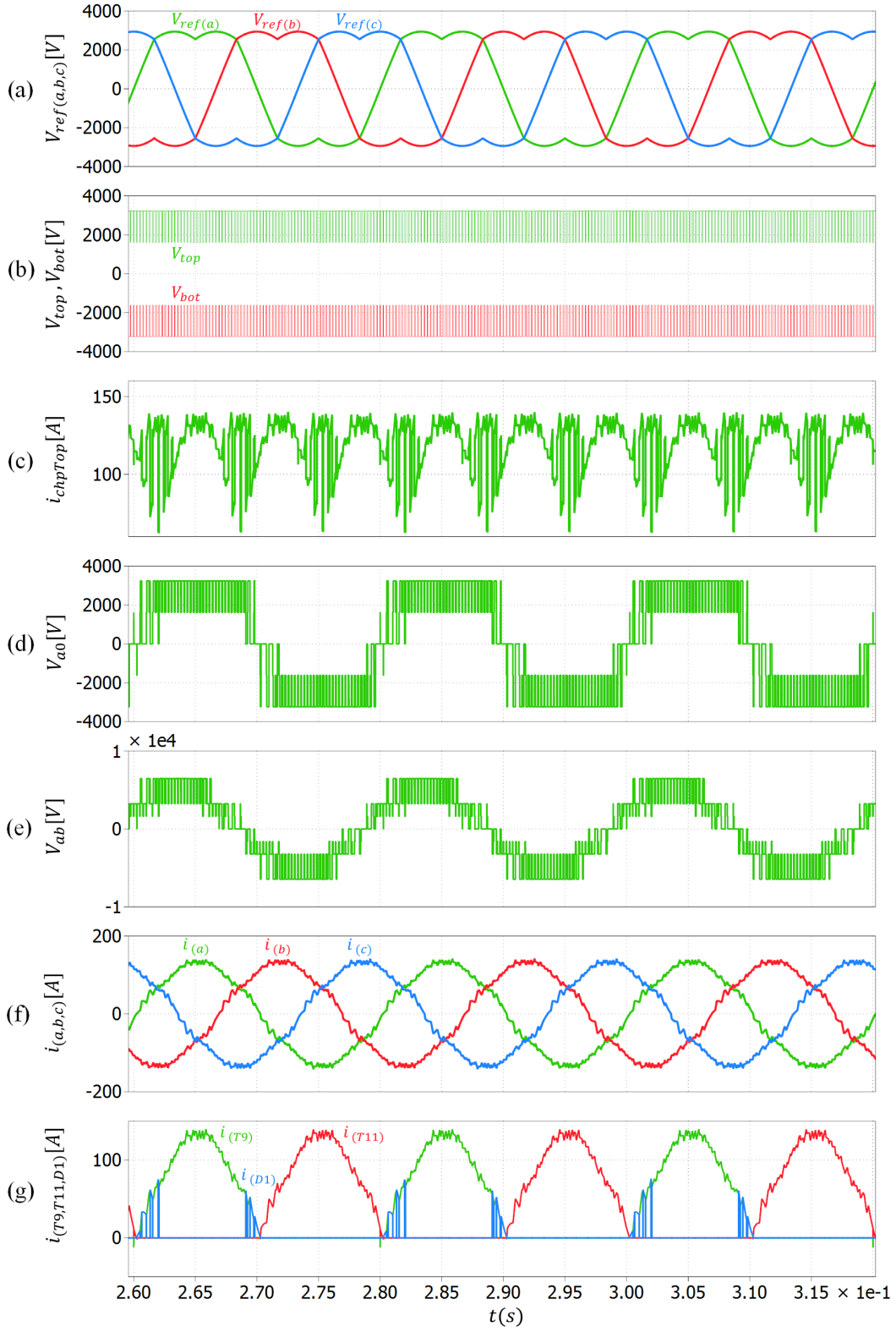


FIGURE 3.15: Simulation waveforms of the 4.16 kV multiplexed inverter operating at nominal conditions. (a) Reference voltages; (b) Chopper output voltages, V_{top} in green,V_{bot} in red; (c) Outpout current of the top chopper; (d): Multi-level voltage of the node a to the DC-link midpoint 0; (e) Multi-level voltage of the node a to the node b; (f) Output phase currents; (g) Current on semiconductors S_9 (green),S_{11} (red) and D_1 (blue).

3.5.2 Space vector modulation

Figure 3.19(b) shows in the state space diagram that the developed space vector modulation is able to use all the states available for this topology that have been presented on Figure 3.9, preserving is working principle. One can observe that the converter does only one commutation at a time when inside a modulation triangle/trapezium according to the Table 3.1. However, it is possible to see that when transiting between modulation triangles some bigger steps happen (longer than the distance between two neighbor states). These bigger steps happen because the defined switching sequences do not take into account the last state from the previous modulation triangle. Therefore, sometimes the last state from one modulation triangle is not side-by-side to the first state from the next modulation triangle causing some extra commutation when transiting between them. This is a consequence of the constraints/requirements that have been used to define the switching sequences and that do not give an extra degree of freedom to manage these transitions with only one commutation.

Figure 3.17 allows to compare the SVM with the carrier-based modulation in terms of the inverter switches efforts for four different output voltages (25%, 50%, 75% and 100%). The first observation that can be made is the fact that independently of the output voltage the inverter switches will always switch at $1/4$ of the bus voltage. The inverter switches will never switch the whole voltage that they need to withstand, however they are not able to switch at zero voltage even for low modulation depths. This is also a consequence of the way the switching sequences have been defined. Besides that, one can observe that mostly of the time the chopper output frequency is twice the inverter switching frequency, having a behavior close to the carrier-based modulation scheme. The moments where the frequency of the top chopper output voltage is not twice the inverter frequency the bottom chopper is switching alternately with the top chopper. As one requirement of the SVM was to have only one commutation at a time, when the bottom chopper switches the top chopper cannot switch simultaneously. Because of this requirement and looking the figure 3.16(b) it is possible to see that the SVM reduces the switching efforts from the choppers by a factor of two regardless of the flying capacitors balance strategy.

Furthermore, Figure 3.16(g) shows that the studied SVM scheme keeps the main characteristic of this topology where each switch switches only one sixth of the time and at low current for a close to the unit power factor. Concerning the output voltage and current waveforms the SVM is responsible for good improvements in the waveform quality comparing with the carrier-based modulation. A comparison in details will be held on Section 3.5.3, after the study of the results of the flying capacitor voltage balance strategy.

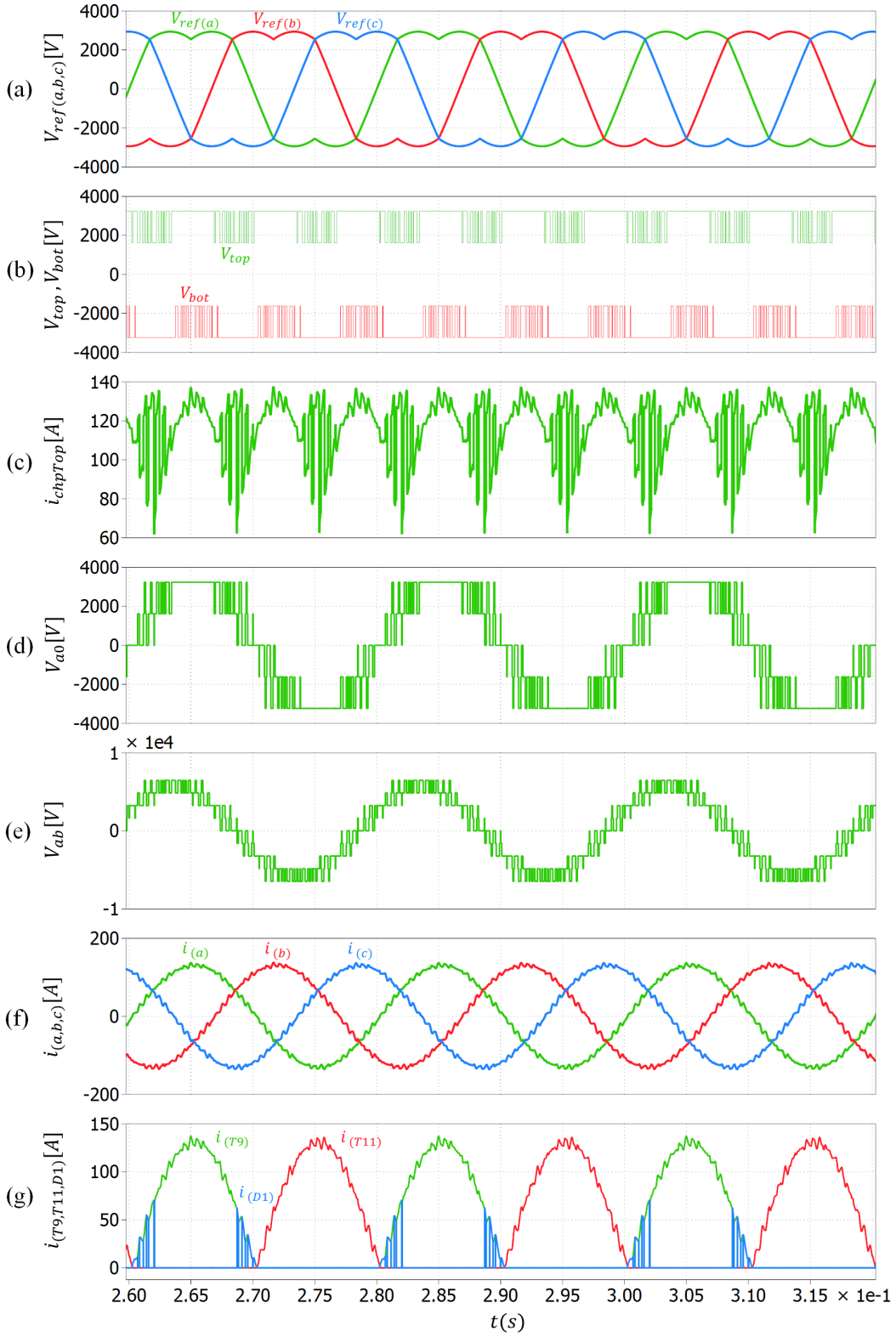


FIGURE 3.16: SVM simulation waveforms of the 4.16 kV multiplexed inverter operating at nominal conditions. (a) Reference voltages; (b) Chopper output voltages, V_{top} in green,V_{bot} in red; (c) Outpout current of the top chopper; (d) Multi-level voltage of the node a to the DC-link midpoint 0; (e) Multi-level voltage of the node a to the node b; (f) Output phase currents; (g) Current on semiconductors S_9 (green),S_{11} (red) and D_1 (blue).

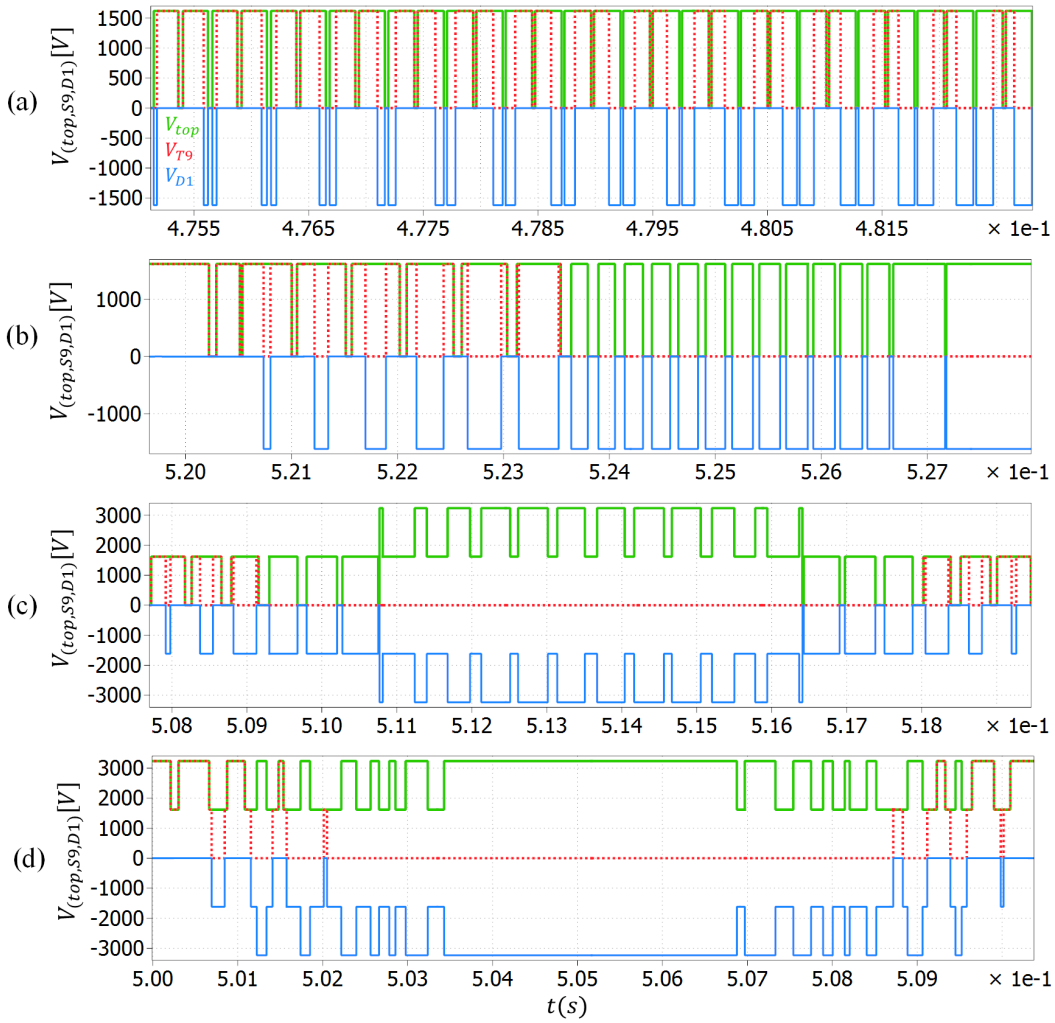


FIGURE 3.17: SVM simulation waveforms of the top chopper output voltage, V_{top} in green, S_9 and D_1 voltages in red and blue for different percentages of the nominal voltage and frequency: (a) 25%; (b) 50%; (c) 75%; (d) 100%.

3.5.2.1 Flying capacitor balance

To analyze the performance of the flying capacitor balance strategy a simulation where the output voltage and frequency vary linearly between 10% and 100% of the nominal values has been done. Figure 3.18(c) and (d) shows, respectively, the top and bottom flying capacitors voltage compared to their references. For this simulation the flying capacitor reference voltage has been set to 1625 V with a threshold of ± 160 V.

One can observe that the flying capacitors voltage in the beginning of the waveform and in the second half of the waveform do not reach the defined threshold voltages. This means that at these operation points a more classical strategy to balance the flying capacitors is enough to control their voltage. I.e., only using the correct redundancy of the intermediate level ($lvl = 1$) of the 3-level flying capacitor when transiting between different levels keeps the capacitors voltage well balanced. Nevertheless, between 1.2 s and 2.5 s the flying capacitors voltage reaches the positive and negative threshold many times, showing that the previous strategy is not enough to keep them balanced. Thus, the strategy where the trigger $actBal$ allows

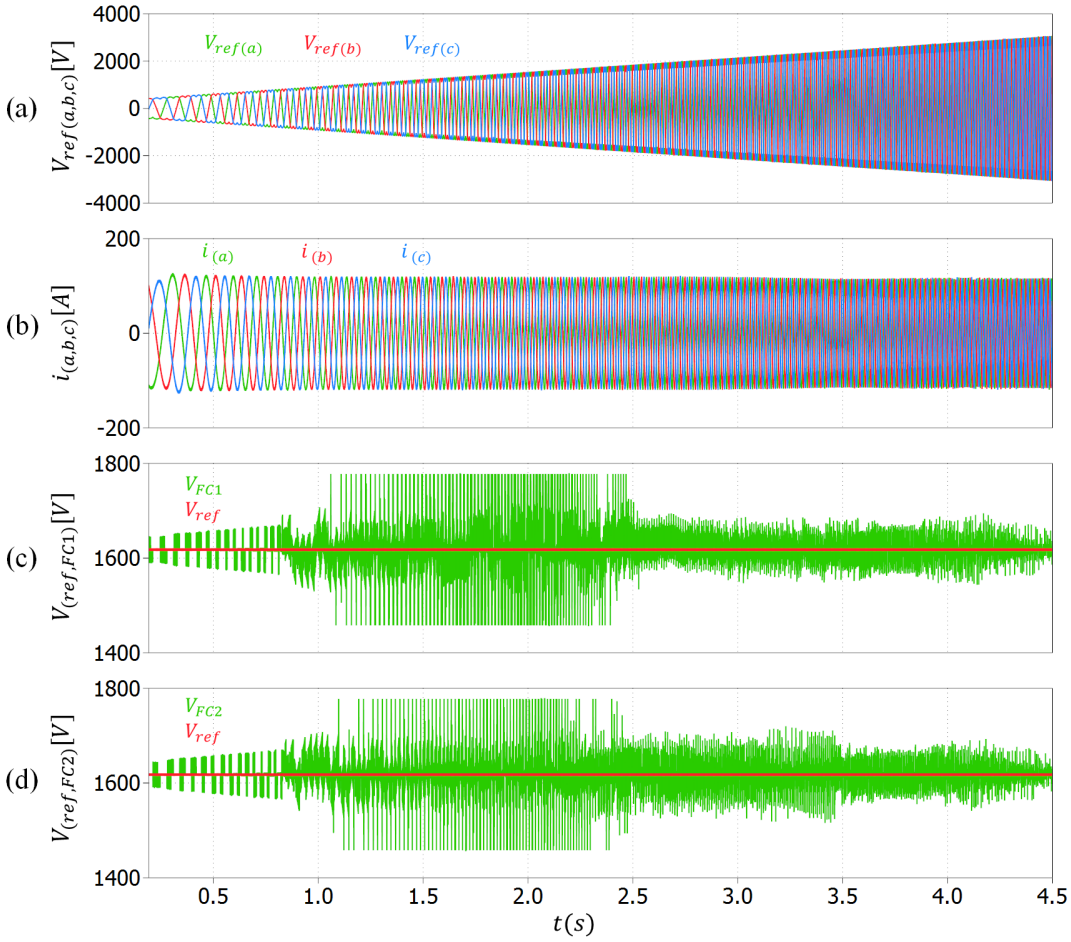


FIGURE 3.18: SVM simulation waveforms of the 4.16 kV multiplexed inverter operating from 10% to 100% of the nominal voltage and frequency. (a) Reference voltages; (b) Output phase currents; (c) Top chopper flying capacitor voltage; (d) Bottom chopper flying capacitor voltage.

direct commutation between the redundancies of the intermediate level takes place when the voltage reaches the threshold keeping the capacitors balanced. The flying capacitor voltage reaches the threshold voltages because for some output voltages some of the modulation triangles used do not switch the corresponding chopper. In other words, the chopper stays saturated at the intermediate level for longer than a period or some periods and the flying capacitor voltage evolves always in the same direction until it reaches the threshold.

This second strategy is able to control the flying capacitor voltages in some operation points where a more classical is not. However, this strategy has a big drawback: when switching directly between intermediate level redundancies two switching cell of the chopper switch at the same time, contrary to normal transitions between levels where only one cell switches. In other words, this transition between redundancies has double the switching losses of a normal transition. Therefore, some care is needed to define the threshold values in order not to overload the chopper switches. Ideally, to avoid increasing switching losses in the chopper the threshold voltage amplitude needs to be at least twice the maximum voltage ripple that the flying capacitor is able to have during one period. This way, when the flying capacitor voltage is controlled by this particular strategy the chopper switches at most at half

the normal frequency, compensating for the double commutation.

3.5.3 Waveform quality comparison

Figure 3.19 shows in the state space diagram the states and the transitions (in red) from both the carrier-based and the space vector modulation for an output voltage going from 10% to 100% (in green). These state space diagrams show that the adopted space vector modulation is able to use all the states available for this topology, preserving its working principle, while the carrier-based modulation uses less than half of the available states. The use of a reduced number of states by carrier-based modulation implies that when switching between different states a bigger step is needed. This bigger steps in the state space diagrams suggests that the carrier-based modulation switches more than one switching cell in the choppers or that the inverter switches at a higher-than-optimal voltage. In fact, some of these bigger steps are a consequence of a synchronized commutation of the top and the bottom chopper, because the carriers of both these converters are synchronized.

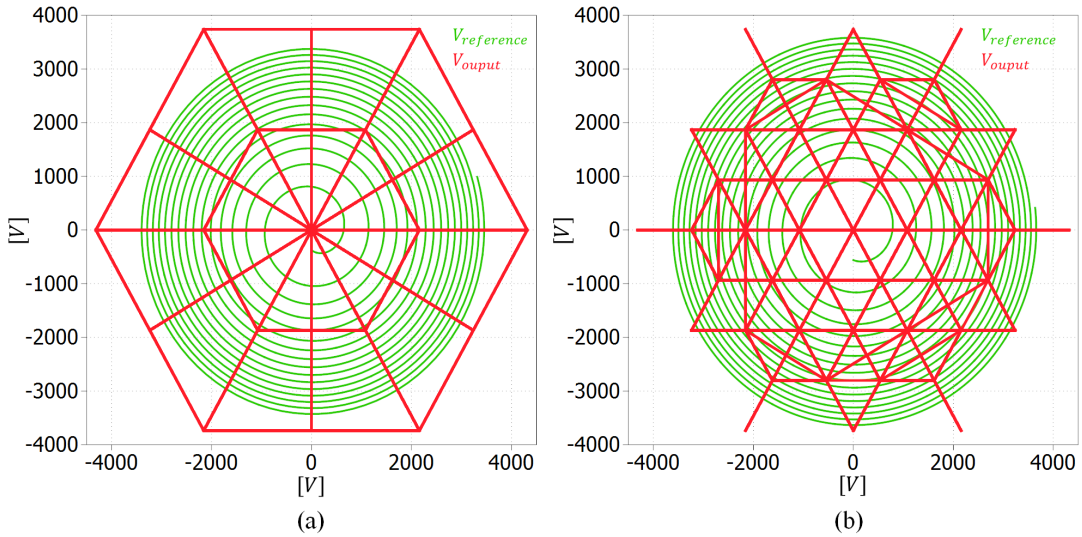


FIGURE 3.19: State space diagram of the reference voltage (in green) and the inverter output voltage (in red) ranging from 10% to the nominal voltage and frequency for the (a) carrier-based modulation; (b) space vector modulation.

Figure 3.19 depicts in the state space diagram the states and the transitions from both the carrier-based and the space vector modulation for the nominal operation point. Here one can clearly observe the presence of the bigger steps in the carrier-based modulation when compared to the space vector modulation. In addition, it is possible to compare how the space vector modulation manages the forbidden transitions compared to the space vector modulation that do not take them into account. One can compare the 3.19(b) with the previously defined space vector diagram with the allowed transitions (Figure 3.9). The simulation results shows that the SVM respects the constraints that have been defined, with some exception for the transition between some different modulation triangles/trapeziums. This has been addressed in Section 3.5.2 and occurs due to the lack of an extra degree of freedom to allow a transition between triangles/trapezium using their commom state and respect all the defined requirements for the SVM.

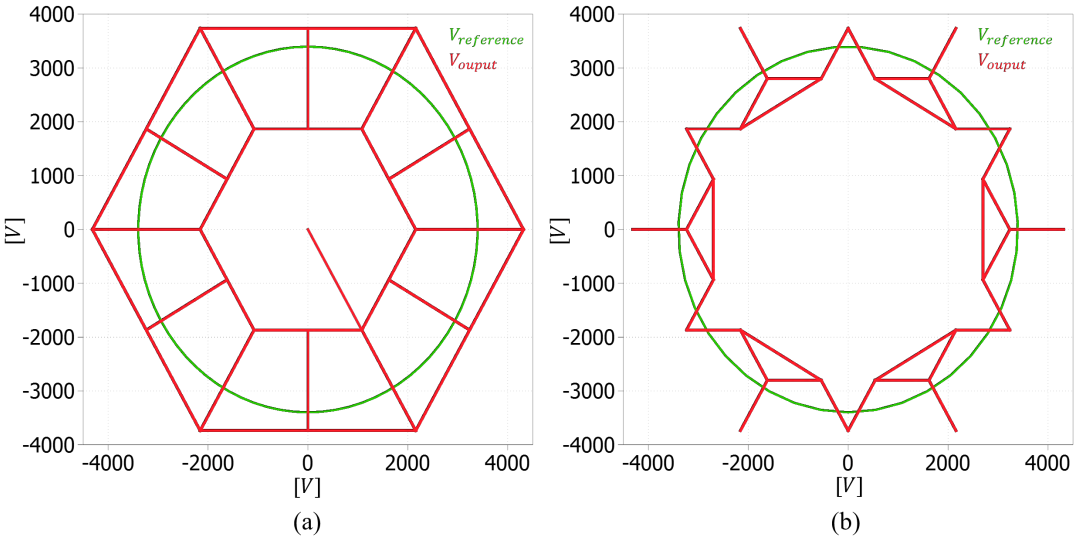


FIGURE 3.20: State space diagram of the reference voltage (in green) and the inverter output voltage (in red) at the nominal conditions for the (a) carrier-based modulation; (b) space vector modulation.

Figure 3.21 shows the line voltage for the carrier-based (a) and space vector modulation. It is possible to see the impact of bigger transitions in the space vector diagram on the voltage waveforms: they are translated as bigger voltage steps in the carrier modulation than in the SVM. The carrier modulation voltage presents a lot of steps that correspond to two or even three voltage levels, while in the SVM they correspond to only one level.

Beyond that, the fact that the carrier-based modulation does bigger steps in the state space diagram and, consequently, uses a bigger surface of the modulation triangles/trapezium has also an effect over the output current ripple. Because of those bigger steps the carrier-based modulation has more important output voltage steps than the space vector modulation generating a bigger current ripple for an equivalent switching frequency. This effect can be seen in the comparison of the current waveforms from both the modulation strategies (Figure 3.21). One can observe also that the carrier-based current waveform has an important distortion around the intersection between the phases. This distortion is caused by the transition between the output voltage produced by the chopper and the inverter leg. This transition represents an important variation in the equivalent duty cycle and switching frequency seen by the load. On the other hand, in the SVM these transitions are much smoother and no distortion can be seen in its current waveform.

The difference in the current ripple and the distortion between each modulation represents also an important difference in the harmonics content of these current waveforms. Figure 3.22 shows a comparison between the harmonics content of the carrier-based (a) and SVM (b) output currents. The carrier modulation presents harmonics with a much bigger amplitude than the SVM. However, the most important difference is the order of the harmonics between the two modulations: The carrier modulation presents big harmonics at lower order (in particular the $5th$ and the $7th$), while the most important amplitudes of the SVM are around the switching frequency. The carrier-based modulation also presents important harmonics around the switching frequency and twice the switching frequency.

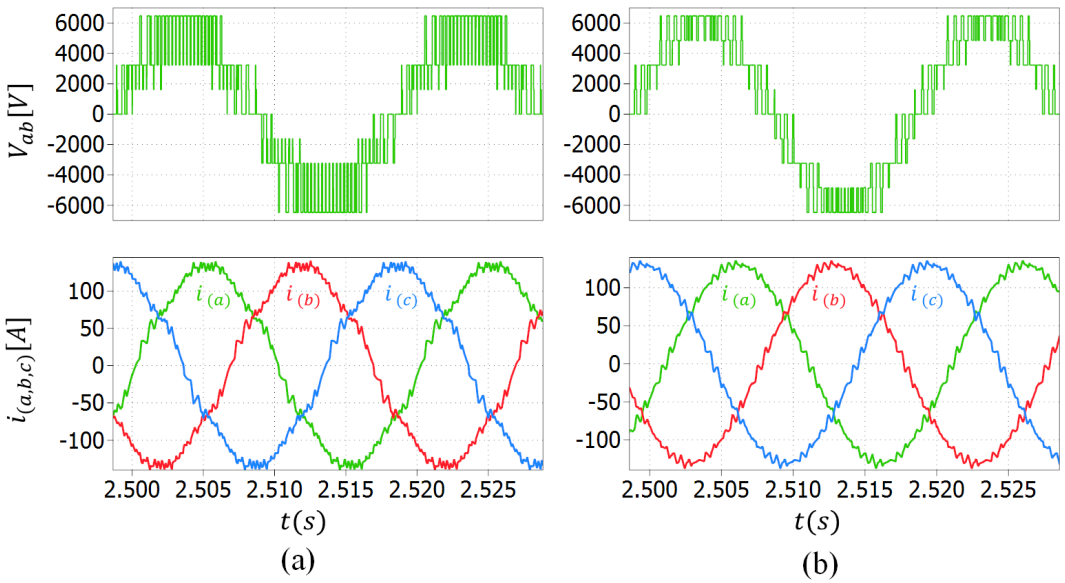


FIGURE 3.21: Multi-level voltage of the node a to the node b and output phase currents for the (a) carrier-based modulation; (b) space vector modulation.

There are two main drawbacks of these low order harmonics: they produce an important distortion in the current waveform (as seen before) producing important vibration in the motor shaft reducing its lifetime and increasing the noise and, in the grid side, the low order harmonics are more difficult to filter demanding bigger filter components increasing the weight, volume, cost and losses.

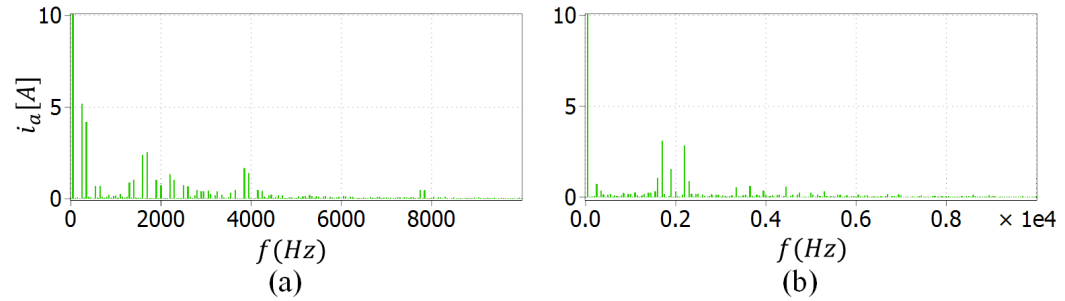


FIGURE 3.22: Output current harmonics for the (a) carrier-based modulation; (b) space vector modulation.

3.5.4 Conclusion

Two modulation schemes for the multiplexed topology applied to the medium voltage power drives have been developed to highlight the main advantages of this topology: a carrier-based modulation scheme and a space vector modulation scheme.

The carrier-based modulation is able to reduce the HV semiconductors efforts through the working principle of the topology and the minimization of the switched voltage. The modulation scheme has been able to impose at least one of the commutation to occur at reduced voltage, this reduced voltage being zero at low modulation depth. However, this modulation scheme has also revealed to be much more complicated

than a classical carrier-based modulation in terms of implementation and duty cycle calculation. This topology presents a lot of degrees of freedom that allow finding different strategies to achieve the main objective of the modulation, but then the strategy may become very complex. The developed schemes are the simplest that could be developed to fulfil the objectives and they have already demonstrated the complexity of a carrier-based modulation for this topology. Other schemes could be applied to this topology to best use its degrees of freedom as, for example, a scheme based only on variable phase triangular carriers for the chopper and the inverter could maximize the duty cycles in which both commutations occur at reduced voltage but calculation of duty cycles would be even more complicated.

The SVM has also demonstrated that is able to reduce the HV semiconductors efforts, always switching at a reduced voltage, although it is not able to switch at zero voltage, thus, having a worst performance in terms of the HV semiconductors efforts at low modulation depth when compared to the carrier-based modulation. On the other hand, because the SVM scheme forbids more than one commutation at the same transition it reduces the overall losses of the converter, also reducing the efforts of the chopper switches. In terms of complexity the space vector modulation scheme is more complicated than a conventional scheme because of its particular modulation triangles/trapezium and the criteria used to define the states transitions. Nevertheless, this scheme takes advantage of sharing a good part of a conventional SVM calculation and implementation process.

Besides its increased complexity, the major drawback of the carrier-based modulation scheme that has been developed is its poor waveform quality when compared to the space vector modulation. SVM provides a current waveform with less low order harmonics and a much better waveform quality, and output voltage with much smoother voltage transitions. In summary, the SVM scheme, associated with its effective flying capacitor balance strategy, is much more interesting and well adapted to this application and its requirements.

Chapter 4

Inverter Design and Experimental Results

4.1 Introduction

In the previous chapters, the multiplexed topology has been introduced and applied to 4.16 kV and 6.6 kV drives. Two different modulations schemes have been proposed to reduce, principally, the HV semiconductors switching efforts. Besides the topology's particular working principle, the switching efforts' reduction has been based on the commutation at reduced voltage and it has been assumed that the switching energies vary linearly with the switched voltage.

Both proposed structures are based on the series connection of 1.7 kV IGBTs in the chopper stage to reduce the use of HV IGBTs and allow a higher switching frequency, thus reducing the size of the flying capacitors. The inverter of 4.16 kV drive uses 6.5 kV semiconductors and the inverter of the 6.6 kV drive is based on the series connection of 4.5 kV IGBTs to withstand the converter's bus voltage.

When constructing such drives, it should be understood that the inverter stage will certainly include a large stray inductance and it must be checked that it is s compatible with the switching times of HV IGBTs.

In order to validate the principles and designs described three different test benches have been developed and two different silicon carbide (SiC) MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) (2 kV and 3.3 kV) have been characterized to allow comparison with the switching performance of the series-connected 1.7 kV IGBTs.

Finally, at the end of this chapter the design of a 4.16 $kV/700$ kVA inverter and its corresponding grid filter will be described and the experimental results of the semiconductors switching characterization will be used to determine the converter losses distribution, the efficiency and evaluate the different modulation schemes.

4.2 1.7kV IGBTs series connection

As presented in Chapter 2, the series connection of 1.7 kV is crucial for the competitiveness of the multiplexed topology in terms of semiconductors cost and for reducing the size of the flying capacitors. Therefore, it is essential to characterize the performances that can be reach with series connection of these IGBTs. In the series connection of the IGBTs it is important to balance the voltage and, consequently, the switching losses of the IGBTs. The most important feature is the dynamic balance

of the IGBTs' voltage, i.e., the voltage during the commutation. Balanced dynamic voltages are needed to ensure that the maximum voltage is not exceeded. Voltage balance is also needed to obtain balanced switching losses. And static voltage balance is also desired to balance the dynamic voltage at turn-on because it provides balanced initial condition.

The power semiconductors parameter spread and the gate drivers delay are the principal causes of voltage unbalance. In order to reduce the semiconductors device spread, the IGBTs series-connected uses IGBTs of the same modules. Initially we hoped that it would reduce the dispersion of electrical parameters because dies would come from the same wafer or at least same batch; we later learnt from the manufacturer that it cannot be guaranteed. At least using IGBTs of the same module has the advantage of increasing thermal coupling which can help. A gate driver based on a pulse transformer has been chosen to drive both the IGBTs from the power module and maximize the synchronization of the gate pulses. Moreover, the gate driver supplies a regulated gate voltage to the IGBTs to reduce the voltage unbalance that it can cause. However, other mitigation methods have to be used to ensure the safe and robust operation of the power semiconductors.

The steady-state (static) voltage unbalance of the IGBTs is minimized by adding a resistor in parallel with each series-connected IGBT [66]. This resistor needs to have a high value to minimize its losses but a value low enough to ensure a current ten times higher than the leakage current to ensure voltage balance [67].

A passive snubber is often used to help voltage balance of series connected power semiconductors [67]. In this testbench, a resistor-capacitor (RC) snubber will be used. The larger the snubber capacitors, the lower the voltage unbalance between the series-connected IGBTs; however lager capacitor increases both the snubber losses and the commutation time of the semiconductors. Therefore, a trade-off between the snubber capacitance (consequently the voltage unbalance) and the snubber losses needs to be done. The literature [68] recommends a capacitance value given by Equation 4.1.

$$C_{snubber} = \frac{i_L \cdot t_f}{2V_d} \tag{4.1}$$

Where t_f denotes the fall time of the IGBT, i_L stands for the load current, andV_d is the voltage to be allowed to rise at the time t_f .

Equation 4.2 gives the energy lost in the snubber circuit (resistor) at each period as a function of the snubber capacitance $C_{snubber}$, the switched voltage V and the number of semiconductors in series n_s.

$$E_{snubber} = n_s \cdot C_{snubber} \cdot V^2 \tag{4.2}$$

To limit the snubber size (and losses) and to have a better voltage balance, other mitigation methods are also present in the gate driver. The gate driver presents a dv/dt circuit that limits the switching speed of the IGBTs and consequently reduces the final voltage unbalance. An active clamping function is also included in the driver to limit the maximum voltage of each of the series-connected IGBTs; if the previous methods act properly active clamping should only be activated in extreme cases.

To conclude, the desaturation function of the series-connected IGBTs are interconnected to synchronize the turn-off of both IGBTs when protection trips. Otherwise, one of the IGBTs might try to turn off alone and the consequences would be terrible.

Figure 4.1 shows the testbench scheme used to test and characterize the series connection of the 1.7kV IGBTs. The testbench comprises a reversible DC source, the DC bus capacitors and an H bridge with an inductive load. The left leg of the H bridge is composed of two strings of two 1.7 kV IGBTs series-connected. The right side leg is composed of 3.3kV SiC MOSFETs that will be used as reference design. This testbench has been conceived to realize double pulse test characterization of the power semiconductors. However, with an appropriate control, it can be used to measure the semiconductors' losses under continuous switching and a sinusoidal current. In the scheme, one can also observe the resistors and the RC snubbers used, respectively, for the steady-state and transient voltage balance. The RC snubber capacitors present in the scheme are lower than the value recommended by the literature. However, it has been checked that when combined with the other mitigation methods they provide a sufficient voltage balance and of course this reduced capacitor value reduces the losses in the resistor.

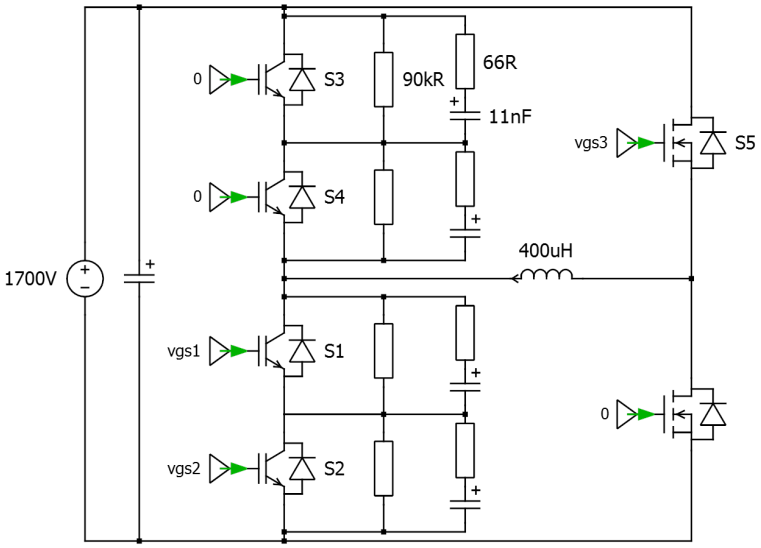


FIGURE 4.1: Testbench scheme for the characterization of series-connected 1.7 kV IGBTs and 3.3 kV SiC MOSFETs.

Figure 4.2 (a) shows the testbench used to characterize 1.7 kV IGBTs (CM300DY-34T - 300 A) series-connected and the 3.3 kV SiC MOSFETs (FMF375DC-66A - 375 A). Most of the elements of the testbench are identified in the image. The series-connected IGBTs are mounted over a heating plate that is used to characterize the components at different temperatures. If necessary, this heating plate can be replaced by a liquid cold plate heatsink in which it is possible to measure the power modules losses when switching continuously.

Figure 4.2 (b) illustrates a 3D view of the layout of the busbar PCB. Special attention has been given to the placement of the 1.7 kV power modules to have the same distances between the modules of this testbench as in the full inverter to have realistic stray inductances. In the inverter, however, the stray inductances will be higher than in this case because it will be a laminated busbar. The laminated busbar has different mechanical limitations from a PCB and the standard corresponding to medium voltage power drives will be applied to its design, increasing the distance between the

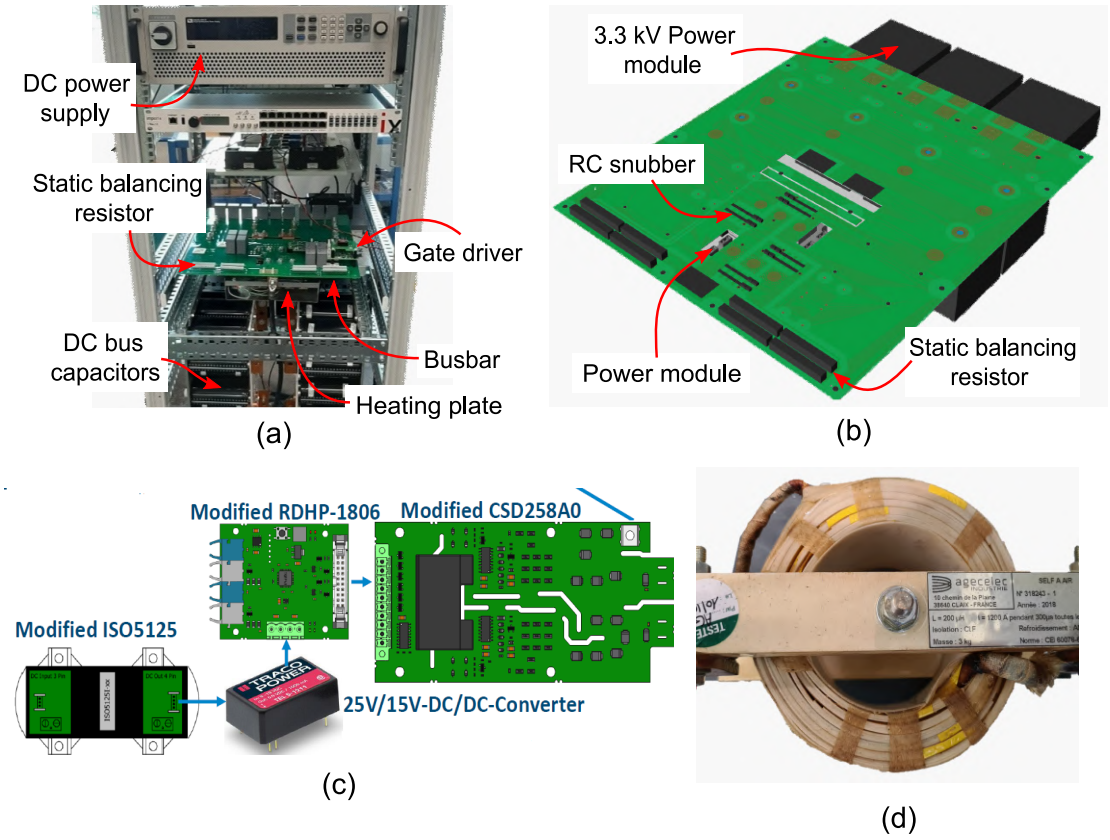


FIGURE 4.2: (a) Testbench for the characterization of series-connected 1.7 kV IGBTs; (b) 3D view of the testbench busbar PCB; (c) gate driver solution to drive the series-connected 1.7 kV IGBTs; (d) 200 μF air-core inductance used in the double-pulse test.

layers. One can observe in this figure the placement of the RC snubbers, the static balancing resistors and the power modules (1.7 kV IGBTs and 3.3 kV MOSFETs)

Figure 4.2 (c) displays the gate driver solution used for the series-connected 1.7 kV IGBTs. It consists of an insulated power supply to withstand the whole voltage of the final converter, a DC-DC converter, an optical fiber interface to isolate the control stage from the power stage and the dual-gate driver used to drive both the series-connected IGBTs of the same power module.

Finally, figure 4.2 (d) shows one of the air-core inductances used as a load for the double-pulse test. Two inductances have been series-connected for the characterizations totaling an inductance of 400 μH.

4.2.1 Series-connected 1.7 kV IGBTs characterization

Figure 4.3 shows the entire double pulse test waveforms used to characterize the series-connected IGBTs. In these waveforms, it is possible to see the different stages of the test. It begins with all the IGBTs blocked and an inductor current of 0 A. Then the devices under test (DUTs) are turned on, applying a voltage to the inductor, and the current starts to rise till it reaches the desired value to realize the measurements. When the current reaches the desired value, the DUTs are turned off and the turn-off energy can be measured. After that, the DUTs receives another short turn-on pulse to measure its turn-on energy. At this moment, it is possible to measure the reverse recovery energy from the complementary diodes of the switching cell. Because this

test bench uses an H bridge configuration, the MOSFET is turned on with the DUTs when the current starts to rise and is still on until the end of the double pulse test. After that, it is turned off and, because of the freewheeling path, a voltage with an opposite polarity of the one on the rising stage is applied to the inductor causing the current to decrease to zero.

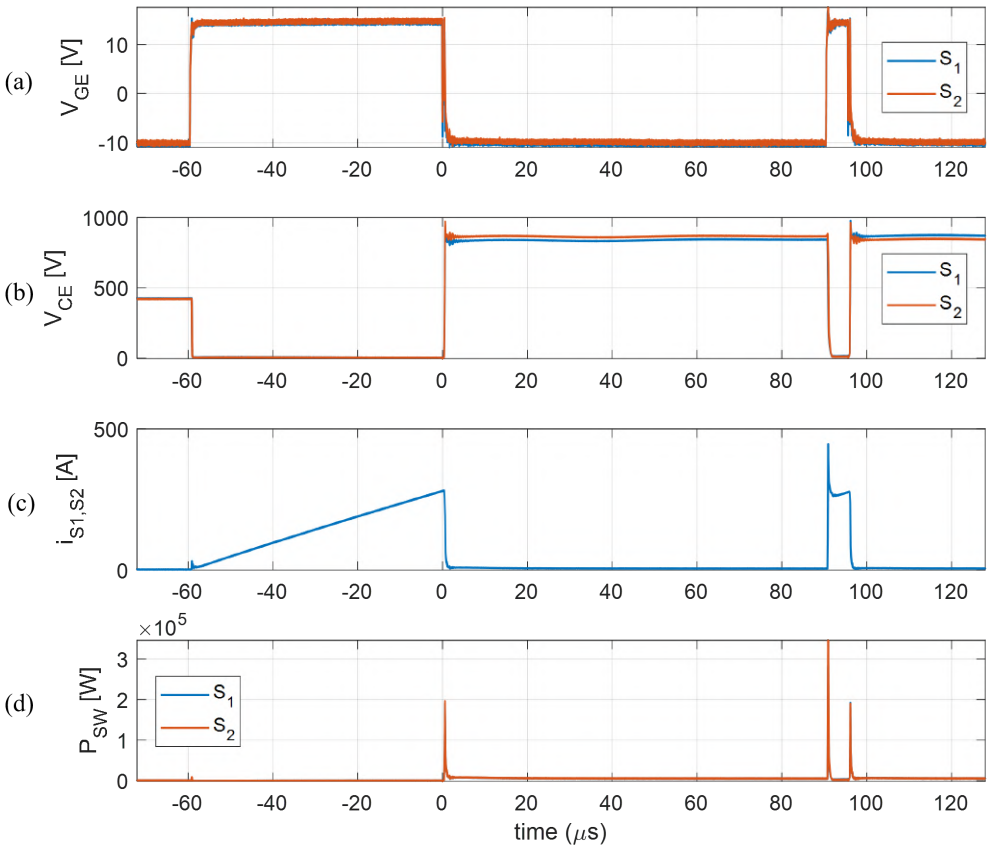


FIGURE 4.3: Double-pulse test waveforms for the characterization of series-connected 1.7 kV IGBTs at 25 $°C$ and 300 A. (a) Gate voltages; (b) collector-emitter voltage; (c) collector-emitter current; (d) switches power.

Figure 4.4 shows more in detail the turn-on and turn-off commutation of the IGBTs and the turn-off commutation of the diode for two different values of current. Regarding the gate voltages of the series-connected IGBTs it is possible to see that they are well synchronized and supply the gate with the same voltage, which is essential for a good transient voltage balance.

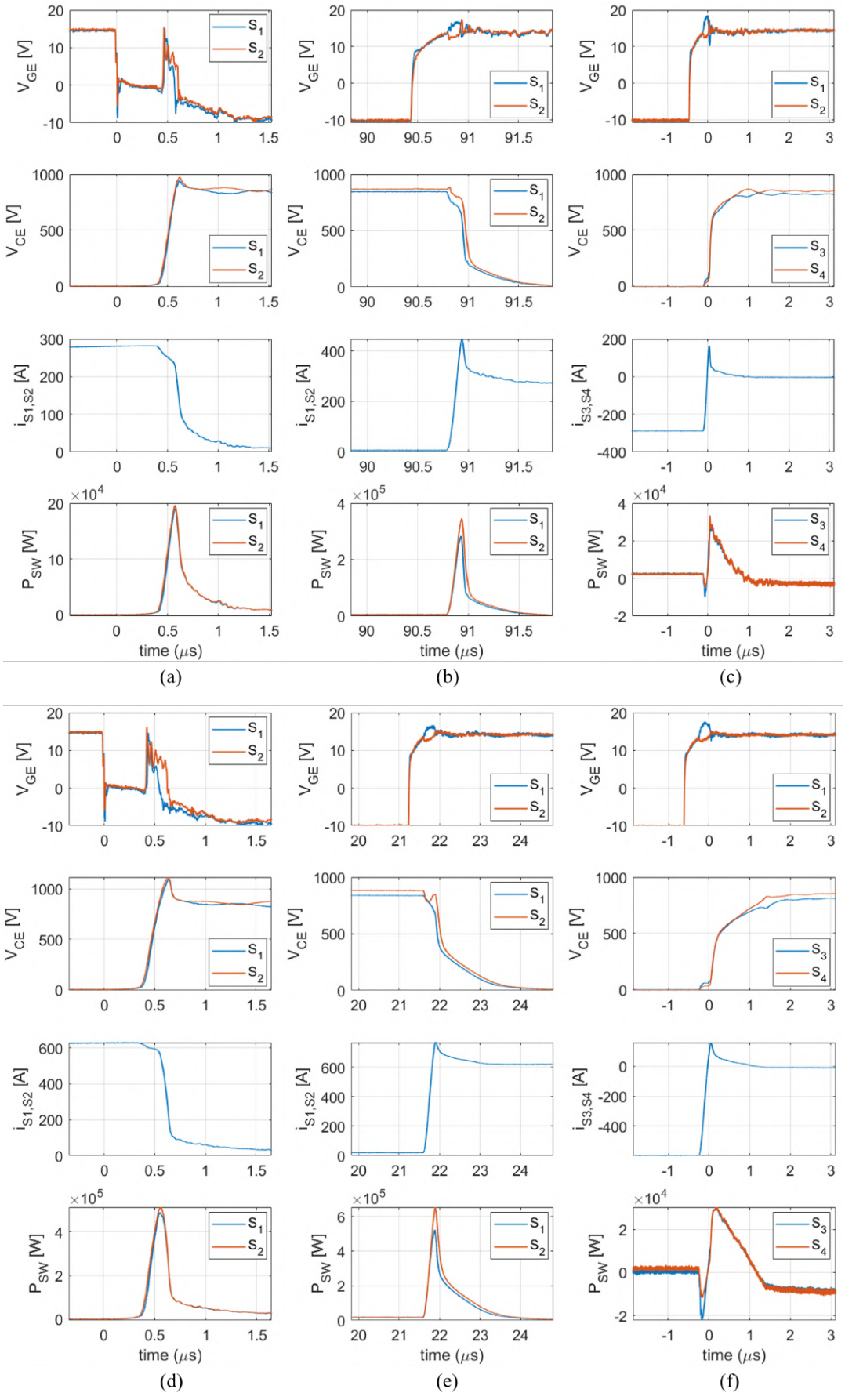


FIGURE 4.4: Commutation waveforms for the characterization of series-connected 1.7 kV IGBTs. $i = 300\ A$, $T = 25\ ^{\circ}C$: (a) Turn-off IGBTs; (b) Turn-on IGBTs; (c) Turn-off IGBTs. $i = 600\ A$, $T = 125\ ^{\circ}C$: (d) Turn-off IGBTs; (e) Turn-on IGBTs; (f) Turn-off IGBTs.

Regarding the turn-off waveforms (Figure 4.4 (a)), one can observe that while the IGBTs voltage is rising, the gate voltage rises for some time. This is the action of the dv/dt feedback and the active clamping circuits controlling the maximum switching speed and overvoltage to ensure the correct transient voltage balance. Therefore, the rising edges of the collector-emitter voltages of the series-connected IGBTs are well synchronized, rising at an almost identical rate and having similar overvoltages. Consequently, one can observe that the instantaneous switching power of series-connected semiconductors are the same.

Although the gate voltages are well synchronized for the turn-on waveforms, the collector-emitter voltages are less symmetric than for the turn-off commutation. It is possible to see that the voltage drop due to the stray inductances, when the current is rising, is uneven between the two IGBTs. This already affects the switching energies because one starts to switch at a lower level than the other. Moreover, even though both switches have a similar collector-emitter voltage falling rate, their voltage falling edge is not as well synchronized as the rising edge. Therefore, for the turn-on commutation, the instantaneous power of both switches is similar but not as even as for the turn-on. The switching energy unbalance will be studied afterward.

Finally, one can observe that the turn-off commutations of the diodes are as well synchronized as for the IGBTs. Thus, the instantaneous switching powers of series-connected diodes are really close.

Figure 4.5 shows a closer look at the turn-off stages of the double-pulse test for two different current values and temperatures. In these waveforms, it is possible to observe the static voltage balance between the IGBTs. The static voltage of the IGBTs are not similar, but they are really close. One can observe that the unbalance voltage increases with the switched current and the semiconductors' temperature. The maximum voltage unbalance switching two times the nominal current at 125 $^{\circ}C$ is 40 V compared to the reference voltage (850 V). This unbalance corresponds to 2.5% of the reference voltage, representing an excellent static voltage balance.

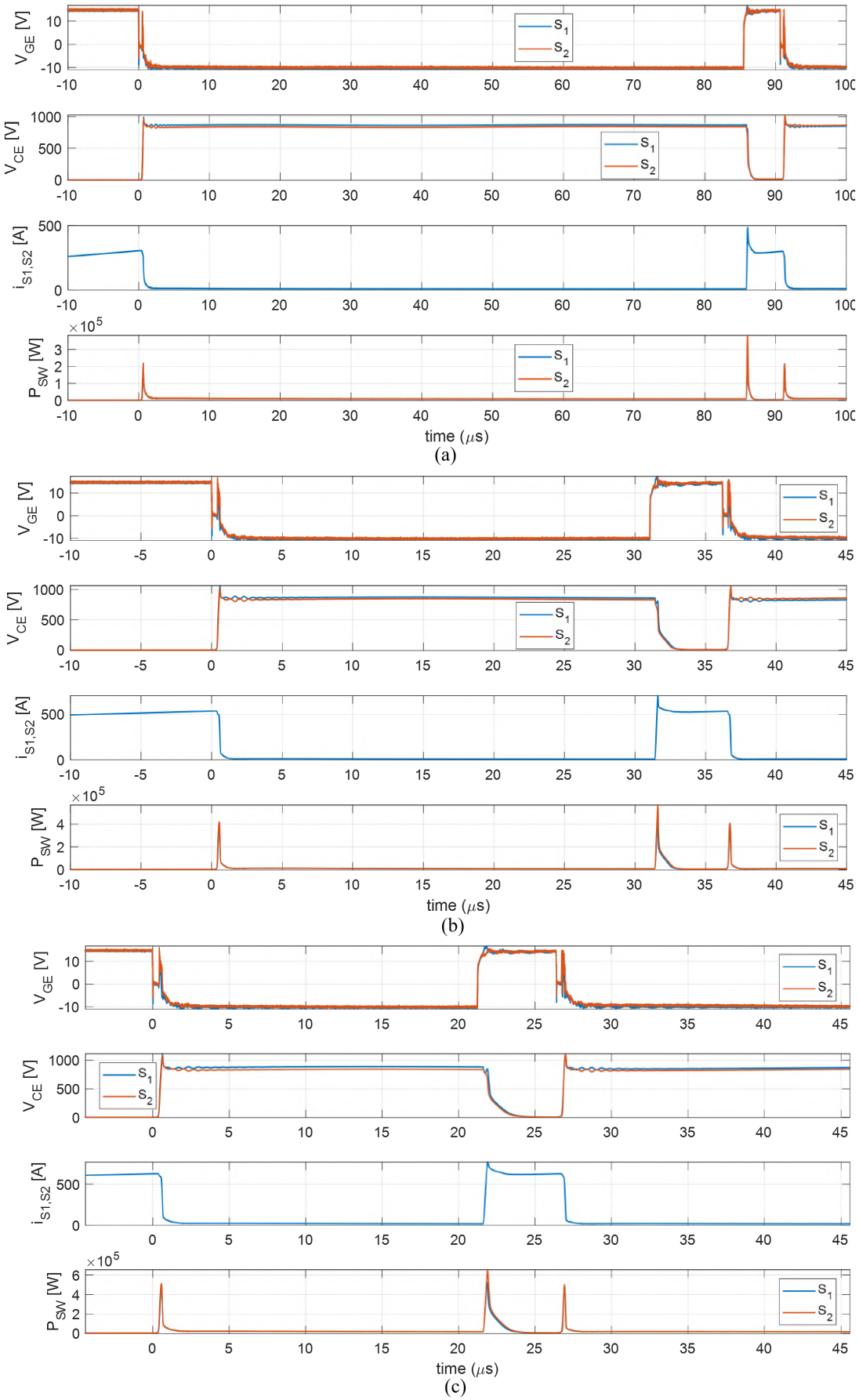


FIGURE 4.5: Turn-off stage waveforms of the double-pulse test. (a) $i = 300\ A$, $T = 125\ ^{\circ}C$; (b) $i = 600\ A$, $T = 25\ ^{\circ}C$; (c) $i = 600\ A$, $T = 125\ ^{\circ}C$.

Figure 4.6 shows the switching energies of each of the 1.7 kV series-connected IGBTs versus the current for two different temperatures. These graphics show more in detail that the unbalance of the turn-on losses is more significant than the unbalance of the turn-off losses. Moreover, the energy unbalances, an image of voltage unbalances, increase with the switched current and the temperature. The turn-on energy unbalance at the nominal current and 125 $°C$ is 7.5% and the turn-off unbalance is 5%. The reverse recovery energy of the diodes has been represented only by the average value because the unbalance is very low (2%). Consequently, even though some unbalance can be observed between the series-connected semiconductors, these energy unbalances are low and will not represent a relevant difference in the semiconductor losses, validating the series connection of the 1.7 kV IGBTs.

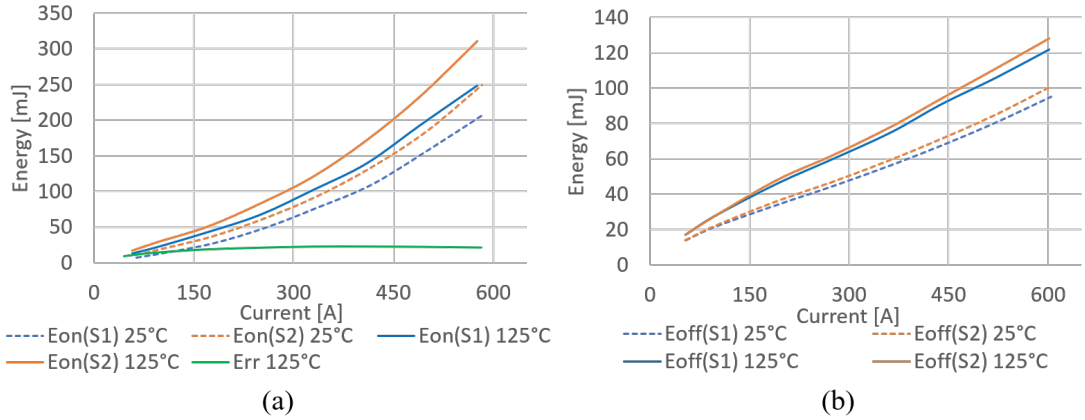


FIGURE 4.6: Switching energies of the 1.7 kV series-connected IGBTs at 25 $°C$ and 125 $°C$: (a) turn-on and reverse recovery energies; (b) turn-off energies.

To conclude, the measured switching energies of the IGBTs and the diodes are close to the datasheet values, which means that the action of the unbalance mitigation methods used (dv/dt feedback , active clamping and RC snubber) do not have a major impact on them.

4.2.2 3.3 kV SiC MOSFET characterization

This testbench has also been used to characterize the 3.3 kV SiC MOSFETs (FMF375DC-66A - 375 A). However, these semiconductors have not been characterized in temperature like the IGBTs. Figure 4.7 shows the turn-on and turn-off commutations of the MOSFET transistors.

Figure 4.8 shows the switching energy of the 3.3 kV MOSFETs versus current. One can observe that the turn-off energy of the 3.3 kV MOSFET transistor is the same as the turn-off energy of 1.7 kV, wichillustrates quite well the advantage of the SiC technology. However, the turn-on energy of one MOSFET and two IGBTs are almost similar. This significant energy is a consequence of the slow turn-on commutation of the MOSFET. On the other side, the transistor's switching speed could not be increased because an external gate resistor of zero Ohm was used, being limited by the internal gate resistor of the power module. Besides that, the MOSFET presents a low overvoltage and almost no oscillations during the commutation.

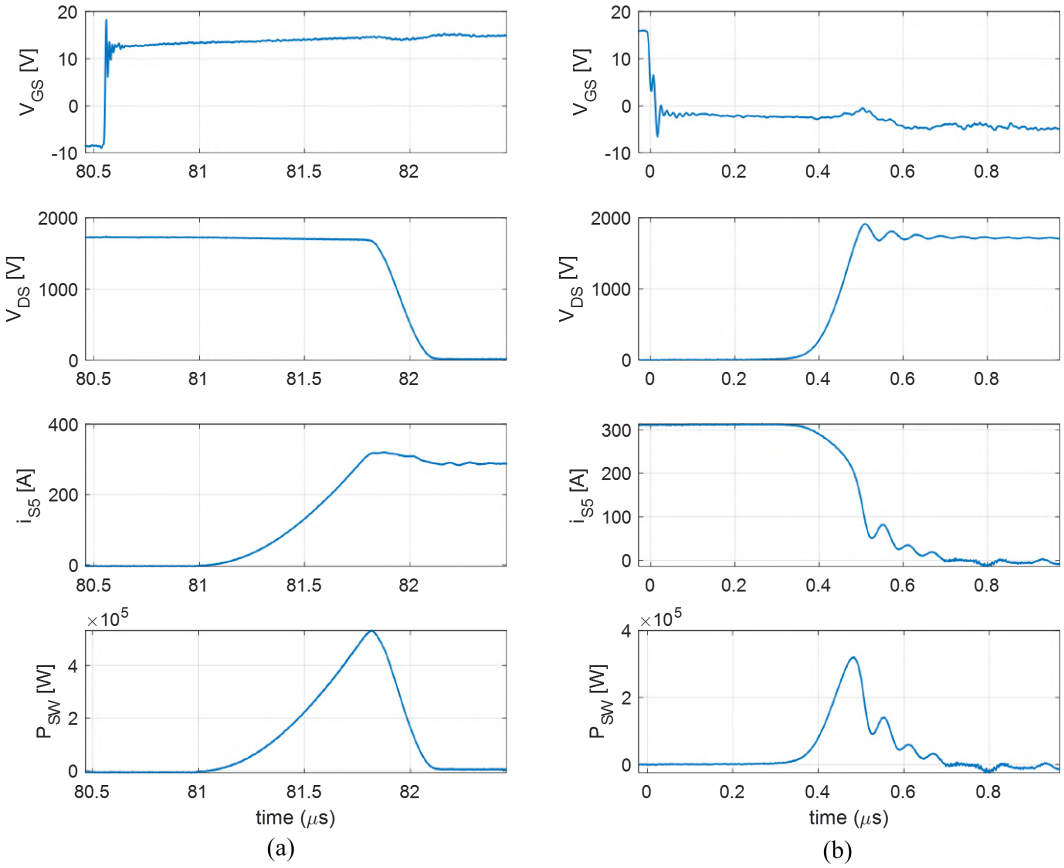


FIGURE 4.7: Commutation waveforms for the characterization of 3.3 kV SiC MOSFETs. $i = 300\ A$, $T = 25\ ^{\circ}C$: (a) Turn-on; (b) Turn-off.

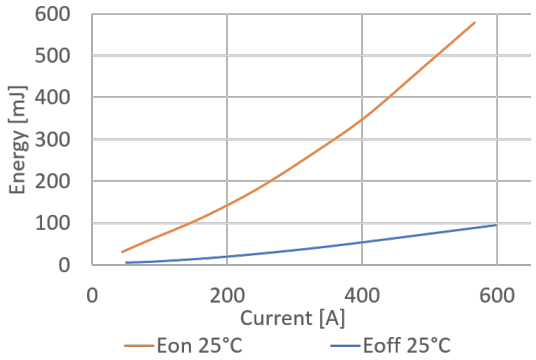


FIGURE 4.8: Switching energies (turn-on and turn-off) of the 3.3 kV SiC MOSFETs at 25 $^{\circ}C$.

4.2.3 Series-connected 2.2 kV SiC MOSFETs characterization

Finally, the testbench has been used to test the 2 kV SiC MOSFETs. The interest in testing these power modules is that they can be a direct evolution of the proposed schematic of Chapter 2 (Figure 2.6), replacing the 1.7 kV IGBTs. Figure 4.9 shows the switching energies of each series-connected MOSFET of the FF4MR20KM1H power module as a current function and for two temperatures (25 $^{\circ}C$ and 125 $^{\circ}C$). Although using the same gate driver (compatible with IGBTs and SiC MOSFETs) and unbalance mitigations methods, the MOSFETs present higher energy unbalance than the

IGBTs. The turn-on energy unbalance at the nominal current and 125 $°C$ is 16.3% and the turn-off unbalance is 9.8%. The reverse recovery energy of the diodes has been represented only by the average value because the unbalance is negligible. This more significant energy unbalance may need more efficient voltage to unbalance mitigation method adapted to high-speed transistors for a better loss equalization between the series-connected MOSFETs.

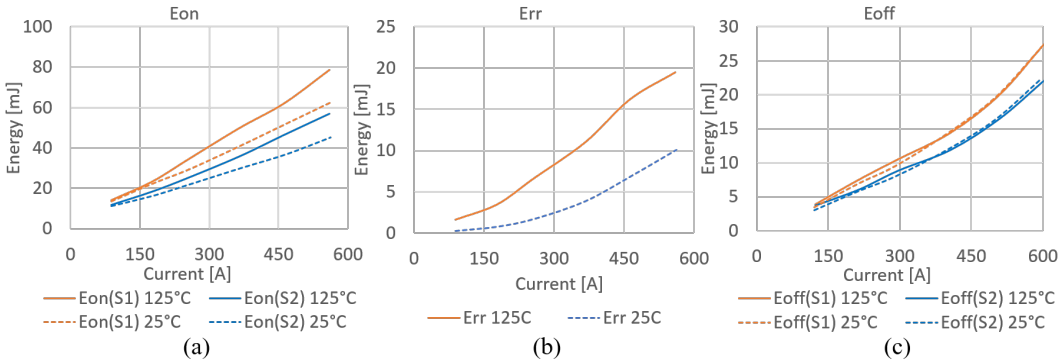


FIGURE 4.9: Switching energies of the 2 kV series-connected SiC MOSFETs at 25 $°C$ and 125 $°C$: (a) turn-on energies; (b) reverse recovery energies; (c) turn-off energies.

4.2.4 Comparison

Figure 4.10 (a) compares the total switching energies of the two series-connected 1.7 kV IGBTs, the 3.3 kV MOSFET and the two series-connected 2 kV MOSFETs at 25 $°C$. In terms of switching energy, the 3.3 kV MOSFET transistors do not represent any advantage compared to the series-connected IGBTs. However, for a fair comparison, this comparison needs to consider the energy dissipated by the RC snubber circuits and the static resistors.

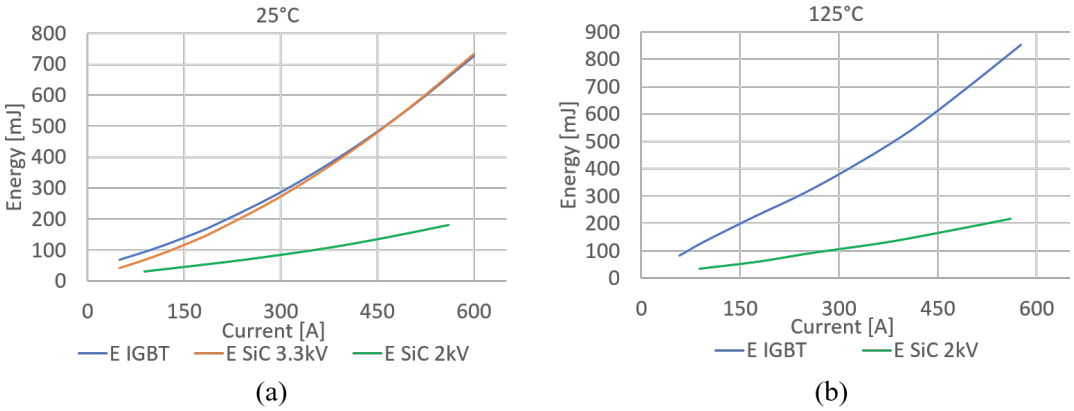


FIGURE 4.10: Comparison between the total switching energies: (a) of the series-connected 1.7 kV IGBTs, the series-connected 2 kV SiC MOSFETs and the 3.3 kVSiC MOSFETs at 25 $°C$; (b) of the series-connected 1.7 kV IGBTs and the series-connected 2 kV SiC MOSFETs at 125 $°C$.

Using the equation 4.2 one can observe that the RC snubber circuit energy dissipated each period for the two series-connected IGBTs is 20 mJ, which is negligible compared to the switching energy of the semiconductors, not changing the previous

conclusion. The same conclusion can be achieved when calculating the power dissipated by the resistor used for the static voltage balance. For two series-connected IGBTs with a duty cycle of 50% the power dissipated is 10 W, which is negligible compared with the energy dissipated by each power module, as will be demonstrated afterward.

On the other side, comparing the series-connected 1.7 kV IGBTs and 2 kV MOSFETs at 125 $^{\circ}C$ (Figure 4.10 (b)) is possible to see that in terms of switching energies, the SiC MOSFETs is very advantageous reducing the total switching energy by a factor of four.

As the 1.7 kV IGBTs the use of 2 kV MOSFETs adds the complexity of a series connection of power semiconductors and the extra losses of the unbalance mitigation circuits. On the other side, the use of 3.3 kV MOSFETs reduces the number of power modules, reducing the complexity and the volume of the chopper stage, and allowing a layout with lower stray inductances.

4.3 4.5kV IGBTs series connection

In Chapter 2, it has been seen that the 6.6 kV converter needs the use of 4.5 kV semiconductors series-connected in the inverter stage to withstand the application's bus voltage. Therefore, it is essential to test and validate the series connection of these IGBTs. As for the 1.7 kV IGBTs, in this case, it is also essential to verify the static and dynamic voltage balance of the series-connected semiconductors to validate the performance of the gate driver, the RC snubber and the static resistors. Besides that, these semiconductors will realize commutations at reduced voltage, as seen in Chapter 3, and it is necessary to validate this aspect and verify the linearity of the switching energies with the switched voltage.

The testbench for the 4.5kV IGBTs series-connected is also an H bridge, as shown in Figure 4.11. In the figure, one can observe the testbench scheme, with the series-connected semiconductors, the RC snubbers and the static resistors with their respective values.

Figure 4.12 shows the laminated busbar for the 4.5kV IGBTs series-connected testbench. The busbar consists of a two-layer structure that has been conceived according to the international standard IEC 61800-5-1 [69]. The main elements of this testbench and the external connections (DC supply, inductive load) are identified in the figure.

For the characterization of the series-connected 4.5kV IGBTs (FF400R45 - 400 A), three different voltages have been used: 5.4 kV, 3.6 kV and 1.8 kV. Those voltages correspond to the voltages that the inverter arm semiconductors will switch in the 6.6 kV structure (these voltages correspond to the voltage levels delivered by the chopper stage). The semiconductors have been tested at 25 $^{\circ}C$ and 125 $^{\circ}C$, but only the results at 125 $^{\circ}C$ will be presented because they are closer to their operating temperature in the converter.

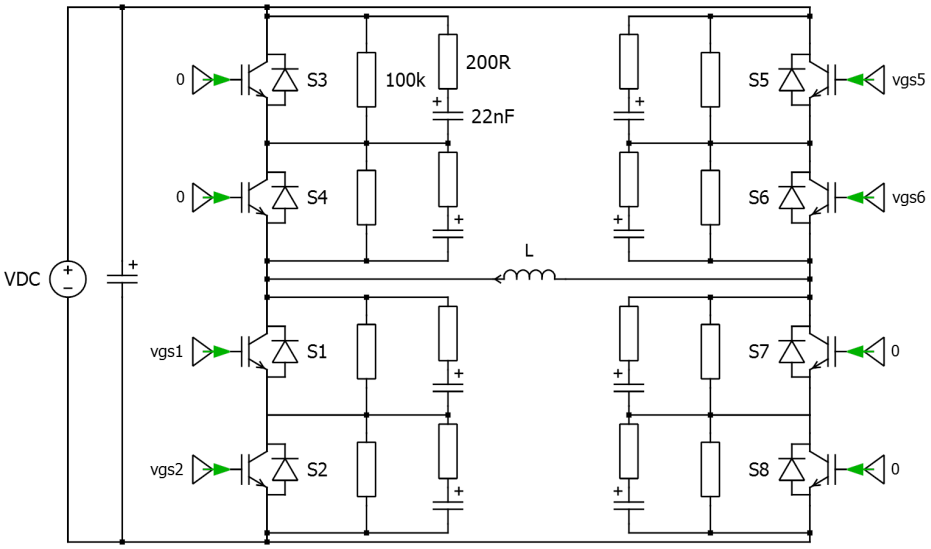
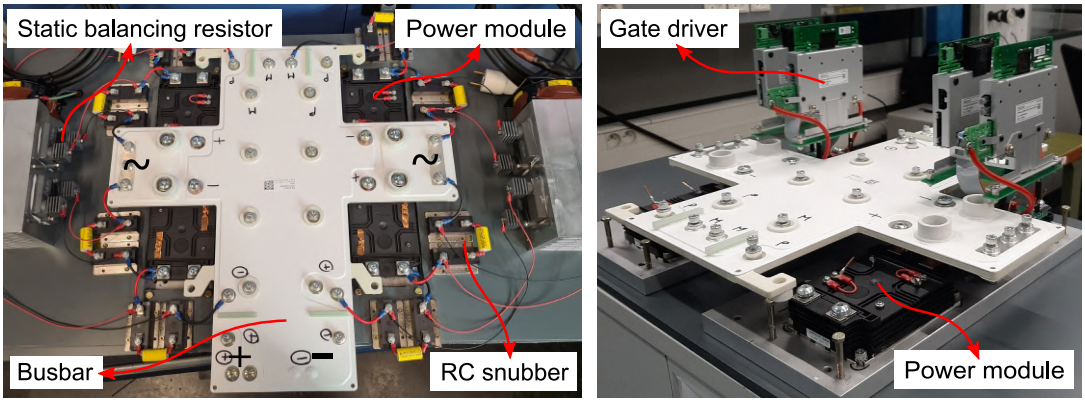


FIGURE 4.11: Testbench scheme for the characterization of series-connected 4.5 *kV* IGBTs.



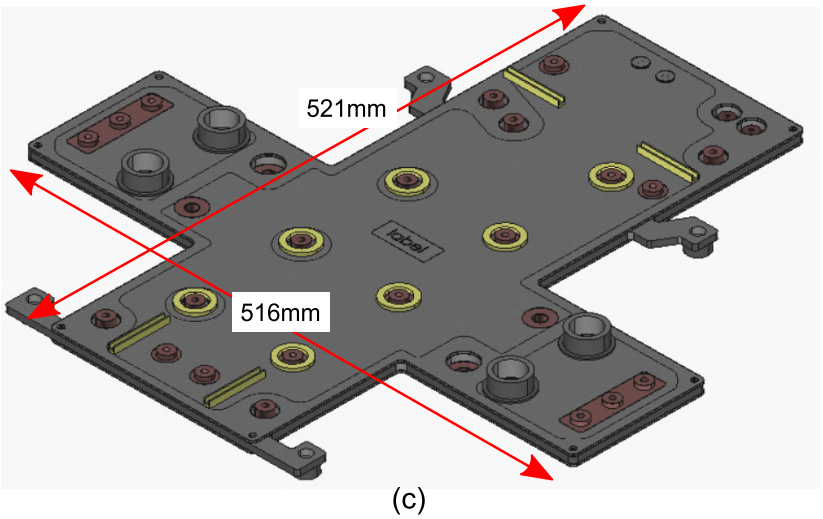


FIGURE 4.12: (a), (b) Testbench for the characterization of series-connected 4.5 *kV* IGBTs; (c) 3D view of the testbench laminated busbar with its dimensions.

4.3.1 Series-connected 4.5 kV IGBTs characterization

Figure 4.13 shows the double pulse waveforms of the series-connected 4.5 kV IGBTs for three different switched voltages (5.4 kV, 3.6 kV and 1.8 kV) at 125 $^{\circ}C$. One can observe that the voltages of the two series-connected IGBTs are very similar and, consequently, the losses are analogous. Table 4.1 shows the maximum voltage at 1.5 times the nominal current (limit of the SOA) and the static voltage unbalance between the IGBTs. These results reveal that the maximum voltage of the series-connected IGBTs is far from the safety limits of the semiconductor. Due to the large margin that the maximum voltage offers, the active clamping feature of the gate driver can be avoided to reduce cost if it does not affect the robustness of the structure.

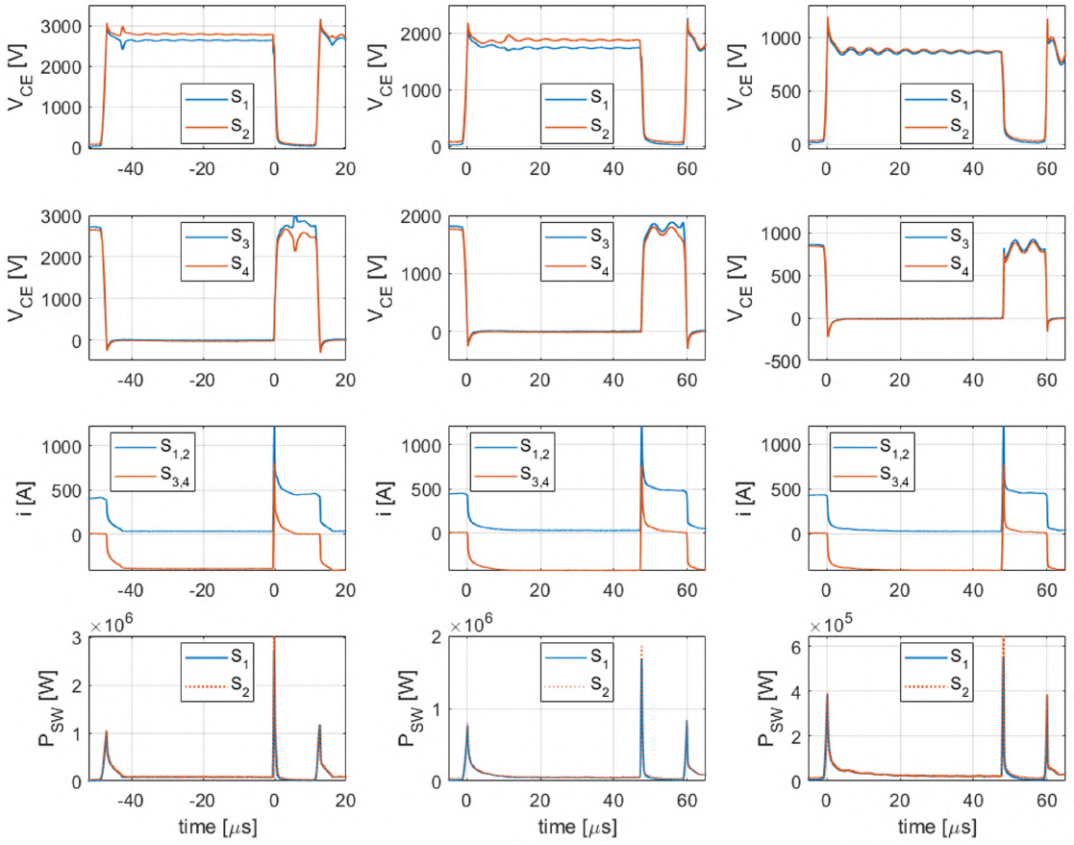


FIGURE 4.13: Double-pulse test waveforms for the characterization of series-connected 4.7 kV IGBTs at 400 A, 125 $^{\circ}C$ and different bus voltages: (a) 5.4 kV; (b) 3.6 kV; (c) 1.8 kV.

TABLE 4.1: Series-connected 4.5 kV IGBTs overvoltage and voltage unbalance.

Switched voltage	V_{max}@600A	ΔV_{ce}@400A
5400 V	3.20 kV	3%
3600 V	2.22 kV	4%
1800 V	1.20 kV	1%

Figure 4.14 shows more in detail the turn-on and turn-off commutation of the IGBTs and the diodes. Regarding the turn-off waveforms (Figure 4.14 (a)), one can observe

that the rising edges of the collector-emitter voltages of the series-connected IGBTs are well synchronized, rising at an almost identical rate and having similar overvoltages. Consequently, one can observe that the instantaneous switching power of series-connected semiconductors are the same. The collector-emitter voltages are less symmetric for the turn-on commutation (Figure 4.14 (b)). Their voltage falling edge is not as well synchronized as the rising edge and there is still a little static voltage unbalance. Therefore, for the turn-on commutation, the instantaneous power of both switches is similar but not as even as for the turn-on. Finally, one can observe that the turn-off commutations of the diodes are well synchronized as for the IGBTs, consequently having even losses.

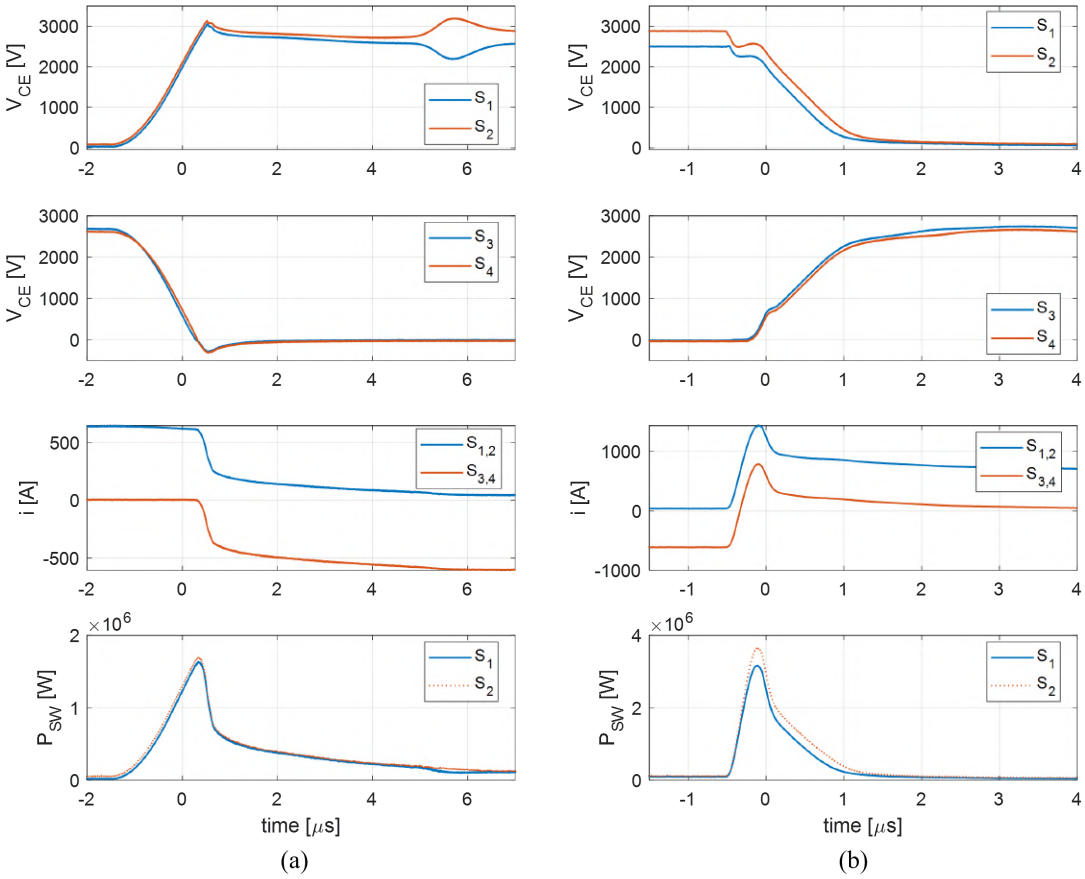


FIGURE 4.14: Commutation waveforms for the characterization of series-connected 4.5 kV IGBTs. $V_{DC} = 5.4\,kV$, $i = 600\,A$, $T = 125\,°C$: (a) Turn-off IGBTs; (b) Turn-on IGBTs.

Figure 4.15 shows the switching energy of the two series-connected devices versus current for a switched voltage of 3600 V. Like for the 1.7 kV IGBTs, one can observe that the energy unbalances at the turn-on commutation are more significant than for the turn-off commutation of the IGBTs or the reverse recovery energy of the diodes. Nevertheless, these switching energy unbalances of 6%, 2.7% , 2.7% for the turn-on, turn-off and reverse recovery energies, respectively, at the nominal current are negligible and will not affect the series connection of the IGBTs. The switching energy unbalances for the other switched voltages are lower than for this case, as shown in figure 4.13, and are not presented. Besides that, the case in which the maximum voltage balance is present is already a case where the converter is switching at reduced voltage and the switching efforts are reduced.

Figure 4.16 shows the switching energy as a current function for different switched

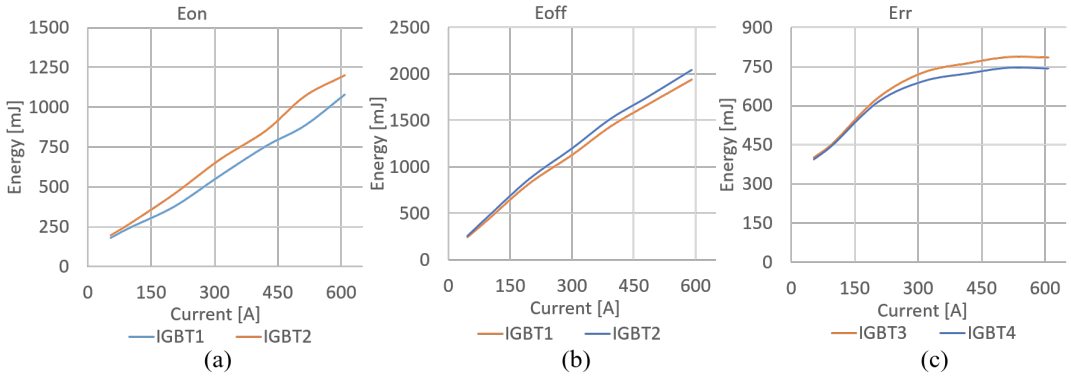


FIGURE 4.15: Switching energies of the two 4.5 kV series-connected IGBTs at $V_{DC} = 3.6\ kV$ and $T = 125\ °C$: (a) turn-on energies; (b) turn-off energies; (c) reverse recovery energies.

voltage values. These results validate that the switching energies vary proportionally to the switched voltage. At nominal current, when switching 2/3 of 5400 V (reference voltage) the ratio between the total switching losses is 64%, i.e. the same ratio as the voltages. However, when switching 1/3 of the reference voltage the ratio between the losses is 25%, i.e., the ratio between the losses is lower than the switched voltage ratio. Consequently, these results confirms a strong advantage of this topology and control: switching a reduced voltage brings significant reduction of switching losses. Moreover, the lower the switched voltage, the more significant the reduction of switching efforts are, reducing the topology losses at low modulation depth.

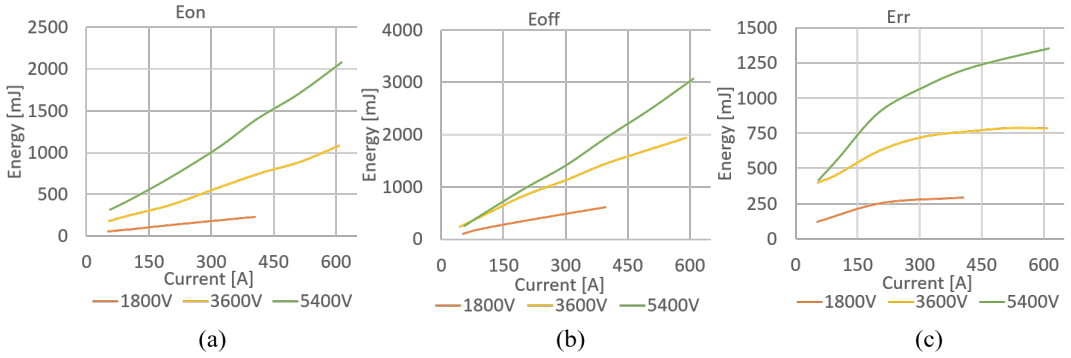


FIGURE 4.16: Switching energies of the 4.5 kV series-connected IGBTs at 125 $°C$ for three different switched voltages: (a) turn-on energies; (b) turn-off energies; (c) reverse recovery energies.

In conclusion, the measured switching energies correspond to the datasheet values of the device, showing that the used RC snubber to the dynamic voltage balance does not affect the switching performances. Besides that, a small side RC snubber has been used for this structure, reducing the switching energy added by this structure. As the inverter arms only switches one-third of the time, the snubber losses will also be reduced. However, they will face losses due to the chopped voltage feed by the chopper stage to the inverter legs. This increase of the snubber losses has not been studied as it needs the development of the SVM for this structure to be appropriately addressed.

4.4 4.16 kV Inverter

In Chapter 2, it has been seen that the 4.16 kV converter needs the use of 6.5 kV semiconductors, and those semiconductors will realize commutations at reduced voltage, as seen in Chapter 3; it is therefore necessary to validate this aspect and verify the linearity of the switching energies with the switched voltage. Moreover, the multiplexed converter based on the association of chopper and inverter stages includes switching cell that can have a high stray inductances and the compatibility with the HV IGBTs switching speed must be checked. Therefore, a dedicated testbench has been realized

The test bench to characterize the 6.5 kV semiconductors and evaluate the stray inductances of the 4.16 kV inverter will be a DC-AC converter, i.e., half the proposed structure of the four-quadrant converter (Figure 2.6). With this testbench it will also be possible, in the future, to test the operation of a full inverter and validate the modulation of this topology.

In this section the sizing of the 4.16 $kV/700\ kVA$ inverter, its grid filter, the inverter busbar, the characterization of the 6.5 kV semiconductors and the evaluation of the stray inductances are described.

4.4.1 Sizing

4.4.1.1 DC bus capacitors and flying capacitors

For the inverter's capacitor sizing there are two main constraints to respect: the Schneider Electric's design rules and the component temperature limitations. The internal design rules recommend the RMS current from the capacitors I_{RMS} to be less than 80% of the nominal RMS current and the maximum voltage to be less than 90% of the rated voltage. On the other hand, the maximum allowed temperature T_{HSmax} determines the maximum losses of the capacitor and, consequently, the maximum RMS current and the voltage ripple ΔV. The maximum losses of the capacitor are given by:

$$P_{cap} = \frac{T_{HSmax} - T_{amb}}{R_{TH}} \tag{4.3}$$

With R_{TH} the thermal resistance of the capacitor and T_{amb} the operating ambient temperature (50 °C is considered for capacitor sizing).

The maximum RMS current of the capacitor is given by:

$$i_{RMS} = \sqrt{\frac{P_{cap}}{ESR}} \tag{4.4}$$

ESR stands for the effective series resistance of the capacitor at the considered switching frequency.

The capacitor losses can be written as Equation 4.5 [70] which is used to determine the maximum capacitor ripple ΔV for the previous calculated RMS current.

$$P_{cap} = i_{RMS}^2 \cdot R_{serie} + \frac{1}{2} C \cdot \Delta V^2 \cdot f \cdot tan\delta_0 \tag{4.5}$$

With R_{serie} the series resistance of the capacitor, C the capacitor's capacitance, f the ripple frequency and $tan\delta_0$ the dielectric dissipation factor of the polypropylene material ($2 \cdot 10^{-4}$).

The RMS current and the ripple voltage of the capacitor must respect both the internal design rules and the maximum temperature criterion so the lowest of the values resulting of these rules are kept for the following calculations.

Knowing the capacitors' limits it is important to define the efforts of the capacitors of the flying capacitor and the DC bus. For the flying capacitors, in a 3-level chopper, the maximum voltage ripple and the maximum RMS current occur at 50% duty cycle. Equation 4.6 gives the voltage ripple of the flying capacitor. The output current of the chopper in the multiplexed topology is almost directly the maximum current of the three phases. Thus, the current considered for the voltage ripple calculation and the capacitor's RMS current is the amplitude of the phase current.

$$\Delta V = \frac{i}{C \cdot f} \tag{4.6}$$

Considering a 4Q converter, it has been considered that each converter side (AFE and inverter) has its own DC bus. To determine the RMS current and the voltage ripple it has been considered that the DC bus supplies the chopper and a continuous current supplies the DC bus with equal average value. Therefore, the RMS current of the DC bus capacitor and the current for the voltage ripple calculation are half the current of the flying capacitors.

Having the currents of the flying capacitors and the DC bus capacitors, one can calculate the number of capacitors in parallel to respect the capacitors' RMS current and voltage ripple. Moreover, one can calculate the number of capacitors series-connected to withstand the DC bus and the flying capacitors' voltage.

These calculations have been done for the 2 kV film capacitors of the TDK B25690 series. This series has been chosen due to its high capability in RMS current. After the calculations, the different sets of capacitors have been compared in terms of volume and stray inductance. Finally, the B25690A2117K001 (110 $\mu F/2\ kV$) has been chosen because it minimizes the volume and requires more capacitors in parallel, which reduces the equivalent stray inductance. For the flying capacitor, four capacitors must be connected in series, and for the DC bus, two capacitors are connected in parallel and four capacitors in series. This set corresponds to the DC bus of one side of the converter, i.e., in the four quadrants converter, two identical sets will be connected in parallel in the DC bus.

4.4.1.2 Semiconductors

Table 4.2 shows the 1.7 kV semiconductors used in the chopper stage and the 6.5 kV semiconductors used in the inverter stage.

TABLE 4.2: 4.16 $kV/700\ kVA$ inverter semiconductors.

Reference	Constructor	Rated voltage	Rated current
CM300DY-34T	Mitsubishi Electric	1.7 kV	300 A
FF225R65T3	Infineon	6.5 kV	225 A

4.4.1.3 AC grid filter

To connect the converter to the grid, the AFE needs a filter to respect the IEEE STD 519-2014 [71] that limits current distortion for general distributions systems. in this standard the allowed amplitude of each individual current harmonic and the allowed total harmonic distortion of the current (THDi) is given as a function of the short-circuit strength at the point of common coupling PCC. The short circuit ratio has been defined to be between 20 and 50 as [30].

In order to satisfy the current harmonic content limits defined by the IEEE519 standard, an LCL filter (Figure 4.17) has been designed. The literature presents many examples of how to size such a filter [30, 72–74]. The converter side inductor is defined by the ripple of the converter-side current (typically set below $15-20\%$ of the rated current. Equation 4.7 gives the current ripple for a 5-level inverter [30]. In this case the current ripple has been set to 15%.

$$\Delta i = \frac{V_{DC}}{24L \cdot f_{sw}} \tag{4.7}$$

According to the literature, the capacitor of the LCL filter typically manages an amount of reactive power Q of about $2-10\%$ of the rated power. Equation 4.8 gives the capacitance value as a function of the reactive power. The reactive power for this filter is 10% in order to reduce the size of the grid side inductor.

$$C = \frac{Q}{2\pi \cdot f_{AC} \cdot V_{grid}} \tag{4.8}$$

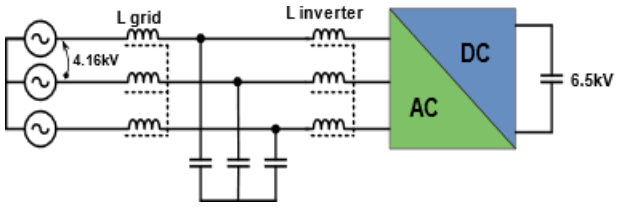


FIGURE 4.17: LCL grid filter scheme.

The grid side inductor is defined by the cutoff frequency that must be low enough to achieve the required current harmonic attenuation. Besides that, to avoid undesired harmonics amplification, the resonance frequency must be set far below the switching frequency. The cutoff frequency has been set to 900 Hz in order to respect the individual current harmonic content, resulting in a resonance frequency of 1060 Hz. Table 4.3 presents the value of the filter elements with the corresponding losses provided by the inductor manufacturer. For the simulations, a passive RLC damping circuit [74] has been used ($R = 12\ \Omega$, $L = 325\ \mu H$ and $C = 59\ \mu F$) . Afterward, the damping circuit can be replaced by an active damping strategy [75–77] to reduce the power losses. Figure 4.18 shows the filter inductors current, the harmonic contents of the grid current compared to the standard limits and the bode plot of the LCL filter. One can observe that the grid current has a sinusoidal form and respects the standard's harmonics limits. Moreover, the current THD is 2.1%, lower than the standard limits.

TABLE 4.3: Grid filter components.

Component	Value	Dimensions(WxLxH)	Constructor	Losses
Linverter	7 μH	570x350x570 mm	Tamura	1290 W
Lgrid	3 μH	570x250x570 mm	Tamura	820 W
C	11 μF	450x120x405 mm	AVX B25161	—

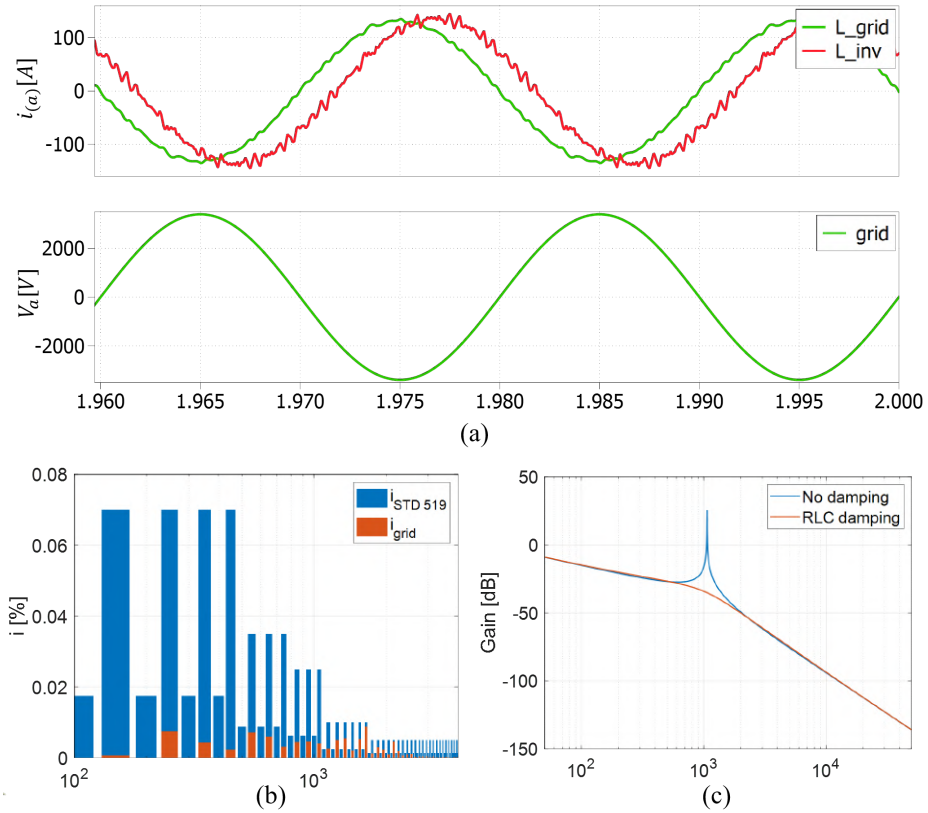


FIGURE 4.18: Grid filter results: (a) inverter and grid inductor current waveforms; (b) harmonic contents of the grid current compared to the standard limits; (c) bode plot of the LCL filter with and without damping.

4.4.2 Laminated busbar

For the conception of the laminated busbar and the choice of the inverter components, the international standard for adjustable speed electrical power drive system IEC 61800-5-1 [69] has been respected. The respect to the standard is essential to have a testbench that better represents mechanically and electrically the final solution.

One of the most important criteria for the conception of the busbar was the reduction of the stray inductances of the chopper and the inverter stages. The reduction of the chopper stage inductances is crucial because it is composed of fast components and the chopper composes the switching cells of the inverter stage. Therefore, a four-layer design has been chosen wich allows interleaving layers with positive and negative polarity to reduce the stray inductances and maximize coupling between the two polarities.

The surfaces corresponding to the positive and negative polarities of the DC bus are face to face in the laminated busbar to increase their coupling. In the same way, the surface that corresponds to the intermediate point of the DC bus covers the whole busbar to maximize coupling with the DC bus potentials, the flying capacitor potentials and the output of the chopper stages. Figure 4.19 shows the laminated busbar with the components of the inverter. In (b), it is possible to observe the four layers that compose the chopper and, over them, the layer corresponding to the DC bus intermediate point covering the whole busbar.

The clearance and creepage distance between the different layers and conductors respect the rules of the IEC 61800-5-1 standard with a pollution degree level 2 and an overvoltage category 3. Moreover, according to the previously cited standard, all the conductors that are face to face have passed the insulation and partial discharge test.

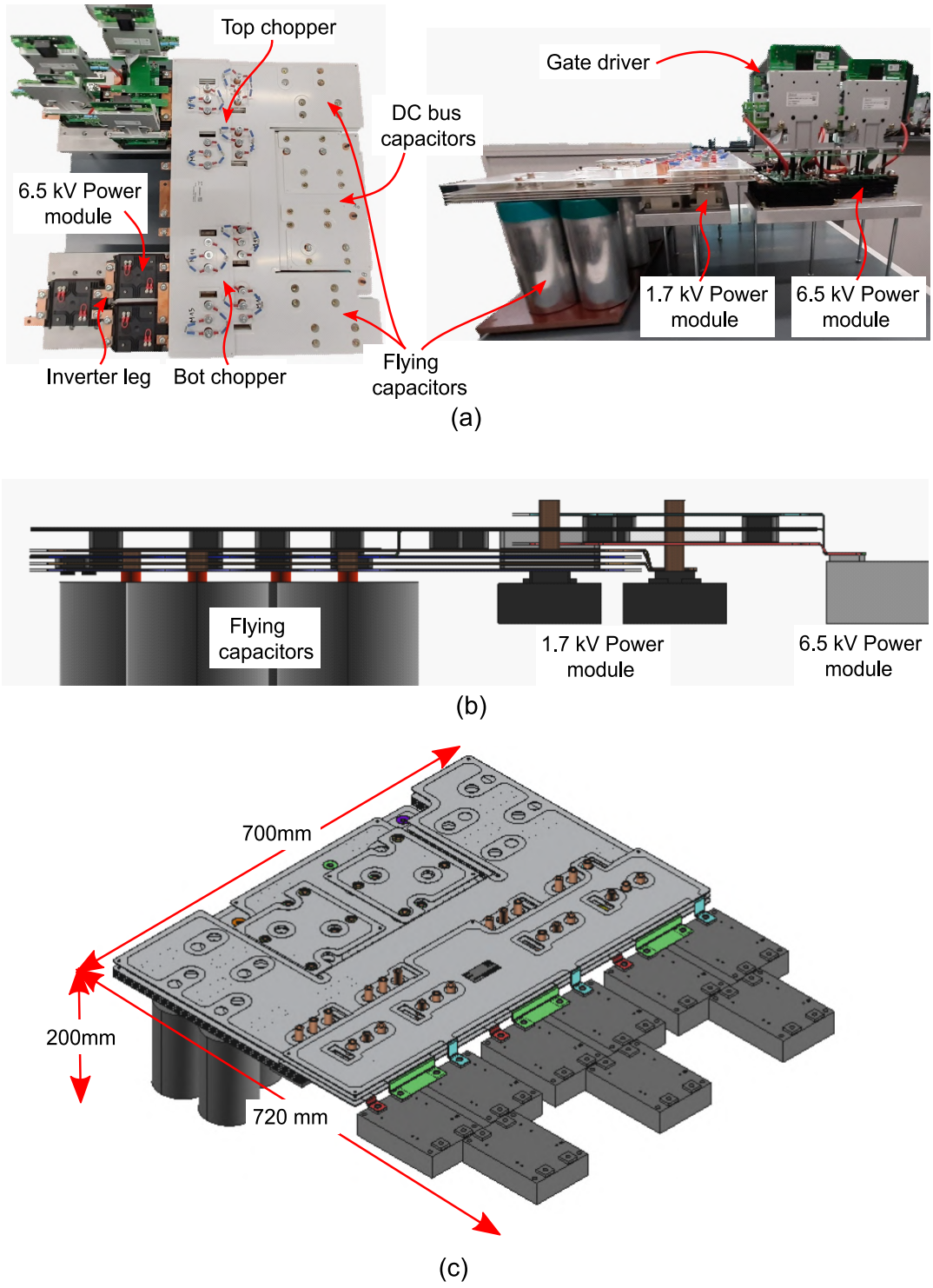


FIGURE 4.19: 4.16 kV/700 kVA inverter: (a) busbar with the mounted inverter components; (b) 3D side view of the laminated busbar; (c) 3D view of the inverter with its dimensions.

4.4.3 6.5 kV IGBTs characterization

Figure 4.20 shows a simplified scheme of the testbench for the characterization of the 6.5 kV semiconductors in the 4.16 kV inverter, presenting only the choppers and the phase leg used for the characterization. One can observe that each blue block corresponds to one power module with two 6.5 kV IGBTs. Each represented IGBT from the chopper stage corresponds to one power module with two 1.7 kV IGBTs

series-connected. The resistors connected to the flying capacitors are used to load and keep the flying capacitors' voltages at their reference voltage without any extra active control for the realization of these tests.

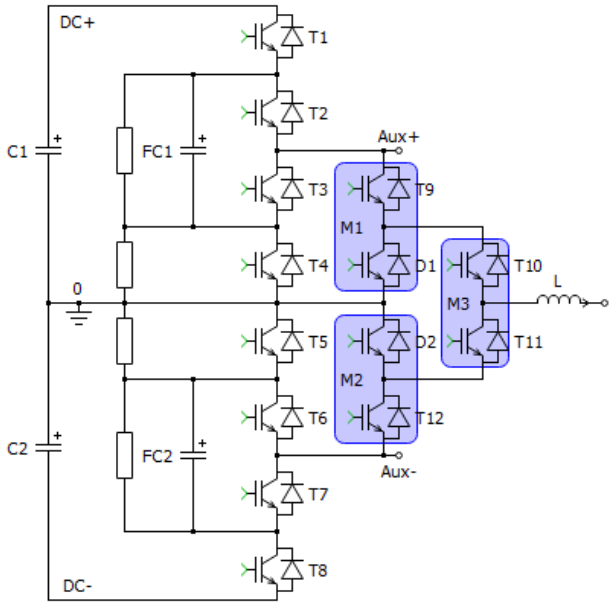


FIGURE 4.20: Simplified scheme of the inverter testbench for the characterization of the 6.5 kV semiconductors.

Table 4.4 presents the state of each switch of the simplified scheme to characterize each of the four quadrants (and consequently, each of the four semiconductors switching cells) at 1.7 kV and 3.4 kV. These two voltages are used to characterize the inverter semiconductors because they correspond to the voltage levels delivered by the chopper stage. DP in this table means double pulse, i.e., the necessary gate signal to measure the switching energies. The bus capacitors are charged at 3.4 kV, and the flying capacitor switches allow controlling the test voltage. The last line of table L corresponds to the point where the second terminal of the load inductor L needs to be connected to correctly close the switching cell.

TABLE 4.4: Simplified scheme switches' state to characterize each of the four quadrants at 1.7 kV and 3.4 kV and inductor connection point.

Switch	**Q1**		**Q2**		**Q3**		**Q4**	
	1.7 kV	3.4 kV	1.7 kV	3.4 kV	1.7 kV	3.4 kV	1.7 kV	3.4 kV
T_9	DP	DP	0	0	0	0	0	0
T_{10}	1	1	DP	DP	0	0	0	0
T_{11}	0	0	0	0	1	1	DP	DP
T_{12}	0	0	0	0	DP	DP	0	0
D_1	0	0	0	0	0	0	0	0
D_2	0	0	0	0	0	0	0	0
T_1	1	1	0	0	0	0	1	1
T_2	0	1	0	0	0	0	0	1
T_3	1	0	0	0	0	0	1	0
T_4	0	0	0	0	0	0	0	0
T_5	0	0	0	0	0	0	0	0
T_6	0	0	1	0	1	0	0	0
T_7	0	0	0	1	0	1	0	0
T_8	0	0	1	1	1	1	0	0
L	0	0	Aux-	Aux-	0	0	Aux+	Aux+

Figure 4.21 shows the voltage and current waveforms from the switching cell semiconductors for each quadrant and two test voltages. Each quadrant characterizes one switching cell of the NPC leg and corresponds to a combination of output current and voltage signal. These waveforms represent tests realized at different currents and temperatures, as specified in the figure caption.

Figure 4.22 shows more details on the commutation for the quadrant Q4, in which it is possible to see the voltage drop when the current in the transistor rises during the commutation. By measuring this voltage drop and using the slope in which the current rises, it is possible to calculate the stray inductance of this switching cell (Equation 4.9).

$$L_{stray} = \frac{\Delta V}{\frac{di}{dt}} \tag{4.9}$$

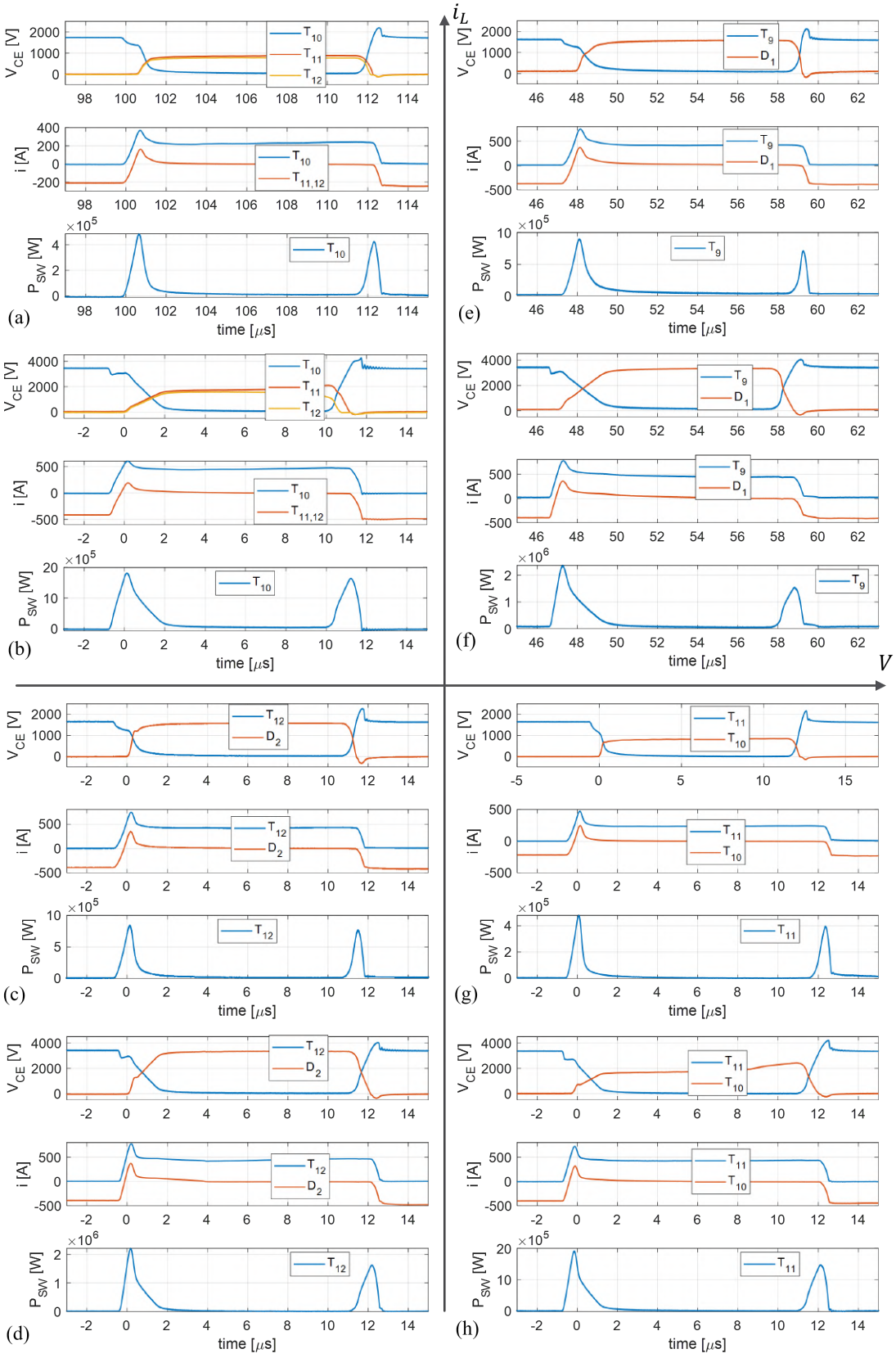


FIGURE 4.21: Voltage, current and power waveforms from the switching cell 6.5 kV semiconductors for each quadrant. Q2: (a) 1.7 kV, 225 A and 25 °C; (b) 3.4 kV, 400 A and 25 °C. Q3: (c) 1.7 kV, 400 A and 25 °C; (d) 3.4 kV, 400 A and 25 °C. Q1: (e) 1.7 kV, 400 A and 125 °C; (f) 3.4 kV, 400 A and 125 °C. Q4: (g) 1.7 kV, 225 A and 25 °C; (h) 3.4 kV, 400 A and 25 °C.

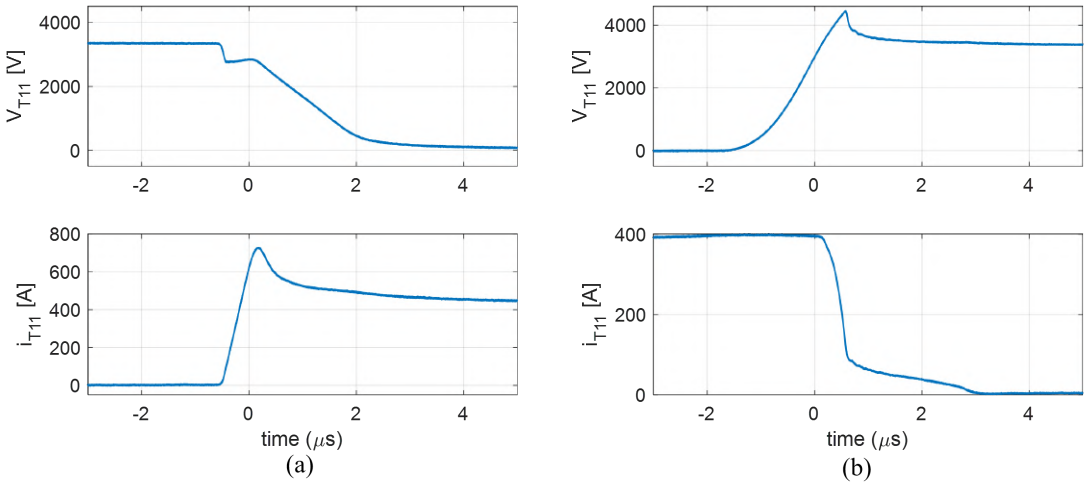


FIGURE 4.22: Voltage and current commutation waveforms for the quadrant Q4 at 3.4 kV, 400 A and 125 °C: (a) turn-on; (b) turn-off.

It is important to calculate the inductance for the different switching cells because the current path changes and so does the stray inductance. This same inductance calculation has been realized for each quadrant of operation of the NPC leg and a chopper output voltage of 1700V and 3400V. However, only one variation of the current path has been used for the tests at 1700 V to have one idea of the magnitude of the stray inductance. The chosen path is the one estimated to have the highest stray inductance due to a longer path and the presence of more capacitors.

More data has been acquired from these tests that are important to ensure the correct working of this structure when switching. One of these tests is the maximum voltage overshoot of the 6.5 kV IGBTs at turn-off (a consequence of the switching cell and the current switching speed). These measures have been realized at 400A, the maximum current of the safe operation area of the component and when the component reaches its maximum switching speed, producing the maximum overvoltage.

Finally, the switching energies have been measured for different values of current and two different values of voltage at 125 °C. Figure 4.23 shows the evolution of the switching energies as a function of the switched current and voltage for the quadrant Q1, the one that presents the highest switching energies. In this figure is possible to observe the ratio between the switching energies and the switched voltages.

Table 4.5 presents the previous data, such as stray inductances, switching speed, maximum voltage and switching energies at nominal current for all the operation quadrants and for both the switched voltages.

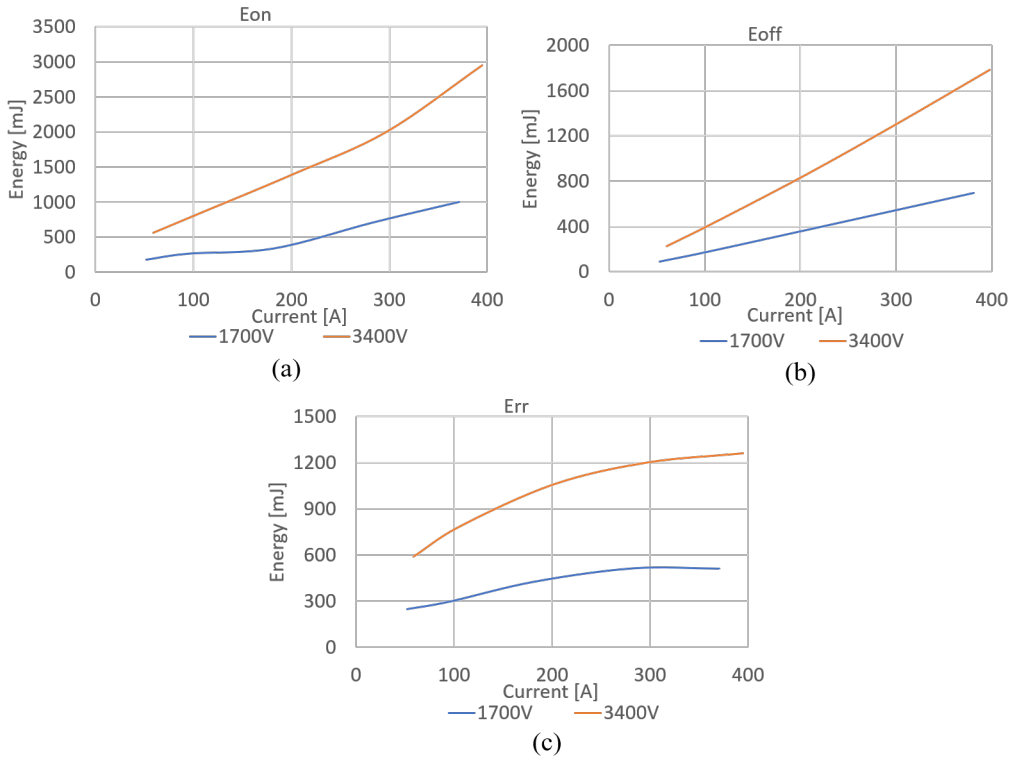


FIGURE 4.23: Switching energies of the 6.5 kV IGBTs for the quadrant Q1 for two switched voltages at 125 $°C$: (a) turn-on energies; (b) turn-off energies; (c) reverse recovery energies.

TABLE 4.5: Stray inductances, maximum current switching speed, overvoltage, total switching energy and energy ratio for each NPC leg quadrant and switched voltage.

Quadrant	V_{SW}	L_{stray}	di/dt_{off}	$V_{CEmax}400A$	$E_{SWtotal}225A$	$\%E_{SWtotal}$
Q1 125°C	1.7 kV	295 nH	1.2 $kA/\mu s$	2.32 kV	1.10 J	33%
	3.4 kV	325 nH	1.4 $kA/\mu s$	4.38 kV	3.32 J	100%
Q2 25°C	1.7 kV	565 nH	545 $A/\mu s$	2.36 kV	0.795 J	33%
	3.4 kV	515 nH	805 $A/\mu s$	4.25 kV	2.41 J	100%
Q3 25°C	1.7 kV	350 nH	1.1 $kA/\mu s$	2.34 kV	0.847 J	40%
	3.4 kV	335 nH	1.6 $kA/\mu s$	4.10 kV	2.11 J	100%
Q4 125°C	1.7 kV	440 nH	1.0 $kA/\mu s$	2.20 kV	0.840 J	30%
	3.4 kV	480 nH	1.5 $kA/\mu s$	4.22 kV	2.93 J	100%

The results presented here verify the assumption made at the beginning of this work in which the switching energy is proportional to the switched voltage. Better than that, the results show that the energies ratio is lower than the switched voltage ratio, showing even more the interest in this topology that reduces the switched voltage of the semiconductors in the inverter stage.

Secondly, the energies measured at nominal voltage correspond to the values given in the datasheets, which shows that in this case the long switching cells do not significantly increase the switching losses.

Finally, one can observe that the long switching cells with high stray inductances are still compatible with the characterized HV semiconductors. The switching speed of

those components is compatible with the stray inductances, and the components do not present a high overvoltage at the turn-off commutation. The IGBT's maximum voltage remains lower than the active clamping overvoltage protection of 4.8 kV. It may even be possible to avoid overvoltage protection in the final application to reduce the gate driver cost.

4.4.4 Efficiency and loss distribution

This section will present the semiconductors losses in the inverter and rectifier operation mode for the two developed modulations, the carrier-based modulation and the space vector modulation. This section aims to study the loss distribution along with the converter and compare both modulations in terms of semiconductors losses. This loss comparison will be developed by simulation using Plecs software using the loss model of the semiconductors. The loss models of the semiconductors use the datasheet information for the conduction losses and the characterization data from the previous sections for the switching losses. The switching energies supplied to the semiconductors model of Plecs are the switching energies measured at 125 $^{\circ}C$. For the 1.7 kV semiconductors the average value of the two series-connected devices has been used. Moreover, for the inverter semiconductors (6.5 kV) the energies correspond to those measured for the first quadrant (Q1). These choices have been made because these energies correspond better to the operating temperature of the semiconductors. Besides that, they correspond to the maximum values of the switching losses, simulating the worst-case scenario in terms of semiconductors switching losses.

The simulations have been done in inverter and rectifier mode at nominal voltage and a switching frequency of $f_{sw} = 1950\ Hz$. The inverter simulation supplies a 700 kVA load with a power factor of $PF = 0.85$. Therefore, the active power supplied to the load is $P_{inv} = 600\ kW$. The grid needs to supply the load's active power plus the chopper and inverter stage losses found in the rectifier simulation. Therefore, for the rectifier simulation, a power of $P_{grid} = 608\ kW$ has been considered. Moreover, the rectifier operates with a unity power factor.

Figure 4.24 (a), (b) shows the loss distribution for the inverter and rectifier (AFE) modes between conduction and switching losses for each converter stage and the whole converter, comparing the SVM and carrier-based modulation. One can observe that the SVM represents a substantial reduction of the semiconductor losses for the chopper and the inverter stage. This loss reduction comes from the reduction of the switching losses. The conduction losses for both modulations schemes are the same.

In the chopper stage, the reduction of switching losses comes principally from the fact that, as presented in Chapter 3, the top and bottom choppers switch simultaneously during a small part of the output period when using the SVM scheme. The exception occurs in some operating points where the flying capacitor stays saturated at the intermediate level. However, in the carrier-based modulation, the top and bottom choppers always switch simultaneously. Therefore, the chopper switching losses of the SVM gain can be lower in other operation points due to the flying capacitors balancing strategy.

In the SVM the inverter stage constantly switches at reduced voltage. At the same time, in the carrier-based modulation, only one commutation (turn-on or turn-off)

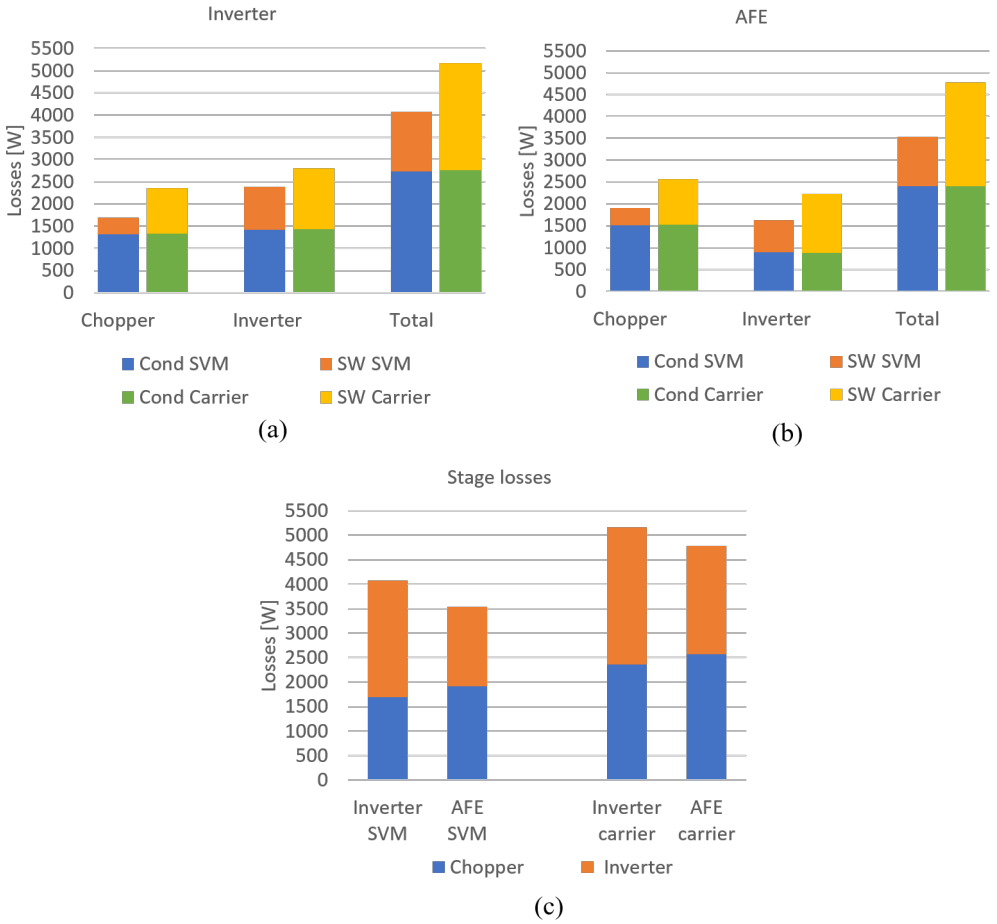


FIGURE 4.24: Losses distribution for two modulation schemes: SVM and carried-based. Conduction and switching losses for the inverter (a) and the rectifier (AFE) (b) modes for each converter stage and the whole converter. Total losses distribution between the chopper and the inverter stages for the two modulation schemes are shown in (c).

per period could be assured to be at reduced voltage. This explains the reduction in the inverter stage switching losses.

The SVM represents a total losses reduction of 21% (1090 *W*) compared to the carrier-based modulation in the inverter mode. In the AFE mode, the total losses reduction is even higher, 26% (1250 *W*).

Figure 4.24 (c) shows the total loss distribution between the chopper and the inverter stages for the two modulation schemes. In the inverter operation mode, the inverter stage presents a higher amount of losses than the chopper one. However, for the AFE mode, the chopper presents higher losses than the inverter stage. This difference of loss ratio between the stages comes principally from the difference in the conduction losses in the inverter and AFE modes. The transistors from the semiconductors used in the chopper stage present better conduction performances than the diodes. However, the diodes from the semiconductors used in the inverter stage present a lower voltage drop than the transistors. On the other hand, the diodes are more requested in AFE than inverter mode when operating at nominal voltage. Therefore, the inverter stage conduction losses decrease and the chopper stage conduction losses increase, comparing the AFE mode with the inverter mode.

With all semiconductors losses determined, a first estimate of converter efficiency can be calculated. The efficiency of a four-quadrant converter (inverter+AFE) using space vector modulation is 98.75% and using carrier-based modulation is 98.37%. To have a better efficiency estimation, the losses of the grid filter inductors can be added to the semiconductors' losses for the SVM. Thus, the efficiency for the SVM becomes 98.40%, meaning that this modulation scheme with the grid filter inductor losses is equivalent to the carrier-based modulation and no filter.

Figure 4.25 shows the power losses of each converter semiconductor using SVM in inverter mode. In the chopper semiconductors, it is interesting to observe that the conduction losses are predominant, showing that the SVM objective of reducing the switching losses has been achieved. On the other hand, the inverter stage semiconductors present conduction and switching equivalent losses. This shows the potential of the topology and the modulation to present such switching losses at such a high switching frequency for HV semiconductors. Moreover, one can observe that at nominal voltage and inverter mode, the power modules losses are well balanced.

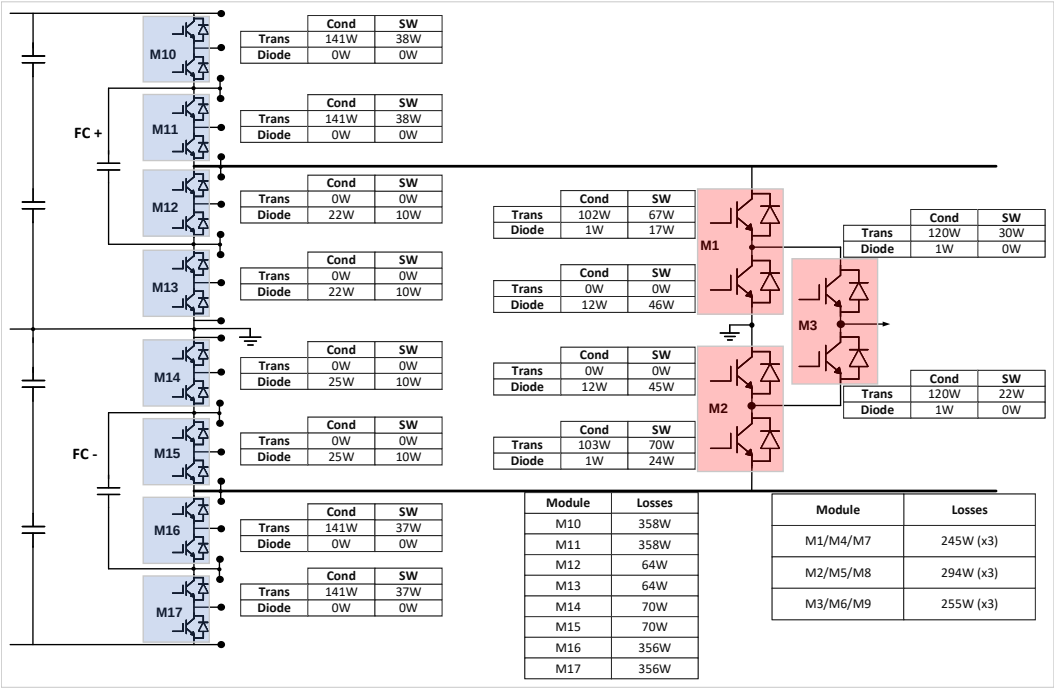


FIGURE 4.25: Power losses of each converter semiconductor, using SVM, in inverter mode at nominal voltage.

4.5 Conclusion

This chapter presented some experimental results in order to validate some crucial technical aspects of the topology and to study the converter distribution losses.The first point that has been validated is the series connection of the 1.7 kV IGTBs, which is crucial for the competitiveness of the multiplexed topology and for reducing the size of the Flying capacitors. The static and dynamic voltage balance and switching energies equalization of the series-connected semiconductors show the efficiency of the unbalance mitigation methods that have been associated. Moreover, the active champing has contributed to limiting the semiconductors' overvoltage.

Additionally, two different silicon carbide MOSFETs have been studied. The switching energies of these devices have been measured and compared with the series-connected IGBTs to study the interest in replacing the IGBTs with SiC MOSFETs in the future.

The 3.3 kV SiC MOSFETs have equivalent switching energy compared to the series-connected IGBTs. I.e., they do not represent a switching loss reduction replacing the IGBTs. One of the advantages of replacing the two series-series connected IGBTs with one MOSFET is the reduction of the conduction losses of the chopper stage. One 3.3 kV MOSFETs presents a lower voltage drop than two series-connected IGBTs. Moreover, as seen previously, with the SVM, conduction losses represent most of the semiconductors losses in the chopper stage. So it can be seen that using 3.3 kV SiC MOSFETs is probably the best way to improve efficiency. The other main benefit of replacing the series-connected IGBTs with one MOSFET is reducing the complexity of the chopper stage. There will be no need for voltage balance mitigation methods and reducing by half the number of gate drivers. Additionally, this replacement will simplify the layout and construction of the chopper stage of the busbar and reduce the stray inductances seen by the inverter stage due to a shorter commutation loop.

The series-connected IGBTs can also be replaced by the series-connected 2 kV SiC MOSFETs. In terms of busbar design, this is a much more straightforward solution because the IGBTs and the MOSFETs use the same housing. Moreover, the gate driver and the balancing circuits are equal or similar. Besides that, the series-connected MOSFETs present lower switching energy and conduction voltage than the series-connected IGBTs representing an important reduction of the chopper stage semiconductors losses. However, the 2 kV MOSFETs keep the complexity added by the series connection. Moreover, they can add extra complexity due to the difficulty of managing such a high-speed component's voltage and losses balance.

Globally, the replacement of the chopper IGBTs with SiC MOSFETs represents a reduction of the chopper losses. Thus, showing that the topology is compatible with this promising technology and being able to benefit from the main advantages of the silicon carbide MOSFETs. However, the main drawback of these semiconductors is still the cost which can reach a ratio of 20 to 30 considering the 3.3 kV MOSFETs. Therefore, this technology is still a solution for the future.

The second validated point was the series connection of the 4.5 kV IGBTs, which are crucial to withstand the bus voltage in the 6.6 kV inverter. These series connections also presented well-balanced voltages and switching energies using a small RC snubber. Moreover, the hypothesis of the linearity of the switching energies with the switched voltage has been validated. The energies ratio is lower than the voltage ratio for low switching voltages, showing even more interest in switching at reduced voltage. The only aspect of these semiconductors that has not been validated is the compatibility with a long commutation cell, including the 4-level flying capacitor chopper.

The third testbench, a 4.16 kV inverter, allowed to validate the compatibility of the 6.5 kV IGTBs with the long commutation cells that include the chopper stage. Even though the commutation cells present high stray inductances, they are compatible with the semiconductors switching speed, presenting low overvoltages. Moreover, the inverter semiconductors usually will not switch half the bus voltage due to the SVM, given even more overvoltage margin for these devices. This testbench also

validated the hypothesis of the linearity of the switching energies with the switched voltage. Likely for the 4.5 kV IGTBs, the energy ratio is inferior to the ratio of the voltages helping to reduce the inverter semiconductors switching losses.

Besides that, the 4.16 kV inverter laminated busbar and grid filter design have been validated. As seen in the previous section, the inverter is very compact for its output power. Additionally, it is possible to increase this inverter output power without a big change in its volume by changing the rated current of the semiconductors and adding some extra capacitors. With the available rated current semiconductors with the same housing, it may be possible to increase the output power to 1 MVA without significantly increasing the converter volume.

Finally, the semiconductors loss distribution has been studied for the two developed modulation schemes. The results show that the space vector modulation significantly reduces the switching losses of the chopper and inverter stage compared to the carrier-based modulation. This loss reduction comes from reducing the chopper stage commutations and the reduction of the switched voltage of the inverter stage. These results reinforce the conclusions of Chapter 3, showing that the SVM modulation has a better waveforms quality and presents a better semiconductor efficiency than the carrier-based modulation.

Chapter 5

Conclusion and perspectives

In this thesis, a new family of multilevel power converter, i.e. multiplexed has been studied. This family of converters is a promising solution for medium-voltage power drive applications. The potential of this structure comes from its capability of reducing the efforts of the HV semiconductors, minimizing the influence of their major disadvantages in the structure cost and efficiency. Two different structures have been proposed for 4.16 kV and 6.6 kV power drives. Moreover, two different modulation schemes have been developed and compared: a carrier-based modulation and a space vector modulation. The space vector modulation has shown numerous advantages compared to the other modulation scheme.

Finally, different test benches have been built in order to verify and validate the assumptions that have been made during this study. These test benches verified many technical aspects of the topology, such as the series-connection of IGBTs, switching energies under reduced voltage and the structure's stray inductances. Moreover, the experimental results allowed to estimate the converter efficiency and the structure size.

5.1 Conclusion

In Chapter 2 the multiplexed family of converters has been presented. Different structures that could meet the cost and performance requirements of this study by minimizing the number of MV semiconductors have been proposed. Furthermore, the proposed structures have been compared in terms of semiconductors cost with two well-established solutions in the market, the 3L-NPC and the 5L-ANPC. The main findings are:

- The multilevel multiplexed family of converters is presented. This family of converters is so-called due to its operating principle. The independent stage (inverter) acts as a multiplexer connecting the voltage generated by the top or bottom chopper to each of the three phases to one of the three phases' output. The inverter stage shares the two choppers i.e., the common stage. The main benefit of this topology is the reduction of the inverter stage switching efforts due to the concentration of the switching efforts in the common stage. Moreover, it is possible to reduce the number of HV semiconductors compared to a state-of-the-art topology for a given number of output levels.
- The concept of dead voltage has been introduced to this family of converters. The main advantage of using a dead voltage is the reduction of the choppers stage bus voltage, reducing the rated voltage of the semiconductors of this

stage. However, using a dead voltage limits the output voltage range in which the converter can take benefit of the topology working principle. Even though the converter can synthesize the output voltage correctly, when the intersection of the output voltages is inferior to the dead voltage, more than one inverter leg switches at a time, highly increasing the inverter stage switching efforts. Moreover, the use of a dead voltage in a four-quadrant power drive requires the use of a bus balancer circuit to compensate for the different operation points of the rectifier and the inverter sides. The introduction of a bus balancer circuit adds a high number of semiconductors and passive components and increases the complexity of the structure. Besides all these drawbacks, the use of a bus balancer also reduces the system's reliability due to a higher component count. Therefore, the use of a dead voltage is not suitable for variable speed drives, where the output voltage can vary in a wide range.

- The use of low voltage semiconductors (1.7 kV) in the chopper stage of the multiplexed topology is crucial for the competitiveness of this topology. It highly reduces the semiconductors' cost and reduces the switching losses of the chopper stage, increasing the overall efficiency. Additionally, low voltage semiconductors allow for an increase in the switching frequency, reducing the size of the flying capacitors, making the 4-level flying capacitor suitable for the studied applications, and increasing the structure power density.
- The cost of the compared solutions is driven by the use of a high number of HV semiconductors that generate a lot of switching losses and need a high current rating. The reduction of the cost provided by the concentration of the efforts in the low voltage semiconductors and the reduced number of the HV semiconductors makes the multiplexed topology very interesting in terms of semiconductors cost.

The working principle of the multiplexed topology and two different modulations schemes for the previously proposed structures has been presented in Chapter 3. A carried-based modulation and a space vector modulation have been developed to reduce the switching efforts of the HV semiconductors. Moreover, the two modulation schemes have been compared in terms of waveform quality. The main findings are:

- The multiplexed topology has a particular working principle compared to the conventional topologies. In the multiplexed topology, the choppers produce the maximum and minimum voltage of the three phases, and the intermediate voltage is produced by the inverter leg of the corresponding phase. Consequently, the choppers switch continuously, while the inverter legs switch only one-third of the time, drastically reducing the inverter legs' switching efforts.
- The inverter stage is supplied with an already chopped voltage by the chopper and, assuming a proper synchronization, the inverter can switch the lowest voltage of this square wave. Therefore, some different schemes of carrier-based modulation have been developed for this topology using different combinations of carriers for the chopper and inverter stage. The carrier-based modulation was able to realize one commutation (turn-on or turn-off) at reduced voltage and the other one depends on the inverter duty cycle. Different schemes of carrier-based modulation could have been developed to maximize the operating points in which it is possible to do both the commutations at reduced voltage; however, the modulation would quickly become very complex.

- The space vector modulation developed for this topology is close those used for conventional topologies. However, the multiplexed topology cannot produce all the vectors of a conventional topology with the same number of levels. Therefore some particularities have been introduced in the SVM scheme to identify the modulation triangles that are not always equilaterals or even the modulation trapeziums. The space vector modulation developed for this topology is able to realize both the commutation at reduced voltage thanks to the dedicated switching sequences that have been defined for each modulation triangle or trapezium. Moreover, an adapted flying capacitor voltage balancing strategy has been coupled to the SVM.
- Comparing both the modulation schemes, it has been seen that besides the possibility to do both the inverter commutation at reduced voltage, the SVM reduces the number of commutations of the chopper stage. The SVM produces an output voltage with a much better waveform quality compared to the carrier-based modulation, supplying the machine with a current with much lower low harmonics amplitude.

Chapter IV presented three different test benches used to validate some particular technical aspects of the multiplexed structure and some assumptions made during this work: the series connection of 1.7 kV and 4.5 kV IGBTs, to measure the switching energies of MV semiconductors under reduced voltage and measure the stray inductances of the inverter. These results have allowed us to estimate the efficiency of the proposed structure, study the distribution of semiconductors losses, and compare the performances of the two developed modulation schemes. The main findings are:

- The first test bench has been used to evaluate the series connection of 1.7 kV IGBTs. The association of the gate driver mitigation methods and external snubber circuits have assured a good voltage and energy balance between the series-connected devices. Additionally, this test bench has been used to characterize the switching energies of 2 kV series-connected and 3.3 kV SiC MOSFETs to study the gains they can provide a future replacement of the series-connected IGBTs. It has been seen that the 3.3 kV MOSFETs do not offer a switching energy gain, but they reduce the conduction losses and they eliminate the complexity added by the series connection of the IGBTs.The 2 kV MOSFETs offer switching and conduction losses gain; however, they keep the complexity of the series connection adding even some extra due to the difficulty of ensuring a good voltage balance of such high-speed devices
- The second test bench has validated the series connection of the 4.5 kV IGBTs needed for the NPC stage of the 6.6 kV structure. Furthermore, the switching energies under reduced voltage have also been analyzed. It has been seen that the switching energy is reduced when the switched voltage is reduced. Moreover, the ratio between the switching energies is lower than the ratio between the switched voltages
- Finally, the third test bench was used to characterize the 6.5 kV IGBTs and also validate the linearity of the losses with the switched voltage. As for the 4.5 kV ones, the lower the switched voltage, the lower the switching energies. Moreover, this testbench, which is a complete inverter, has validated the compatibility of the high stray inductances intrinsic to this topology with the switching speed of the 6.5 kV IGBTs. Finally, this testbench, that has been designed as

an 4.16 $kV/700\ kVA$ inverter, has also given a good idea of the volume of the power cell of such an inverter structure.

- The characterization results from the previous test benches have been used to study the inverter efficiency and losses distribution. It has been seen that this topology, with its associated modulation scheme, is able to reduce the losses of the HV semiconductors having low switching losses at a switching frequency that is not compatible with conventional topologies. Besides, it has been seen that the space vector modulation presents lower switching losses than the carrier-based modulation which, associated to a better waveform quality, demonstrates its superiority for this topology. Finally, the good semiconductors efficiency has shown the potential of this structure using only IGBTs.

To conclude, the concentration of the switching effort in a single-stage combined to an inverter performing only a few switchings could lead to a WideBandGap/Si combination, but today, even with a reduced number of WBG devices, the cost is not compatible with market expectations. However, in this thesis it has been shown that a realistic option is to build such a MV converter using only low-cost silicon devices.

5.2 Perspectives and future work

This thesis work was mainly concentrated on proposing multiplexed-based structures converter for medium voltage power drives of 4.16 kV and 6.6 kV and a dedicated modulation scheme. Therefore some suggestions for future work and research lines are presented.

A modulation scheme dedicated for the multiplexed topology has been developed and validated by simulation. As the inverter switches and an already switched voltage without a filter, the synchronization of the chopper and inverter pulses is crucial. Therefore, due to its complexity and the use of different rated voltage components with different switching times, it is essential to implement and validate this modulation in the developed inverter. Moreover, some investigation needs to be done on the minimum and maximum pulse duration, dead-time, and their influence on the output waveforms. This is necessary because the degrees of freedom used in conventional SVM modulation that allows minimizing the influence of these factors do not exist in this case due to the fixed implemented switching sequences of each modulation triangle. Therefore, the developed modulation needs to be implemented in a controller system, validated in a Hardware in the Loop (HIL) system and then tested in the inverter test bench.

The semiconductors models from the characterization can be used to study, in simulation, the efficiency and the losses distribution for different operation points that are not the nominal ones. Moreover, simulations can be carried out to determine the maximum output power and the efficiency of the converter for given rated current semiconductors. Similar simulations can be done with conventional topologies, and these results can be used for a more complete comparison between them and the multiplexed topology.

The test of the developed modulation in the inverter testbench will allow the verification of the waveform quality, the losses distribution and the efficiency of the structure. The loss distribution can be measured using a colorimetric method based on measuring the power losses on the water flow exchanger. Since each converter

stage is fitted with its own water flow exchanger, it is pretty straightforward to implement this method. The efficiency can be measured using the previously cited colorimetric method or the electrical method, which measures the input and output power.

The space vector modulation scheme has only been studied and developped for the 5-level 4.16 kV structure. Due to the waveform quality and the switching losses that this modulation scheme has provided, this modulation scheme needs to be extended to the 7-level 6.6 kV inverter. Most of the modulation scheme will be identical to the 5-level one, but special attention will be needed in some modulation triangles/trapezium definition and the switching sequences that will be particular to the 7-level inverter.

Furthermore, the proposed structure has only been studied in normal operating conditions. Thus, special operating conditions need to be studied. For example, the start-up of the converter with dc bus and flying capacitors pre-charge and different short-circuits conditions. Many strategies have already been studied in the literature for the flying capacitors pre-charge and can be adapted to this topology and application. For the short-circuits conditions, different strategies can be considered using the chopper and inverter stage association to accelerate the converter reaction and balance the semiconductors' efforts.

Another technical aspect that needs to be studied and verified in the inverter test bench is the current measurement. The synchronization of the measure with the average value of the current in the switching period still a challenge for this structure.

Finally, no reliability study has been carried out in this work. This topology has the major particularity that it does not have three independent legs, and the choppers are common to the three output phases of the inverter stage. Thus, this topology can be more prone to failure. However, the presented topology has a lower semiconductors count for the 4.16 kV inverter compared to some classical topologies, which helps to improve the topology robustness.

Appendix A

Inverter duty cycle calculation for carrier-based modulation

To develop the equations that link the inverter average output voltage V_{Inv} to the inverter duty cycle D_{Inv}, the chopper average output voltage V_{Chp}, its output voltage levels V_1 and V_2, the chopper equivalent duty cycle D_{Eq} and the number of flying capacitor cells n_{cell} an example with 2 cells, i.e., a three-level flying capacitor, will be used. Developing those equations, the inverter duty cycle can be calculated for a generic case, no matter how many cells compose the flying capacitor converter. Inverter duty cycle is the same for either a rising (Figure A.1(a)) or a falling sawtooth carrier (Figure A.1(b)).

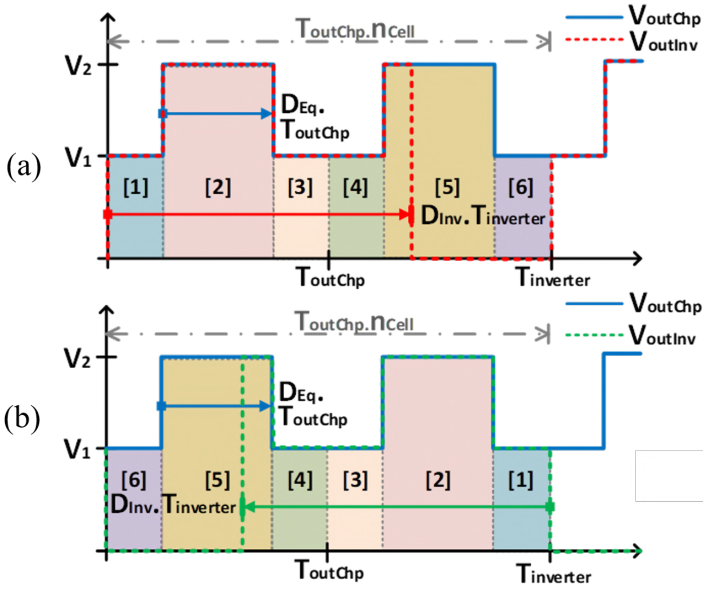


FIGURE A.1: Duty cycle evolution for rising (a)(red) and falling (b)(green) sawtooth carrier in function of chopper output voltage (blue) and number of chopper cells n_{cell}.

$$V_{Inv} = \begin{cases} [1]\ D_{Inv} \cdot V_1 & \text{for} \quad 0 \leq D_{Inv} < \dfrac{1 - D_{Eq}}{2n_{cell}} \\ [2]\ D_{Inv} \cdot V_2 + \dfrac{1 - D_{Eq}}{2n_{cell}} \cdot (V_1 - V_2) & \text{for} \quad \dfrac{1 - D_{Eq}}{2n_{cell}} \leq D_{Inv} < \dfrac{1 + D_{Eq}}{2n_{cell}} \\ [3]\ D_{Inv} \cdot V_1 + \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) & \text{for} \quad \dfrac{1 + D_{Eq}}{2n_{cell}} \leq D_{Inv} < \dfrac{1}{n_{cell}} \\ [4]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_1 & \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} \leq D_{Inv} < \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \\ [5]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_2 + \dfrac{1 - D_{Eq}}{2n_{cell}} \cdot (V_1 - V_2) & \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} \leq D_{Inv} < \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \\ [6]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_1 + \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) & \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \leq D_{Inv} \leq \dfrac{2}{n_{cell}} \end{cases} \tag{A.1}$$

Equation (A.1)[1] corresponds to its respective zone on Figure A.1, i.e., to the zone where the inverter on-time is lower than half the equivalent off-time of the chopper on its first period. When the inverter on time exceeds it but is lower than one chopper period minus half the equivalent off-time of the chopper, i.e., it enters the zone 2, (A.1)[2] gives the corresponding output voltage. Furthermore, when the inverter on time exceeds the previous condition but is lower than one chopper equivalent period (A.1)[3] gives the output voltage. Additionally, if the inverter on-time exceeds one chopper period but is lower than one chopper period plus half the equivalent chopper off-time it enters the zone 4 where the equation (A.1)[4] gives the output voltage. The logic continues for an inverter on-time that evolves over the upcoming zones.

One should note that a term like the one given by (A.2) appears in the average output voltage equation when the inverter on-time exceeds one chopper period. It represents the contribution of the entire period of the chopper voltage on the inverter average voltage. The lvl variable gives the information of how much chopper entire periods are included in the inverter on time. lvl goes from zero to the number of choppers switching cells minus one and its mathematical definition is given by (A.3).

$$lvl \cdot \frac{V_{Chp}}{n_{cell}} \tag{A.2}$$

$$lvl = floor\left(\frac{V_{Inv}}{V_{Chp}} \cdot n \right) \cdot \frac{1}{n} \tag{A.3}$$

Applying (A.3) on (A.1) it becomes generic for any number of chopper cells.

$$V_{Inv} = \begin{cases} lvl \cdot \dfrac{V_{chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_1 & \text{for } \dfrac{lvl}{n_{cell}} \leq D_{Inv} < \dfrac{lvl}{n_{cell}} + \dfrac{1 - D_{Eq}}{2\, n_{cell}}, \\ lvl \cdot \dfrac{V_{chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_2 + \dfrac{1 - D_{Eq}}{2\, n_{cell}} \cdot (V_1 - V_2) & \text{for } \dfrac{lvl}{n_{cell}} + \dfrac{1 - D_{Eq}}{2\, n_{cell}} \leq D_{Inv} < \dfrac{lvl}{n_{cell}} + \dfrac{1 + D_{Eq}}{2\, n_{cell}}, \\ lvl \cdot \dfrac{V_{chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_1 + \dfrac{1 - D_{Eq}}{2\, n_{cell}} \cdot (V_2 - V_1) & \text{for } \dfrac{lvl}{n_{cell}} + \dfrac{1 - D_{Eq}}{2\, n_{cell}} \leq D_{Inv} \leq \dfrac{lvl + 1}{n_{cell}}. \end{cases} \tag{A.4}$$

Inverter duty cycle for any number of chopper cells is given by (A.5).

$$D_{Inv} = \begin{cases} \left(V_{Inv} - lvl \cdot \dfrac{V_{Chp}}{n_{cell}} \right) \cdot \dfrac{1}{V_1} + \dfrac{lvl}{n_{cell}} & \text{for } V_{Inv} \leq lvl \cdot \dfrac{V_{chp}}{n_{cell}} + V_1 \cdot \dfrac{1 - D_{Eq}}{2\, n_{cell}} \\ \left(V_{Inv} - lvl \cdot \dfrac{V_{Chp}}{n_{cell}} - \dfrac{D_{Eq}}{n_{cell}} \cdot (V_1 - V_2) \right) \cdot \dfrac{1}{V_1} + \dfrac{lvl}{n_{cell}} & \text{for } V_{Inv} \geq lvl \cdot \dfrac{V_{chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_1 + \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) \\ \left(V_{Inv} - lvl \cdot \dfrac{V_{Chp}}{n_{cell}} - \dfrac{1 - D_{Eq}}{2\, n_{cell}} \cdot (V_1 - V_2) \right) \cdot \dfrac{1}{V_2} + \dfrac{lvl}{n_{cell}} & \text{, otherwise.} \end{cases} \tag{A.5}$$

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