Pinned Photodiode Imaging Pixel With Floating Gate Readout and Dual Gain

Pinned Photodiode Imaging Pixel with Floating Gate Readout and Dual Gain

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***Abstract*—We present an imaging pixel featuring dual conversion gain in a single exposure, based on the pinned photodiode (PPD). The signal charge is first converted to voltage non-destructively using a floating gate, and a second conversion is done at a *pn* junction-based sense node. Higher signal dynamic range is achieved due to the sensing of the same charge with two different conversion gains. The results from a prototype 10 µm pitch pixel manufactured in a 180 nm CMOS image sensor process demonstrate a gain ratio of 3, dynamic range of 90 dB, 3.6 e^- RMS readout noise, and negligible image lag.**

***Index Terms*—Dual conversion gain, high dynamic range (HDR), pinned photodiode (PPD)**

I. Introduction

CMOS image sensors with high dynamic range (HDR) are used in many applications, such as automotive, surveillance, industrial, and scientific. Among the huge variety of existing HDR methods, those using a single exposure are preferred when motion artifacts must be minimized, for example in automotive imaging [1].

One of the most widely used methods to boost the dynamic range (DR) is to use column-level amplifiers with dual gain [2]. Other types of single exposure HDR imagers implement multiple signal readout paths within the pixel, such as dual photodiodes [3] or multiple conversion gains [4][5]. In-pixel signal storage with lateral overflow integration capacitor (LOFIC) [6][7] offers some of the highest DR because the maximum signal is not limited by the capacity of the photodiode. Recently, quanta image sensor offering both deep sub-electron readout noise in photon counting mode and HDR using signal integration has been demonstrated [8].

Virtually all HDR CMOS image sensors use a pinned photodiode (PPD) as the photosensitive element due to its low dark current and readout noise. The maximum output signal, commonly known as the full well capacity (FWC), is often not limited by the charge capacity of the PPD, but by the available voltage span at the sense node. This is particularly true for larger pixels above approximately 5 µm pitch. For a typical area charge capacity of 4 $ke^-/\mu m^2$, a PPD on 5 µm pitch and 60% fill factor can hold up to 60 ke^-. On the other hand, the voltage span at the sense node cannot be much larger than 1.5 V, which for a modest conversion gain (charge to voltage factor, CVF) of 50 $\mu V/e^-$ corresponds to 30 ke^-. Increasing the CVF further limits the amount of charge that can be converted, and although the DR may be improved due to the lower readout noise, a DR significantly higher than 80 dB is difficult to achieve in this way.

The presented development aims to keep the readout noise low while allowing a much larger part of the charge stored in the PPD to be converted to voltage before signal saturation is reached, thus increasing the DR.

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II. Operation and Design

In the proposed pixel the signal charge is converted to voltage twice following a single exposure and a single transfer out of a PPD: first on a floating gate with low CVF, and then a second time on a sense node with high CVF.

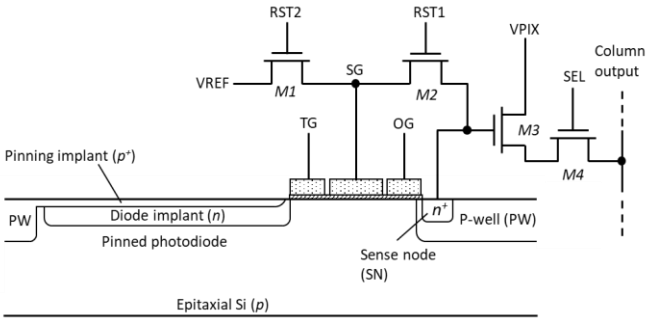

Fig. 1. Cross section along the central line of charge transfer. The n-channel transistors M1-M4 are placed in the p-well (PW).

Figure 1 shows a simplified cross section along the central line of charge transfer in the pixel. A normal PPD is used as the photosensitive element. Following the transfer gate (TG), the charge passes under a floating sense gate (SG) and an output gate (OG) before reaching the sense node (SN). The MOSFET M1 is used to reset SG to the reference voltage VREF. M2 connects SN to SG so that it can be reset to VREF too, and to allow readout of both paths using only one source follower, the M3. M4 is the usual row select switch.

The diagram in Fig. 2(a) depicts the potentials in the pixel at the end of the signal integration period, and after both the SG and the SN have been reset to VREF by turning M1 and M2 on. With M1 turned off and M2 kept on, the charge is transferred out of the PPD with the help of a voltage pulse applied to the transfer gate (Fig. 2(b)). The charge goes under the sense gate while the OG is biased at 0 V to create a potential barrier to the sense node. The signal-induced voltage step on SG is read out non-destructively via M2, M3 and M4 in Fig. 2(c). This readout path has low CVF due to the large

area of the SG and its high capacitance to substrate, and also due to the junction capacitances of M1, M2 and the SN which are all connected in parallel with the SG. Readout of this type has been considered for other applications, although with the opposite requirement – to achieve high CVF on the sense gate [9]. Based on the "skipper" technique [10], multiple signal readouts can be used to reduce the white and 1/*f* noises. Floating gate readout of a *pn*-junction-based storage node for HDR imaging has also been reported [11].

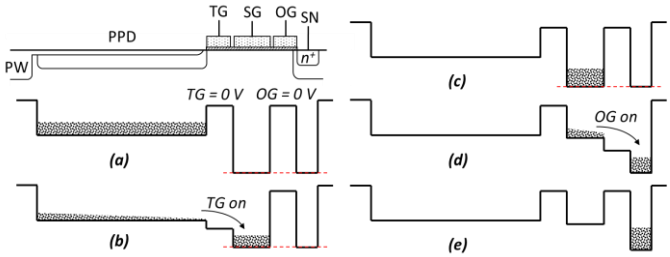

Fig. 2. Potential diagrams during pixel operation.

Next, the charge is transferred to the sense node for the normal charge-to-voltage conversion on a *pn* junction. First, the SN is reset to the voltage VREF by simultaneously turning on M1 and M2, while the charge is kept under SG. Following that, the voltage VREF is lowered while M1 is on, M2 is off, and OG is biased in a way to create a potential gradient towards the SN, as shown in Fig. 2(d). The charge reaches the SN and the signal is read out in Fig. 2(e). This second readout path has high conversion gain because the capacitance of the sense node is small and M2 is turned off. Correlated double sampling (CDS) is implemented for both readout paths by storing the signal at the column output before and after the corresponding charge transfer, thus eliminating the reset noise.

A prototype pixel with the layout shown in Fig. 3 was included in a test chip together with normal PPD (4T) reference pixels. All were laid on a 10 µm pitch, with each type occupying a 128×512-pixel sub-array. The device was manufactured in a 180 nm CMOS image sensor process using 5 µm thick, *p*-type epitaxial silicon with resistivity of 8 Ω.cm. The gap between the polysilicon gates TG-SG, and SG-OG is 0.2 µm.

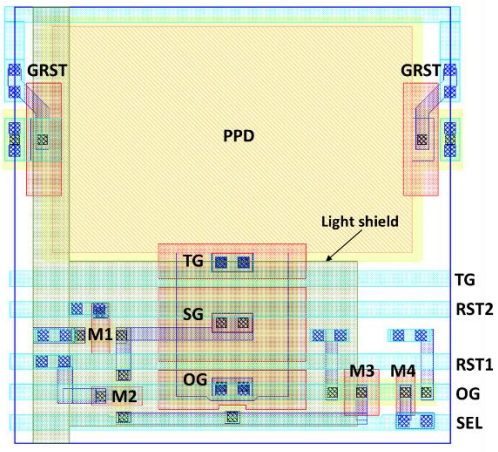

Fig. 3. Layout of the proposed pixel.

The estimated charge storage capacity of the PPD is 170 ke⁻. From TCAD simulations of the charge coupling to the SG, and after including all the capacitances from the layout, the expected CVF for the low and high gain paths was calculated as 13.7 µV/e⁻ and 54.2 µV/e⁻, respectively. As seen in Fig. 1, there is no additional doping under TG, SG and OG. This was chosen to achieve surface channel conditions under SG, so that the largest charge storage capacity can be realized.

The metal track providing the source follower supply VPIX has been enlarged to form a light shield over the SG and the OG. The pixel has global shutter (GS) capability with the help of two global reset (GRST) gates, seen on both sides of the PPD in Figure 3. A distinct advantage of the proposed pixel design is that no changes to the manufacturing process are required.

III. Experimental Results

The performance of the pixel was characterized in rolling shutter mode readout using the control signals shown in Fig. 4. In addition to the signals required to achieve the operation described in Section II, an optional charge clear was added before the PPD charge transfer. The clear is used to remove the charge collected under the SG during integration and is identical to the transfer SG-OG-SN shown in Fig. 2(c)-(e). The sample & hold reset (SHR) is used to store the reset samples in the column CDS circuitry, and SHS does this for the signal samples.

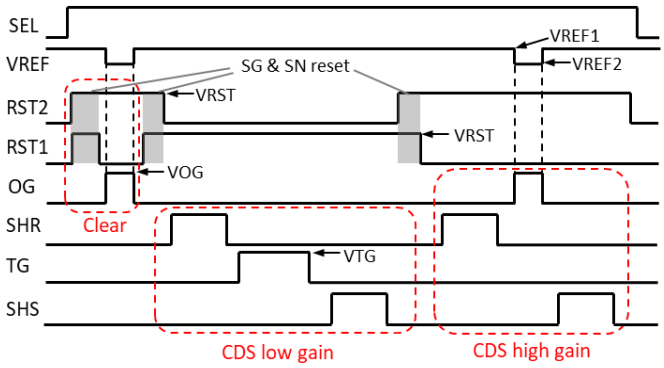

Fig. 4 Timing diagram used for pixel characterization showing the amplitudes of the control signals. The high levels of the signals not indicated are 3.3 V. All low levels are 0 V.

Figure 5(a) shows the photoresponse under visible illumination at 25 °C, and the caption lists the operating conditions used. The conversion gains were determined from the mean-variance curve and the external electronic gain at 15.5 µV/e⁻ and 46.8 µV/e⁻ for the low and high gain readout paths, respectively. Figure 5(b) plots the residuals between the data points and a linear fit to the data between 0 and 90% FWC as a measure of the photoresponse linearity.

A gain measurement using an ^{55}Fe x-ray source, creating charge of 1620 e⁻ from the 5.9 keV Mn-Kα line was also performed and is shown in Fig. 6. The conversion gains obtained from the x-ray measurements are 16.9 µV/e⁻ and 50.0 µV/e⁻ for the low and high gain readout paths, respectively, and agree to better than 10% with the values from the mean-variance derivation.

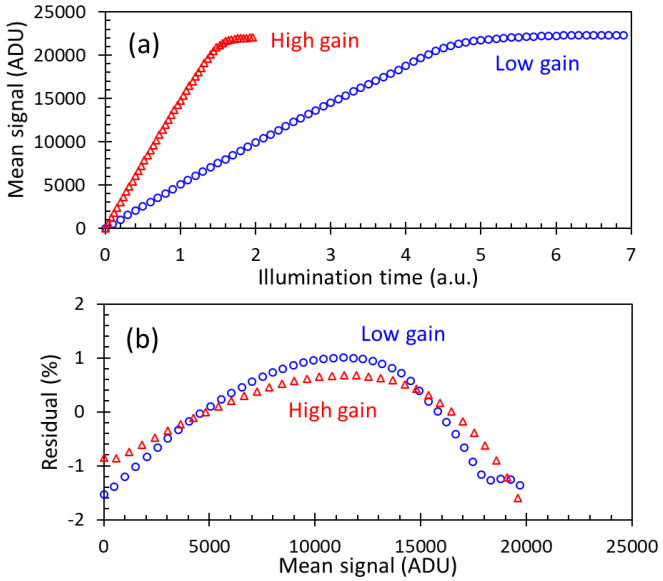

Fig. 5. Photoresponse (a) and linearity (b) at both gains for the following conditions: VREF1 = 2.9 V, VREF2 = 1.0 V, VOG = 1.5 V, VRST = 3.6 V, VTG = 3.3 V, VPIX = 3.3 V. One ADU is 80.1 µV.

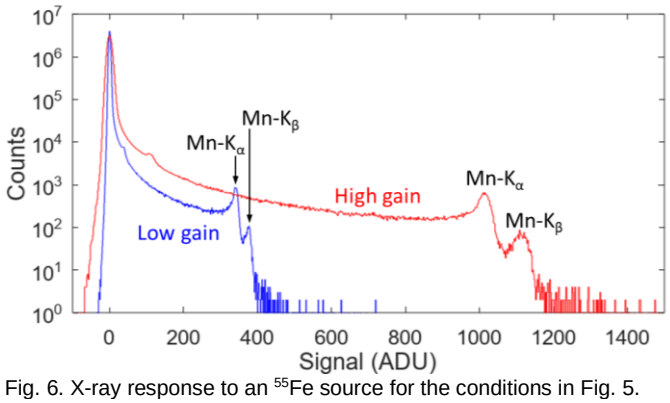

Fig. 6. X-ray response to an ^{55}Fe source for the conditions in Fig. 5.

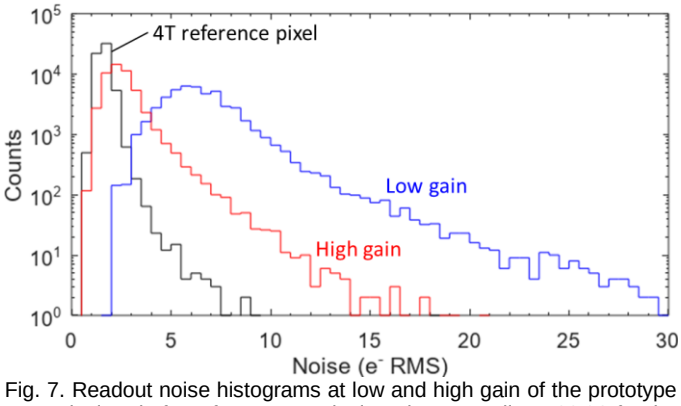

Fig. 7. Readout noise histograms at low and high gain of the prototype HDR pixel and of a reference 4T pixel on the same die at 23 °C for the bias voltages listed in the caption on Fig. 5.

The FWC and the readout noise for the low and high gain paths were measured to be 114 ke⁻ and 6.8 e⁻ RMS, and 38 ke⁻ and 3.6 e⁻ RMS, respectively. The measurements were carried out at 20 fps readout rate and 23 °C and include the shot noise contribution from the dark current. The gain ratio is very close to 3, and the dynamic range is 31700 (90 dB). In one of the reference 4T pixels the FWC is 22 ke⁻ for a CVF of 68 µV/e⁻, and despite the mean noise being lower at 1.63 e⁻ RMS due to the higher conversion gain, the DR is only 82.5 dB.

The readout noise histograms of both gain paths are shown in Fig. 7 together with the noise histogram of the reference 4T pixel. To eliminate the shot noise from the dark current, the transfer gate voltage was kept low for all noise measurements, and the second OG pulse in the timing diagram in Fig. 4 was not applied. With the dark signal eliminated, the readout noise at high gain becomes 2.4 e⁻ RMS and the DR increases to 93.5 dB. This value could be reached if the dark signal is negligible, for example at higher readout rates or if the sensor is cooled.

If not cleared before charge transfer out of the PPD, the dark current measured at the sense node would include the signal generated by interface traps under the SG because the silicon surface there is not pinned. The dark current in high gain mode as a function of VOG, shown in Fig. 8, indicates that VOG must be higher than 1.5 V for efficient clearing of the dark signal when VREF2 = 1.0 V. Under these conditions, the dark currents in low and high gain mode are nearly identical and are close to the values in the reference 4T pixels.

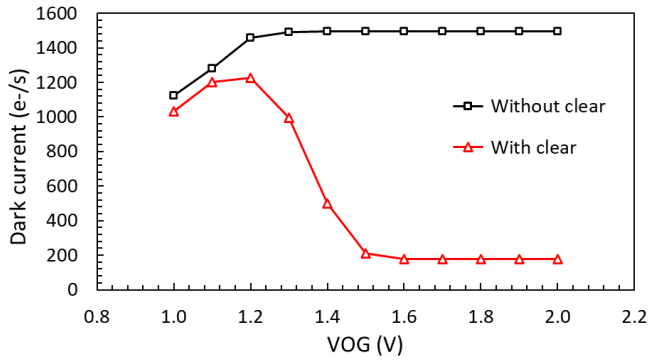

Fig. 8. Dark current in high gain mode, with and without initial signal clear at VREF2 = 1.0 V and 25 °C.

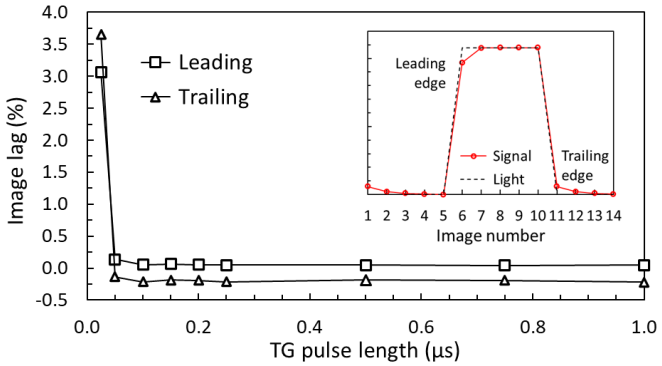

Fig. 9. Image lag as a function of the length of the TG pulse in low gain mode for the bias voltages listed in the caption of Fig. 5 and signal at approximately half FWC (≈54 ke⁻). The dark signal at the device operating temperature of 25 °C is approximately 30 e⁻. The data were obtained from sequences of 5 dark and 5 bright images as shown in the inset.

Both the leading and the trailing image lag were measured because the initial dark signal clear could create a lag asymmetry. The leading edge lag was calculated as the normalized difference between the signals under steady-state illumination and in the first bright image following several dark images. Similarly, the trailing edge lag is the signal in the

first dark image following sufficient number of bright ones, normalized to the signal under steady-state illumination. Experimentally it was established that series of 5 bright and 5 dark images were more than enough to reach the steady state signal levels, as shown in the inset of Fig. 9.

The transfer out of the PPD was confirmed to be lag-free for VTG > 2.7 V when the TG pulse length is 1.5 µs. For the nominal VTG = 3.3 V the lag is negligible for TG pulses as short as 50 ns and is shown in Fig. 9. The lag performance is very good because the transfer gate is relatively wide, and so is the SG, which behaves as a large charge collecting element. A systematic offset of -0.2% in the measured trailing edge lag was found but remained unexplained.

The transfer from the SG to the SN has negligible lag for VOG > 1.3 V as shown in Fig. 10. At VOG = 1.5 V the low lag performance is maintained even for OG pulse lengths below 100 ns.

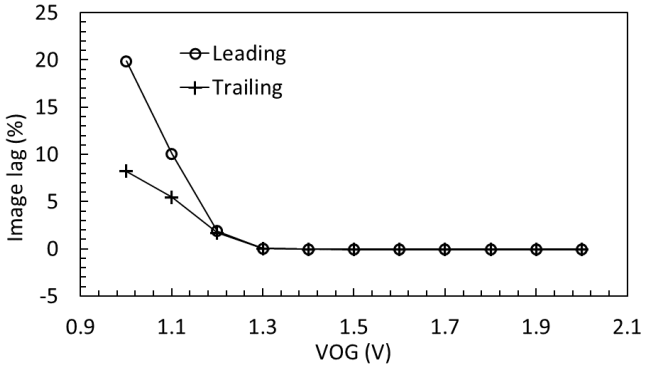

Fig. 10. Image lag as a function of VOG in high gain mode for the bias voltages listed in the caption of Fig. 5 and signal at half FWC (≈18 ke⁻).

The proposed pixel was characterized only in rolling shutter mode to demonstrate its operating principles, but it can also be operated in GS mode. Due to the signal storage under the sense gate, the readout path with high conversion gain accomplishes the same CDS as in rolling shutter mode, and should therefore exhibit the same readout noise. The low gain path would not perform CDS, as is common for most GS imagers.

TABLE I
COMPARISON OF IN-PIXEL DUAL GAIN IMPLEMENTATIONS

Reference	[3]	[4]	[6]	[11]	This work
Method	Dual photodiode	Dual conversion gain	LOFIC	Floating diffusion capacitor	Floating gate
Pixel pitch	3.2 µm	6.5 µm	7.5 µm	5.6 µm	10 µm
Process	110 nm	180 nm	350 nm	350 nm	180 nm
Exposure	Triple	Single	Single	Dual	Single
RMS noise	0.94 e⁻	2 e⁻	5 e⁻	10 e⁻	3.6 e⁻
DR	120 dB	87 dB	100 dB	100 dB	90 dB

Table 1 summarizes and compares the main characteristics of several PPD-based HDR pixels employing different in-pixel dual gain methods with this work.

IV. CONCLUSION

In this brief we present a new PPD-based pixel design using a floating gate to accomplish two consecutive signal readouts with different conversion gains. The pixel operates with a single exposure and a single charge transfer out of the PPD. The first prototype demonstrates significantly increased DR and negligible image lag. Although this implementation is for a pixel on 10 µm pitch, the proposed architecture could be scaled down to smaller pixels. Further improvements to the DR could be achieved by reducing the sense node capacitance and the readout noise, and also by increasing the sense gate capacitance. The proposed pixel architecture could be attractive for HDR imagers using single exposure.

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