DESIGN AND ANALYSIS OF A DISCRETE, PCB-LEVEL LOW-POWER, MICROWAVE CROSS-COUPLED DIFFERENTIAL LC VOLTAGE-CONTROLLED OSCILLATOR

A Thesis

presented to

the Faculty of California Polytechnic State University,

San Luis Obispo

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

by

Pavin Singh Virdee

September 2022

COMMITTEE MEMBERSHIP

TITLE: Design and Analysis of a Discrete, PCB-Level Low-Power, Microwave Cross-Coupled Differential LC Voltage-Controlled Oscillator

AUTHOR: Pavin Singh Virdee

DATE SUBMITTED: September 2022

COMMITTEE CHAIR: Dean Y Arakaki, Ph.D., Associate Professor of Electrical Engineering

COMMITTEE MEMBER: Dennis Derickson, Ph.D., Professor of Electrical Engineering

COMMITTEE MEMBER: Steve Dunton, M.S., Electrical Engineering Lecturer

ABSTRACT
Design and Analysis of a Discrete, PCB-Level Low-Power,
Microwave Cross-Coupled Differential
LC Voltage-Controlled Oscillator
Pavin Singh Virdee

Radio Frequency (RF) and Microwave devices are typically implemented in Integrated Circuit (IC) form to minimize parasitics, increase precision and tolerances, and minimize size. Although IC fabrication for students and independent engineers is cost-prohibitive, an abundance of low-cost, easily accessible printed circuit board (PCB) and electronic component manufacturers allows affordable PCB fabrication.

While nearly all microwave voltage-controlled oscillator (VCO) designs are IC-based, this study presents a discrete PCB-level cross-coupled, differential LC VCO to demonstrate this more affordable and accessible approach. This thesis presents a 65 mW, discrete component VCO PCB with industry-comparable RF performance. A phase noise of -103.7 dBc/Hz is simulated at a 100 kHz offset from a 4.05 GHz carrier. This VCO achieves a 532 MHz (13.25%) tuning bandwidth. A figure of merit, FOM_P, [1] value of -177.7 dB (includes phase noise and power consumption) is calculated at 4.05 GHz. This surpasses the performance of an industry standard VCO (HMC430LPx, Analog Devices), -176.5 dB, and four other commercially available VCOs. Furthermore, this study presents novel discrete design implementations to minimize both power consumption and capacitive loading effects, while optimizing phase noise. Finally, this project serves as a reference for analyzing and implementing low-level, complex RF and Microwave circuits on a PCB accessible to all students and independent engineers.

Keywords: Voltage-Controlled Oscillator, PCB, RF and Microwave Circuits, HBT, Low-Power, Differential Pair, Phase Noise, Discrete

ACKNOWLEDGMENTS

I would like to personally thank Astranis Space Technologies for sponsoring and facilitating this design study and project. In particular, Charles Chen for his technical expertise, mentoring, and guidance through this process. I would like to thank Dr. Dean Arakaki for all his unwavering support and guidance as both my Senior Design Project and Master's Thesis Advisor. Additionally, my Thesis Committee of Dr. Dennis Derickson and Professor Steve Dunton have played a crucial, positive role in my entire Cal Poly, SLO education. I finally thank my family and close friends for supporting me through thick and thin, always pushing me to become the best version of myself.

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Chapter 1

INTRODUCTION

A key performance parameter for most electronic devices is power consumption. Operating voltage and current levels are always stated on datasheets from which power consumption can be determined. From aerospace applications to consumer electronics, power consumption is a crucial design consideration because it defines battery and thermal requirements along with system efficiency. For example, reduced cell phone power consumption leads to increased operating time between charges, decreased operating temperature, and increased overall system lifetime. Hence, power consumption must be minimized without compromising system performance.

Almost all modern wireless systems require reference or clock signals. A frequency synthesizer is an electronic device that produces a signal at a user-defined frequency. Frequency synthesizers are ubiquitous in RF systems due to the wide range of local oscillator (LO) signals. Evolving technology demands greater frequencies, wider bandwidths, and overall enhanced performance [2]. The challenge lies in attaining this increased performance while limiting power consumption.

A voltage-controlled oscillator (VCO) generates a sinusoidal output whose oscillation frequency is controlled by an external voltage. The RF performance of the frequency synthesizer is heavily dependent on the VCO's RF performance. Generally, phase noise and output power are VCO dependent since it is the frequency synthesizer's output stage. Although optimal RF performance is desired, VCO power consumption

must be minimized. VCOs consume a large fraction of RF front end power, specifically in frequency synthesizers [3].

The objective of this project is to design, analyze, and implement a low-power microwave voltage-controlled oscillator. The design features a cross-coupled differential pair, LC tank circuit, current sink, and output buffer comprised of discrete transistors, varactor diodes, lumped components, and transmission lines. Target design specifications are listed in Table 1.1 below and are generally defined by this project's industry sponsor, *Astranis Space Technologies*. The phase noise and power consumption based figure of merit, FOM_P is an industry and academia standard [1] defined below in Table 1.1. Minimizing FOM_P by reducing PN and P_{DC}, corresponds to improved VCO performance. The $(f_{carrier}/f_{offset})$ ratio term compensates for phase noise; PN increases with $f_{carrier}$, but decreases with f_{offset}, hence this term is negative.

Table 1.1: Target VCO Design Specifications

Parameter	Description	Min	Typ	Max	Units
f	Operational frequency range	4.5	5	-	GHz
P_{out}	Output power at 4.5 GHz	-5	-	-	dBm
I_{CC}	Supply Current	-	-	100	mA
V_{CC}	Supply Voltage	2.5	3.3	4.0	V
PN	Phase Noise @ 4.5 GHz; 100 kHz offset; 1 Hz BW	-	-	-100	dBc
FOM_P [1]	Phase Noise based Figure of Merit	-	-170	-167.9	dB

[1] $FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])$

Optimized techniques are applied to minimize VCO phase noise and loading effects and overall power consumption. Circuit parasitics and printed circuit board (PCB)

layout effects are analyzed using Keysight's Momentum, a Method of Moments based Electromagnetic Simulator.

High-frequency, transistor-based, low-level circuits are generally implemented as integrated circuits (ICs) in surface mount technology (SMT). To increase accessibility to the general student and independent engineer, this VCO is designed and implemented using discrete components on a PCB. Implementing this circuit on a PCB as opposed to an IC is avoided due to increased circuit parasitics, decreased precision and tolerance, and larger size. However, IC fabrication for an independent student or engineer is expensive and impractical. With an abundance of PCB manufacturers now offering accessible and low cost services, PCB fabrication is practical. This project serves as a reference for analyzing and implementing a low-level, complex RF circuit on a printed circuit board accessible to all students and engineers.

Chapter 2

BACKGROUND AND DESIGN THEORY

Electronic oscillators include a non-linear, initially unstable (steady-state stable) frequency generator and a resonant circuit to specify the oscillation frequency. To initiate and sustain oscillations, low frequency oscillators generally satisfy Barkhausen Criterion [4] while high frequency microwave and millimeter wave oscillators utilize negative resistance circuit behavior [5]. Fixed-frequency and voltage-controlled oscillators are introduced along with general RF PCB fundamentals. Distributed and lumped component theory are also discussed.

2.1 Microwave Oscillators

An oscillator is an electronic circuit that generates a sinusoidal output signal at a particular frequency. High-Q resonant circuits select the oscillation frequency. At microwave frequencies these passive, resonant circuits are cavities, transmission lines, high-Q discrete components, or dielectric resonators [6]. Lower frequency, RF oscillators utilize quartz crystals in their resonant circuits to achieve high quality factors (Q), however as quartz crystals approach microwave frequencies, quality factor degrades [6]. High-Q discrete components, such as chip inductors and capacitors, are more common at lower microwave frequencies since self-resonant frequencies (SRF) limit usage (more on SRF in Section 2.6). An ideal resonant circuit is lossless with an infinite-Q, theoretically oscillating on its own. However, in practice, device parasitics in resonant circuits

introduce losses, resulting in a finite quality factor. This loss requires additional circuitry to provide sufficient oscillation energy.

Non-linear, active circuits provide energy to the resonant circuit to negate losses in one- or two-port devices. Two-port oscillators operate below microwave frequencies and are composed of a feedback network, shown in Figure 2.1.

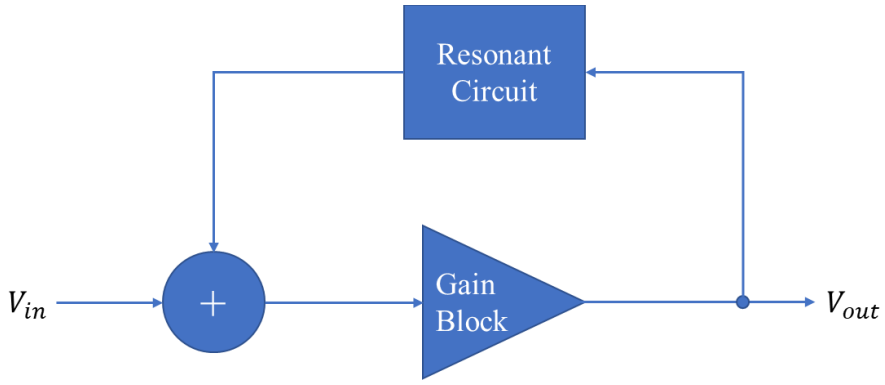


Figure 2.1: Feedback Network, Two-Port Oscillator

The Barkhausen criterion defines the oscillation conditions of these two-port, feedback devices [7]. The oscillation frequency f_o requires,

I. Closed-loop gain magnitude greater than unity.

II. Closed-loop, positive feedback (2π integer multiple phase shift).

A noise source, such as a transient from powering on a DC power supply, is the input voltage V_{in}, whereas the output voltage V_{out} is the sinusoidal signal.

Microwave oscillators are typically one-port negative resistance oscillators or reflection oscillators, shown in Figure 2.2.

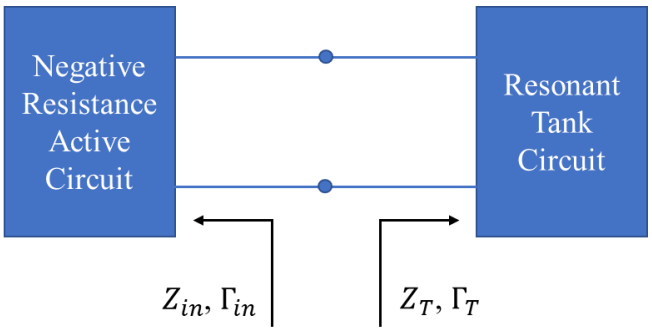


Figure 2.2: One-Port Oscillator Network Diagram

These active circuits include diodes or transistors which exhibit a negative resistance and conductance [6]. Impedance, admittance, and reflection coefficient are defined below in Equations (2.1) - (2.3), respectively.

$$Z = R + jX \tag{2.1}$$

$$Y = \frac{1}{Z} = G + jB \tag{2.2}$$

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.3}$$

Equation (2.1) shows that both active circuit Z_{in} and resonant circuit Z_T include both real and imaginary components. From Kirchhoff's Voltage Law (KVL), the sum of voltages in the one-port network loop diagram of Figure 2.2 must equal zero, $(Z_{in} + Z_T)I = 0$ [6]. To produce an RF signal with nonzero current flow ($I \neq 0$), $(Z_{in} + Z_T)$ must equal zero to satisfy KVL [6]. Therefore, the one-port oscillator start-up criteria are [6],

$$R_{in} + R_T = 0 \tag{2.4}$$

$$X_{in} + X_T = 0 \tag{2.5}$$

Since the passive tank circuit exhibits positive resistance, R_T, the active circuit must have a negative resistance ($R_{in} < 0$) to satisfy equation (2.4). Intuitively, the active circuit provides negative resistance (producing energy) to overcome resonant circuit losses (dissipated energy), resulting in a net lossless equivalent network. Since R_{in} represents the active circuit's input resistance from non-linear devices such as transistors, it is frequency and current dependent.

The start-up oscillation frequency is determined by evaluating the frequency dependence of equation (2.5). A zero-crossing in equivalent reactance ($X_{in} + X_T$), results in resonance, specifying the start-up oscillation frequency. Figure 2.3 illustrates this theoretical equivalent reactance behavior.

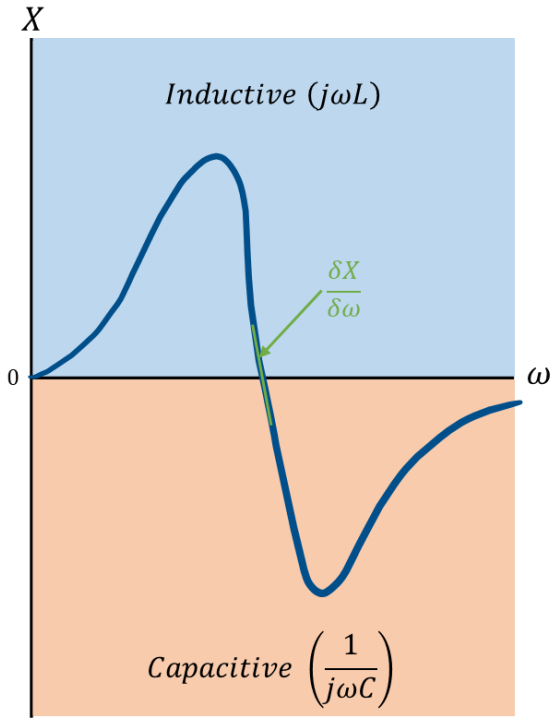


Figure 2.3: One-Port Oscillator Equivalent Reactance Frequency Response

The transition state slope $\delta X/\delta\omega$ between the inductive and capacitive regions is proportional to quality factor and frequency stability [8]. Additionally, the inductive and capacitive regions describe parallel LC equivalent reactance. The capacitor/inductor behavior dominates at frequencies above/below resonance.

Following oscillation start-up, Kurokawa's Laws guarantees stable, steady-state oscillations [5]. For a passive resonant circuit, $\partial R_T/\partial I = \partial X_T/\partial I = \partial R_T/\partial\omega = 0$, therefore, equation (2.6) defines Kurokawa's oscillator condition [9].

$$\frac{\partial R_{in}}{\partial I}\frac{\partial}{\partial \omega}(X_{in} + X_T) - \frac{\partial X_{in}}{\partial I}\frac{\partial R_{in}}{\partial \omega} > 0 \tag{2.6}$$

From equation (2.6), given $\partial R_{in}/\partial I > 0$, maximum oscillator stability is guaranteed if $\frac{\partial}{\partial \omega}(X_{in} + X_T) \gg 0$. Since $X_{in} + X_T$ is the equivalent reactance of the one-port network, this term is simplified to total reactance, X, and the frequency-derivative term of equation (2.6) is rewritten as $\partial X/\partial \omega$. As mentioned above and shown in Figure 2.3, this term represents the slope of the reactance, as it transitions from inductance to capacitance. The $\partial X/\partial \omega$ term is also proportional to resonance quality factor [5]. Therefore, maximizing quality factor enhances oscillator stability.

From equation (2.6), R_{in} varies with current, and hence power. In transistor-based microwave oscillators, R_{in} may increase (become less negative) with oscillator power. To ensure both oscillation start-up and steady-state stability, a sufficient margin must exist between R_{in} and R_T. Equation (2.7) defines a practical relation between the two circuit characteristics to guarantee and sustain oscillations [6].

$$-R_{in} \geq 2\, R_T \tag{2.7}$$

Since most microwave oscillators are one-port devices (negative resistance, reflection oscillators), two-port oscillator topologies are not discussed. Common single transistor-based topologies include Colpitt's, Hartley, and Clapp oscillators. The main distinction between Colpitt's, Hartley, and Clapp oscillators is their resonant tank feedback network, shown in Figure 2.4.

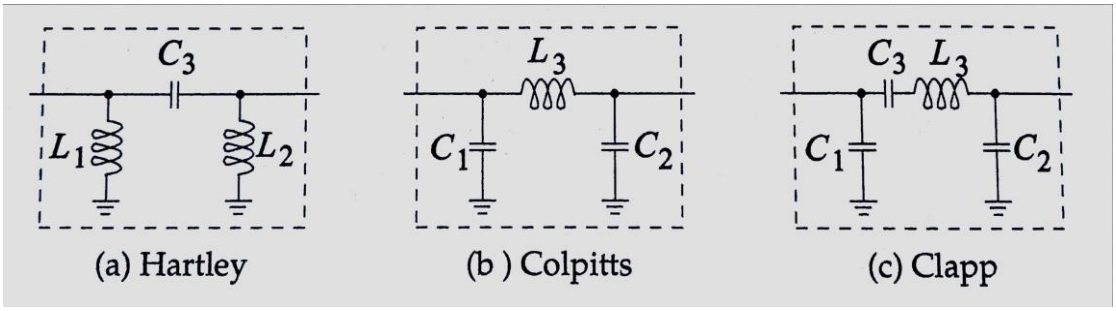


Figure 2.4: Single Transistor-based Resonant Feedback Circuit Topologies [4]

These feedback networks are typically applied to common-source/emitter or common-gate/base circuits to enhance device instability [6]. The Colpitt's topology is common in microwave oscillators as C_1 and C_2 absorb the shunt transistor device capacitances (they are summed due to a parallel configuration) [4]. The Clapp oscillator is typically applied to lower frequency (< UHF-band) crystal oscillators as L_3 and C_3 model a quartz crystal.

A popular oscillator topology utilizes a cross-coupled, differential pair, also known as a negative transconductance differential oscillator, shown in Figure 2.5.

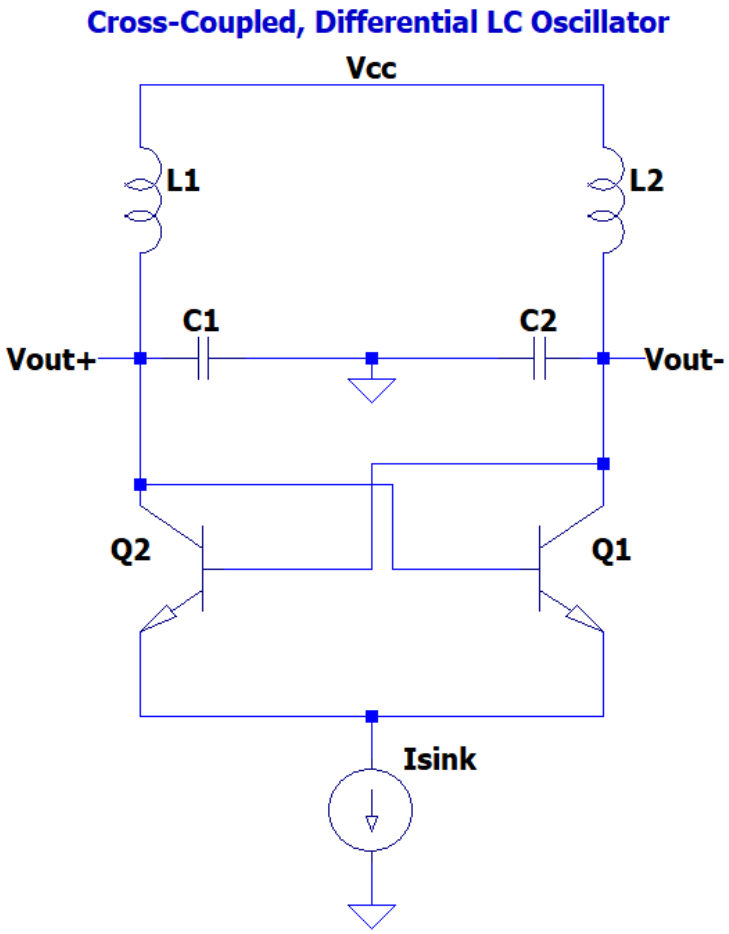


Figure 2.5: Cross-Coupled Differential Oscillator Circuit

This circuit topology has increased in popularity due to its cross-coupled feedback, differential nature, optimized harmonic suppression, maximized output power, excellent phase noise capabilities, and simple negative resistance realization.

2.2 Voltage-Controlled Microwave Oscillators

Voltage-controlled oscillators (VCO) use an external DC voltage to tune the oscillation frequency. In nearly all cases, VCOs use fixed-frequency oscillator configurations; varactor diodes replace fixed capacitors in the resonant tank circuit [3].

For example, in the cross-coupled, differential oscillator topology of Figure 2.5, capacitors C_1 and C_2 are replaced with varactor diodes controlled by an external DC tuning voltage.

Varactors are reversed-biased diodes that act as variable capacitors. The applied reverse-bias voltage is proportional to depletion region width. Equation (2.8) below defines capacitance as a function of dielectric permittivity (ϵ), plate area (A), and plate separation distance (d). The effective area (A) in a varactor diode is the cross-section of the p- or n- doped regions. The distance term (d) is the depletion region width.

$$C = \frac{\epsilon A}{d} \tag{2.8}$$

From equation (2.8), the varactor's effective junction capacitance is inversely proportional to depletion region width. Therefore, its capacitance is also inversely proportional to the reverse-bias voltage. The varactor capacitance voltage dependence controls the tank circuit (and VCO) resonance frequency, as shown in equation (2.9).

$$f_o = \frac{1}{2\pi\sqrt{L_{total}\, C_{total}}} \tag{2.9}$$

L_{total} and C_{total} represent the total inductance and capacitance within the oscillator circuit. Varactor capacitance is directly proportional to C_{total} and inversely proportional to f_o. Therefore, the applied reverse-bias voltage, or VCO control voltage, is directly proportional to the VCO's output frequency. Figure 2.6 below defines the varactor diode equivalent circuit model.

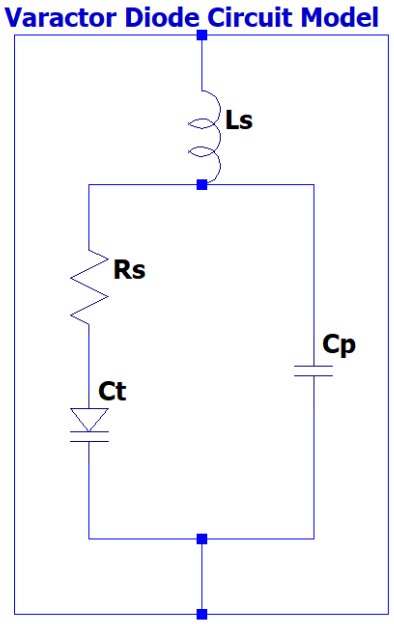


Figure 2.6: Equivalent Varactor Diode Circuit Model

Table 2.1: Varactor Diode Circuit Model Parameter Definitions

Circuit Parameter	Description	Units
L_S	Equivalent series inductance (ESL)	H
R_S	Equivalent series resistance (ESR)	Ω
C_P	Port-to-port parasitic capacitance	F
C_t	Varactor effective junction capacitance	F

Since parasitic capacitance, C_P, is small relative to the varactor's junction capacitance, C_t, it is neglected, and the circuit simplifies to a series RLC network. The self-resonant frequency (SRF) is defined by C_t and L_s through equation (2.9). The varactor's ESR introduces device losses and limits the quality factor via equation (2.10).

$$Q_v = \frac{1}{\omega_o RC} \tag{2.10}$$

When selecting a discrete varactor diode, it is critical to ensure ESL is minimized to maximize the SRF. Since the device equivalent circuit model is a series RLC, the capacitor dominates the equivalent impedance at frequencies below the SRF; the inductor dominates at frequencies above. Therefore, to ensure the varactor diode exhibits capacitor operation, operating frequencies must be below the SRF.

As previously mentioned, the general VCO theory matches that of traditional microwave oscillators, however start-up and steady-state criterion must be verified at all operating frequencies. Additionally, common VCO circuits use fixed-frequency oscillator configurations, with the addition of varactor diodes.

2.3 Oscillator/VCO Applications

Fixed-frequency and voltage-controlled oscillators are found in nearly all RF and wireless systems. From communications to aerospace to consumer electronics, wireless hardware is ubiquitous today. Oscillators are used in complex RF systems including phased-locked loops, transmitters, receivers, and frequency synthesizers.
Figure 2.7 defines a phase-locked loop-based frequency synthesizer, whose performance is VCO dependent.

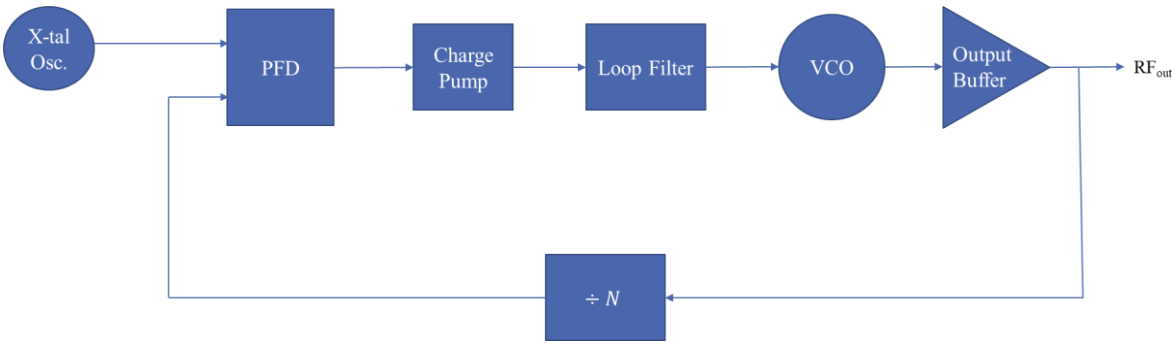


Figure 2.7: General Phase-Locked Loop based Frequency Synthesizer Block Diagram

While oscillators provide greater frequency stability than voltage-controlled oscillators due to their fixed-frequency operation, VCOs are equally prevalent in communication systems due to their frequency flexibility. VCO's are also in frequency modulation (FM). Applying a low frequency voltage signal to a VCO's control input produces a frequency-varying FM output signal.

As previously mentioned, VCO's consume the bulk of the power in RF components and front ends, while also defining the RF performance of such devices [3]. Therefore, finding a low-power, high-performing VCO can be expensive. Companies such as *Analog Devices* currently offer off-the-shelf VCO's for purchase, ranging from ≈ $21 to ≈ $241 per chip. Table 2.2 below highlights several in-stock, off-the-shelf VCO's with best-case, rated performances, sorted by FOM_P. This table includes the phase noise based figure of merit, FOM_P; minimum value corresponds to best-case VCO performance. Note, VCO cost is proportional to operating bandwidth, which increases phase noise and FOM_P.

Table 2.2: Alternative Stocked Market VCO's

VCO Part	Manufacturer	Price (USD)	Operating Frequency (GHz)	% Bandwidth (%)	Phase Noise[1] (dBc/Hz)	Power Consumption (mW)	FOM_P (dB)
HMC587LC4B **[10]**	Analog Devices	$241.71	5 – 10	66.7	-95	275	-164.6
HMC586LC4B **[11]**	Analog Devices	$241.71	4 – 8	66.7	-100	275	-167.6
PE1V11027 **[12]**	Pasternack	$121.99	4.26 – 5	16.0	-105	275	-173.2
CVCO55HB **[13]**	Crystek Corp.	$24.37	4.75 – 5.1	7.1	-106	210	-176.1
HMC430LPx **[14]**	Analog Devices	$21.64	5.0 – 5.5	9.5	-103	110.5	-176.5

[1] Best case phase noise (in these devices, minimum operating output carrier frequency) taken at a 100 kHz offset frequency and nominal DC power consumption

2.4 Microwave PCB Design

High frequency printed circuit board design requires transmission lines, layer substrate stack-ups, material selection, and discrete component models. Additionally, microwave PCBs generally require greater care when routing traces since most RF traces are considered transmission lines, hence full transmission line effects must be considered. Grounding, return current path, and signal integrity also must be considered for sufficient electromagnetic compatibility.

2.4.1 Layer Stack-Ups

A printed circuit board includes “stacked-up” layers, either conductive signal or plane layers with insulative, dielectric substrates separating them. Materials such as copper, gold, or even silver compose the conductive layers. These materials are common as they have superior electrical and thermal conductivity [15]; hence, used for signal routing or planes. Plane layers are full conductor sheets; ground or power planes. Vias are tunnel-like conductive structures that interconnect conductive signal layers.

Insulative, dielectric materials compose the base, core, and prepeg of circuit boards – they serve as substrates separating conductive layers. Substrates are application-dependent dielectric materials. This material is specifically chosen to minimize circuit parasitics and loss, to provide increased mechanical rigidity, or to optimize thermal properties. The most common PCB dielectric material is FR4, a woven glass fiber epoxy compound [16]. Although FR4 is a low-cost, mechanically rigid dielectric material, it suffers a high dielectric constant (4.5) and dissipation factor, or loss tangent (0.018). These electrical characteristics detract from microwave PCB design in the GHz and beyond frequencies. In contrast, *Rogers Corporation* produces high-performing dielectric materials for microwave circuit boards. Their 5880 RT/Duroid laminate features an excellent 0.0004 dissipation factor and 2.20 dielectric constant at 10 GHz. These electrical properties not only minimize losses, but also decrease transmission line size [15].

The number of PCB layers can vary from 2 to beyond 32. This layer selection is application dependent, where design complexity increases with layer count. The specific layer stack-up and dimensions are at the discretion of both the designer and board

manufacturer. For example, if the PCB manufacturer supports the layout, the designer has the freedom to select specific dielectric materials, conductive layer separation, layer count, via structures, and much more.

2.4.2 Design Considerations

Most circuit designs include RF, baseband (low-frequency analog), digital, and power lines. It is recommended to isolate RF/analog signals from both digital and power lines to avoid unintentional coupling and maintain controlled impedances [17]. Additionally, the type of RF transmission line (i.e., microstrip, stripline, grounded coplanar waveguide) must be considered. For example, if microstrip is used, a solid ground plane layer must be directly below the microstrip layer. Transmission lines are further discussed in Section 2.5. Furthermore, although power planes are AC/RF grounds, traditional ground planes are recommended to decrease ground impedance and noise, minimize ground loops, and reduce return current loop area (minimizing parasitic inductance).

Kirchhoff's Current Law states that the sum of currents flowing into or out of a node must equal zero. In other words, all electric currents must return to their source. Usually, only the forward current path is considered (most board traces), however the return current path is equally, if not more, important. If the return current path is too long or creates a large loop, it can absorb noise along its path, create parasitic inductance, and cause board radiation. Planning this return current path while routing traces and including adjacent ground plane layers [17] in designs reduce these parasitic effects and optimize signal integrity.

Noise and harmonic suppression are important for RF PCBs since they can potentially leak into the operating frequencies and cause unintentional interference. Power (or any general DC) lines must be sufficiently decoupled to reduce external noise. Ground shunted bypass capacitors placed near power pins and board power inputs provide a direct, low-impedance path to ground for noise while preserving power integrity. Additionally, when routing several close-proximity traces, the separation distance should be considered to avoid unintentional coupling. Different transmission line structures provide shielding to critical traces, reducing external radiation. Furthermore, ground plane regions (not full layers) also provide additional shielding to critical, externally exposed signals.

Circuit parasitics must be evaluated at microwave frequencies. Parasitic inductance and capacitance in a RF PCB vary based on the substrate dielectric material. At microwave frequencies, these parasitics drastically shift impedances and affect circuit performance. For example, in an oscillator, these parasitic ESL and shunting capacitance contribute to L_{total} and C_{total} which define the resonant frequency. Generally, increasing line length increases parasitic inductance, while increasing trace area (or width) increases parasitic capacitance. Vias also add considerable inductance to signal paths [17]. Additionally, trace shapes affect loss, reflections, and parasitics. In RF traces it is recommended to use smooth turns and transitions to minimize reflections since most high frequency current flows along the trace surface and edge, per skin effect [18].

Another important design consideration is impedance matching. Significant reflections and power loss occur if trace characteristic and port impedance are not matched. Impedance mismatch also leads to increased power loss and dissipation in the

form of heat. Thermal effects should also be evaluated. High-power lines or circuits require wider and thicker traces to handle increased power. Signal planes serve as an alternative to traditional traces for increasing power handling capabilities. However, the increased parasitics (specifically planar capacitance) and controlled impedance requirements must be considered when switching from signal traces to planes. Grounding vias can also be placed near high power circuits to increase thermal conductivity. These vias help transfer and distribute heat to larger ground planes where there is more surface area to dissipate heat away from critical circuits. Via stitching adjacent ground planes can further improve thermal conductivity as well as increase ground continuity.

2.5 Transmission Lines

Transmission lines transfer electrical signals through electromagnetic wave propagation at the speed of light, v_p (m/s), in the transmission line. v_p is the product of transmission line wavelength (m) and frequency (Hz), shown in equation (2.11):

$$v_p = \lambda_r f = \frac{c}{\sqrt{\epsilon_r}}\ , \tag{2.11}$$

where, λ_r is transmission line wavelength, c is speed of light in vacuum, and ϵ_r is substrate relative permittivity. This relation highlights the inverse relationship between frequency and wavelength and is fundamental to RF transmission line theory. Typically, RF transmission lines are considered distributed circuits modeled by lumped elements per unit length. Series inductors with shunt capacitors model a lossless transmission line.

Series resistance and shunt conductance are added for lossy transmission lines. Figure 2.8 defines the equivalent lumped circuit model for a length dz general transmission.

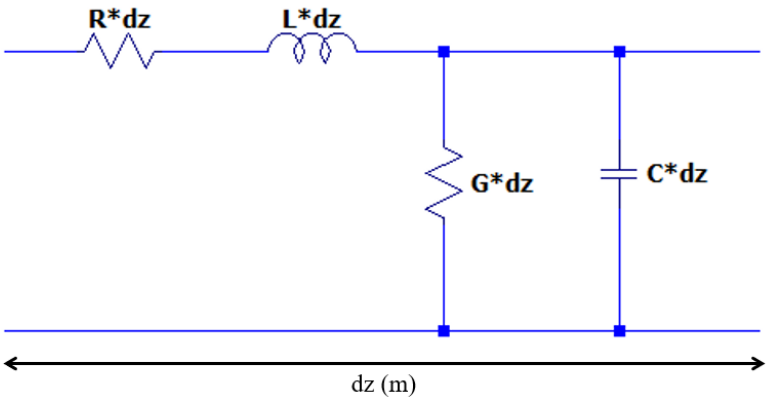


Figure 2.8: General Transmission Line Lumped Circuit Model

As frequency increases, wavelength decreases, approaching the size of the physical channel itself. As wavelength approaches physical channel length (typically, $l_p > \lambda/10$), alternating current (AC) signals become travelling waves, propagating down the channel. As the wave propagates it is susceptible to reflections, phase delays, and losses. Controlled impedance channels and port impedance matching minimize reflections and losses.

Planar transmission lines are some of the most common transmission line types and are all of those implemented on a printed circuit board. The most common planar transmission line types are stripline, grounded coplanar waveguide (CPWG), and microstrip. Microstrip lines have a top signal trace with a bottom adjacent layer ground plane. Grounded coplanar waveguide features a top middle signal trace with ground planes on either side around it. Similar to microstrip, CPWG features a bottom adjacent

layer ground plane. Stripline differs from both microstrip and CPWG as the signal trace is within the dielectric substrate, unexposed to free space air. The stripline architecture features the middle signal trace with two top and bottom adjacent layer ground planes. Figure 2.9 illustrates these three transmission line types.

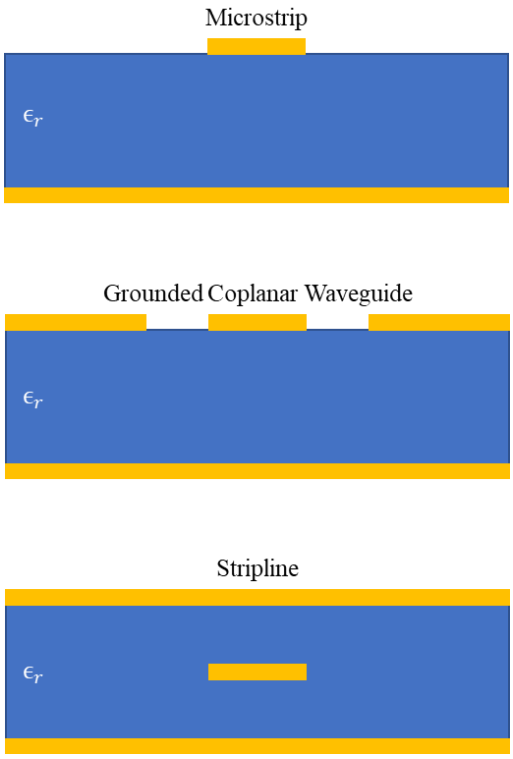


Figure 2.9: Common Planar Transmission Line Types

Where stripline offers superior shielding for the RF signal lines, it can suffer poor losses as all the propagating wave's electric fields are confined within the dielectric material. CPWG still offers top layer shielding, protecting traces from external radiation while offering less dielectric loss. CPWG electric fields are evenly distributed between the top layer adjacent ground planes and the bottom layer ground plane. This is beneficial because the top layer electric field propagates through free space (not the substrate) minimizing loss. However, CPWG requires an increased surface area and more vias to

stitch the top and bottom ground planes together, altogether increasing cost. Microstrip is the most popular planar transmission line type for microwave frequencies (up to around 30 GHz) [15]. It offers a simpler architecture than both CPWG and stripline, making it the simplest to fabricate and integrate with both passive and active devices [19]. Microstrip lines reduce losses relative to stripline because electric fields travel through air in addition to dielectric. Although, CPWG still offers lower loss than microstrip, this minimized loss is not significantly observed until frequencies reach the tens of GHz. However, microstrip line characteristics (i.e., impedance, phase delay) vary with the substrate dimensions, therefore high fabrication tolerance must be ensured to guarantee optimal RF performance. Table 2.3 below compares each planar transmission line architecture for ten design parameters. The best assigned value is 3, while 1 is the worst assigned value. CPWG totals the greatest value showing its strong overall performance. Although Microstrip has the lowest overall value, selecting a planar transmission line type is frequency and application dependent. For example, if decreased cost and manufacturing difficulty at low, microwave frequencies is desired, Microstrip is optimal.

Table 2.3: Planar Transmission Line Architecture General Comparison

Parameter	Microstrip	CPWG	Stripline
Shielding	1	2	3
Least Loss	2	3	1
Reducing Line Dispersion	1	2	3
Ease of Manufacturing	3	2	1
Least Radiation	1	2	3
Cost	3	2	1
Impedance Control	2	3	1
Coupling Control	1	3	2
Design Compactness	2	1	3
Total /30 (∴highest value desired)	16	20	18
Note: 3 = best, 1 = worst			

2.6 Discrete, Lumped Passive Components

A discrete component is a single circuit element confined to a single package. Lumped components are circuit elements that have fixed values over a given area or length. Discrete, lumped passive components are fixed-valued circuit elements confined within single packages, such as resistors, capacitors, and inductors.

At lower analog frequencies these components will typically follow their ideal circuit model, however microwave frequencies demand a more analytical approach to selecting these components. Although the ideal and actual circuit model of a resistor closely resembles a resistor, a capacitor and inductor are unique. Figure 2.10 and Figure 2.11 highlight the ideal vs. actual component circuit models for an inductor and capacitor, respectively.

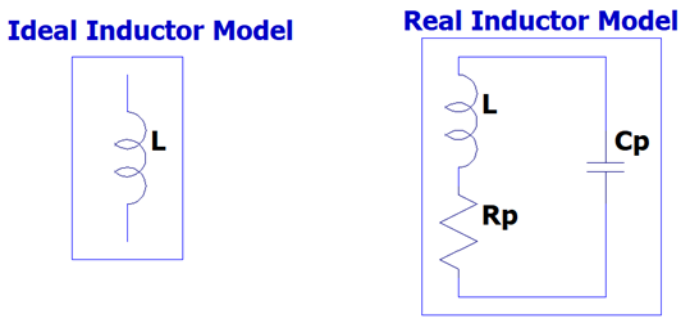


Figure 2.10: Ideal vs. Actual Inductor Component Circuit Models

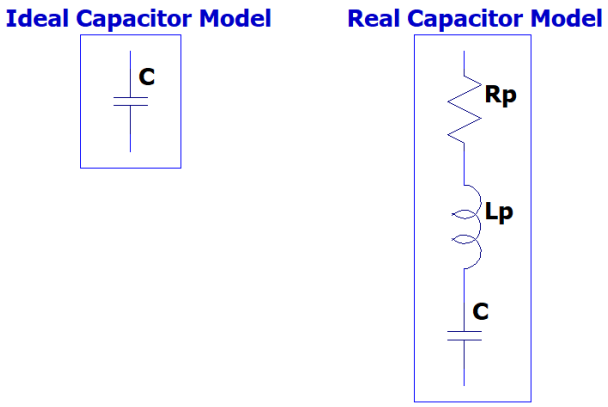


Figure 2.11: Ideal vs. Actual Capacitor Component Circuit Models

Both cases include parasitic ESR, which represents inherent loss in practical components. For RF applications, such as in filters and tank circuits, this loss must be minimized. As previously mentioned, quality factor characterizes circuit loss. Since these discrete, passive component elements are actually equivalent circuits, quality factor characterizes passive component loss.

Quality factor describes the ratio between stored and dissipated energy, or reactance and resistance, as shown in equation (2.12).

$$Q = \frac{f_o}{BW_{3dB}} = \frac{X}{R} = \frac{Stored\ Energy}{Dissipated\ Energy} \tag{2.12}$$

The impedance of an inductor is $j\omega L$ while that of a capacitor is $\frac{1}{j\omega C}$, where $\omega = 2\pi f$ is angular frequency in radians per second. This results in equations (2.13) and (2.14), expressing the quality factor of a capacitor and inductor, respectively.

$$Q_C = \frac{X_C}{R_C} = \frac{1}{j\omega R_p C} \tag{2.13}$$

$$Q_L = \frac{X_L}{R_L} = \frac{j\omega L}{R_p} \tag{2.14}$$

When designing high-Q circuits, such as resonant circuits, each component's quality factor must be maximized. Additionally, from the equations above quality factor is frequency dependent. Typically, as frequency increases, quality factor will decrease due to the resistive losses increasing, however this behavior is application dependent.

Inductor and capacitor models introduce shunt capacitance and parasitic ESL, respectively. These reactive parasitics introduce a self-resonant frequency, also seen in the varactor diode. In an inductor, the parasitic capacitance dominates at high frequencies (above the SRF) and the component becomes an equivalent capacitor. In a capacitor, the parasitic inductance dominates at high frequencies (above the SRF) and the component becomes an equivalent inductor. Hence capacitors and inductors must operate at frequencies below SRF, especially critical in microwave systems.

This theory also explains why multiple valued, parallel capacitors are used for power line noise decoupling. Lower valued capacitors typically have less parasitic inductance and hence a higher SRF. Using several decreased-valued capacitors in parallel increases the overall SRF.

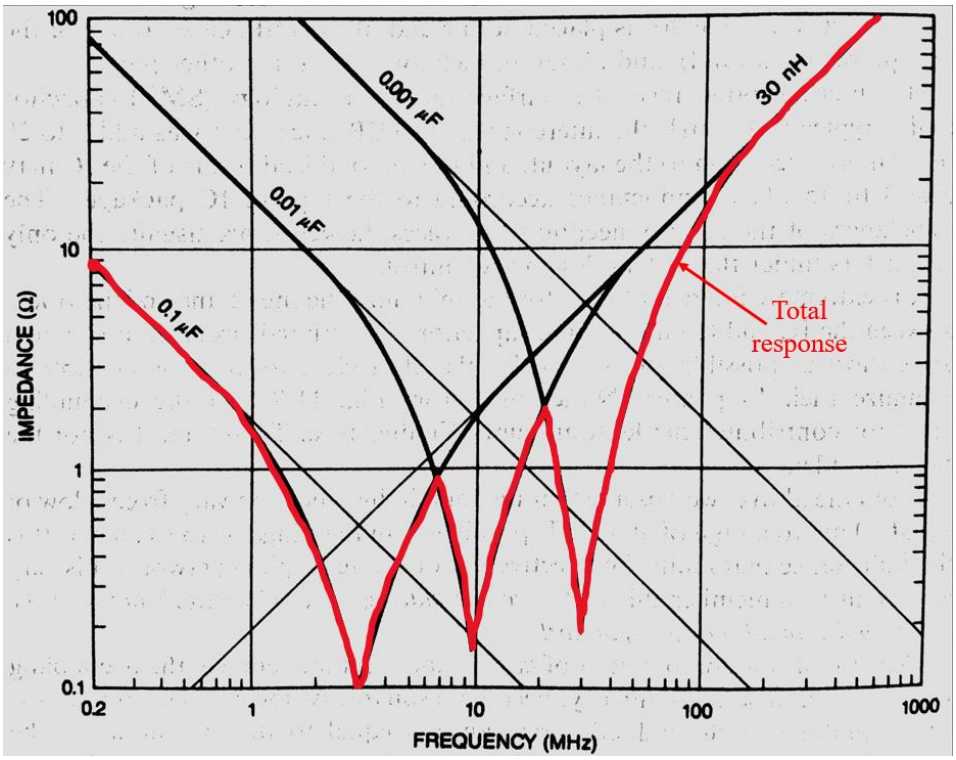


Figure 2.12: Impedance Frequency Response, Multiple Value Decoupling Capacitors [20]

Figure 2.12 above defines the impedance frequency response of 0.1 μF, 0.01 μF, and 0.001 μF capacitors in a stacked, parallel decoupling architecture. In each individual capacitor's impedance curve, the impedance increases above the SRF due to parasitic inductance. Decreasing capacitance increases the SRF. The impedance frequency response for three parallel capacitors is the red curve in Figure 2.12, with increased bandwidth over a single 0.1 μF capacitor.

Chapter 3

SCHEMATIC CIRCUIT DESIGN AND SIMULATION

The cross-coupled, differential LC oscillator VCO architecture optimizes RF performance, described in Section 2.1. Figure 3.1 defines the full VCO design's block diagram. It features SiliconGermanium:Carbon (SiGe:C) NPN Heterojunction Bipolar Transistors (HBTs) by *Infineon Technologies*. Infineon provides a Keysight Advanced Design System (ADS) project design kit (PDK) with nonlinear transistor models to accurately analyze and simulate available HBTs. The selected transistor is the BFR740L3RH, featuring a high transition frequency (f_T), a low noise profile, and high maximum power gain further described in Section 3.2. Additionally, full schematic design, simulation, and optimization is presented in this chapter.

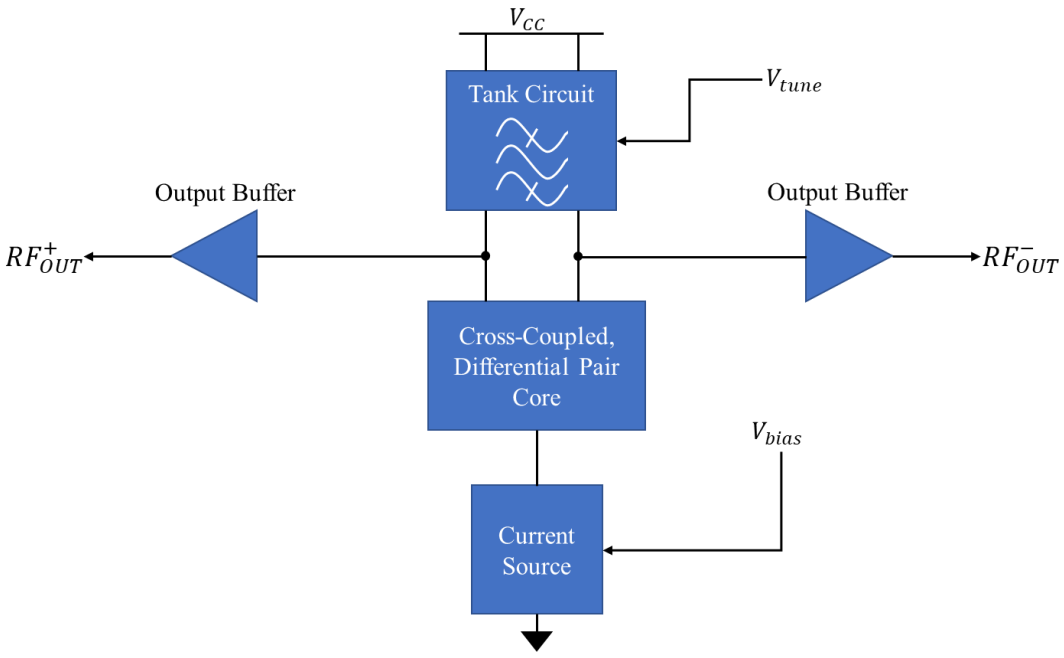


Figure 3.1: Full VCO Block Diagram

3.1 Cross-Coupled, Differential VCO Architecture and Operation

This common circuit topology includes optimized harmonic suppression, output power, phase noise capabilities, and negative resistance realization [8, 21]. The differential outputs suppress even harmonics, doubles signal amplitude, and minimizes phase noise [8]. This circuit also exhibits negative resistance through the cross-coupled differential pair, described below and similarly derived in [21].

Figure 3.2 below defines the cross-coupled, differential oscillator AC equivalent circuit model. DC bias nodes at the tank circuit inductors and HBT emitters are AC grounds. Additionally, the interconnection between the tank circuit capacitors is a common, virtual ground due to the symmetric, differential architecture.

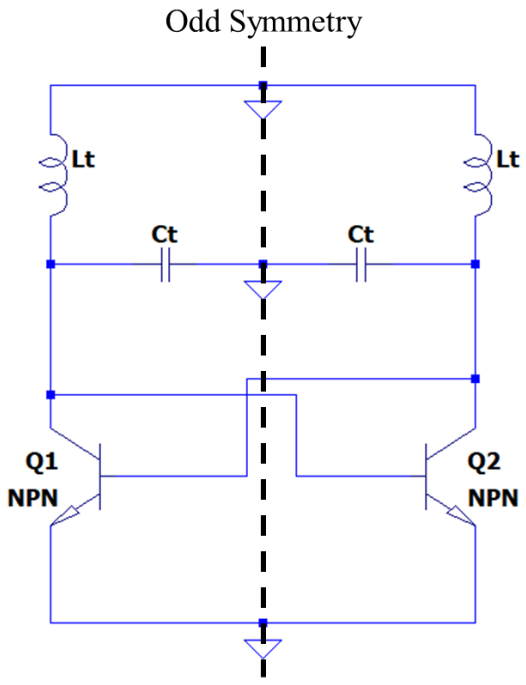


Figure 3.2: Cross-Coupled, Differential Oscillator AC Equivalent Circuit Model

Similar to a traditional bipolar junction transistor (BJT), the HBT has parasitic capacitance at the collector-base, base-emitter, and collector-emitter junctions. These parasitic capacitances are modeled in the small-signal circuit model of Figure 3.3 as C_{CB}, C_{BE}, and C_{CE}, respectively. R_p represents the tank circuit's loss resistance. Since both transistors are matched, all HBT parameters are identical (same parasitics and transconductances). Also, the HBT's dynamic input resistance, r_π, can be neglected as it is relatively large compared to the negative input resistance magnitude, therefore the parallel equivalent is approximately R_{IN}.

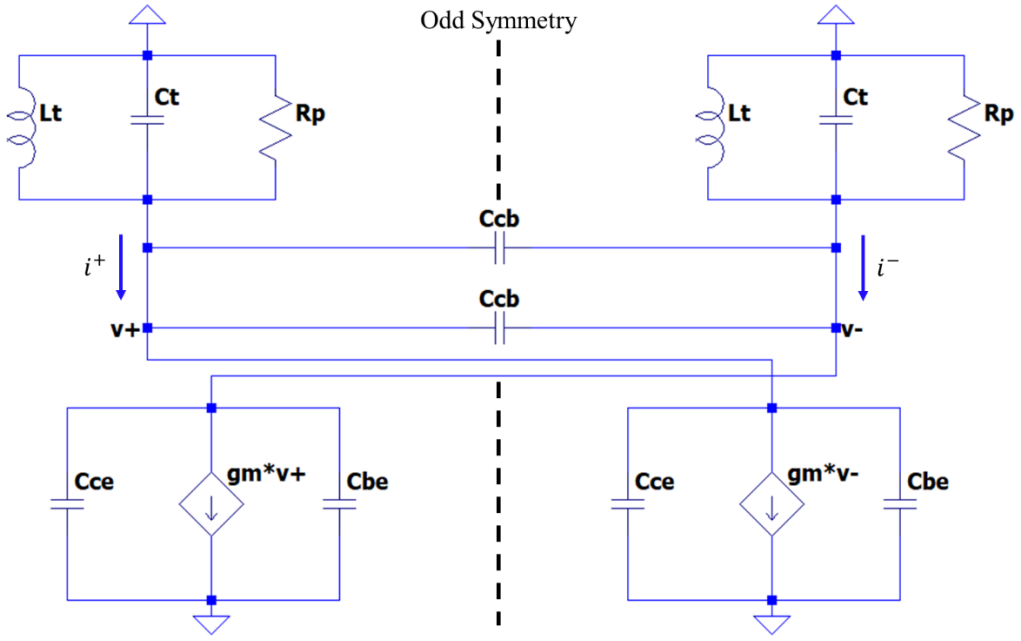


Figure 3.3: AC Small-Signal Equivalent Circuit Model of Figure 3.2

The, v^+ and v^- nodes denote the positive and negative differential oscillator output voltages between the resonant tank and differential core. Both C_{CB} capacitances are across v^+ and v^-, since the collector and base terminals are cross-coupled, therefore C_{CB} effectively interconnects both collector terminals and is added to the resonant tank

equivalence, shown in Figure 3.4. Note, the oscillator output voltages are also the effective input signals to each HBT due to the cross-coupled, feedback network, shown in Figure 3.4.

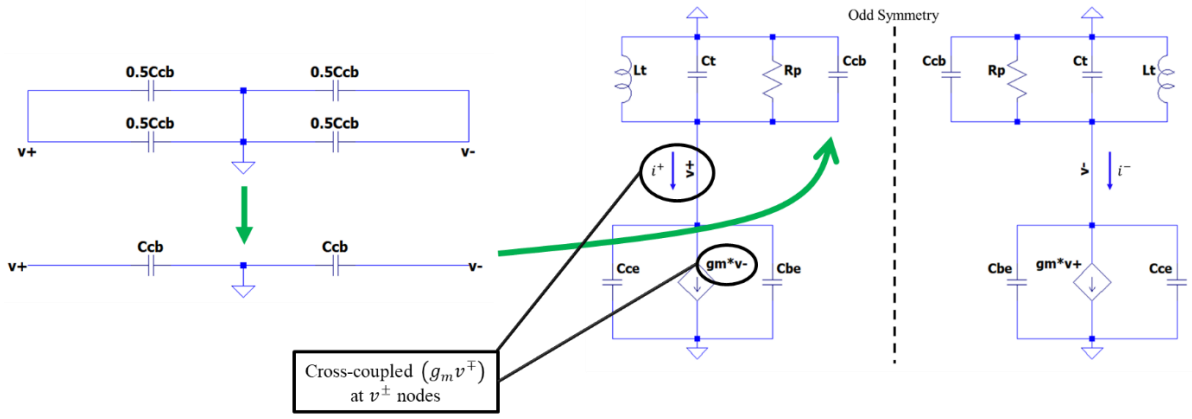


Figure 3.4: C_{CB} Simplification and Cross-Coupled $v^{\pm}$ Interconnection

Figure 3.5 below defines the simplified cross-coupled, differential oscillator small-signal equivalent circuit. The individual collector-base capacitances have been added to each tank circuit as they are already in a differential orientation about the odd symmetric common ground. The dotted black vertical line of Figure 3.5 defines the odd-symmetry differential pair virtual ground – both sides of the differential pair are effectively the same circuit network due to the matched transistors.

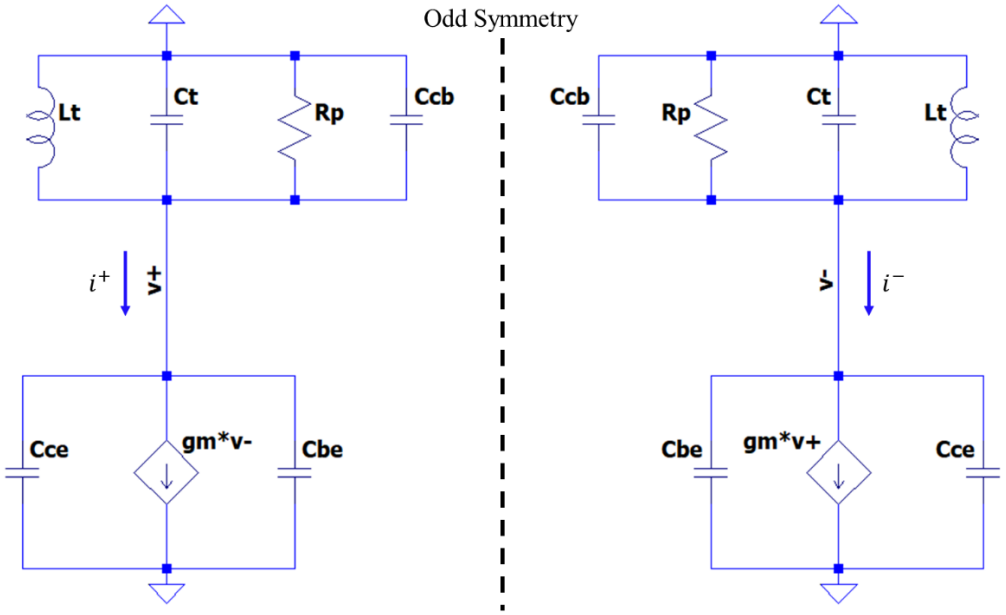


Figure 3.5: Simplified Small-Signal Model of Figure 3.3

To show the negative input resistance behavior of this circuit, the input admittance, Y_{IN}, of the differential core is analyzed, Figure 3.6.

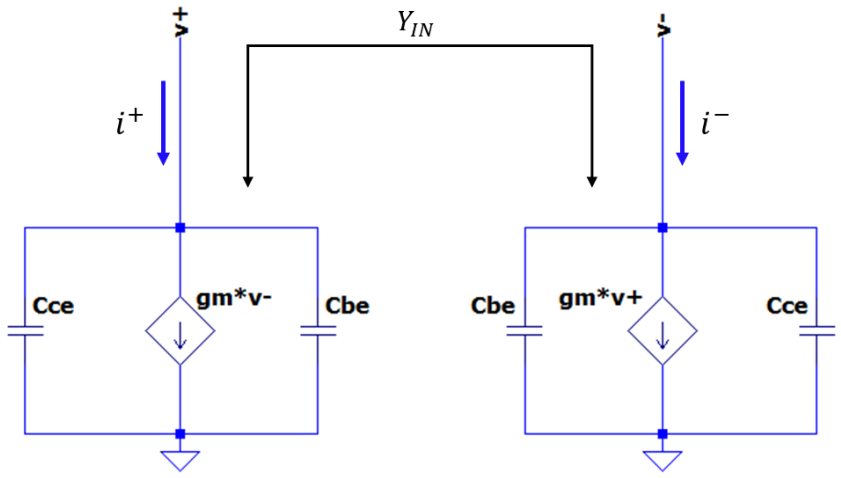


Figure 3.6: Equivalent Input Impedance of Cross-Coupled, Differential Pair Core

Input admittance is evaluated opposed to impedance since the differential pair is a parallel network symmetric about a center virtual ground. Input admittance of the differential network is defined below in equation (3.1); each current is summed in equations (3.2) and (3.3). Note, the $(g_m\, v^{\pm})$ terms are cross-coupled.

$$Y_{IN} = \frac{i_{diff}}{v_{diff}} = \frac{i^+ - i^-}{v^+ - v^-} = G_{IN} + jB_{IN} \tag{3.1}$$

$$i^+ = j\omega C_{CE}\, v^+ + j\omega C_{BE}\, v^+ + g_m\, v^- \tag{3.2}$$

$$i^- = j\omega C_{CE}\, v^- + j\omega C_{BE}\, v^- + g_m\, v^+ \tag{3.3}$$

The difference between each current results in equation (3.4).

$$i^+ - i^- = j\omega(C_{CE} + C_{BE})(v^+ - v^-) - g_m(v^+ - v^-) \tag{3.4}$$

Substituting the differential current back into equation (3.1), the input admittance is

$$\begin{aligned} Y_{IN} &= \frac{i^+ - i^-}{v^+ - v^-} = \frac{j\omega(C_{CE} + C_{BE})(v^+ - v^-) - g_m(v^+ - v^-)}{(v^+ - v^-)} \\ &= -g_m + j\omega(C_{CE} + C_{BE}) \end{aligned} \tag{3.5}$$

From the above derivation it is clear the equivalent input conductance is negative, $G_{IN} = -g_m$. This is the "negative transconductance" oscillator architecture. To initiate and sustain oscillations there must be a sufficient margin between the input conductance

magnitude and the parasitic tank conductance. This relation is similar to equation (2.7) but is written in terms of conductance, equation (3.7).

$$|G_{IN}| \geq 2\,|G_T| \tag{3.6}$$

The equivalent input susceptance is the sum of collector-emitter and base-emitter parasitic capacitance. Figure 3.7 shows the equivalent resonant tank circuit input impedance.

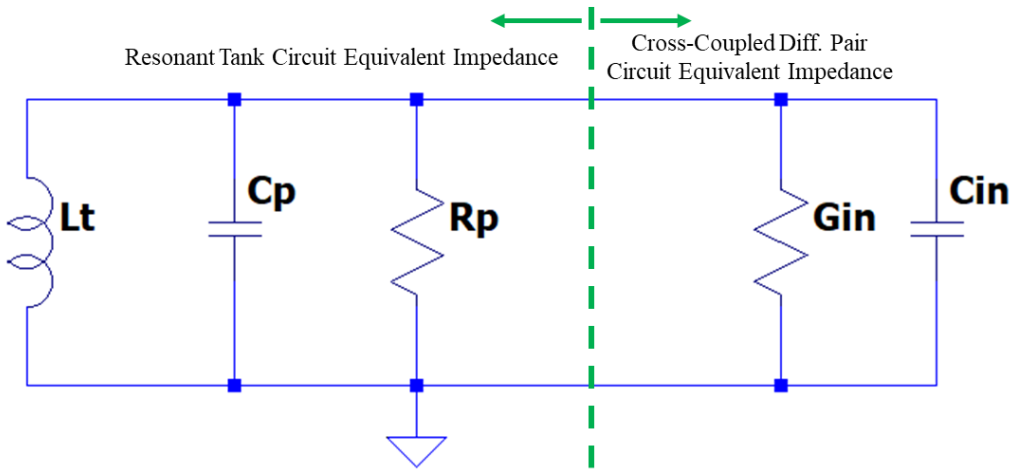


Figure 3.7: Unloaded Full VCO Equivalent Circuit Impedance Model

Figure 3.7 above defines the VCO equivalent circuit impedance model. The complete circuit is modeled as a parallel network of passive, lumped elements. Note the tank circuit's capacitance is now C_p, tank and collector-base capacitance, $(C_p = C_t + C_{CB})$. The VCO's oscillation frequency now becomes parasitic dependent, equation (3.7). This parasitic dependence is compensated by varactor diode capacitance tuning. Note, parasitic capacitance is relatively stable with bias voltage variations, quantified by VCO performance parameter, frequency pushing.

$$f_{o,unloaded} = \frac{1}{2\pi\sqrt{L(C_p + C_{IN})}} = \frac{1}{2\pi\sqrt{L(C_t + C_{CB} + C_{CE} + C_{BE})}} \quad (3.7)$$

Note equation (3.7) corresponds to an unloaded VCO. In the actual circuit, cross-coupled, differential pair, parasitic "loading capacitance" is in parallel with the output buffer's input. Therefore, this loading capacitance also affects the oscillation frequency. The final, loaded VCO oscillation frequency now becomes:

$$f_{o,loaded} = \frac{1}{2\pi\sqrt{L_{total}C_{total}}} = \frac{1}{2\pi\sqrt{L_{total}(C_t + C_{CB} + C_{CE} + C_{BE} + C_{load})}} \quad (3.8)$$

Note, L_{total} represents the equivalent circuit total inductance. Later sections describing VCO circuit layout include parasitic inductance introduced. Therefore, L_{total} serves as an interim placeholder for the circuit's total inductance.

3.2 Transistor Selection and ADS Characterization

The selected transistor is the BFR740L3RH (BFR) by *Infineon technologies*. This discrete component is a Silicon-Germanium:Carbon (SiGe:C) Heterojunction Bipolar Transistor (HBT) device. HBT's offer an increased frequency response while maintaining considerable transistor gain and low noise capabilities (reference Appendix A). The BFR is selected due to its high transition frequency, f_T, of 42 GHz, low 0.5 dB NF_{min}, and high maximum power gain of 20 dB at 5.5 GHz [22]. Additionally, an ADS non-linear transistor model is available for design and simulation.

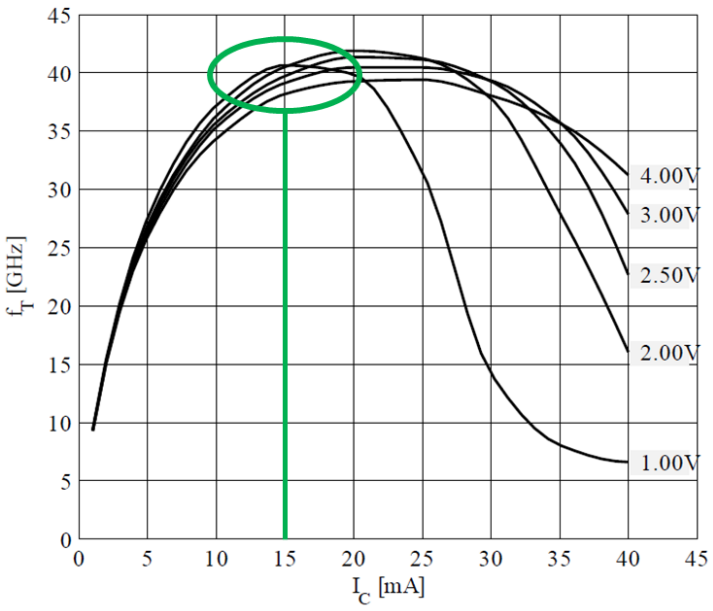


Figure 3.8: Transition Frequency $f_T = f(I_C)$, $f = 2$ GHz, V_{CE} = [1, 2, 2.5, 3, 4] V [22]

Figure 3.8 above defines the transition frequency vs. collector bias current. An initial collector current of 15 mA is selected to maximize f_T while minimizing power consumption. To characterize the BFR at the selected bias level, a Scattering Parameter

(S-Parameter) simulation is performed on the non-linear ADS transistor model, Figure 3.9.

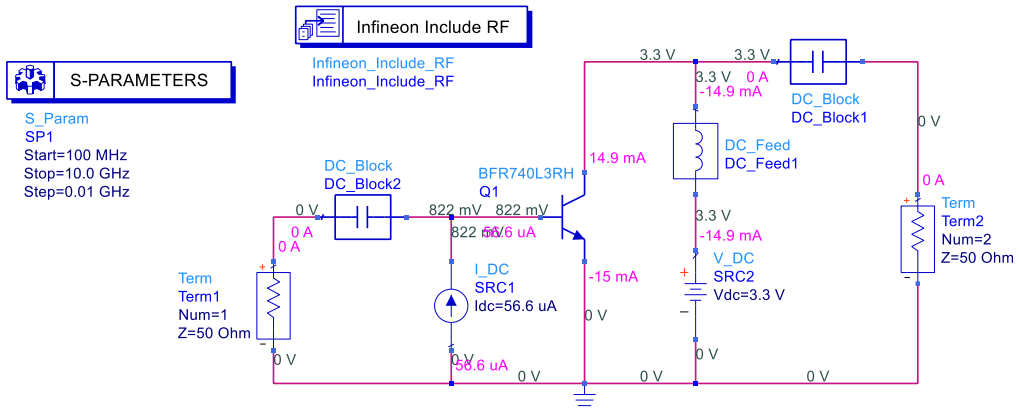


Figure 3.9: BFR740L3RH Transistor Characterization ADS Schematic

Note, the 15 mA collector current bias corresponds to ≈57 μA base current. These current bias conditions are set with an ideal current source while an ideal voltage source sets the collector-emitter voltage to 3.3 V, per initial voltage design specifications. DC blocks and feeds (ideal AC coupling capacitors and RF chokes, respectively) define DC and RF signal paths. An S-Parameter simulation is executed using the S-Param ADS block with two 50 Ω terminations.

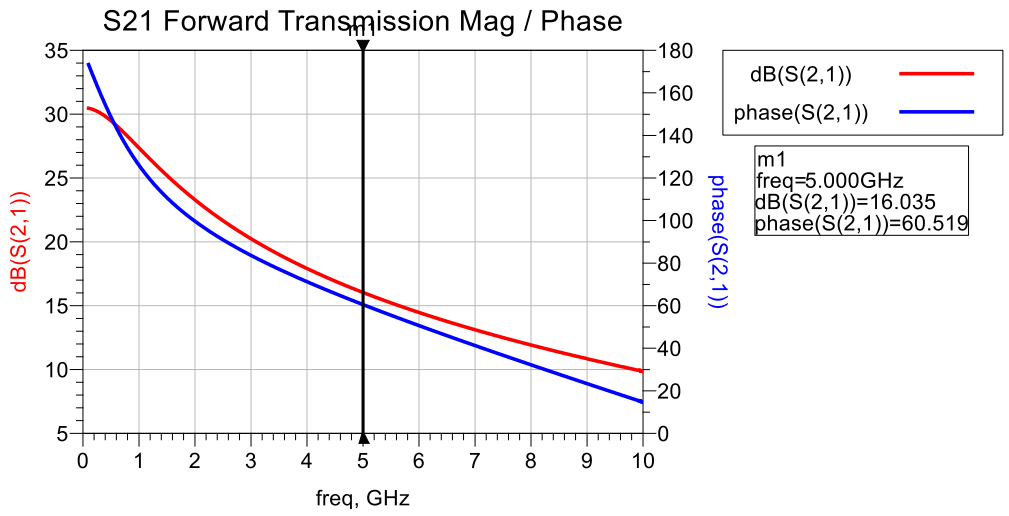


Figure 3.10: BFR740L3RH Transistor Forward Transmission

Figure 3.10 above defines the HBT forward transmission, or gain. As expected, gain decreases as frequency increases. Ideally, the forward phase shift should remain at 180° for all frequencies in the inverting, common emitter (CE) topology. However, high frequency parasitics and the Miller effect reduce the forward transmission phase shift as frequency increases. At 5 GHz, a 16 dB gain is simulated with 60.5° phase shift. Figure 3.11 below simulates the input return loss. The return loss curve rotates clockwise and decreases in impedance (≈10 Ω at 5 GHz) as frequency increases.

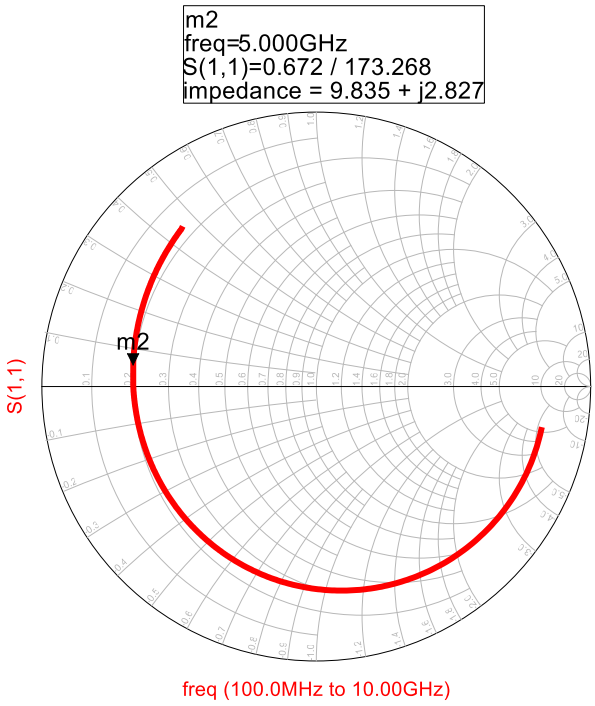


Figure 3.11: BFR740L3RH Transistor Input Return Loss

3.3 Cross-Coupled, Differential VCO Core Design

The VCO core cross-coupled differential pair orientation connects the Q1/Q2 collector to the Q2/Q1 base. These connections direct DC collector currents into each HBT base terminal. However, these milliamp-scale DC currents overpower HBTs, resulting in transistor damage. To prevent this, AC coupling capacitors are placed in the cross-coupled feedback paths to block DC collector current from entering the base terminals, C4 and C5 in Figure 3.12. The differential pair common emitter tail node connects to a current source feeding the collector bias currents. The differential pair collector nodes are the VCO outputs and the junction between the core, tank circuit, and load (output buffer). The remainder of this section analyzes the cross-coupled, differential pair VCO core.

3.3.1 Cross-Coupled Differential Pair Parasitics Characterization

A voltage-controlled oscillator design includes parasitic conductance and capacitance, which affects oscillation frequency. The capacitance is approximated using datasheet values. However, datasheet values are not stated at microwave frequencies such as 4 to 5 GHz. To characterize the parasitic capacitance at these frequencies, ADS simulations calculate the equivalent Y_{IN}, which is converted to capacitance. Figure 3.12 below defines the ADS schematic. The termination is placed across the differential output nodes to enable input admittance calculations. Incorporating the initial designed current sink yields a more accurate model (current sink design discussed in Section 3.4). C4 and C5 are AC coupling capacitors, blocking the 15 mA DC collector current from the base terminals. For an initial calculation, ideal current sources bias the cross-coupled pair base nodes with $\approx 57\ \mu$A.

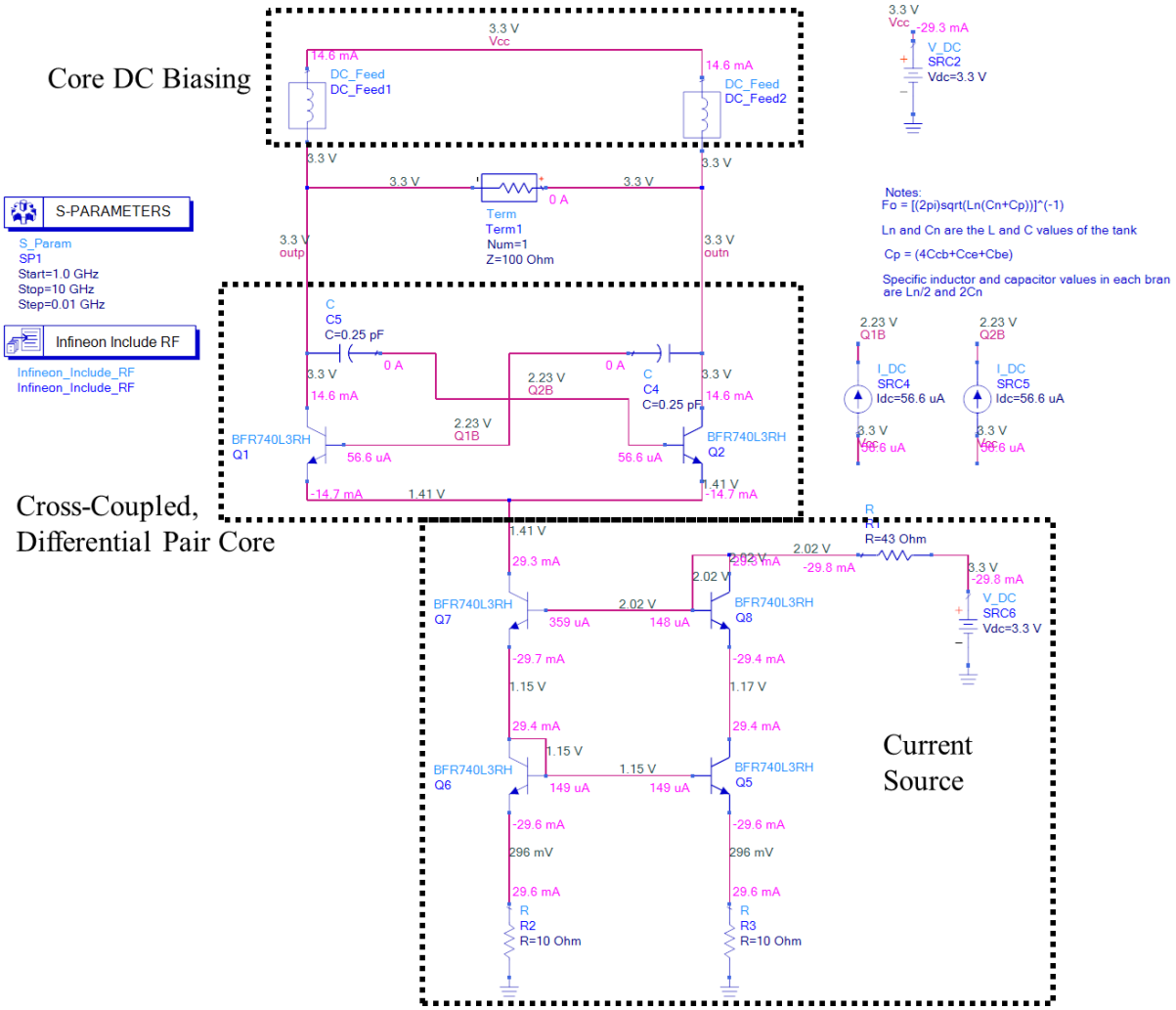


Figure 3.12: Cross-Coupled, Differential Pair Parasitic Characterization

Figure 3.13 below defines the simulated core input admittance. The negative conductance oscillation condition is confirmed through this simulation. Note a negative conductance (or resistance) represents a reflection coefficient magnitude greater than one. Additionally, the positive susceptance represents a capacitance since $Y_{Cap} = jB_{Cap} = j\omega C$ (positive ωC value).

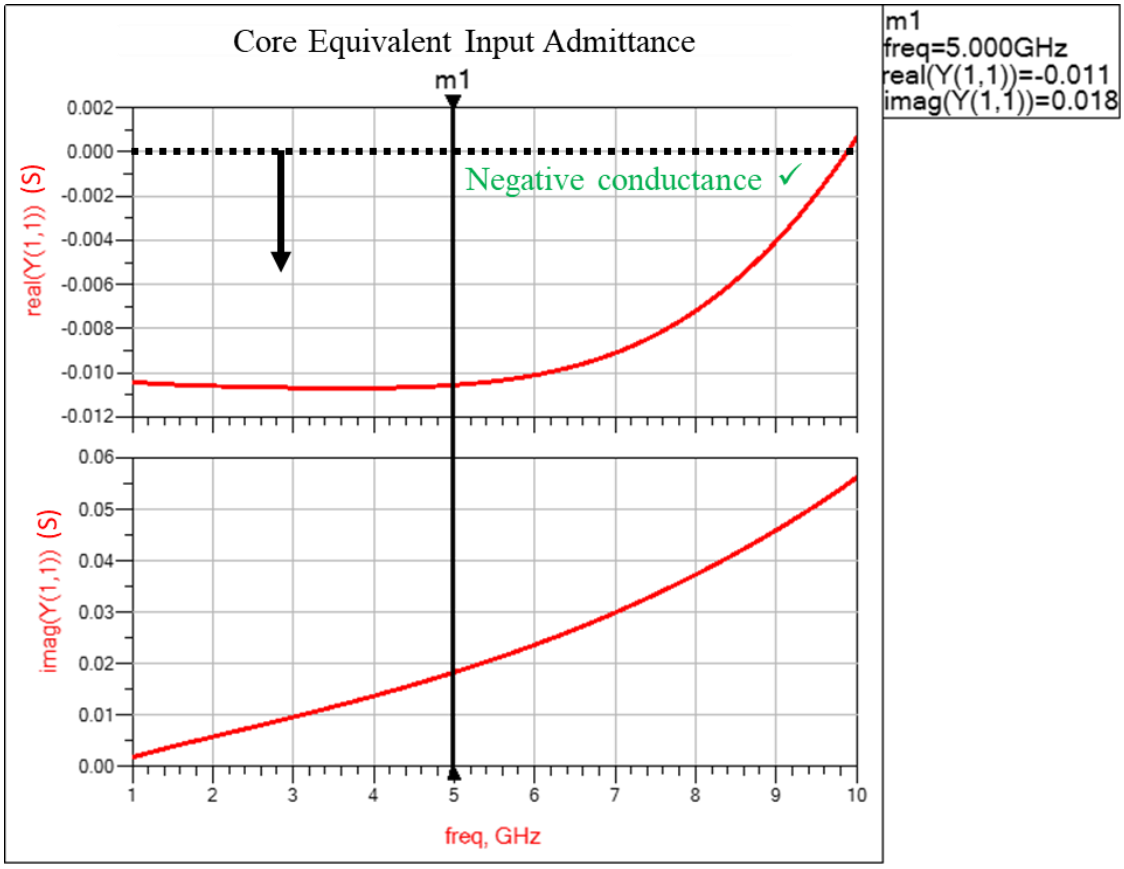


Figure 3.13: Cross-Coupled Pair Equivalent Parasitic Conductance (S) and Susceptance (S)

Figure 3.14 below defines the corresponding core equivalent parasitic capacitance. From 5 to 8 GHz, a 0.58 to 0.74 pF parasitic capacitance is calculated, ≈ 0.5 pF is calculated at 3 GHz. These values quantify the parasitic effect on the VCO's oscillation frequency.

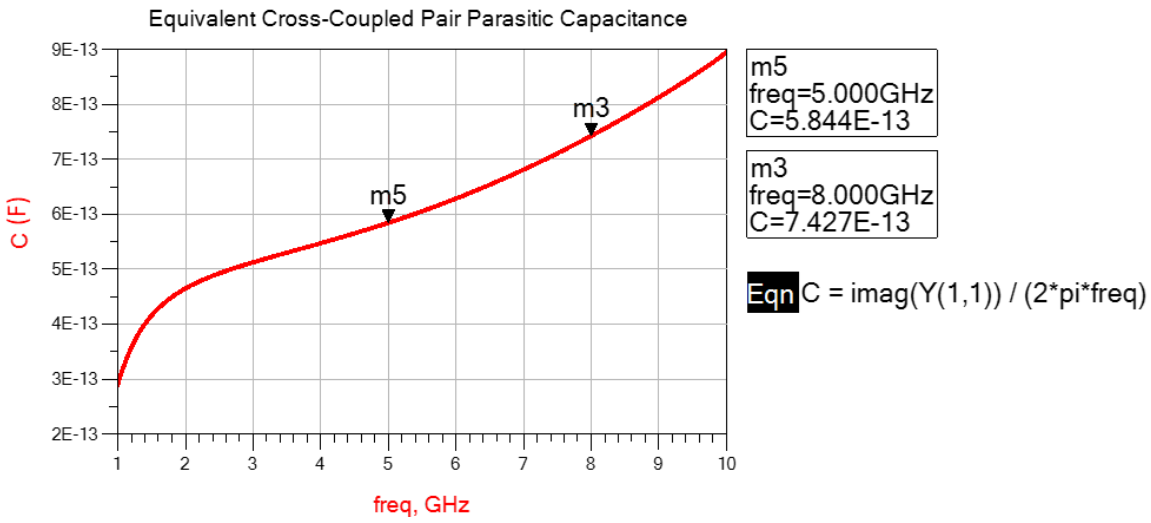


Figure 3.14: Cross-Coupled Pair Equivalent Parasitic Capacitance

3.3.2 Core Base Bias Network

The cross-coupled pair base terminal DC bias networks use a resistive divider. High impedance resistors approximate RF chokes feeding the base terminals with DC bias current. Resistors are used as opposed to inductors or traditional RF choke components due to compact SMT packages and decreased parasitics. An RF choke equivalent circuit model includes inductance, equivalent series resistance (ESR), and shunt capacitance, similar to an inductor's equivalent circuit model. As described in Section 2.6, this parallel capacitance creates a self-resonance frequency within the inductor, leading to circuit instabilities and RF leakage through the choke.

In contrast to RF chokes, resistor packages have minimal parasitics and are typically neglected. Large resistor values provide a high-impedance to attenuate or 'choke' RF that may flow into the bias network, while allowing low-magnitude bias currents into the HBTs. Although resistors are lossy, minimal current (microamp-scale)

flows through these large-valued components (kilohm-scale), therefore power dissipation is minimized.

Figure 3.15 below defines the base bias circuit. R1 and R2 directly set the voltage level at the R1-R2-RFC common node, and consequently the HBT base current through the RFCs.

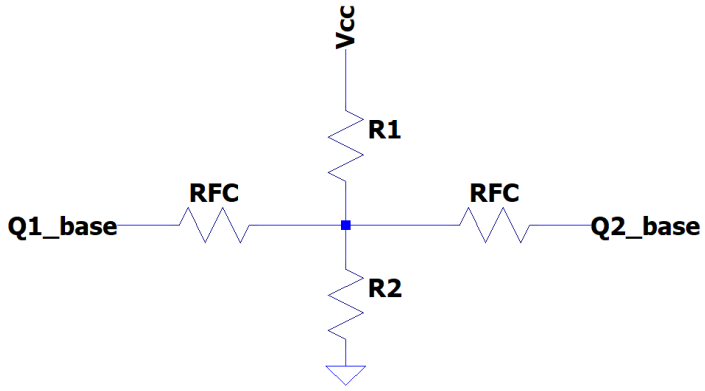


Figure 3.15: Core HBT Base Bias Network Model

If the RFC value is considerably larger than R2, the parallel combination of RFC and R2 is R2. This simplifies the derivation to a voltage divider, shown in Equation(3.9); V_A denotes the R1-R2-RFC common node voltage.

$$V_{Qn,base} \approx V_A \approx V_{CC} \frac{R_2}{R_1 + R_2} \tag{3.9}$$

Note that R1 and R2 are set to large-valued (kilohm-scale) resistors to minimize network power consumption. The specific resistor values are set once the full VCO is integrated.

3.5 Current Source

3.5.1 Initial Current Sink Design

The initial current source architecture chosen is the Full-Wilson Current Mirror [23]. This topology features four HBTs, optimizing the loading/output impedance and current setting capabilities. The bias current is set with R1 in Figure 3.16, derived via equation (3.10).

$$R_{Bias} = \frac{V_{CC} - (I_C R_E + V_{BE} + V_{BE})}{I_C} \tag{3.10}$$

V_{CC}, I_C, and R_E are user-defined while V_{BE} is from the datasheet [22]. This architecture features a high output impedance at the Q7 collector node, minimizing differential pair common emitter loading effects, Figure 3.16. Additionally, the transistor pair equalizes the Q5 and Q6 collector voltages, eliminating base and collector current mismatches between the two vertical HBT branches [23]. This further ensures a stable unity current gain between the two branches. Figure 3.16 below defines the initial current sink design with the DC operating points and bias conditions.

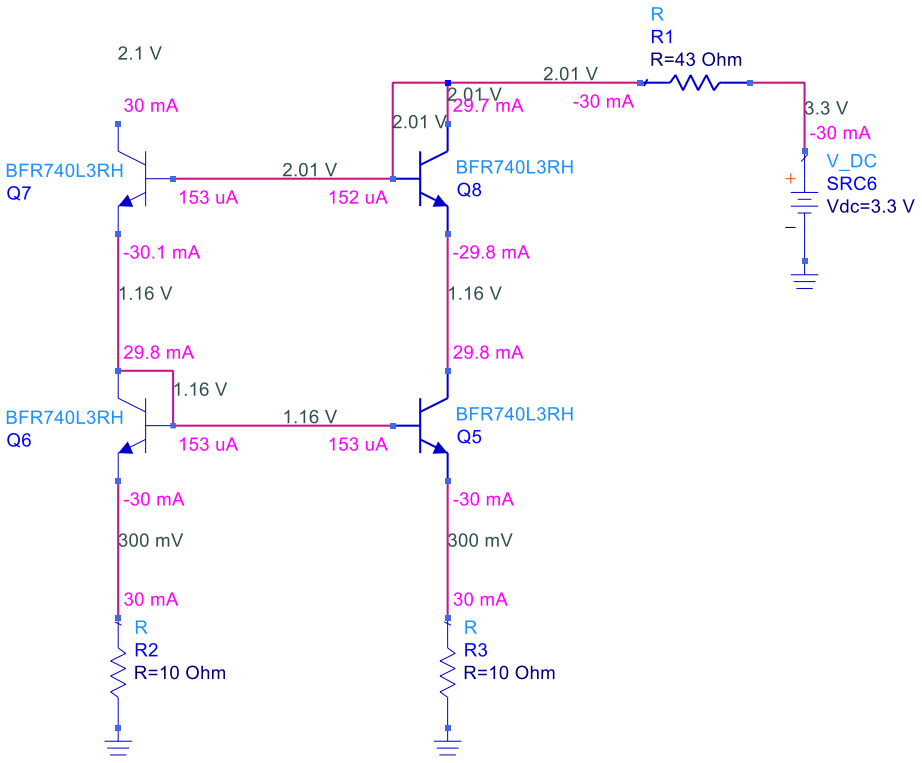


Figure 3.16: Initial Full Wilson Current Mirror Design

3.5.2 Final Current Sink Design

After further analysis a new, lower-power current sink architecture is realized, decreasing the overall current consumption by one-half. Instead of a classic current mirror topology, a single transistor configuration is used to implement the current source. The current source collector current is set by the base bias current, which is set by a resistive divider. The base bias current is set to $\approx 47\ \mu$A to yield 12 mA collector current. This feeds the cross-coupled pair and equals the differential pair emitter tail current. Note the final 12 mA tail current is less than half of the initial 30 mA shown in Figure 3.16 and is further discussed in Section 3.7. Figure 3.17 defines this updated schematic design.

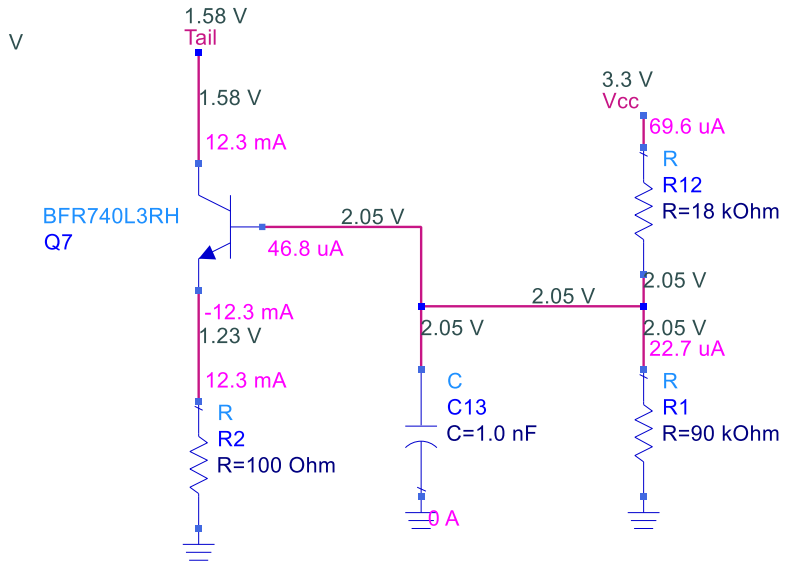


Figure 3.17: Final Single-Transistor Current Source Circuit

The tail current is controlled by the injected Q7 base current (I_B) and voltage (V_B), set by the R1 and R12 voltage divider, shown in Figure 3.17 and equation (3.11).

$$V_B = V_{CC}\frac{R_1}{R_1 + R_{12}} \tag{3.11}$$

C13 serves as a de-coupling capacitor to suppress noise through the external DC voltage source. Additionally, the degenerative emitter resistor R2 increases the HBT's collector output impedance (current source equivalent output impedance) [23].

The motivation behind this design modification is to decrease current consumption. In a traditional current mirror, half the supply current is unused to set the load current of the current sink – wasting power. In an IC design this issue is handled by varying the physical HBT emitter widths. In IC design, transistor emitter width defines current handling capabilities. By decreasing the transistor's bias-side to load-side emitter

widths, a current gain is created. Increasing this current gain while maintaining the load-side branch current reduces current flow through the bias-side, minimizing overall power consumption. However, when using discrete components, varying the transistor's emitter width is not a design option. By modifying the circuit to a single transistor architecture, the current source power consumption is greatly minimized while still providing the required VCO tail current.

3.6 Tank Circuit

The tank circuit, the VCO's frequency selecting circuit, includes fixed inductors, capacitors, and varactor diodes. Implementing a parallel fixed capacitor bank reduces the required varactor tuning range. This also benefits the overall quality factor as wide-range varactor diodes typically have lower quality factors.

3.6.1 Inductor Implementation

To design inductors at microwave frequencies, transmission line-based approaches are typically utilized. One design approach uses microstrip series transmission lines as inductors. As described in Section 2.5, conductive transmission lines have equivalent series inductance, where line length is proportional to inductance. This phenomenon is utilized to create low-value, high-Q, inductors for resonant circuits. Although general design equations approximate inductor transmission lines, ADS simulations more accurately model the line's inductance. S-parameter simulations are run, and Y-parameters are extracted. From the Y-parameters, the equivalent inductance,

resistance, and associated quality factor are extracted. Y-Parameters are used opposed to Z-parameters since they accurately model and account for high-frequency shunt parasitic capacitance [24].

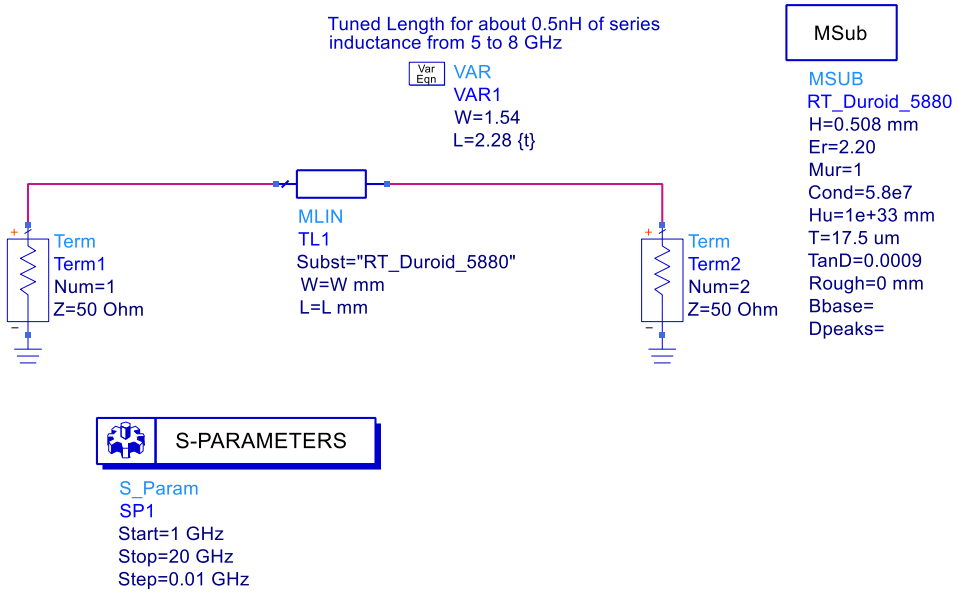


Figure 3.18: Microstrip Line Inductor ADS Schematic Characterization

Note the microstrip substrate definition (MSub) shown in Figure 3.18. The Rogers Corporation 5880 RT/Duroid laminate is initially characterized. The associated dielectric substrate height is set to 0.5 mm, or about 20 mils. This material features an extremely low 0.0009 dissipation factor and 2.2 dielectric constant.

Figure 3.19 below highlights the equivalent inductance, resistance, and associated quality factor. The susceptance of an inductor is $Y_L = jB_L = \frac{1}{j\omega L} = -\frac{j}{\omega L}$. At 5 GHz, about 0.5 nH and 0.024 Ω are calculated corresponding to approximately a 667 quality factor.

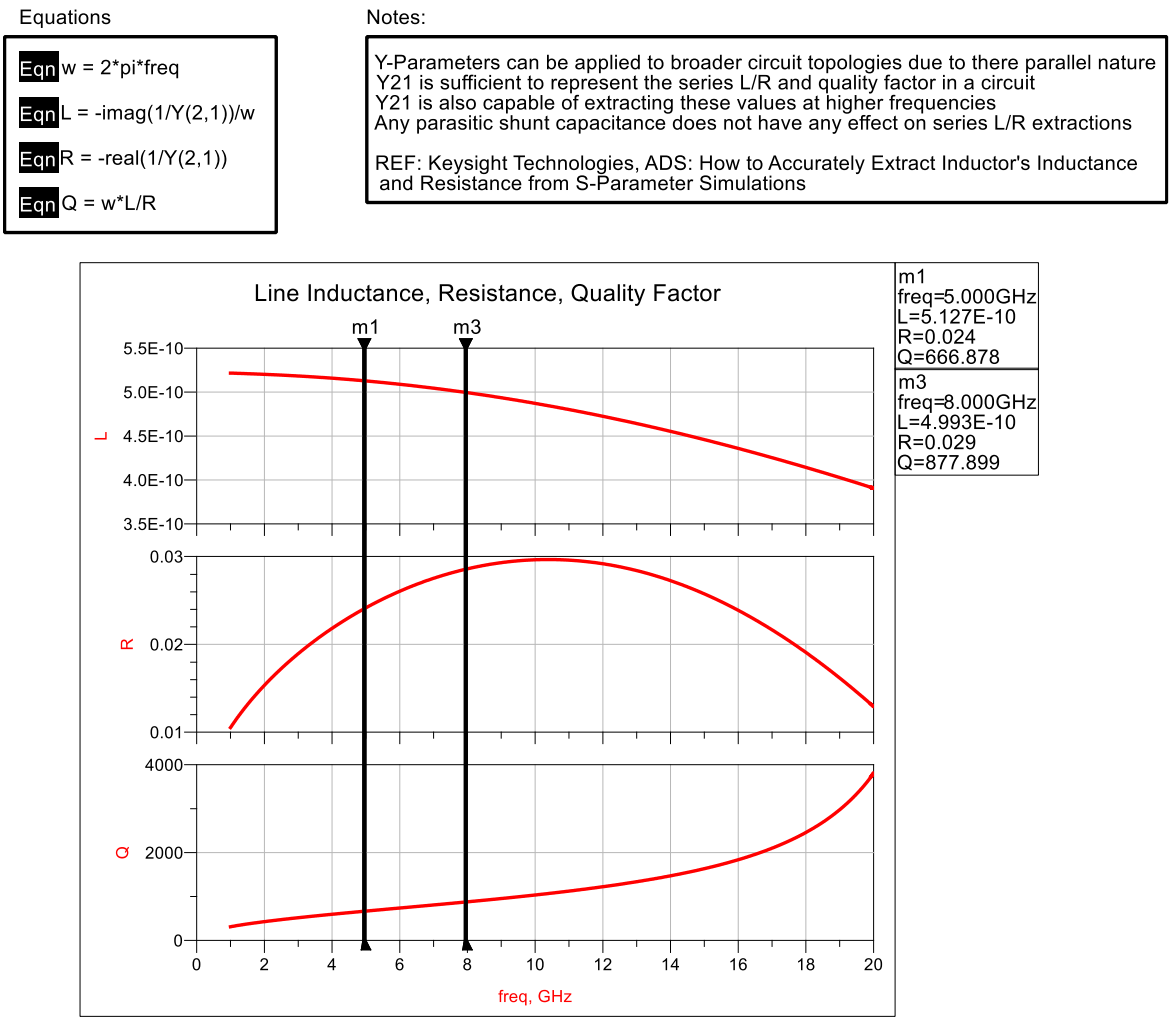


Figure 3.19: ADS Simulation MLine Inductor: Inductance (H), Parasitic Resistance (Ω), Quality Factor

Although the described approach presents a low-loss, high-Q inductor, once this microstrip line is implemented in the PCB layout, considerable parasitics are introduced. These losses significantly degrade quality factor and introduce a self-resonance. Although using distributed elements, such as microstrip transmission lines, minimizes inductance, they lack tuning flexibility for future design optimization. For example, if future design optimization requires an inductance-value change, the microstrip line must be re-routed. In contrast, if a discrete SMT component is used, the part can be replaced

with the new required inductance value. This approach is implemented for this VCO design.

Discrete SMT inductors are used to realize the fixed inductors in the tank circuit. *Kyocera AVX* designs thin-film RF/Microwave Inductors in SMT packages. A 0.47 nH L0201 RF Inductor with $\pm$0.05 nH tolerance, a 32 GHz minimum SRF, and minimum quality factor of 30 at 2.4 GHz in a 0201 package [25]. Although this quality factor may seem relatively low, Q is frequency dependent and for an inductor, increases with frequency.

3.6.2 Fixed-Capacitor Bank

Reviewing Sections 2.2 and 2.6, two critical varactor diode considerations are equivalent series resistance (ESR) and equivalent series inductance (ESL). A varactor diode's quality factor is indirectly proportional to its ESR. Therefore, to maximize Q, ESR must be minimized. Additionally, a varactor's ESL decreases its self-resonant frequency, determining the reactive component (capacitance or inductance) dominating the equivalent impedance. For a varactor to operate as an expected capacitor, the operational frequency must be below the SRF.

There are effectively two ways to ensure this; operate the varactor at a lower capacitance to increase the SRF or decrease the ESL to increase the SRF. In many cases the ESL value is fixed as it is inherent to the device, therefore, to minimize ESL a specific varactor diode must be selected. However, these low-ESL varactors may not be available, nor affordable. Therefore, the alternative method of increasing the SRF is favorable, operating the varactor diode at a lower capacitance.

The equivalent capacitance of parallel capacitors is the sum of all capacitances. Therefore, varactor diodes are placed in parallel with a high-Q capacitor bank to decreases the required varactor capacitance, C_t. This increases the varactor's SRF and the resonant tank's overall quality factor.

This design's tank circuit requires 1.25 to 1.75 pF equivalent capacitance. However, available varactor diodes covering this range are costly, scarce, and lacking sufficient performance. Alternatively, a 0.75 pF high-Q, fixed capacitor bank is implemented, reducing the varactor diode requirement to a more affordable, abundant 0.5 to 1 pF tuning range.

Figure 3.20 below highlights an initial 0.5, 1, 2 pF capacitor bank ADS model. The top three parallel-C rows establish the fixed capacitor bank while the bottom row two capacitors model varactor diodes.

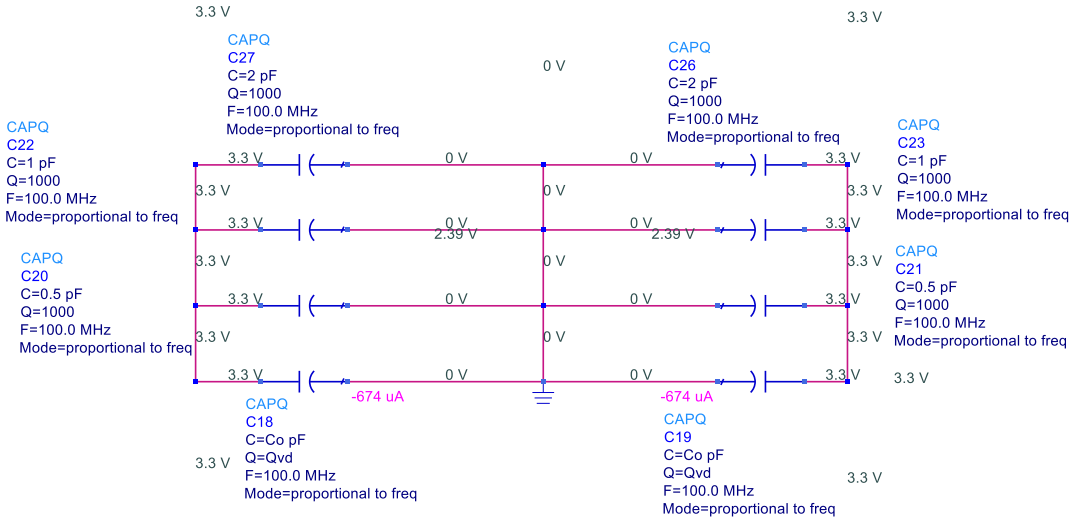


Figure 3.20: Initial Switch Capacitor Bank Model

More branches of fixed capacitors allow each capacitor to have a higher SRF and Q, but also increase frequency tuning resolution if switches are integrated at the bank's middle common ground node. These switches allow for different capacitive branches to be "toggled," shifting up or down the frequency response. Ultimately, a fixed bank composed of 0.25 pF and 0.5 pF capacitors is implemented for the final design.

3.6.3 Varactor Diode Selection

Four varactor diodes are compared in Table 3.1, sorted by minimum diode capacitance. They all have high quality factors (however, note varactor quality factor degrades as frequency increases). The SMV1231 presents the smallest achievable capacitance value of 0.47 pF at a reverse voltage of 15 V. Although the SMV1231 by *Skyworks Solutions* has the lowest L_S value, it also presents the greatest ESR, reducing quality factor. The Skyworks SMV1245 provides a minimum 1 pF with a 0.7 nH L_S, resulting in an approximately 6 GHz SRF. Though this is above the operational frequency range, a greater SRF margin is desired. Although the MAV2615 presents minimal ESR, the series inductance is not stated neither on the datasheet, nor the part website to estimate the device's SRF.

Table 3.1: Market Available Varactor Diodes

Parameter	**BBY53-02V [26]**	**SMV1245 [27]**	**MAV26V15 [28]**	**SMV1231 [29]**	**Units**
Manufacturer	Infineon Technologies	Skyworks Solutions	Panasonic Electronics	Skyworks Solutions	-
Minimum Diode Capacitance, $C_{d,min}$	2.4, $V_R = 3V$	1.0, $V_R = 12V$	0.7, $V_R = 12V$	0.47, $V_R = 15V$	pF
Maximum Diode Capacitance, $C_{d,max}$	8.5, $V_R = 0V$	7.5, $V_R = 0V$	10, $V_R = 0V$	2.35, $V_R = 0V$	pF
Series Resistance, R_S	0.47	1.6	0.45	1.50	Ω
Series Inductance, L_S	0.6	0.7	-	0.45	nH
Quality Factor, Q, Equ. (2.10)	63,892, $V_R = 1V$, 1MHz	16,240, $V_R = 1V$, 1MHz	58,946, $V_R = 1V$, 1MHz	455.4, $V_R = 3V$, 500MHz	-
SRF at $C_{d,min}$	4.2	6.0	-	11	GHz

The SMV1231 Hyperabrupt Junction Tuning Varactor by *Skyworks Solutions* is the best performing varactor diode. Its single SOD-882 package minimizes inductance L_S to 0.45 nH and 1.5 Ω series resistance, R_S, (at 500 MHz) resulting in a quality factor of 455. Additionally, this varactor diode's SRF is the greatest among all options, comfortably past this design's operating frequency range.

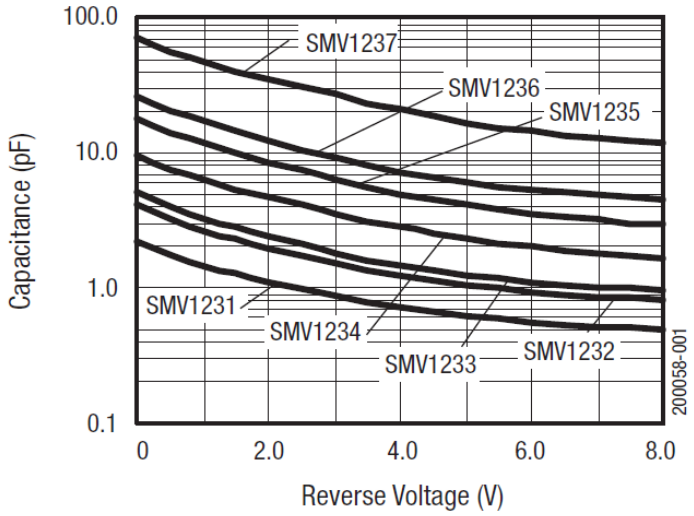


Figure 3.21: SMV1231 Capacitance vs Reverse Voltage [29]

Figure 3.21 above defines the SMV varactor series capacitance vs. reverse voltage characteristic. The SMV1231 curve is located at the bottom, providing the lowest variable capacitance. The decreased capacitance vs. voltage curve slope is due to the diode's hyperabrupt junction [30].

3.7 Full VCO Integration

ADS's S-Param and Harmonic Balance schematic simulators are used to test and optimize the VCO design. Scattering parameter simulations characterize and calculate the S-, Z-, and Y- parameters as a function of frequency. The Harmonic Balance (HB) simulator analyzes nonlinear circuits in both frequency- and time-domains [31].

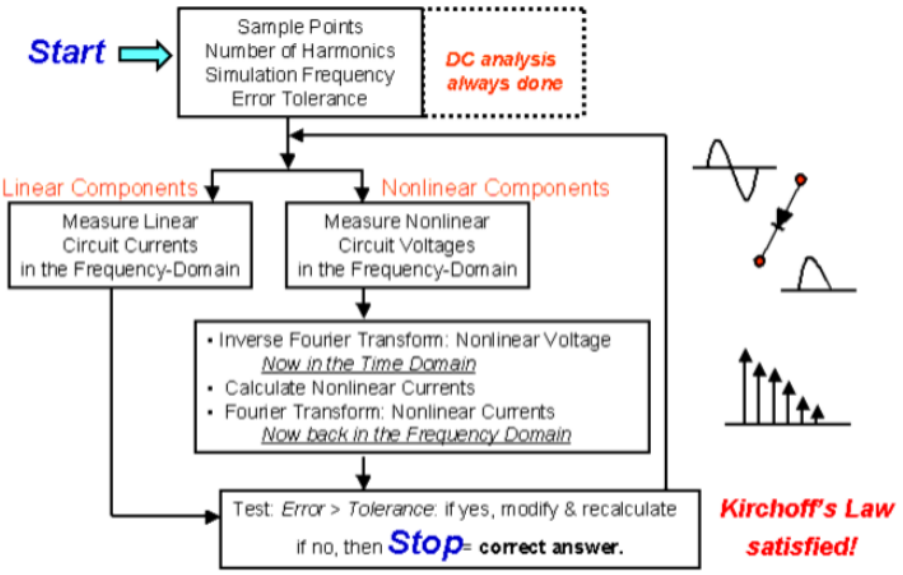


Figure 3.22: Harmonic Balance Simulation Flow Chart [31]

HB requires input frequencies and respective power levels, for nonlinear circuit simulation [31]. The HB simulator derives steady-state responses when analyzing nonlinear, microwave circuits, such as VCOs [31].

3.7.1 Initial Design and Performance

Figure 3.23 defines an initial full VCO schematic design. The base bias network and capacitor bank with varactor diodes are omitted to simplify simulations and increase processing efficiency.

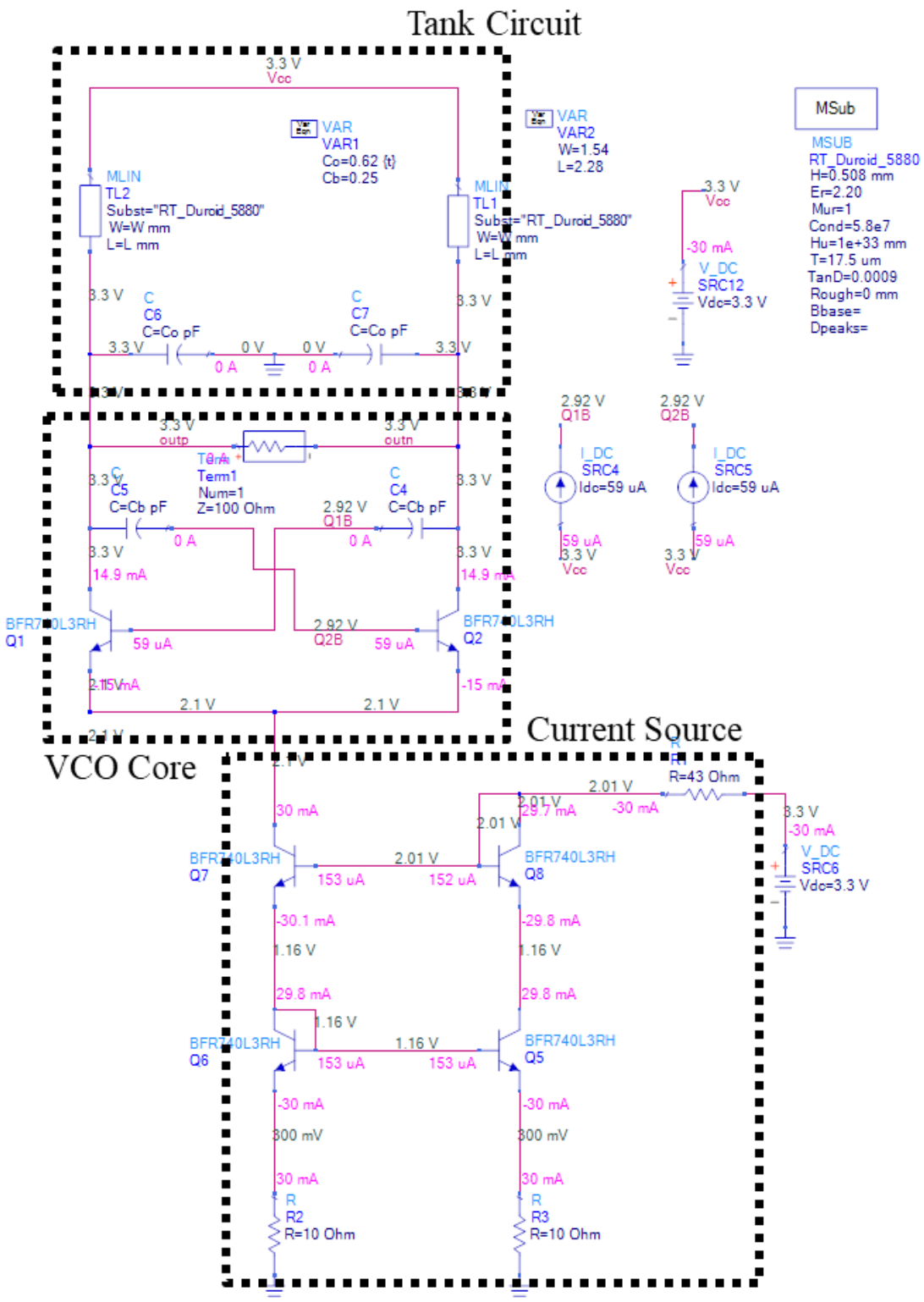


Figure 3.23: Initial Cross-Coupled, Differential VCO Design Schematic

The microstrip line inductors characterized in Section 3.6.1 are implemented in this initial design. The 0.62 pF fixed capacitor value, C_o in Figure 3.23, are tuned to yield a 5 GHz oscillation frequency.

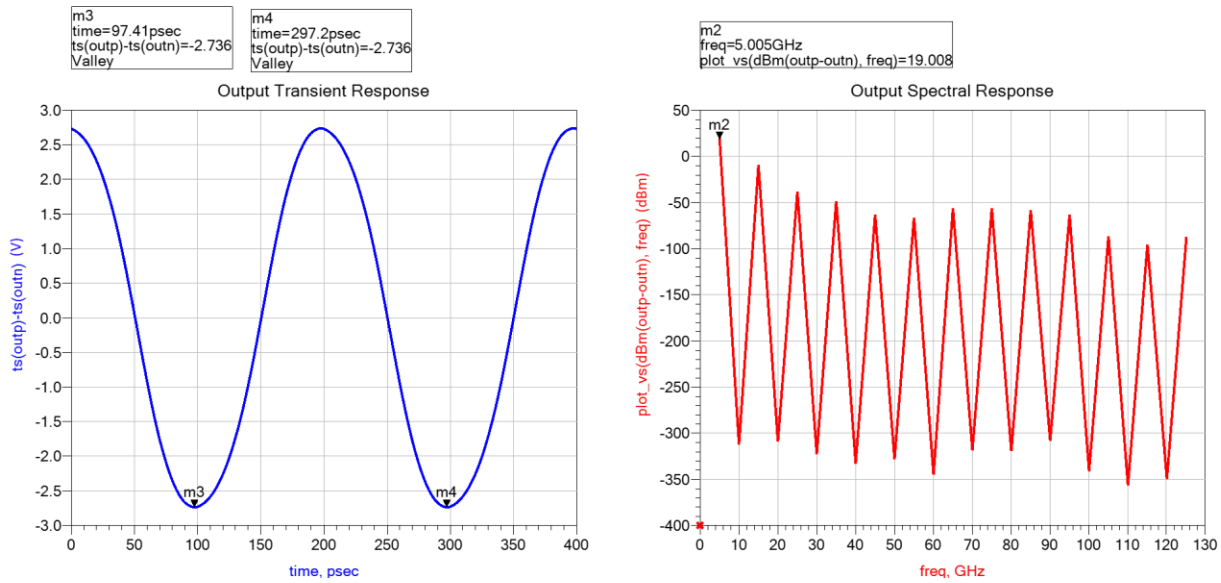


Figure 3.24: Initial Cross-Coupled, Differential Output VCO Transient (V_{pp}) and Spectral Response (dBm)

Figure 3.24 highlights the VCO schematic's open circuit, unloaded time and frequency domain simulated results. At the 5 GHz output tone, the unloaded differential output power is 19 dBm. The differential voltage swing (peak to peak voltage) is about 5.4 V, with a 2.7 V amplitude. With an initial 30 mA VCO with a 3.3 V supply, power consumption is 99 mW. The frequency response is discontinuous due to differential odd symmetry and discrete harmonic simulation. Figure 3.25 below defines the single-ended output, single-sideband phase noise response as a function of offset frequency. The 5 GHz carrier frequency is the same as shown in Figure 3.24 simulations.

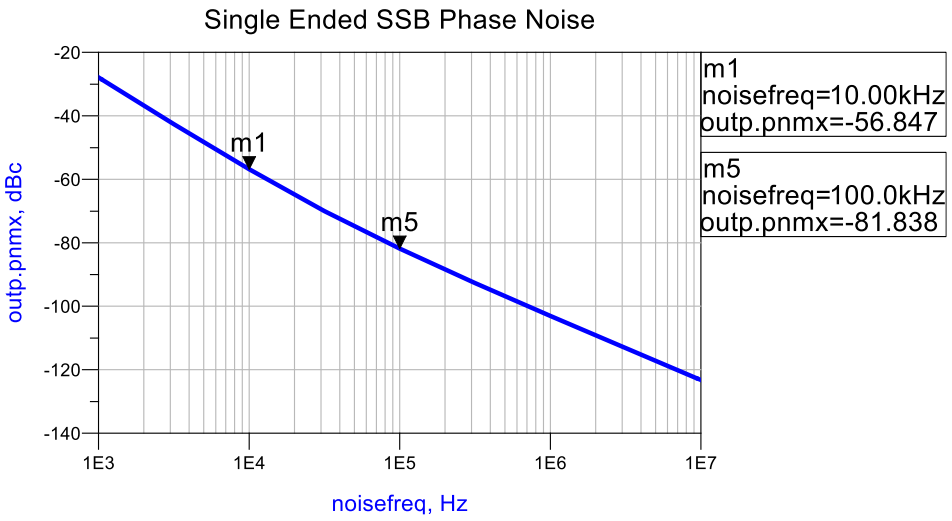


Figure 3.25: Initial Cross-Coupled Differential Pair VCO Single-Side Band Phase Noise, 5 GHz Carrier

An unloaded phase noise of -82 dBc/Hz is calculated at a 100 kHz offset, 18 dB below the initial target specification of -100 dBc/Hz. The following Section 3.7.2 further investigates phase noise and power optimization.

3.7.2 Performance Optimization

The initial schematic design yields a phase noise of -82 dBc/Hz at a 5 GHz carrier and 100 kHz offset. The following section features an improved -111 dBc/Hz phase noise at the same 5 GHz carrier and 100 kHz offset. Table 3.2 defines the improved phase noise contribution per component in the VCO design. ADS's Harmonic Balance (HB) simulates and quantifies each circuit component's noise contribution and how to improve total phase noise.

Table 3.2: ADS Optimized Phase Noise Contribution per Component

index	outp.NC.name	outp.NC.type	outp.NC.vnc
noisefreq=100.0 kHz			
0	_total	_total	-111.4 dBc
1	Q1.q1	BJT	-115.0 dBc
2	Q1.q1.ice	BJT	-116.2 dBc
3	Q1.q1.ibe	BJT	-123.8 dBc
4	Q1.q1.Rb	BJT	-126.4 dBc
5	Q1.q1.flicker	BJT	-132.5 dBc
6	Q1.q1.Rc	BJT	-133.5 dBc
7	Q1.q1.Re	BJT	-139.3 dBc
8	Q2.q1	BJT	-115.0 dBc
9	Q2.q1.ice	BJT	-116.2 dBc
10	Q2.q1.ibe	BJT	-123.8 dBc
11	Q2.q1.Rb	BJT	-126.4 dBc
12	Q2.q1.flicker	BJT	-132.5 dBc
13	Q2.q1.Rc	BJT	-133.5 dBc
14	Q2.q1.Re	BJT	-139.3 dBc
15	R5	R	-127.2 dBc
16	RFC2	R	-127.2 dBc
17	RFC	R	-127.2 dBc
18	R4	R	-131.5 dBc
19	Q1.rsub	R	-134.4 dBc
20	Q2.rsub	R	-134.4 dBc
21	TL2	MLIN2	-135.0 dBc
22	TL1	MLIN2	-135.0 dBc
23	Q1.rpsinker	R	-135.1 dBc
24	Q2.rpsinker	R	-135.1 dBc
25	R2	R	-135.7 dBc

QN.q1.x (N = 1,2; x = transistor parameter) represents a specific transistor in the circuit design, referenced to the single-ended output of ‘q1’. The HB simulation shows that the cross-coupled pair transistor’s noise generation contributes the most phase noise. Even in the improved phase noise breakdown of Table 3.2, the collector-emitter current of each differential HBT (Q1.q1.ice and Q2.q1.ice), contributes the most phase noise, -116.2 dBc/Hz.

Generally, increasing the VCO outputs signal’s magnitude and the tank circuit’s quality factor improves phase noise [32], however this paper approaches phase noise improvement techniques solely within the VCO core circuit, since the tank circuit’s quality factor is already maximized (reference Appendix B for more on phase noise). Three critical, primary methods resulting in significant phase noise improvement are decreasing the

I. Collector-emitter current

II. Base AC voltage and current variation (swing)

III. Common emitter tail AC voltage and current variation (swing)

General BJT (also applying to HBT) theory states that collector-emitter current magnitude and transistor shot noise (hence, phase noise) are proportional [33, 34]. Therefore, decreasing the collector-emitter current improves phase noise. However, decreasing the collector-emitter current also decreases transistor gain and varies impedance. This affects negative resistance, oscillation start-up, and steady-state conditions. These performance parameters are characterized and still satisfied as the collector-emitter current is tuned down to approximately 6.2 mA.

Base AC voltage and current variation is the input AC voltage and current on each cross-coupled, differential pair transistor. An HBT base terminal has a high input impedance (100s of Ohms), dominated by ohmic resistance, which generates input thermal noise scaled by current gain, β, to the output. Additionally, the HBT base terminal generates shot noise. Large AC voltage and current increase this base shot noise which is amplified by β to the HBT collector output [34]. Therefore, minimizing the AC variations at the input base terminals of each differential pair transistor, minimizes output phase noise. To minimize base AC swing, ground-shunt de-coupling capacitors are placed at the base terminals of each differential pair HBT. The base-collector AC coupling capacitor values are also decreased to 0.1 pF to increase the impedance seen by AC/RF signals at the collector terminal feeding back to the input base terminal. This further reduces base AC voltage and current magnitude.

The Hajimiri Linear Time-Varying (LTV) Phase Noise Model states that both lower and higher frequency (relative to the carrier) noise is up-converted and down-converted, respectively, into the carrier region [32, 35], shown in Figure 3.26.

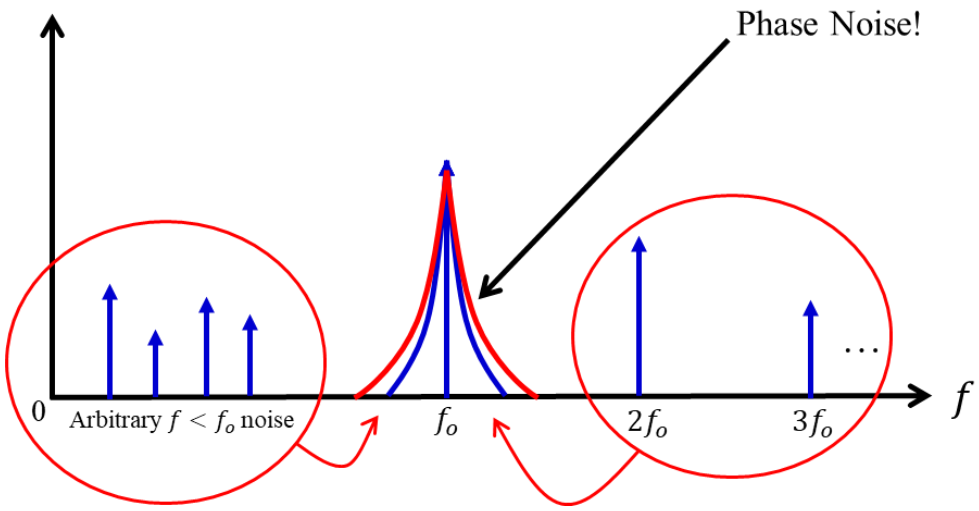


Figure 3.26: Hajimiri's LTV Phase Noise Model Showing Lower and Higher Frequency Up- and Down-Conversion

Since oscillators are inherently time-varying devices, they produce random voltage and current fluctuations or impulses, with high harmonic content, directly coupling into the oscillator's resonant frequency region, increasing phase noise. If the tank circuit's quality factor is sufficiently high, it suppresses all harmonic content and isolates the VCO's oscillation frequency. However, the practical tank circuit has a finite Q and some harmonic content, although low in power relative to the carrier. When this harmonic content is up- or down-converted, it may increase in power relative to the carrier, ultimately increasing phase noise, per Hajimiri's theory [32, 35]. The process of reducing the base voltage and current variations, described in the previous paragraph,

further reduces noisy, time-varying fluctuations and harmonic content from the device's cross-coupled feedback path, hence improving phase noise.

The cross-coupled pair's common-emitter node, commonly referred to as the differential pair's tail, also has an associated AC voltage and current. Differential circuit's odd symmetry suppress even harmonics if their outputs are combined, however, purely even harmonics reside at the differential circuit's common nodes. The dominant AC signal at the common-emitter node, or tail, is the second harmonic [36]. Although this tail node is a common virtual ground to the differential pair, the HBT's parasitic base-emitter and collector-emitter capacitances capacitively couple the tail node to the oscillator's feedback path and outputs. At harmonic frequencies above the carrier region, this capacitive coupling acts as low impedance paths. As previously discussed, the VCO is an LTV device and which generates random impulses or I-V (current-voltage) fluctuations, rich in harmonic content. Therefore, tail signal noisy harmonics capacitively couple to the VCO's outputs, down-convert to the carrier region, and degrade the overall phase noise. To alleviate this issue, a ground-connected de-coupling capacitor is placed at the common-emitter tail node. This capacitor provides an alternative low-impedance path to ground, reducing the second harmonic's I-V swing along with all its potential higher-order harmonics, ultimately improving overall phase noise.

Figure 3.27 below shows the minimized base and tail voltage variations in the time-domain. The base voltage peak-to-peak value is about 100 mV, while the tail node is less than 30 mV. The tail node's AC signal period of approximately 100 ps, yields a 10 GHz frequency, the second harmonic of a 5 GHz VCO fundamental.

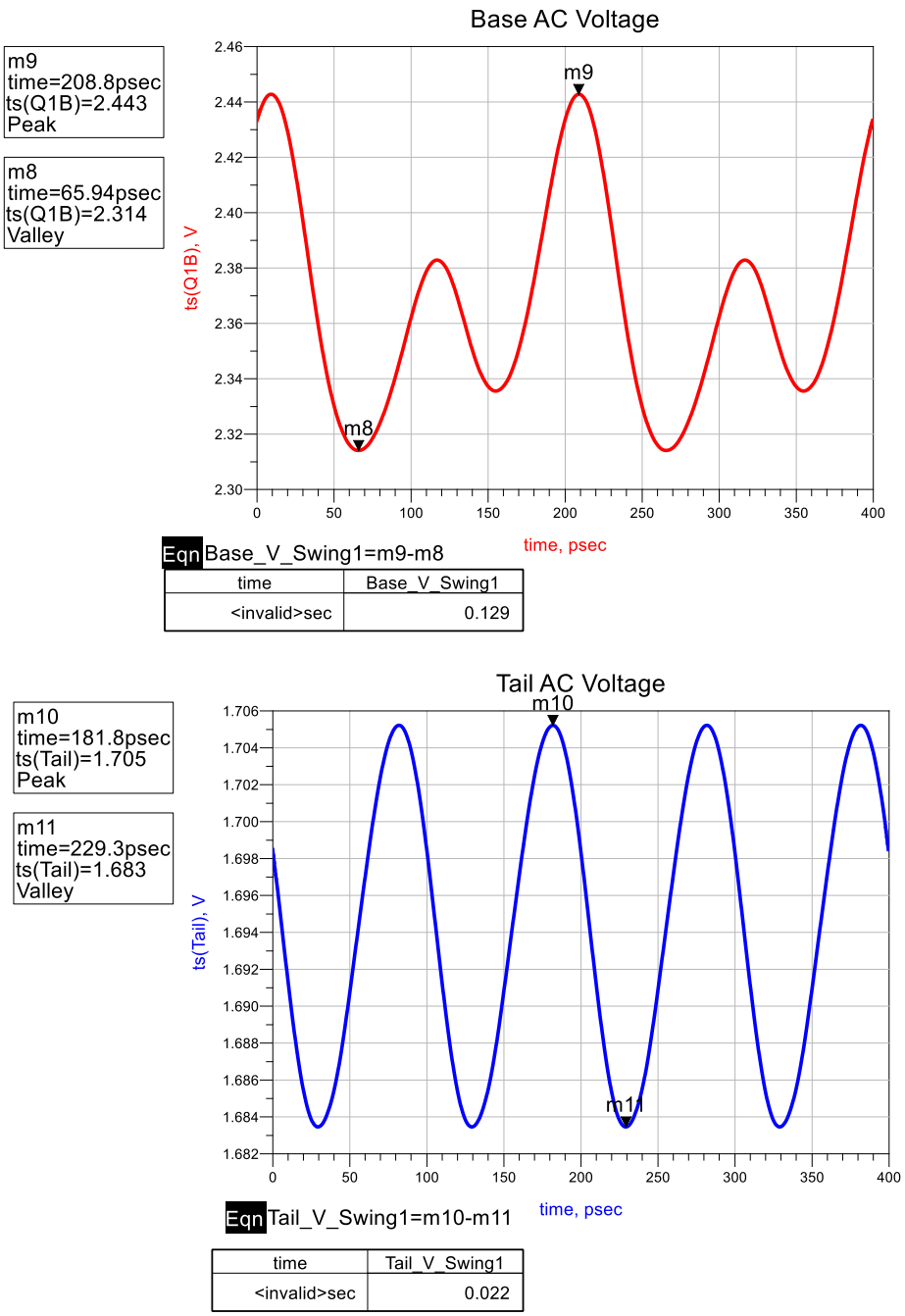


Figure 3.27: Base and Common-Emitter Tail Time Domain Voltage

In summary, careful tuning of the three described methods improves the overall phase noise by about 30 dB. Figure 3.28 below defines the improved single-ended, unloaded output phase noise measurement.

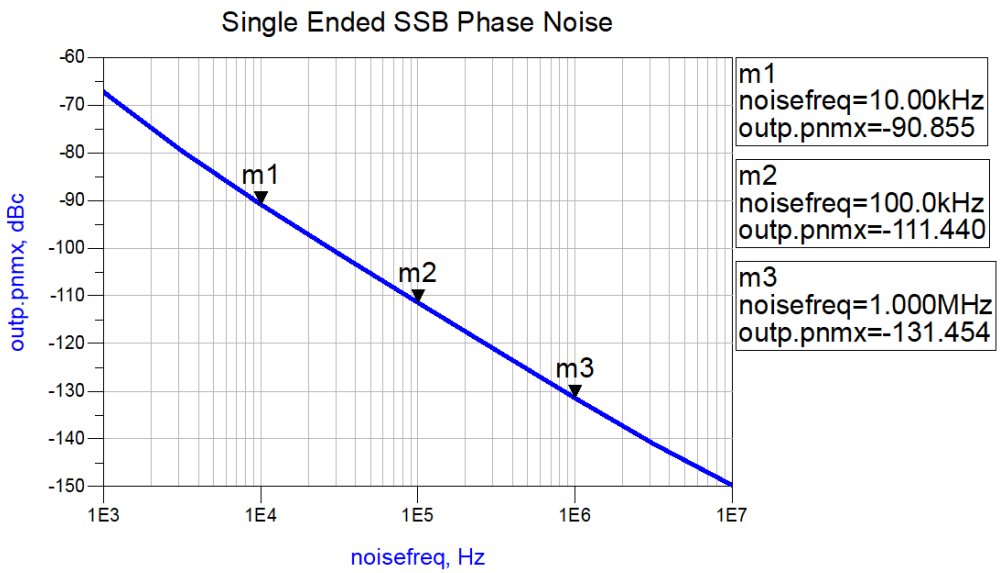


Figure 3.28: Phase Noise at 5 GHz Carrier Frequency

Figure 3.29 displays an updated VCO schematic for improved phase noise. C9 and C10 represent the added base de-coupling capacitors while C8 is the added tail de-coupling capacitor. C9 and C10 are 3 pF, while C8 is 50 pF.

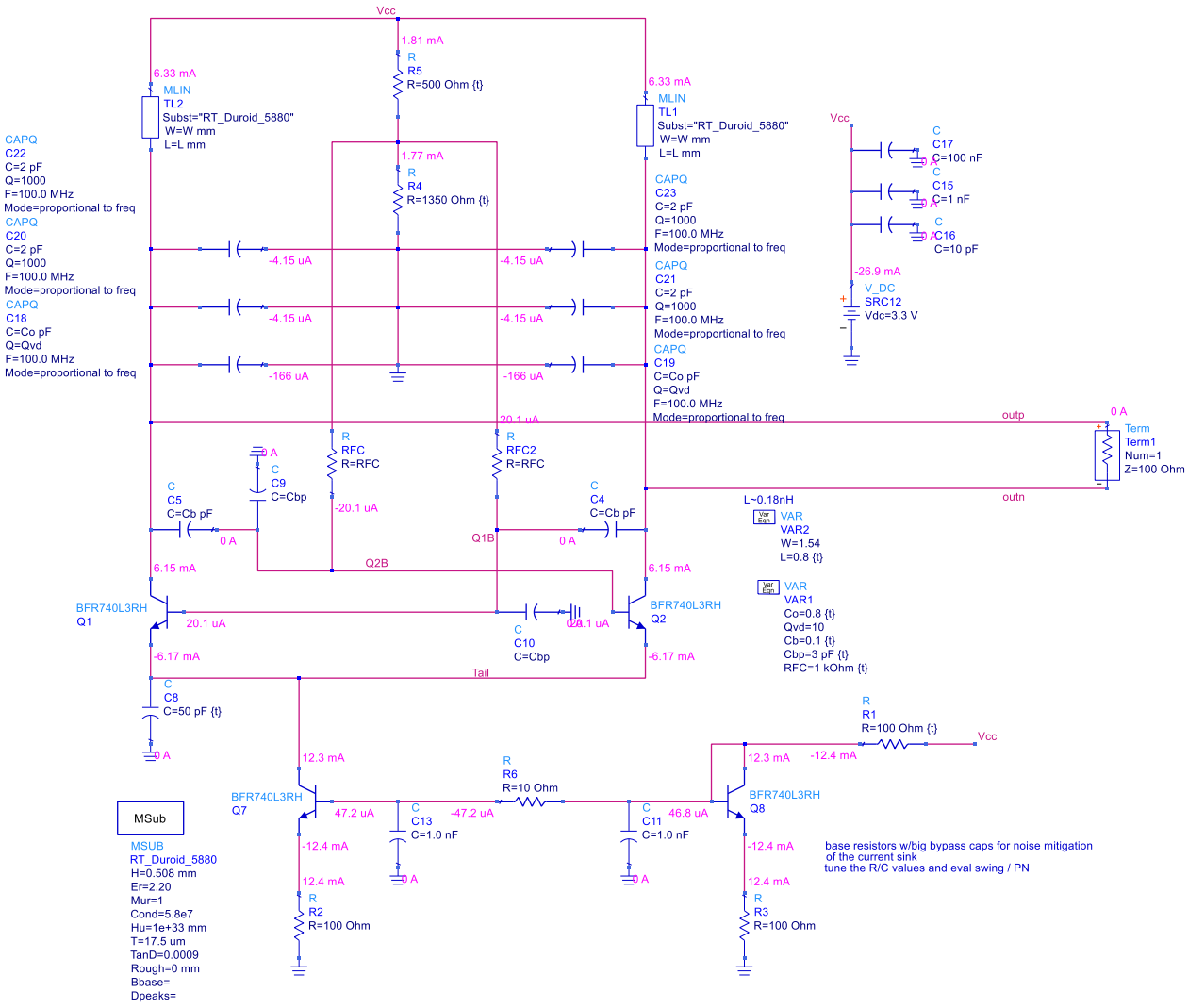


Figure 3.29: Improved Phase Noise, Updated Full VCO Schematic

3.8 Output Buffer

The output buffer is designed to provide a high-impedance to the VCO's output collector nodes, while providing a 50 Ω output impedance for direct integration to other devices.

3.8.1 Initial Output Buffer Architecture Characterization

The initial output buffer architecture is a single, common-emitter HBT. The HBT base terminal provides an input impedance of ≈ 200 Ω and 1.4 pF of parallel input capacitance (Figure 3.32). This prevents VCO load pulling, decreased output power, and decreased oscillator resonant frequency as described in Section 3.1, equation (3.8). With a collector current of 5 mA, a minimum 13 dB gain (Figure 3.31) at 5.5 GHz is still achieved while minimizing power consumption.

Figure 3.30 defines the ADS schematic characterizing the common-emitter architecture for S- and Y-parameters.

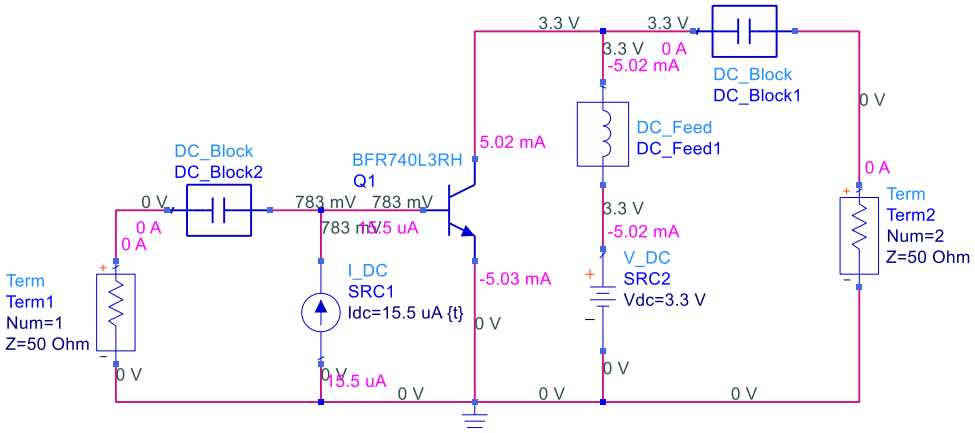


Figure 3.30: Initial Output Buffer Schematic Characterization

Figure 3.31 below highlights the output buffer's forward transmission S_{21} parameter (gain) with 50Ω input/output (I/O) port terminations.

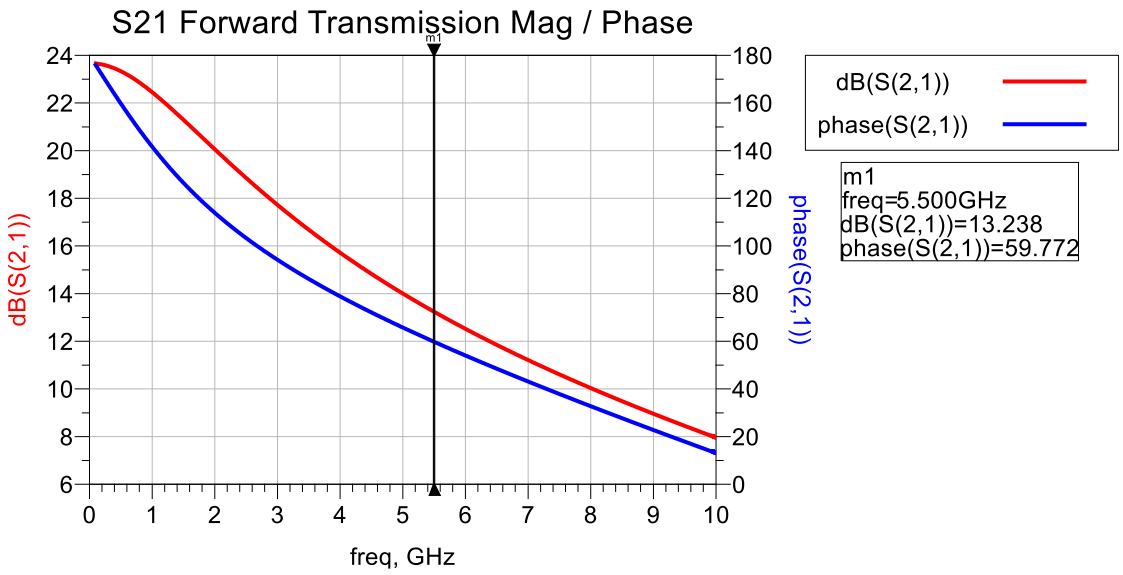


Figure 3.31: Initial Output Buffer Forward Transmission vs. Frequency

Figure 3.32 below defines the output buffer's parallel equivalent input resistance and capacitance. The VCO output is loaded by this equivalent input impedance.

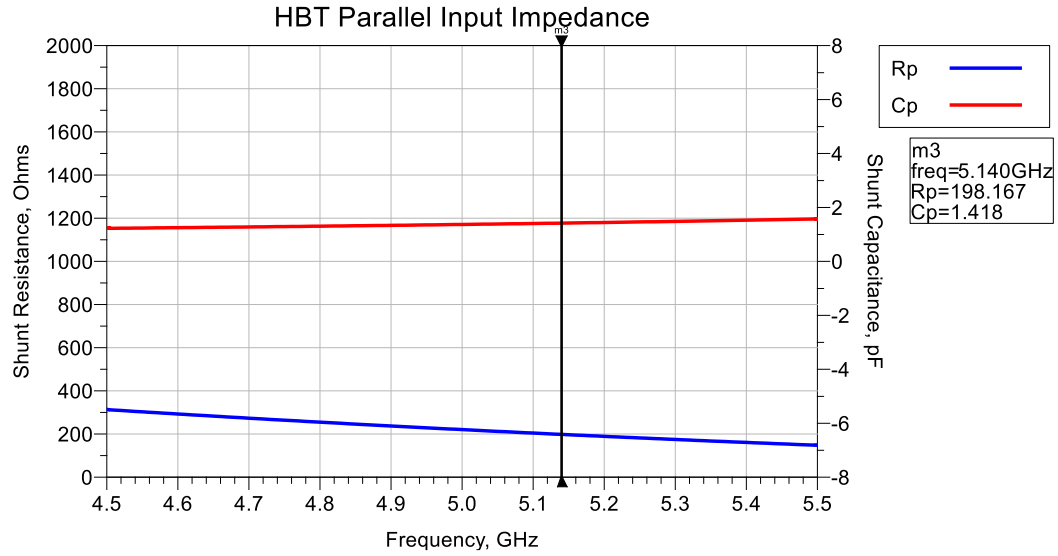


Figure 3.32: Initial Output Buffer Parallel Input Impedance

3.8.2 Emitter Follower Architecture

An alternative to the initial common emitter output buffer is an emitter follower (common collector or CC). Previously, the common emitter topology provides a minimum voltage gain of 13 dB, however the VCO output is already approximately 85% rail-to-rail (≈ 2.8 V output swing). This results in output buffer compression and a clipped, non-linear output signal. The common collector, emitter follower architecture provides power drive but in the form of current gain, not voltage gain. Ideally, the emitter follower has unity voltage gain, however, voltage loss is possible. This alternative current drive avoids buffer compression, preventing output signal nonlinearities.

The first step in this design is setting the emitter DC bias point to 1.65 V, half of the rail to the rail voltage – 0 to 3.3 V. This allows the output signal to have increased voltage margin for maximum peak-to-peak AC voltage. The emitter current is the collector current if the HBT's β-value is sufficiently large, which is applicable. With a bias emitter/collector current of 5 mA and 1.65 V emitter voltage, the emitter resistor value is 330 Ω.

Next the base voltage is estimated to 2.43 V since the base-emitter voltage drop is approximately 0.78 V [22] set by a voltage divider and Vcc (3.3 V); R2 is set to 50 kΩ, R1 = 17.5 kΩ. These relatively large resistances (10s kΩ) minimize the base bias network's overall current consumption, and hence power consumption.

The input and output AC coupling capacitor values are computed to approximate AC shorts. If the target impedance is 1 Ω and lowest operational frequency is 4.5 GHz,

the minimum capacitance is 35 pF. 0.1 nF (100 pF) is selected for both input and output AC coupling capacitors.

An important requirement is a high input impedance. The equivalent emitter follower input resistance is approximated in equation (3.12).

$$R_{IN} \approx R_{B1} \,||\, R_{B2} \,||\, \beta(R_E + r_E) \,||\, R_{Load} \tag{3.12}$$

Note, $\beta(R_E + r_E)$ is the HBT's dynamic input resistance, r_π. Since $r_E \approx \frac{V_t}{I_E} \approx \frac{V_t}{I_c}$, R_E dominates over r_E since it is much larger. Since $\beta R_E \ll (R_{B1}\ and\ R_{B2})$, it dominates the entire expression, and the equivalent emitter follower input impedance can be approximated as βR_E. Since load impedance is in parallel with R_E, it affects input impedance. If this value is substantially less than R_E, the load dominates and decreases the input impedance. Decreasing the output AC coupling capacitors, increasing its effective series impedance at the operational frequencies, helps mitigate this loading effect. However, the output AC coupling capacitor now consumes output power and contributes to the emitter followers' loss.

Figure 3.33 below displays the realized emitter follower circuit schematic. Notice the increased 750 Ω emitter resistor and decreased 0.5 pF output coupling capacitor. These values are finalized through tuning to optimize a high input impedance while minimizing the circuit's forward transmission loss.

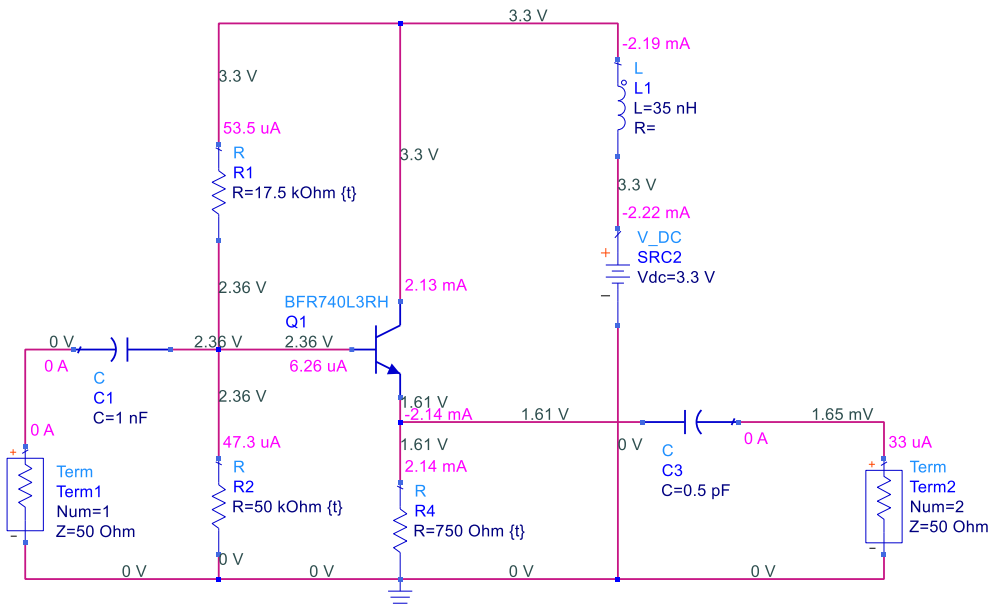


Figure 3.33: Emitter Follower Output Buffer Circuit Schematic

Figure 3.34 below defines the equivalent input impedance, separated as a parallel resistance and capacitance. The calculated input resistance, R_P, is 855 Ω to 933 Ω, varying with frequency due to β-value variations at microwave frequencies. The shunt capacitance, C_P, is minimized to less than 0.4 pF, to prevent capacitive loading.

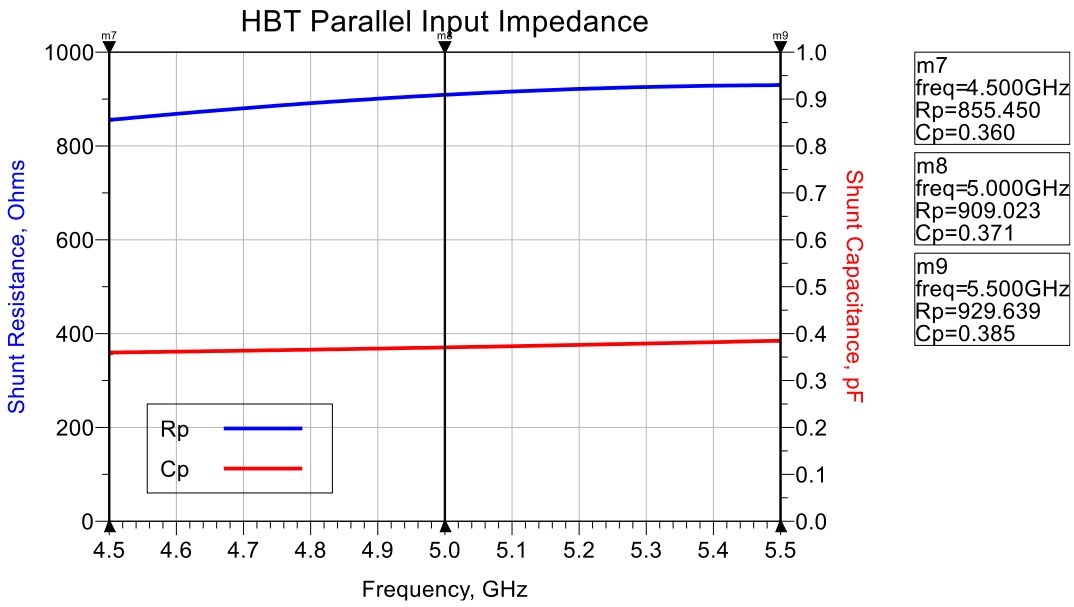


Figure 3.34: Emitter Follower Equivalent Input Impedance vs. Frequency

Figure 3.35 defines the design's forward transmission, simulating ≈ -2 dB.

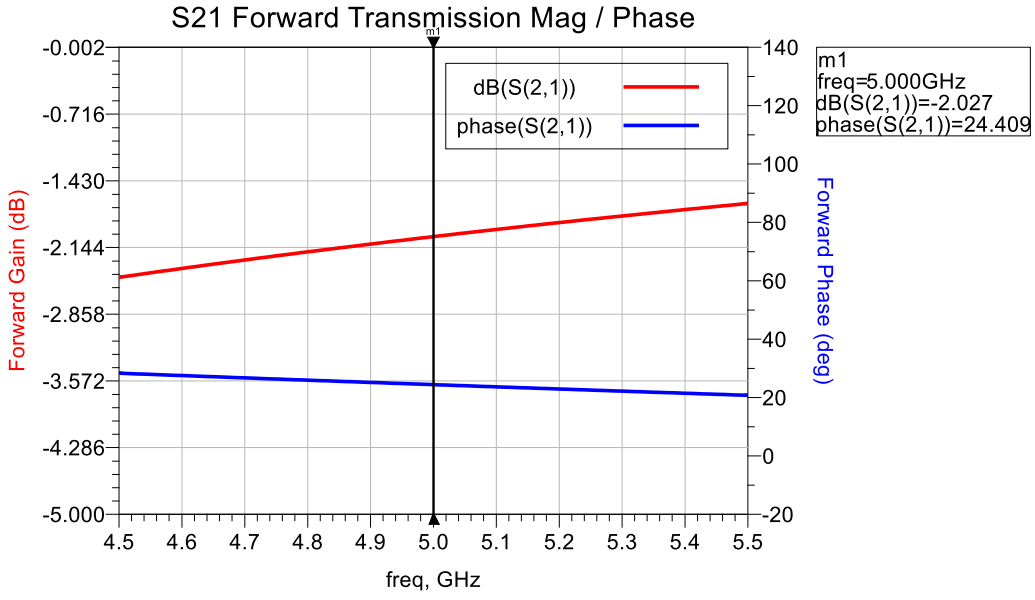


Figure 3.35: Emitter Follower Forward Transmission vs. Frequency

3.8.3 Final Output Buffer Design

To maintain a distortionless VCO output signal, the output buffer must operate linearly. The emitter follower topology minimizes transistor compression, however, after integrating the emitter follower with the cross-coupled, differential pair, the full VCO output appears distorted. Therefore, the output buffer's linearity performance is further investigated. To eliminate buffer input impedance loading, the initial common emitter topology is redesigned.

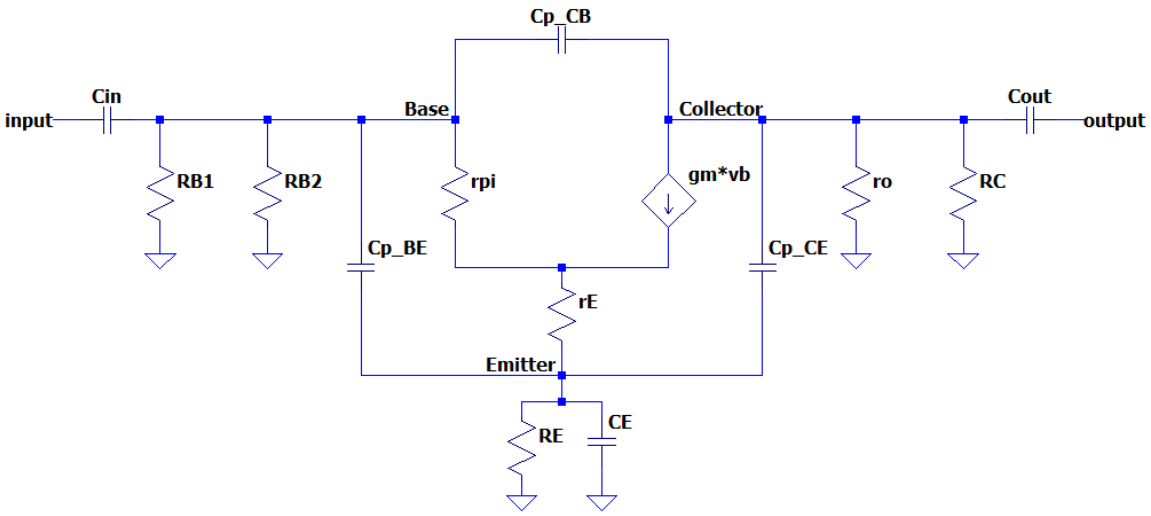


Figure 3.36: Full Common Emitter Small-Signal Hybrid-π Model

Figure 3.36 presents the common emitter amplifier's full AC, small-signal hybrid-π model including parasitic capacitances and the DC bias network. Table 3.3 below defines all hybrid-π circuit parameters of Figure 3.36.

Table 3.3: Common Emitter Hybrid-π Model Parameter Definitions

Circuit Parameter	Description	Units
$\boldsymbol{g_m}$	HBT transconductance; $g_m \approx I_C/V_t$	S or Ω^{-1}
$\boldsymbol{V_t}$	HBT thermal voltage; $V_t \approx kT/e \approx 26$	mV
$\boldsymbol{V_A}$	HBT early voltage; typically, a large value	V
$\boldsymbol{C_{in}}$	Input AC coupling capacitance	F
$\boldsymbol{C_{out}}$	Output AC coupling capacitance	F
$\boldsymbol{R_{B1}}$	Base bias resistor	Ω
$\boldsymbol{R_{B2}}$	Base bias resistor	Ω
$\boldsymbol{R_C}$	Collector bias resistor	Ω
$\boldsymbol{R_E}$	Emitter degeneration resistor	Ω
$\boldsymbol{r_\pi}$	Dynamic input resistance; $r_\pi \approx \beta/g_m \approx V_t/I_B$	Ω
$\boldsymbol{r_E}$	Dynamic emitter resistance; $r_E \approx 1/g_m \approx V_t/I_C$	Ω
$\boldsymbol{r_o}$	Dynamic output resistance; $r_o \approx V_A/I_C$	Ω
$\boldsymbol{C_E}$	Emitter degeneration capacitance	F
$\boldsymbol{C_{P\_BE}}$	Base-emitter parasitic capacitance	F
$\boldsymbol{C_{P\_CE}}$	Collector-emitter parasitic capacitance	F
$\boldsymbol{C_{P\_CB}}$	Collector-base parasitic capacitance	F

Disregarding parasitic capacitances, equations (3.13) and (3.14) define the common emitter equivalent input and output resistances, respectively. Note, $r_\pi = \beta(R_E + r_E)$.

$$R_{IN} \approx R_{B1} \,||\, R_{B2} \,||\, r_\pi \approx r_\pi \tag{3.13}$$

$$R_{out} \approx r_o \,||\, R_C \,||\, R_{Load} \tag{3.14}$$

The input resistance is independent of the buffer's output load and dominated by the dynamic input resistance. However, the output resistance is in parallel with the output load. Output loading is compensated by integrating a matching network into the design – matching the amplifier's Z_{out} to Z_{Load} (50 Ω).

The output node DC voltage is set to half of the rail-to-rail voltage, 1.65 V, to achieve maximum peak-to-peak output voltage. The collector resistor in equation (3.15), is 665 Ω.

$$R_C = \frac{V_{CC} - V_C}{I_C} \tag{3.15}$$

To maintain linear CE amplifier operation, $V_C > V_B > V_E$. Since the base-emitter voltage is ≈ 0.76 V for a 2.5 mA collector current [22], an emitter voltage of 0.5 V satisfies the above inequality. The DC base voltage is ≈ 1.26 V enabling R_{B1} and R_{B2} computations, shown in equation (3.16). Note, $V_{CC} = 3.3\,V$ and $V_B = 1.26\,V$.

$$\begin{gathered} V_B \approx V_{CC}\frac{R_{B2}}{R_{B2}+R_{B1}} \rightarrow \frac{V_B}{V_{CC}} \approx \frac{R_{B2}}{R_{B2}+R_{B1}} \rightarrow \\ Let\ A = V_B/V_{CC}, \\ A(R_{B2}+R_{B1}) \approx R_{B2} \\ \vdots \\ R_{B1} \approx R_{B2}\frac{(1-A)}{A} \end{gathered} \tag{3.16}$$

Substituting A in equation (3.16) yields $R_{B1} \approx 1.5\,R_{B2}$. Setting, R_{B2} to 10 kΩ, results in a 15 kΩ R_{B1} value. An emitter degeneration resistor increases the buffer input resistance, as shown in equation (3.13). With a 0.5 V DC emitter voltage and approximately 2.5 mA

emitter current ($I_E \approx I_C$ since β is sufficiently high) $R_E \approx 200\ \Omega$. Although R_E helps increase R_{IN}, it also decreases the buffer's gain. To alleviate this effect, a capacitor is placed in parallel with the degeneration resistor. This provides a low impedance RF path at operational frequencies. To ensure the bypass capacitors effective impedance is less than the emitter resistor, $Z_{C_E} \rightarrow \frac{1}{10} R_E \approx 20\ \Omega$. Setting this impedance to $(1/\omega C)$, a 1.8 pF capacitance is derived at 4.5 GHz. A 10 pF capacitor value is selected. However, through tuning a 1 nF emitter capacitor (with a sufficiently high SRF) is selected to provide low impedance RF paths and DC blocks for the buffer input and output terminals. Figure 3.37 displays the described common emitter buffer.

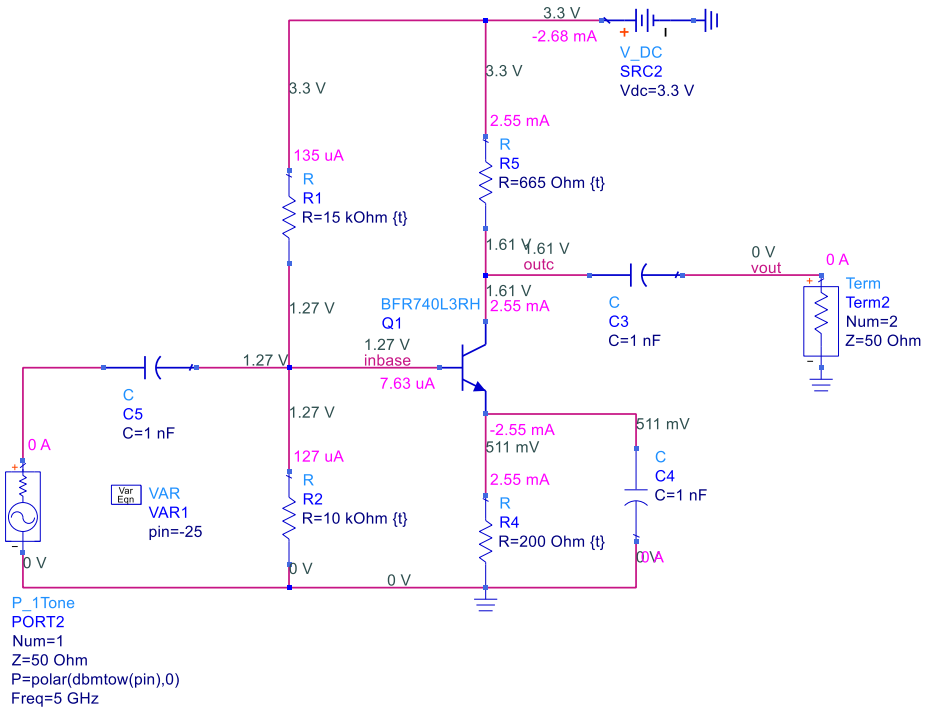


Figure 3.37: Modified CE Output Buffer Schematic

RF amplifier linearity is quantified by the 1 dB compression point. As input power increases an RF amplifier becomes compressed (or saturated) and the output signal

begins to “clip”. As input power increases, gain decreases and clipping increases; the output signal begins to generate input signal harmonics, becoming non-linear. The 1 dB compression point is defined relative to input or output power, IP1dB or OP1dB, respectively, and is the power at which the gain compresses (decreases) by 1 dB at a particular frequency. Figure 3.38 shows the designed output buffer’s gain vs. input power curve at 5 GHz. This reveals a ≈ -19 dBm IP1dB and a ≈ -9.8 dBm OP1dB. OP1dB is the sum of IP1dB and gain.

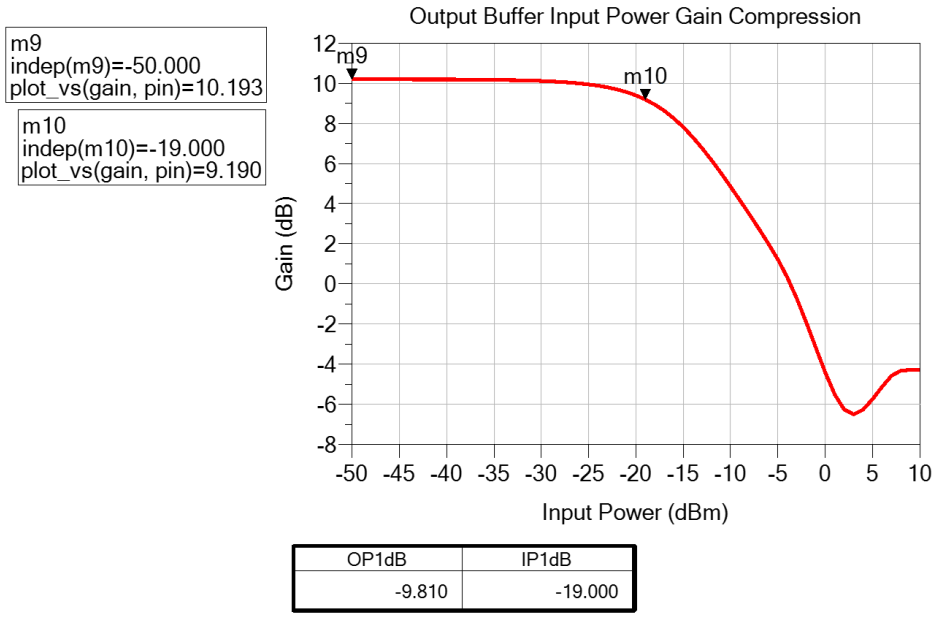


Figure 3.38: CE Output Buffer Gain Compression

This simulation shows buffer compression with cross-coupled, differential pair output signal power greater than 0 dBm. Therefore, the buffer’s 1 dB compression point must be increased. To solve this, the transistor’s bias level must be increased, a new transistor device must be chosen, or the output buffer’s input signal power must be

decreased before entering the base terminal. To minimize power consumption and maintain system components, the buffer's input signal power is decreased. Decreasing this power level also decreases the buffer's output power level and therefore the full VCO output power. However, VCO RF output power is a lower priority performance parameter compared to both linearity (or phase noise) and DC power consumption.

A series capacitor, with a sufficient SRF, is a high-pass filter. Decreased capacitance leads to an increased frequency response. Therefore, minimizing capacitance presents a greater impedance and attenuation. Combining two capacitors in series effectively halves the equivalent capacitance, further increasing the equivalent impedance and attenuation. A capacitive divider, modeled below in Figure 3.39 is implemented in Figure 3.40.

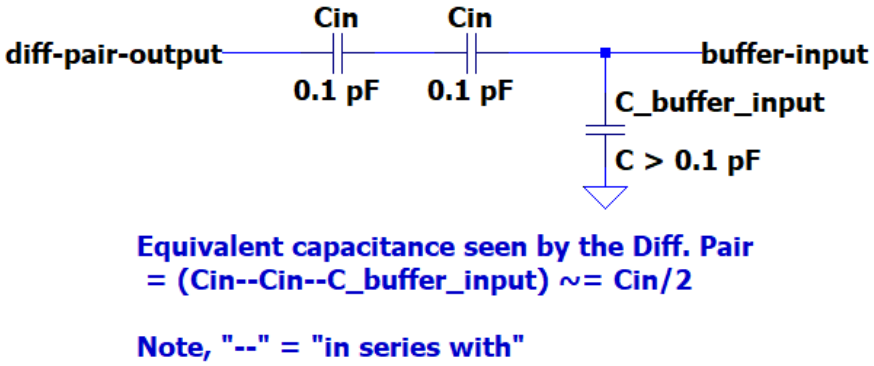


Figure 3.39: Cross-Coupled, Differential Pair to Output Buffer Capacitive Divider Model

Since a series capacitor at the buffer's base input serves as an AC coupling capacitor, a second series capacitor is added. Note this solution still satisfies its initial purpose as an AC coupling capacitor, blocking direct current (DC).

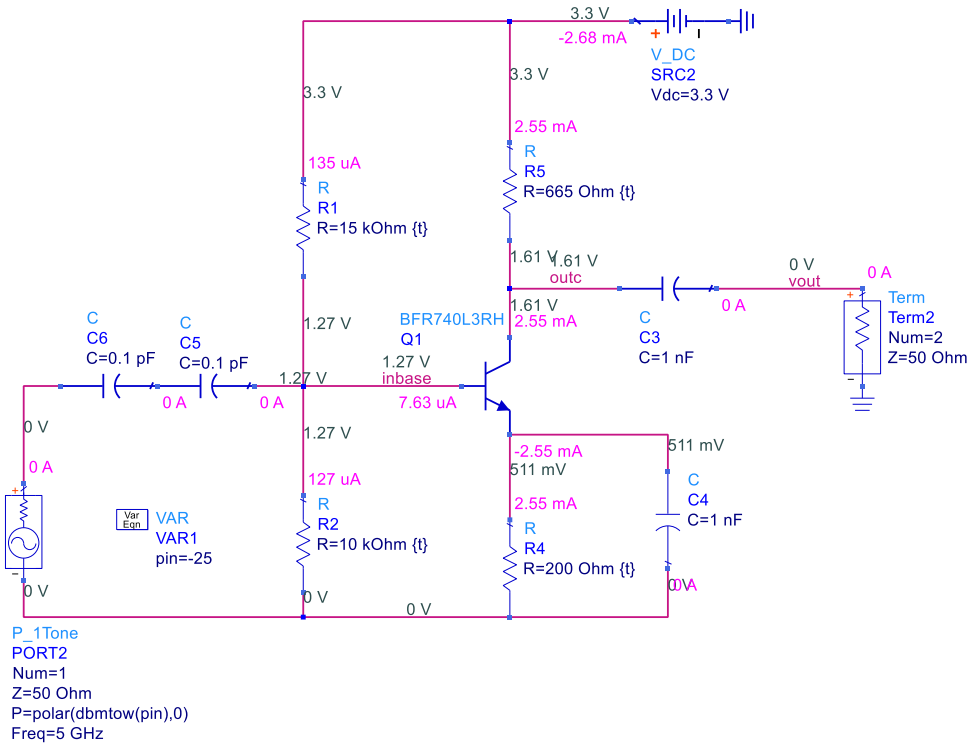


Figure 3.40: Modified Final Output Buffer with Capacitive Divider

Two capacitors in series have equivalent capacitance, $\frac{C_1 C_2}{C_1+C_2}$. When both capacitors are equal, this results in half the value ($C/2$). When the value of one capacitor is much greater than the other, the smaller capacitance dominates. The output buffer's input capacitance has minimal effect on the equivalent capacitance seen by the differential pair. The differential pair sees an equivalent capacitance approximately $\leq C/2$ (0.05 pF). This reduces capacitive loading effects on the cross-coupled, differential pair VCO's resonant frequency. Additionally, Figure 3.39 and Figure 3.40 specify 0.1 pF capacitors. These are minimum valued capacitors with a 19.4 GHz SRF [37] sufficient for this design's operational frequencies.

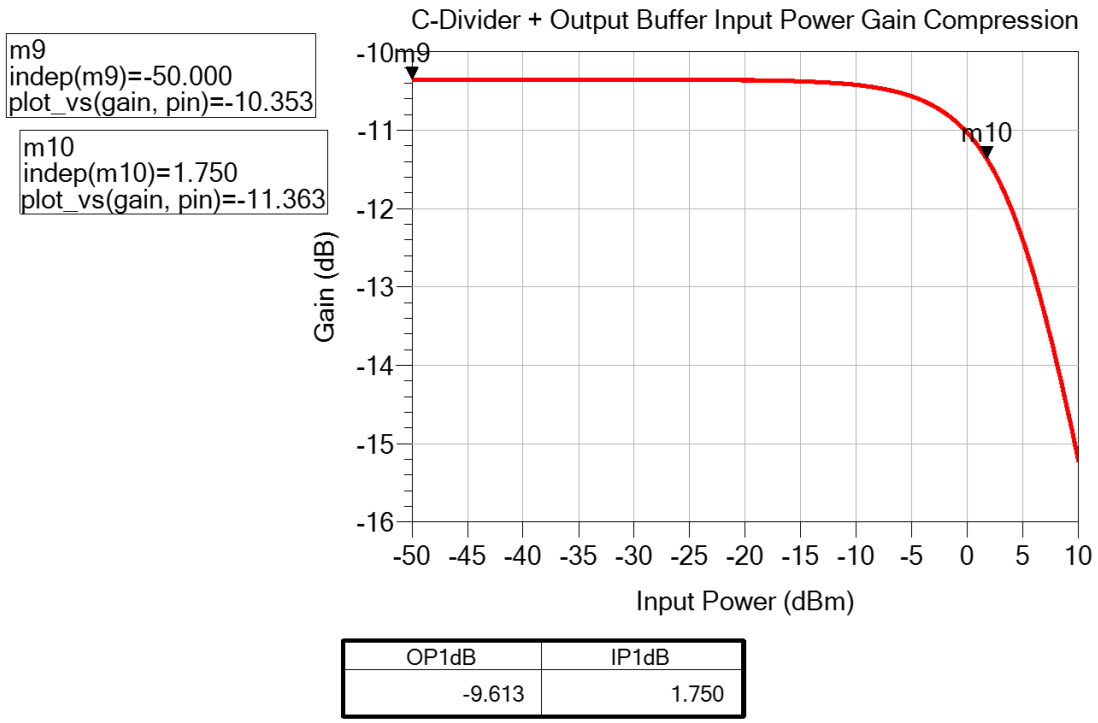


Figure 3.41: Capacitive Divider + Output Buffer Gain Compression

Figure 3.41 above defines the revised input gain vs. input power curve at 5 GHz. The IP1dB has increased to 1.75 dBm. This 20.75 dB improvement allows the full output buffer architecture to tolerate higher power input signals while maintaining linearity. The OP1dB is -9.6 dBm (similar to previous value) since the capacitive divider attenuation is greater than the initial buffer amplifier gain. Comparing the initial buffer gain (≈10.2 dB) and the observed buffer + the capacitive divider gain (≈ -10.4 dB), the capacitive divider has an attenuation of 20.6 dB. As expected, this corresponds to the 20.75 dB IP1dB improvement since IP1dB is indirectly proportional to gain.

The equivalent input resistance and capacitance of the final output buffer is characterized below in Figure 3.42. As expected, the input resistance is on the order of 100s of kΩ and MΩ due to the high impedance series capacitive divider at the buffer's

input. Additionally, the input capacitance is as expected, approximately 0.05 pF from 4.5 GHz to 5.5 GHz.

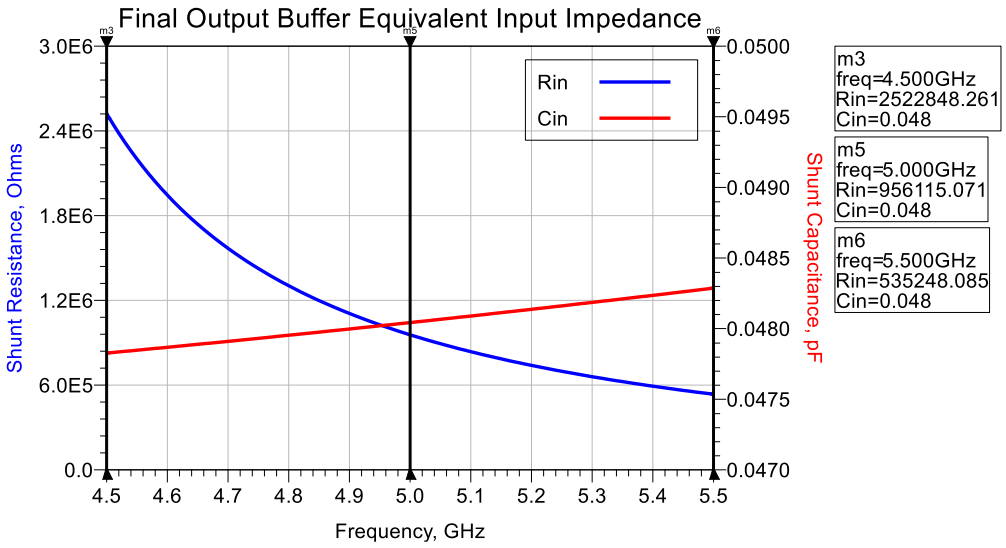


Figure 3.42: Final Output Buffer Equivalent Input Resistance and Capacitance

Figure 3.43 and Figure 3.44 define the output return loss for the buffer with the initial 1 nF output AC coupling capacitor. Figure 3.43 plots the return loss on a Smith chart while Figure 3.44 plots the output return loss logarithmically from 4.5 to 5.5 GHz.

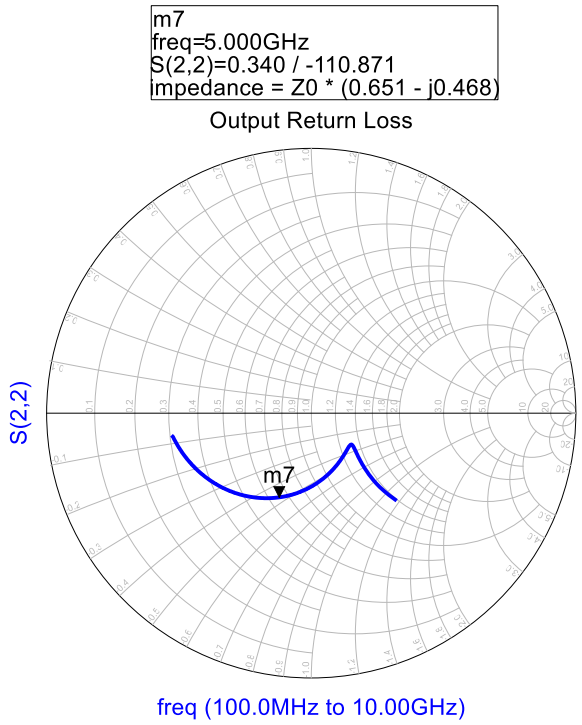


Figure 3.43: Output Buffer Output Return Loss, No Matching Network

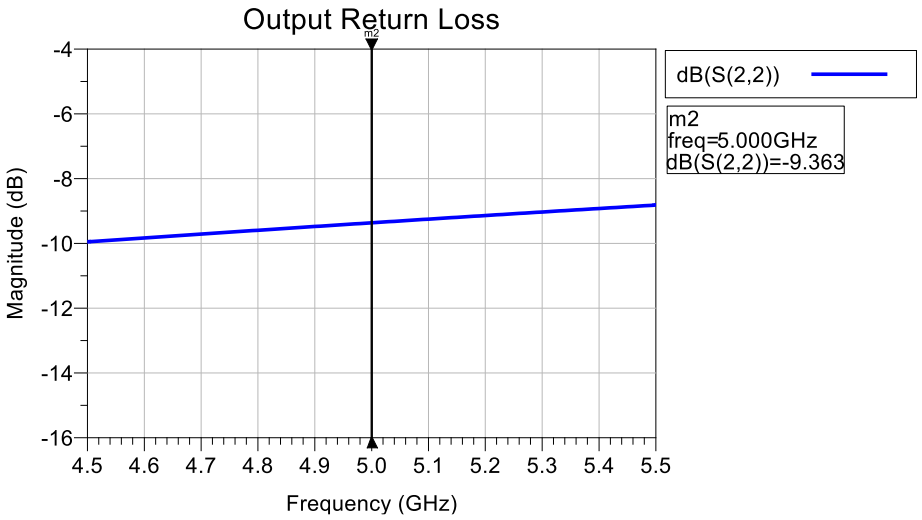


Figure 3.44: Output Buffer Output Return Loss, No Matching Network

The previous two figures show unacceptable output return loss performance for the operational frequencies, -9.4 dB at 5 GHz. To achieve a maximum -10 dB return loss for all operational frequencies, a matching network is designed. A discrete CLC T-

network design, composed of a series capacitor, shunt inductor, and series capacitor is implemented. This third-order topology is selected as the network utilizes the already incorporated output series capacitor to maintain AC coupling. Since the topology is a third-order network, it provides greater bandwidth capabilities than a second order network. It also matches to more area on the Smith chart compared to a second-order L-network. Three discrete circuit elements provide increased tuning capabilities for future design optimization or troubleshooting as chip inductor and capacitor values are easily replaceable.

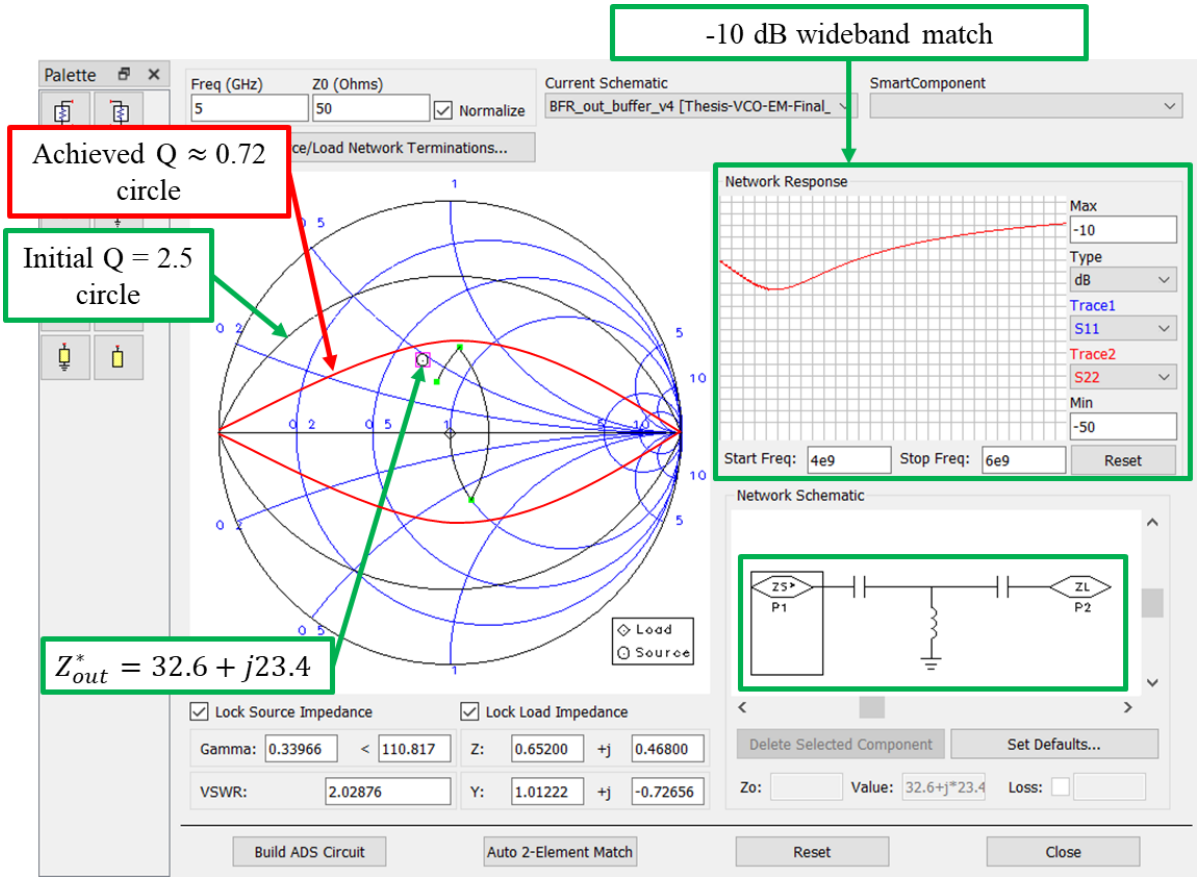


Figure 3.45: Output Buffer Output Matching Network Design

Figure 3.45 above displays the Smith Chart tool in Keysight ADS to match the $32.6 - j23.4\ \Omega$ buffer output impedance, Figure 3.43, to 50 Ω at 5 GHz. The actual

impedance is translated to $32.6 + j23.4\ \Omega$, to conjugate match for maximum power transfer. Figure 3.45 shows a Q-circle of 2.5 (eye-shape on the Smith chart) to achieve a minimum bandwidth of 2 GHz, covering from 4 to 6 GHz, respectively. The network's response computes a return loss less than -10 dB (< 30% reflected power) for the full bandwidth, as shown in the top right corner of Figure 3.45. Note the matching network does not fully transform the output buffer impedance to 50 Ω, however, the differences between nominal inductor and capacitor values from design values are acceptable. Figure 3.46 below shows the final output buffer design with both the input capacitive divider and output matching network.

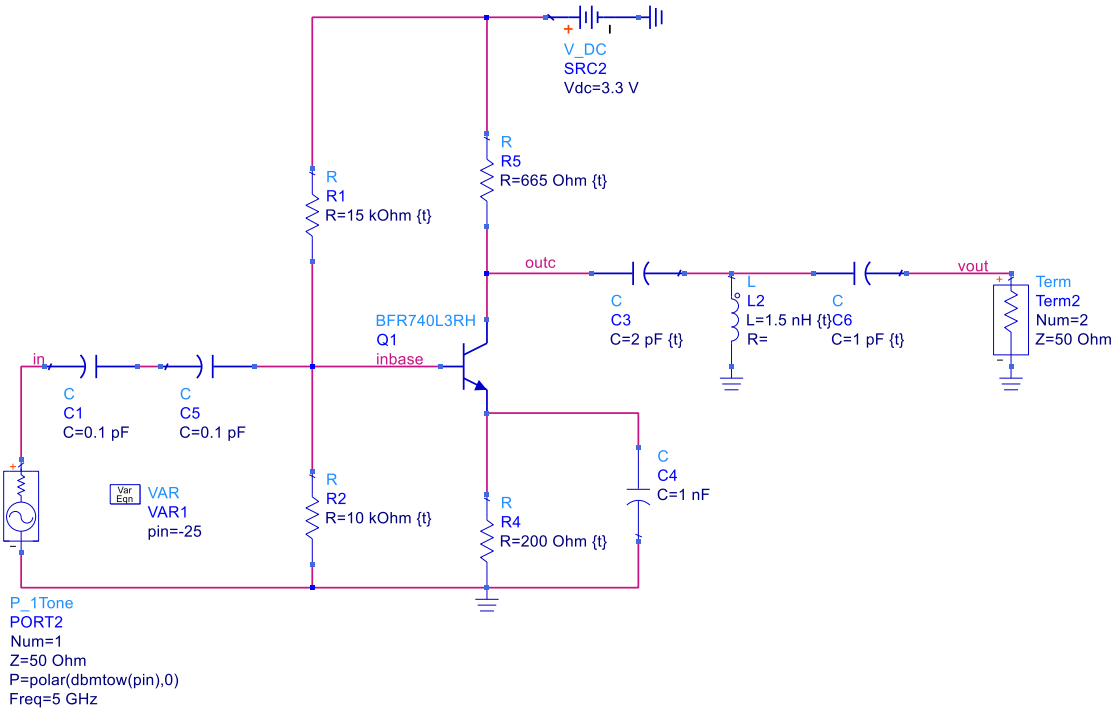


Figure 3.46: Final Output Buffer Schematic Design

Figure 3.47 and Figure 3.48 below defines the improved final output buffer's output return loss with the integrated output matching network of Figure 3.46.

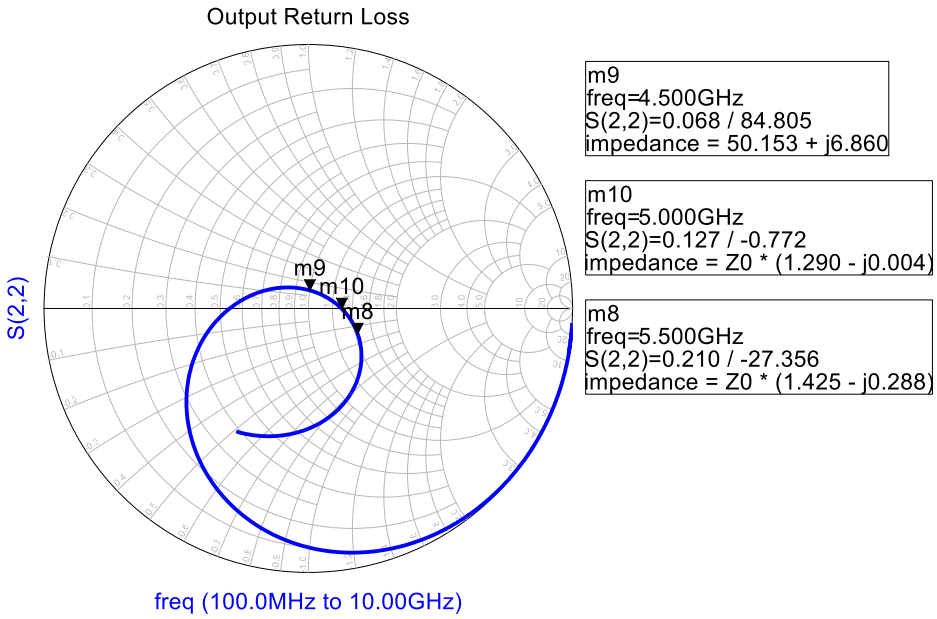


Figure 3.47: Final Output Buffer Output Return Loss, Smith Chart

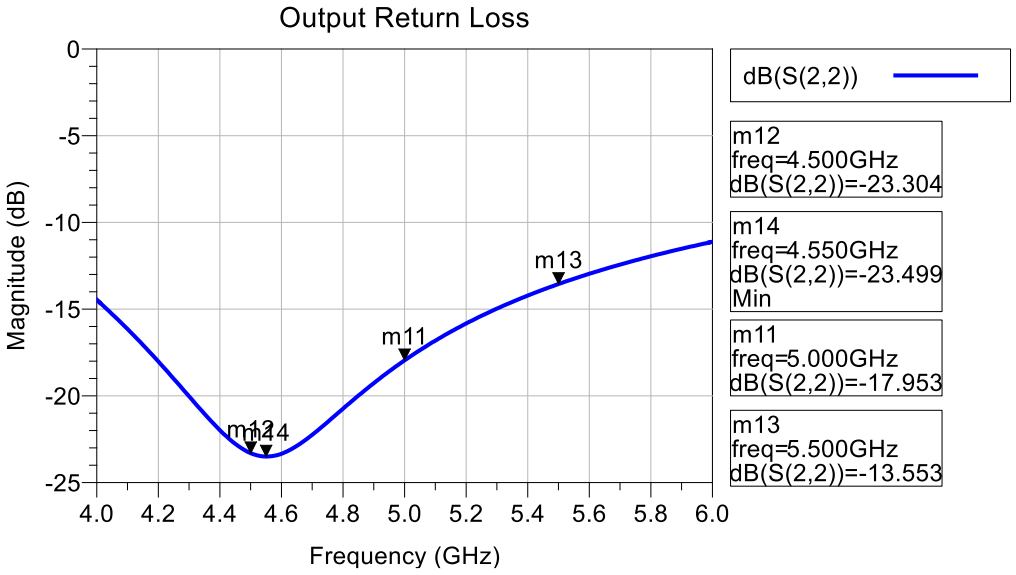


Figure 3.48: Final Output Buffer Design Output Return Loss

3.9 Final Schematic Design and Performance

Figure 3.49 below shows the full output buffer schematic. Note that this circuit is mirrored for both differential outputs.

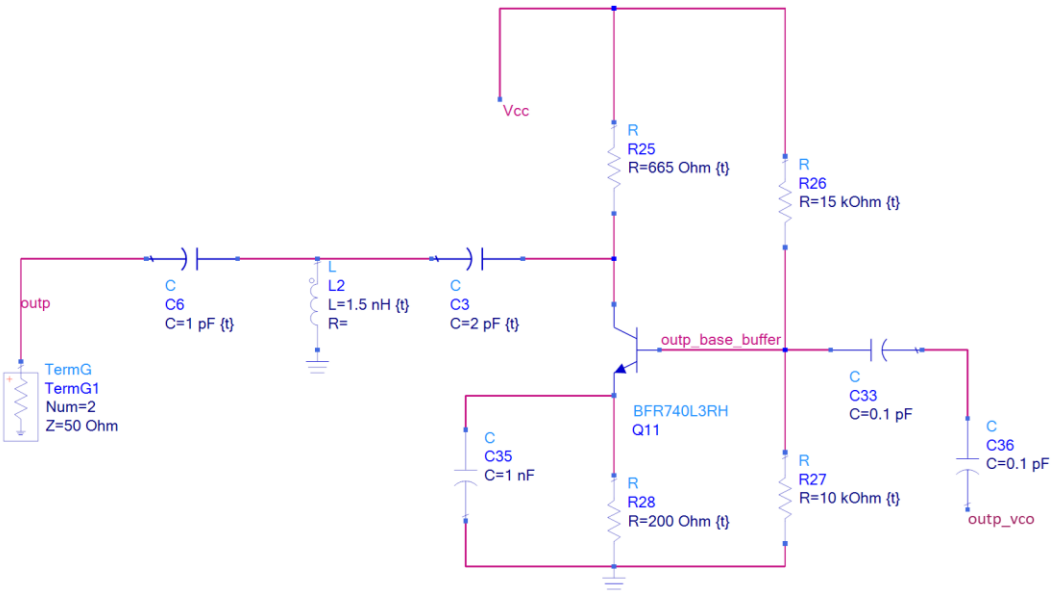


Figure 3.49: Final Output Buffer Schematic (Both Differential Outputs)

Figure 3.50 below shows full cross-coupled, differential VCO stage, composed of the tank circuit, cross-coupled core, base bias network, and current source. Inductors are lumped, fixed components with datasheet ESR [25]. Resistors R14 – R16 and R18 – R20 represent ESR in fixed capacitors and varactor diodes. These resistors model actual circuit parasitics that decrease the tank circuit's quality factor. C18 and C19 are fixed capacitors that represent the varactor diode's effective capacitance. C15 – C17 are supply de-coupling capacitors for noise and harmonic suppression.

The bias voltage for the current supply is implemented using a separate DC voltage source, SRC13. This voltage is nominally set to 3.3 V, but allows adjustment, hence the cross-coupled, differential pair's tail bias current is user defined.

(Please proceed to page 88 for the enlarged VCO stage schematic)

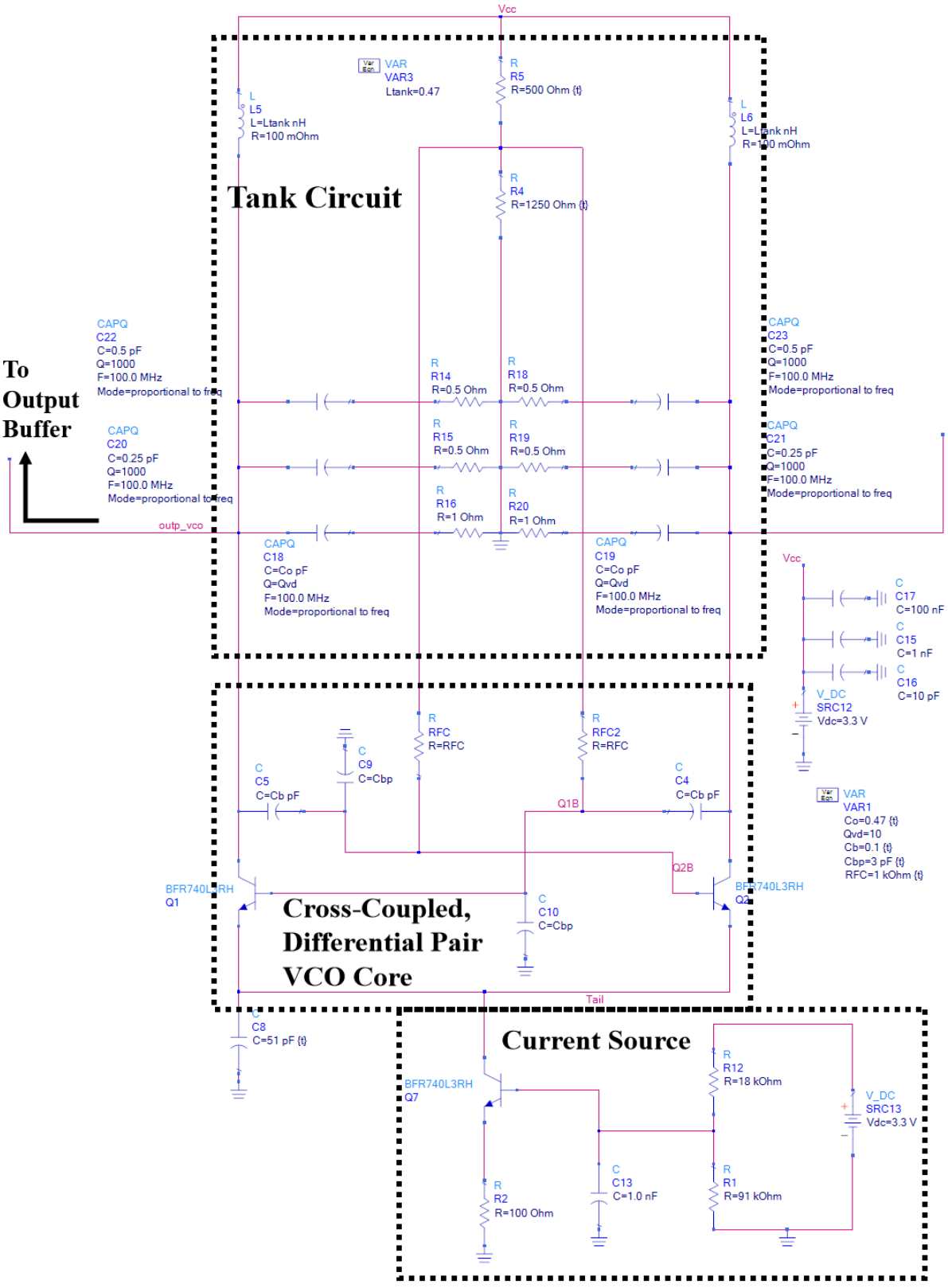


Figure 3.50: Final Cross-Coupled, Differential Pair VCO Stage Schematic

Table 3.4 below defines the single-ended simulated performance at multiple voltage tuning levels and oscillation frequencies.

Table 3.4: Final Schematic Design Simulated Single-Ended Output Performance

Parameter	**5.8 V_{tune}**	**6.8 V_{tune}**	**7.8 V_{tune}**	**10.8 V_{tune}**	**18.3 V_{tune}**	**Units**
Effective Varactor Capacitance	1.09	0.88	0.73	0.55	0.47	pF
VCO Output Frequency, f_o	4.53	4.73	4.88	5.08	5.18	GHz
G_{IN} at f_o	-2.05	-2.40	-2.70	-3.15	-3.40	mS
G_T at f_o	0.8	0.69	0.59	0.47	0.43	mS
VCO Output Swing	257	295	315	327	328	mV_{pp}
Output Power	-7.94	-6.73	-6.16	-5.80	-5.74	dBm
100 kHz Offset Phase Noise	-94.3	-94.8	-94.9	-94.6	-94.4	dBc/Hz
2nd Harmonic Suppression	17.2	17.2	16.8	16.1	15.8	dBc
3rd Harmonic Suppression	34.7	31.3	29.2	26.6	25.4	dBc
4th Harmonic Suppression	53.7	46.8	42.9	39.1	37.6	dBc
Output Return Loss at f_o	-23.6	-22.2	-19.8	-17.2	-16.1	dB
Power Consumption	65.3	65.3	65.3	65.3	65.3	mW
Frequency Pushing	2	3	3	4	3	MHz/V
Frequency Pulling (2:1 VSWR)	45	N/A	3	82	135	kHz
FOM$_P$[1]	-169.3	-170.1	-170.5	-170.6	-170.5	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Figure 3.51 below defines the single-ended, single side-band phase noise as a function of offset frequency. The tuning voltage is set to 10.8 V yielding a 5.08 GHz carrier frequency.

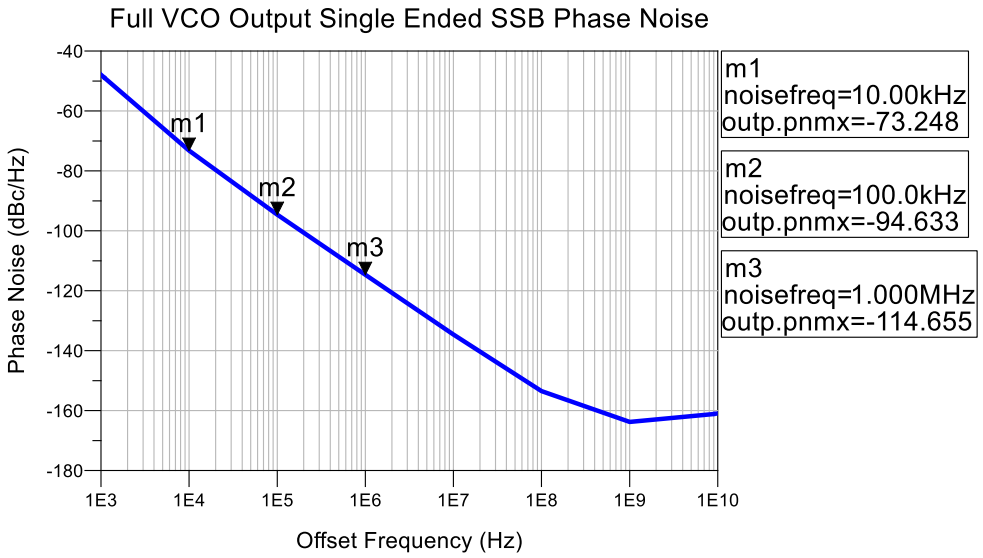


Figure 3.51: Full VCO Single-Ended, Single Side-Band Phase Noise, f_o = 5.08 GHz, V_{tune} = 10.8 V

Figure 3.52 below defines the VCO single-ended output time and frequency domain responses. The tuning voltage for this simulation is again 10.8 V, yielding a 5.08 GHz carrier.

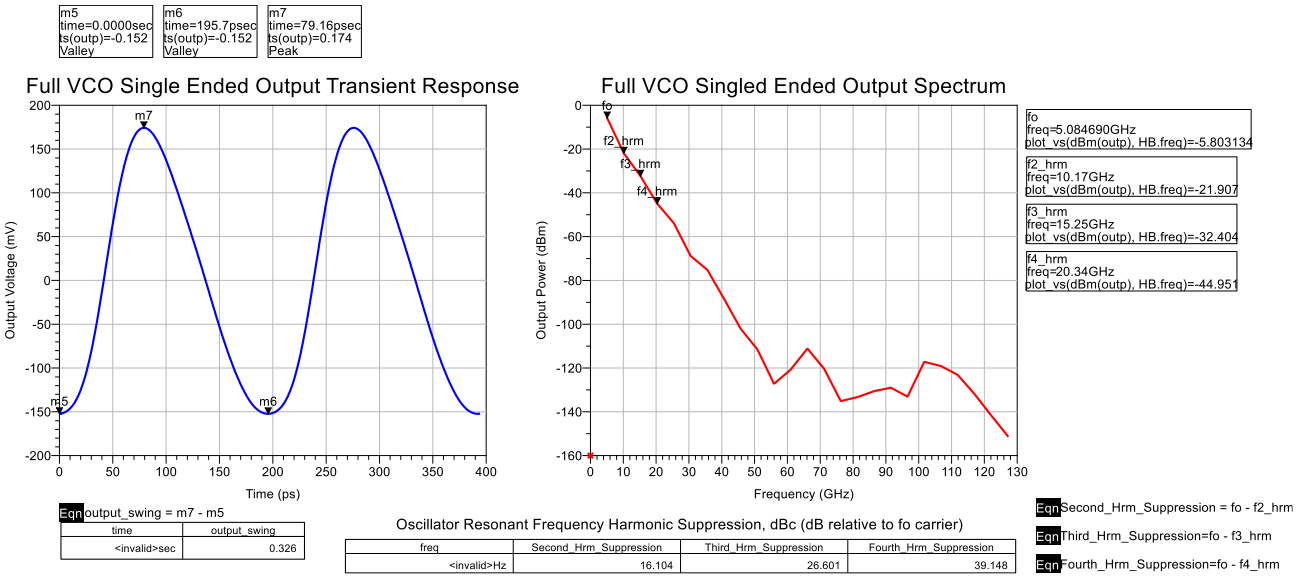


Figure 3.52: Full VCO Single-Ended Output Time and Frequency Domain Response, f_o = 5.08 GHz, V_{tune} = 10.8 V

Figure 3.53 (left/right) represent VCO stage output/input signal spectrums, outp_vco/outp_base_buffer nodes in Figure 3.50 and Figure 3.49, respectively. These spectra show the oscillator stage created signal before entering and after exiting the output buffer's capacitive divder. As expected from Section 3.8.3 analysis, the capacitive divider heavily attentuates the VCO stage's output signal before entering the output buffer stage to preserve device linearity.

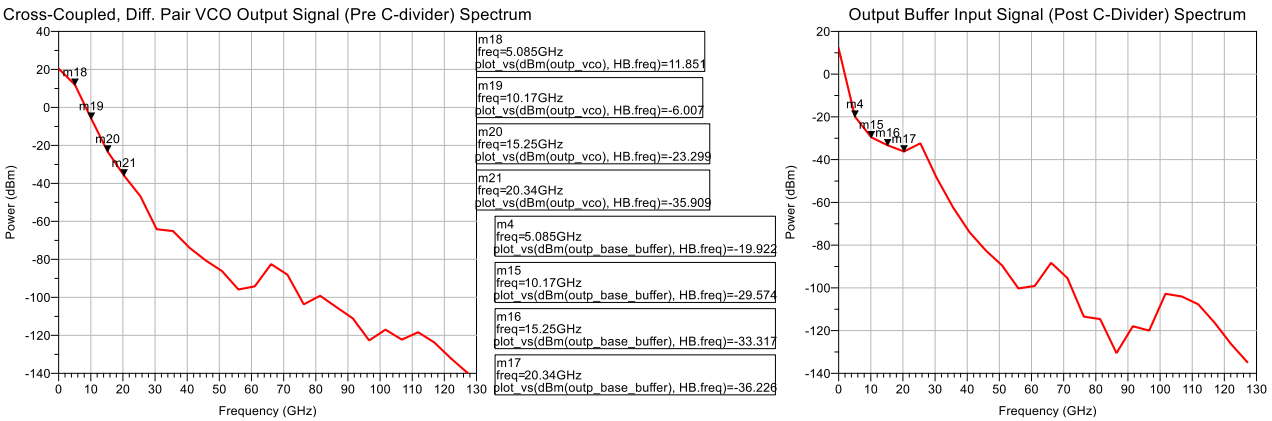


Figure 3.53: Differential Pair Output and Output Buffer Input Signal Spectra, f_o = 5.08 GHz, V_{tune} = 10.8 V

Figure 3.54 below defines the full VCO's output return loss (for each individual differential output). Note, this response matches the improved output return loss achieved by the output matching network.

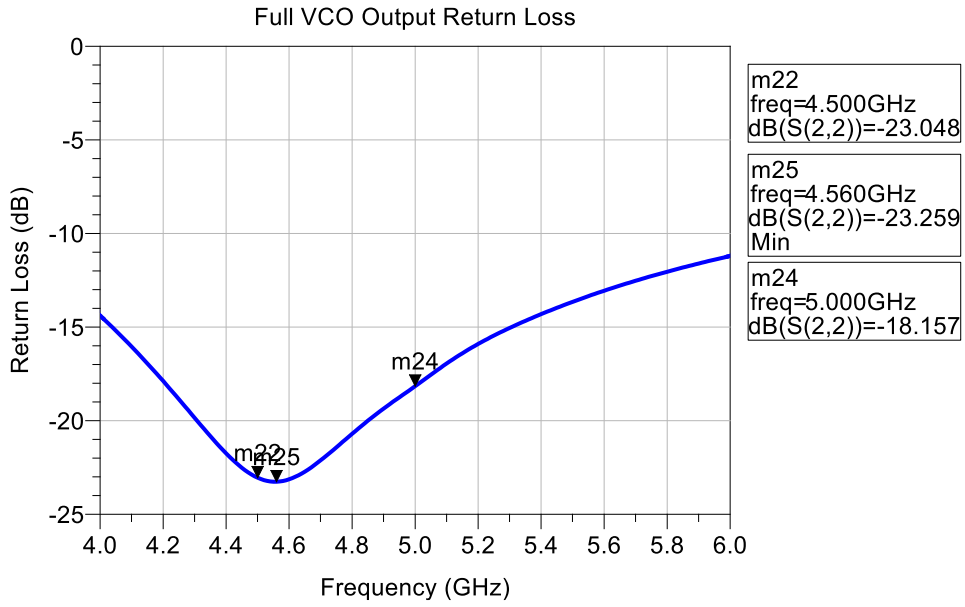
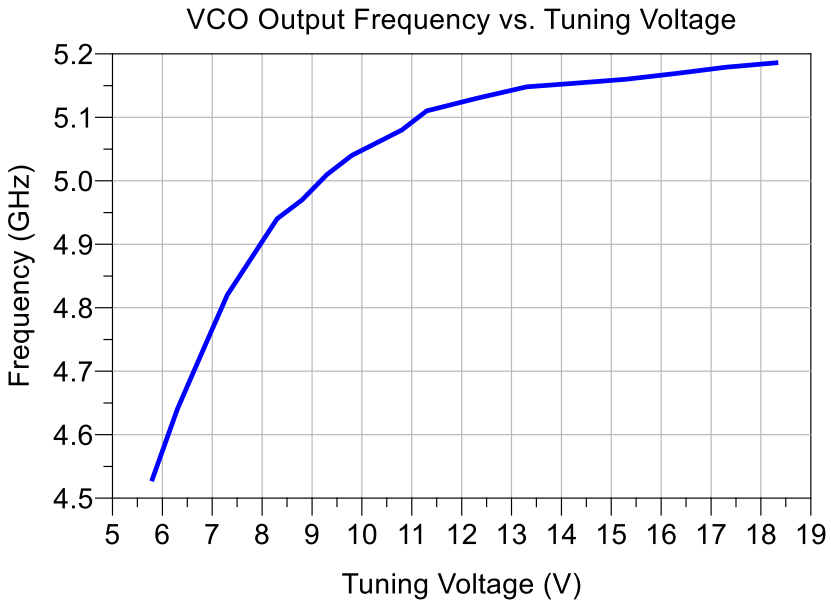


Figure 3.54: Final VCO Output Return Loss

Figure 3.55 defines the VCO output frequency (f_o) vs. tank circuit tuning voltage (V_{tune}) response. The curve begins to saturate as voltage increases, matching the varactor diode's capacitance vs. reverse voltage relationship shown in Section 3.6.3, Figure 3.21. Figure 3.55 below also reveals the schematic VCO design's tuning bandwidth (656 MHz), center frequency (4.858 GHz), and corresponding percent bandwidth (13.5%).



BW (GHz)	Fc (GHz)	P_BW (%)
0.656	4.858	13.503

Figure 3.55: Final VCO Output Frequency vs. Tuning Voltage Relation

Chapter 4

PCB DESIGN, LAYOUT, AND ELECTROMAGNETIC SIMULATION

After the schematic circuit is designed, simulated, and optimized, it is converted to a printed circuit board (PCB) layout. One of the most common, industry-standard PCB design software is Altium Designer. To simplify the layout and electromagnetic (EM) simulation and optimization process the full design is split into four sections. Keysight ADS's Momentum with Method of Moments computational electromagnetics (CEM) solver (Appendix C), electromagnetically simulates the layout. The four-layer PCB stack-up is described in Section 4.1. *Digi-Key* and *Mouser Electronics* provide the selected off the shelf components (reference Appendix D for the Bill of Materials). The following sections describe the layout, EM simulation, and re-optimization of the tank circuit, cross-coupled differential VCO core, output buffer, and current source. Finally, the VCO layout is integrated, and EM performance is compared to specifications.

4.1 PCB Layout Layer Stack-Up

The initial design's base, core dielectric material is RO4003C, a *Rogers Corp.* Laminate with a 3.38 dielectric constant and dissipation factor of 0.0027, minimizing dielectric losses. The design features four signal layers; two signal routing and two signal plane layers. Layers 2 and 3 are ground and Vcc power planes, respectively. RF microstrip traces are primarily routed on the first, top layer, however RF traces are also routed on the second layer (these traces will be discussed in Section 4.3). The fourth, bottom layer is reserved for DC tuning and control voltages. Dielectric separation

between layers 1-2 and 3-4 are both 0.11 mm height FR4 based 2116 Prepeg (PP2116) with a 4.29 dielectric constant and a 0.02 dissipation factor. Although the PP2116's dissipation factor and dielectric constant are large, the small 0.11 mm height minimizes RF dielectric losses and parasitic inductance and capacitance. A 1.2 mm height (Roger's core) separates layers 2-3. Figure 4.1 below illustrates the initial layer stack-up defined in Altium Designer.

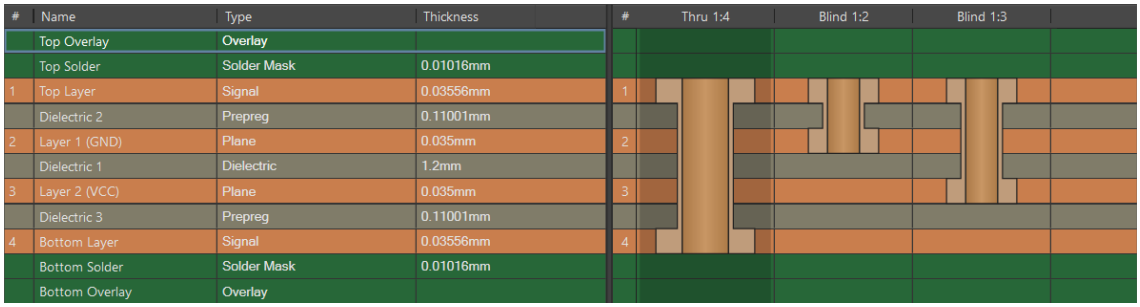


Figure 4.1: Initial Altium Designer Layer Stack-up Manager

Top layer RF traces with a ground layer directly beneath isolates sensitive RF traces from control and power traces.

Roger's core substrate is switched to FR4 core due to cost and 6-month lead time. The FR4 core has a 4.6 maximum dielectric constant and a maximum dissipation factor of 0.02. The most significant dielectric material substrate for RF traces is the PP2116, between layers 1-2, which remains unchanged. This Prepeg dielectric material creates the microstrip transmission line architecture with RF traces on layer 1 and a ground plane on layer 2. Most RF signal electric fields are within the PP2116, not the core substrate between layers 2-3. Therefore, switching the core material to FR4 reduces cost while maintaining RF signal integrity. Note, none of the layer stack-up dimensions are

modified. This updated and final layer stack-up is shown in the ADS Momentum substrate definition, Figure 4.2.

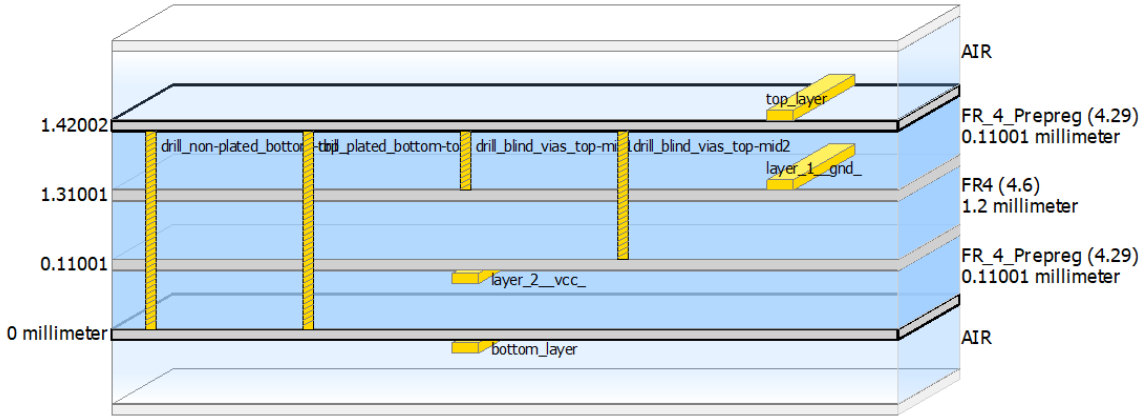


Figure 4.2: Final 4-layer FR4 PCB Stack-Up, ADS Momentum Substrate Definition

Additionally, all standard stack-up dimensions and materials are received from *PCBWay* [38], the board manufacturer and assembler. Figure 4.3 below defines the final Altium Designer Layer Stack-Up Manager, including all layout via types.

	Top Overlay	Overlay		
	Top Solder	Solder Mask	0.01016mm	
1	Top Layer	Signal	0.03556mm	1
	Dielectric 2	Prepreg	0.11001mm	
2	Layer 2 (GND)	Signal	0.035mm	2
	Dielectric 1	Dielectric	1.2mm	
3	Layer 3 (VCC)	Signal	0.035mm	3
	Dielectric 3	Prepreg	0.11001mm	
4	Bottom Layer	Signal	0.03556mm	4
	Bottom Solder	Solder Mask	0.01016mm	
	Bottom Overlay	Overlay		

Figure 4.3: Final Altium Designer Layer Stack-up Manager

Figure 4.4 defines Altium Designer layer colors for the four signal layers – applies to all discussion.

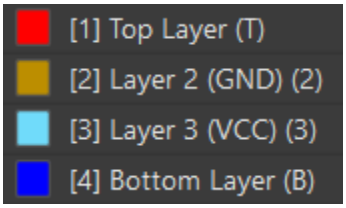


Figure 4.4: Altium Designer Layer-Color Definitions

4.2 Tank Circuit

4.2.1 Layout

The tank circuit, Figure 4.5, features 0201 chip inductors with two pairs of parallel, fixed 0402 capacitors. The varactor diodes are SOD 882 chip packages and tune from 0.466 pF to 2.4 pF [29]. The V_{tune} node, common to D1 and D2 cathodes, controls the capacitance of both varactor diodes.

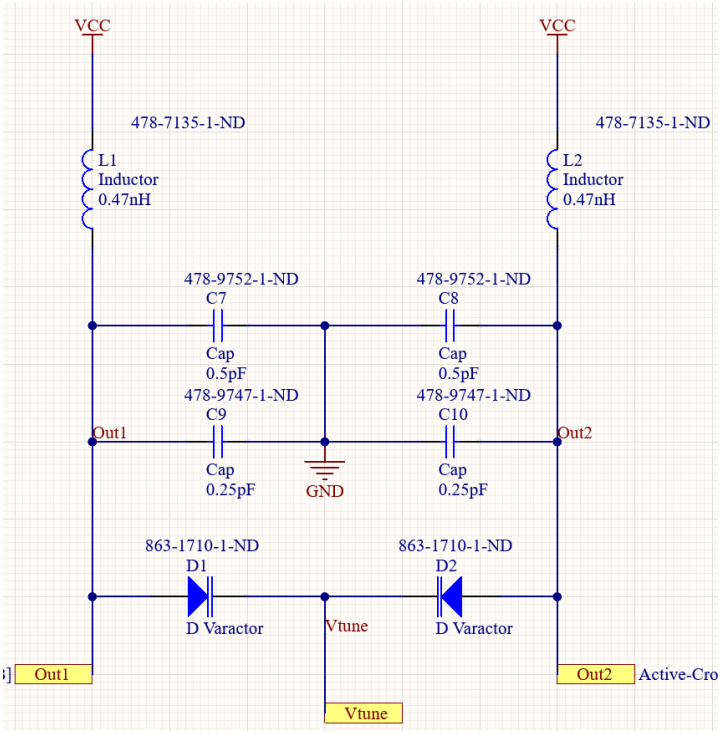


Figure 4.5: Tank Circuit Altium Schematic

The tank circuit layout, Figure 4.6, includes vias connecting ground and power planes. An additional via for V_{tune} minimizes D1 to D2 spacing and parasitics ensuring accurate resonant frequency.

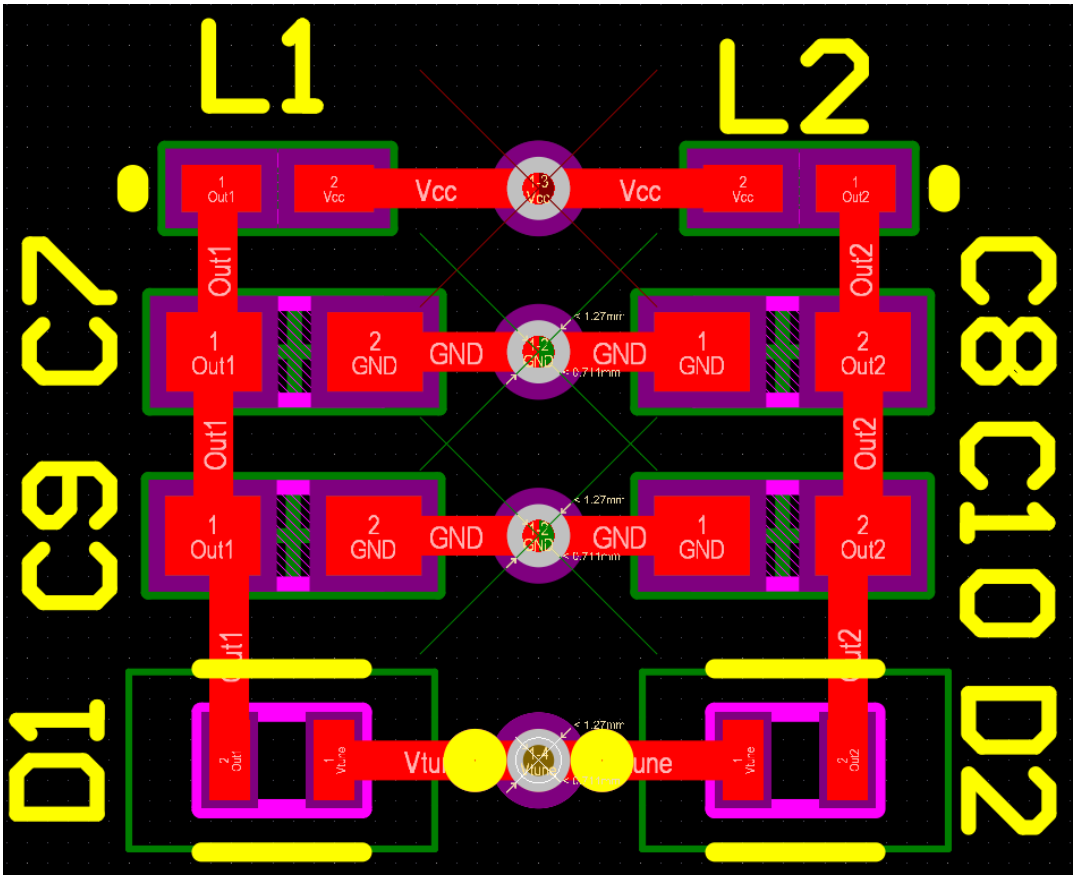


Figure 4.6: Initial Tank Circuit Altium Layout

Figure 4.7 shows rearranged capacitors C7 – C10, minimizing overall trace length and parasitic inductance. Parasitic inductance decreases tank circuit resonant frequency. A signal plane replaces traces at the shared OUT1 and OUT2 nodes, reducing parasitic inductance, but increasing parasitic capacitance.

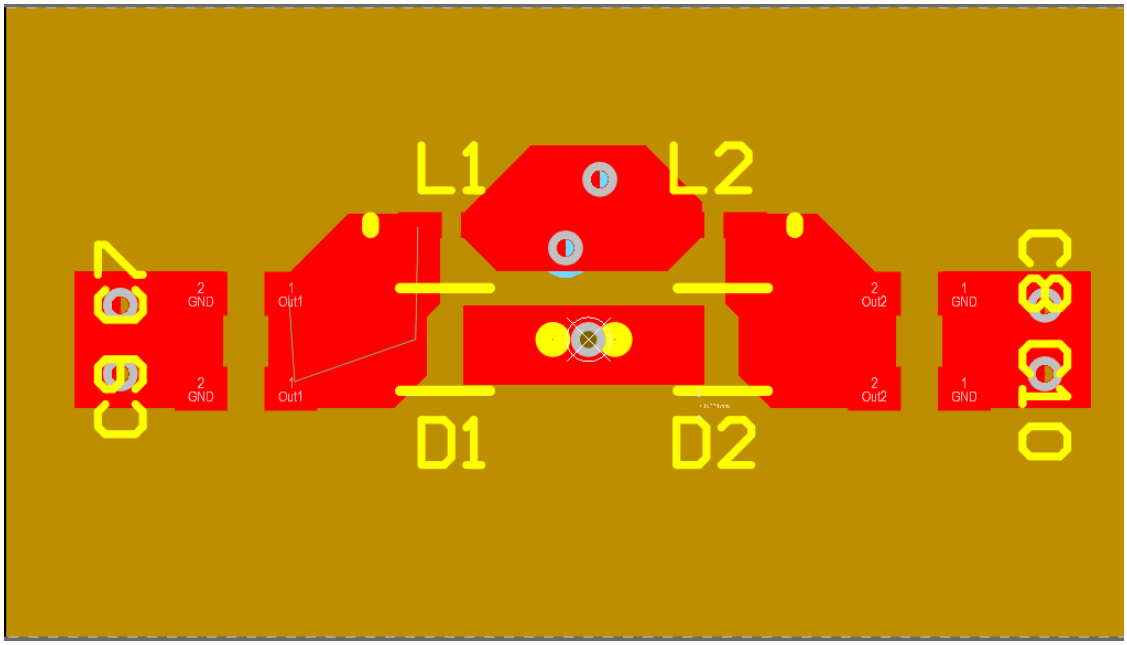


Figure 4.7: Updated Tank Circuit Altium Layout

4.2.2 Electromagnetic Simulation and Optimization

The Altium Designer Layout is converted and exported into Keysight ADS for electromagnetic simulations, Figure 4.8. A Method of Moments CEM solver is implemented with Keysight's Momentum simulator, increasing computational efficiency. The Momentum meshing frequency is set to twice the highest operating frequency, 11 GHz, and mesh density is set to 50 cells per wavelength to increase simulation accuracy. The simulation is run from DC to 11 GHz and sampled up to 151 points as shown in Figure 4.9.

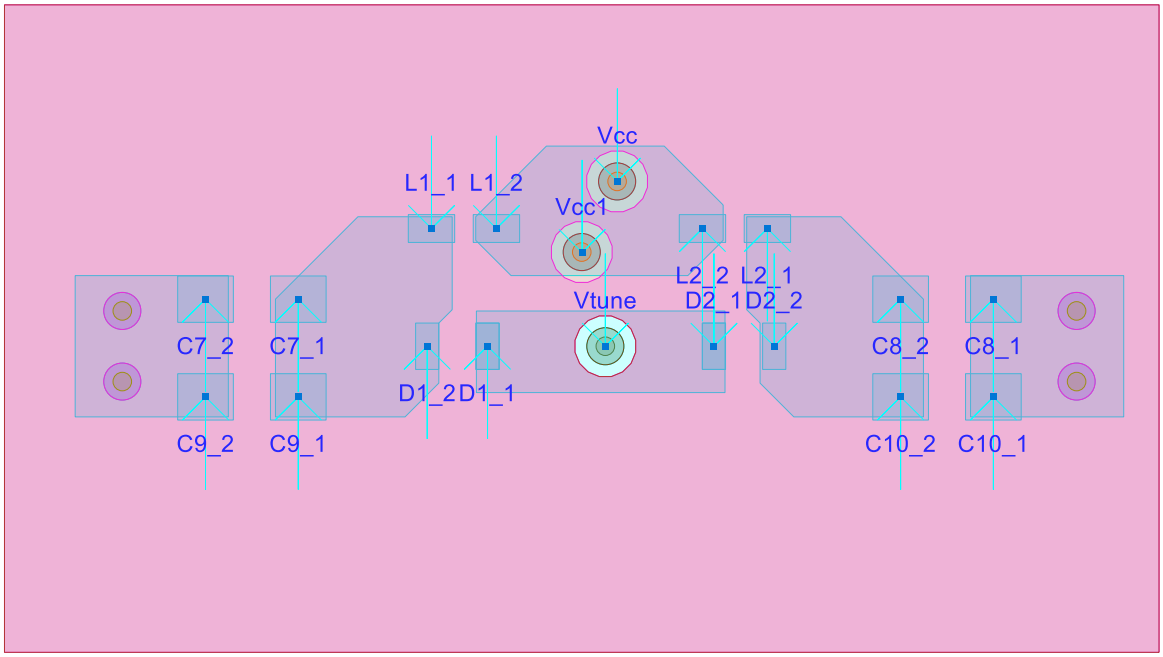


Figure 4.8: ADS MoM EM Tank Circuit Layout; OUT1, OUT2 Planes

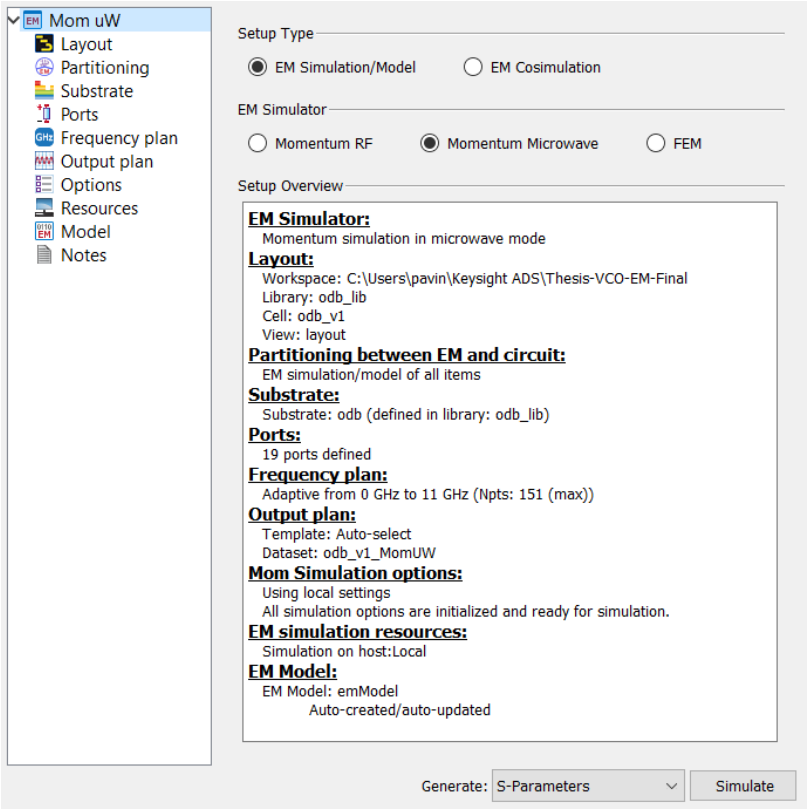


Figure 4.9: Momentum Simulator EM Setup

Figure 4.10 below shows the same circuit layout of Figure 4.8 above, but with signal traces opposed to planes at both OUT1 and OUT2 nodes. This second layout architecture is designed to compare the parasitic contribution of signal traces vs. signal planes in the tank circuit.

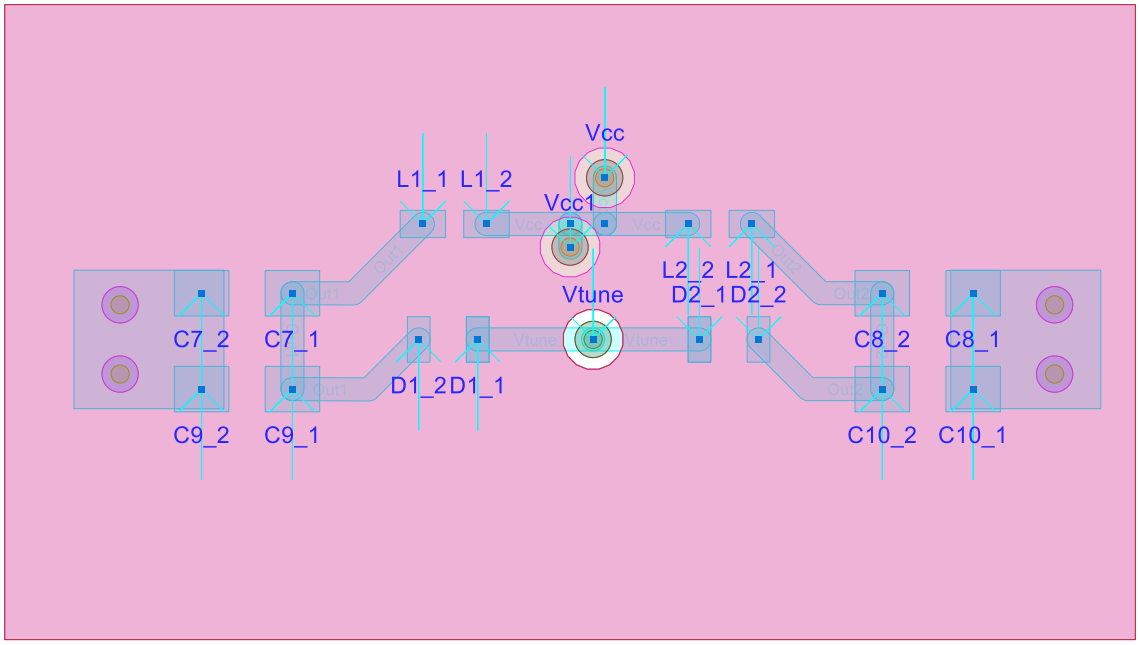


Figure 4.10: Optimized ADS MoM EM Tank Circuit Layout; OUT1, OUT2 Traces

The EM RF performance of the tank circuit, Figure 4.11, highlights the tank circuit's equivalent input susceptance and conductance for all three layout topologies shown in Figure 4.6, Figure 4.8, and Figure 4.10; representing the green Stacked_Trace_Interconnection curve, red Plane_Interconnections curve, and blue Trace_Interconnections curve, respectively.

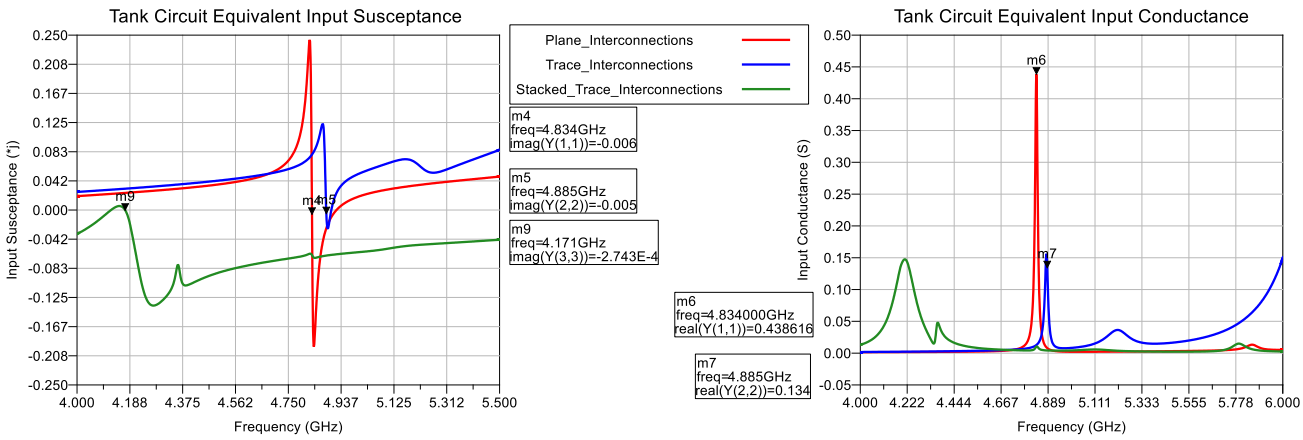


Figure 4.11: ADS Tank Circuit MoM EM RF Performance Comparison

Revised non-stacked layouts indicate a 4.8 GHz resonance, however the OUTn (n=1,2) trace layout shows a 50 MHz greater resonance than the OUTn plane layout due to reduced parasitic capacitance. The OUTn trace layout has a greater resonance frequency, but lower quality factor than the plane layout. Increased zero crossing susceptance slope increases Q. Figure 4.11 (right) shows increased Q and decreased loss for OUTn planes relative to OUTn traces due to increased conductance.

Although the OUTn trace layout has a lower quality factor, minimizing parasitic capacitance to maintain the resonant frequency is more desirable, therefore the OUTn trace layout is the final tank circuit layout architecture. Figure 4.12 integrates and co-simulates the VCO core, including both schematic based simulations (i.e., active components such as non-linear transistors) and electromagnetic simulations (i.e., passive components such as transmission lines). ADS converts the EM simulated tank circuit into an EM model. Fixed, lumped components are connected to EM excitation ports (layout pins) to enable tank circuit co-simulation with schematic-based components. The EM-

simulated, cross-coupled differential VCO core is co-simulated with non-linear, schematic-based transistors.

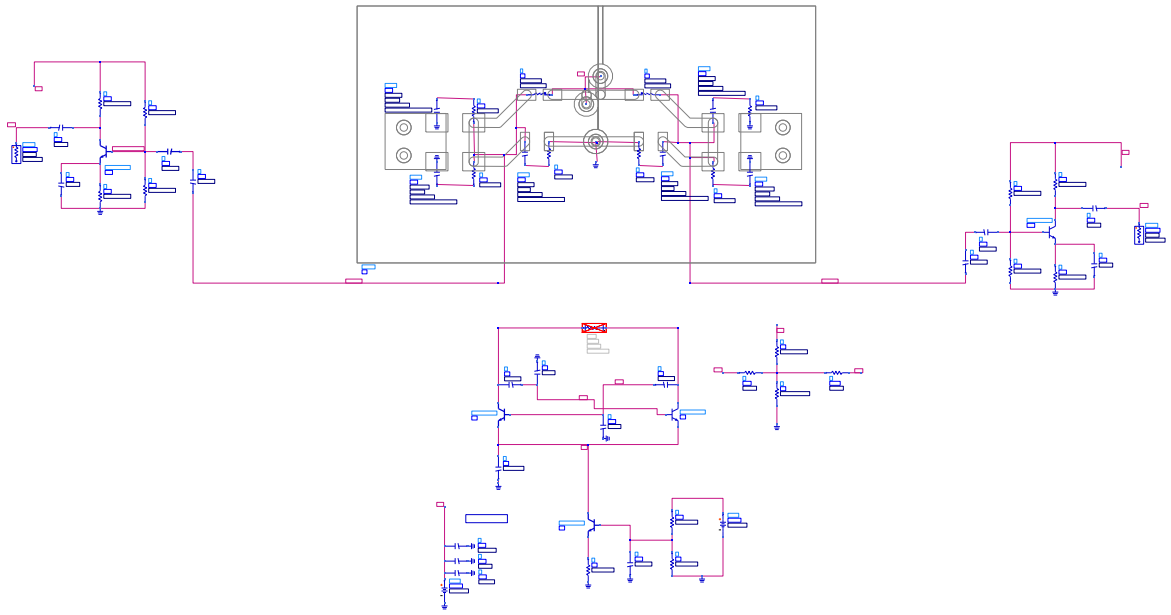


Figure 4.12: High Level ADS Full Circuit Schematic with EM Tank Circuit Co-simulation

Figure 4.13 defines the full VCO single-ended output co-simulated vs. time and frequency. Figure 4.14 defines phase noise. From Figure 4.13 tank circuit parasitics decrease the output frequency to 4.15 GHz (previously ≈ 5 GHz), at $V_{tune} = 10.8$ V. The output signal power remains at ≈ -6 dBm with harmonic suppression of 11, 38, and 40 dBc at the second, third, and fourth harmonics, respectively.

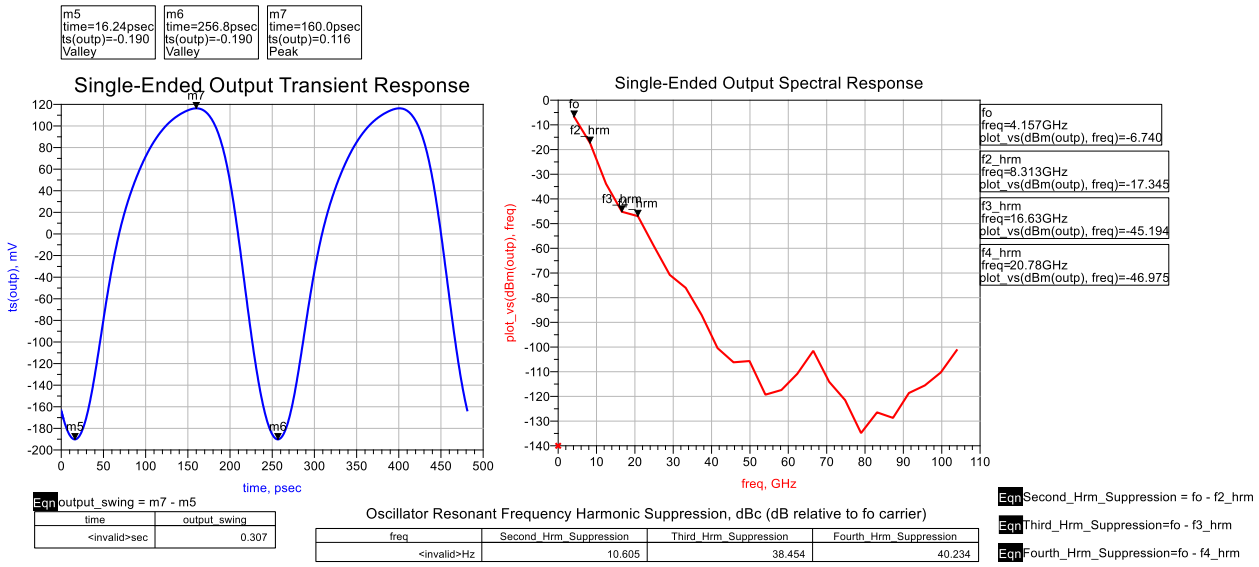


Figure 4.13: Full VCO Single-Ended Output with MoM EM Tank Circuit Co-simulation; $V_{tune} = 10.8\,V$

The phase noise simulation at a 100 kHz offset frequency decreases to -104 dBc/Hz. However, decreased carrier frequency reduces phase noise.

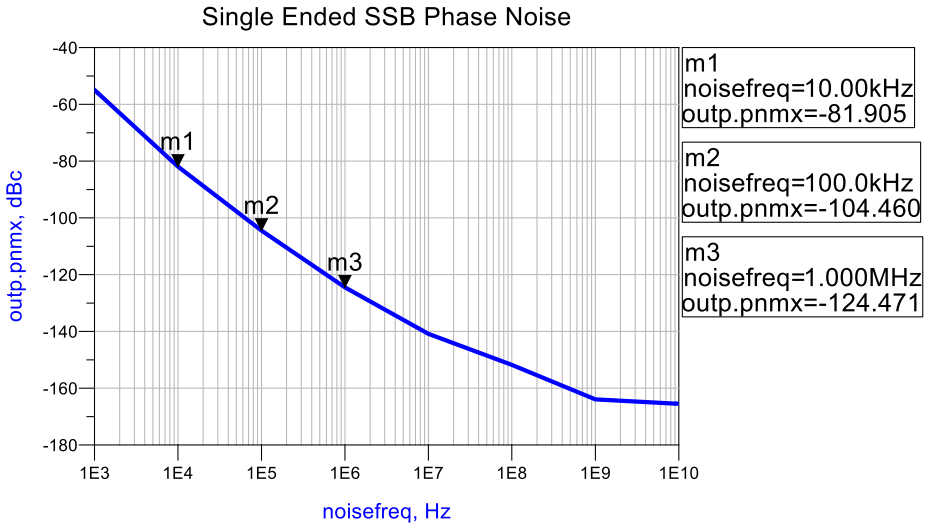


Figure 4.14: Full VCO Phase Noise with MoM EM Tank Circuit Co-simulation; $V_{tune} = 10.8\,V$

To increase oscillation frequency to 5 GHz (or as close to it as possible) at V_{tune} = 10.8 V, the 0.25 and 0.5 pF capacitors are removed; the 0.47 nH inductor is

removed and shorted. Oscillation frequency should increase. The tank circuit is now dependent on parasitic inductance and capacitance and varactor diode effective capacitance.

These modifications result in VCO oscillation frequency increasing to 4.77 GHz at V_{tune} = 10.8 V. The output power is similarly around -7 dBm and the phase noise simulates -103 dBc/Hz at a 100 kHz offset. The harmonic suppression is approximately 17, 27.6, and 24.9 dBc at the second, third, and fourth harmonics, respectively.

4.3 Cross-Coupled, Differential VCO Core

4.3.1 Layout

Figure 4.15 defines the cross-coupled, differential pair VCO core schematic in Altium Designer. Q1 and Q2 establish the cross-coupled, differential pair, with C1/C2 collector-base coupling capacitors and C3/C4 ground de-coupling capacitors. Resistors R1 through R4 establish the differential pair base bias.

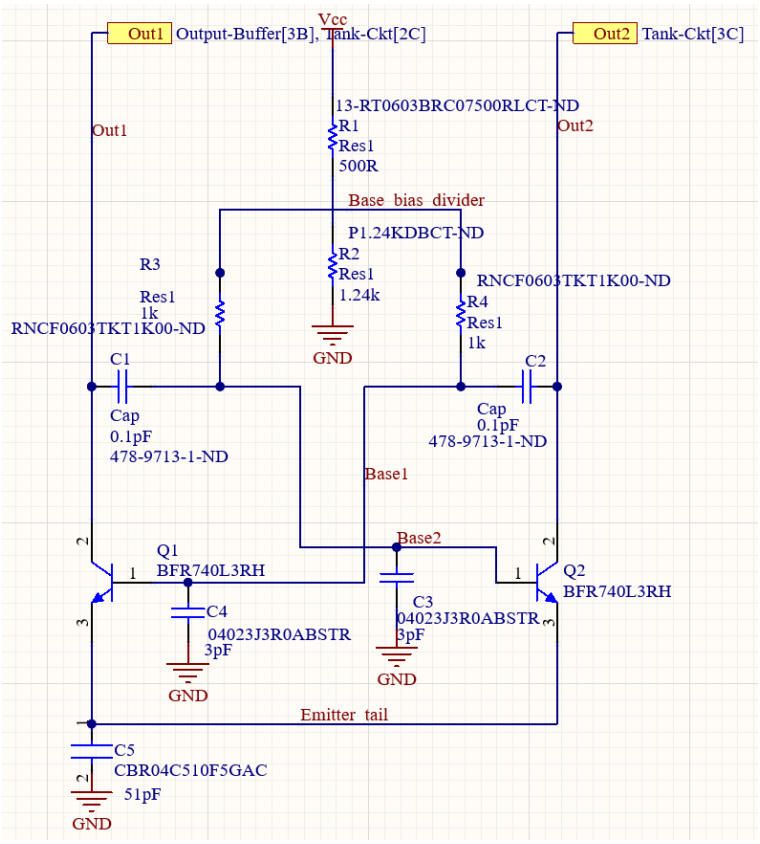


Figure 4.15: Cross-Coupled, Differential Pair VCO Core Altium Schematic

Figure 4.16 shows the initial VCO core layout with its respective base bias network (corresponds Figure 4.15 schematic). Signal traces on layers 1 and 4 are connected with 1.2 mm height vias. Layers 2 and 3 are ground and Vcc power planes, respectively. The open area between C5 and R2 is for the current source. The initial layout objective is to horizontally center all RF components. RF trace length and width are minimized to reduce parasitic line inductance and capacitance, respectively. The outer resistors R1 – R4 establish the DC base bias network while all other components are horizontally centered to minimize component spacing and parasitics.

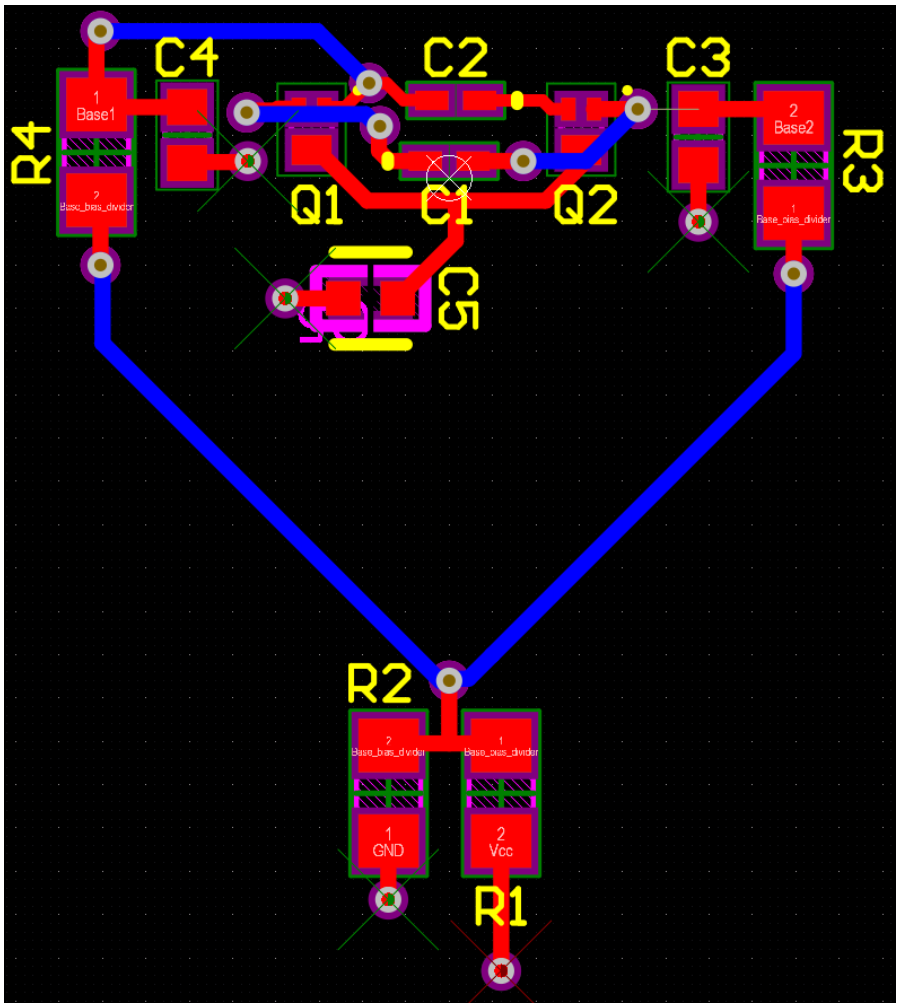


Figure 4.16: Initial Cross-Coupled, Differential Pair VCO Core Altium Layout

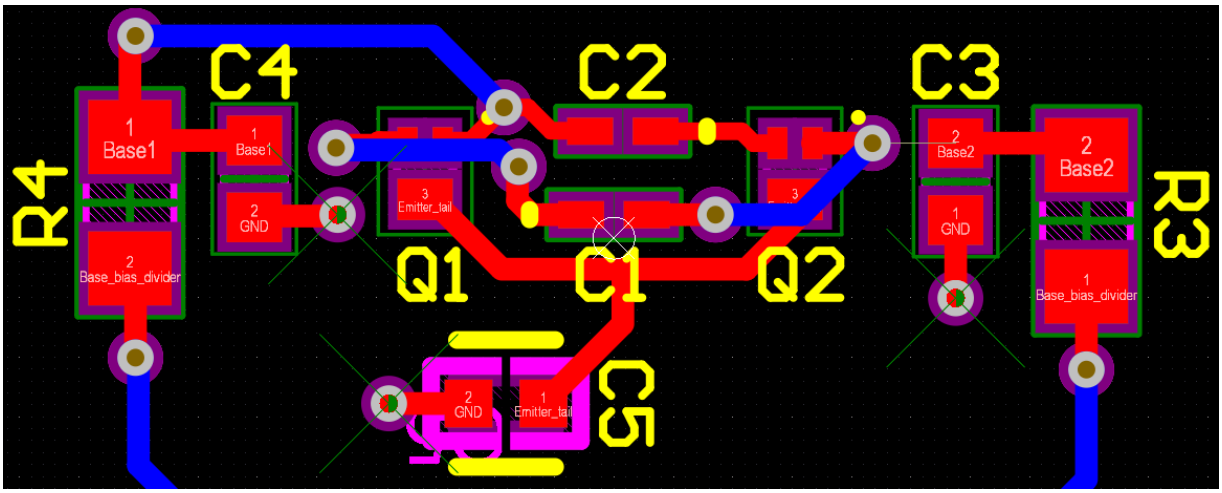


Figure 4.17: Zoomed-in Initial Core Altium Layout

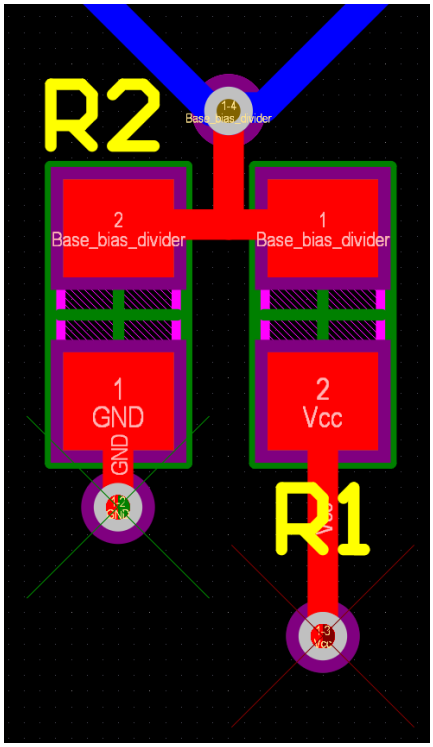


Figure 4.18: Zoomed-in Initial Core Altium Layout (Base Bias Resistive Divider)

The initial circuit layout, Figure 4.16, includes RF signal traces on layers 1 and 4. RF signal traces on layer 4 are moved to layer 2 (Figure 4.19) to minimize dielectric loss

and trace length. Layer 4 dielectric height was previously 1.32 mm causing loss. Moving RF traces to layer 2 eliminates dielectric losses since all electric fields are within the adjacent layer 2 ground plane. Additionally, trace lengths are decreased due to via height reduction from 1.2 mm to 0.11 mm, minimizing parasitic inductance.

Typically, transmission line effects are eliminated if their physical length is less than $\lambda_r/10$, where λ_r is wavelength relative to substrate dielectric constant as shown in equation (4.1).

$$\lambda_r = \frac{\lambda_o}{\sqrt{\epsilon_r}} = \frac{c}{f_o\sqrt{\epsilon_r}} \tag{4.1}$$

Using equation (4.1) above, at 5 GHz in the PP2116 dielectric between layers 1-2, $\lambda_r \approx 30$ mm. Although this layer 4 to layer 2 trace movement creates a coplanar waveguide transmission line structure in the layer 2 ground plane, trace lengths are less than $\lambda_r/15$ (2 mm), therefore coplanar waveguide transmission line effects for layer 2 RF traces are eliminated. Furthermore, all RF traces in the cross-coupled, differential VCO core layout, Figure 4.19, are less than 3 mm, or $\lambda/10$, to eliminate transmission line effects and minimize parasitic line inductance.

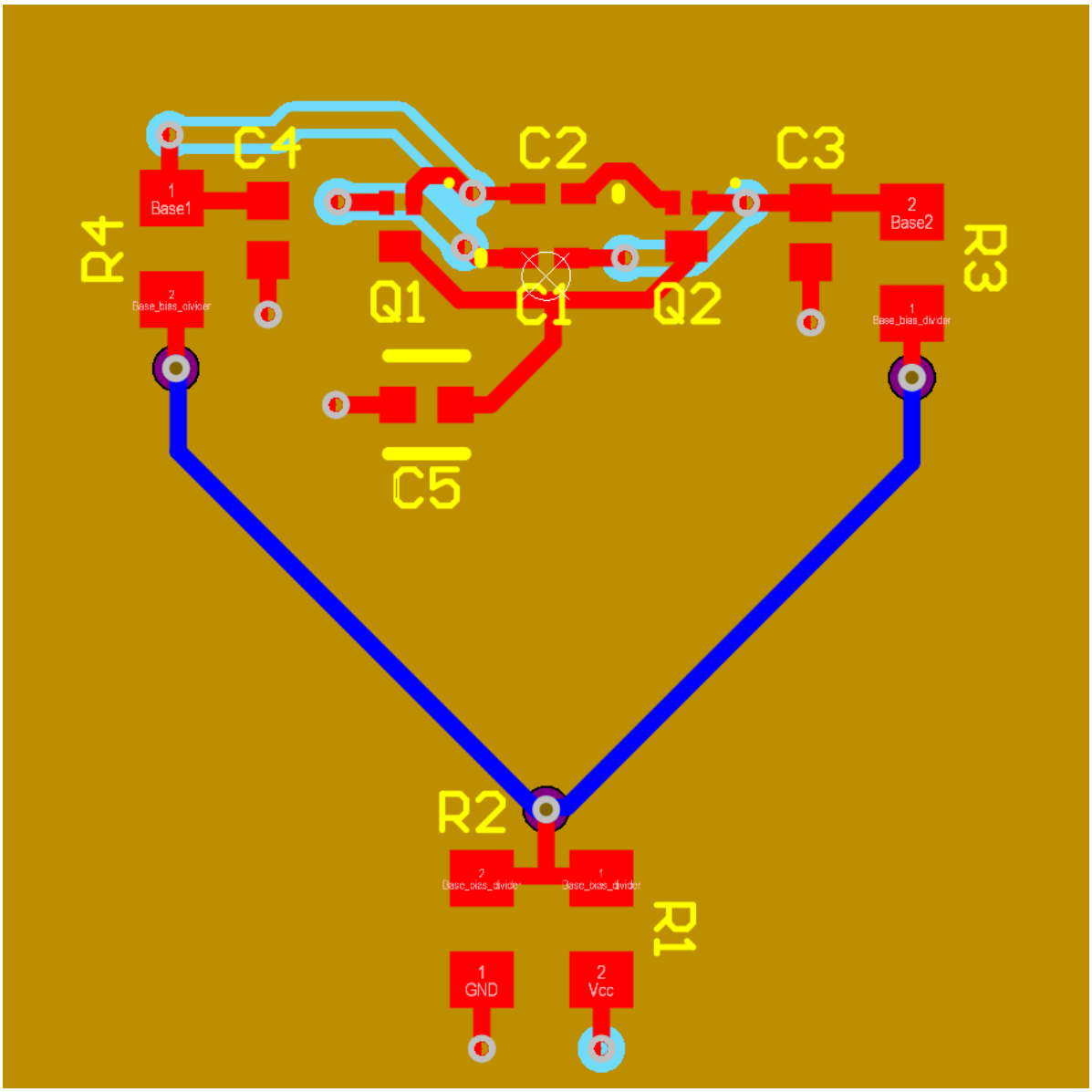


Figure 4.19: Enhanced Cross-Coupled, Differential Pair VCO Core Altium Layout

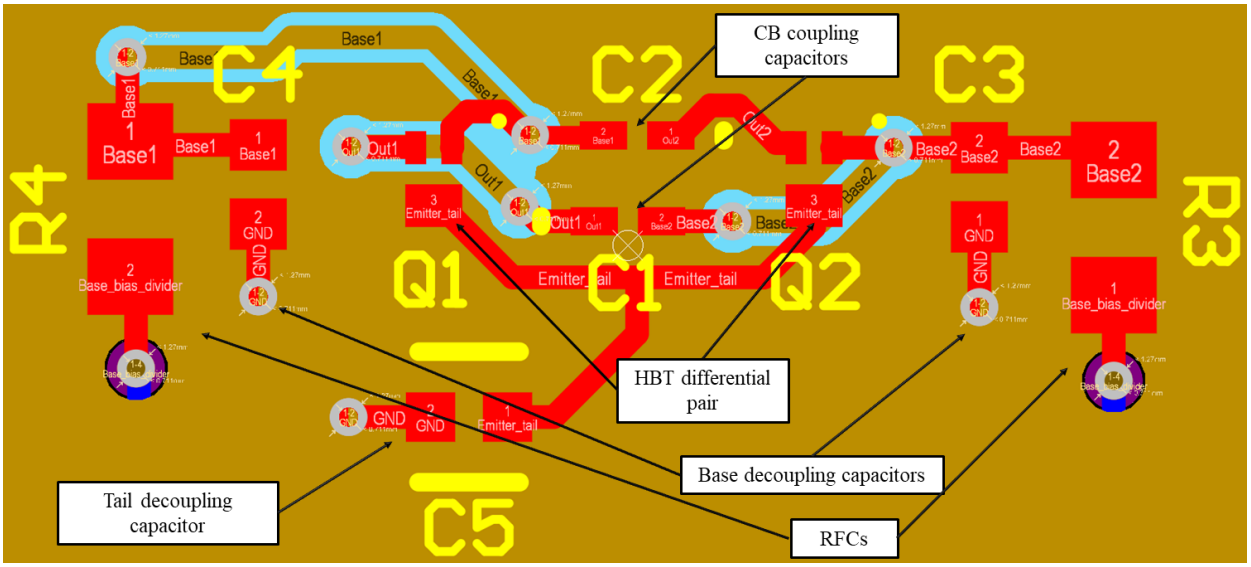


Figure 4.20: Zoomed-in Enhanced Cross-Coupled, Differential Pair VCO Core Altium Layout

4.3.2 Electromagnetic Simulation and Optimization

Following tank circuit simulations, 50 cells per wavelength meshing density and 11 GHz meshing frequency are used for Momentum simulation. Figure 4.21 below illustrates the VCO core layout imported into Momentum.

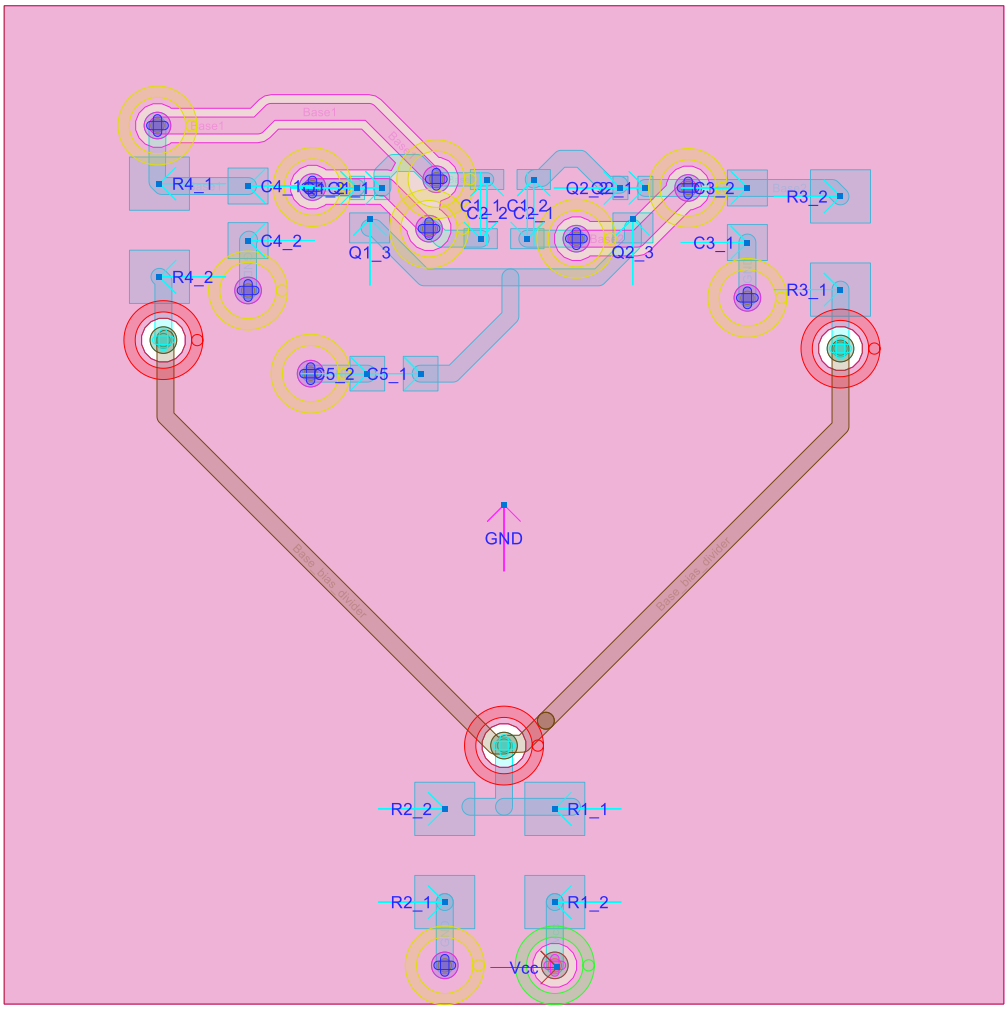


Figure 4.21: Cross-Coupled, Differential Pair VCO Core ADS Momentum Layout

Figure 4.23 below shows the same VCO core layout with cell meshing. Pins are placed at each component's pad serving as EM excitations ports. A Vcc pin at the bottom via connects to the power supply. The layer 2 plane (centered GND pin) defines the primary ground reference for VCO core EM simulations.

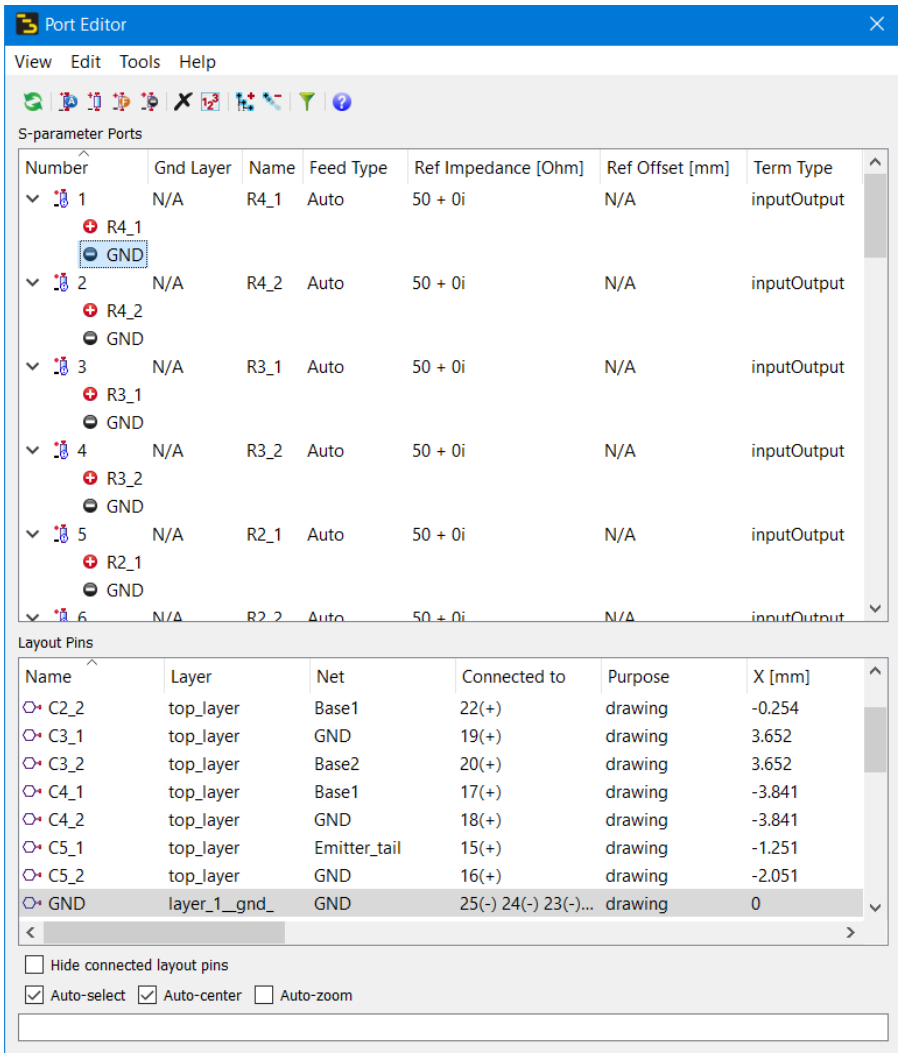


Figure 4.22: Cross-Coupled, Differential Core ADS Layout MoM EM Pin Editor

In defining EM excitation ports, either a conductive layer is selected as the Gnd Layer or a reference pin is defined as a port's negative terminal, see Figure 4.22. For the cross-coupled core layout, although layer 2 is primarily a ground plane, it includes several RF traces. If layer 2 is selected as the Gnd Layer in all Port Editor pin/port definitions, layer 2 shorts all RF traces to ground. Therefore, the GND pin is placed in the center of the layer 2 plane, isolating the layer 2 RF traces and ground plane.

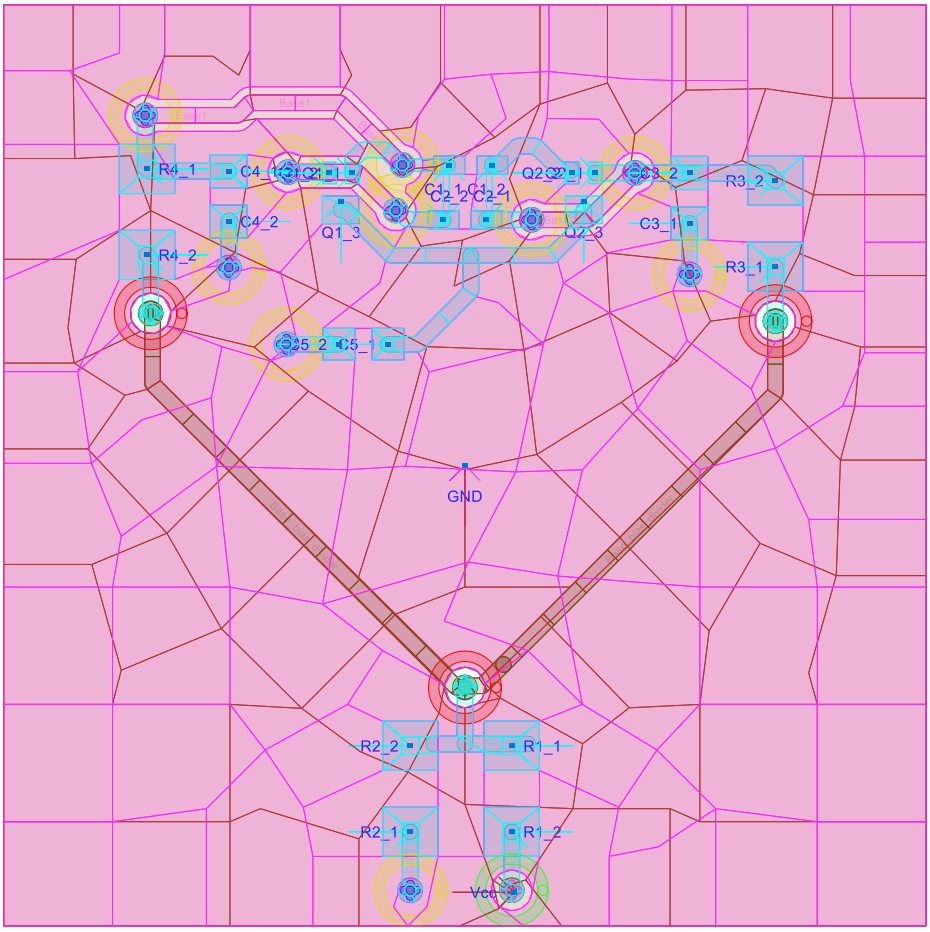


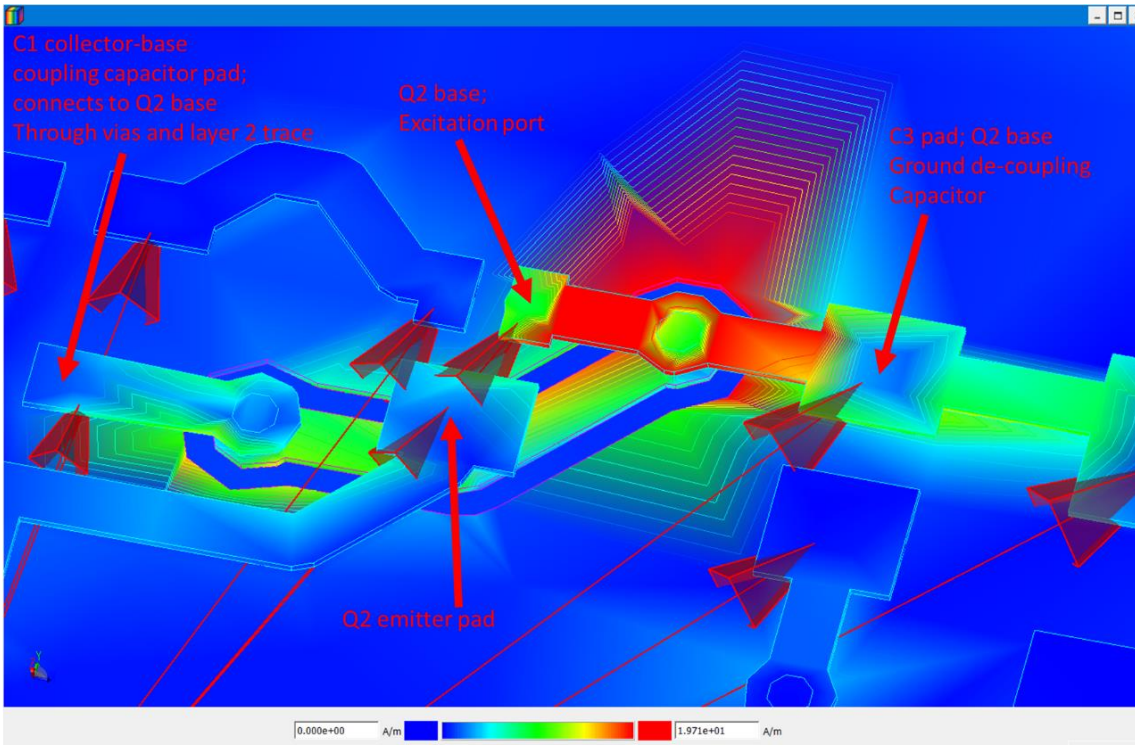
Figure 4.23: Cross-Coupled, Differential Pair VCO Core Momentum Cell Meshing

A powerful tool of an electromagnetic simulator is its ability to capture and view surface current densities and electromagnetic fields; this is the fundamental theory of Method of Moments CEM solver. Momentum can visualize EM simulated surface current densities.

This visualization property can determine transmission line effects. As previously mentioned, transmission line effects are eliminated for lengths less than $\lambda_r/10$. If the trace acts as a transmission line, AC surface current becomes a travelling wave, propagating along the trace. Therefore, if the applied cosine's phase shift is at 90° (0 magnitude), there will still be surface current present, travelling along the line. However, if trace

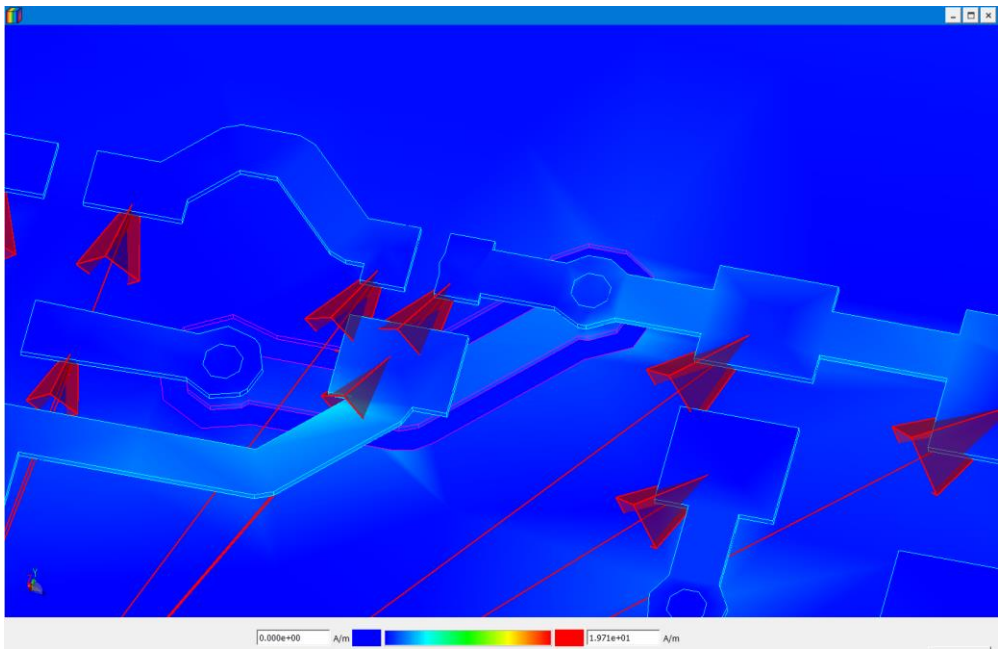
length is insufficient to cause transmission line effects, constant magnitude AC surface current standing waves exists along the line. This theory and simulation verifies transmission line effects are eliminated from all core layout traces, as intended.

Figure 4.24 below shows a 5.09 GHz signal applied to the Q2 base pad, where a 2.7 mm, $\lambda/11$ trace length exists ($\lambda_r \approx 30$ mm).

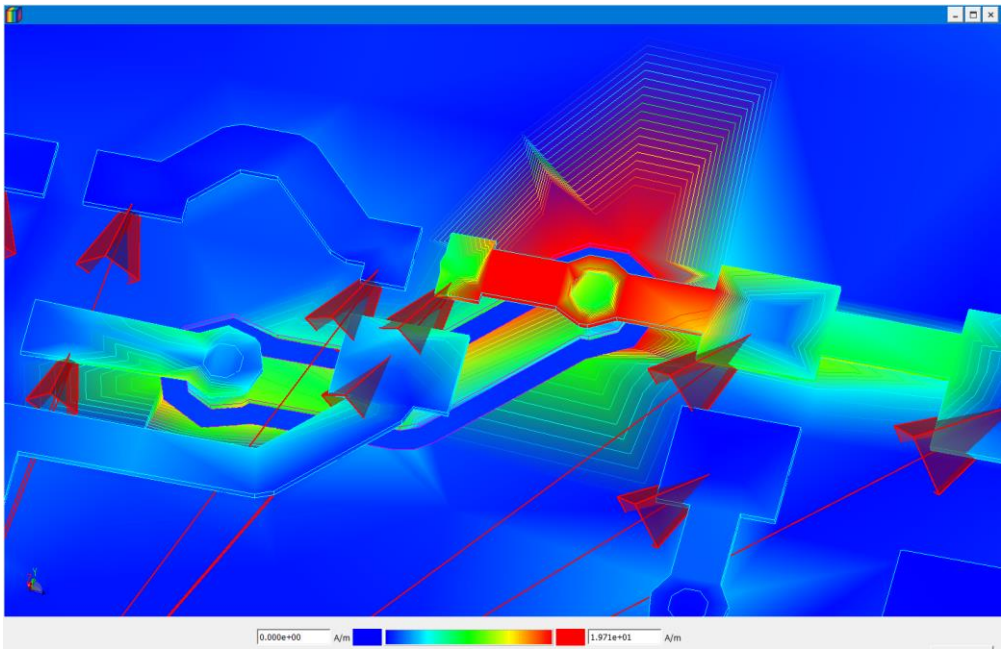


(a) 0°-Phase Shift Excitation Signal

Figure 4.24: 5.09 GHz Excitation Surface Current at Q2 Base Pad; Multiple Excitation Signal Phase Shifts; Trace Electrical Length $\approx \lambda/11$



(b) 90°-Phase Shift Excitation Signal



(c) 180°-Phase Shift Excitation Signal

Figure 4.24: 5.09 GHz Excitation Surface Current at Q2 Base Pad; Multiple Excitation Signal Phase Shifts; Trace Electrical Length $\approx \lambda/11$

Figure 4.24 (a) and (c) show identical responses. 0° and 180° phase-shifted signals are applied; maximum surface current density flows along the entire trace. Figure 4.24 (b) response shows a 90°-phase shifted signal applied at the excitation port. As expected, minimum (near-zero) current density magnitude appears along the entire trace. This verifies that the RF trace exhibits no transmission line effects at 5.09 GHz.

To demonstrate transmission line effects, an 11 GHz, 90°-phase shifted signal is applied to the same Q2 base pad of Figure 4.24. At 11 GHz, $\lambda_r \approx 13$ mm and the trace's electrical length becomes $\approx \lambda/5$. Transmission line effects should now be apparent and, in contrast to Figure 4.24 (b), surface current should be observed along the trace. Figure 4.25 below illustrates this response and confirms the expected theory.

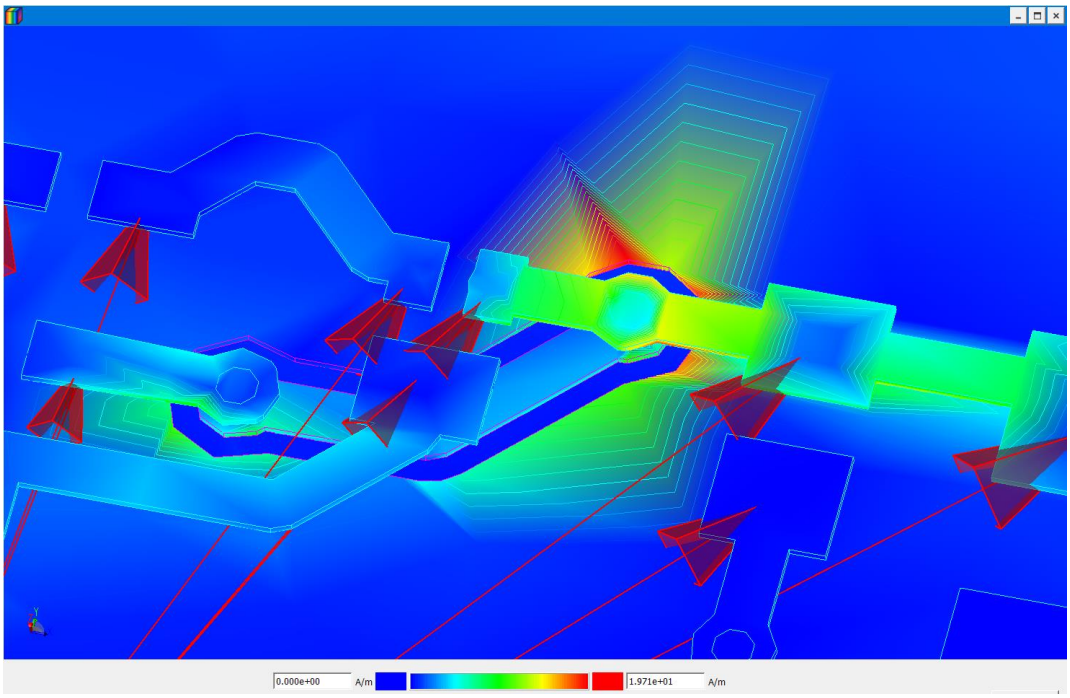


Figure 4.25: 11 GHz, 90°-Phase Shift Excitation Surface Current at Q2 Base Pad; Trace Electrical Length $\approx \lambda/5$

After the cross-coupled core's layout is initially EM simulated, the full VCO circuitry is co-simulated. The negative conductance oscillation condition is not satisfied; hence, the oscillator does not start up.

It is discovered the core's input conductance becomes more negative moving from 4 GHz to 5 GHz. Increasing the collector-base coupling capacitor directly helps improve the negative input conductance condition by adding more negative series reactance to the cross-coupled feedback paths. Figure 4.26 below shows how increasing the collector-base coupling capacitor improves the negative conductance oscillation condition. Note, the equivalent input capacitance also increases.

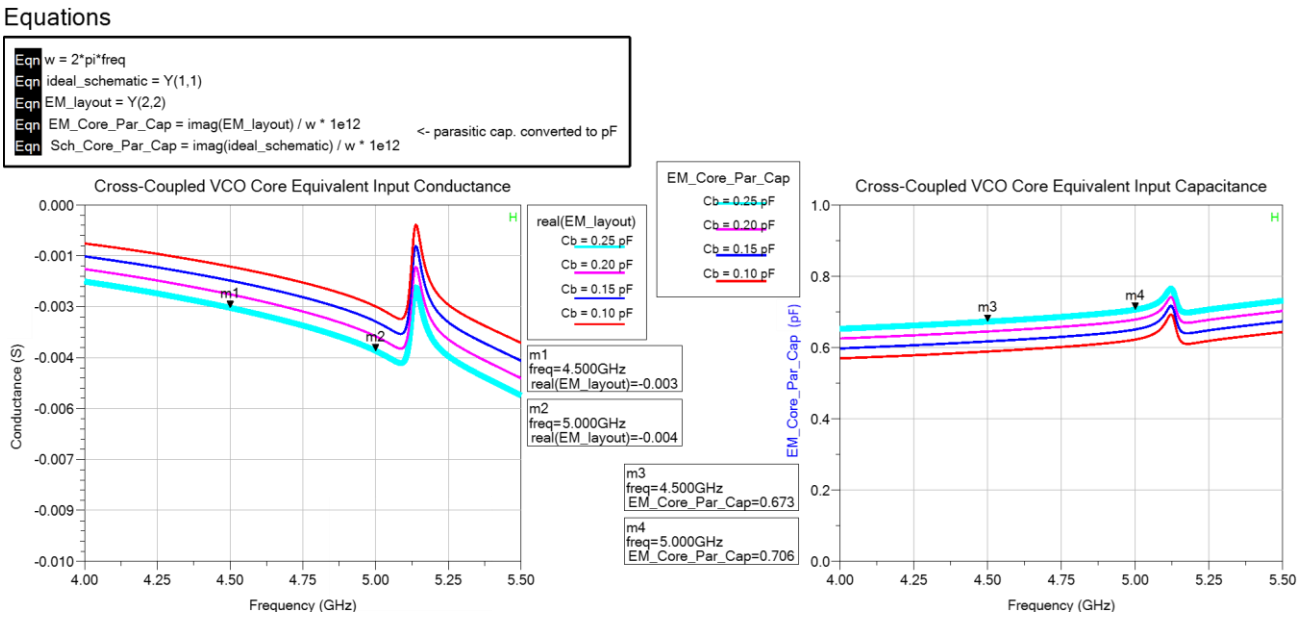


Figure 4.26: Cross-Coupled VCO Core Equivalent Input Conductance and Capacitance; Varying Collector-Base Coupling Capacitor from 0.1 pF to 0.25 pF

Figure 4.27 below defines the updated cross-coupled, differential VCO core Altium Schematic, with tuned 0.25 pF feedback, coupling capacitors (C1, C2).

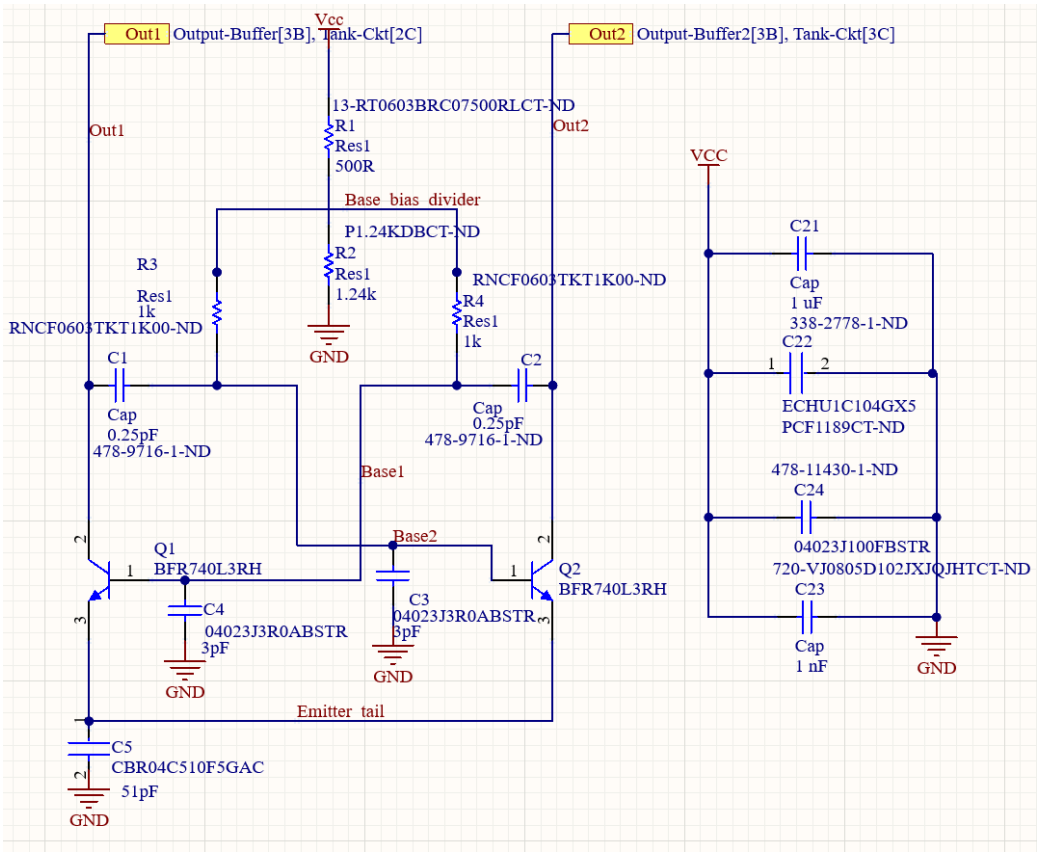


Figure 4.27: Updated, Final Cross-Coupled, Differential VCO Core Altium Schematic

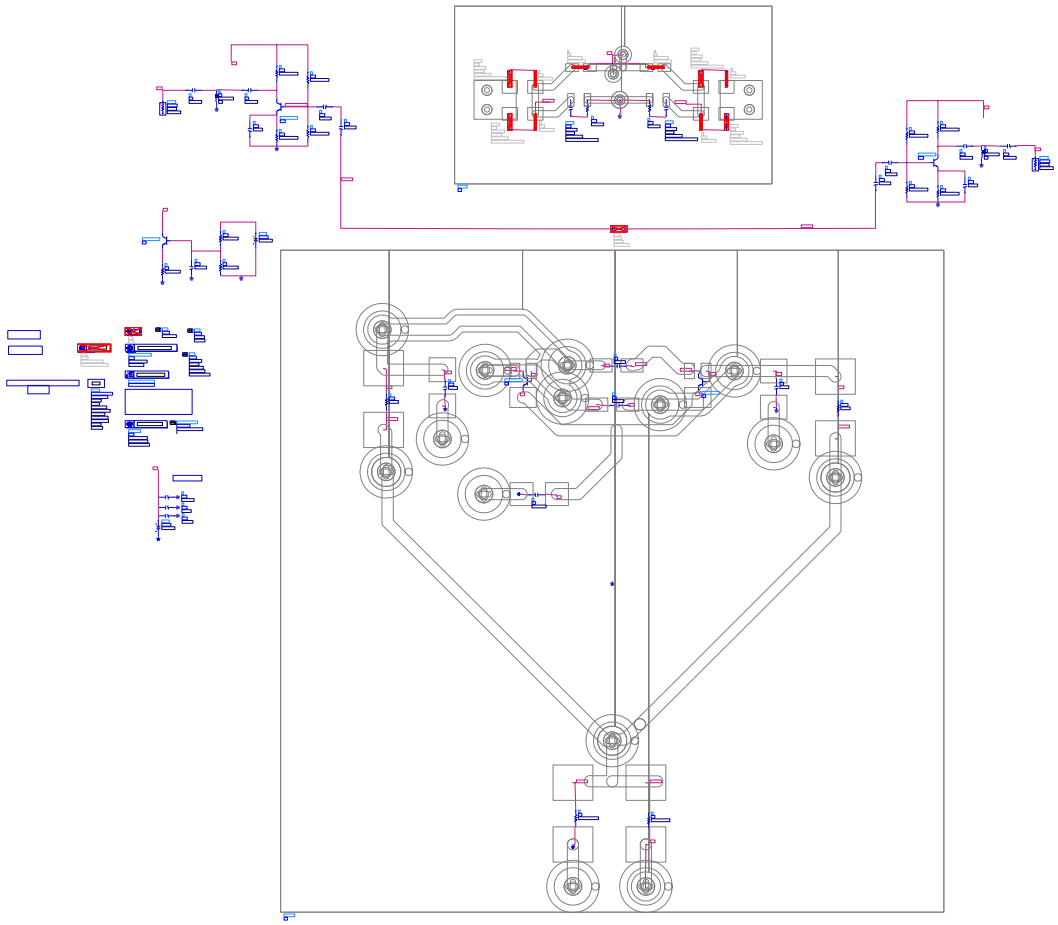


Figure 4.28: Top-Level ADS Full Circuit Schematic with EM Tank Circuit and EM VCO Core Co-simulation

The Figure 4.28 complete design co-simulation results in the VCO oscillation frequency decreasing to 4.4 GHz with V_{tune} = 18.3 V. The output power simulates ≈ -6.6 dBm with a phase noise of -98.1 dBc/Hz at a 100 kHz offset. The harmonic suppression measures approximately 16.6 dBc, 20.6 dBc, and 28.9 dBc at the second, third, and fourth harmonics, respectively.

4.4 Current Source

4.4.1 Layout

Figure 4.29 below defines the current source design Altium schematic. The 100 Ω emitter resistor, R7, increases the current source's output impedance, ensuring the differential pair tail node does not become loaded. Resistors R5 and R6, 18 kΩ and 91 kΩ, create a resistive divider, setting the 2 V base bias voltage. The 1 nF ground de-coupling capacitor, C6, eliminates noise from the DC bias control voltage, V_current_sink.

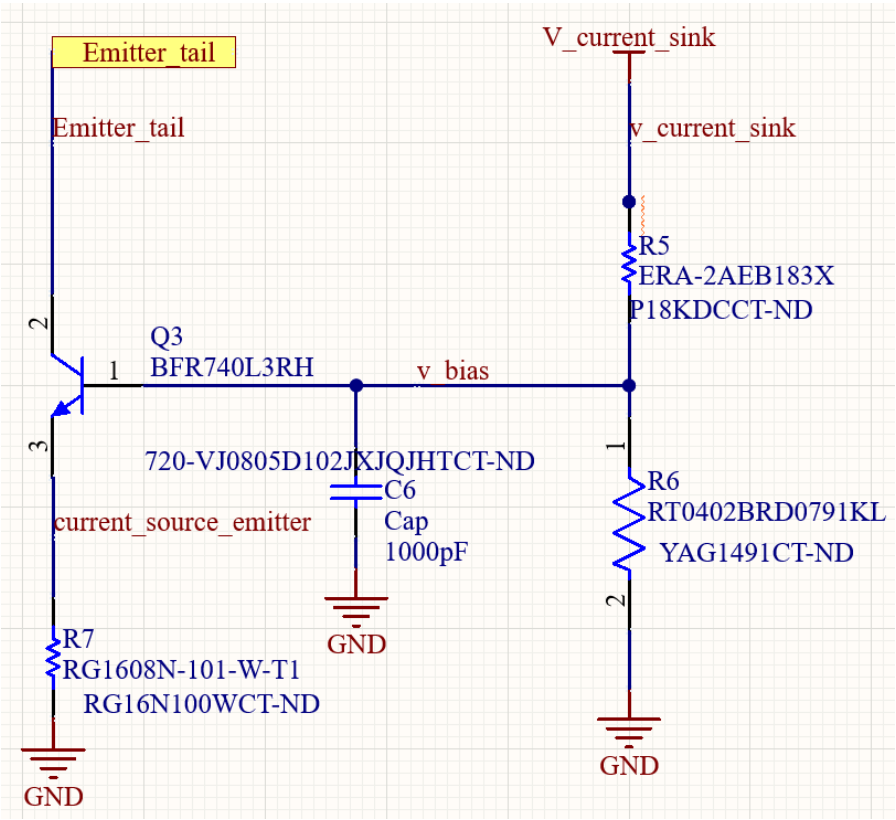


Figure 4.29: Current Source Design Altium Schematic

Figure 4.30 below illustrates the current source layout. R5, R6, and C6 are all 0402 SMT packages while R7 is a 0603 SMT package.

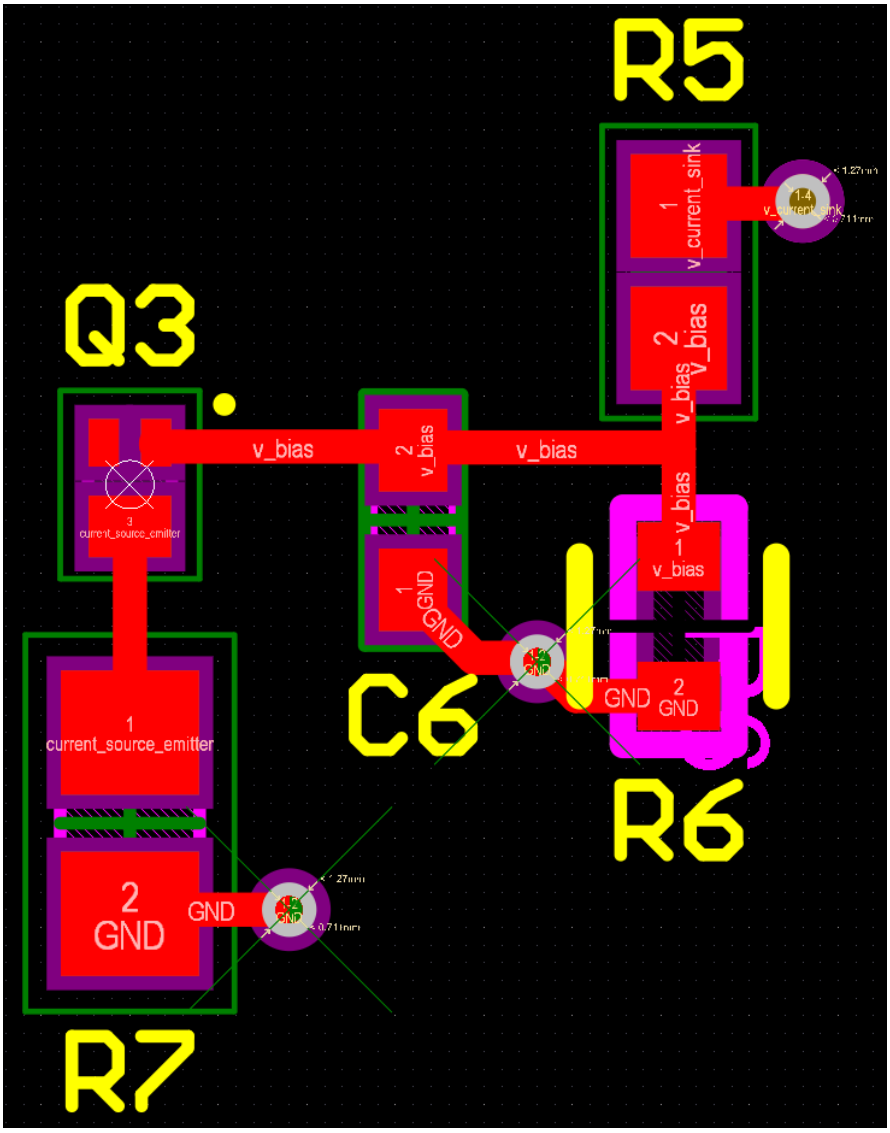


Figure 4.30: Initial Current Source Design Altium Layout

The updated current source layout (Figure 4.31) minimizes inter-component spacing and board area. R5 is rotated 90° to minimize spacing. C6 and R6 have separate ground vias and R7 has an additional ground via. These via modifications increase ground continuity, minimizing potential ground loops and random I-V fluctuations, per Section 2.4.2.

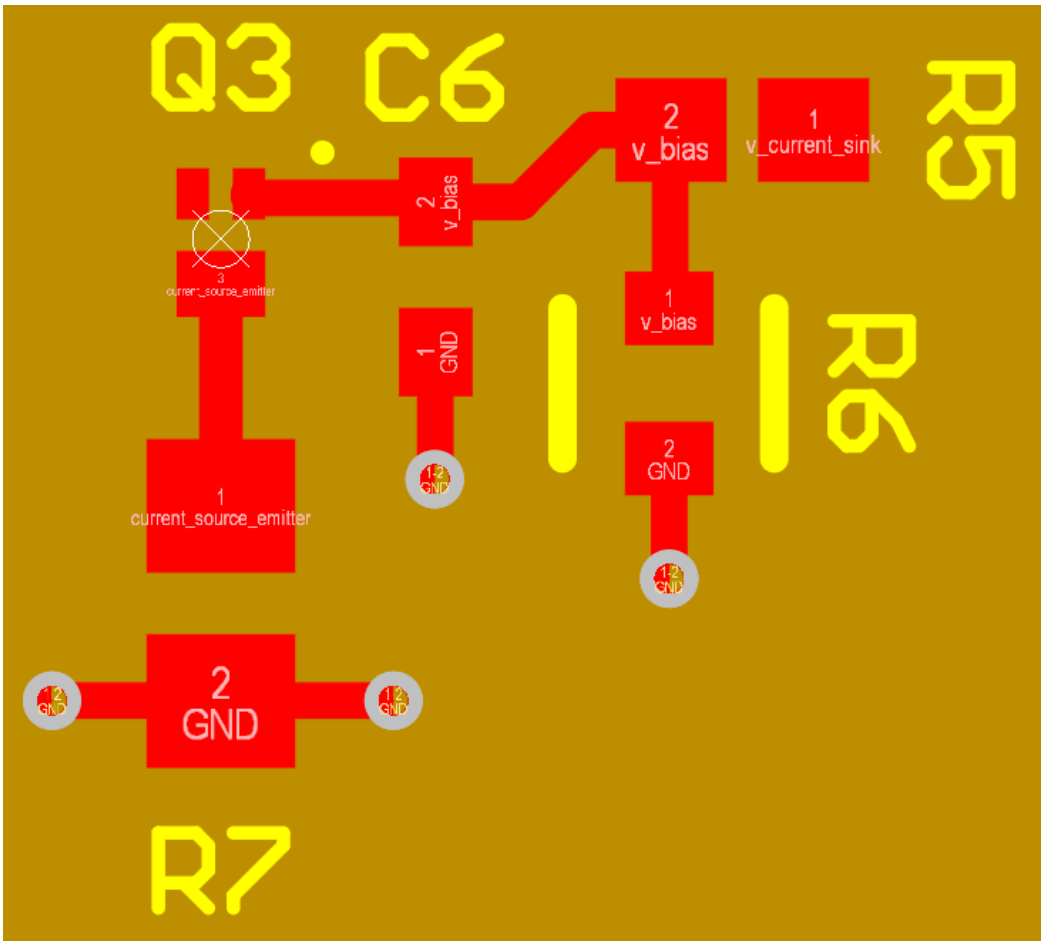


Figure 4.31: Updated, Final Current Source Altium Layout

4.4.2 Electromagnetic Simulation and Optimization

Although the current source is a DC circuit, it is still EM simulated. The final current source design is converted and imported into ADS, Figure 4.32.

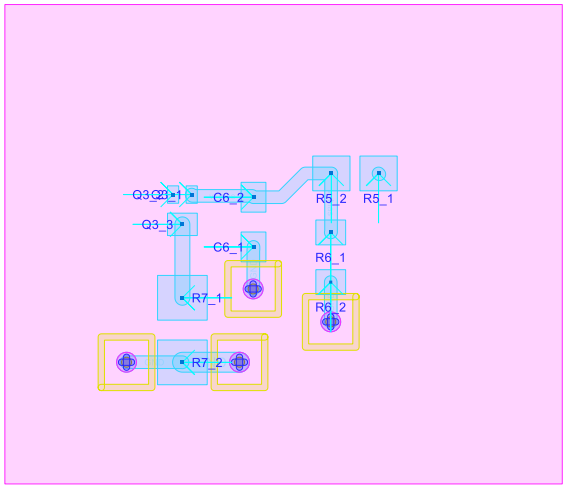


Figure 4.32: Final Current Source Design ADS Momentum Layout

Figure 4.33 below illustrates the top-level schematic co-simulation setup with EM models for the tank circuit, cross-coupled differential core, and current source. The co-simulation confirms the EM simulated current source model has negligible effects on VCO RF performance.

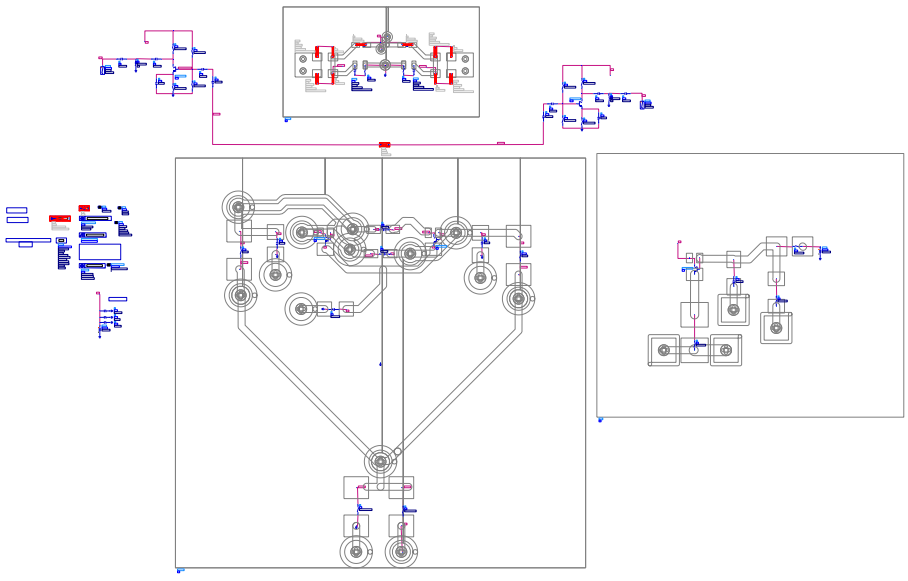


Figure 4.33: Top-Level ADS Full Circuit Schematic with EM Tank Circuit, EM VCO Core, and EM Current Source Co-simulation

4.5 Output Buffer

4.5.1 Layout

Figure 4.34 below defines the output buffer schematic design in Altium Designer. Resistors R8 – R11 establish the DC bias network and are all 0402 SMT resistors. Additionally, C14 is an 0402 SMT chip capacitor. Capacitors C11, C12, C13, and C15 are all 0201 SMT packages, minimizing ESR and maximizing both quality factor and SRF. Inductor L3 is the same 0201 fixed inductor in the tank circuit (high-Q and SRF). The HBT is the same TSLP-3-9 SMT package BFR used in current source and differential pair designs.

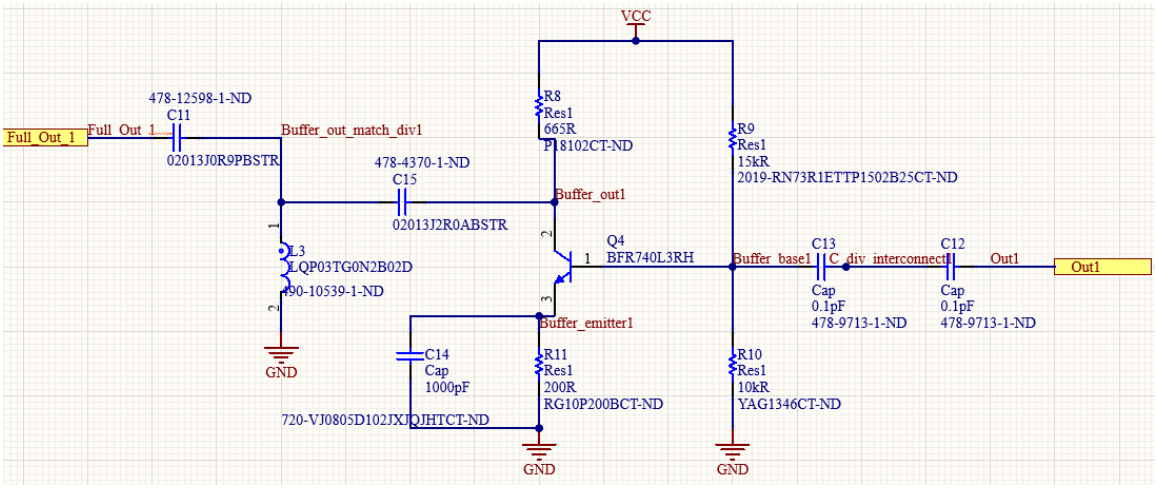


Figure 4.34: Output Buffer Altium Schematic

Figure 4.35 below shows the output buffer layout. Note, C15, L3, and C11 establish the output matching T-network.

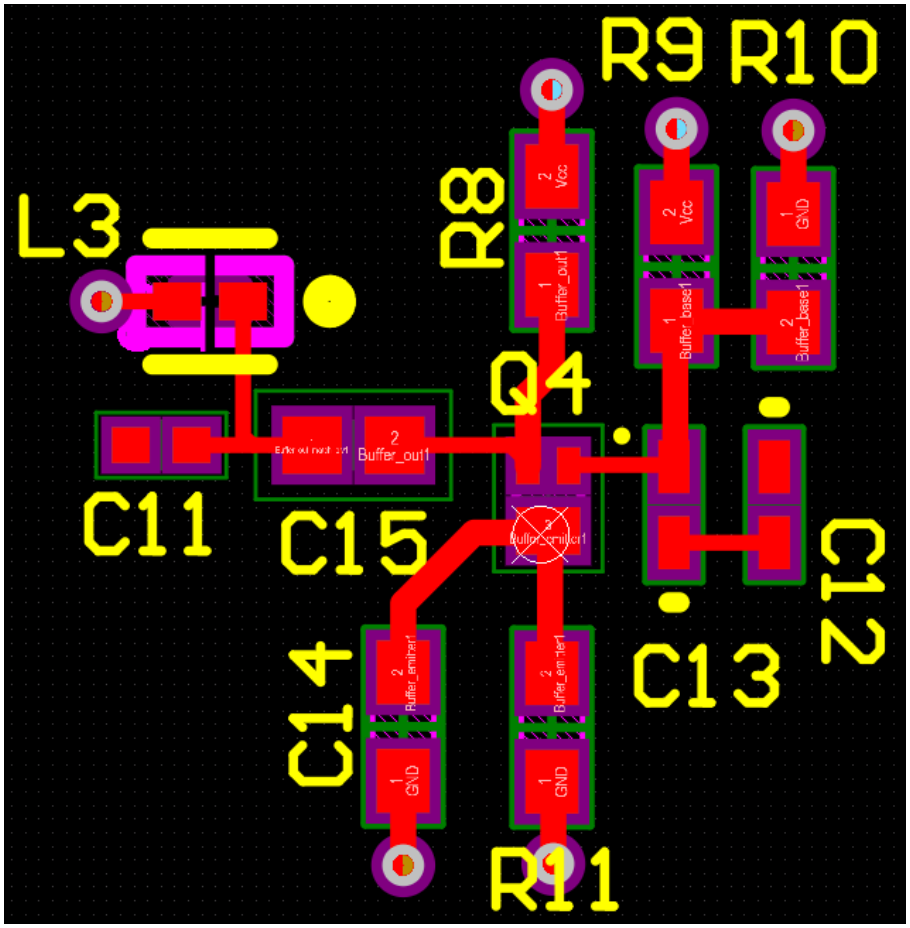


Figure 4.35: Output Buffer Altium Layout

Resistor R10 is placed beside R9 above the capacitive divider (C12, C13) to minimize component spacing and base input shunt parasitic capacitance. Since R9 and R10 are large-valued resistors, 15 and 10 kΩ respectively, these terminals are RF open circuits forming open circuit stubs at the base input. Placing R9 and R10 in close proximity with the base buffer input reduces parasitic open circuit shunt stub effects. C12 and C13 are closely placed in parallel to minimize interconnecting trace lengths and parasitics. RF trace lengths are less than $\lambda_r/20$, or 1.5 mm to eliminate transmission line effects.

4.5.2 Electromagnetic Simulation and Optimization

Figure 4.36 and Figure 4.37 below show the imported ADS layout design and its Momentum cell meshing, respectively.

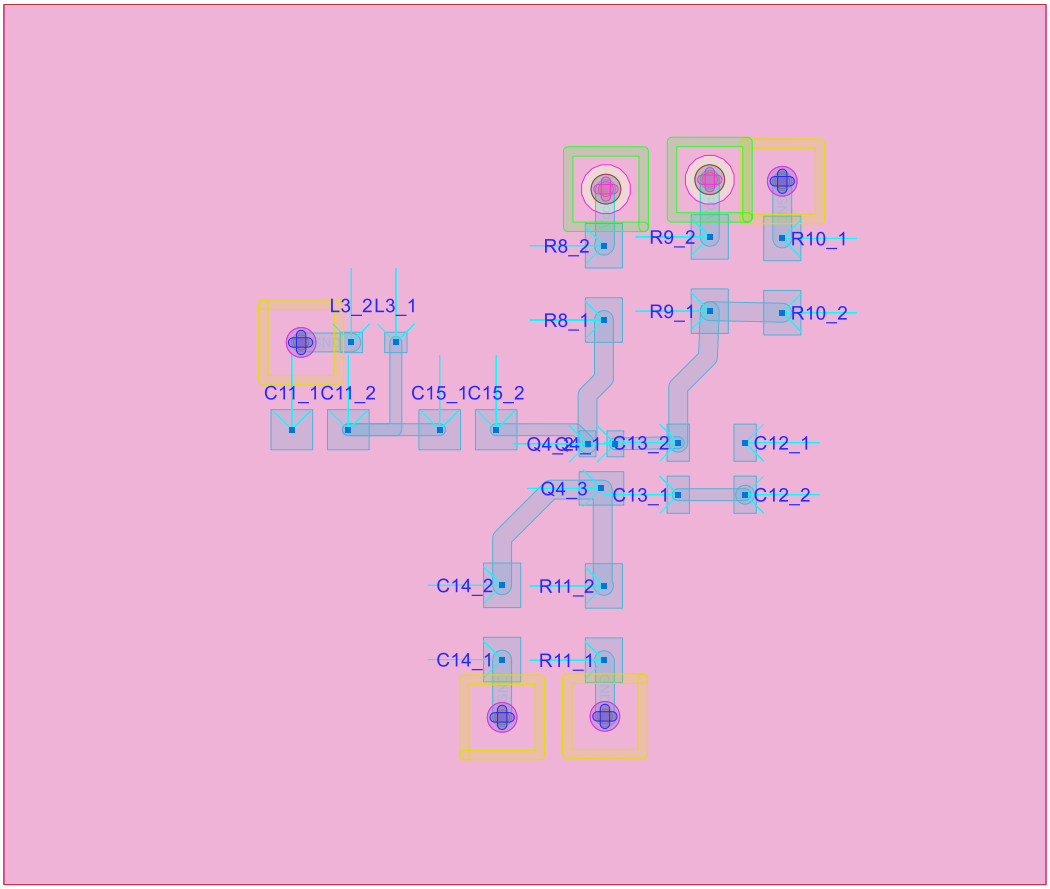


Figure 4.36: Output Buffer ADS EM MoM Layout

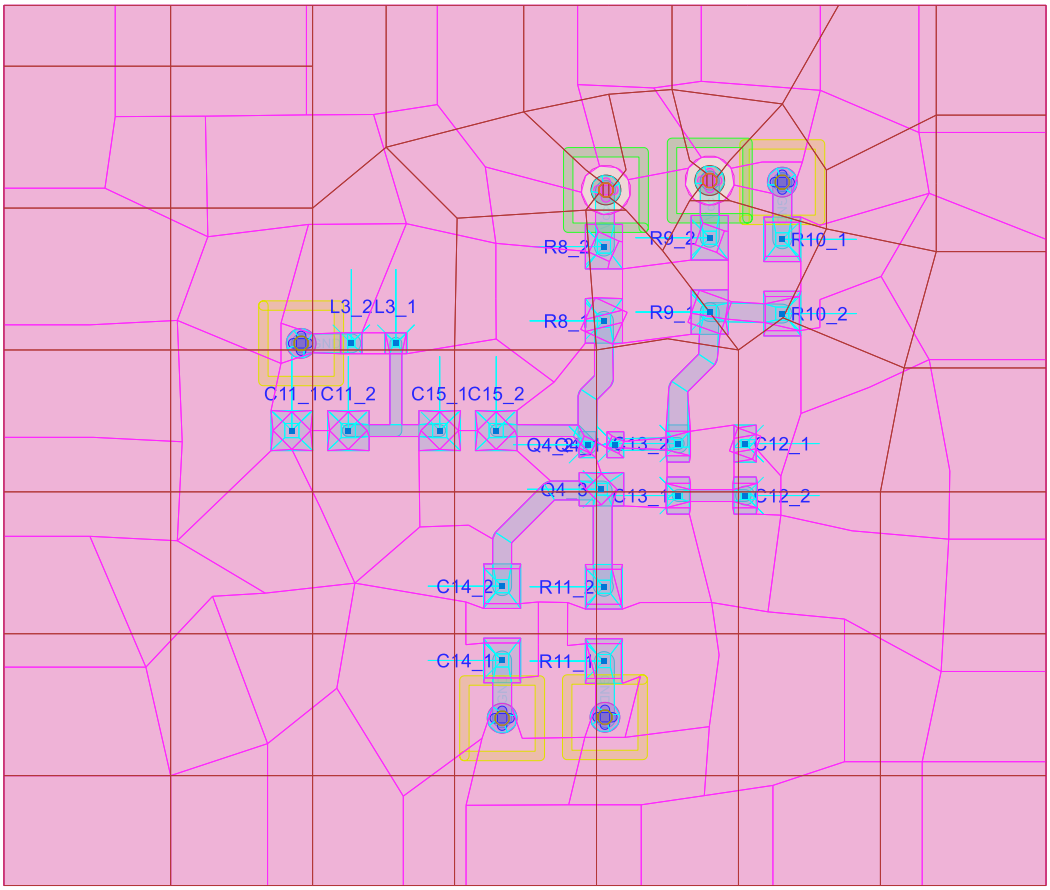


Figure 4.37: Output Buffer ADS EM Momentum Cell Meshing

Initial output buffer EM simulations (includes capacitive divider) do not match schematic simulations. The output return loss increases and forward transmission decreases in the operational frequency range. Figure 4.38 below illustrates the output buffer's forward transmission S_{21} parameter and output return loss for both the schematic design and EM co-simulated layout design.

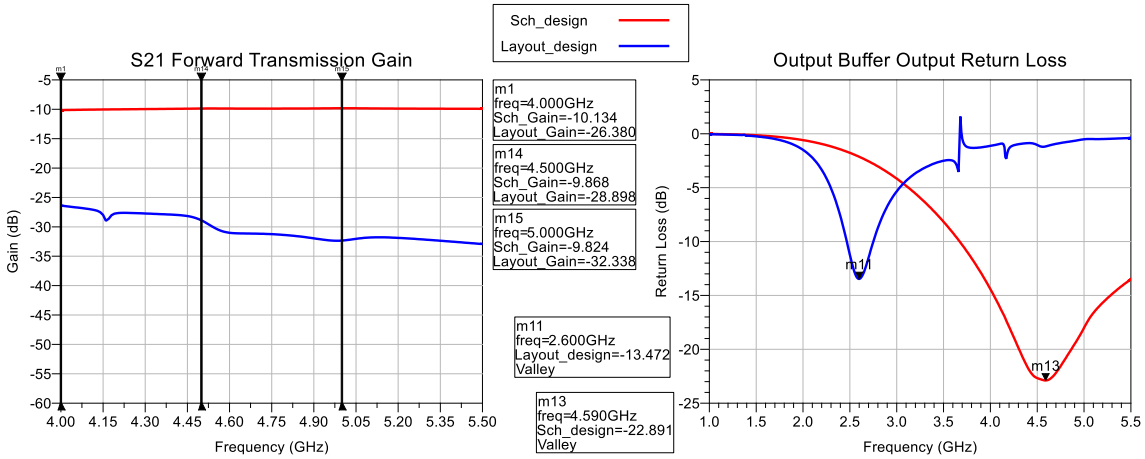


Figure 4.38: Output Buffer Gain and Output Return Loss, Schematic vs. Layout Design

The output buffer forward transmission decreases over 20 dB at frequencies greater than 4.5 GHz. The output return loss frequency response shifts down by 2 GHz, becomes narrow-band, and increases in magnitude. Figure 4.39 below defines the EM simulated output buffer layout design's equivalent input resistance and capacitance. The input resistance is greater than 12 kΩ in the operating frequency range. However, the equivalent input capacitance increases from 0.05 pF to 0.19 pF.

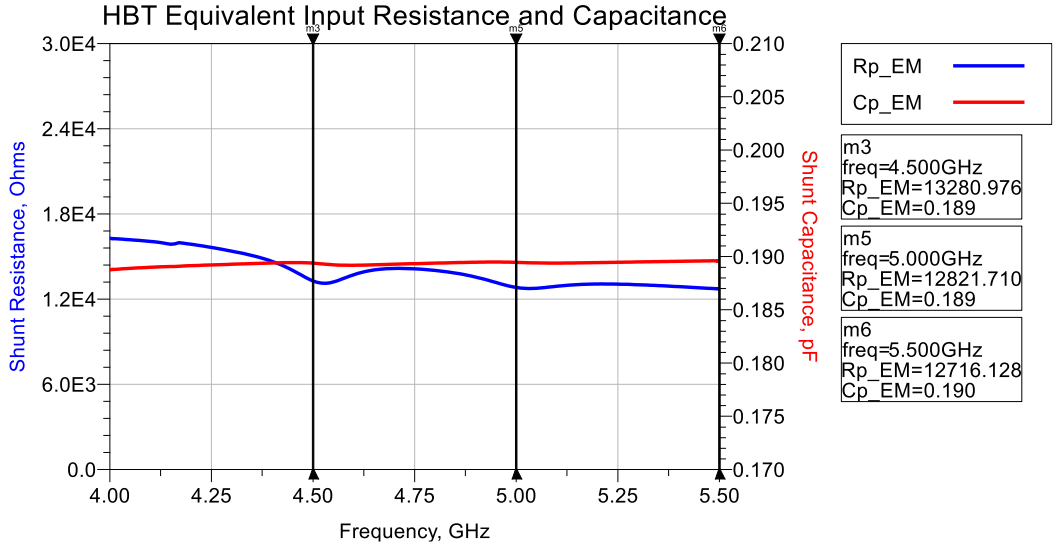


Figure 4.39: Output Buffer EM Simulated Layout Design Equivalent Input Impedance

Keysight ADS Optimization determines capacitor and inductor values for output return loss greater than 10 dB. A Quasi-Newton optimization algorithm is applied to avoid a local minimum error result [39]. Figure 4.40 below displays the optimization status window.

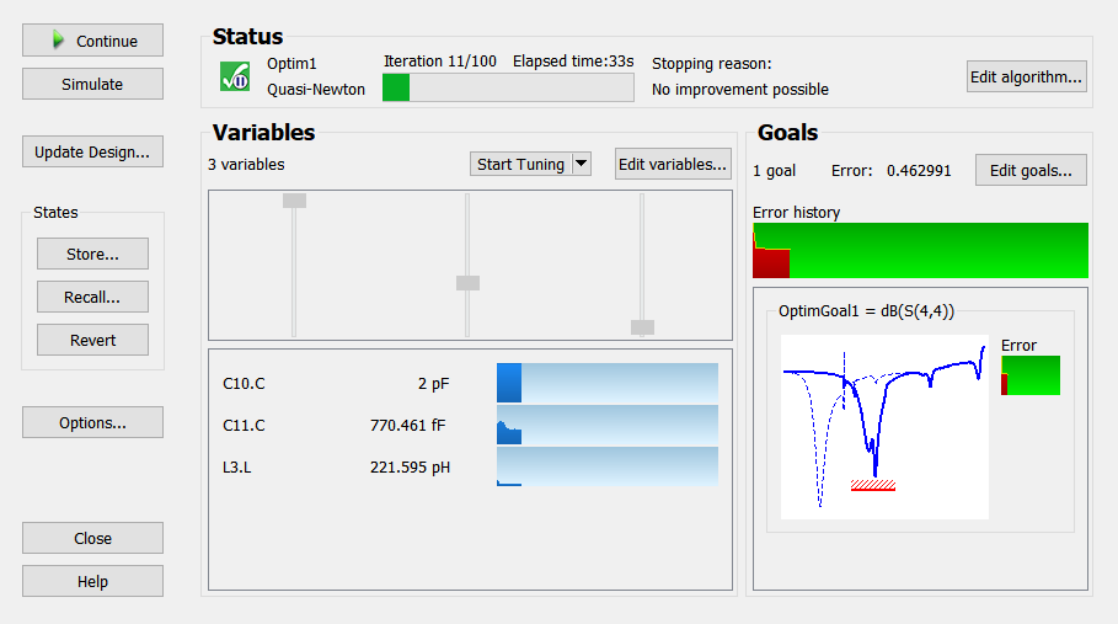


Figure 4.40: Output Buffer Output Matching Network Optimization Portal

Following numerous tuning and optimization iterations, the Quasi-Newton algorithm yielded an inductor value of 0.2 nH. The two T-network series capacitors are 2 pF and 0.9 pF. Figure 4.41 below shows the buffer's forward transmission and output return loss with tuned component values. The output return loss improves by 8 dB; its relative resonance shifts to the operating band. This results in forward transmission increase by 2, 6, and 8 dB at 4, 4.5, and 5 GHz, respectively. This design change did not significantly change the output buffer's equivalent input impedance of Figure 4.39.

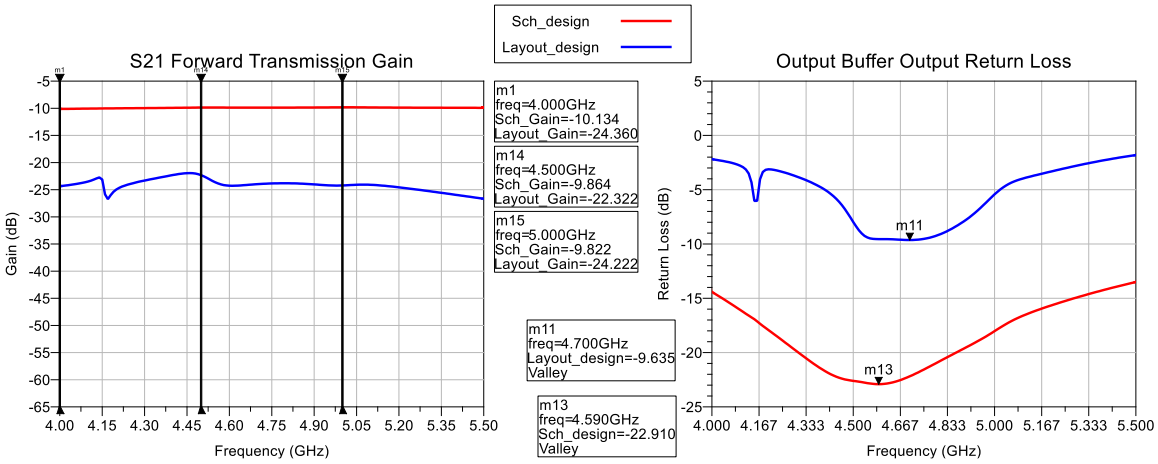


Figure 4.41: Output Buffer Schematic vs. Layout Design Gain and Output Return Loss; EM-Tuned Output Matching Network Component Values

4.6 Final Layout Design and Electromagnetic Performance

All circuit stages are fully integrated and co-simulated to test final layout design performance. Figure 4.42 below shows the top-level full ADS schematic for final circuit EM co-simulations.

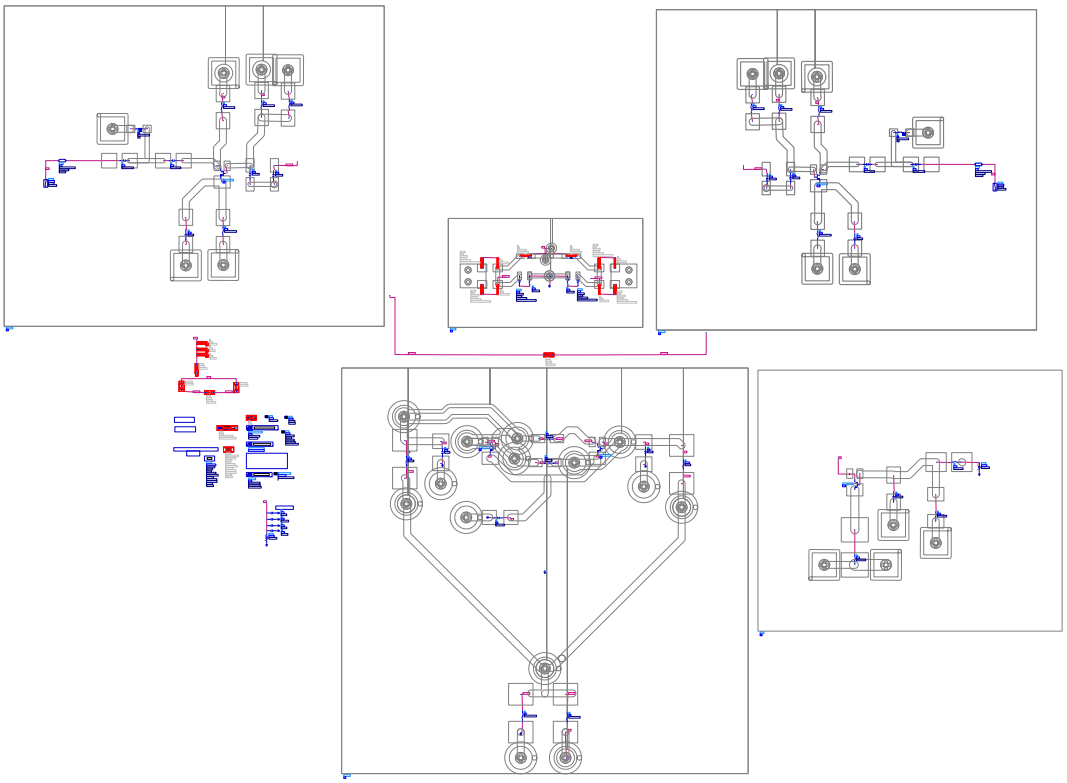


Figure 4.42: Top-Level ADS Full Circuit Schematic with Full EM Co-Simulation

Figure 4.43 defines the VCO single-ended output signal with V_{tune} = 18.3 V. The output frequency decreases from 4.40 GHz to 4.28 GHz when integrating the output buffer. The buffer's increased equivalent input capacitance (Figure 4.39) loads the VCO core and decreases the resonant frequency. Additionally, the output power level decreases from -6 dBm to -21 dBm. This is due to the output buffer's decreased forward transmission shown in the previous section.

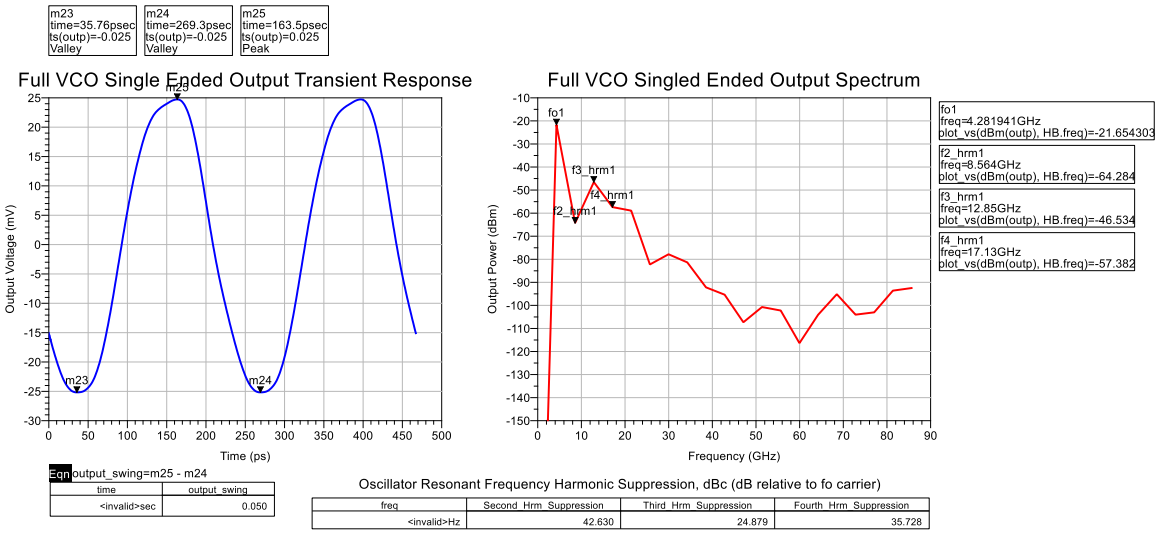


Figure 4.43: Full VCO Layout Single-Ended Output Time and Frequency Domain Response, f_o = 4.28 GHz, V_{tune} = 18.3 V

Figure 4.44 below defines the single-ended, single side-band output phase noise. Compared to schematic simulations at a similar tuning voltage, the phase noise is similar at -96.8 dBc/Hz at 100 kHz offset from a 4.28 GHz carrier.

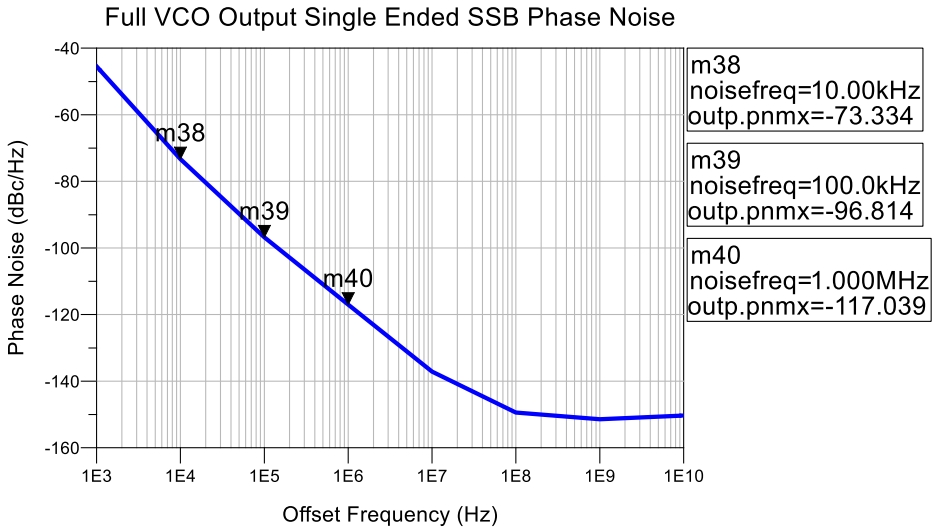


Figure 4.44: Full VCO Layout Single-Ended, Single Side-Band Phase Noise, f_o = 4.28 GHz, V_{tune} = 18.3 V

As described in the previous section, the buffer's output return loss is degraded due to layout parasitics, shown in Figure 4.45. A -10.8 dB minimum output return loss is measured at 5.01 GHz.

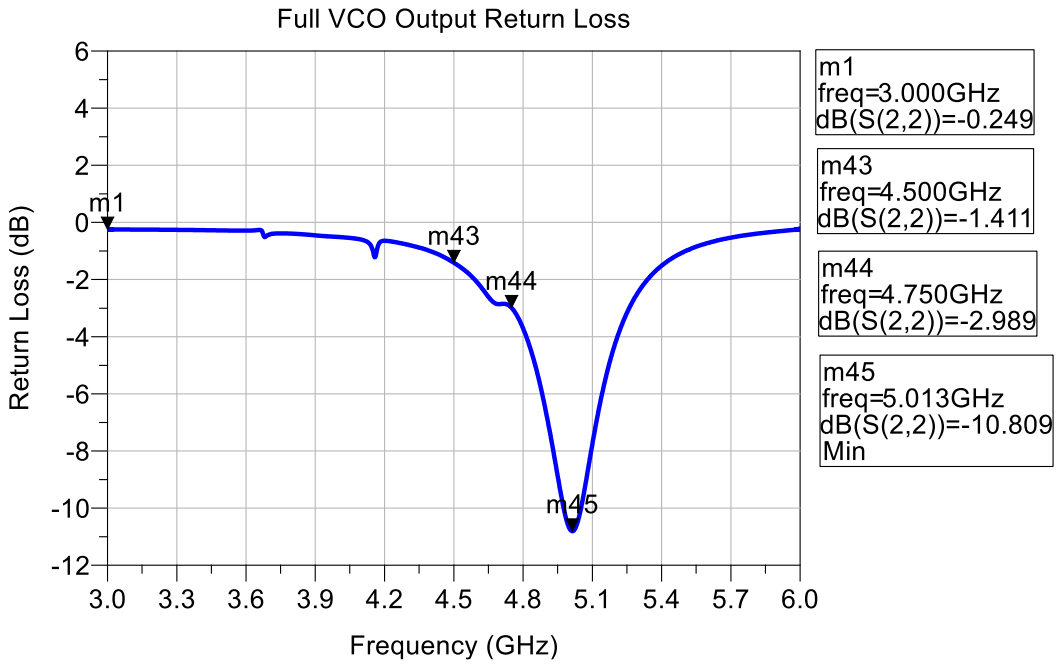


Figure 4.45: Final VCO Layout Output Return Loss

Table 4.1 below defines the comprehensive EM co-simulation performance on the final VCO layout design.

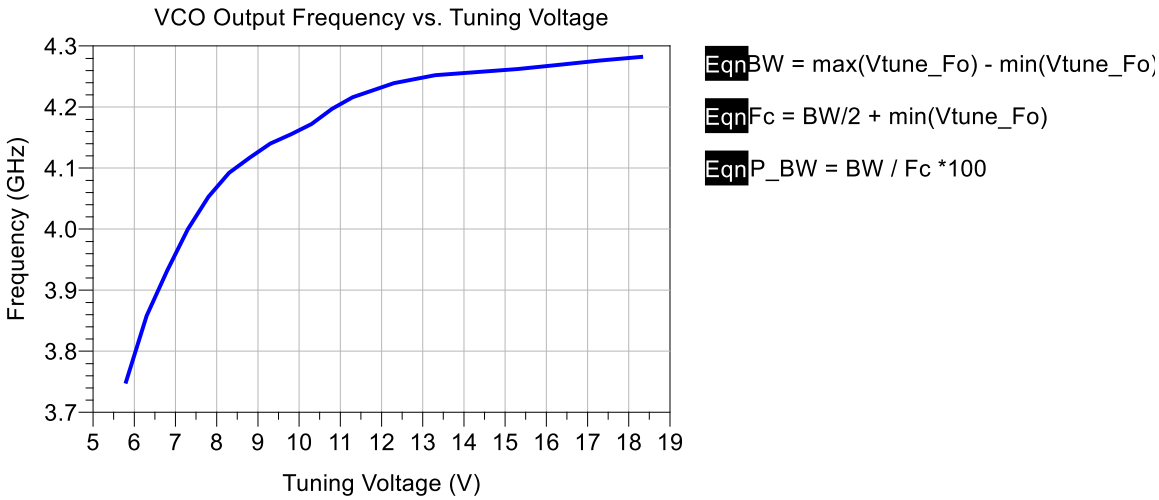
Table 4.1: Final VCO Layout Design EM Co-Simulated Single-Ended Output Performance

Parameter	$5.8\ V_{tune}$	$6.8\ V_{tune}$	$7.8\ V_{tune}$	$10.8\ V_{tune}$	$18.3\ V_{tune}$	Units
Effective Varactor Capacitance	1.09	0.88	0.73	0.55	0.47	pF
VCO Output Frequency, f_o	3.75	3.93	4.05	4.20	4.28	GHz
G_{IN} at f_o	-4.26	-4.62	-4.88	-5.24	-5.45	mS
G_T at f_o	1.36	1.15	1.02	0.89	0.85	mS
VCO Output Swing	69	54	53	46	50	mV_{pp}
Output Power	-19.3	-21.7	-21.7	-22.6	-21.6	dBm
100 kHz Offset Phase Noise	-89	-100.9	-103.7	-96.4	-96.8	dBc/Hz
2nd Harmonic Suppression	32.8	40.0	44.2	43.0	42.6	dBc
3rd Harmonic Suppression	29.6	24.4	25.2	23.2	24.9	dBc
4th Harmonic Suppression	65.2	46.2	38.8	35.1	35.7	dBc
Output Return Loss at f_o	-0.38	-0.48	-0.54	-0.64	-0.74	dB
Power Consumption	65.3	65.3	65.3	65.3	65.3	mW
Frequency Pushing	19	10	7	7	2	MHz/V
Frequency Pulling (2:1 VSWR)	10	9	13	15	18	kHz
FOMP[1]	-162.3	-174.6	-177.7	-170.7	-171.3	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Overall, FOMP improves compared to final schematic design performance defined in Table 3.4. This is mostly due to improved phase noise performance. However, the layout design's EM co-simulated output power is 16 dB (average) less than schematic design simulations.

Figure 4.46 defines the VCO layout design output frequency (f_o) vs. tank circuit tuning voltage (V_{tune}) response. This behavior resembles the schematic design (Figure 3.55) except at lower frequencies due to increased layout parasitics. Figure 4.46 shows a 532 MHz tuning bandwidth (13.2%) with a 4.016 GHz center frequency. Note, the VCO schematic design has 656 MHz tuning bandwidth (13.5%) with a 4.858 MHz center frequency.



BW (GHz)	Fc (GHz)	P_BW (%)
0.532	4.016	13.247

Figure 4.46: Final VCO Layout Output Frequency vs. Tuning Voltage

4.7 Final Layout Design Additions

RF output ports and input DC supply/control voltage pads are added. Supply de-coupling capacitors are integrated in addition to the RF output launch stage.

4.7.1 Power Supply Pads and De-Coupling Capacitors

PCB pads provide physical interfaces for DC supply rails and control voltages. V_{tune} controls varactor diode capacitance and device frequency tuning. V_{CC} is the VCO's 3.3 V supply rail and operates nominally at 3.3 V. Maximum V_{CC} variation (±1 V) is from frequency pushing characteristics in Table 4.1. V_{bias} supplies and tunes the current source. This external supply rail allows for flexible current source tuning, hence differential pairs tail current tuning.

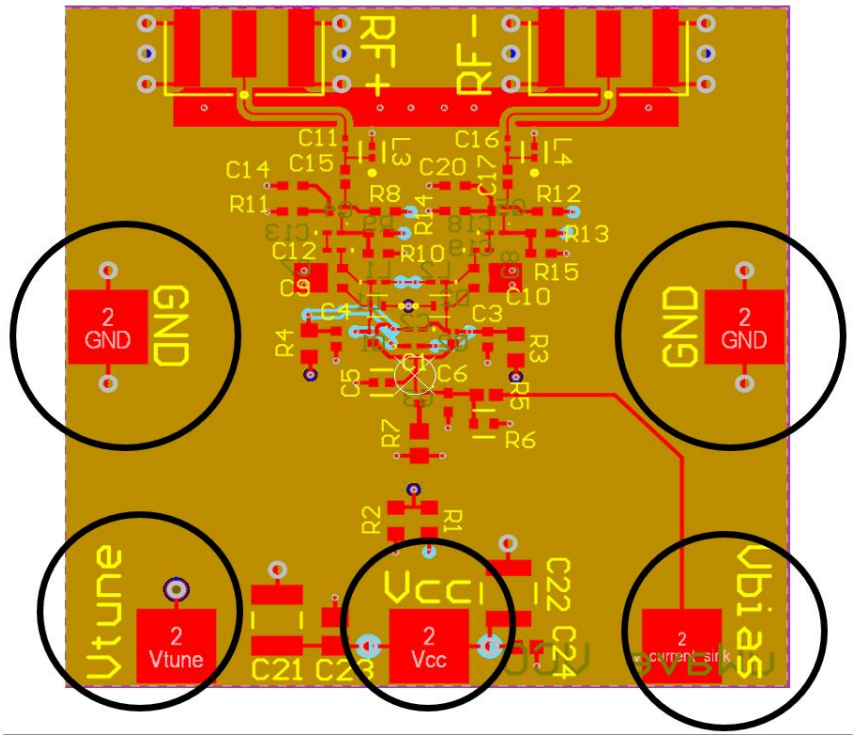


Figure 4.47: Final VCO Layout DC Pad Locations and Labels

Two GND pads are included on either side of the board as references for each DC supply/control voltage, shown in Figure 4.47. These ground pads are directly connected to the layer 2 ground plane through vias on either side of the pads. V_{tune}, V_{CC}, and V_{bias} pads are located on the bottom of the board, moving from left to right, respectively,

shown in Figure 4.47. V_{tune} is connected to the varactors through vias and layer 4 traces. V_{CC} is directly connected to the layer 3 power plane through two vias on either side of the pad. V_{bias} is connected to the current source through a top layer trace.

Per Sections 2.4.2 and 2.6, several parallel, grounded de-coupling capacitors connect to V_{CC} for wideband noise and harmonic suppression. This is critical to ensure V_{CC} remains a stable DC voltage and AC/RF ground. Figure 4.48 defines the de-coupling parallel capacitor network; 10 pF, 1 nF, 100 nF, and 1μF capacitors chosen to increase the network's frequency response, shown in Figure 4.49.

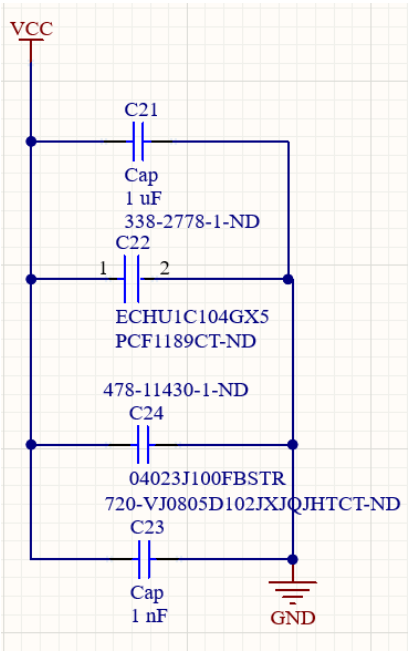


Figure 4.48: V_{CC} Supply De-Coupling Capacitor Network; Altium Schematic

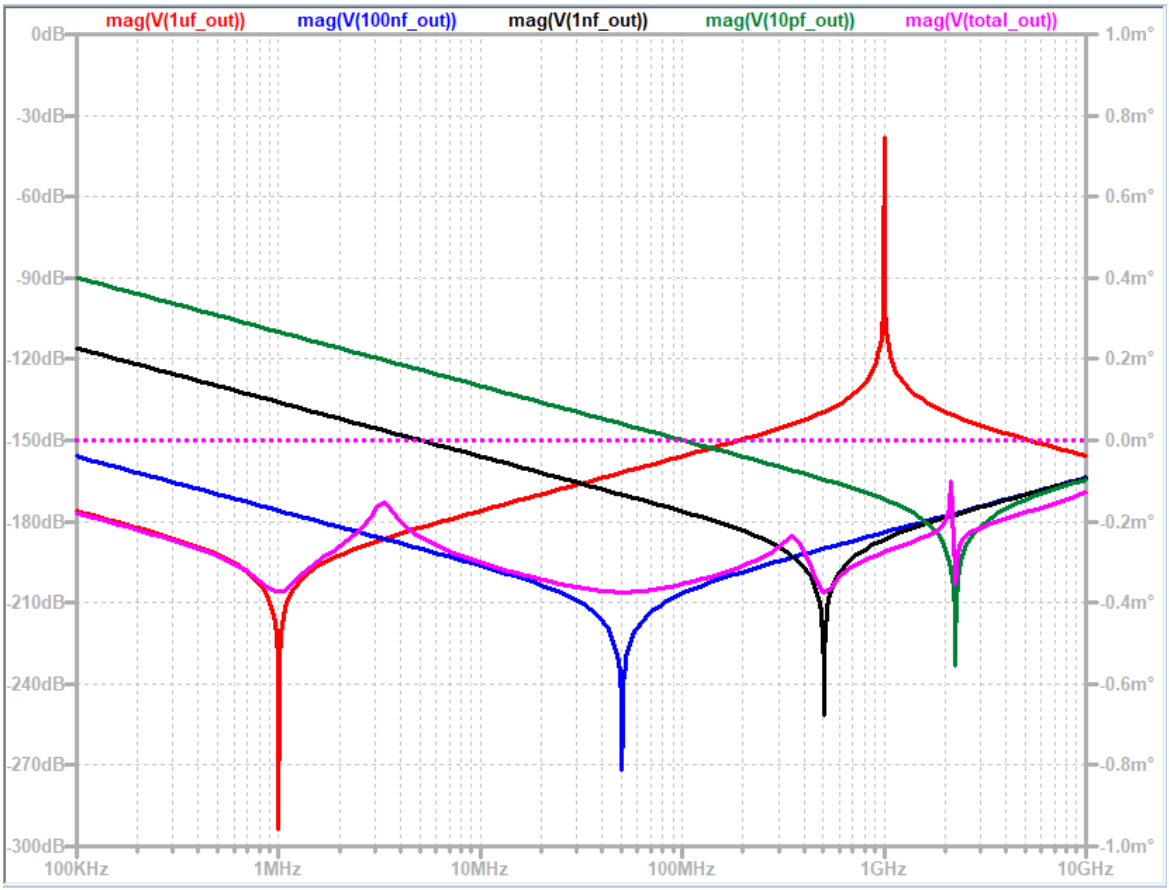


Figure 4.49: De-Coupling Capacitor Network Response; Pink Trace = Total Response

Figure 4.50 shows the capacitive de-coupling network layout connected beside the V_{CC} board input to suppress power supply noise. These capacitors also eliminate conducted and radiated emissions.

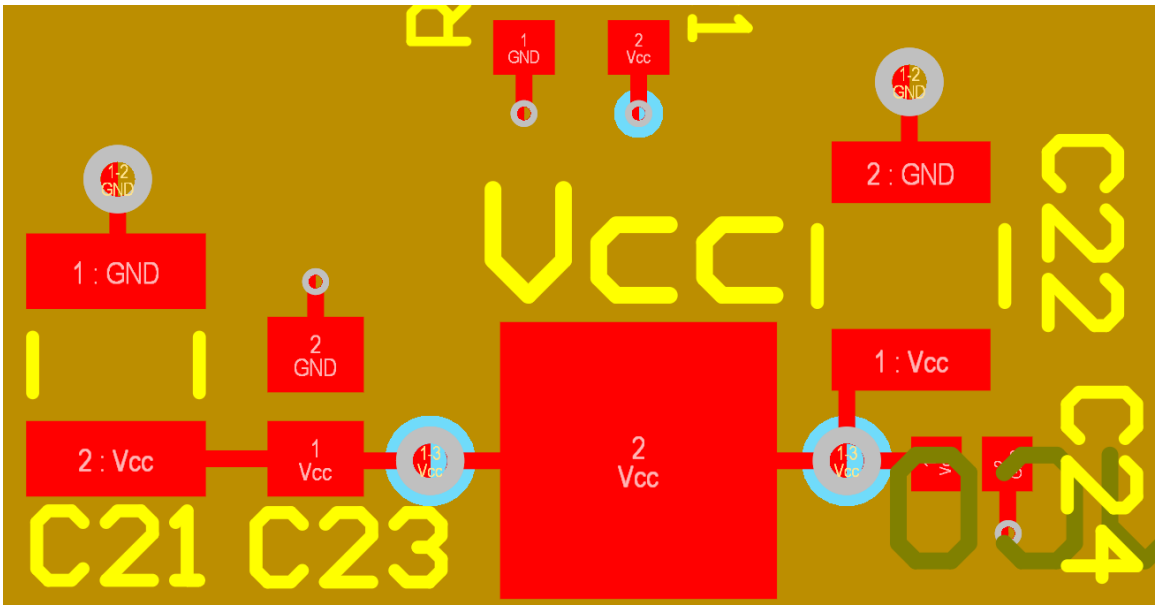


Figure 4.50: V_{CC} Supply De-Coupling Capacitor Network; Layout Implementation

4.7.2 RF Output Launch

The RF output launch includes a microstrip line transition from the output buffer outputs to the VCO board outputs. Female SMA pins with a 50 Ω characteristic impedance interface the design's outputs with other devices. A 50 Ω controlled impedance microstrip transmission line connects the SMA pins to the buffer outputs. Keysight ADS's Linecalc tool computes a 50 Ω microstrip width of 0.2 mm verified by the Momentum EM simulator. Figure 4.51 shows a 0.2 mm wide microstrip transmission line of arbitrary length. To verify this width yields a 50 Ω characteristic impedance, two 50 Ω pins (EM port terminations) are placed on either end of the microstrip line. If the measured reflection coefficient is zero, the line and termination impedances match. If not, the Smith Chart reflection coefficient location defines the characteristic impedance (complex value).

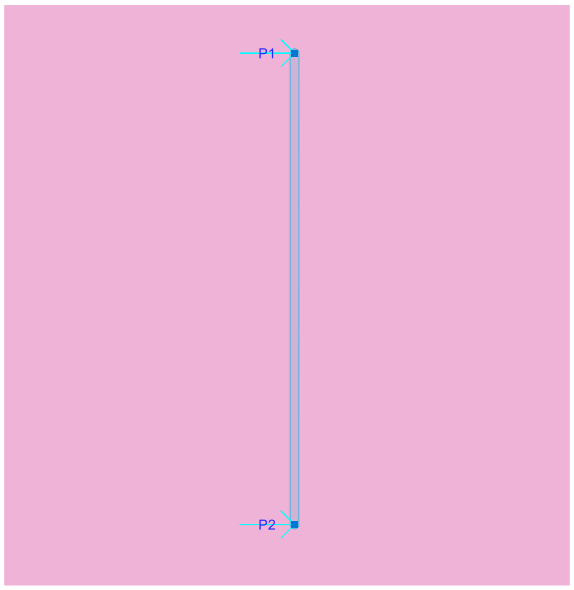


Figure 4.51: 50 Ω Microstrip Line Characterization; ADS Momentum Layout

Figure 4.52 below shows the 0.2 mm wide microstrip line's return loss from 1 to 8 GHz.

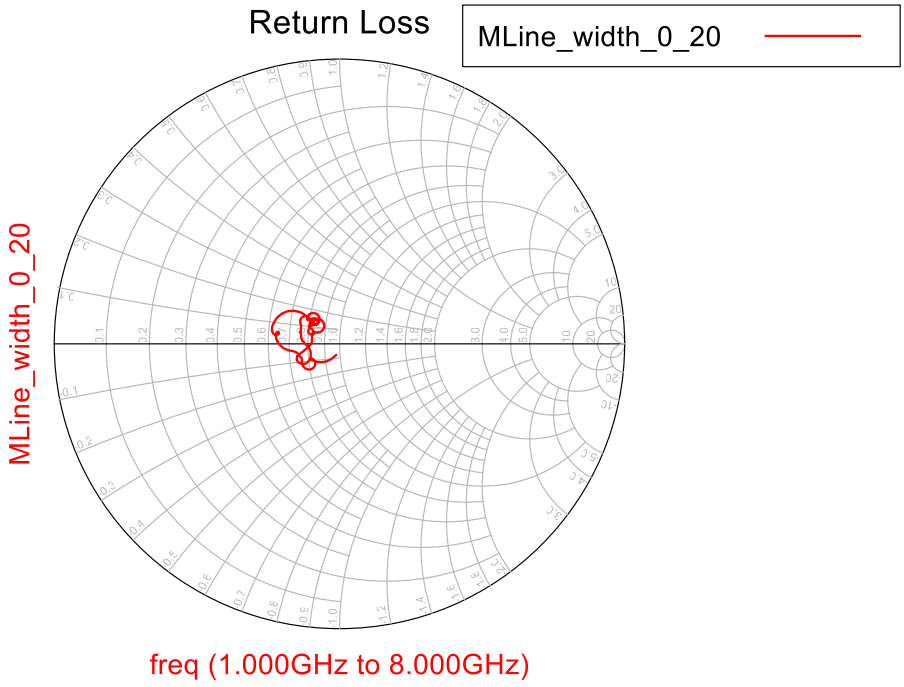


Figure 4.52: Smith Chart Return Loss, 50 Ω Microstrip Line, 0.2 mm Width

The return loss curve is not located at the Smith chart origin; therefore, the line's characteristic impedance is 35 – 45 Ω. Since the curve resides to the left of the center point on the Smith chart, it represents a characteristic resistance less than 50 Ω, whereas a curve to the right of the center point represents a characteristic resistance greater than 50 Ω. Therefore, the microstrip line's resistance must be increased to reach the Smith chart's center and a 50 Ω characteristic impedance (purely resistance). The microstrip line width is decreased to 0.16 mm, as a decreased microstrip line width yields a higher characteristic impedance. Figure 4.53 below shows this decreased 0.16 mm line width's return loss on the same Smith chart as the initial 0.2 mm line width's return loss.

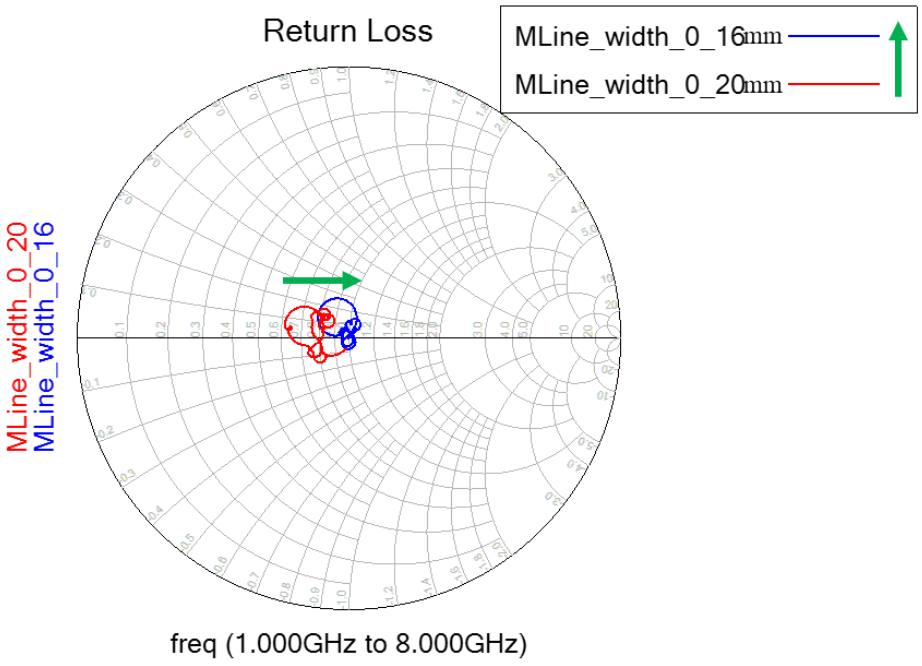


Figure 4.53: 50 Ω Microstrip Line Smith Chart Impedance Tuning

From the figure above, the 0.16 mm wide line is more centered on the Smith chart than the 0.2 mm wide line. This results in a more controlled 50 Ω impedance microstrip transmission line with a decreased VSWR, shown in Figure 4.54. Additionally,

Momentum tuning of the microstrip line width accounts for RF/EM effects, excluded from Linecalc's computations, that alter wave propagation delay and impedance variations as frequency increases (i.e., line dispersion, Skin effect, material frequency dependence) [18].

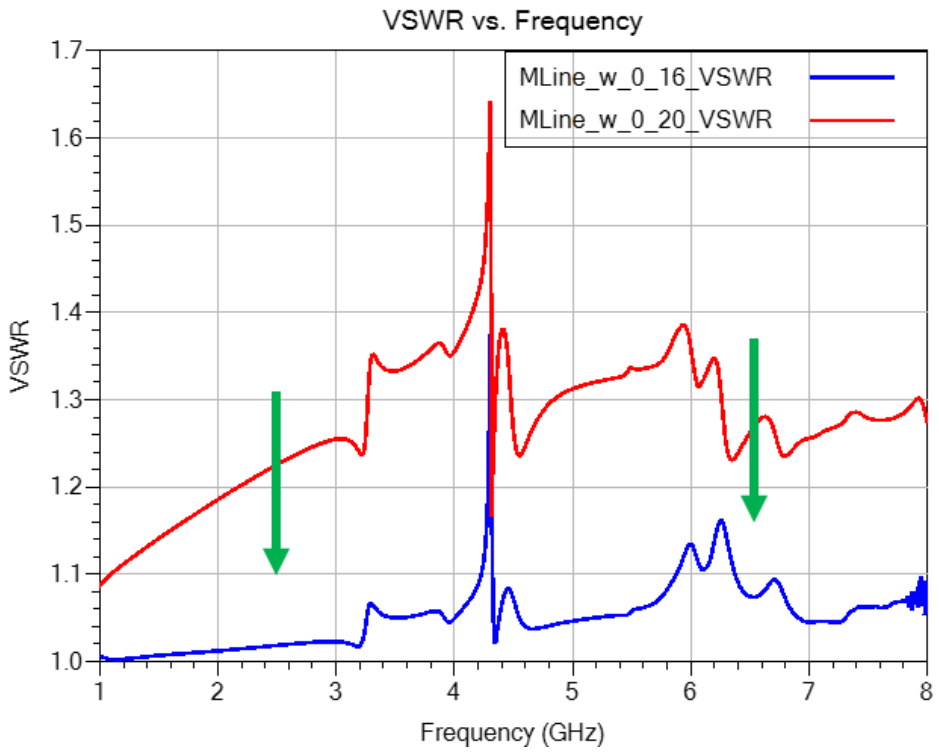


Figure 4.54: VSWR vs. Frequency; Initial 0.20 mm vs. Tuned 0.16 mm Microstrip Line Width

Shielding is added around the microstrip line output transition, protecting the trace from external radiation or potential coupling. This approximates a coplanar waveguide, except the microstrip to adjacent ground plane gap (0.3 mm) is larger than the dielectric substrate height (0.11 mm). Figure 4.55 below shows the final RF output launch stage. Smooth curved output microstrip traces prevent reflections, parasitic effects, and Skin effect. RF^{+} and RF^{-} sides are identical to preserve symmetry.

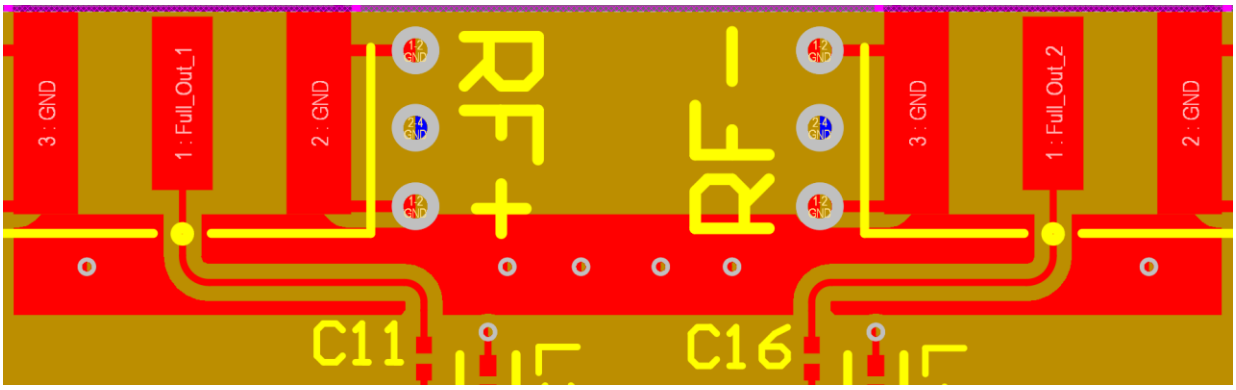


Figure 4.55: Final 50Ω Differential RF Output Launch Stage

Figure 4.56 and Figure 4.57 display the final full VCO layout board design.

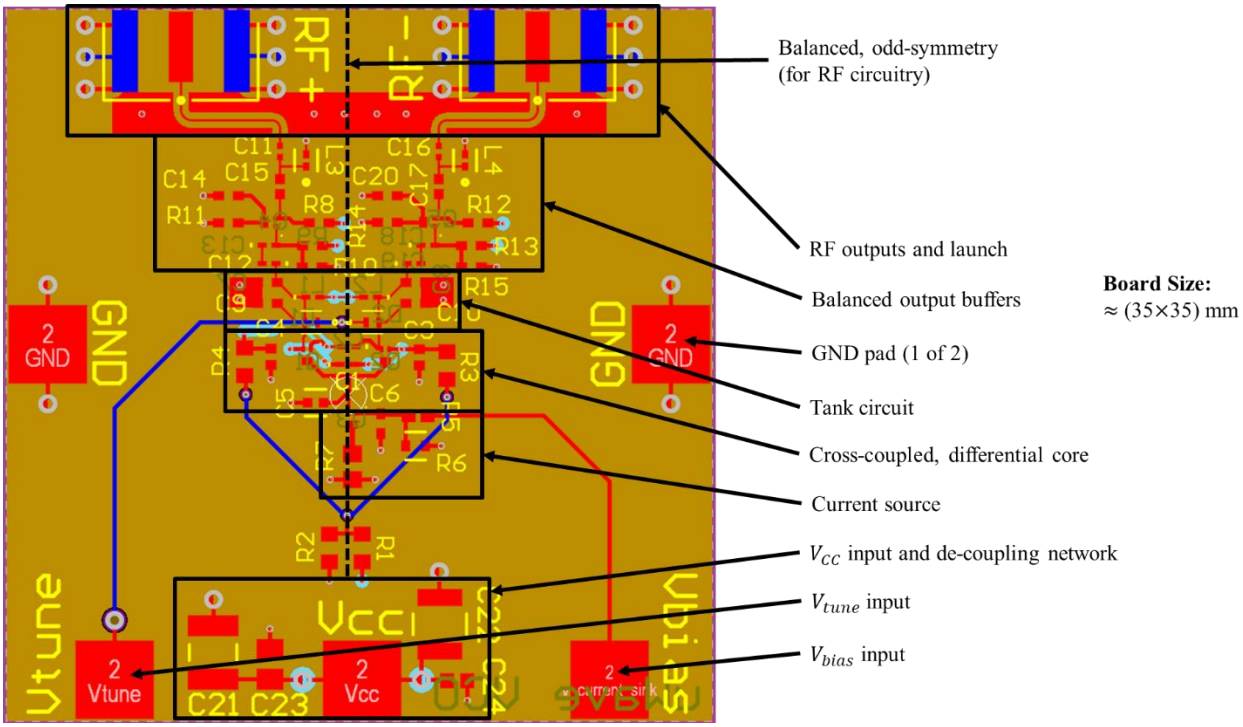


Figure 4.56: Labeled Full VCO Layout Design

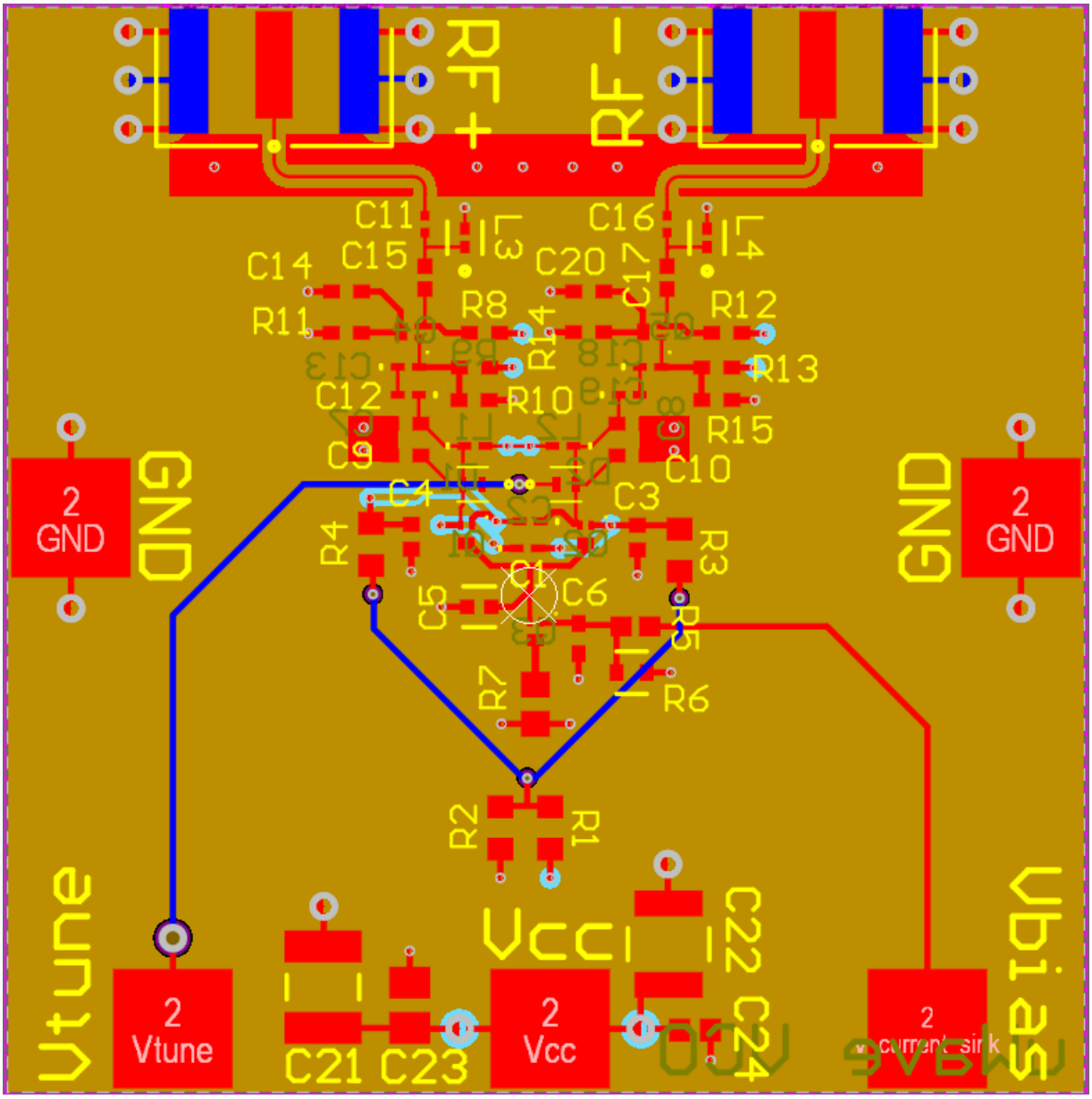


Figure 4.57: Enlarged Full VCO Layout Board Design

Figure 4.58 and Figure 4.59 show the finished board design 3D top and bottom views, respectively.

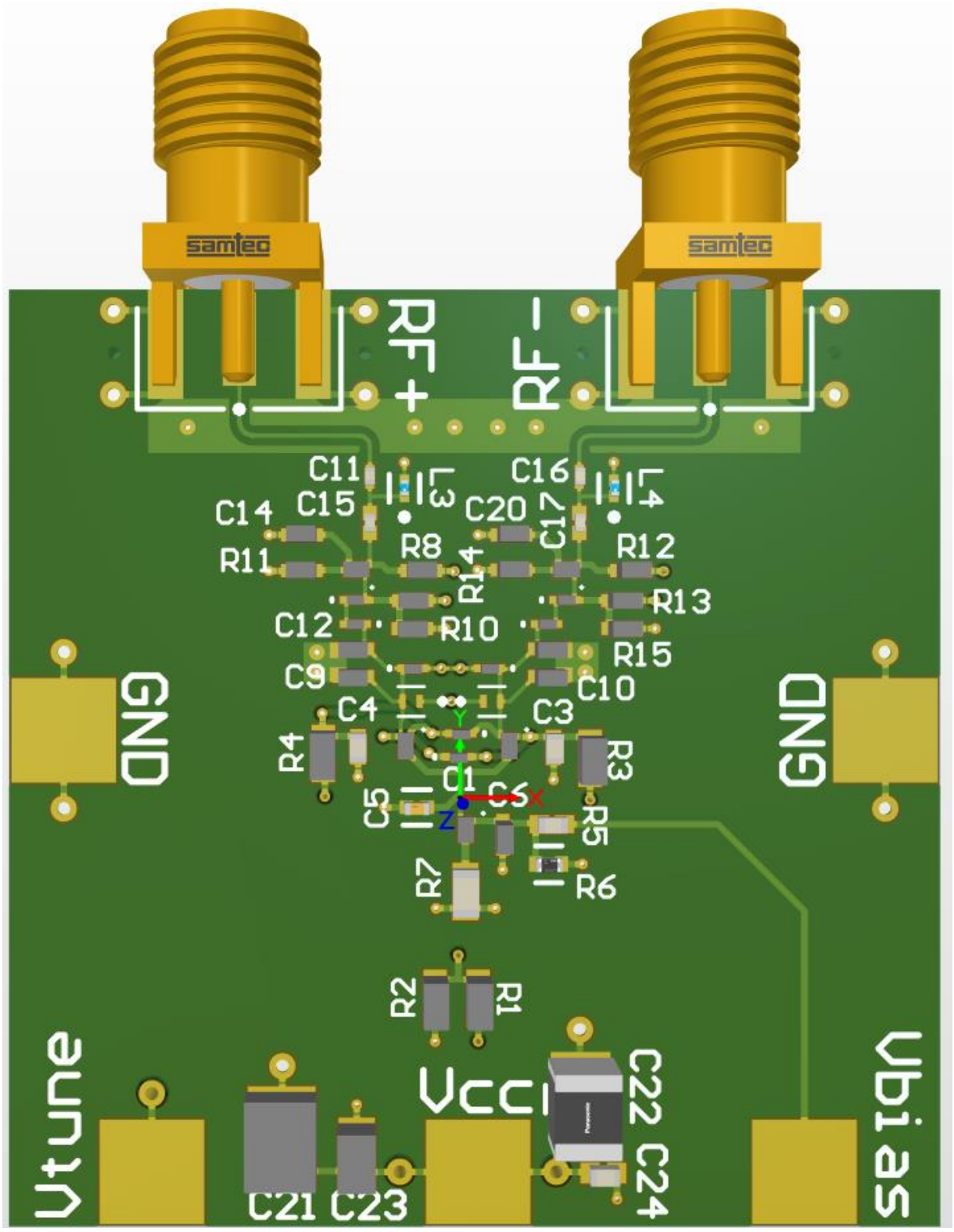


Figure 4.58: Final VCO Board Layout Design, 3D Top View

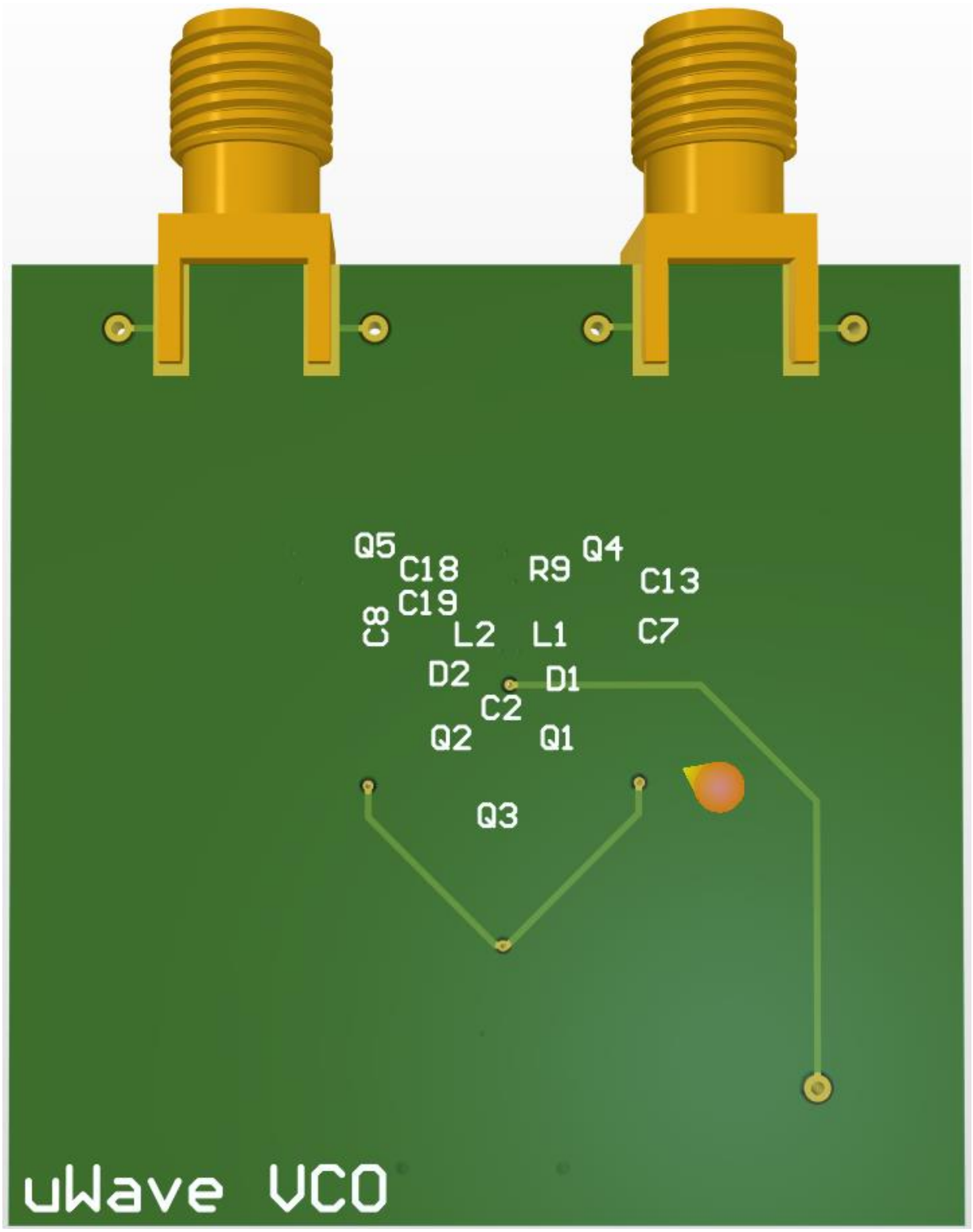


Figure 4.59: Final VCO Board Layout Design, 3D Bottom View

Chapter 5

CONCLUSION

This study presents the design, analysis, optimization, and implementation of a low-power, microwave cross-coupled differential LC voltage-controlled oscillator. Compared to five industry standard VCOs defined in Table 2.2, this design consumes the least DC power of 65.3 mW while surpassing the best figure of merit of -176.5 dB (HMC430LPx, Analog Devices, 110.5 mW power consumption). This enhanced performance is achieved while utilizing affordable, easily accessible manufacturing processes, components, and design software available to all students and independent engineers. This section compares schematic and layout design performance, explains discrepancies, and suggests future improvements.

5.1 Performance Comparison

Table 5.1 below compares target specifications, the schematic design, layout design, and HMC430LPx by Analog Devices all at each respective center frequency. Although both designs have similar operational bandwidths, the key difference is center frequency. The layout design's center frequency decreased from 4.86 GHz to 4.02 GHz due to layout circuit parasitics. The HMC430LPx center frequency performance is also included in Table 5.1 for comparison, as it has the best FOM_P of all noted alternative market VCOs. Of all specification, designs, and market alternatives, the layout design has the best FOM_P of -177.7 dB and least power consumption of 65.3 mW at its 4 GHz center frequency.

Table 5.1: Center Frequency, f_c, Performance Comparison:
Target Specifications vs. Schematic Design vs. Layout Design vs. HMC430LPx

Parameter	Target	Schematic Design	Layout Design	HMC430LPx Analog Devices [14]	Units
Bandwidth	500	656	532	500	MHz
Center Frequency, f_c	4.25	4.86	4.02	5.25	GHz
Percent Bandwidth	11.76	13.50	13.25	9.5	%
Power Consumption	330	65.3	65.3	110.5	mW
f_c Output Power (Z = 50Ω)	-5	-6.2	-21.7	-1	dBm
100 kHz Offset PN @ f_c	-100	-94.9	-103.7	-103	dBc/Hz
2nd Harmonic Suppression	-	16.8	44.2	15	dBc
F-Pushing	-	3	7	12	MHz/V
F-Pulling (2:1 VSWR)	-	3	13	12,000	kHz pp
FOM_P	-170	-170.5	-177.7	-176.5	dB

Figure 5.1 – Figure 5.8 are derived from all tables in Appendix E; reference Appendix E for additional comprehensive performance comparison. Figure 5.1 compares the schematic and layout design's output return loss vs. output frequency. A -20 dB resonance at 5.2 GHz in the layout response is approximately 600 MHz above the schematic's resonance at 4.6 GHz. At the layout design's output frequencies of 3.75 GHz to 4.3 GHz, the output return loss measures greater than 4 dB.

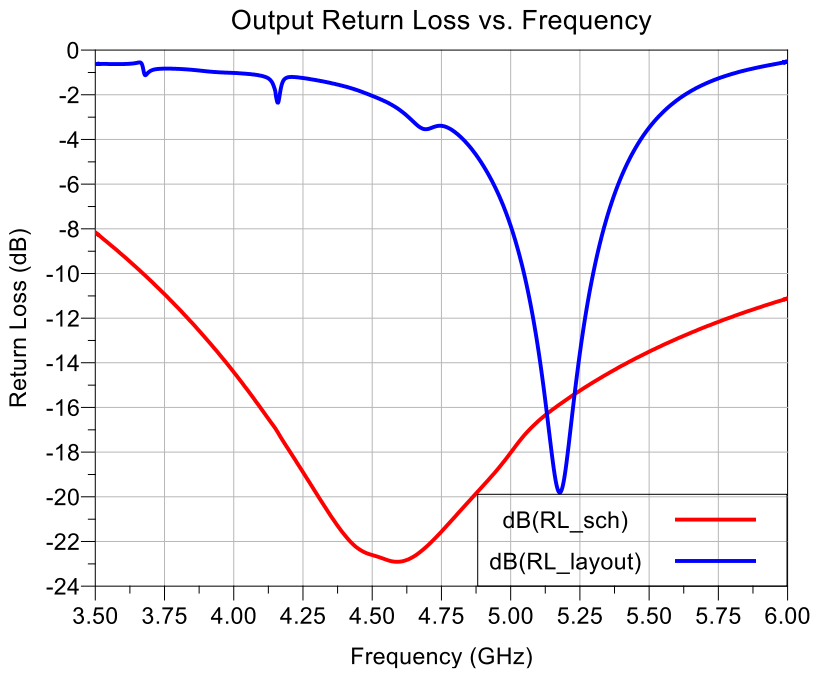


Figure 5.1: Output Return Loss vs. V_{tune}; Schematic vs. Layout Design

Figure 5.2 below compares the schematic and layout design's output frequency vs. tuning voltage. This plot shows the layout design's ≈ 800 MHz reduction in output frequency compared to the schematic design, due to increased parasitic capacitance and inductance in the PCB layout design.

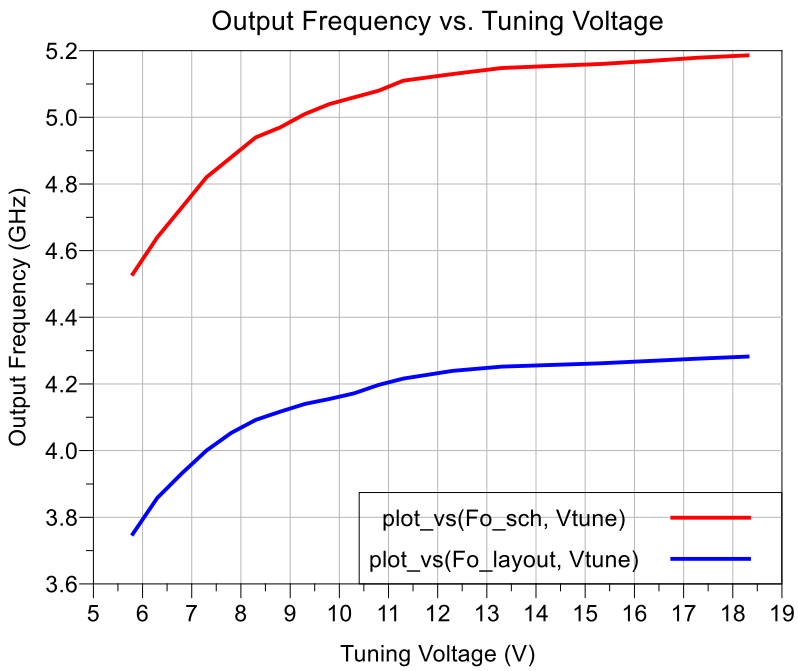


Figure 5.2: Output Frequency vs. V_{tune}; Schematic vs. Layout Design

Figure 5.3 defines the negative conductance ratio, G_{IN}/G_T, for both the schematic and layout designs vs. tuning voltage. Both designs show a ratio less than -2 (magnitude greater than 2), satisfying the negative conductance start-up and steady state definition, equation (3.6).

Figure 5.4 defines the schematic and layout designs output power vs. tuning voltage. As mentioned in Chapter 4, a significant 16 dB average loss in power is observed in the layout design. This can be attributed to the shifted output return loss response.

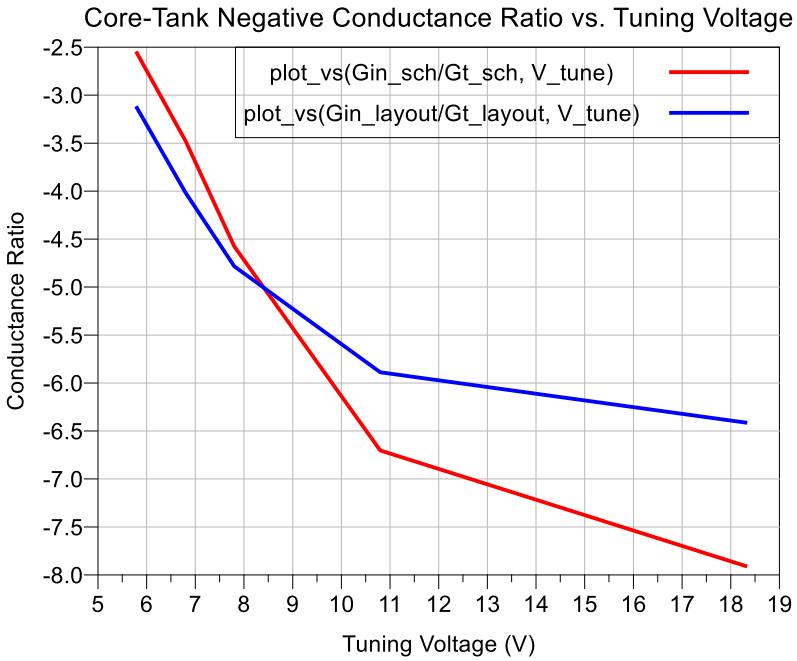


Figure 5.3: Negative Conductance Ratio (G_{IN}/G_T) vs. V_{tune}; Schematic vs. Layout Design

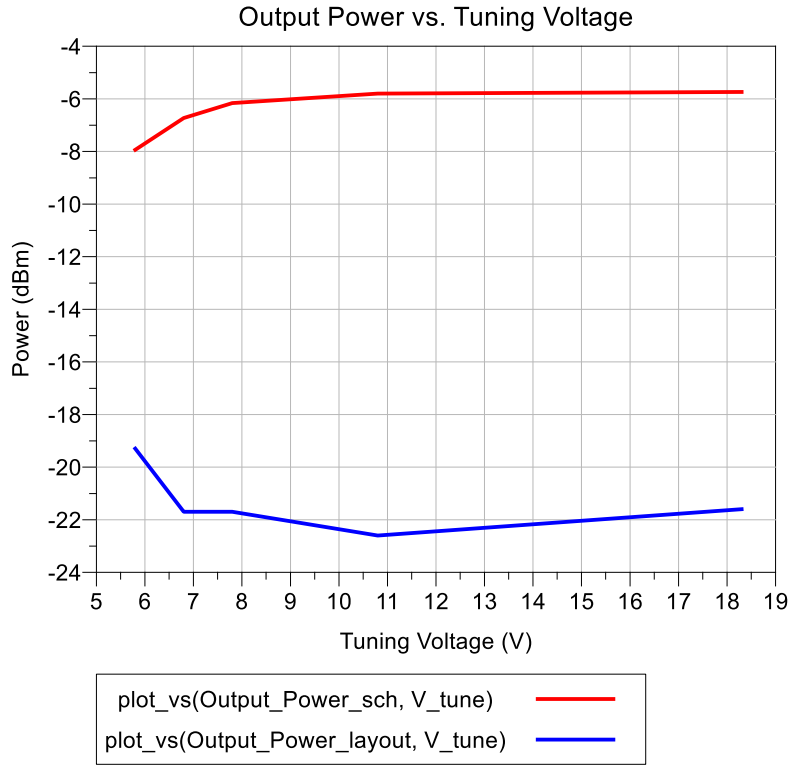


Figure 5.4: Output Power vs. V_{tune}; Schematic vs. Layout Design

Figure 5.5 below displays harmonic suppression vs. tuning voltage for both schematic and layout designs. The schematic design curves are solid traces while the layout traces are dashed. The layout design's second harmonic suppression is 28 dB (average) higher than the schematic. The layout's third and fourth harmonic suppression both measure 3 dB (average) less than the schematic.

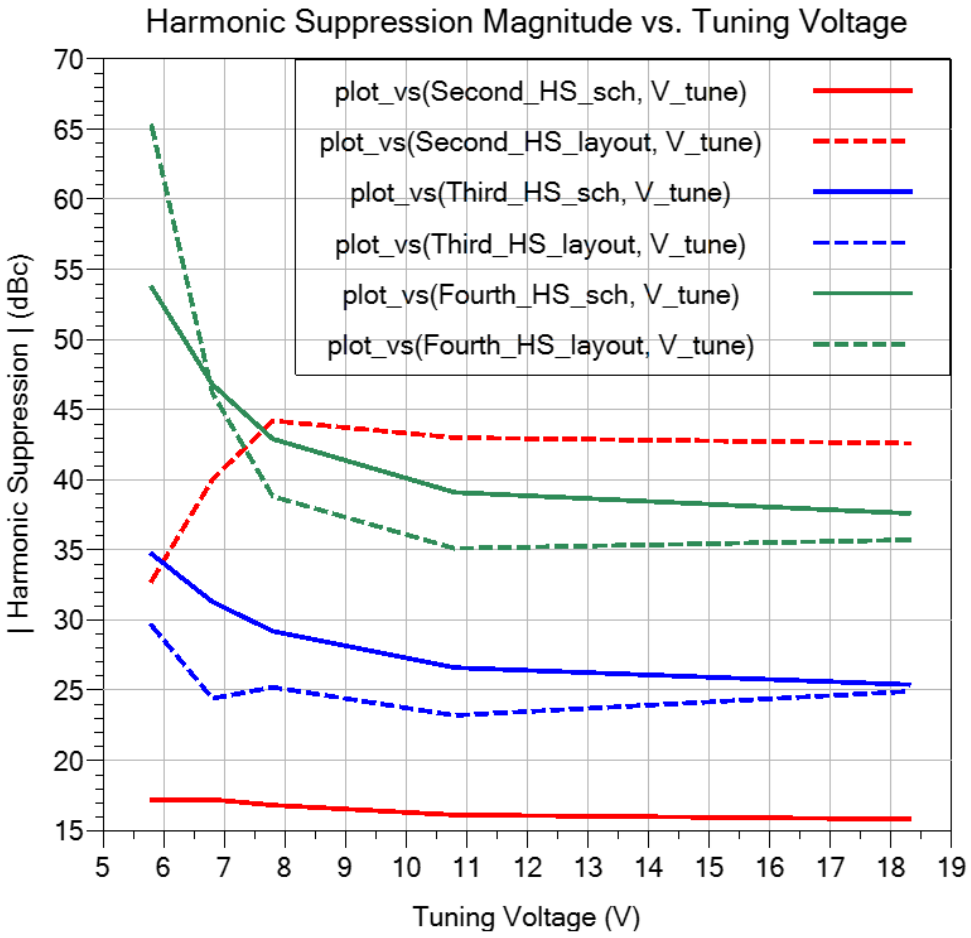


Figure 5.5: Harmonic Suppression vs. V_{tune}; Schematic vs. Layout Design

Figure 5.6 below compares the schematic and layout designs frequency pushing and pulling vs. tuning voltage. Frequency pushing is defined in maximum MHz/V in V_{CC} variation while frequency pulling is simulated at a maximum 2:1 VSWR, defined in kHz. The solid traces represent schematic results while the dashed traces represent the layout

design. On average, the layout simulates a 4 MHz/V increase in frequency pushing (relative to schematic results) with maximum 18 kHz frequency pulling at V_{tune} = 18.3 V.

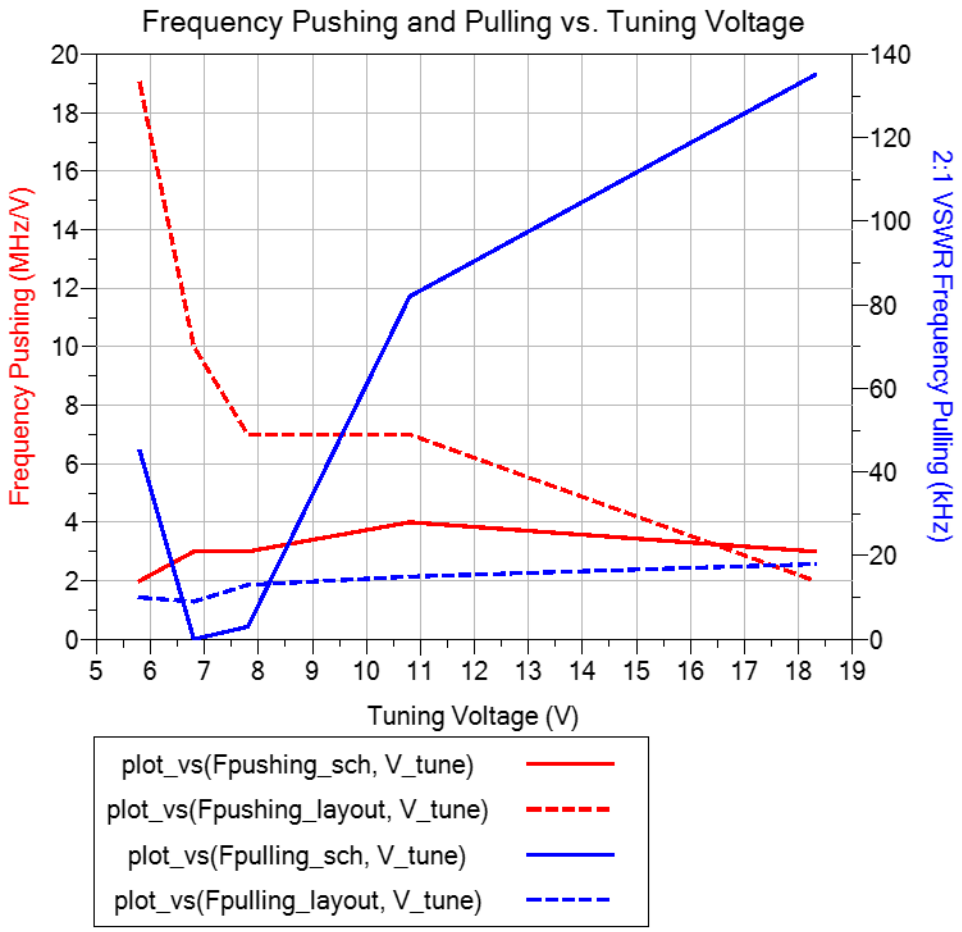


Figure 5.6: Frequency Pushing and Pulling vs. V_{tune}; Schematic vs. Layout Design

Figure 5.7 below compares the schematic and layout design phase noise vs. tuning voltage. All phase noise is simulated at a 100 kHz offset and normalized 1 Hz bandwidth. Aside from the initial tuning voltage of 5.8 V, all layout design phase noise simulates less than the schematics. A minimum layout design phase noise of approximately

-104 dBc/Hz is simulated at V_{tune} = 7.8 V ($f_o \approx$ 4 GHz), corresponding to a minimum, best-case FOM_P of approximately -178 dB.

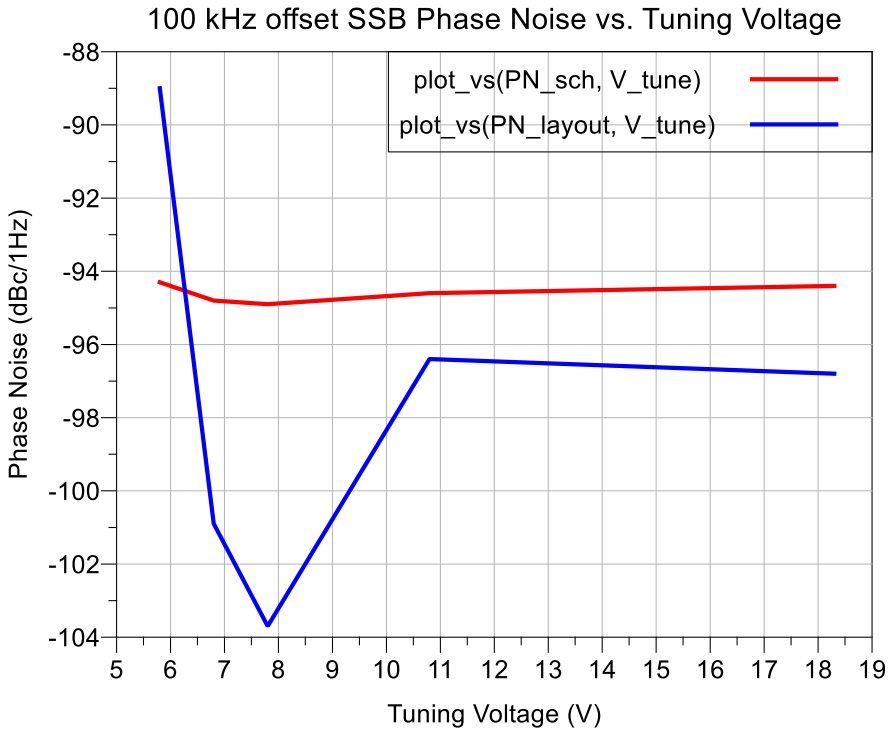


Figure 5.7: Phase Noise vs. V_{tune}; Schematic vs. Layout Design

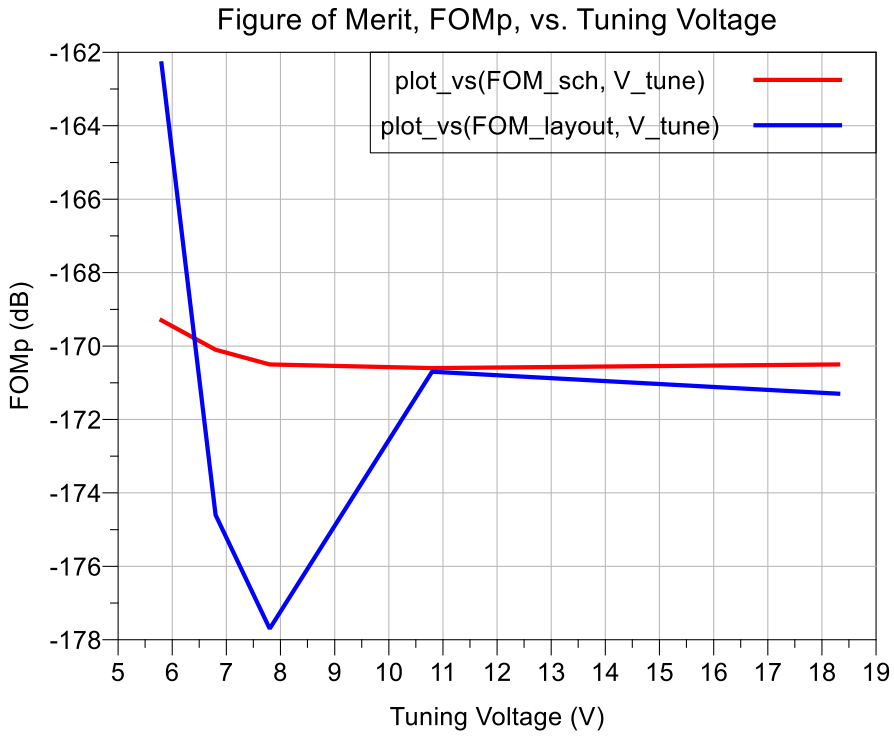


Figure 5.8: Figure of Merit (FOM_P) vs. V_{tune}; Schematic vs. Layout Design

Generally, the layout design outperforms the schematic design in phase noise and hence FOM_P. However, the layout design output power levels do not meet target specifications and schematic design performance. This could be attributed to parasitic circuit elements shifting impedance matching characteristics and increasing reflected power.

Overall, the final design's minimized power consumption proved exceptional; 65.3 mW compared to 330 mW and 110.5 mW target specification and minimum commercial component value, respectively. This was attained using high performing HBTs and novel design techniques. Phase noise optimization techniques of reducing HBT collector-emitter current, reducing base AC I-V swing, and reducing common emitter tail AC I-V swing improved phase noise performance in the layout design

compared to target specification by 4 dB at a 4 GHz output frequency. As previously mentioned, the operating frequency range was the largest discrepancy between the two designs. This, along with most discrepancies between the two designs, are primarily a result of increased circuit parasitics. Parasitic resistance, capacitance, and inductance increase circuit loss and change impedance, quality factor, and resonance.

5.2 Future Work

To further improve this design study, several aspects of this device could be further examined. The first is examining new techniques to minimize parasitic resistance, capacitance, and inductance. As mentioned, these parasitics degrade device performance and shift operating frequencies. New techniques for minimizing these effects can be further studied or modifications to circuit/PCB components or materials can be implemented.

Additionally, the 10+ dB decrease in layout design output power should be examined. Output impedance mismatch, electromagnetic simulation discrepancies, and circuit parasitics should be examined to improve output buffer schematic and layout performance correlation. The output buffer's input impedance and parasitics effect on the output should be considered. Additionally, improved output matching networks may enhance the output match and increase tuning flexibility.

A final future objective to this study is characterizing the actual hardware. Due to manufacturing and societal climate inconsistencies, such as COVID-19 and chip delays, the expected PCB turn-time increased to well over the allotted project timeframe.

REFERENCES

[1] T. K. K. Tsang and M. N. El-Gamal, ""A high figure of merit and area-efficient low-voltage (0.7-1 V) 12 GHz CMOS VCO," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 89-92, 2003.

[2] N. Mahalingam, Y. Wang, B. K. Thangarasu, K. Ma and K. S. Yeo, "A 30-GHz Power-Efficient PLL Frequency Synthesizer for 60-GHz Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4165-4175, 2017.

[3] M. Steer, "Voltage-Controlled Oscillator (VCO)," in *Microwave and RF Design: Amplifiers and Oscillators*, NC State University, 2019, pp. 172-176.

[4] M. Steer, "Oscillator Theory," in *Microwave and RF Design: Amplifiers and Oscillators*, NC State University, 2019, pp. 160-164.

[5] M. Steer, "Reflection Oscillators," in *Microwave and RF Design: Amplifiers and Oscillators*, NC State University, 2019, pp. 165-167.

[6] D. M. Pozar, "Oscillators and Mixers," in *Microwave Engineering*, John Wiley & Sons Inc., 2012, pp. 652-657.

[7] P. Horowitz and W. Hill, "Oscillators and Timers," in *The Art of Electronics*, Cambridge University Press, 2015, pp. 425-472.

[8] T. H. Lee, "Negative Resistance Oscillators," in *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998, pp. 509-514.

[9] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits," *The Bell System Technical Journal*, vol. 48, no. 69, pp. 1937-1955, 1969.

[10] A. Devices, *HMC587LC4B, WIDEBAND MMIC VCO w/BUFFER AMPLIFIER, 5-10 GHz Datasheet*, Analog Devices, v03.0514.

[11] A. Devices, *HMC586LC4B WIDEBAND MMIC VCO w/BUFFER AMPLIFIER, 4-8 GHz Datasheet*, Analog Devices, v06.0514.

[12] Pasternack, *PE1V11027 0.5 inch Commerical Surface Mount (SMT) Voltage Controlled Oscillator (VCO) From 4.26 GHz to 5 GHz With Phase Noise of -79 dBc/Hz*, Irvine, CA: Pasternack Enterprises, Inc. , 2016.

[13] C. Vales, *Voltage Controlled Oscillator-VCO CVCO55BH-4940-4940 Datasheet*, Crystek Microwave, 2022.

[14] A. Devices, *HMC430LP4 / 430LP4E MMIC VCO w/BUFFER AMPLIFIER, 5.0-5.55 GHz Datasheet,* Analog Devices, v06.1106.

[15] M. Steer, "Planar Transmission Lines," in *Microwave and RF Design: Transmission Lines*, NC State University, 2019, pp. 131-161.

[16] C. S. Analysis, *Common PCB Dielectric Materials and Their Properties,* Cadence System Analysis, 2022.

[17] H. W. Ott, "PCB Layout and Stackup," in *Electromagnetic Compatibility Engineering*, John Wiley & Sons Inc. , 2009, pp. 622-659.

[18] M. Steer, "Extraordinary Transmission Line Effects," in *Microwave and RF Design: Transmission Lines*, NC State University, 2019, pp. 165-202.

[19] D. M. Pozar, "Microstrip Line," in *Microwave Engineering*, John Wiley & Son's, Inc., 2012, pp. 147-153.

[20] H. W. Ott, "Effective Decoupling Strategies," in *Electromagnetic Compatibility Engineering*, John Wiley & Sons, Inc., 2009, pp. 436-452.

[21] M. Steer, "Negative Transconductance Differential Oscillator," in *Microwave and RF Design: Amplifiers and Oscillators*, NC State University, 2019, pp. 190-193.

[22] I. Technologies, *BFR740L3RH SiGe:C NPN RF bipolar transistor datasheet,* Infineon Technologies, 2019.

[23] D. Mercer, *The Current Mirror,* Analog Devices, 2021.

[24] E. E. C. Education, *How to Accurately Extract Inductor L/R/Q from S-Parameters in ADS,* Keysight Technologies, 2021.

[25] K. AVX, *Thin-Film RF/Microwave Inductor Technology L0201 Tight Tolerance RF Inductor Datasheet,* Kyocera AVX.

[26] I. Technologies, *BBY53... Silicon Tuning Diode Datasheet*, Infineon Technologies, 2011.

[27] S. Solutions, *SMV1245 Series: Hyperabrupt Junction Tuning Varactors Datasheet,* Skyworks Solutions, 2015.

[28] Panasonic, *Variable Capacitance Diodes, MA26V15 Silicon Epitaxial planar type datasheet,* Panasonic Electronic Components, 2003.

[29] S. Solutions, *SMV123x Series: Hyperabrupt Junction Tuning Varactors Datasheet,* Skyworks Solutions, 2020.

[30] E. Notes, *Abrupt & Hyperabrupt Varactor Diodes,* Electronics-Notes.

[31] K. K. Center, *Harmonic Balance Basics,* Keysight Technologies.

[32] T. H. Lee, "The Hajimiri Model: A Time-Varying Phase Noise Theory," in *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998, pp. 536-544.

[33] T. H. Lee, "Noise," in *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge University Press, 1998, pp. 243-266.

[34] D. o. Informatics, *Noise in Bipolar Transistors,* University of Oslo.

[35] A. Hajimiri and T. H. Lee, "Phase Noise in CMOS Differential LC Oscillators," *Symposium on VLSI Circuits ,* pp. 48-51, 1998.

[36] H. Wu, *Divide-by-Odd-Number Injection-Locked Frequency Dividers,* University of Rochester, Advanced Integrated Circuits and Systems Laboratory, 2019.

[37] K. AVX, *Thin-Film RF/Microwave Capacitor Technology,* Kyocera AVX.

[38] PCBWay, *Stackup for 4,6,8 layers Multi-Layer laminated structure,* PCBWay, 2019.

[39] G. Miller, *Quasi-Newton Optimizer,* Keysight Technologies Knowledge Center, 2009.

[40] P. Ashburn, SiGe Heterojunction Bipolar Transistors, John Wiley & Sons, Inc., 2003.

[41] J. D. Cressler and G. Niu, Silicon-Germanium Heterojunction Bipolar Transistors, Artech House, Inc., 2003.

[42] D. B. Davidson, Computational Electromagnetics for RF and Microwave Engineering, Cambridge University Press, 2011.

[43] C. A. Balanis, Advanced Engineering Electromagnetics, John Wiley & Sons, Inc., 2012.

A HETEROJUNCTION BIPOLAR TRANSISTORS

The Heterojunction Bipolar Transistor (HBT) is a type of BJT that uses differing semiconductor materials for the base and emitter regions, resulting in a heterojunction. A HBT is advantageous over a normal BJT since it utilizes a wide bandgap emitter on a low bandgap base, which provides a necessary band offset. This limits the injection of holes from the base into the emitter region since the valence band potential barrier is higher than the conduction band. Additionally, this allows the base region to be heavily doped, in turn decreasing the base resistance while still maintaining transistor gain. These characteristics make the HBT a desirable component for Radio Frequency (RF) engineering due to its increased frequency response while still maintaining a suitable amount of transistor gain and low noise capability.

The Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) is produced by sandwiching a SiGe base between a Si collector and a Si emitter as observed in the structural diagram provided in Figure A.1.

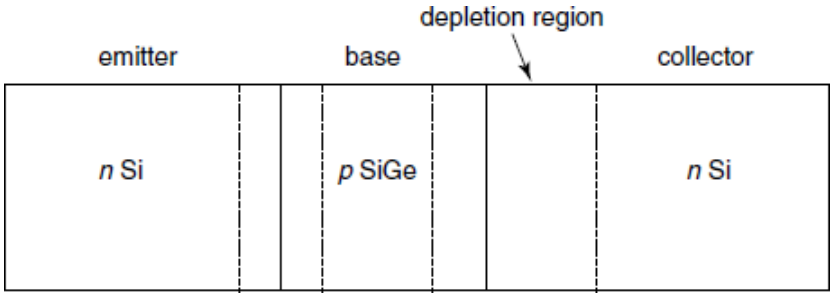
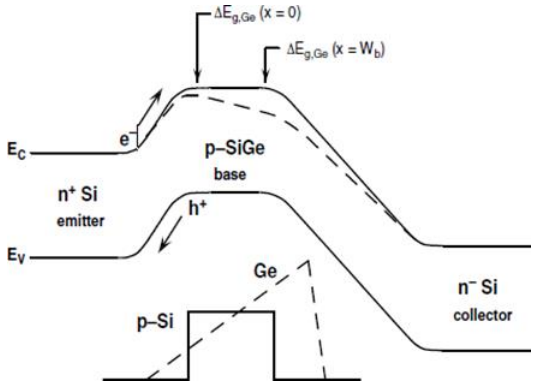
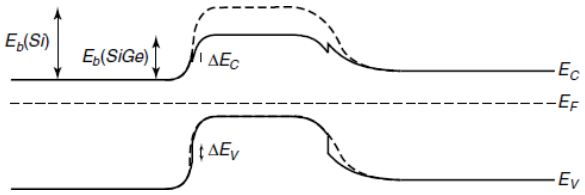


Figure A.1: SiGe HBT Structural Diagram [40]

The band diagram shown in Figure A.2(a) displays the graded doping of the base relative to the emitter region of the HBT. Figure A.2(b) compares the band diagram of a SiGe HBT to a Si BJT.



(a) SiGe HBT band diagram [41]



(b) Comparison of band diagrams of a SiGe HBT (solid line) and a Si BJT (dashed line) [40]

Figure A.2: Band Diagrams

The Si BJT is represented as a dashed line where the SiGe HBT is represented as a solid line in Figure A.2(b). Observe from this figure that the conduction band barrier height of the base region is much higher in the Si BJT compared to the SiGe HBT. This decreased barrier height in the SiGe HBT allows for a larger collector-emitter current at a given base-emitter voltage relative to the Si BJT. Additionally, note that the valence band base region barriers are similar in both the Si BJT and SiGe HBT. This means that the hole flow from the base to the emitter (or the base-emitter current) will be approximately the same in both devices. The take-away from this is that if a Si BJT and SiGe HBT were to be biased at approximately the same base current level, the SiGe HBT would allow for

a higher collector-emitter current to flow, yielding an increased device performance (such as gain).

The fabrication and processing of SiGe HBT's requires special care due to the extremely high-doped, thin base layers. Epitaxy methods such as differential or strained epitaxy as well as molecular beam epitaxy possess the capabilities to process these devices through crystal growth or crystalline thin- film material deposition. One common processing technique that will be evaluated is differential epitaxy. Figure A.3 summarizes a simplified process sequence for fabricating SiGe HBT's utilizing differential epitaxy [40]. Figure A.3(a) highlights the starting point for the sequence where the p-substrate serves as the foundation below two n-substrates. A single-crystal material and polycrystalline material are then grown and a diagonal interface between the two is created as shown in Figure A.3(b). The next stage highlights the deposition of a thin oxide layer, depositing a polysilicon layer, and etching. This stage is shown in Figure A.3(c) and results in extrinsic base formation. Finally, an extrinsic base implant is performed to heavily dope the base region and complete the SiGe HBT, as pictured in Figure A.3(d). Furthermore, SiGe Heterojunction Bipolar Transistors highlights an excellent, description of this process in [40].

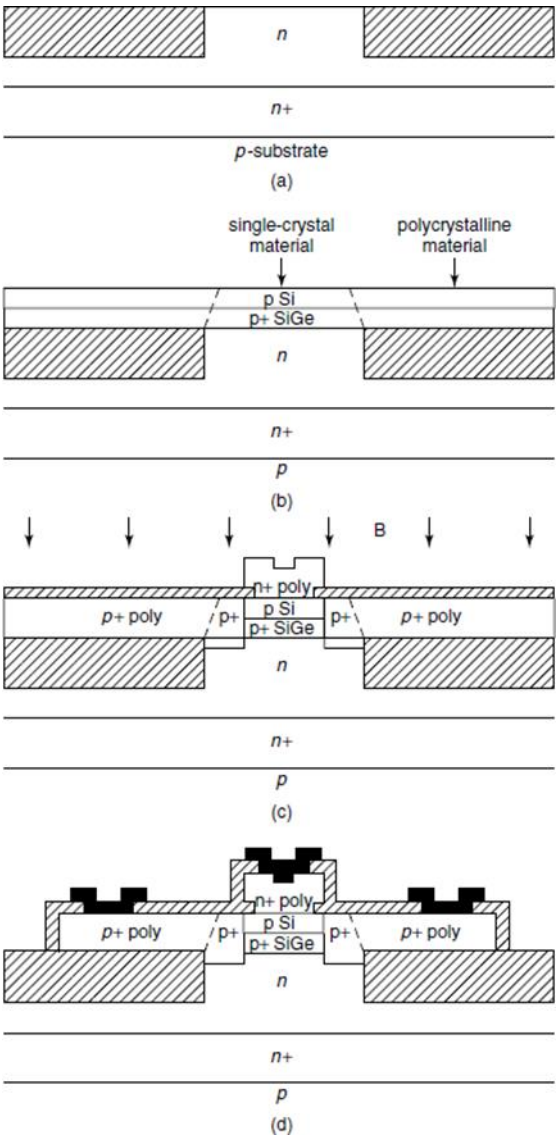


Figure A.3: Simplified process sequence for a SiGe HBT fabricated using differential epitaxy [40]

The intricate processing and extensive structure of the SiGe HBT results in an improved performance compared to its BJT counterpart. One of the most attractive characteristics of the SiGe HBT is its increased frequency response. Gain and bandwidth of electronic devices are indirectly proportional. Meaning as the gain of a device increases, the operational bandwidth decreases, and as the bandwidth increases, the

available gain will decrease. The gain-bandwidth-product (GBW) parameter expresses the maximum operational bandwidth that a device can achieve at unity gain (a gain of one). This parameter is one of the most common ways to express the gain-bandwidth performance capabilities of a device and is also one of the most important high-frequency (HF) parameters for a BJT. The higher the GBW, the higher performing and more attractive a device generally is. The equivalent GBW of a transistor is more commonly known as the transition frequency, f_T. More specifically to a bipolar technology transistor, it refers to the frequency at which the current gain, with a HF short-circuit output, becomes unity. Figure A.4 below highlights the historical trends of the cut-off frequency of Si BJT's compared to the first SiGe HBT back in the 1990's. From this figure it is apparent how much more superior SiGe HBT's are in terms of gain-bandwidth performance relative to their BJT counterparts, and performance has only been increasing since then.

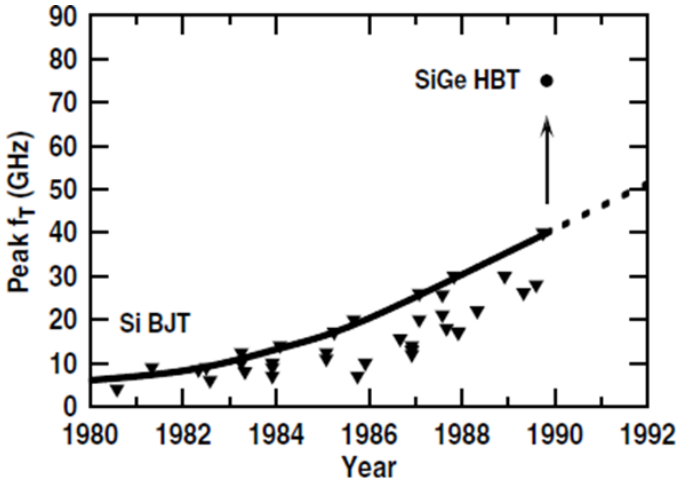


Figure A.4: Historical trends of peak cut-off frequency values for various Si BJTs compared with the first SiGe HBT in the 1990's [41]

One of the most desirable attributes of a SiGe HBT is their low noise capability [41]. Low noise performance is crucial for high-frequency electronics due to the abundant amount of HF electromagnetic interference (EMI) present, along with the need for high sensitivity products. The more sensitive a product is, the more susceptible it is to experiencing noise that will degrade system performance. At a high level, transistor noise (specifically, shot noise) increases as the bias (base) current and forward (collector-emitter) current increase, but as previously stated, gain increases as the bias/forward current increases – so arises another push-pull scenario with performance parameters. As gain increases, noise will also increase, but ideally both parameters would like to be optimized. Since SiGe HBT's can allow for an increased forward current at an equivalent bias current relative to a normal BJT they can achieve larger gains with decreased bias currents compared to BJT's. This consequently decreases the contribution of transistor (shot) noise from bias, while still allowing for increased gain – resulting in overall gain-noise optimization.

Since SiGe HBT's provide an increased frequency response and gain while still boasting low noise capabilities, they have a broad range of applications. SiGe HBT's are found in almost every high-frequency industry such as RF semiconductor development, Aerospace and Defense, Consumer Electronics, Aviation, Telecommunications, and much more. Many different companies have started developing SiGe HBT's such as Infineon, Qorvo, Analog Devices, Qualcomm, Texas Instruments, and many more.

B PHASE NOISE

Phase Noise is defined as the frequency domain representation of phase fluctuations in a signal. This frequency domain measurement is related to the time domain measurement, jitter. Jitter is defined as the time domain representation of phase fluctuations in a signal over time. The simplest example of this is if you were to hook up a signal generator to an oscilloscope and measure a simple sinusoid. Jitter is the horizontal, back and forth movement (phase change) of the signal at a particular time location. Taking the Fourier Transform of an ideal sinusoid, with no jitter, results in a delta function, or single peak, in the frequency domain. By adding phase fluctuations, or jitter, to that same ideal sinusoid, power leaks into the side lobes of the delta function/single peak. Measuring the sidelobe's power level at a particular offset frequency, relative to the carrier (sinusoid), yields phase noise. Phase noise is typically measured in offset frequencies of 10 kHz or 100 kHz and measured with a 1 Hz bandwidth. For example, if a phase noise with a 10 kHz offset of a 1 MHz carrier is measured, the power level from 1.010 MHz to 1.010 MHz + 1 Hz is measured, hence a 1 Hz bandwidth at a 10 kHz offset. This measurement has units of dBc/Hz, which represents decibels (dB) relative to the carrier (c) for a 1 Hz bandwidth.

As previously mentioned, phase noise is considered at both system and component device level. Introducing phase noise into a system can result in many undesirable effects such as an increased noise floor, issues decoding wireless communications, and instability. One example of this is wireless communication systems. When mixers "frequency combine" two signals (i.e., a received RF signal and a defined constant local oscillator LO signal) it is imperative the LO signal is stable with

minimized phase noise. If this signal's frequency is not constant, a phase-changing (and frequency-changing) signal is down-converted. This yields false decoding measurements since systems are reliant upon having a steady, constant LO frequency.

There are many ways to improve phase noise. Generally, at the device level, increasing a signal's magnitude and the corresponding resonant circuit's quality factor minimizes phase noise [32]. One way to generate a clean, steady frequency signal is to use crystals. Crystal-based oscillators use mechanical vibrations within crystals of piezoelectric materials to create resonant frequencies, and hence single frequency electric oscillators. The vibrational resonances observed in crystals are extremely stable, thus creating a stable, steady electric signal, lacking jitter and phase noise. At a higher, system level, one way to mitigate phase noise uses phase-locked loops (PLLs). A PLL is a control system that uses a phase detector, filters, frequency dividers, and a voltage-controlled oscillator (VCO) to control and correct a signal's frequency. The phase detector compares the phase (and hence, frequency) of a reference signal to the VCO output and outputs an error signal applied to the VCO, correcting the output frequency. This negative-feedback loop and error correction scheme ultimately controls the VCO output to "lock" onto a constant frequency.

C METHOD OF MOMENTS (MOM)

Method of Moments is one of the most widely used CEM techniques in the high frequency world [42]. In MoM, radiating and scattering structures are replaced by equivalent surface currents that become discretized in either wire segments or surface patches, also known as meshing. Once discretized, each cell's current density is computed utilizing Green's function. Green's function uses integration techniques to compute closed-form solutions to uncoupled, partial-differential equations, derived from Maxwell's equations [43]. This solution is specifically obtained using a unit source, such as an impulse response, as the driving function. In system theory, Green's function is simply solving the impulse response, or transfer function, of each the segmented sections for its current density. This method enables enhanced computational speed and increased efficiency. It is worth noting that MoM and Green's function only directly solve for the surface current density, while using approximations to account for equivalent substrate and volumetric currents. For this reason, MoM is sometimes only considered a 2.5D EM solver. Additionally, these MoM computations are applied in the frequency domain, hence the working variables are complex, with both magnitude and phase components [42].

Some strengths of Method of Moments are its efficient treatment of conductive surfaces. Since MoM only performs surface meshing, "air" and boundary meshing are eliminated. This increases overall efficiency while still attaining high accuracy surface current modelling. Additionally, MoM automatically incorporates the far-field behavior from the source or "radiation condition," which is particularly important when evaluating radiation or scattering parameters [42]. Conversely, an apparent weakness of MoM is that

is cannot accurately handle pure three-dimensional structures where inhomogeneous materials are used. This is because MoM utilizes surface meshing and to appropriately analyze inhomogeneous three-dimensional structures, volumetric meshing is required. Furthermore, meshing frequency and runtime do not increase together linearly. That is, as frequency of operation, or meshing frequency, increases the runtime will be scaled by the power of six. For example, if the meshing frequency doubles, the runtime can be up to 64 times longer [42] – proving increasingly difficult to work with at higher microwave frequency devices or applications that require finer meshing (i.e., higher a meshing frequency). Nonetheless, Method of Moments is a powerful, efficient, and potentially accurate solver for a majority of RF and microwave circuit applications.

D BILL OF MATERIALS (BOM)

Name	Designator	Quantity	Manufacturer	Manufacturer Part Number
Cap	C1, C2	2	Kyocera AVX	02011JR25ZBSTR
04023J3R0ABSTR	C3, C4	2	Kyocera AVX	04023J3R0ABSTR
CBR04C510F5GAC	C5	1	KEMET	CBR04C510F5GAC
Cap	C6, C14, C20	3	Murata Electronics	GCM1555C1H102FA16D
Cap	C7, C8	2	Kyocera AVX	04021J0R5ZBSTR
Cap	C9, C10	2	Kyocera AVX	04021JR25ZBSTR
02013J0R9PBSTR	C11, C16	2	Kyocera AVX	02013J0R9PBSTR
Cap	C12, C13, C18, C19	4	Kyocera AVX	02011J0R1ZBSTR
02013J2R0ABSTR	C15, C17	2	Kyocera AVX	02013J2R0ABSTR
Cap	C21	1	Cornell Dubilier	FCA1210C105M-G2
ECHU1C104GX5	C22	1	Panasonic	ECH-U1C104GX5
Cap	C23	1	Vishay Vitramon	VJ0805D102JXJQJHT
04023J100FBSTR	C24	1	Kyocera AVX	04023J100FBSTR
D Varactor	D1, D2	2	Skyworks Solutions	SMV1231-040LF
Inductor	L1, L2	2	Kyocera AVX	L0201R47AHSTR\500
LQP03TG0N2B02D	L3, L4	2	Murata	LQP03TG0N2B02D
BFR740L3RH	Q1, Q2, Q3, Q4, Q5	5	Infineon	BFR740L3RH
Res1	R1	1	Yageo	RT0603BRC07500RL
Res1	R2	1	Susumu	RG1608P-1241-B-T5
Res1	R3, R4	2	Stackpole Electronics	RNCF0603TKT1K00
ERA-2AEB183X	R5	1	Panasonic	ERA-2AEB183X
RT0402BRD0791KL	R6	1	Yageo	RT0402BRD0791KL
RG1608N-101-W-T1	R7	1	Susumu	RG1608N-101-W-T1
Res1	R8, R12	2	Panasonic	ERA-2ARB6650X

Res1	R9, R13	2	KOA Speer	RN73R1ETTP1502B25
Res1	R10, R15	2	Yageo	RT0402BRD0710KL
Res1	R11, R14	2	Susumu	RG1005P-201-B-T5
SMA	RF+, RF-	2	Samtec Inc.	SMA-J-P-H-ST-EM1

E ADDITIONAL PERFORMANCE COMPARISON

Table E.1 and Table E.2 compare schematic and layout design performance at tuning voltages of 5.8 V and 6.8 V, respectively.

Table E.1: VCO Schematic vs. Layout Design Single-Ended Output Performance; V_{tune} = 5.8 V

Parameter	Target Specification	Schematic Design	Layout Design	Units
VCO Output Frequency, f_o	4.5 – 5	4.53	3.75	GHz
G_{IN} at f_o	-	-2.05	-4.26	mS
G_T at f_o	-	0.8	1.36	mS
VCO Output Swing	-	257	69	mV_{pp}
Output Power	-5	-7.94	-19.3	dBm
100 kHz Offset Phase Noise	-100	-94.3	-89	dBc/Hz
2nd Harmonic Suppression	-	17.2	32.8	dBc
3rd Harmonic Suppression	-	34.7	29.6	dBc
4th Harmonic Suppression	-	53.7	65.2	dBc
Output Return Loss at f_o	-	-23.6	-0.38	dB
Power Consumption	330	65.3	65.3	mW
Frequency Pushing	-	2	19	MHz/V
Frequency Pulling (2:1 VSWR)	-	45	10	kHz
FOMP[1]	-170	-169.3	-162.3	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Table E.2: VCO Schematic vs. Layout Design Single-Ended Output Performance; V_{tune} = 6.8 V

Parameter	Target Specification	Schematic Design	Layout Design	Units
VCO Output Frequency, f_o	4.5 – 5	4.73	3.93	GHz
G_{IN} at f_o	-	-2.40	-4.62	mS
G_T at f_o	-	0.69	1.15	mS
VCO Output Swing	-	295	54	mV_{pp}
Output Power	-5	-6.73	-21.7	dBm
100 kHz Offset Phase Noise	-100	-94.8	-100.9	dBc/Hz
2nd Harmonic Suppression	-	17.2	40.0	dBc
3rd Harmonic Suppression	-	31.3	24.4	dBc
4th Harmonic Suppression	-	46.8	46.2	dBc
Output Return Loss at f_o	-	-22.2	-0.48	dB
Power Consumption	330	65.3	65.3	mW
Frequency Pushing	-	3	10	MHz/V
Frequency Pulling (2:1 VSWR)	-	N/A	9	kHz
FOM$_P$[1]	-170	-170.1	-174.6	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Table E.3 compares schematic and layout design performance with V_{tune} = 7.8 V, yielding the layout design's highest performance with a minimized FOM$_P$ of approximately -178 dB.

Table E.3: VCO Schematic vs. Layout Design Single-Ended Output Performance; V_{tune} = 7.8 V

Parameter	Target Specification	Schematic Design	Layout Design	Units
VCO Output Frequency, f_o	4.5 – 5	4.88	4.05	GHz
G_{IN} at f_o	-	-2.70	-4.88	mS
G_T at f_o	-	0.59	1.02	mS
VCO Output Swing	-	315	53	mV_{pp}
Output Power	-5	-6.16	-21.7	dBm
100 kHz Offset Phase Noise	-100	-94.9	-103.7	dBc/Hz
2nd Harmonic Suppression	-	16.8	44.2	dBc
3rd Harmonic Suppression	-	29.2	25.2	dBc
4th Harmonic Suppression	-	42.9	38.8	dBc
Output Return Loss at f_o	-	-19.8	-0.54	dB
Power Consumption	330	65.3	65.3	mW
Frequency Pushing	-	3	7	MHz/V
Frequency Pulling (2:1 VSWR)	-	3	13	kHz
FOM$_P$[1]	-170	-170.5	-177.7	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Table E.4 compares schematic and layout design performance with V_{tune} = 10.8 V, yielding the schematic design's highest performance with a minimized FOM$_P$ of -170.6 dB and ≈ 5 GHz oscillation frequency.

Table E.4: VCO Schematic vs. Layout Design Single-Ended Output Performance; V_{tune} = 10.8 V

Parameter	Target Specification	Schematic Design	Layout Design	Units
VCO Output Frequency, f_o	4.5 – 5	5.08	4.20	GHz
G_{IN} at f_o	-	-3.15	-5.24	mS
G_T at f_o	-	0.47	0.89	mS
VCO Output Swing	-	327	46	mV_{pp}
Output Power	-5	-5.80	-22.6	dBm
100 kHz Offset Phase Noise	-100	-94.6	-96.4	dBc/Hz
2nd Harmonic Suppression	-	16.1	43.0	dBc
3rd Harmonic Suppression	-	26.6	23.2	dBc
4th Harmonic Suppression	-	39.1	35.1	dBc
Output Return Loss at f_o	-	-17.2	-0.64	dB
Power Consumption	330	65.3	65.3	mW
Frequency Pushing	-	4	7	MHz/V
Frequency Pulling (2:1 VSWR)	-	82	15	kHz
FOMP[1]	-170	-170.6	-170.7	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$

Table E.5 below compares the schematic and layout designs for the highest 18.3 V tuning voltage. This yields a maximum oscillation frequency for both the schematic and layout designs of 5.18 GHz and 4.28 GHz, respectively.

Table E.5: VCO Schematic vs. Layout Design Single-Ended Output Performance; V_{tune} = 18.3 V

Parameter	Target Specification	Schematic Design	Layout Design	Units
VCO Output Frequency, f_o	4.5 – 5	5.18	4.28	GHz
G_{IN} at f_o	-	-3.40	-5.45	mS
G_T at f_o	-	0.43	0.85	mS
VCO Output Swing	-	328	50	mV_{pp}
Output Power	-5	-5.74	-21.6	dBm
100 kHz Offset Phase Noise	-100	-94.4	-96.8	dBc/Hz
2nd Harmonic Suppression	-	15.8	42.6	dBc
3rd Harmonic Suppression	-	25.4	24.9	dBc
4th Harmonic Suppression	-	37.6	35.7	dBc
Output Return Loss at f_o	-	-16.1	-0.74	dB
Power Consumption	330	65.3	65.3	mW
Frequency Pushing	-	3	2	MHz/V
Frequency Pulling (2:1 VSWR)	-	135	18	kHz
FOM$_P$[1]	-170	-170.5	-171.3	dB

[1] $\boldsymbol{FOM_P = PN - 20log10\left(\frac{f_{carrier}}{f_{offset}}\right) + 10log10(P_{DC}[mW])}$