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FULLY MICROELECTROMECHANICAL NON-VOLATILE MEMORY CELL

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ABSTRACT

This paper reports the first non-volatile memory cell composed entirely of MEM relays that does not need CMOS circuitry for reading or writing. The cell uses a 7-terminal non-volatile relay for information storage and two 3-terminal relays for read and write access. This three-relay cell has been fabricated and characterised to demonstrate read and write operations. The cell architecture has been designed such that multiple cells can be tiled in combination with a relay-based multiplexer to make a digital all MEM reprogrammable non-volatile memory. Such a memory will have near zero standby power and ability to operate in harsh environments beyond the capabilities of conventional memory technologies.

INDEX TERMS

MEMS, Microswitches, Nonvolatile memory, Radiation hardening (electronics), High-temperature

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KEYWORDS

MEMS, Microswitches, Nonvolatile memory, Radiation hardening (electronics), High-temperature

INTRODUCTION

Data storage in harsh environmental conditions characterised by high temperatures and high radiation levels is a requirement in many applications ranging from automotive and manufacturing to space and nuclear decommissioning. To cope with these conditions, conventional CMOS and Flash technologies require additional cooling, special packaging and custom design techniques [1]–[3]. While emerging MRAM and ReRAM memory technologies show potential for integrated non-volatile memory, they are still susceptible to radiation upsets and have similar or worse high temperature resilience as compared to CMOS [2], [4]. Further, they have unresolved development and integration challenges and depend on CMOS driving circuitry. By contrast, MEM-based data storage offers the promise of robust operation at high-temperatures as well as high-radiation levels with near zero standby power across all environmental conditions. However, to date, non-volatile memories either incorporate CMOS and charge storage [5] or focus on singular devices for proof of concept [6]–[9]. By contrast, this work uses a nonvolatile 7-terminal (7-T) rotational relay as the storage device [8], [9], and combines it with two 3-terminal (3-T) relays [10] to produce the first all MEM storage cell including read and write circuitry. As this cell does not depend on stored charge or CMOS addressing circuitry, it can be tiled with the aid of a relay-based multiplexer [11] to produce a fully MEM, addressable memory that consumes near zero standby power and is resilient to high temperatures and high levels of radiation.

DESIGN

Our memory cell uses a 7-T non-volatile rotational relay [8] as the storage element. The straight section of the relay beam (source) is anchored via a short soft hinge that allows the entire suspended beam to rotate anticlockwise to drain D1 by actuating gate pair PG1/AG1, or clockwise to drain D2 by actuating gate pair PG2/AG2 (see Fig. 1). Once rotated, the beam stays switched through surface adhesion forces and can be reprogrammed by actuating the opposing gate pair. The relative balance between the adhesion force, elastic force in the hinge and applied electric force dictates the voltages for rotating from neutral and switched states [9]. A logic '1' is stored by rotating the beam to drain D1, and a logic '0' by rotating it to D2. We use two conventional 3-terminal (3-T) relays [10] where the beam pulls out when the actuation voltage is removed, i.e. volatile behaviour, to enable digital reading and writing as explained below. Having this access circuitry contained within the cell itself allows for simplified control through a read/write line and a data-in signal.

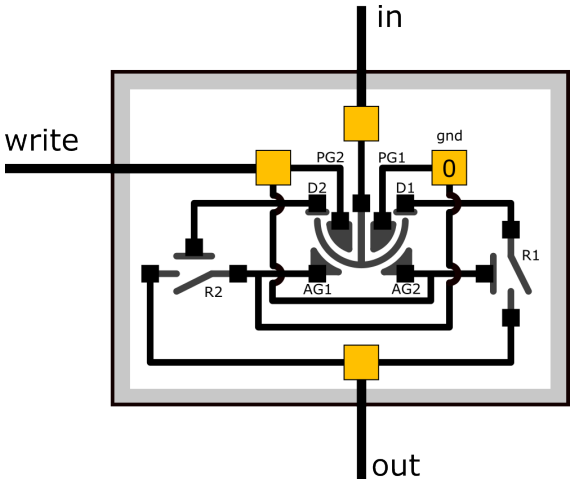


Figure 1: Schematic view of the proposed memory cell architecture consisting of one 7-T device [8] and two 3-T devices [10]. Two logical inputs ("in", "write") and one output ("out") are used for writing and reading the cell. The cell is programmed by switching the central 7-T relay to drain D2 to store a '0', or to drain D1 to store a '1'.

To store a value in the cell, "write" is asserted high, and the value to be stored is presented at "in". The potential difference between the gate pairs and the movable beam causes the beam to either rotate clockwise to contact the drain D2 (if a '0' is present on "in") or anticlockwise to drain D1 (if a '1' is present on "in"). The signal values for writing a '0' and '1' are shown in Fig. 2, top, where the grey cells labelled LUT (short for look up table) cell represent the circuit of Fig. 1. After contact, surface adhesion forces overcome the restorative spring force in the hinge to ensure non-volatility [9] until reprogramming occurs.

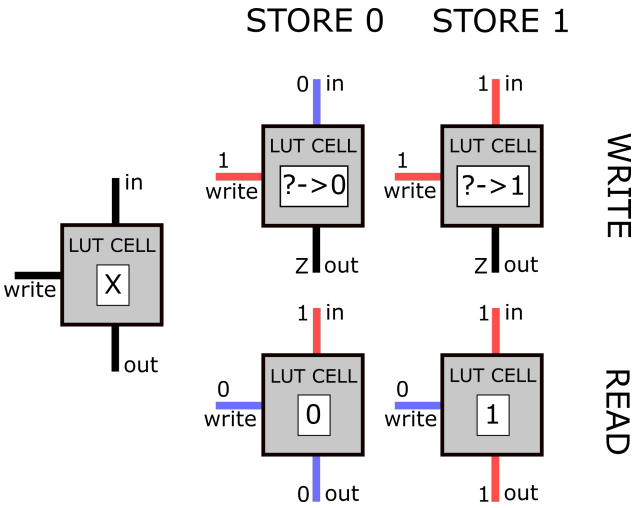


Figure 2: Operating principle of the memory cell showing signals required to read or write a value. Writing a value occurs by asserting "write" and applying the value to "in". Reading is achieved by applying a '1' to "in" and deasserting "write", after which the stored value will present at "out".

To read a stored value, "in" is driven high and "write" driven low, ensuring that all gates of the 7-T relay are grounded so that the clockwise and anticlockwise moments cancel, and the state remains unchanged (i.e. a read upset does not occur). The logic high on "in" propagates through the beam of the 7-T relay to a 3-T relay determined by the stored value. If a '1' was stored the beam of relay R2 in Fig. 1 is driven high, while its gate is driven low via "write". Thus, it pulls in and transmits the stored '1' to "out". Alternatively, if a '0' was stored, the logic high on "in" drives the gate of relay R1, which causes it to pull in as its beam is grounded, propagating a '0' to "out". The signal values for reading a stored '0' and '1' are shown in Fig. 2, bottom.

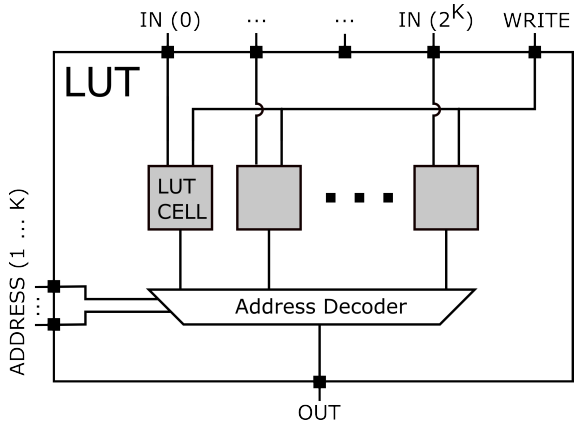


Figure 3: Combining a tiled array of memory cells with a multiplexer [11] to produce a look-up-table memory. All cells are simultaneously written to or read from through the shared "write" signal, with the multiplexer selecting a single value from the array.

This cell architecture has been designed such that multiple cells can be combined to provide a larger MEM non-volatile memory as shown in Fig. 3. Here, the grey cells represent the memory cell of Fig. 1, and all of the cells have a common "write" signal, so that all cells are written to or read from at the same time. With the use of a relay-based multiplexer (such as, for example, demonstrated in [11]) an exclusively MEM relay-based addressing scheme can easily be implemented, preserving the harsh-environment capability and zero standby power of the entire memory.

FABRICATION

The cell was fabricated with critical dimension of 2 μm on a silicon-on-insulator (SOI) chip with device and buried oxide (BOX) layer thicknesses of 5 μm and 4 μm respectively. E-beam lithography followed by deep reactive ion etching was used to pattern the silicon device layer. The moving parts were suspended by etching the BOX using vapour phase HF. Finally, a layer of gold was thermally evaporated to act as the relay contact material and provide a metal layer on top of the probe pads. Two additional pads were introduced into the design to compensate for the lack of a multi-layer interconnect stack, allowing each primary and auxiliary gate-pair connection to be made off-chip. An SEM of a cell after the silicon etch step can be seen in Fig. 4, showing the e-beam written pattern has been cleanly transferred to the silicon device layer.

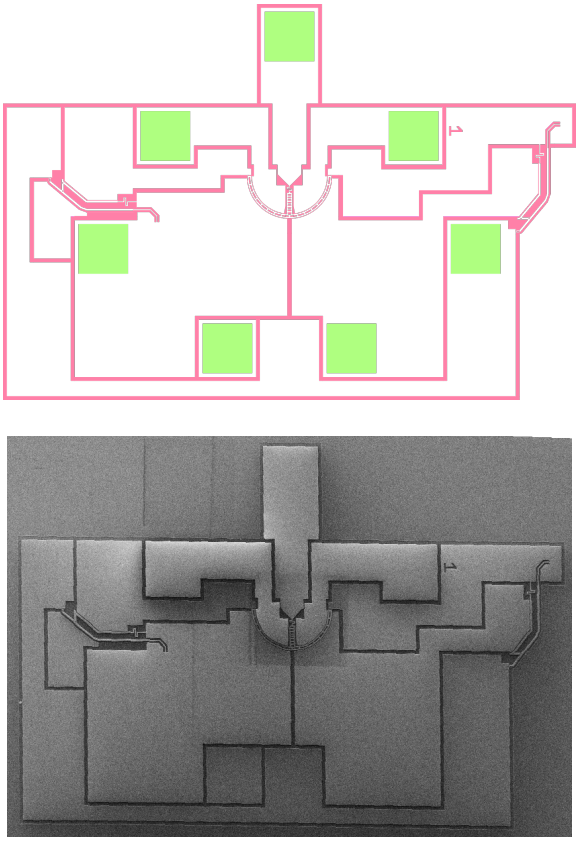
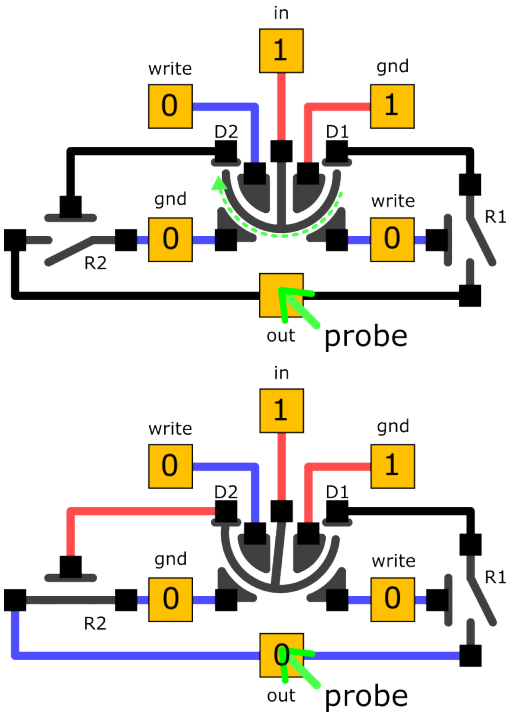


Figure 4: Original GDS design with pad locations marked (top) and SEM (bottom) of the fabricated memory cell before suspension. The circuit is patterned with ebeam lithography on an SOI wafer with 5 μm device layer and 4 μm BOX layer.

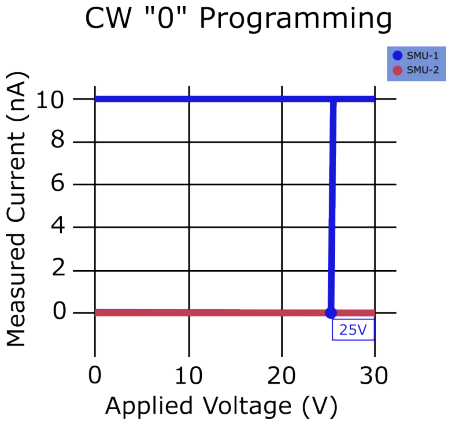
RESULTS

Electrical testing was carried out using a measurement setup equipped with six probes and four source measure-

ment unit (SMU) channels. Each probe was placed on one of the designated pads “in”, “out”, “write”, and “gnd” to either drive it to the requisite voltage or measure the voltage and current. To characterise the cell, first a ’0’ was written and subsequently a ’1’. Due to the specific device layer and BOX layer thicknesses of the wafer used for prototyping (5 μm and 4 μm respectively) and the critical dimension used in the design (2 μm), we saw out-of-plane bending caused by the potential difference across the air gap between the substrate and the beam, when the beam was driven to the pull-in voltage. To minimise the risk of the beams collapsing onto the substrate, we modified the applied voltage patterns, taking advantage of the ambipolar nature of electrostatically actuated relays. Therefore, in order to write a ’0’, i.e. rotate the 7-T beam to drain D2, “in” was driven to ’1’ and gate pair 1 was driven to ’0’ as shown in Fig. 5a, top. At the same time, a bias was applied to the drain of relay R2, and its source grounded. After the 7-T relay completes switching and its beam contacts D2, the gate of relay R2 is driven high, and it pulls in. This event is shown in Fig. 5b, where the voltage on the x-axis is the value applied to the source of the 7-T. Next, the gate voltages were maintained and the voltage on the 7-T relay source ramped down, when the current continued to flow, demonstrating its non-volatile behaviour. The 3-T relay, though designed to be volatile, remained switched after its gate voltage was reduced initially. It was observed to eventually pull out after two days with the gate actuation removed. Following the initial storage of a ’0’ the cell was reprogrammed to ’1’, again by applying a modified pattern to avoid out-of-plane collapse, as shown in Fig. 6a, top. This operation was monitored via relay R1, in a similar fashion to the write ’0’ operation, shown in Fig. 6b. The pull-in was higher as only the principle gate (PG1) and not the auxiliary gate (AG1) of the 7-T relay was driven, due to the limitations imposed by a single layer of wiring and maximum of four SMU channels in our measurement setup. These reprogramming cycles were repeated several times before the gold contact failed and the current compliance of 10 nA could no longer be reached.



(a) Procedure



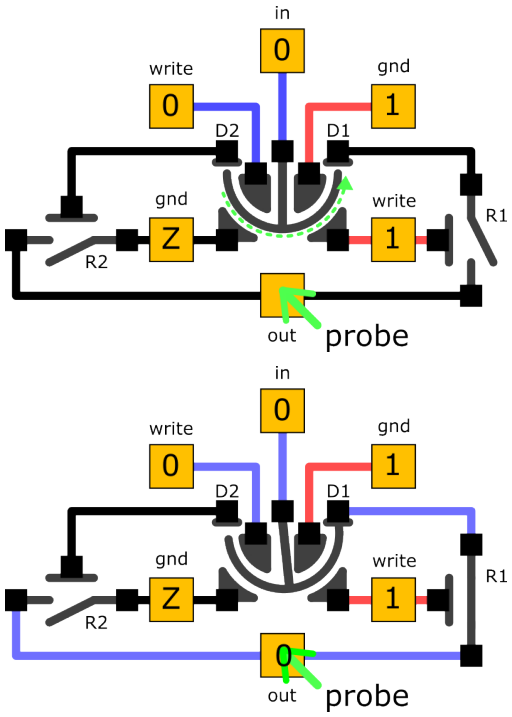
(b) Characterisation

Figure 5: a) Probing procedure to validate functionality of the LUT memory cell being written to ’0’. “In” is driven high, which along with ”write” deasserted causes the 7-T to rotate clockwise to contact D2 (top). This state connects “in” to the gate of R2 to make it pull-in and allow a current to flow between ”out” and ”gnd” (bottom).
b) I-V characterisation ramps up the voltage at ”in” to rotate the 7-T clockwise, close relay R2 and enable current to flow between the bottom left ”gnd” pad and the ”out” pad. Current starts to flow once the pull-in voltage for the 7-T is reached, and continues throughout ramp-down due to the nonvolatile nature of the devices.

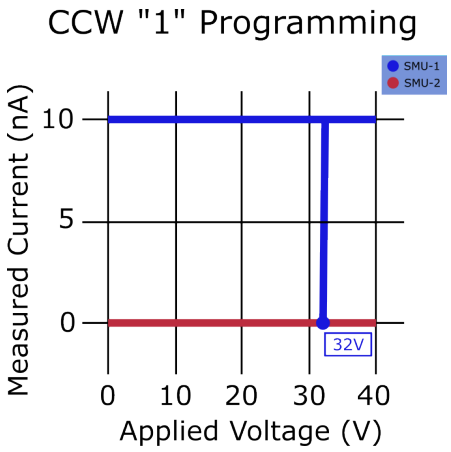
DISCUSSION

In this work we proposed a MEM only non-volatile memory cell combining two types of in-plane relays, a rotational 7-T relay as the storage device, and two 3-T relays for driving it. The cell was designed to be tiled to realise a MEM only memory using a standard word-line / bit-line arrangement. The main challenge we faced was caused by out-of-plane bending due to comparable in-plane and out-of-plane forces when a voltage was applied to the suspended structures. Nevertheless, we achieved proof of concept of the cell operation by utilising a modified access pattern, showing that MEM only memories without the need for CMOS drive circuitry or charge trapping schemes for information storage can be achieved. We expect to resolve the out-of-plane bending by ensuring the BOX layer thickness and critical dimension are such that there is an order of magnitude difference in the in-plane and out-of-plane forces for more robust operation.

Further challenges were encountered with the Au contact layer: high contact resistance; low number of switching cycles; and unpredictability of the surface adhesion force causing variation in switching event behaviour. We expect the number of cycles to increase with a more suitable contact layer such as NCG [10], while a hermetic packaging solution will eliminate contaminants and reduce cycle-to-cycle variation in stiction. Finally, the lack of any additional routing layers can be addressed by a heterogeneous integration scheme [12]. With such an approach, MEM-based logic can be integrated with non-volatile memory on a single chip to provide processing alongside storage. Thus, this work has potential to yield



(a) Procedure



(b) Characterisation

Figure 6: a) Probing procedure to validate functionality of the LUT memory cell being written to '1'. "In" is driven low, which along with "gnd" forced high causes the 7-T to rotate counterclockwise to contact D1 (top). This state connects "in" to the source of R1 to make it pull-in and allow a current to flow between "in" and "out" (bottom). b) I-V Characterisation ramps up the voltage at "in" to rotate the 7-T counterclockwise, close relay R1 and enable current to flow between the "in" and "out" pads. An increased pull-in voltage comes from primary gate (PG1) actuation rather than using the gate pair (PG1 and AG1).

high-temperature, radiation-hard, zero standby power non-volatile memory to serve emerging edge-computing applications that have stringent environmental and power constraints.

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