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Virtual Shifting Impedance Method for Extended Range High-Fidelity PHIL Testing

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***Abstract*—A novel power hardware-in-the-loop interface algorithm, the Virtual Shifting Impedance, is developed, validated and demonstrated in this paper. Building on existing interface algorithms, this method involves shifting a part of the software impedance to the hardware side to improve the stability and accuracy of power hardware-in-the-loop setups. However, compared to existing approaches, this impedance shifting is realized by modifying the command signals of the power amplifier controller, thus avoiding the requirement for hardware passive components. The mathematical derivation of the Virtual Shifting Impedance interface algorithm is realized step-by-step, while its stability and accuracy properties are thoroughly examined. Finally, the applicability of the proposed method is verified through power hardware-in-the-loop simulation results.**

***Index Terms*—power system testing, power hardware-in-the-loop, interface algorithms, real-time simulation, stability analysis, accuracy assessment.**

I. Introduction

HARDWARE-in-the-loop (HIL) methodologies have been proven capable to de-risk and accelerate the deployment of novel power system components, with power hardware-in-the-loop (PHIL) adopted for power components and controller hardware-in-the-loop (CHIL) for controls validation [1]. However, the increasing complexity brought on by the paradigm shift in power system operation through the increased incorporation of distributed generation and digitization, warrants more rigorous validation under extended range of scenarios and corner cases, to ensure a secure operation under high level of expected uncertainty.

For the PHIL simulation case particularly, a power amplifier (PA) unit is required to interface the power hardware device with the system designed in the digital real-time simulator (DRTS) [2], a fact that can introduce additional dynamics to the original system and can cause instabilities and inaccuracies in the PHIL setup. Indeed, for the results of the PHIL simulation to be credible, a proper coordination of the employed devices (e.g. DRTS, signal processing units and PA) needs to be ensured through the use of appropriate PHIL interface algorithms (IAs) [2]. The PHIL interface algorithm basically consists of the PHIL coupling structure (PCS) and the PHIL interface control (PIC). The PCS corresponds to the circuit models to be utilized within the PHIL-IA, one representing the software side and one the hardware side. Each PCS inherits to the total PHIL topology different stability and accuracy properties. A review of different PCSs is performed in [2]–[5], with the most widely used being the ideal transformer model (ITM). The main advantages of ITM are, first, the straightforward and simple implementation and second, its good accuracy, while the main drawback is related to the associated stability issues [5]–[9]. Alternatively, different coupling structures have been found capable of improving the stability of the PHIL setup, like the partial circuit duplication (PCD). In the PCD method, the impedance between the power grid and the power hardware device is duplicated both on the software and the hardware parts of the simulation. Advanced stability properties are also ensured through the damping impedance method (DIM), which is basically combining the ITM and PCD coupling structures. Nevertheless, despite the fact that the stability properties of the PCD and DIM methods are efficient for a wide range of simulation scenarios, a number of issues related to the difficulty of accurately measuring the impedance in the hardware side and introducing it in the software side make those PCSs challenging to be accurately utilized in practice [10]. Another highly stable PCS is the transmission-line model (TLM) which models the assumed one time step delay through the natural propagation delay of a transmission line [11]. Even though TLM decouples the computational tasks and separates the two networks, it has limited practical value due to the necessity of adding a hardware resistor that in turn might lead to an oversizing of the required amplifier [12].

As it is previously mentioned, the second aspect of an IA is the PIC, which can be combined with the appropriate PCS to achieve natural coupling between the simulator and the hardware device under test (DUT). Even though the conventional ITM PCS corresponds to straight-forward implementation and very accurate approach, its stability characteristics are limited. These stability criteria are determined by the PHIL setup impedance ratio (IR), with system tending to instability when the software impedance is greater than the hardware impedance [13]–[15]. To address this issue through the PIC, stability augmentation methods and PHIL control algorithms can be utilized. In fact, a low-pass filter (LPF) is usually employed on the hardware current measurement which is fed back into the DRTS to close the loop [16], [17]. This Feedback Filtering (FBF) method has been found to be stabilizing the PHIL setup, nevertheless, the utilized LPF reduces the accuracy of the system. To alleviate this need for low-pass filtering, advanced IAs are being investigated, aiming to realize at the same time stable and accurate

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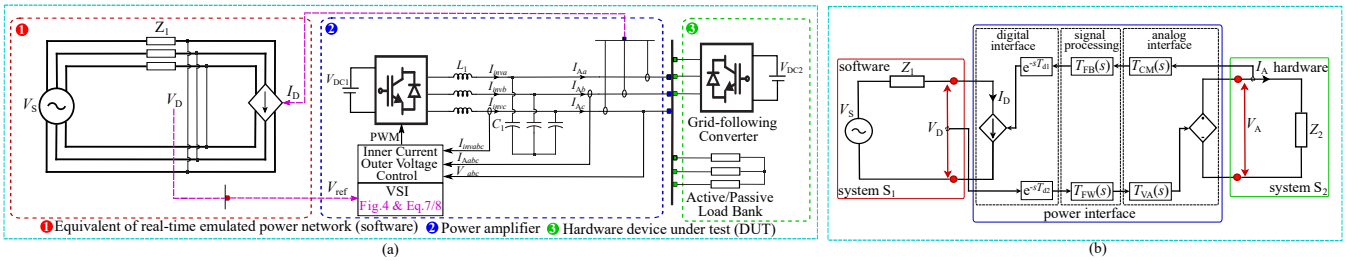


(a) (b)

Fig. 1: (a) A representation of the PHIL setup, and (b) equivalent PHIL interface modelling.

PHIL testing, e.g. through optimal control approaches [7], interface compensation approaches [8], Smith-predictor based stabilization schemes [15], [18], as well as delay compensation techniques [8], [19], while advanced analysis tools have been also reported, such as discrete domain modeling in [6]. Among the various PHIL algorithms that have been proposed to improve stability and accuracy, the delay signal compensation (DSC) method manages to compensate for the delays of the system [8], [19] in a straight-forward manner. Nevertheless, it still requires a LPF on the feedback path to maintain a stable system operation, which compromises its accuracy improvement capability. Methods that improve accuracy by reducing the requirement for LPF have recently been proposed based on the concept of introducing a virtual series or parallel impedance through the interface algorithm or through shifting a part of the software impedance to the hardware side [14], [20]–[24]. Nevertheless, the introduced virtual impedance in the methods proposed to this day are not part of the original system of investigation and may thus lead to inaccurate results. On the other hand, shifting a part of impedance to the hardware requires having impedances of different values readily available at hand to perform multiple test cases, a stringent requirement for most research laboratories.

To address the above issues, a novel IA, the Virtual Shifting Impedance (VSI) method, is proposed in this paper to realize extended-range accurate and stable PHIL testing. The main contributions of the paper are summarized below:

- A virtual implementation of the shifting impedance algorithm has been proven to be extending the range of stable PHIL simulations, without a need for additional hardware components.
- At the same time, the VSI has been rigorously proven to be offering a substantially improved accuracy, compared to legacy methods, throughout its range of operation.
- Extensive simulation and PHIL results have validated the proposed VSI algorithm and its superiority compared to legacy methods.

Particularly, building on existing IAs [14], [23], this method virtually introduces a shifted impedance through the control scheme of the PA unit to accurately extend the range of stable scenarios to be simulated through the PHIL approach. The mathematical derivation of the VSI method is analytically given, while its stability and accuracy properties are thoroughly examined. Finally, the applicability of the proposed IA is verified through extensive PHIL experimental results.

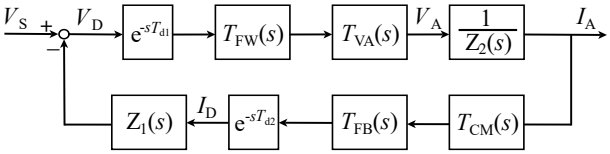


Fig. 2: V-ITM interface modelling and equivalent block diagram.

II. Challenges in Stability and Accuracy of PHIL Testing

A. System Modeling and Interfacing

A typical PHIL setup comprises a simulated power network in a DRTS interfaced to power hardware via a PA in a closed-loop configuration enabling testing under a safe and controlled environment. As it was discussed above, a PHIL-IA defines the configuration of the interfacing elements of the PHIL setup. A number of PCSs have been proposed in the literature [2], [3], [22], however, the voltage-type ideal transformer model (V-ITM) has been extensively preferred over the past decade as it offers acceptable stability and accuracy yet is simple in terms of its implementation. Hence, for the sequel of this paper V-ITM will be considered as the PCS of the IAs under discussion, which in fact are focusing on the PHIL control algorithms aspect.

In the V-ITM, the device under test (DUT) is modeled as a current sink in the simulation and the PA acts as a voltage source, as shown in Fig. 1. The appropriate control of the current sink and the voltage source can realize a relatively accurate and stable PHIL setup. The entire PHIL setup, including the simulated and hardware system along with the interfacing components, can be represented as a single-input-single-output (SISO) closed-loop system, whose equivalent block diagram is illustrated in Fig. 2. The system open-loop transfer function $F_{\mathrm{O}}(s)$ is given by:

$$F_{\mathrm{O}}(s) = \underbrace{e^{-sT_{\mathrm{d1}}} T_{\mathrm{FW}}(s) T_{\mathrm{VA}}(s)}_{FF(s),\ \text{feed-forward}} \frac{Z_1(s)}{Z_2(s)} \underbrace{e^{-sT_{\mathrm{d2}}} T_{\mathrm{FB}}(s) T_{\mathrm{CM}}(s)}_{FB(s),\ \text{feed-back}}, \tag{1}$$

where T_{d1} and T_{d2} represent the time delay of the digital interface in the feed-forward and feedback path respectively, $T_{\mathrm{FW}}(s)$, $T_{\mathrm{FB}}(s)$ represent the signal processing units, $T_{\mathrm{VA}}(s)$ and $T_{\mathrm{CM}}(s)$ represent the equivalent transfer function of the PA and current sensor, respectively, $Z_1(s)$ (i.e., $R_1 + sL_1$) and $Z_2(s)$ (i.e., $R_2 + sL_2$) represent the equivalent impedances in the simulation and hardware side respectively.

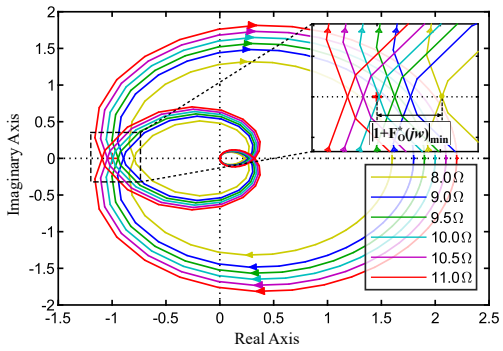


Fig. 3: Nyquist plot of the open-loop transfer function of the PHIL system with variable software impedance.

B. PHIL Stability Analysis

Based on the open-loop transfer function $F_{\mathrm{O}}(s)$ of the PHIL closed-loop system in Fig. 2, the system stability can be analyzed by applying the Nyquist stability criterion [25] to the system characteristic equation, which is given by

$$1 + F_{\mathrm{O}}(s) = 0. \tag{2}$$

A practical implementation of V-ITM inherently comprises non-idealities compared to that of an ideal theoretical V-ITM interface implementation. These non-idealities include time delay, dynamics of the PA and the non-unity gain to name a few. While all the characteristics play a role in determining the stability of a closed loop PHIL system, the stability and its analysis is dominated by the ratio of the impedance between the software side and the hardware side - referred to simply as IR. Taking a PHIL system with hardware side impedance of $Z_2 = 5 + s0.001\,\Omega$ and aggregated time delay of $250\mu s$ as an example, Fig. 3 presents the Nyquist plot of the open-loop transfer function of the PHIL system with variable software side impedance (Z_1). As can be observed, with the increase in the software impedance, the Nyquist curve tends towards the critical point (-1,0), representing an unstable system once the critical point has been encircled. Therefore, the system stability is susceptible to variations in impedance and presents a limitation in realization of stable PHIL setups.

C. Methods for Stability Enhancement

With the IR between the simulation and hardware side as a key determinant of the PHIL stability, many research efforts have been devoted to improving the stability of the setup by physically or artificially manipulating the IRs. The approaches adopted for enhancement of stability can be broadly classified into two: (i) approaches that manipulate the interface signals (such as the voltage or current) or (ii) approaches that manipulate the impedances of the two systems (hardware or software). Three commonly adopted practices for stability improvement discussed below, first of which manipulates the interface signal and the latter two the impedance of the setup.

- Feedback Filtering Method: Most of the times, a low-pass filter (LPF) is utilized in the feedback path to improve PHIL setup stability [14]. The addition of the LPF impacts the current and therefore classes under approaches that manipulate the interface signals. While the inclusion of a LPF has proven to improve the stability of the system, lower cut-off frequencies can lead to unacceptable inaccuracies and the approach also fails to stabilize systems of high IRs.
- Virtual Impedance Insertion Method: In [20], a method of virtual impedance insertion is proposed to reduce the IR between simulation and hardware side. This is achieved by inserting an extract shunt capacitance within the simulated network, thereby reducing the equivalent impedance of the simulation side. However, the system stability is improved at the expense of deteriorated accuracy, arising from the inserted additional component, especially in cases that appropriate shaping or compensation does not take place.
- Physical Shifting Impedance Method: As the name suggests, a portion of the impedance from simulation side is physically shifted to the hardware side, thereby changing the IR of the PHIL setup and improving stability in a simple manner. As no additional component is added, theoretically this approach offers no deterioration in accuracy. In practice, as has been reported in [14], the approach still requires the inclusion of a LPF in the feedback path. However, higher cut-off frequency suffice to ensure the stability, and therefore the deterioration in accuracy is limited. Nevertheless, the required hardware impedance to be incorporated in the hardware system limits the applicability of this method.

III. The Proposed Interface Algorithm

With the limitations of the approaches in literature identified, this paper proposes a novel stability enhancement interface algorithm that incorporates the principles of both, the manipulation of interface signals and the manipulation of the IR. The proposed approach is the Virtual Shifting Impedance (VSI) method. The forward interface signal, voltage in this case, is manipulated in the controller of the PA to represent the voltage after the shifted impedance. This manipulation of the interface signal emulates the physical shifting impedance and thereby improves the stability of the PHIL setup. The practical implementation of the approach is realised through the advanced control capabilities of modern PAs, where a virtual impedance algorithm within the inner control loop can realise the implementation of the VSI method.

As in the modelling description in Section II-A, consider that the initial software system impedance is

$$Z_1 = R_1 + jX_1. \tag{3}$$

Aiming to shift a portion of Z_1 to the hardware System 2, inspired by [14], and assuming that the ratio of the shifted resistance and reactance is a, with $a \in (0, 1)$, then the new software system impedance is

$$Z_{1n} = (1 - a)R_1 + j(1 - a)X_1. \tag{4}$$

Assume the voltage after impedance Z_{1n} is V_{D}. With the software impedance reduced, the voltage after the original system impedance Z_1 is to be emulated by the PA to realise

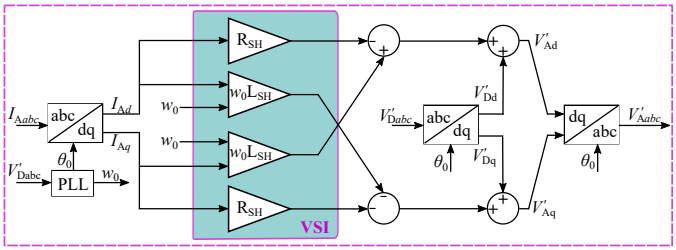


Fig. 4: Virtual Shifting Impedance algorithm implementation.

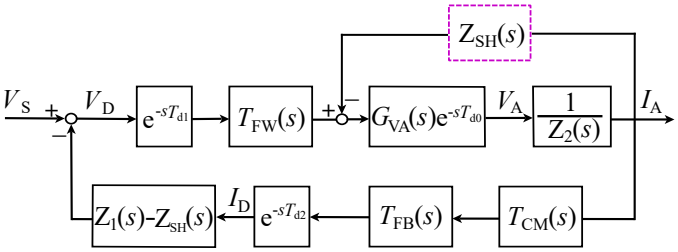


Fig. 5: Equivalent block diagram of PHIL system with VSI.

the virtual shift in impedance and ensure accurate simulation. In fact, the voltage $V'_{\rm A}$ can be obtained by subtracting the voltage drop across the shifted impedance $R_{\rm sh} = aR_1$ and $X_{\rm sh} = aX_1$ from $V'_{\rm D}$ as described in [26]

$$V'_{\rm Ad} = V'_{\rm Dd} - R_{\rm SH} I_{\rm Ad} + \omega_0 L_{\rm SH} I_{\rm Aq} - L_{\rm SH} \frac{dI_{\rm Ad}}{dt} \quad (5)$$

$$V'_{\rm Aq} = V'_{\rm Dq} - R_{\rm SH} I_{\rm Aq} - \omega_0 L_{\rm SH} I_{\rm Ad} - L_{\rm SH} \frac{dI_{\rm Aq}}{dt}. \quad (6)$$

This makes it feasible to generate the voltage at the output of the shifted impedance by manipulating the reference voltage of the PA, without requiring the addition of any hardware impedance component in System 2. The steady-state approximation of the virtual impedance implementation, widely used in inverter control schemes, can also be adopted to overcome practical implementation issues [27]–[29]. The inclusion of the transient (derivative) term in the control action can lead to possible amplification in noise, requiring a low-pass filter that can deteriorate the response of the proposed method. In addition, the incorporation of the derivative term also increases the computational burden significantly. Therefore, ignoring the derivative dynamic term, the reference voltage takes the form

$$V'_{\rm Ad} = V'_{\rm Dd} - R_{\rm SH} I_{\rm Ad} + \omega_0 L_{\rm SH} I_{\rm Aq} \quad (7)$$

$$V'_{\rm Aq} = V'_{\rm Dq} - R_{\rm SH} I_{\rm Aq} - \omega_0 L_{\rm SH} I_{\rm Ad}, \quad (8)$$

where $V'_{\rm A}$ is the manipulated reference voltage of the inner voltage control scheme of the PA and $I_{\rm A}$ is the current of the hardware system. The implementation of the VSI methodology is depicted graphically in Fig. 4 that is practically implemented in the PA's control card, as shown with in Fig. 1. The original impedance of the hardware system remains the same, i.e. $Z_2 = R_2 + jX_2$, without requiring the additive physical impedance, as it would in the PSI method case.

IV. Stability Analysis

This section presents the stability analysis of a PHIL setup with VSI. First, the transfer function of a PHIL setup with VSI is derived, followed by derivation of the minimum shifted impedance required to ensure stability of any given system. The section further presents analytical stability assessment of PHIL systems with both FBF and VSI methods to establish the effectiveness of the proposed approach.

A. Stability Conditions

The virtual impedance shifting implemented in (7) and (8) can be further modelled as an equivalent impedance ($Z_{\rm SH}$), arising as an additional feedback loop to manipulate the reference signal of the power amplifier. The equivalent block diagram of the PHIL system with VSI method implemented is illustrated in Fig. 5, whose open-loop transfer function is given by (9).

Assuming the transfer functions of signal processing, measurement units and PA as unity and substituting $Z_{\rm SH}(s) = aZ_1(s)$ into (9), the open-loop transfer function of VSI-based PHIL system can be written as:

$$F^*_{\rm O}(s) = \frac{(1-a)Z_1(s)}{Z_2(s) + aZ_1(s)e^{-sT_{\rm d0}}} e^{-s(T_{\rm d0}+T_{\rm d1}+T_{\rm d2})}. \quad (10)$$

Accordingly, the system characteristic equation is given by:

$$1 + \frac{(1-a)Z_1(s)}{Z_2(s) + aZ_1(s)e^{-sT_{\rm d0}}} e^{-s(T_{\rm d0}+T_{\rm d1}+T_{\rm d2})} = 0. \quad (11)$$

According to the Nyquist stability criterion [25], the minimum PHIL system stability margin is the shortest distance between $F^*_{\rm O}(jw)$ and the critical point (-1,0) in the polar diagram as presented in Fig. 3. The condition for the minimum stability margin is achieved when the real-part of $F^*_{\rm O}(jw)$ is greater than -1, and can be represented as

$$\Re\{F^*_{\rm O}(jw_0)\} + 1 > 0, w_0 = \left\{ \arg\min_{w\in\mathbb{R}} |1 + F^*_{\rm O}(jw)| \right\} \quad (12)$$

Using the condition for marginal stability, the minimum VSI ratio a can be determined. Substituting (9) into (12) yields the shifting impedance at marginal boundary for stabilizing the PHIL system.

B. Analytical Stability Assessment

This section presents the stability assessment of the VSI-based PHIL system along with a comparison against the conventional FBF method. As given in Table I, two sets of hardware impedance are employed to emulate different impedance ratios and to assess the stability boundary of the VSI method. The remainder of the PHIL interfacing component parameters have been identified in Table I. The stability performance of VSI (with different shifting IRs) and

$$F^*_{\rm O}(s) = e^{-sT_{\rm d1}} T_{\rm FW}(s) \frac{Z_1(s) - Z_{\rm SH}(s)}{Z_2(s) + e^{-sT_{\rm d0}} G_{\rm VA}(s) Z_{\rm SH}(s)} e^{-sT_{\rm d0}} G_{\rm VA}(s) T_{\rm FB}(s) T_{\rm CM}(s) e^{-sT_{\rm d2}} \quad (9)$$

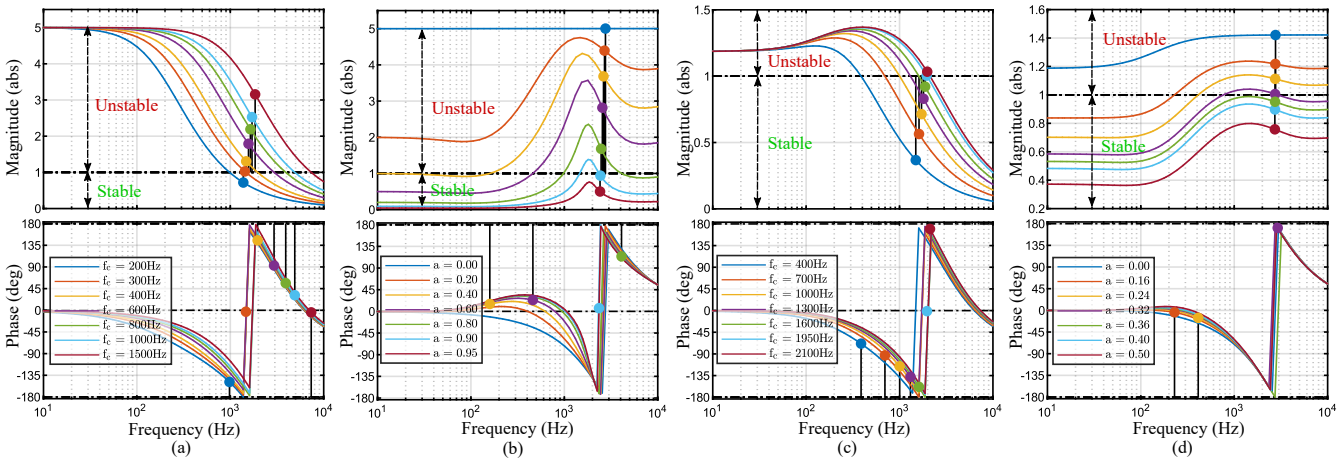


Fig. 6: Bode plot of (a) PHIL (set 1) with FBF, (b) PHIL (set 1) with VSI, (c) PHIL (set 2) with FBF, (d) PHIL (set 2) with VSI.

TABLE I: System parameters for performance validation.

Description	Symbol	Unit	Value	
Time delay of power amplifier	T_{d0}	µs	130	
Time delay of digital interface in feed-forward path	T_{d1}	µs	30	
Time delay of digital interface in feed-back path	T_{d2}	µs	40	
Delay-free part of power amplifier transfer function	$G_{\mathrm{VA}}(s)$	-	1	
Feed-forward signal processing	$T_{\mathrm{FW}}(s)$	-	1	
Feed-back signal processing	$T_{\mathrm{FB}}(s)$	-	FBF	VSI
			$\frac{1}{\frac{s}{2\pi f_c}+1}$	1
System impedance set	-	-	Set 1	Set 2
Hardware impedance	R_2	Ω	0.16	0.24
	X_2	Ω	0.0628	0.221
Software impedance	R_1	Ω	0.8	0.8
	X_1	Ω	0.3124	0.3124
Impedance ratio (**IR**)	$\lvert Z_1\rvert/\lvert Z_2\rvert$	-	5	1.2

convectional FBF method (with different cut-off frequencies) for the two impedance sets are investigated with the frequency responses of the open-loop transfer function shown in Fig. 6.

The PHIL system with impedance Set 1 presents a high IR (IR = 5) that requires a LPF with cut-off frequency that is rated below 300 Hz to maintain its stability as presented in Fig. 6a. However, this stability is achieved at the expense of deteriorated accuracy and limited bandwidth which degrades the fidelity of the PHIL system. The VSI-based interface can stabilize the system with such high IR with a virtual impedance shifting ratio around 90 %, as presented in Fig. 6b, without the limitation in bandwidth as presented in the FBF method.

The PHIL impedance Set 2 presents a lower IR that can be stabilized by a LPF with higher cut-off frequency (∼1900 Hz) than that required by the PHIL with impedance Set 1, as presented in Fig. 6c. Although a higher cut-off frequency is utilized, this still limits bandwidth and accuracy. As illustrated in Fig. 6d, the VSI-based interface can stabilize the PHIL system with a minimum impedance shifting ratio (∼32 %).

V. Performance Validation

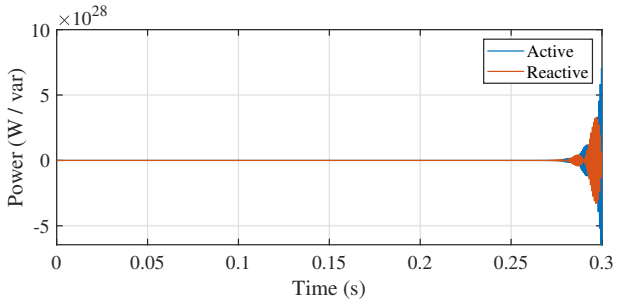
In this section, the performance of the proposed VSI method is validated in simulation. The VSI offers two distinct advantages: (i) extends the range of realisable PHIL setups, not otherwise possible through conventionally available stability enhancement approaches in literature and (ii) improved accuracy for PHIL setups where stability can otherwise be achieved by employment of conventional approaches. This section will present two cases, one for the extended range of PHIL setups that can be realized and the second on the enhancement of accuracy. In both cases, the performance of the VSI will be compared to that of the FBF method. The two sets of IR employed in stability analysis are again utilized, as presented in Table I. The following sub-sections will present the performance evaluation in detail.

A. Extending the Range of Realisable PHIL Setups

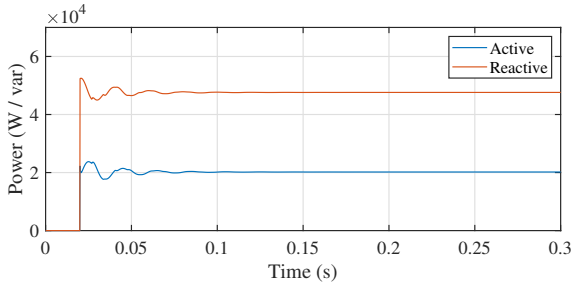
The first set of hardware impedance chosen leads to an unstable PHIL setup that remains unstable even with the incorporation of a very low cut-off frequency LPF, i.e., 300 Hz (as shown in Fig. 7). To the best of author's knowledge, the utilized cut-off frequency is less than the lowest reported feedback LPF tuning found in literature, i.e., 350 Hz in [30]. The VSI method is able to realize a stable PHIL setup with a software impedance shift of 90 % as shown in Fig. 7 (in accordance with the analytical stability assessment presented in previous sub-section). This clearly demonstrates the capability of the proposed approach to extend the range of realisable PHIL setups, enabling the validation of novel technologies and controls in broader range of scenarios than feasible with conventional approaches.

B. Accuracy Enhancement

This section evaluates the improvement in accuracy that the proposed VSI approach offers over the FBF method. The second set of hardware impedance is utilized for the implementation of the PHIL setup. For a fair assessment, the accuracy is assessed with the realization of the setup at the boundary of stability i.e, a marginally stable system. For the



(a) Using Feedback Filtering method.



(b) Using Virtual Shifting Impedance method.

Fig. 7: Simulation results using FBF and the VSI methods.

TABLE II: Accuracy assessment.

Metric	Feedback Filter	VSI (32%)	VSI (90%)
η_{P}	1.64 %	1.25 %	1.51 %
η_{Q}	11.35 %	8.79 %	10.68 %

FBF method, this is with the incorporation of the LPF with a cut-off frequency that leads to a marginally stable PHIL setup. Similarly, for the VSI approach, the amount of impedance shifted is such that it realizes a marginally stable PHIL setup.

To aid the assessment of accuracy, a metric capable of quantifying the resulted accuracy in steady-state is needed. In this regard, as presented in [8], the power tracking error (PTE) is defined as

$$\begin{cases} \eta_{\mathrm{P}} = \frac{|P(t)-P^{'}(t)|}{|P(t)|} \\ \eta_{\mathrm{Q}} = \frac{|Q(t)-Q^{'}(t)|}{|Q(t)|} \end{cases} \tag{13}$$

where $P(t)$ and $Q(t)$ are the active power and reactive power measured at the source of the monolithic system of interest (SoI), respectively. Moreover, $P^{'}(t)$ and $Q^{'}(t)$ are the active power and reactive power at the source of the simulated PHIL setup under investigation, respectively.

The maximum allowed LPF to stabilize the chosen PHIL setup is 1800 Hz, while an impedance shift of 32 % realizes a marginally stable setup for the VSI case. The results of the accuracy assessment in steady state are presented in Table II. As can be observed, the proposed approach outperforms the FBF approach. This demonstrates the enhancement in accuracy that the proposed approach offers over conventional approaches, enabling more accurate PHIL testing of novel technologies and controls.

C. Applicability: VSI vs FBF

An additional scenario is also investigated, where a high share of impedance (90 %) is virtually shifted to the hardware side. The results are presented in Table II. While it is intuitive that a very stable implementation is realised, it is interesting to note that the accuracy of the approach is deteriorated. However, it should be noted that even with such high percentage of virtual impedance shift, the proposed approach outperforms the FBF approach that is at marginal stability (higher stability through FBF implies use of smaller cut-off frequency and therefore higher inaccuracy). To support generalization, the investigation has been repeated for varied IRs from 1 to 2. In that case, the shifting ratio required to stabilise the system increases with the increase in IR, as it was also proven in the stability analysis. However, for all cases considered, the accuracy of the system with 90 % shifting ratio is still better than with the incorporation of FBF realising marginal stability. Hence, for cases considered, the VSI should be chosen for implementation over the FBF, while for much higher IRs, it has been proven that VSI is the only viable option. However, two factors can limit its employment:

- Availability of suitable PA: The implementation of VSI required the availability of a power amplifier that allows the manipulation of reference signals through a control card. In case of unavailability, the FBF approach can be adopted within the DRTS.
- Determining a: If the IR of a PHIL setup is not known, determining the minimum shift in impedance can be a challenge for users not familiar with stability analysis.

A simple procedure to determine the impedance shift can however be adopted. As the accuracy of the VSI with 90 % shift is better than the accuracy of FBF, a quick confirmation of stability can be performed at this value. If a stable setup is realised with 90 % shift in impedance, the value of shifted impedance can be reduced in decrements of 10 %. While this still serves as a trial-and-error approach, it simplifies the process of utilizing VSI and its proven unique features.

VI. Laboratory Validation

Having established the superior performance of the proposed approach by means of simulations and analytical assessments, this section establishes its practical applicability through experimental validation. The experiments were undertaken in the Dynamic Power System Laboratory (DPSL) at the University of Strathclyde, Glasgow, United Kingdom. The experimental setup, as shown in Fig. 8, comprises a real-time digital simulator from RTDS technologies, a Triphase 90 kVA voltage source back-to-back converter (TP90 kVA) acting as the PA, and a 256-step passive load bank as DUT. An equivalent voltage source with a nominal Line-to-Line AC voltage $V_{\mathrm{S,LL}}$ of $0.4\,\mathrm{kV}$ and a low X/R ratio grid impedance, as given in Table III, are emulating a low-voltage grid within the DRTS side. The TP90 kVA power amplifier bridges the DUT (i.e., static load bank) and the DRTS. The signal conversion between DRTS and TP90 kVA is achieved by leveraging two signal conversion cards (i.e., giga-transceiver analog output (GTAO) card and giga-transceiver analog input

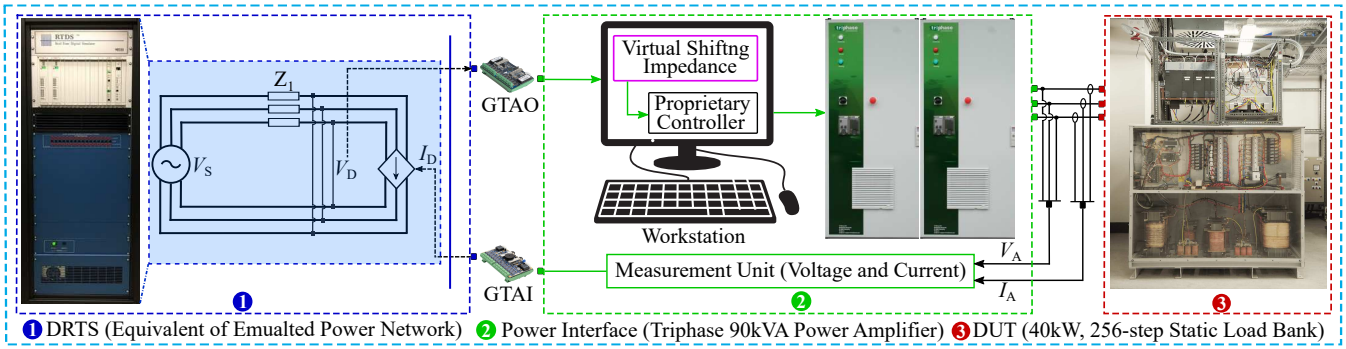


Fig. 8: PHIL experimental setup.

TABLE III: PHIL experimental setup Parameters.

Description	Symbol	Unit	Value
Software side voltage source	$V_{\mathrm{S,LL}}$	V	400
System fundamental frequency	f_0	Hz	50
Total time delay	T_d	µs	250
Software side impedance	Z_1	Ω	12
Hardware side impedance	R_2	Ω	11.5
	X_2	Ω	0.3141
Power amplifier (TP90 kVA) [31]			
DC voltage	V_{DC}	V	700
PWM switching frequency	f_{sw}	kHz	16
Sampling frequency	f_s	kHz	16
Inverter side filter inductance	L_f	mH	0.5
Filter capacitance	C_f	µF	47
Emulated virtual resistance	R_e	Ω	6.842
Emulated virtual inductance	L_e	mH	0.05

(GTAI) card. The remainder of the parameters for this PHIL setup are presented in Table III.

To realize the V-ITM structure, as shown in Fig. 8, the digital voltage signal V_{D} measured at the point of common coupling of the equivalent network is transmitted to TP90 kVA as its command signal, which is manipulated by the proposed VSI unit, when the latter is enabled. The current response of the passive load bank I_{A} is then measured and transmitted to the DRTS as the command signal for the controllable current source. The digital signal V_{D} and analog signal I_{A}, are recorded by RTDS and Triphase datalogger with a sampling rate of 20 kHz and 16 kHz, respectively. For the validation that follows, the software and hardware side impedances are presented in Table III, selecting an IR greater than 1, which poses a challenge for PHIL stability. The following subsections present a comparative assessment of the FBF and VSI methods, regarding their performance in stabilizing a PHIL setup and maintaining an accurate response.

A. Assessment of the FBF Method

Fig. 9 presents the hardware current signal I_{A} of the FBF-aided PHIL setup, which incorporates a LPF with different cut-off frequencies. Before the FBF is enabled, as illustrated in Fig. 9, the hardware side current presents remarkable oscillations, as such the PHIL system tends to instability. When the FBF is enabled, the hardware current presents fewer

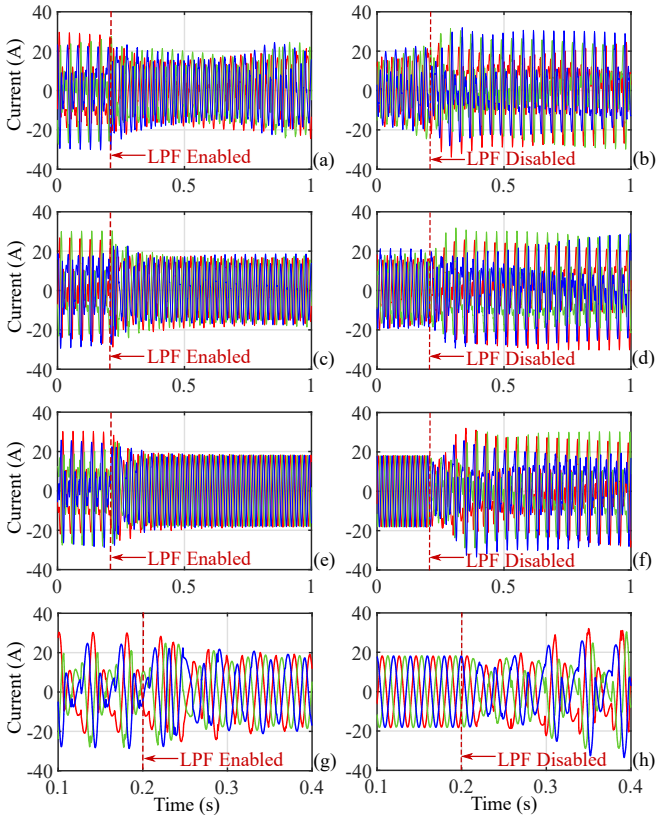


Fig. 9: Hardware side current behavior of the LPF-based PHIL setup with cut-off frequency: (a),(b) 100 Hz, (c),(d) 75 Hz, (e),(f) 50 Hz, (g) zoomed in version of Fig. (e), and (h) zoomed in version of Fig. (f).

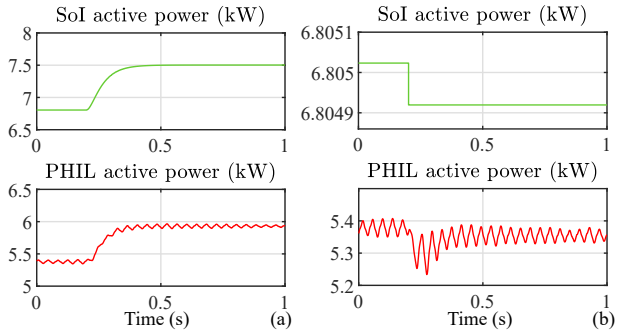


Fig. 10: Grid side active power of LPF-aided PHIL setup that is subject to (a) voltage step change, and (b) frequency step change.

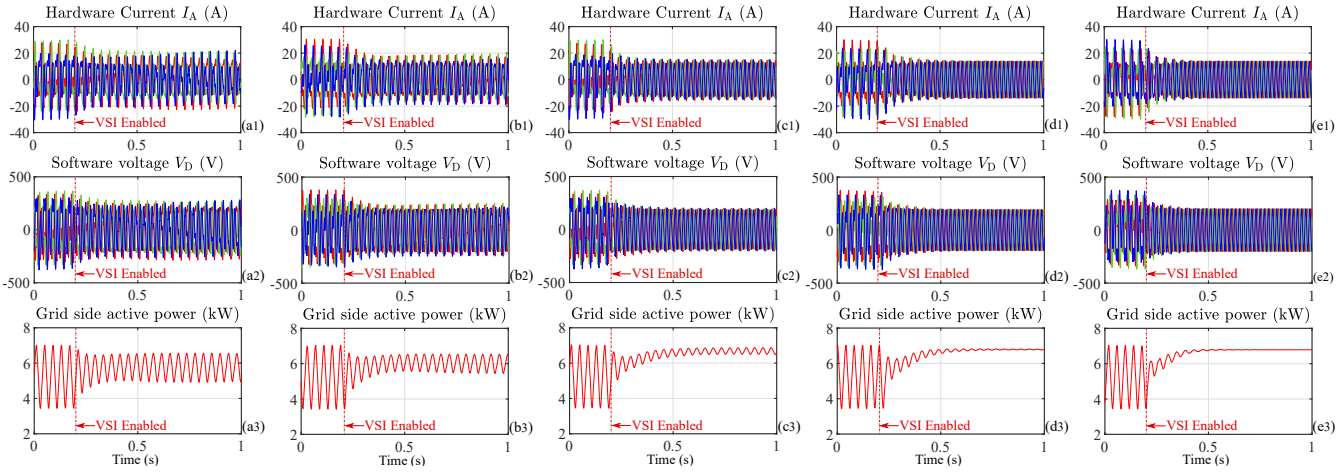


Fig. 11: VSI-aided PHIL setups with different shifting impedance R_{sh}: (a) 1.0 Ω (a=8.3%), (b) 1.5 Ω (a=12.5%), (c) 2.0 Ω (a=16.7%), (d) 2.4 Ω (a=20.0%), and (e) 3.0 Ω (a=25.0%).

oscillations compared to the previous case. However, as shown in Fig. 9(a), (c), and (e), only with a significant decrement of the LPF cut-off frequency to the range of 50 Hz, the hardware current of the PHIL setup converges to a sinusoidal response.

Even if a LPF with an extremely low cut-off frequency can stabilise a PHIL, this comes at the expense of the accuracy of the PHIL setup. In particular, as shown in Fig.10, when the software side voltage source $V_{\text{S,LL}}$ witnesses an amplitude step variation from 0.4 kV to 0.42 kV and a frequency step change from 50 Hz to 50.5 Hz, the active power of the PHIL setup (implemented with FBF with 50 Hz cutoff frequency) presents significant discrepancies compared to the original SoI. In fact, for these two test scenarios, the active power PTEs are 20.67% and 20.86%, respectively. Hence, it is validated that the enhanced stability is achieved at the expense of a reduced PHIL closed-loop system bandwidth and a deteriorated accuracy. The former is attributed to the implementation of the LPF, where an extremely-low cut-off frequency is needed to stabilise the PHIL setup. While the latter arises from the non-unity magnitude and non-zero phase response of the LPF, it leads to magnitude distortion and phase lag of the PHIL interfacing signals. These attributes significantly limit the applicability of the FBF method in stabilising a PHIL setup.

B. Performance Evaluation of VSI Method

To validate the effectiveness of the proposed VSI method in stabilising a PHIL setup, the VSI unit is applied to the PHIL setup, as presented in Fig. 8, while considering different shifting IRs a. The hardware current, software voltage and active power responses are presented in Fig. 11. As is evident, the implementation of the proposed VSI method mitigates the active power oscillations of the PHIL setup to a lower level compared to the case of the PHIL setup without VSI. Moreover, with the impedance shifting ratio increment, the power signals tend to converge and present fewer oscillations. The VSI-aided PHIL system reaches a stable state once the shifting IR a satisfies the stability criterion defined in (12). As shown in Fig. 11(d) and Fig. 11(e), once the shifting IR is sufficient enough to stabilise the PHIL setup, the higher the shifting IR is, the faster the power signals converge to a stable state.

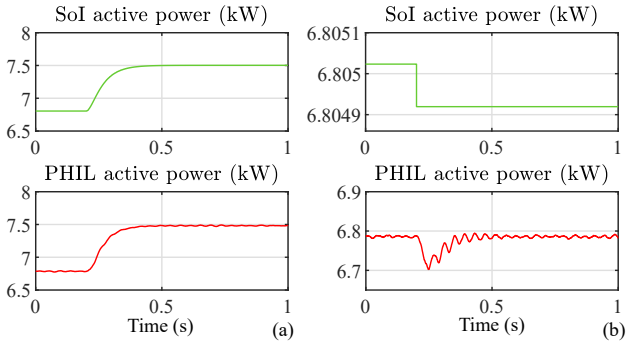


Fig. 12: Grid side active power of VSI-aided PHIL setup that is subject to (a) voltage step change, and (b) frequency step change.

Furthermore, to demonstrate the capability of the proposed VSI method in withstanding power system transients, an amplitude step variation from 0.4 kV to 0.42 kV and a frequency step change from 50 Hz to 50.5 Hz, are applied to the software side voltage source $V_{\text{S,LL}}$. Once the voltage step change is implemented at t = 0.2 s, as can be observed from Fig. 12(a), the proposed VSI-aided PHIL setup maintains stable operation during the transient, while the active power PTE is 0.31% once the PHIL system reaches a stable state. Note that, as presented in Fig. 12(b), after the frequency step change is triggered at t = 0.2 s, the PHIL active power takes a longer duration to reach a steady state than the SoI. This is attributed to the frequency variation response of the signal processing and synchronization units (i.e., abc to dq, dq to abc, and phase-locked-loop) that are utilized for the realisation of the proposed VSI presented in (5) and (6). After the transient oscillations, the active power converges to a stable state with an active power PTE 0.33%. Finally, as proven in the previous sections, even with a higher shifted IR, this accuracy should remain at the same levels, thus allowing the selection of the appropriate ratio based on the discussion provided in Section V-C.

VII. Conclusions

This paper presented the concept of virtual shifting impedance to realise stable power hardware-in-the-loop (PHIL) setups. Utilizing the advanced control capability of modern PAs, the software impedance is virtually shifted to the hardware through manipulating the reference voltage signal sent through the DRTS. Through the derivation of the transfer function-based model, the criteria for the minimum shift in impedance to realise stable PHIL setups have been attained. The approach offers a significant advantage over the existing state-of-the-art approach commonly adopted in practice, i.e., the FBF method. The performance enhancement in comparison to the FBF method has been demonstrated through analytical assessment and simulations. The real-world applicability of the approach has been proven through an experimental study, with the VSI incorporated within a commercial power amplifier.

References

[1] M. D. Omar Faruque *et al.*, "Real-time simulation technologies for power systems design, testing, and analysis," *IEEE Power and Energy Technology Systems Journal*, vol. 2, no. 2, pp. 63–73, 2015.

[2] G. F. Lauss, M. O. Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and design of power hardware-in-the-loop simulations for electrical power systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406–417, 2015.

[3] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1286–1294, 2008.

[4] C. Edrington, M. Steurer, J. Langston, T. El-mezyani, and K. Schoder, "Role of power hardware in the loop in modeling and simulation for experimentation in power and energy systems," *Proceedings of the IEEE*, vol. 103, pp. 1–9, 10 2015.

[5] Z. Feng, A. Alassi, M. Syed, R. Peña-Alzola, K. Ahmed, and G. Burt, "Current-type power hardware-in-the-loop interface for black-start testing of grid-forming converter," in *IECON 2022 – 48th Annu. Conf. of the IEEE Ind. Electron. Society*, 2022, pp. 1–7.

[6] K. Upamanyu and G. Narayanan, "Improved accuracy, modeling, and stability analysis of power-hardware-in-loop simulation with open-loop inverter as power amplifier," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 369–378, 2020.

[7] B. Lundstrom and M. V. Salapaka, "Optimal power hardware-in-the-loop interfacing: Applying modern control for design and verification of high-accuracy interfaces," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10 388–10 399, 2021.

[8] Z. Feng *et al.*, "Interface compensation for more accurate power transfer and signal synchronization within power hardware-in-the-loop simulation," in *IECON 2021 – 47th Annual Conference of the IEEE Ind. Electron. Society*, 2021, pp. 1–8.

[9] M. Pokharel and C. N. M. Ho, "Stability analysis of power hardware-in-the-loop architecture with solar inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 4309–4319, 2021.

[10] R. Brandl, "Operational range of several interface algorithms for different power hardware-in-the-loop setups," *Energies*, vol. 10, no. 12, 2017.

[11] I. D. Yoo and A. M. Gole, "Compensating for interface equipment limitations to improve simulation accuracy of real-time power hardware in loop simulation," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1284–1291, 2012.

[12] O. Tremblay, "Contribution to the design of the closed-loop control of a real-time power simulator," Ph.D. dissertation, Ecole De Technologie Superiere, Universite Du Quebec, 12 2020.

[13] O. Nzimako and R. Wierckx, "Stability and accuracy evaluation of a power hardware in the loop (phil) interface with a photovoltaic micro-inverter," in *IECON 2015 - 41st Annual Conference of the IEEE Ind. Electron. Society*, 2015, pp. 005 285–005 291.

[14] P. C. Kotsampopoulos, F. Lehfuss, G. F. Lauss, B. Bletterie, and N. D. Hatziargyriou, "The limitations of digital simulation and the advantages of phil testing in studying distributed generation provision of ancillary services," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5502–5515, 2015.

[15] Z. Feng, R. Peña-Alzola, M. H. Syed, P. J. Norman, and G. M. Burt, "Adaptive smith predictor for enhanced stability of power hardware-in-the-loop setups," *IEEE Trans. Ind. Electron.*, pp. 1–10, 2022.

[16] M. Dargahi, A. Ghosh, and G. Ledwich, "Stability synthesis of power hardware-in-the-loop (phil) simulation," in *2014 IEEE PES General Meeting — Conference Exposition*, 2014, pp. 1–5.

[17] G. Lauss, F. Lehfuß, A. Viehweider, and T. Strasser, "Power hardware in the loop simulation with feedback current filtering for electric systems," in *IECON 2011 - 37th Annual Conference of the IEEE Ind. Electron. Society*, 2011, pp. 3725–3730.

[18] Z. Feng *et al.*, "A scheme to improve the stability and accuracy of power hardware-in-the-loop simulation," in *IECON 2020 The 46th Annu. Conf. of the IEEE Ind. Electron. Society*, 2020, pp. 5027–5032.

[19] A. J. Roscoe, A. Mackay, G. M. Burt, and J. R. McDonald, "Architecture of a network-in-the-loop environment for characterizing ac power-system behavior," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1245–1253, 2010.

[20] Z. Zhang *et al.*, "Power hardware-in-the-loop test for cyber physical renewable energy infeed: Retroactive effects and an optimized power hardware-in-the-loop interface algorithm," in *2016 17th International Scientific Conference on Electric Power Engineering*, 2016, pp. 1–6.

[21] X. Zha, C. Yin, J. Sun, M. Huang, and Q. Li, "Improving the stability and accuracy of power hardware-in-the-loop simulation using virtual impedance method," *Energies*, vol. 9, no. 11, 2016.

[22] B.-I. Crăciun *et al.*, "Grid integration of pv power based on phil testing using different interface algorithms," in *IECON 2013 - 39th Annual Conference of the IEEE Ind. Electron. Society*, 2013, pp. 5380–5385.

[23] C. Yin *et al.*, "Virtual impedance method of the power hardware-in-the-loop simulation to improve its stability and accuracy," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 2752–2758.

[24] C. Yin, B. Ye, X. Wang, and L. Dai, "Power hardware-in-the-loop simulation of a distributed generation system connected to a weak grid," in *2017 IEEE Conference on Energy Internet and Energy System Integration (EI2)*, 2017, pp. 1–6.

[25] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 7th ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2014.

[26] Y. Wu, T. B. Soeiro, A. Shekhar, J. Xu, and P. Bauer, "Virtual resistor active damping with selective harmonics control of lcl-filtered vscs," in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, pp. 207–214.

[27] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019–7037, 2015.

[28] J. He and Y. W. Li, "Analysis, design, and implementation of virtual impedance for power electronics interfaced distributed generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2525–2538, 2011.

[29] J. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected ups inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, 2005.

[30] G. Lauss, Z. Feng, M. H. Syed, A. Kontou, A. D. Paola, A. Paspatis, and P. Kotsampopoulos, "A framework for sensitivity analysis of real-time power hardware-in-the-loop (phil) systems," *IEEE Access*, vol. 10, pp. 101 305–101 318, 2022.

[31] P. Vanassche, "Triphase hpc explained white paper, shaping dynamic response using virtual circuit control," Triphase, N.V., Tech. Rep., 2014.

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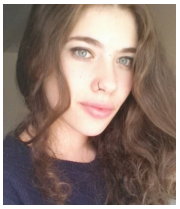

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