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High Efficiency Power Management Unit for Implantable Optical-Electrical Stimulators

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ABSTRACT Battery-less active implantable devices are of interest because they offer longer life span and eliminate costly battery replacement surgical interventions. This is possible as a result of advances in inductive power transfer and development of power management circuits to maximize the overall power transfer and provide various voltage levels for multi-functional implantable devices. Rehabilitation therapy using optical stimulation of genetically modified peripheral neurons requires high current loads. Standard rectification topologies are inefficient and have associated voltage drops unsuited for miniaturized implants. This paper presents an integrated power management unit (PMU) for an optical-electrical stimulator to be used in the treatment of motor neurone disease. It includes a power-efficient regulating rectifier with a novel body biased high-speed comparator providing 3.3 V for the operation of the stimulator, a 3-stage latch-up charge pump with 12 V output for the input stage of the optical-electrical stimulator, and 1.8 V for digital control logic. The chip was fabricated in a 0.18 μm CMOS process. Measured results show that for a regulated output of 3.3 V delivering 30.3 mW power, the peak power conversion efficiency is 84.2% at 6.78 MHz inductive link tunable frequency reducing to 70.3% at 13.56 MHz. The charge pump with on chip capacitors has 90.9% measured voltage conversion efficiency.

INDEX TERMS Charge pump, comparator, inductive power transfer, integrated circuits, power management, regulating rectifier.

I. INTRODUCTION

STEM cell-derived motor neurons in combination with hybrid optical-electrical stimulation might potentially help to regenerate damaged motor nerves. Engrafting stem cell motor neurons close to the targeted muscle would allow for patient rehabilitation before paralysis becomes irreversible in the case of motor neurone disease (MND) patients. Optical stimulation could help control muscle contraction after muscles are innervated with light-sensitive ion channel channelrhodopsin-2 (ChR2) [1], [2]. To personalize the stimulation process in optogenetic implantable devices, electrophysiological recording sensors such as electromyography (EMG) are added to sense muscle movements.

Multi-functional active implantable medical devices are essential for extensive *in-vivo* studies with rodents to ensure successful clinical translation of the optogenetics approach. Miniaturised implanted devices can reduce the incidence of tissue inflammation, astroglial scarring and cell death [3], [4]. The use of wireless power transfer is preferred for battery-less operation. To optimize power transfer in multi-functional implantable devices, a power management unit (PMU) must generate different dc output voltage levels from one input ac voltage. Although efforts have focused on increasing the power carrier frequency to reduce the size of the coil and output capacitor while improving transient responses, this can increase switching losses and degrade efficiency [5]. Passive rectifiers typically suffer from poor power conversion efficiency (PCE) and voltage conversion efficiency (VCE) due to their high voltage drops. Combining both processes of rectification and regulation into a single stage can eliminate the decoupling capacitor between them, decrease the overall area, and increase the overall system

efficiency [6]–[9]. In addition, it avoids the need for multiple low-dropout regulators (LDOs) in multi-functional systems.

Current research focuses on the development of integrated optical-electrical stimulators that are fully implantable and miniaturized, consisting of an integrated PMU powered by wireless power transfer (WPT) [7], [8]. Active rectifiers for optogenetics have been used consisting of active diodes and comparators to improve PCE and VCE providing rectified currents from 100 μA to 5 mA [6], [7], [8], [9]. In hybrid optical/electrical stimulator implants the stimulation is pulsatile, often requiring larger current pulses for optical stimulation than the PMU can provide. A wide bandwidth regulation feedback loop is required to support the delivery of transient load currents with accurate high efficiency voltage regulation.

This paper presents an efficient PMU chip as part of an optogenetic ASIC providing optical LED stimulators and electrical stimulators generating flexible pulse patterns. It provides three output voltage levels for the stimulator unit, as shown in Figure 1. (*HV*: electrical stimulation, *LV*: control logic, *RV*: optical stimulator). The PMU dc voltage regulation accepts a wide range of ac levels from the inductive link. A high efficiency rectifier topology with pulse width modulation (PWM) regulation and a body-biased high-speed comparator are used to regulate the output and minimize leakage currents. The PMU can accept inductive link carrier frequencies from 6.78 MHz to 13.56 MHz. The PMU has an optimized area-efficient 20 MHz 3-stage charge pump (CP) required for electrical stimulators.

This work is an expansion of [10] and provides further details on the circuit design topology; it includes measured results from the fabricated chip of the PMU highlighted in Figure 1. Further circuit details on the stimulator unit and EMG sensor can be found in [11]. The rest of the paper is organized as follows. Section II describes the theory and a short review of power management circuits. Section III presents the system architecture and elaborates on the design choices for the various building blocks including the regulating rectifier and latch CP. Section IV shows measured results and analysis including testing with an optical-electrical stimulator. Concluding remarks are drawn in Section V.

II. POWER MANAGEMENT CIRCUITS

In a conventional PMU design shown in Figure 2, a CMOS active rectifier followed by voltage regulation circuitry has been commonly used to power implantable devices. The total efficiency of a conventional WPT system can be represented as

$$\eta_{Total} = \eta_{coil} \cdot \eta_{Rec} \cdot \eta_{Reg} \tag{1}$$

where η_{coil} is the link efficiency between the two coils, η_{Rec} the rectifier efficiency, and η_{Reg} the regulators' efficiency. The coil efficiency is limited due to the physical constraints of the implanted coil. The received power depends on the coupling coefficient k between the primary (external) and

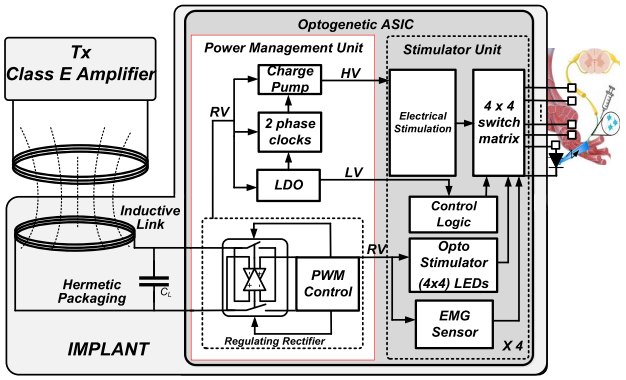


FIGURE 1. The overall WPT system with the proposed PMU topology highlighted within the optical-electrical stimulator ASIC.

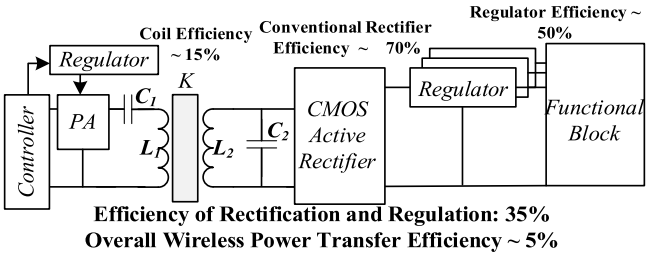


FIGURE 2. Architecture and power distribution of a conventional wireless implantable power management unit.

the secondary (internal) coil; k varies significantly with the distance between and orientation of the two coils. As shown in Figure 2, the coil coupling misalignment significantly degrades the overall system efficiency [12].

Maximizing power and voltage efficiency in a conventional design is limited due to the use of LDOs which lower the overall power efficiency in current hungry circuits. In Figure 2, in the conventional inductive link only 15% of the input power is available for the following stages. Even with an ideal coil with 100% efficiency, after passing through the conventional rectifier and regulator, the overall power efficiency is limited to about 35%.

PN junction diodes shown in Figure 3(a) have large forward voltage drops (about 0.7 V) and power dissipation. Schottky diodes have lower forward voltage drop (about 0.5 V) but higher leakage currents and are not widely available in CMOS fabrication processes [13]. Active rectifiers operating in deep triode region shown in Figure 3(b)-(d) have improved power efficiency and reduced conduction losses of transistors with a much lower leakage current than a junction diode-based passive rectifier [14]. The voltage-drop V_{GS} (about 0.6 V) in a diode-connected MOS transistor with drain current I_D is

$$|V_{GS}| = |V_{DS}| = |V_{TH}| + \frac{2I_D}{\mu C_{ox}\left(\frac{w}{L}\right)V_{TH}} \tag{2}$$

where $I_D \ll (V_{TH}\mu_o C_{ox}\frac{W}{L})$ (in deep triode region) and the symbols have their usual meaning. The threshold voltage, V_{TH}, is a process-dependent parameter which can be minimised by eliminating the body effect. It can be reduced

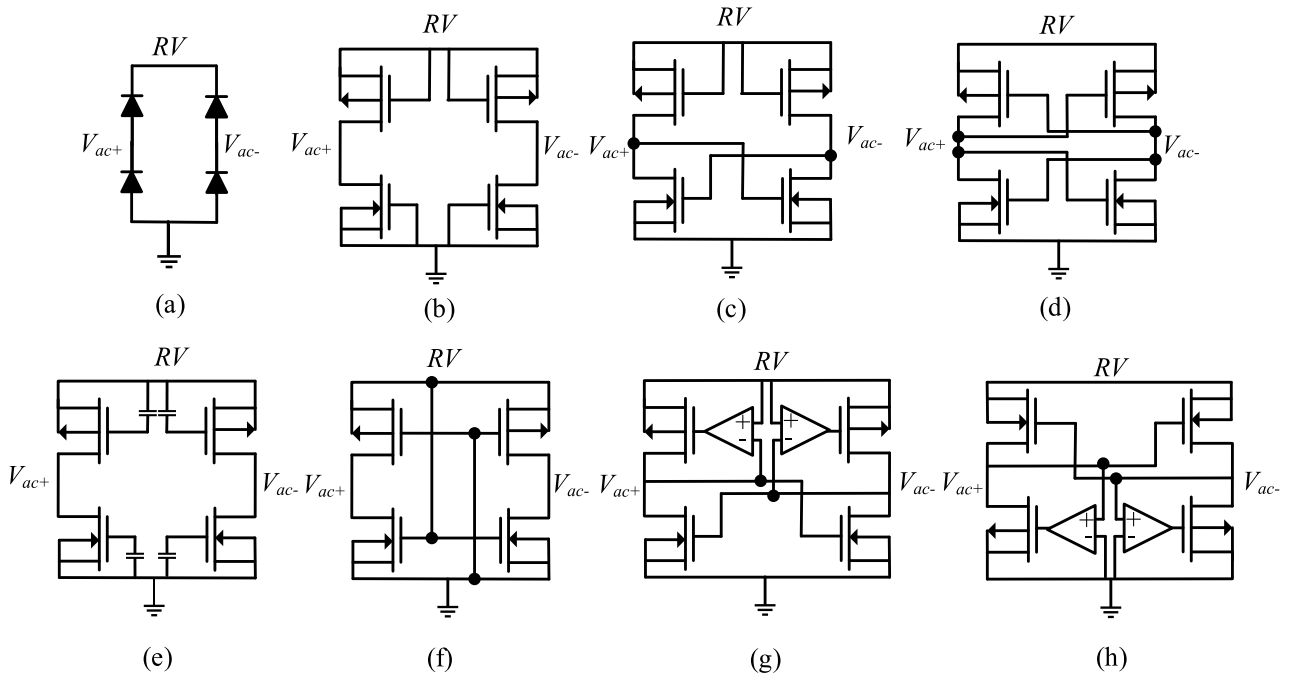


FIGURE 3. Conventional ac-dc rectifier topologies: (a) junction diode-based passive rectifier (b) diode-connected MOS passive rectifier (c) gate-cross coupled passive rectifier, (d) differential fully gate-cross coupled passive rectifier, (e) external V_{TH} cancellation (EVC), (f) internal V_{TH} cancellation (IVC), (g) active rectifier with comparators added to cross-coupled pMOS switches, and (h) active rectifier with comparators added a cross-coupled nMOS switches.

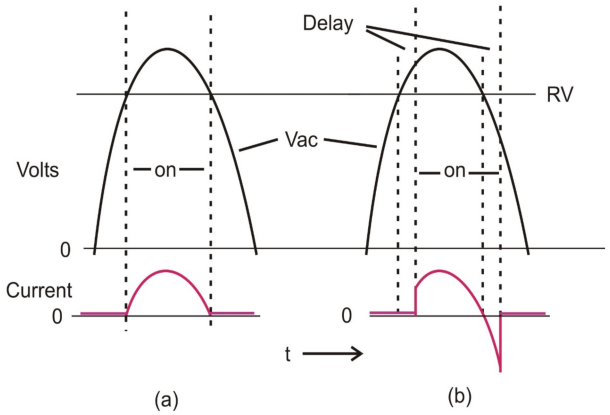


FIGURE 4. Illustrating reduction of positive charging current and reverse current due to comparator delays. (a) No delays (b) 'On' and 'off' delays.

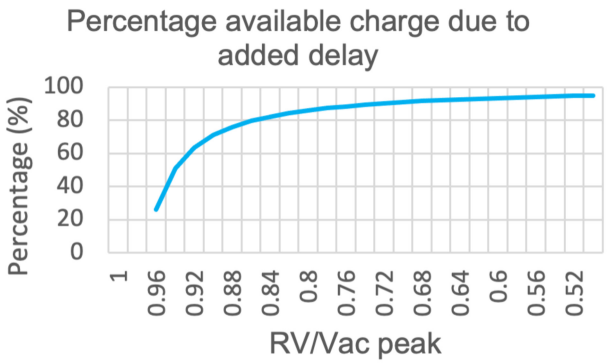


FIGURE 5. Percentage of available maximum charge width when delay is added. Delay 1/30th of V_{ac} period.

using techniques such as external V_{TH} cancellation (EVC) (about 0.53 V) shown in Figure 3(e), or internal V_{TH} cancellation (IVC) (about 0.4 V) shown in Figure 3(f) [15]. These architectures add circuitry to reduce the effective threshold voltage and improve the overall conversion efficiency. Floating gates were suggested [16] to reduce the effective threshold voltage in CMOS rectifiers and improve the overall PCE but require the threshold to be reprogrammed and adjusted.

In general, slow transients and long delays are limitations to PCE. In [17], two auxiliary pMOS transistors, also known as dynamic body biasing, are added to each of the rectifying pMOS transistors to connect the n-well to the drain or the source (whichever is at a higher potential). The added comparators shown in Figure 3 (g), (h) [18], [19] provide fast transients and switching delays limited by the comparator performance. They have low-voltage and auto-switching gate characteristics due to the use of comparators, but still suffer from power losses due to the switch 'on' resistance of the active rectifiers and reverse conduction.

As shown in Figure 4(a) the 'on' and 'off' switching delays lead to reduced positive charge and some negative charge at the rectified output which can be significant in high-speed applications. Figure 4(b) shows the output with no delays. Figure 5 shows the charge reduction as output voltage RV approaches the peak voltage of the secondary coil received voltage V_{ac} when the comparator delay is about 1/30 of the period of V_{ac}.

To increase power efficiency in active rectifiers, the turn on voltage of the switching transistors should be small and have

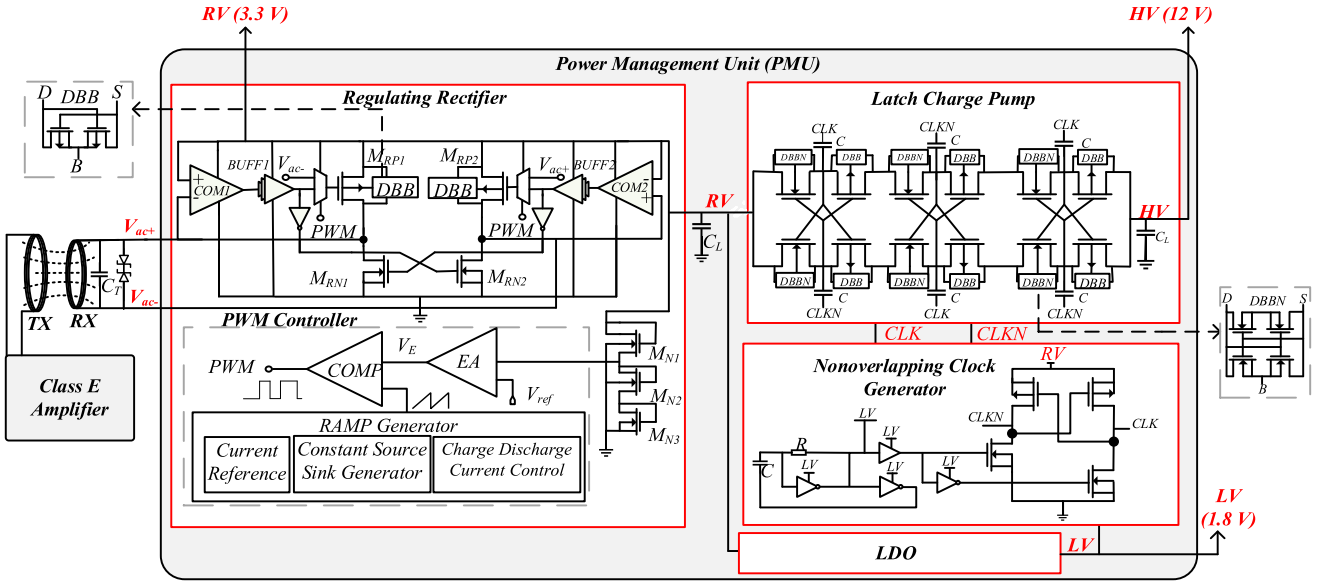


FIGURE 6. System architecture of the single stage regulating rectifier, body biased latch CP, and two-phase nonoverlapping clock.

a low 'on' and 'off' threshold. However, there is a limitation in the efficiency as the input amplitude increases causing an increase in reverse current. Control circuits are used in the proposed design to address the following issues: 1) The mismatch between the on-off time of the active switch and the crossover time of the input and output voltages can cause a reverse leakage current loss. 2) The synchronous circuit will not operate at the exact on-off time of the switches when the input and output cross one another [20]. 3) High reverse current caused by slow switching can lead to a reduction in charge and PCE [21]. To address the reverse current issue, in the industrial, scientific and medical (ISM) band range (6.78 – 13.56 MHz) comparator based active rectifiers are used to improve VCE and PCE [22]. In the active rectifier design, the turn on and turn off times are limited by the speed of the comparators. Power regulation operates by tracking the envelope of the RF input and when it drops it pulls the output voltage back up. The comparators control the gates' turn on and turn off times. The comparators will experience delays at higher operational frequencies due to the parasitic resistance and capacitance, and the system offsets and mismatches. The feedback control scheme added to the rectifier increases the circuit complexity and requires very fast comparators to drive their switches at the conduction time.

The power consumption of the state-of-the-art high-speed comparators is large which limits the PCE of the rectifier. The number of comparators must be minimized to improve the overall system's PCE. The proposed regulating rectifier topology uses two comparators with inverters to switch both nMOS and pMOS rectifiers as shown in Figure 6. Improving the speed of the comparators and addressing the limitations of the conventional comparator design, can be realised with PWM control topologies to ensure the comparators perform at their optimum point and regulate the output voltage. Topology configurations to enhance the performance of conventional comparators are proposed in this paper.

III. SYSTEM ARCHITECTURE

The proposed system shown in Figure 6 is designed to generate three independently regulated supply voltages (*LV*: 1.8 V, *RV*: 3.3 V and *HV*: 12 V) from an input ac voltage within the ISM frequency band 6.78-13.56 MHz received from the inductive link. As shown in Figure 1, the system has four hybrid optical-electrical stimulator units, control logic, and EMG sensor [23] in a single chip for a fully implantable solution. The proposed regulating rectifier features single-stage rectification and regulation with PWM control, an LDO with internal bandgap reference, and a high voltage latch CP with a two-phase non-overlapping clock generator [24]. The LDO is powered by 3.3 V and provides a stable 1.8 V output for the block control logic [25].

The light intensity demand for the targeted optical stimulation of around 1-10 mW/mm^2 [2] requires at least 10 mA for the LEDs. The design avoids reduction of efficiency in the regulation stage by combining regulation and rectification into a single stage.

The PWM feedback control loop has changeable links between the input voltages, V_{ac+} and V_{ac-}, from the inductive link and the comparator inputs to ensure regulation for both high and low values of V_{ac} and maintenance of high output current. The regulating rectifier operates over a wide input power range of 40-60 mW to deliver up to 30-40 mW with up to 10.5 mA current delivery to provide efficient power accounting for the alignment mismatch of the inductive link coils. As shown in Figure 6, Zener diodes in series are added across *RX* coil to limit the ac voltage to below the breakdown voltage of the CMOS technology transistors. At the transmitter side, voltage $V_{tx}(t)$ and current $I_{tx}(t)$ in the *TX* coil is:

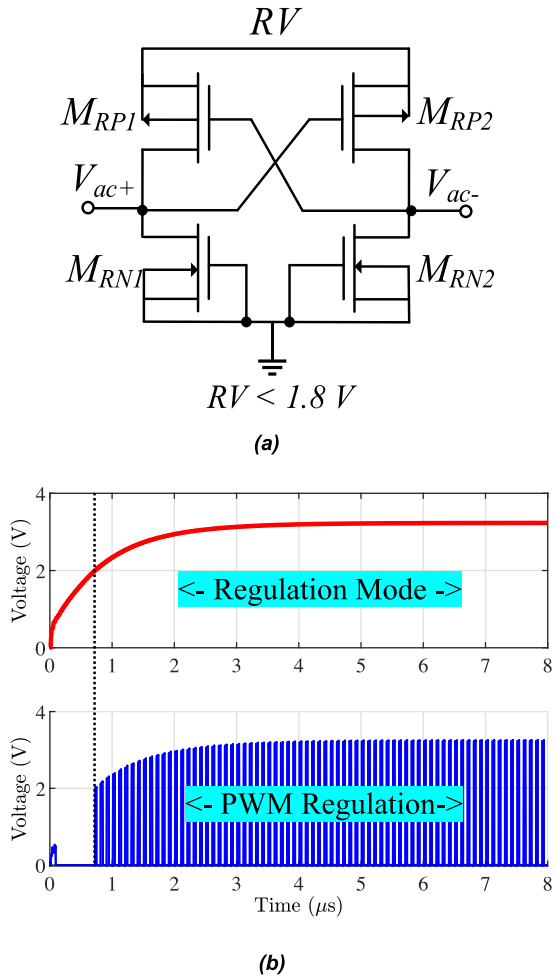


FIGURE 7. (a) Startup mode configuration (PWM = 0 V) (b) Simulation of startup performance of the regulated output and the PWM signal turn 'on' under mismatch.

$$V_{tx}(t) = V_{tx} \sin \omega t \tag{3}$$

$$I_{tx}(t) = \frac{V_{tx}(t)}{Z_1} \tag{4}$$

where $V_{tx}(t)$ is the applied voltage and Z_1 the impedance reflected from the secondary side. At the receiver side, the current in the RX coil $I_{rx}(t)$ is

$$I_{rx}(t) \approx \frac{M}{L_2} \cdot I_{tx}(t) \tag{5}$$

$$M = K\sqrt{L_1 L_2} \text{ and } k = \frac{r_1^2 r_2^2}{\sqrt{r_1 r_2}} \cdot \frac{1}{\left(\sqrt{X^2 + r_1^2}\right)^3} \tag{6}$$

where M is the mutual inductance, k is the coupling coefficient, r_1 is the transmitter coil radius with L_1 inductance, and r_2 is the radius of the receiver coil with L_2 inductance. X is the distance between the coils [25]. The voltage across RX, $V_{rx}(t)$ due to $I_{rx}(t)$ is

$$V_{rx}(t) \approx I_{rx}(t) \cdot Z_2 \tag{7}$$

$$\approx \frac{\sqrt{r_1 r_2}}{\left(\sqrt{x^2 + r_1^2}\right)^3} \cdot \frac{\sqrt{L_1 L_2}}{L_2} \cdot V_{tx} \sin \omega t \cdot \frac{Z_2}{Z_1} \tag{8}$$

where Z_2 is the sum of the reflected impedance from the primary side to the secondary impedance. The total input ac power, $P_{rx}(t)$, is measured by taking the average product of $V_{rx}(t)$ and $I_{rx}(t)$ over several cycles.

A. START UP PERFORMANCE

Figure 7(a) shows the regulating rectifier configuration during startup as full wave passive diodes when V_{ac} and the voltages V_{gs} and V_{sg} on the parasitic capacitances of the switch transistors M_{RP1} and M_{RN2} are zero before proceeding to the active rectification mode. As input V_{ac+} increases, V_{sg} of the transistor increases to above its threshold voltage. In the negative cycle, transistors M_{RP2} and M_{RN1} act as passive diodes to charge up the output RV. Only when the output RV is at a sufficient voltage will the PWM controller turn on for active rectification. Otherwise, the PWM output is off until it increases to around 1.89 V; subsequently the rectifier works in the normal mode as shown in Figure 7(b).

B. REGULATING RECTIFIER CONTROL

The regulating rectifier's four different configurations in the V_{ac} period are shown in Figure 8. The terminals are connected to the input voltages V_{ac+} and V_{ac-} of the floating RX coil. The nMOS and pMOS transistors $M_{RN1,2}$ and $M_{RP1,2}$ in the regulated rectifier are driven by self-dynamically powered comparators that do not need a fixed voltage supply making it a power-efficient and low-noise topology. To convert V_{ac} to a regulated RV input, the design employs four transistors ($M_{RN1,2}$, $M_{RP1,2}$), two comparators ($COM1$, $COM2$) and two buffers ($BUFF1$, $BUFF2$) whose circuit details are shown in Figure 9. The high-speed comparators and inverters are used to drive the gates of $M_{RN1,2}$ and $M_{RP1,2}$ to control the operation in such a way that the forward current is maximized, and the reverse leakage current is minimized. When the output voltage RV increases above 3.3 V the pMOS gates are connected to the input voltages, V_{ac+} and V_{ac-} [Figure 8(c), (d)]. When RV decreases below 3.3 V it is connected to the comparators controlled by the PWM feedback loop [Figure 8 (a), (b)]. In Figure 8(a), when V_{ac+} is high then MR_{P1} and MR_{N2} are on. In Figure 8(b), when V_{ac-} is high MR_{P2} and MR_{N1} are on. There are only two comparators shared between nMOS and pMOS transistors.

Dynamic body biasing (DBB) connecting the body of the pMOS/nMOS transistors to the highest/lowest voltage level is used to optimize PCE, allowing a tradeoff between the conduction and switching losses. The regulating rectifier has two operating modes: mode 0 and mode 1. At $RV < 3.3$ V (mode 1), the switching losses are small and PCE is high when connected to the comparator as the conduction time of the comparator is maintained. When RV

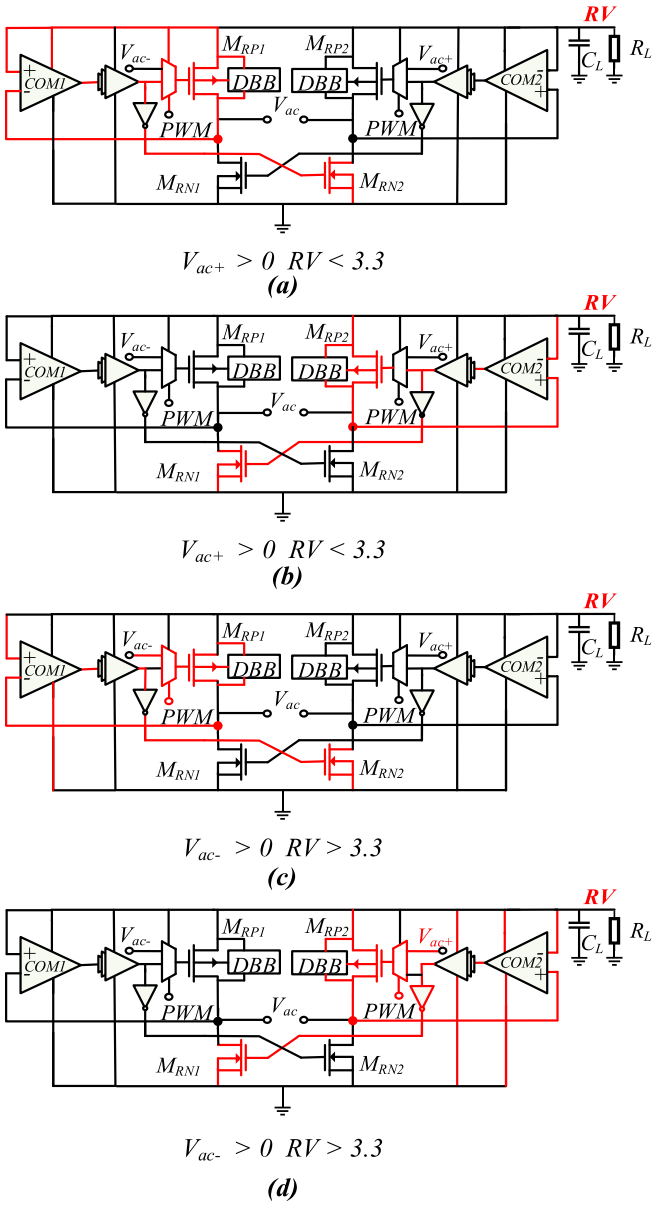


FIGURE 8. Reconfigurable regulating rectifier topologies for different output and input voltages.

> 3.3 V (mode 0), instead of conducting at every cycle, and reducing the overall efficiency due to slow switching of the comparators, the rectifier gates are connected to the inputs to maintain the overall PCE/VCE as the cross-coupled configuration efficiency increases at higher inputs. PWM controls the conduction time of switches M_{RP1} and M_{RP2} during every cycle of the input signal to regulate the output *RV*.

The architecture of the high-speed comparators (*COM*1 and *COM*2) is shown in Figure 9. The off-delay compensation in the unbalanced-biased mechanism with DBB for push-pull comparator eliminates the reverse leakage providing a constant artificial offset. By reducing the subthreshold leakage and increasing the activating voltage the high-speed

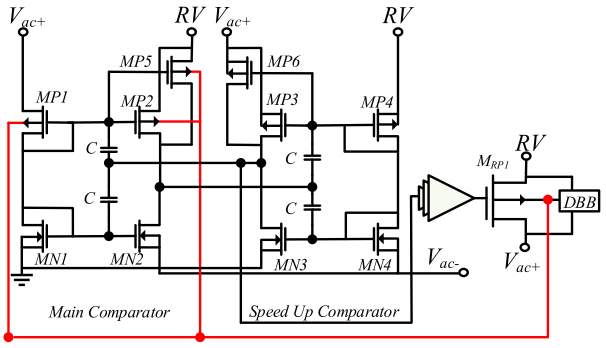


FIGURE 9. Body biased high speed comparator.

comparators have a decreased response time and slightly higher dc voltage output in the regulated rectifier. The design also includes DBB in the comparator to avoid latch-up of the device and prevent breakdown. The system has no multi-pulsing problem that can reduce the efficiency and has a higher input range and power delivery due to the use of asymmetrical differential input transistors similar to [26] with additional DBB. The self-biased comparator starts up at the input V_{ac+} around 0.9-1 V_{pp}, which results in an increase in the output voltage, VCE and PCE. The regulation only starts when the voltage is reached. After the start-up of the comparator, *RV* increases linearly following the input voltage until it reaches the threshold voltage.

In an active rectifier, during operation when the output dc voltage *RV* is higher than the input voltage in the transition, V_{ac+} and V_{ac-}, a slow switching speed from one cycle to the next cycle can result in reverse leakage current flowing out from the output load, which reduces efficiency. Also, the comparator will be high in the same cycle causing an additional pulse, especially with light load conditions when switching losses dominate. This is mainly due to the transition being limited by the speed of the comparator; careful design of the comparator is crucial for maximizing the efficiency. To retain the efficiency and prevent the output from being higher than the input, an additional PWM feedback loop prevents the increase in the voltage output and limits the reverse leakage current flowing out of the output load and helps regulation. Lowering the threshold voltages of the switching transistors in the comparators mitigates the body effect and optimizes the efficiency by having a faster response. Another advantage is that it can combine both ac-dc and dc-dc into one and eliminate the need for calibration comparators in the active rectifier, keeping the design simple without the need for additional digital control. The forward current will be delivered continuously to the load and capacitor to produce a rectified voltage as in a conventional design [27] but with faster current response as shown in the transient simulation in Figure 10. The voltage output will be slightly higher due to the additional feedback loop limiting the increase of the output voltage in order to limit the degradation in speed which increases leakage current and decreases efficiency.

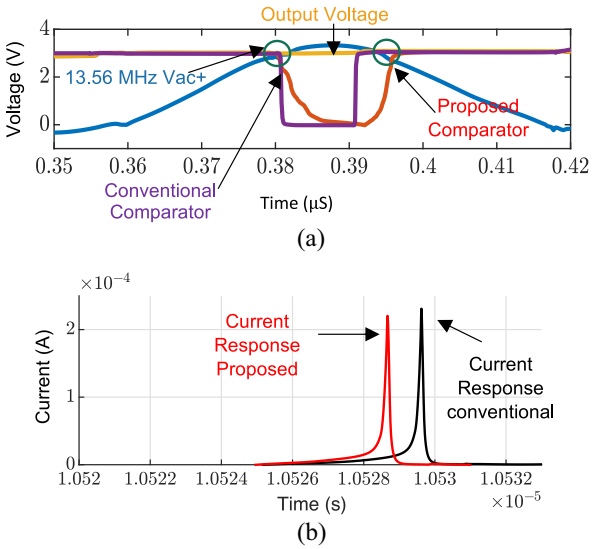


FIGURE 10. Comparison of transient simulation plot of the proposed regulating rectifier with dynamic body biased to a conventional comparator. (a) Voltage response (b) Current response.

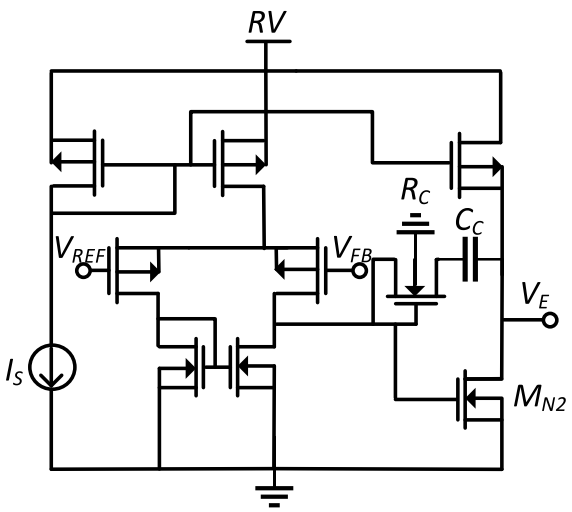


FIGURE 11. OTA circuit in the error amplifier (EA).

C. ANALYSIS OF REGULATION WITH LOCAL PWM CONTROL

The analog PWM controller is shown in Figure 6. It consists of an error amplifier (EA) as shown in Figure 11 which senses the error between a reference voltage V_{ref}, and $RV{\cdot}(R_2+R_3)/(R_1+R_2+R_3)$, and a *RAMP* signal to generate a pulse width modulated output via a comparator (COMP). R_1, R_2, R_3 are pseudo nMOS resistors (M_{N1}, M_{N2} and M_{N3} shown in Figure 6). They are used to control the feedback gain and stability. The duty cycle of the generated pulse output *COMP* is altered based on the output of the error amplifier, V_E, providing a controlled conduction window.

Adding the PWM control reduces switching and conduction losses and increases PCE. The pulse is used to switch on the active rectifier depending on whether the input voltage V_{ac} is higher or lower than the bias voltage, as shown in

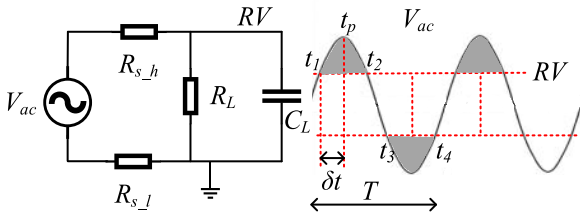


FIGURE 12. Simplified input signal analysis for PWM control.

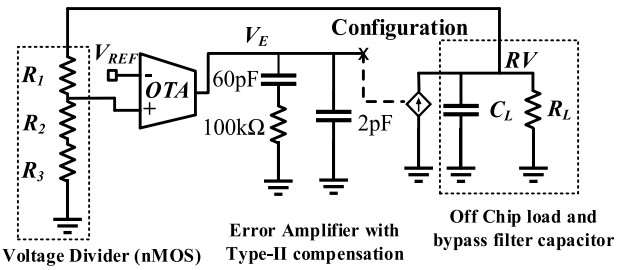


FIGURE 13. Simplified small-signal model of the PWM controller block for stability analysis.

Figure 12. It is achieved using the feedback loop to control the conduction window. In Figure 12, the rectifier conduction time starts from t_1 and t_3 for a period δt during the positive and negative cycles, respectively. The total charge supplied by the input voltage V_{ac} in both the negative and positive conduction cycles is given by

$$\begin{aligned} Q_{in} &= 2\int_{t_1}^{t_p} \frac{V_{ac}\sin(\omega_0 t) - RV}{R_S}dt \\ &= \frac{2V_{ac}}{\omega_0 R_S}\left[\cos(\omega_0 t_1) - cos(\omega_0 t_p)\right] \\ &\quad - \frac{2(RV)\delta t}{R_S} \end{aligned} \tag{9}$$

where $t_p = t_1 + \delta t$. The switch resistance R_s is the sum of the resistor at the high switch, R_{s_h} and the resistor at the low switch, R_{s_l} active transistors. Equation (9) is based on the principle of conservation of charge, where the charge from the input Q_{in} in time-period T is independent of the output load R_L. The output voltage RV is

$$RV = \frac{\frac{2}{\omega_0}\left[\sqrt{V_{ac}^2 - (RV)^2}(1-\cos\delta t) + (RV)\sin\delta t\right]}{\left(\frac{R_s}{R_L}T + 2\delta t\right)}. \tag{10}$$

where C_L, R_L are the load capacitance and resistance respectively, and V_{ac} is the ac input voltage. RV is a function of the conduction time δt. By modulating δt the regulating rectifier can regulate RV independent of the load R_L. The power conversion efficiency of the PWM, η_{PWM}, is

$$\eta_{PWM} = \frac{P_{out}}{P_{in}} = \frac{(RV)^2/R_L}{P_{cond} + P_{switch} + P_{static} + P_{out}}. \tag{11}$$

where P_{cond}, P_{switch}, P_{static}, and P_{out} are the conduction, switch, static and output powers respectively. P_{switch} are a function of P_{cond} associated with the switching in each cycle. Operation at a lower frequency provides higher PCE. P_{static}

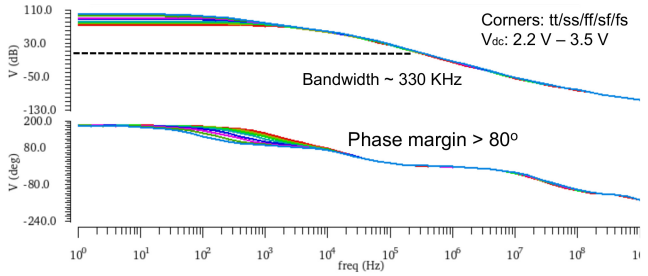


FIGURE 14. Loop gain at various ranges of voltage feedback, VFB, with gain margin of 81.8 dB at various PVT corners.

of the PWM controller is calculated when the system is inactive. The PWM topology is utilized for the application's high current requirement and designed for $R_L = 100\ \Omega$ to 2 kΩ.

The PWM control is represented by the small-signal model in Figure 13. The EA has a Miller capacitor in series with compensation resistor R_C. It has an additional Type II compensation + equivalent series resistance (ESR) zero that can provide higher than 80^o phase margin to ensure stability. The EA with one dominant pole minimizes complexity and provides a large dc gain of 87 dB with bandwidth of 300 kHz for a supply range of 2.2 V to 3.5 V. The Type II compensation ensures the feedback loop stability for loads of 500 Ω to 2 kΩ. To evaluate the sensitivity, Monte Carlo simulations were performed for various resistive loads. As shown in Figure 14. to ensure optimum performance the loop stability is simulated under different PVT corner tests for nonideal effects of the sampling switch, so that the VCE and PCE are optimized.

D. CHARGE PUMP (CP)

The latch CP topology in Figure 6 significantly improves the efficient pumping operation and minimizes the voltage drop when charging. Conventional CPs use large ($\sim$1 μF) off-chip flying capacitors and operate at a low frequency of $\sim$100 kHz. The proposed CP operates at 20 MHz to eliminate the need for off-chip capacitors; an off-chip load $R_L$is used for testing. The value of the capacitors is limited to 60 pF to minimize their chip area. A three-stage CP is shown in Figure 6 with on-chip flying capacitors, which boosts the 3.3 V (RV) generated by the regulating rectifier to 12 V output for the stimulator. The body terminals of the switches are dynamically biased to ensure that the substrate and n-well are always connected to the correct voltages during operation.

IV. MEASURED RESULTS AND DISCUSSION

An integrated chip including the PMU was fabricated in a 0.18 μm HV CMOS technology. Figure 15 (a) shows the die microphotograph. The PMU occupies an area of 0.048 mm^2 including the regulating rectifier, CP, LDO, 2-phase nonoverlapping clock generator and 13 on-chip capacitors. A discrete power transmitter circuit was designed to deliver 60–100 mW power to the implant through a pair of coils over a linear distance of 1.5–3 cm.

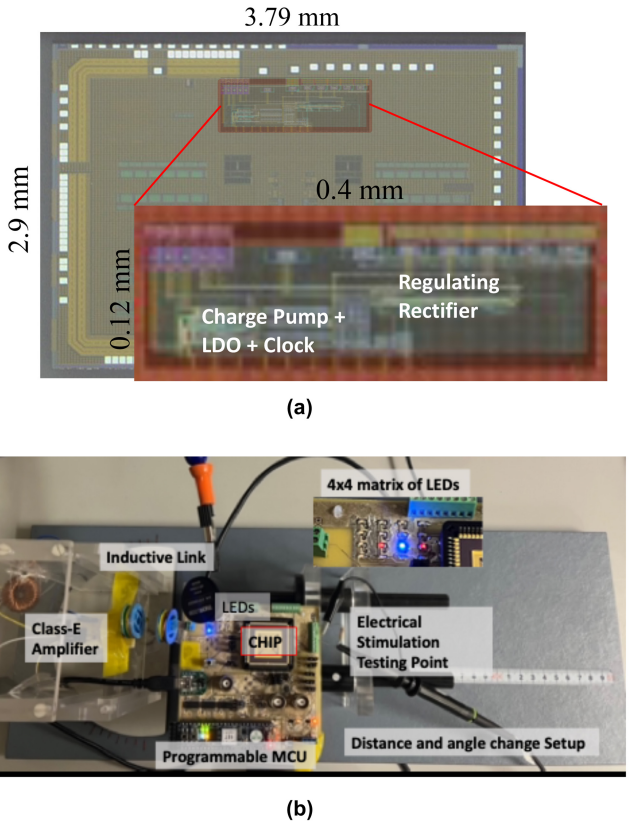


FIGURE 15. (a) Chip micrograph (b) The measurement setup; of the optical and electrical stimulation with focus on the PMU.

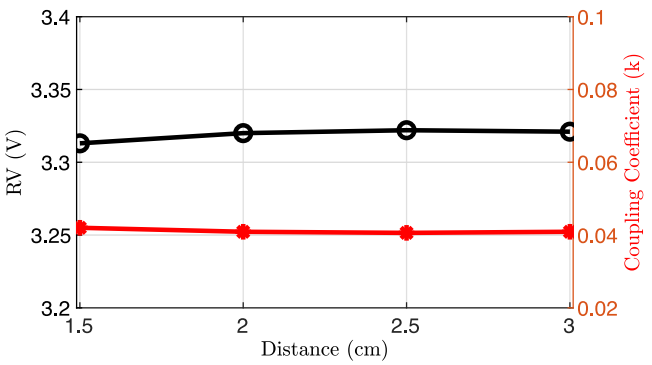


FIGURE 16. Measured output voltage RV and coupling coefficient k at various distances from 1.5 to 3 cm at 13.56 MHz.

Two class-E amplifiers for test frequencies of 6.78 MHz and 13.56 MHz were used. The test setup is shown in Figure 15 (b). The TX and RX coils have a diameter of 20 mm, and their inductances are 1.13μH and 890.1nH, respectively. The quality factors measured at 13.56 MHz are 483.59 and 1752.7, respectively. The measured output voltage and coupling coefficient k at 13.56 MHz with different x-axis distances is shown in Figure 16. The system was tested for various distances between coils, voltage levels and frequencies to establish the optimum performance. Figure 17 shows the output voltages of the regulating rectifier (RV) and the charge pump (HV) at light load for RX output $V_{ac} = 7.2\ V_{pp}$ at a load R_L of 1 kΩ. Similarly Figure 18 (a), (b)

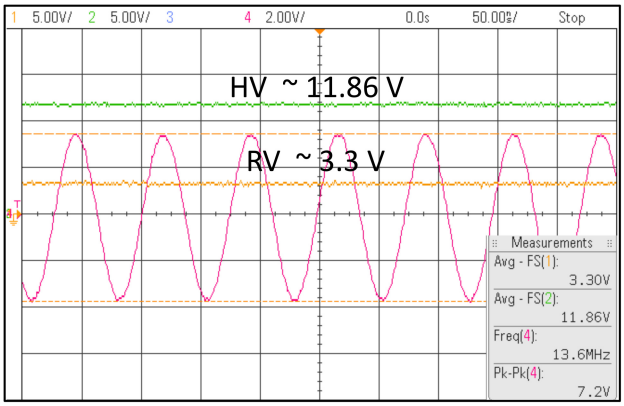
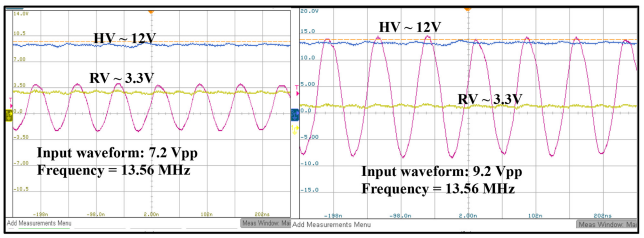


FIGURE 17. Measured outputs of the regulating rectifier and charge pump at 220 Ω load.



(a) (b)

FIGURE 18. Measured outputs of the charge pump and regulating rectifier: (a) input Vac = 7.2 Vpp, (b) input Vac = 9.2 Vpp.

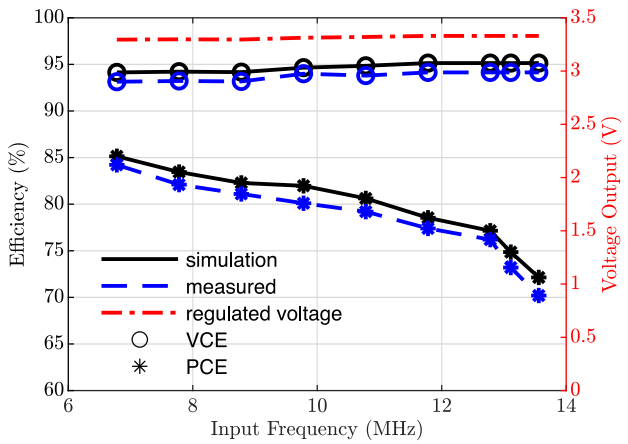


FIGURE 19. PCE, VCE and regulated voltage of the active rectifier over various frequencies at load resistance of 1 kΩ *and Vac = 7 V_{pp}*.

shows *HV* and *RV* for *RX* outputs V_{ac} = 7.2 and 9.2 V_{pp}. Under steady state, the output capacitor C_L and the resistor load R_L generate voltage ripples $V_{ripples}$:

$$V_{ripples} = I_L \cdot R_L + (RV) \cdot \left(1 - e^{\frac{-n \cdot T}{R_L \cdot C_L}}\right) \tag{12}$$

where I_L is the load current and $n{\cdot}T$ is the rate of discharging. $V_{ripples}$ can be reduced by increasing the output capacitor value or the operating frequency.

A. RECTIFIER REGULATION PERFORMANCE

For a variation of the input from 7.2–9.2 V_{pp} and a 2 kΩ load the regulated output RV was 3.3 V ±0.23%. The input

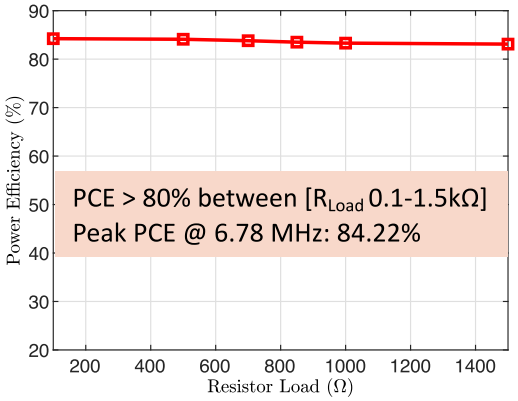


FIGURE 20. Measured PCE of the regulating rectifier at different resistive loads.

variation was limited to 2 V to protect the 3.6 V transistors in the regulating rectifier. The design can successfully generate; RV = 3.3 V ±0.23% using PWM regulation while delivering 30.3 mW power to satisfy the high current requirement of the optogenetic application.

Figure 19 shows the measured VCE and PCE for inductive power carrier frequencies from 6.78 MHz to 13.56 MHz at a load of 1 kΩ and V_{peak} of 3.5 V (V_{ac}= 7 V_{pp}). VCE increases by 0.03% at higher frequencies due to the fixed decoupling and parasitic capacitances. PCE decreases at higher frequencies in both the simulated and measured results due to the high frequency switching losses. The measured results are compared to a simulation environment which includes tuning a capacitance to provide a more realistic performance comparison.

The highest VCE is 95.1% and PCE = 70.3% at a frequency of 13.56 MHz. The highest measured PCE is 84.2% and VCE = 92.1% at 6.78 MHz at V_{ac} input of 7 V_{pp} The measured line load regulation is 0.59% at 6.78 MHz and 0.68% at 13.56 MHz inductive power carrier frequencies. The regulating rectifier can deliver up to 10.44 mA to the optical stimulators with an average optical power of 1.45 mW, 452 nm wavelength measured by a power energy meter. The design improves reliability and decreases the overall system area while supporting full load ranges with a fast transient response suitable for the optical-electrical stimulator.

The measured PCE at different loads are shown in Figure 20. The regulating rectifier has a PCE peak of 84.2% at an operating frequency of 6.78 MHz. The loads are tested at the lower frequency as these are the required ranges for the application of optical and implantable stimulations. The proposed system requires high current outputs.

B. CHARGE PUMP PERFORMANCE

Figure 21 shows the measured CP output voltage when the load demand was 420 μA with 20 MHz pumping frequency from the on-chip nonoverlapping clock (Figure 6). Figure 22 shows the measured charge pump output voltage and PCE at different loads. At a light load of 100 μA, the power efficiency reduces to 40% increasing to 65% at 220 μA

TABLE 1. Measured performance summary and specifications.

Reference	This Work	[28]	[29]	[6]	[7]	[30]	[31]
Process	180-nm CMOS	180-nm TSMC 1P/6M	180-nm CMOS	180-nm Standard	180-nm HV BCD	65-nm LPCMOS	180-nm SOI
Power Carrier Frequency (MHz)	6.78-13.56	1-10	40.68	2.7	1.314	1.85	144
$P_{out,Max}$ (mW)	30.3 (330 Ω @13.56 MHz) 76.22 (100 Ω @ 5.56 MHz)	65 (100 Ω)	56.5	2.454	N/A	0.146	0.7
V_{dc} (V)	Optical: 3.3 Electrical: 12	Electrical: 1.5-3.3	3.35	Optical: 2.84	Optical: 3 Electrical: 15	Electrical: 2.5	Electrical: 1
R_{load} (kΩ)	0.22-5	0.1	0.5	N/A	N/A	N/A	8
Max VCE (%)	95.1	75.8	73.2~84.1	93.57	92	N/A	N/A
Regulating Rectifier	Yes	Yes	Yes	No	No	No	Yes
Regulation Type	Regulating Rectifier	Regulating Rectifier	Active Rectifier (no regulation)	Double Pass Regulator	LDO	LDO	Regulating Rectifier
PCE (%)	84.2 @ 6.78 MHz (Rec+Reg)	83.8 (@ 5 MHz)	70.7~80.9	92.6 (only rectifier)	71.4 (only rectifier)	82 (only rectifier)	54
Area (mm^2)	0.048*	6	0.00158	0.09	3.58	1	0.0078
Proposed Application	Optical/ Electrical + Sensing and Recording	NA	Electrical	Optical	Optical/ Electrical	Electrical	Electrical and Recording

*Including charge pump, clock, and LDO.

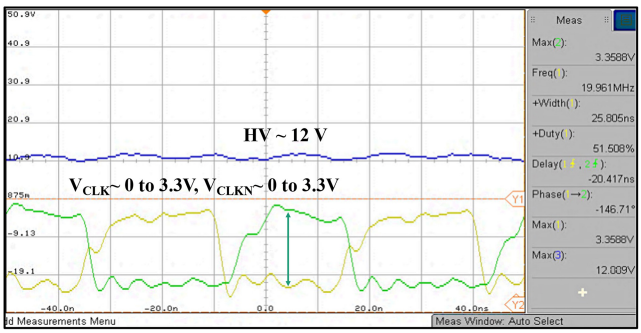


FIGURE 21. Charge pump output voltage at 420 μA load current.

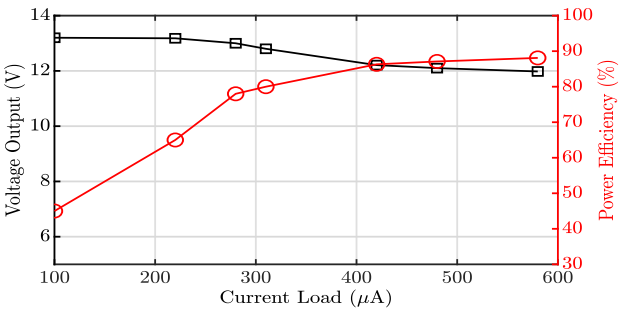


FIGURE 22. Measured charge pump output voltage and PCE versus load current.

load. The maximum power efficiency is 89.1% at a maximum output current of 4 mA. Compared to previous reported integrated CPs [27], the proposed circuit is area efficient and has high overall VCE and PCE. Using a low-voltage standard CMOS process, the CP provides a reliable high voltage output at a high PCE. Due to the application specification, a regulation scheme for the CP is not required since at high frequency and 12 V output the ripple is only 110 mV with an additional off-chip decoupling capacitance. The maximum measured VCE is 90.9%.

C. TESTING WITH LED

The system was tested with a blue 452 nm LED (Blue 2214 SMD, Wurth Electronic WL-SMTW 150224BS7310). It has an intensity of around 1-10 mW/mm^2 and an emitting area of 0.8 mm^2 [26]. A dc supply voltage of 3.3 V from the regulating rectifier provides a 10.44 mA to the LED via a 4 × 4 matrix in the stimulator unit [see Figure 1 and Figure 15 (a)]. The optical power pP_{LED} measured using a power energy meter console (PM100D) with a cable (S121C) was 3.6 mW. The power density, $P_{LED\_Density}$ is:

$$P_{LED\_Density} = \frac{pP_{LED}}{(0.8\text{mm})^2} = 2.31\text{mW/mm}^2 \quad (13)$$

which is suitable for optical stimulation. The measured power consumption of the LDO, P_{LDO}, is 864 μW. Equations (14) to (16) calculate the system efficiency for the outputs that will be used for the targeted stimulation application:

$$\eta_{chip} = \frac{P_{REG\_REC}}{P_{RX}} = 84.2\% \quad (14)$$

$$\eta_{PMU} = \frac{P_{REG_{REC}} + P_{CP}}{P_{RX}} = 76.6\% \quad (15)$$

$$\eta_{system} = \frac{P_{LED}}{P_{RX}} = 66.7\%. \quad (16)$$

The overall system efficiency, η_{system}, from the receiver, P_{RX}, to the LED, P_{LED}, is sufficient for optogenetic stimulation. The dc supply HV (12V) drives the high voltage electrical stimulators. The charge pump was tested for electrical stimulation with a load resistance of 100 Ω to generate the pulse waveform shown in Figure 23. The waveform shapes are controlled by the logic within the stimulator unit for different applications.

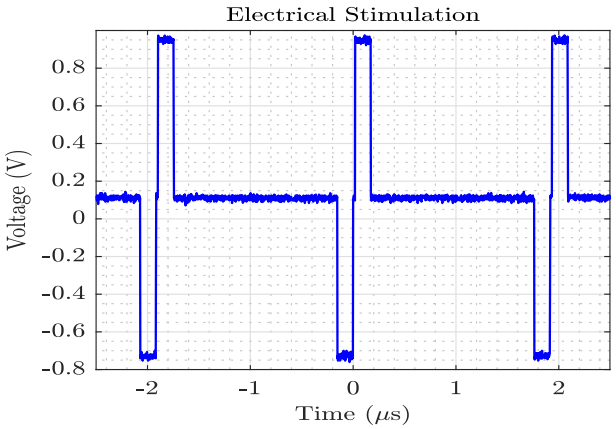


FIGURE 23. Voltage stimulation pulses with a load resistance of 100 Ω.

Table 1 compares the measured performance of the circuit to state-of-the-art PMUs for optogenetic applications. The design provides high PCE/VCE compared to other work and has only one off-chip capacitor for the *RX* coil tuning. It provides high power delivery that is suitable for high current applications.

V. CONCLUSION

A power-efficient PMU for an implantable optical-electrical stimulator has been presented. The system exploits power optimization techniques, including two different modes of operation for optimum power delivery. The paper details the design of a regulating rectifier with a novel body biased high-speed comparator, providing 3.3 V for the operation of the stimulator, a 3-stage latch-up charge pump with 12 V output for the output stage of the optical-electrical stimulator, and 1.8 V for digital control logic. The chip has been fabricated in a 180 nm CMOS process and tested with electrical and optical stimulators. Measured results show that for a regulated output of 3.3 V delivering 30.3 mW power, the peak power conversion efficiency is 84.2% at 6.78 MHz inductive link frequency reducing to 70.3% at 13.56 MHz. The VCE and PCE of the charge pump are 90.9% and 89.1%, respectively. The system operates at frequencies that are also suitable for data delivery. It achieves a high efficiency, high level of integration and small area compared to other state-of-the-art designs. This work can be further explored and optimized for different biomedical applications that require fully on-chip systems.

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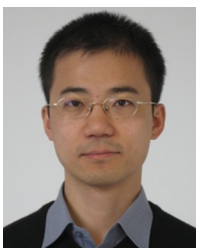

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