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A Reconfigurable Setup for the On-Wafer Characterization of the Dynamic R_{ON} of 600 V GaN Switches at Variable Operating Regimes

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Abstract: Charge-trapping mechanisms observed in high-voltage GaN switches are responsible for the degradation of power converter efficiency due to modulation of the effective dynamic ON-resistance (R_{ON}) with respect to its static value. Dynamic R_{ON} degradation is typically dependent on the blocking voltage and the commutation frequency and is particularly significant in new technologies under development. The possibility to characterize this phenomenon on GaN switch samples directly on-wafer, under controlled operating conditions that resemble real operations of the DUT in a switching mode power converter is extremely valuable in the development phase of new technologies or for quality verification of production wafers. In this paper, we describe a setup that allows this characterization: dynamic R_{ON} degradation of on-wafer 600 V GaN switches is characterized as a function of the V_{DS} blocking voltage, the V_{GS} driving voltage, and at different temperatures. The dependency on the switching frequency is identified by measuring the current recovery of the switch after the application of blocking voltages of different durations.

Keywords: GaN switches; trapping effects; ON-resistance; dynamic ON-resistance; GaN device characterization

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1. Introduction

Wide band gap (WBG) semiconductors have recently become an important reality in the power electronic converter market and their intrinsic superior performance with respect to Si-based counterparts [1–3] is progressively increasing the number of applications where they become the preferred choice since their added value justifies the nominally larger cost per part. Probably the most important field of application of power WBG technology is the automotive industry, which is under a tremendous renovation towards vehicle electrification [4,5]. As a matter of fact, the main power converters of an electric or hybrid vehicle, namely the traction inverter, the DC-DC high voltage bus converter, and the on-board battery charger, are components that gain exceptional advantages from the exploitation of WBG devices since the higher volumetric power density and higher efficiency achieved by exploiting these technologies enable components miniaturization, extend the vehicle range, and shorten the charging time. In particular, low conduction resistance R_{ON} and low gate charge and parasitic capacitances are the key parameters of WBG devices that provide low conduction and switches losses, enabling higher switching frequency operation with associated high efficiency [6].

Between WBG technologies, silicon carbide (SiC) power switches have already achieved popularity: these switches are commercially available from a fairly large number of providers [7] and several end-user products exploiting this technology are present in the market [8].

GaN power switch technologies have shown the potential to further increase power converter performances due to their even better $R_{DS} \times Q_G$ figure of merit (FOM). GaN transistors are HEMT devices (high electron mobility transistors) based on a complex AlGaN/GaN hetero-epitaxy structure that provides very high charge density and mobility. They are lateral conduction devices derived from RF/microwave GaN transistor technologies that apply, among others, techniques to further increase the breakdown voltage [9] and to shift the gate voltage threshold to a positive value, thus obtaining enhance-mode normally off power switches [10], which are the sole product employable in some power applications (for RF/microwave applications, GaN HEMTs are normally on devices). As a matter of fact, the technological process for obtaining normally off devices, while maintaining high conduction and dynamic characteristics, has historically required several process iterations. Thus, at present GaN technology is less mature than SiC and only a few providers can offer high voltage (i.e., >600 V) commercial GaN switches with the performance and reliability levels required by automotive applications [11–14]. Nonetheless, given the enormous potential of this technology, all the main providers of power electronic devices are pursuing the optimization of their power GaN devices and then several foundries are working towards the development and optimization of these processes.

One well-known and peculiar issue of GaN transistors is the presence of charge-trapping effects, which are responsible for the modulation of the charges available for current conduction, with a consequent degradation of the conductivity of the channel during dynamic regimes. This issue has been largely investigated in more mature RF/microwave technologies where trap-related phenomena are responsible for power amplifiers' efficiency degradation and signal distortion [15–18]. In power device technologies, these phenomena have a direct effect on the increment of the ON-resistance in dynamic regime with respect to its static (DC) value.

This dynamic R_{ON} degradation proportionally increases the converter conduction losses. In the literature, a large interest can be found for both the identification of the physical mechanisms that support these phenomena [19] and their characterization [20,21]. A good understanding of physics-based modeling is helpful for the optimization of the technologies, whereas a precise characterization is fundamental for performance assessment. The physical description of these phenomena is beyond the scope of this paper; nonetheless, it is interesting to observe that R_{ON} degradation is a function of the application voltages, of the switching frequency and varies with temperature [10,21]. Indeed, it has been observed that the trapping state density increases with the electric field and then with the blocking voltage applied at the device terminal during the OFF state in dynamic switching-mode operation. For the same reasons, the gate driving voltage can also play a role in this mechanism. As for dynamic effects, the charge-trapping and release-time constants (that give the frequency dependency of dynamic R_{ON} modulation) vary with the technological solutions and their energy levels are a function of the temperature.

In this context, this paper describes a measurement set-up for a precise characterization of the dynamic R_{ON} of high-voltage on-wafer devices with the possibility to modify the V_{DS} blocking voltage, the V_{GS} gate driving voltage, the commutation period, and the temperature to assess the impact of each contribution. This type of setup can be valuable for foundries to test different solutions of experimental devices during the optimization of a new process and for the quality verification of production wafers. Indeed, since it is associated with trapping phenomena, the wafer to wafer dispersion of the dynamic R_{ON} can be also considered an indication of possible reliability concerns. The proposed measurement methodology is described in Section 2; Section 3 describes the implemented setup; the experimental measurements are provided in Section 4.

2. Dynamic Measurement Methodology

The proposed time-domain technique for the evaluation of the power switch DUT $R_{DS,ON}$ is described in this section. The DUT is measured under a periodic isothermal regime described in the waveforms of Figure 1. The diagram of Figure 2 summarizes the

measurement procedure settings and steps. During the period, the DUT is switched between a bias state $(V_{GS,ON}, V_{DS,ON})$ and a blocking state $(V_{GS,OFF}, V_{DS,Block})$. As described in the waveforms of Figure 1, a short safety margin T_D (500 ns, as will be described in the next section) between V_{GS} and V_{DS} transitions is used to avoid over-currents at the application/release of the blocking voltage $V_{DS,Block}$. The blocking state duration is negligible with respect to the period, thus the DUT is biased in the selected bias state for more than 99% of the period (i.e., the V_{GS} waveform duty cycle is more than 99%). The bias state $(V_{GS,ON}, V_{DS,ON})$ is selected so that the corresponding $I_{DS,ON}$ meets the following requirements: (1) it must be large enough to enable high-accuracy current sensing; (2) it must be small enough to induce a negligible power dissipation $(P_{DISS} = R_{DS,ON} \cdot I_{DS,ON}^2)$ so that the DUT can be considered isothermal with the thermal chuck of the probe station over which is placed during the entire duration of the measurement.

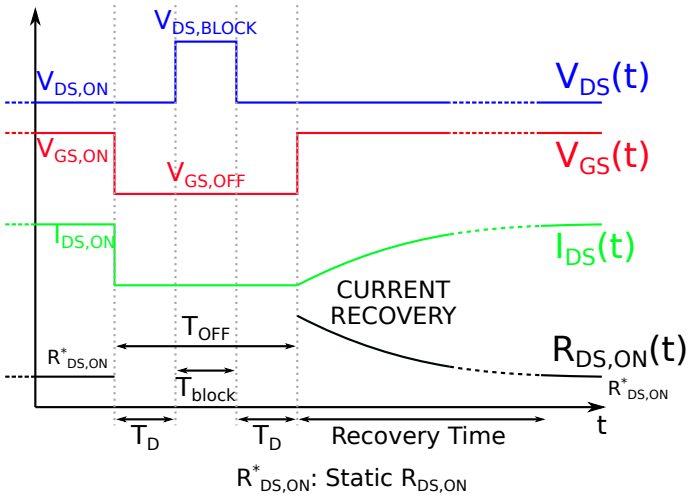


Figure 1. Typical waveforms of V_{GS}, V_{DS}, and I_{DS} during the dynamic characterization in periodic regime: waveforms of one period.

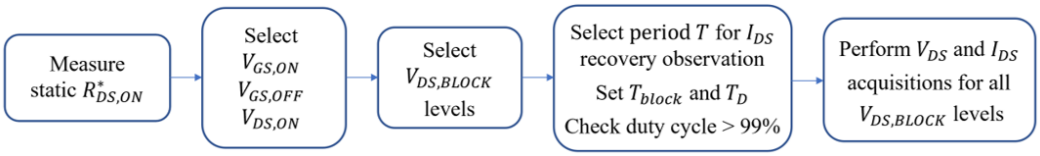


Figure 2. Setting and steps of the proposed measurement procedure under periodic regime.

In this way, thermal effects are not involved in the observed dynamics of the drain current, and they can be exclusively ascribed to trapping/de-trapping mechanisms. During the application of the blocking voltage in T_{Block}, the combination $(V_{GS,OFF}, V_{DS,Block})$ applies high electric fields to the DUT channel that trigger charge trapping phenomena, as in switching-mode power converter operation. By reapplying the same bias state $(V_{GS,ON}, V_{DS,ON})$ after the blocking event, the slow recovery of the drain current towards the $I_{DS,ON}$ can be observed. If the period duration is selected large enough to complete the entire de-trapping mechanism, $I_{DS,ON}$ at the end of the period can be considered the static value of the current, and the corresponding value of the ratio $R_{DS,ON}(T_P) = R^*_{DS,ON} = V_{DS}(T_P)/I_{DS}(T_P)$ at the end of the period T_P the static $R^*_{DS,ON}$. The result of this characterization is the dynamic variation of $R_{DS,ON}$ over time after the blocking voltage event that triggers the trap capture, which is the lower plot in Figure 1. This gives an immediate indication of the time constants related to the de-trapping mechanisms, which is a useful input for process evaluation and physical modeling. On the other hand, a direct indication related to the application can also be obtained considering the inverse of the recovery time $f_s = 1/T_{recovery}$ as the corresponding switching frequency of the application: in this way, $R_{DS,ON}$ degradation for the actual switching frequency of the application can be evaluated. By varying the values of $V_{DS,Block}$

and $V_{GS,OFF}$, the dependence of $R_{DS,ON}$ degradation from applied voltages is assessed. Finally, by varying the thermal chuck temperature (and thus the DUT temperature since it is practically iso-thermal) the effect of temperature can also be evaluated; indeed, trap energy states are temperature dependent. The proposed setup can implement this characterization with the flexibility to vary all the described parameters. The main challenges of this implementation are the capability to apply precise dynamic high voltage excitations to the DUT and to realize precise and noiseless dynamic sensing of current/voltages for the computation of the dynamic $R_{DS,ON}$.

3. Setup Description

A functional simplified description of the setup is illustrated in Figure 3. The DUT is placed in a probe station where gate, source, and drain pads are directly contacted with low-parasitic on-wafer probes, while a thermally controlled chuck (Temptronic TP03215A) sets the working temperature beneath the wafer or the metal carrier used for soldering bare die device samples.

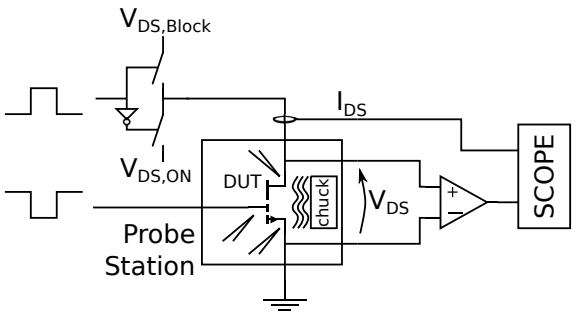


Figure 3. Functional simplified description of the setup.

The V_{DS} excitation switching between $(V_{DS,ON}, V_{DS,Block})$ values needs to be provided by an isolated and fast switching leg that alternatively connects the DUT drain pad between two isolated voltage sources at $V_{DS,ON}$ and $V_{DS,Block}$ values provided by dedicated power supplies. The DUT $I_{DS,ON}$ and $V_{DS,ON}$ are sensed by current/voltage probes and acquired by a digital oscilloscope. A more detailed description of the implemented set-up is provided in Figure 4.

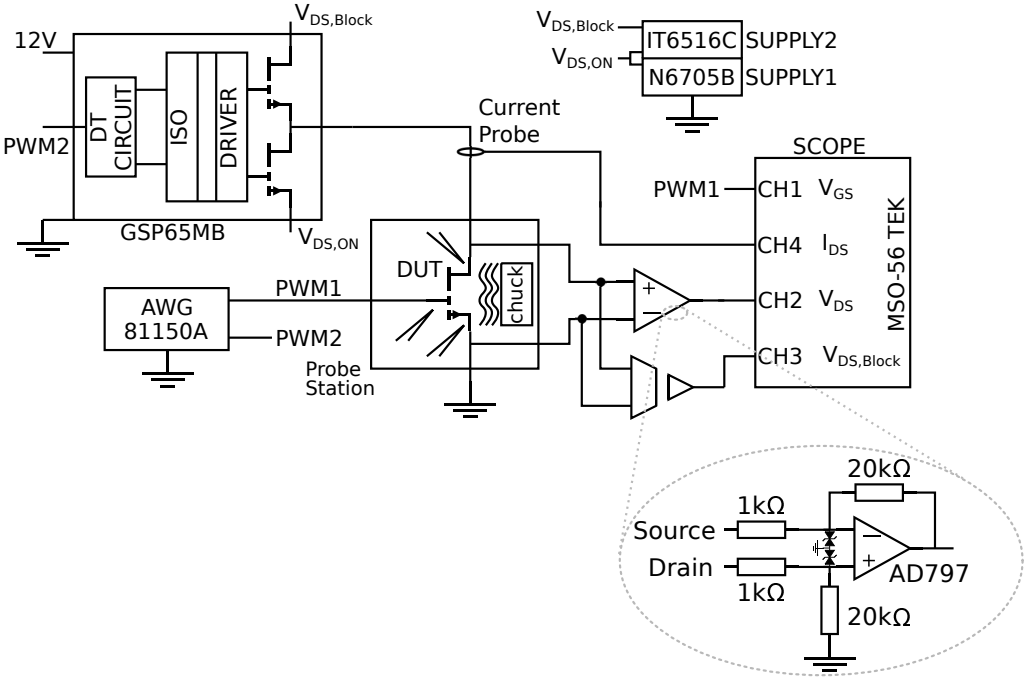


Figure 4. Schematic of the reconfigurable setup for dynamic R_{ON} measurement.

The probe station is a Cascade Microtech Summit 9000 equipped with a Temptronic ThermoChuck system. In order to reproduce excitations similar to operative regimes, the switching leg needs to have dynamic characteristics similar to the DUT. Thus, it is realized by exploiting the GSP65MB Evaluation Board of the GaN system [22]: this is basically a half-bridge exploiting commercial 25 mΩ, 650 V GaN HEMT devices (which represent the state-of-the-art high-voltage GaN switches), Silicon Labs Si4121 isolated gate drivers, dead-time logic circuitry for selectable dead-time control, and local low-inductance DC-link capacitors to sustain fast commutations without voltage drops. The DC supplies for the bias $V_{DS,ON}$ and blocking voltage $V_{DS,Block}$ generation are Agilent N6705B and ITECH IT6516C, respectively. The Agilent 81150A arbitrary waveform generator is used to control the switching leg (PWM2 in the figure) and to directly control the DUT gate (PWM1 in the figure), assuring the required synchronization to the two excitations (V_{GS}, V_{DS}). Wide-band current sensing is provided with Keysight 100 MHz N2783A current probe with 1% accuracy. The sensing of the device V_{DS} is quite complex because of the required dynamic range: the characterization procedure needs to measure high $V_{DS,Blocking}$ during the device switch-OFF to verify the blocking voltage and its synchronization with the DUT V_{GS}, and very low $V_{DS,ON}$ during device conduction for an accurate evaluation of $R_{DS,ON}$. In particular, for 600 V GaN switch technology, the maximum $V_{DS,Block}$ is in the order of 400 V and $V_{DS,ON}$ in the order of mV. For this reason, a single acquisition channel for V_{DS} is not a viable solution, but two different methods are used simultaneously, as described in Figure 4. A first acquisition channel uses the isolated active differential probe with 40 MHz bandwidth Aaronia ADP1 to acquire the entire evolution of V_{DS} in the period and scale it 100:1 to fit the oscilloscope voltage range: this is useful to monitor $V_{DS,Block}$ and the synchronization with V_{GS}, but this acquisition does not have enough sensitivity for a precise and useful acquisition of $V_{DS,ON}$. For this acquisition, a high sensitivity and wide-band acquisition channel is implemented in a dedicated PCB exploiting the low-offset and low-noise Analog Devices AD797 operational amplifier in the $\times 20$ voltage gain configuration described in the inset of Figure 4. This acquisition channel enables the accurate characterization of a V_{DS} waveform below 1 mV. As described in [23], with this configuration, the Op-Amp input is protected by means of two TVS diodes in antiparallel configuration from high-voltage $V_{DS,Block}$. This solution avoids the saturation of the oscilloscope acquisition channel and largely limits the saturation of the Op-Amp. As a consequence, a few µs after the blocking event, the Op-Amp exits saturation and is capable of correctly measuring $V_{DS,ON}$, and then $R_{DS,ON}$ can be computed. Finally, a simple passive probe is used to sense the driving voltage V_{GS} applied to the DUT. The digital oscilloscope used in the setup is Tektronix MSO-56 scope. A picture of the entire setup is provided in Figure 5.

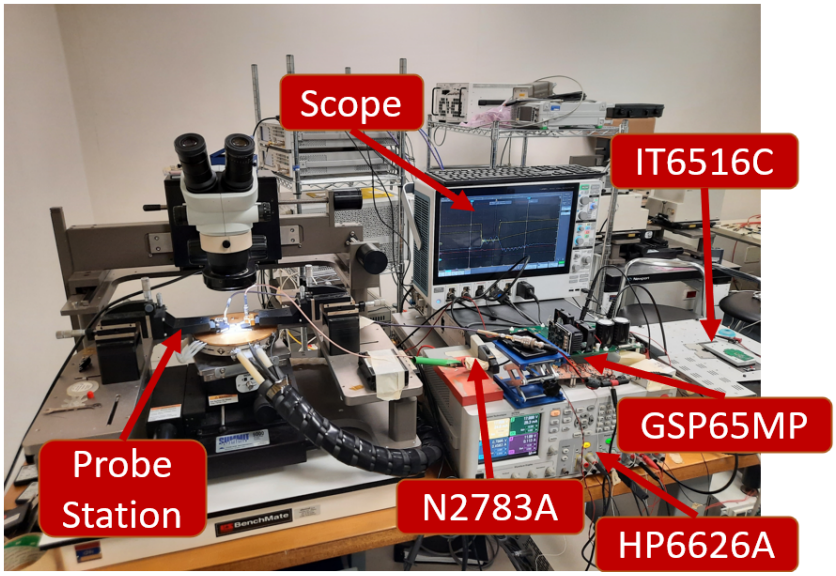


Figure 5. Picture of the reconfigurable setup for dynamic R_{ON} measurement in the laboratory.

4. Experimental Characterization of 600 V GaN Switches

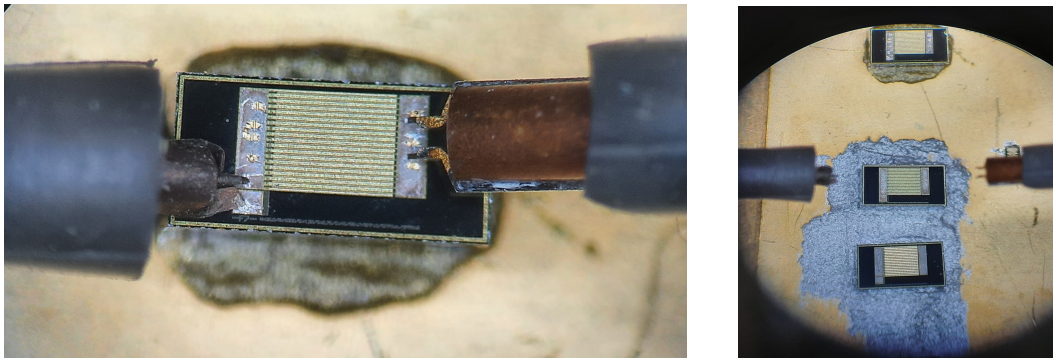
The described measurement setup is used to characterize the dynamic ON-resistance of 600 V GaN transistors. The transistors are p-GaN e-mode HEMTs on a silicon substrate coming from an experimental wafer of a process in the development phase in a research foundry. The preliminary electrical specifications of the switches are shown in Table 1. The very low values of parasitics are indicative of the capability of this technology for high-switching frequencies.

Table 1. DUT preliminary electrical specifications.

V_{BD}	V_{gs}	V_{th}	R_{DS}	C_{ISS} [1]	C_{OSS} [1]	C_{RSS} [1]
600 V	5–6 V	2–2.5 V	0.5 Ω	43 pF	18 pF	1 pF

[1] V_{DS} = 200 V.

The transistor dies have been soldered to a metal carrier and contacted with on-wafer micro-probes as described in the pictures of Figure 6.

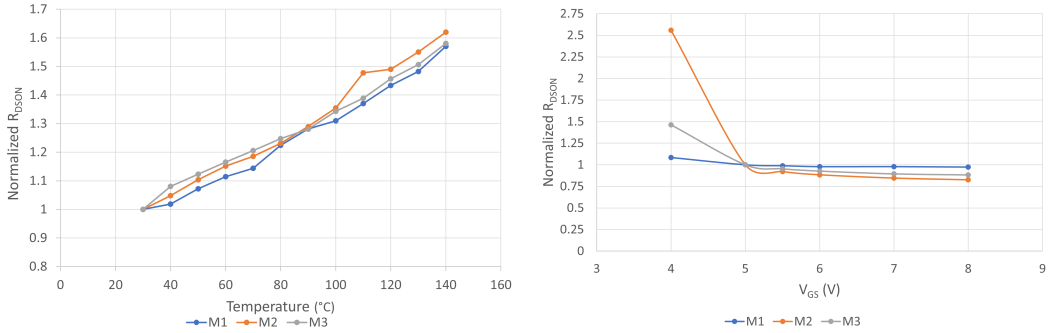


(**a**) (**b**)

Figure 6. Integration of the DUT within the measurement setup. (**a**) Probe connection to the DUT. (**b**) Three samples (M1, M2, and M3) are placed on the same metal carrier through epoxy with high electrical and thermal conductivity.

4.1. Static Measurements

For the evaluation of the dynamic ON-resistance degradation, the static $R_{DS,ON}$ must be identified. A de-embedding procedure based on the measurement of the parasitic resistance of the setup when the DUT is replaced by a short circuit was performed. As discussed before, to guarantee iso-thermal conditions in temperature-dependent measurements of the sole trapping phenomena, the DUT must be properly biased to show negligible self-heating compared to the temperature controlled by the chuck. Thus a "measuring" bias current of 500 mA was selected as a good compromise between current measurement accuracy and device self-heating. Indeed, since the estimated thermal resistance of the DUT is 2.2 °C/W and the static $R_{DS,ON}$ around 0.5 Ω, the dissipated power is about 125 mW with a resulting negligible temperature increase $\Delta T = 0.275$ °C. This bias current was used for both static and dynamic measurements, which can consequently be considered isothermal. The static $R_{DS,ON}$ of three samples (M1, M2, and M3) was measured at increasing temperatures up to 140 °C (maximum rating of the probes); the results are shown in Figure 7a, where the $R_{DS,ON}$ is normalized to the reference value at 30 °C. Additional static measurements were carried out at different V_{GS} to evaluate the gate driving voltage requirements. The results are shown in Figure 7b, where the static R_{DS} is plotted versus the gate driving voltage and normalized to the value at V_{GS} = 5 V. Above V_{GS} = 5 V, all the samples are fully ON since the channel resistance reveals a negligible improvement for higher voltages, whilst for V_{GS} = 4 V the devices show different behaviors probably due to a shift of threshold voltage which is expected for a young technological process [24]. Hence, $V_{GS,ON}$ = 5 V is chosen for dynamic measurements.



(**a**) (**b**)

Figure 7. Static measurements for M1, M2, and M3 samples. (**a**) Normalized $R_{DS,ON}$ vs. temperature at V_{GS} = 5 V; (**b**) normalized $R_{DS,ON}$ vs. V_{GS} for ON state.

4.2. Dynamic Measurements

The dynamic measurements were carried out following the procedure described before in Figure 1. The measurement period is fixed to 1 ms; indeed, this corresponds to an equivalent application-related switching frequency regime of 1 kHz, and any additional recovery from traps related to higher time constants is of no interest for any practical application. According to the notation of Figure 1, the selected T_{Block} = 500 ns, whereas the entire T_{OFF} = 1.5 µs to include two additional 500 ns dead bands to avoid over-current events. The first test was the sensitivity of $R_{DS,ON}$ to the gate switch-OFF voltage $V_{GS,OFF}$. Normally ON GaN devices are typically switched off with null or negative V_{GS}. While $V_{GS,OFF}$ = 0 V is suitable for a complete device turn-off, negative values are often used to shorten the commutation time and increase the margin against undesired turn-ON due to the G-D Miller capacitance effect. Nonetheless, negative $V_{GS,OFF}$ values increase the electric fields in the channel during turn-off and can potentially increase trapping with a consequently higher degradation of the dynamic $R_{DS,ON}$ effects. The investigation on the sensitivity towards the sole $V_{GS,OFF}$ was performed by setting the blocking voltage $V_{DS,Block}$ = 0 V at 25 °C. The time domain waveforms of this test are shown in Figure 8.

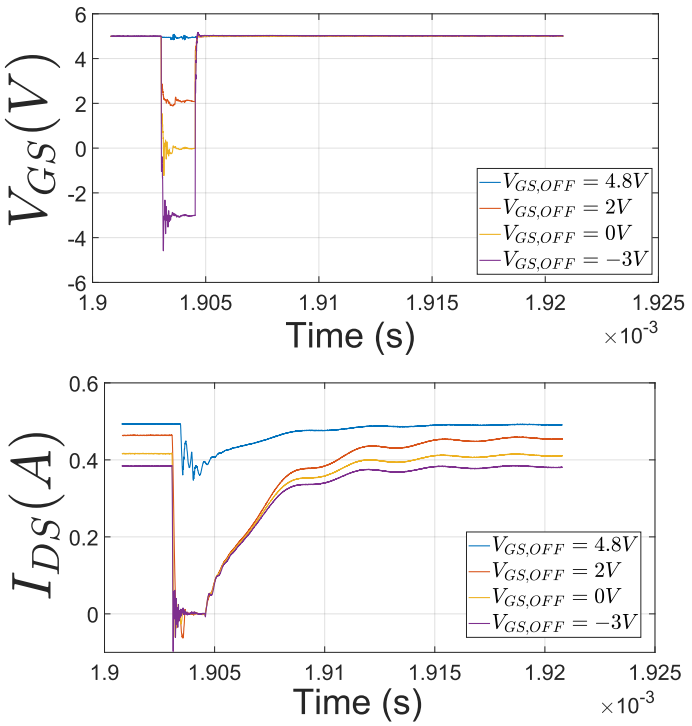


Figure 8. V_{GS} (**up**) and I_{DS} (**down**) waveforms in case of null blocking voltage at 25 °C. The displayed time interval starts 5 µs before the trigger event and ends 20 µs after the trigger event.

It is evident that $V_{GS,OFF}$ = 2 V is sufficient to completely switch off the device: the simple event of device switch-off triggers trap-capturing mechanisms that cause a decrease of the drain current, which does not recover completely even after the entire period of 1 ms. Indeed, the asymptotic current value (i.e., $I_{DS,ON}$ in Figure 1) for all the conditions where the device has effectively switched-off (i.e., $V_{GS,OFF}$ = 2 V, 0 V, −3 V) is lower than the reference value with $V_{GS,OFF}$ = 4.8 V. The lower $V_{GS,OFF}$, the higher the current $I_{DS,ON}$ reduction for fixed $V_{GS,ON}$, $V_{DS,ON}$. From the figure it can also be observed that the current recovery is divided into two parts: an initial fast recovery where in 15–20 µs the current reaches about 90% of its asymptotic value and a second slow recovery that lasts for the rest of the 1 ms period. This is an indication of different time constants associated with the de-trapping mechanisms as observed in other studies [16]. As a summary, in Figure 9 the measured degradation of $R_{DS,ON}$ (evaluated at 1 ms) for the three samples and normalized to the nominal case is shown. For this particular technology, still in the early development phase, if the device is switched-off with negative $V_{GS,OFF}$ for better driving performance (increased noise immunity and fast commutation), the conduction performance is worse due to increased trapping effects. $V_{GS,OFF}$ = 0 V is chosen to perform dynamic measurements at variable blocking voltage provided in the following.

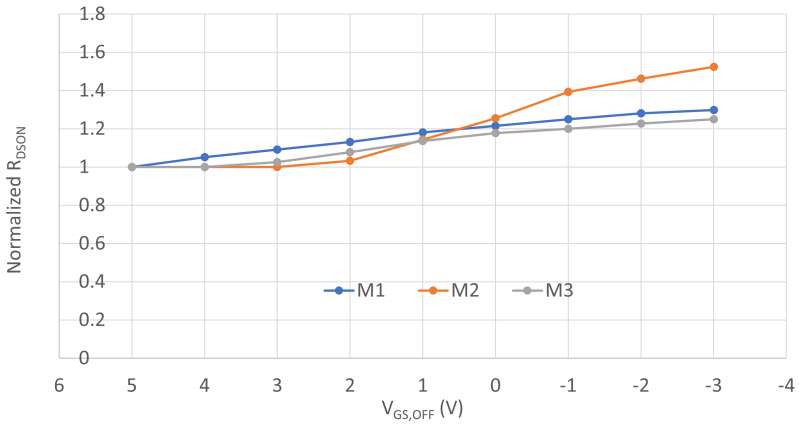


Figure 9. Normalized $R_{DS,ON}$ vs. $V_{gs,OFF}$ for M1, M2, and M3 samples.

The effect of increasing blocking voltages $V_{DS,Block}$ on $R_{DS,ON}$ = 0 V has been investigated varying $V_{DS,Block}$ up to 400 V, which is typically the maximum DC link voltage for a 600 V technology. In Figure 10, the four main characteristics measured by the setup are displayed.

The two different acquisition channels of V_{DS} show significant information during different parts of the period. The increasing blocking voltages during T_{Block} can be evaluated from the acquisition of the isolated voltage probe, whereas the small value of V_{DS} during the rest of the period is acquired by the high accuracy Op-Amp channel and used for the computation of $R_{DS,ON}$.

It is interesting to observe that the V_{DS} waveform from this latest channel shows the saturation interval of the Op-Amp that lasts only about 2 µs after T_{Block}. Once the Op-Amp exits saturation, an additional 15–18 µs is necessary for the complete extinction of a residual oscillation. Thus, the computation of $R_{DS,ON}$ can be considered completely reliable about 20 µs after the blocking voltage event. Additional minimization of parasitics in the construction of the bench could be implemented to shorten this acquisition delay. From the data in Figure 10, $R_{DS,ON}$ is computed for the entire period and is shown in Figure 11, normalized to the $V_{DS,Block}$ = 0 V case.

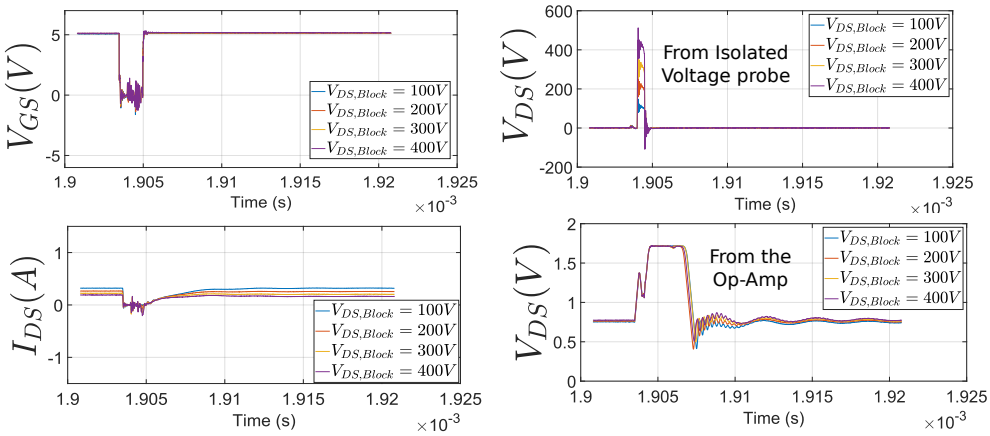


Figure 10. V_{GS}, I_{DS}, and V_{DS} (from isolated voltage probe and Op-Amp) acquired waveforms for $R_{DS,ON}$ calculation at increasing blocking voltage. The displayed time interval starts 5 µs before the trigger event and ends 20 µs after the trigger event.

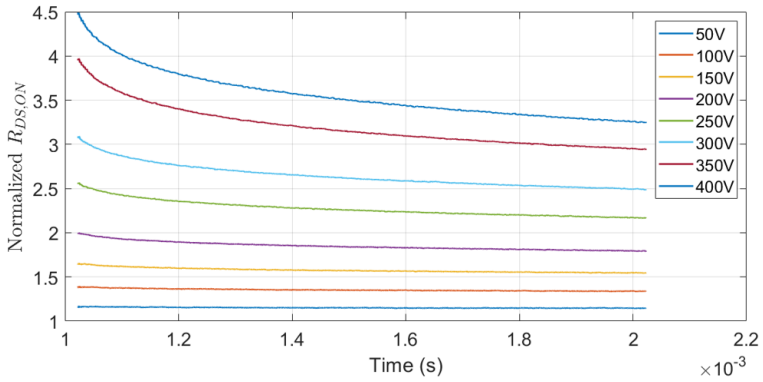


Figure 11. Normalized $R_{DS,ON}$ of a single sample measured over the entire ON-time.

The waveforms point out that the trap-activated degradation of the dynamic $R_{DS,ON}$ for this technology under development is very relevant. This effect is already detectable at $V_{DS,Block}$ = 50 V and becomes worse at increasing voltages with $R_{DS,ON}$ reaching up to $\times$4.5 degradation just after the blocking voltage pulse for the higher $V_{DS,Block}$ = 400 V. In Figure 12, the measured $R_{DS,ON}$ at the end of the ON-state is shown for the three samples as a function of blocking voltage. These data confirm the high degradation levels and the dependence on the applied voltage. Nonetheless, non-negligible differences between samples suggest significant parameter dispersion among devices, another sign of the low level of maturity of the process. The effect of temperature was estimated by measuring the DUT $R_{DS,ON}$ for different chuck temperatures. The $R_{DS,ON}$ measured at the end of the 1 ms period for sample M2 at different chuck temperatures is shown in Figure 13. $R_{DS,ON}$ is normalized to its static value at the corresponding temperature. The plots show that the trap-related degradation effect on $R_{DS,ON}$ decreases for higher temperatures. As observed in [25], this is probably due to the fact that higher temperatures accelerate trap release transients and increase the number of compensating trap release events during T_{Block}. The flexibility of the setup enables setting different parameters according to different requirements. For instance, for trap physical modeling purposes, it could be interesting to evaluate the trap release mechanisms for a longer time frame. The dynamic test at different blocking voltages has been repeated with a much wider period of 40 ms. Figure 14 shows the $R_{DS,ON}$ evolution from 5 ms to 40 ms after T_{Block}: it can be observed that even in a such large time frame the static value of $R_{DS,ON}$ is not reached, indicating that the time constants associated to traps are extremely long.

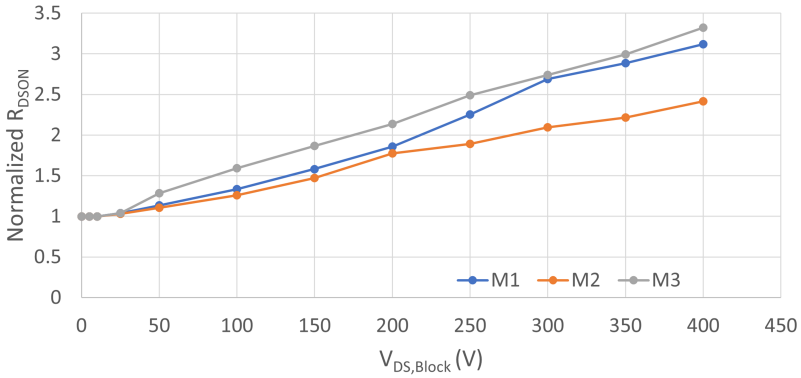


Figure 12. Normalized $R_{DS,ON}$ evaluated at the end of ON-time for the M1, M2, and M3 samples.

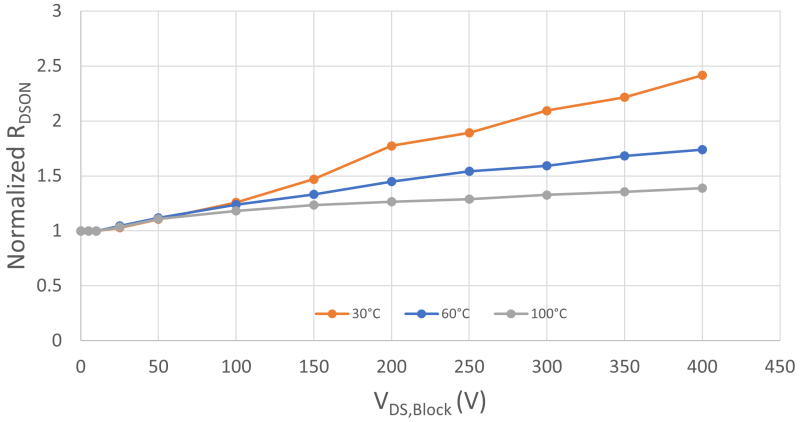


Figure 13. Normalized $R_{DS,ON}$ vs.V_{block} of sample M2 for three temperatures: 30 °C, 60 °C, and 100 °C.

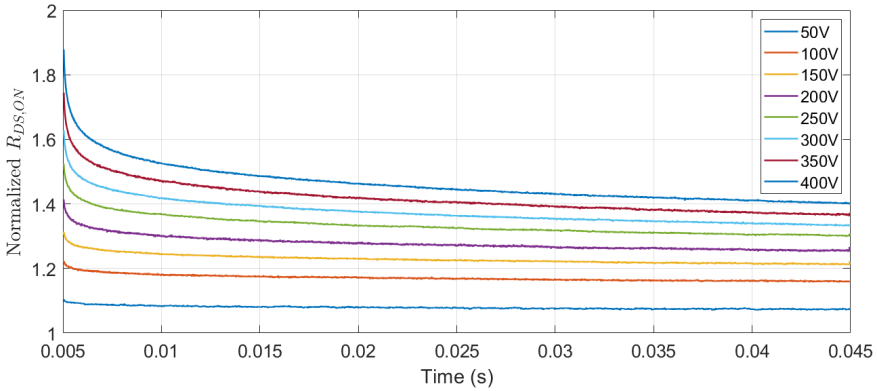


Figure 14. Normalized $R_{DS,ON}$ vs.$V_{DS,Block}$ with an extended 40ms period to evaluate the traps' long time constants.

Another parameter that can be varied is the duration of the blocking voltage application T_{Block}. This parameter is often described in the literature as the duration of the trap-filling pulse. The dependence of the trap-induced degradation to the duration of the trap-filling pulse has been investigated in the literature, sometimes with observed opposite behaviors depending on the duration scale of T_{Block} [15,26–28]. For switching mode power converter applications, a dependency of $R_{DS,ON}$ on T_{Block} implies additional dependency of the device performance versus the variation of the duty cycle. Since the target application frequency of this technology is tens to hundreds of KHz, measurements with T_{Block} ranging from 500 ns to 50 µs, while maintaining the same duty cycle, were carried out. These measurements showed practically no dependence of $R_{DS,ON}$ degradation to T_{Block} (in this pulse width variation range).

5. Conclusions

A flexible setup for the characterization of the dynamic $R_{DS,ON}$ of on-wafer high-voltage power transistor has been implemented and used for the characterization of 600 V GaN on Si power switches. The setup enables characterizing the degradation of $R_{DS,ON}$ varying driving voltage, blocking voltage, temperature, and the duration/timing of the applied waveforms, enabling us to explore the degradation of the device performance at different application regimes and also to acquire important information for the process' physical modeling and optimization. Due to the very limited power dissipation involved in the measurement, the proposed technique can accurately control the DUT temperature without the need for advanced thermal modeling and allows us to apply high voltage excitations compatible with real application scenarios directly on-wafer. The capability to characterize the dynamic $R_{DS,ON}$ of GaN devices directly on wafer before the dicing and packaging of the power transistor is very valuable and time-saving. Therefore, the proposed setup and measurement technique can be useful for foundries during the evolution of a new technology or for quality tests of production wafers. The measurement described in this paper on a new high-voltage GaN technology under development shows the degradation of the dynamic $R_{DS,ON}$ as a function of both the off-state driving voltage $V_{GS,OFF}$ and the V_{DS} blocking voltage $V_{DS,Block}$. The selection of negative off-state gate voltage is responsible for increased charge trapping that causes degradation of dynamic $R_{DS,ON}$ up to 20–50%. The observed dynamic $R_{DS,ON}$ degradation versus $V_{DS,Block}$ blocking voltages up to 400 V are as relevant as $\times$4.5 factor increase with respect to its static value. The measurement shows that the time constant associated with de-trapping is in the order of several milliseconds; therefore, the corresponding current recovery does not have any beneficial effect on the dynamic $R_{DS,ON}$ at the application frequencies of interest for this technology (from tens to hundreds of kHz). Finally, it is observed that at increased temperatures the charge recovery is faster and some limited benefit can be observed on the dynamic $R_{DS,ON}$.

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