Toward Sustainable Transparent and Flexible Electronics with Amorphous Zinc Tin Oxide

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Abstract:

The present thesis addresses a sustainable approach to mechanically flexible and transparent electronic devices based on the amorphous oxide semiconductor zinc tin oxide (ZTO) as abundant and low-cost alternative to already industrially established materials such as amorphous indium gallium zinc oxide. ZTO thin films are deposited by radio frequency long-throw magnetron sputtering at room temperature to generally enable the implementation of common photolithography processes and further facilitate patterning of digital circuit elements on thermally unstable organic substrates.

Starting with the most basic device building blocks of integrated circuitry, various types of field-effect transistors are fabricated by implementation of amorphous ZTO as active channel material. Metal-semiconductor field-effect transistors and *pn* heterodiode based junctions field-effect transistors as well as conventional metal-insulator-semiconductor field-effect transistors are then compared regarding their electrical performance and long-term stability over a couple of months. A decisive step toward the successful interconnection of fundamental digital circuit elements, such as previously demonstrated simple inverters, is to ensure sufficient output level compatibility between the signals of associated logic components. Accordingly, the Schottky diode field-effect transistor logic approach is adapted for amorphous ZTO based devices in order to facilitate cascading of multiple inverters consisting of unipolar devices. Field-effect transistor properties as well as the circuit design have been continuously improved to enhance the overall performance in terms of functionality and low-voltage operation. Corresponding logic inverters are finally integrated in ring oscillator circuits to gain insights into the dynamic properties of digital circuit building blocks based on amorphous ZTO.

Ultimately, ZTO has been fabricated on mechanically flexible polyimide substrates to determine the elastic and electrical properties of amorphous ZTO thin films in dependence on external tensile and compressive stress induced by mechanical bending. Further, associated flexible metal-semiconductor field-effect transistor are investigated regarding their performance stability under tensile strain.

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Die vorliegende Arbeit umfasst die Herstellung und Charakterisierung aktiver elektrischer Bauelemente und integrierter Schaltkreise auf Basis des amorphen Oxidhalbleiters Zink-Zinnoxid (ZTO). Als vielversprechende nachhaltige und kostengünstigere Alternative zu dem bereits industriell etablierten Halbleiter Indium-Gallium-Zinkoxid wird insbesondere die Eignung von ZTO in optisch transparenter sowie mechanisch flexibler Elektronik untersucht. Um entsprechend Kompatibilität mit thermisch instabilen organischen Substraten sowie herkömmlichen Fotolithografieverfahren zu gewährleisten, beschränkt sich die Züchtung von ZTO-Dünnfilmen mittels Hochfrequenz-Magnetron-Distanzkathodenzerstäubung ausschließlich auf Herstellungsprozesse bei Raumtemperatur.

Zunächst wird auf die Umsetzung verschiedener Feldeffekttransistor-Typen auf Basis amorphen ZTOs eingegangen, welche elektrisch charakterisiert und schließlich vor dem Hintergrund der Anwendung in integrierten Schaltkreisen vergleichend gegenübergestellt werden. Neben konventionellen Metall-Isolator-Halbleiterstrukturen wird vor allem näher auf Metall-Halbleiter-Feldeffekttransistoren sowie Sperrschicht-Feldeffekttransistoren auf der Grundlage von *pn*-Heteroübergängen eingegangen, da diese hauptsächlich in Bereichen hoher geforderter Schaltfrequenzen zum Einsatz kommen. Da integrierte Schaltkreise auf Basis unipolarer Feldeffekttransistoren eines Ladungsträgertyps inkonsistente Signaleingangs- sowie -ausgangspegel aufweisen, wird die Schottky-Dioden-Transistorlogik adaptiert, um entsprechend die Verknüpfung mehrerer Logikgatter auf Basis amorphen ZTOs zu gewährleisten. Durch geeignete Signalrückkopplung werden komplexere Schaltungen wie Ringoszillatoren realisiert, welche anhand von Laufzeitanalysen Aufschluss über die Schaltgeschwindigkeit ZTO basierter Feldeffekttransistoren geben.

Abschließend werden amorphe ZTO-Dünnfilme auf flexiblen Polyimid-Substraten hergestellt und bezüglich der elastischen sowie elektrischen Eigenschaften in Abhängigkeit von exzessivem mechanischen Stress untersucht. Darüber hinaus werden flexible Metall-Halbleiter-Feldeffekttransistoren hinsichtlich ihrer Funktionalität und Stabilität gegenüber durch Biegeprozesse induzierte Verspannungen elektrisch charakterisiert.

Contents

I

Introduction

Throughout the past couple of decades, the semiconductor thin-film industry has been undergoing a disruptive technological evolution in order to keep pace with the ever-growing global market demands. Expectations driving change have more than ever centered around the need to continuously enhance performance efficiency while simultaneously reducing size and costs across all electronic device platforms. With traditional silicon based technology being already pushed to its limits, oxide semiconductors in particular have started to advance bulky and rigid electronics toward transparent, light-weight and flexible next-generation applications [1–3].

Until 2012, the pixels in liquid crystal displays (LCDs) were driven exclusively by transistors based on hydrogenated amorphous silicon [4]. Backlit displays, however, require transistors to be either transparent or, in case of silicon, sufficiently small, which in turn limits their current-driving ability. As LCD technology is more frequently replaced by organic light-emitting diodes (OLEDs) due to direct emission of richer colors, associated pixel-driving transistors require even higher supply current in such amounts amorphous silicon can not provide. Back in 1996, metal oxide thin films based on $CdO\text{-}GeO_2$ have been demonstrated to exhibit an extraordinary high electron mobility of about $10\,cm^2V^{-1}s^{-1}$ in spite of being amorphous, whereas the mobility in amorphous silicon barely reaches $1\,cm^2V^{-1}s^{-1}$ [5,6]. To this point, only a few amorphous conductors had been suggested, including InO_x and tin doped In_2O_3 [7,8]. It took more than ten years until amorphous oxide semiconductors (AOSs) eventually began to revolutionize the thin-film industry by proposing materials with unique and superior electrical and optical properties [9]. Key features of AOSs include low preparation temperatures, ease of fabrication combined with excellent uniformity and surface flatness as well as a wide processing temperature window depending on the chemical composition [10]. Consequently, AOSs are suited for large-area roll-to-roll production of mechanically flexible and therefore bendable electronics using thermally unstable organic substrates [11]. Since common polymers provide excellent flexibility, are lightweight and typically low in costs, flexible electronics eliminates the requirements for expensive wafers [12]. In addition, the feasibility of AOSs to bypass the physical rigidity of conventional semiconductor electronics opens up a wide range of innovative applications like wearable and textile-integrated systems [13–16]. Owing to the strong ionic character, AOSs further tend to exhibit fewer subgap states compared to covalent amorphous semiconductors, facilitating transistors to operate at significantly lower voltages due to the reduced contribution of defects to the subthreshold characteristics [17]. Above all, however, their high charge carrier mobility renders AOSs suitable for a broad variety of electronic applications, since the mobility inherently determines the device behavior through its frequency response in terms of higher charge carrier velocity and higher amounts of available driving current to charge capacities more rapidly [18].

Starting in 2006, the ultimate breakthrough of AOSs began with the demonstration of active-matrix LCDs and OLED displays based on amorphous indium gallium zinc oxide (IGZO) by major companies such as LG Electronics, Sharp and Samsung Electronics, as indicated by the rapid increase of annually released publications referring to amorphous IGZO in Fig. 1 [19–22]. With the IGZO patents being later licensed to Samsung Electronics and Sharp, both companies started to launch mass productions of amorphous IGZO based active-matrix LCDs in the 2010s for cutting-edge applications such as smart phones, tablets, notebooks and televisions [23,24]. In

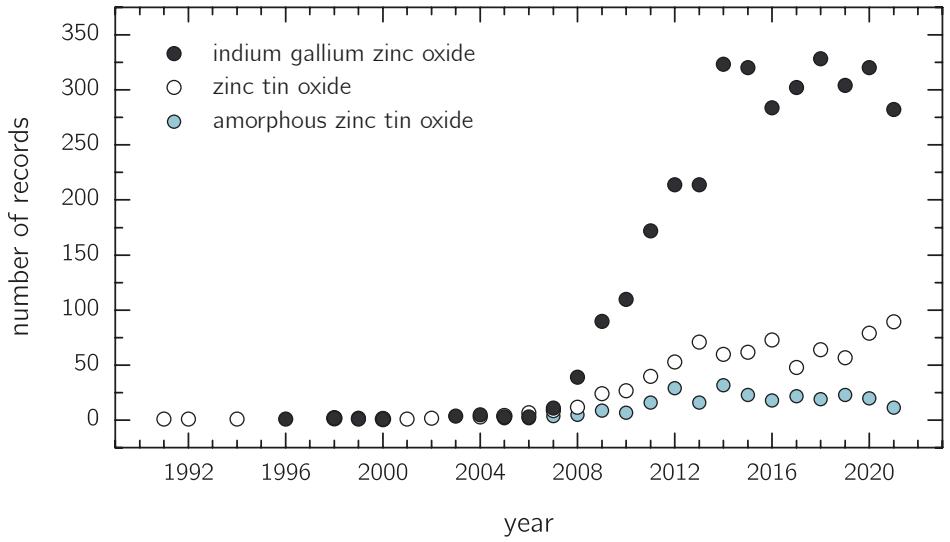


Figure 1: Comparison between the annual number of publications referring to the topics of IGZO and ZTO from their first appearance up to the present, retrieved from the *Web of Science core collection* database and all accessible additionally subscribed resources [27]. Filled blue circles represent the annual number of listed records specifically related to material properties and devices based on amorphous ZTO, since the vast majority of otherwise published data involve predominantly crystalline or extrinsically doped thin films and nanostructures.

response, IGZO related research once again continued to further intensify, given by the steep increase of the total number of annual records in Fig. 1 by the end of 2013.

The main drawback of IGZO is based on the fact that gallium and especially indium are scarce and thus expensive elements with rather high criticality [25,26]. Ideally, next-generation AOS based technology should be targeted toward indium-free and gallium-free compounds, providing at least comparable performance to amorphous IGZO. There has already been quite some effort to substitute IGZO by material systems containing only naturally earth-abundant elements. An appropriate and promising, yet technologically far less mature semiconductor is the transparent AOS zinc tin oxide (ZTO). Both zinc and tin are abundant, inexpensive and non-toxic elements with a strong background in oxide semiconductor related research [28]. ZTO based field-effect transistors are reported to exhibit a field-effect mobility of more than $20\,\mathrm{cm^2V^{-1}s^{-1}}$ [29,30] and have further been demonstrated to be capable of driving OLED based pixels [31–33]. According to the vast majority of previous studies, however, devices so far require amorphous ZTO thin films to be either directly deposition at elevated temperatures or at least to be annealed at 300°C to yield proper device functionality.

Within the scope of this thesis, recent development and optimization progress of amorphous ZTO is advanced toward new routes in terms of implementing novel device technologies while limiting the deposition process to room temperature in order to maintain compatibility with flexible organic substrates and common preparation techniques such as photolithography. Starting with the most fundamental device building blocks, ZTO is investigated as optically transparent active channel material within various types of field-effect transistors, including metal-semiconductor field-effect tran-

sistors (MESFETs), junction field-effect transistors based on *pn* heterodiodes as well as metal-insulator-semiconductor field-effect transistors. Aside from comparing the overall device functionality, both the long-term performance stability and the stability under bias is discussed. On the basis of previously reported simple inverters, the Schottky diode field-effect transistor logic approach is adapted in order to investigate the suitability of amorphous ZTO in more complex, cascaded unipolar digital integrated circuits. Ring oscillators are demonstrated accordingly, giving further insights into the dynamic properties of ZTO based field-effect transistors. Eventually, amorphous ZTO thin films are prepared on flexible polyimide substrates to determine the elastic and electrical properties while being subjected to excessive external stress induced by mechanical bending. Subsequently, the strain dependence of characteristic MESFET properties is investigated with regard to the performance stability to conclude whether amorphous ZTO is suited for flexible electronic applications.

II

General background

1 Amorphous oxide semiconductors

Within the last few decades, oxide semiconductors have regained considerable interest attributed to their unique combination of optical transparency in the visible spectral range and tunable electrical conductivity. Among the most intensively researched materials are ZnO and related (Mg,Cd,Zn)O compounds, SnO_2, Ga_2O_3 as well as the $(In,Ga,Al)_2O_3$ sesquioxide alloy systems [34–37]. Due to the strong ionicity of metal oxides given by the electrostatic interaction of constituent oppositely charged ions, charge transfer between metal and oxygen atoms causes the outer s states of metal cations to be empty and the outer p states of oxygen anions to be filled. In the ionic bonding configuration, the exchange of charges then induces a Madelung potential which in turn stabilizes the electronic structure and separates the metal and oxygen ion orbitals by energetically raising the electronic levels derived from cations and lowering the electronic levels derived from anions [38]. Consequently, the conduction band minimum of most metal oxides is predominantly formed by unoccupied spherical metal s orbitals, while the valence band maximum is composed of filled oxygen 2p orbitals, as illustrated in Fig. 1.1 (a). Since s orbitals of heavy metals have a large spatial spread and thus are highly dispersive while oxygen 2p orbitals are rather localized, oxide semiconductors typically feature small effective masses for electrons compared to holes.

It was not until 1996 that amorphous oxide semiconductors (AOSs) have been considered a viable approach toward the development of future transparent electronics [5,6]. Back then, AOSs were already expected to maintain a high charge carrier mobility comparable to those of corresponding crystalline materials in spite of being amorphous. Assuming an amorphous oxide containing heavy cations, the spatial spread of associated vacant metal ns orbitals is then large compared to the inter-cation distance, causing the electron wave functions of neighboring cations to directly overlap. Since s orbitals are spherically isotropic, the mutual overlap is insensitive to angular disorder and only weakly affected by local variations of the bond length, as schematically depicted in Fig. 1.1 (b), causing electrons to remain at least partly delocalized and thus

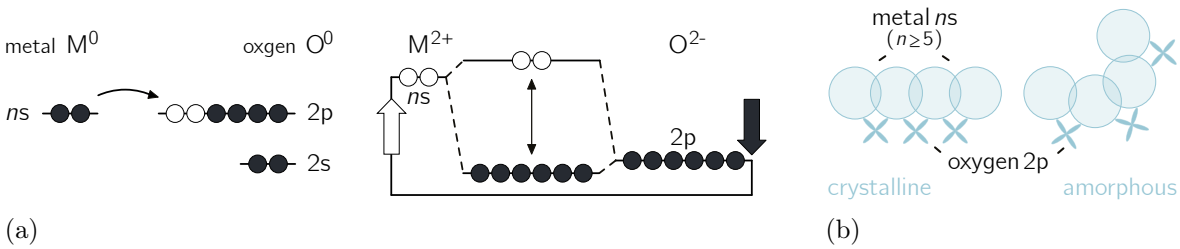


Figure 1.1: (a) Band gap formation mechanism in metal oxides due to separation of ion orbitals induced by charge exchange between metal cations and oxygen anions. (b) Overlap of neighboring spherical s orbitals in crystalline and amorphous oxide semiconductors comprising heavy post-transition metal cations associated with a principal quantum number of $n \geq 5$. Adapted from Ref. [17].

to yield a small effective mass. Notably, the spatial extent of the s orbital is primarily determined by the principal quantum number n and altered by the charge state of the cation [39]. Accordingly, heavy post-transition metal cations with an electron configuration of $(n-1)\mathrm{d}^{10}n\mathrm{s}^0$ and $n \geq 5$ such as In^{3+} and Sn^{2+} are effective when it comes to forming a wide-spread conduction band minimum with large band dispersion. Often, AOSs feature multicationic species with varying electronegativity and different ion radii in order to further improve the stability of the amorphous phase due to the suppression of crystallization and to upward shift the crystallization temperature, giving access to a broader temperature range regarding thin-film deposition and processing. By contrast, such expectations of a preservable high charge carrier mobility in ionic AOSs are distinctively different from those in conventional covalently bound semiconductors. In, for instance, silicon, the conduction band minimum and the valence band maximum are formed by bonding and antibonding states of sp^3 hybridized orbitals with strong spatial directivity. Consequently, vacant orbitals of neighboring atoms in covalent semiconductors are highly sensitive to variations in both the bond angle and length [40].

Hall effect sign anomaly in amorphous semiconductors

In strongly disordered materials, the Hall coefficient might exhibit a sign anomaly, i.e. having a positive sign for electrons or a negative sign for holes [41–44]. Such phenomena are typically observable for covalently bound amorphous semiconductors due to their short mean free path being usually below the bond length [45]. Ionic amorphous semiconductors, however, feature a much larger mean free path compared to the bond length, since the conduction band minimum is predominantly shaped by s orbitals [46–48]. Consequently, electrons are subjected to only weak disorder and less likely to form deep localized states.

1.1 Zinc tin oxide

Zinc tin oxide (ZTO) is a ternary metal oxide compound described by the stoichiometric configuration $(\mathrm{ZnO})_x(\mathrm{SnO_2})_{1-x}$ for $0 < x < 1$. Depending on the growth conditions, ZTO typically crystallizes either in the thermally metastable trigonal ilmenite-like and orthorhombic perovskite-like zinc stannate structure $\mathrm{ZnSnO_3}$ with a zinc-to-tin cation composition ratio of 1:1 or in form of cubic spinel-like $\mathrm{Zn_2SnO_4}$ with a cation composition ratio of 2:1 [49–53]. According to previous studies, ZTO starts to crystallize at temperatures around 400°C, while the phase transition from $\mathrm{ZnSnO_3}$ to $\mathrm{Zn_2SnO_4}$ occurs at approximately 600°C [54–57]. Thin films fabricated at significantly lower temperatures typically turn out amorphous for a sufficiently high tin content [58]. Often, ZTO is claimed to remain amorphous even when thin films have been annealed far beyond 450°C. The use of conventional probing techniques such as X-ray diffraction, however, is typically limited for amorphous thin films, combining both a reduced scattering volume and the lack of long-range order [59]. Consequently, poor crystalline quality or the formation of nanocrystalline features of ZTO thin films grown at elevated temperatures might remain undetected.

Several values for the optical band gap have been reported for crystalline ZTO, ranging from 3.05 eV up to 3.9 eV and certainly depending on the structure, the stoichiometry as well as the carrier concentration under consideration of the pronounced Burstein-Moss shift observed for degenerate Zn_2SnO_4 thin films [60–62]. Purely amorphous ZTO, on the other hand, usually exhibits a broadening of the absorption edge, which is most likely associated with Urbach tail absorption due to structural disorder related subgap states [63,64].

Numerous industrially relevant fabrication methods have turned out to be suitable for the preparation of amorphous ZTO thin films, including physical and chemical vapor deposition techniques such as magnetron sputtering from either metallic or ceramic targets [64–68], pulsed laser deposition [69–72], atomic layer deposition [73–76] and chemical vapor deposition [77,78] as well as solution based synthesis [79,80] by inkjet printing [81], spin coating [82–86] or solution combustion [87]. Aside from the actual deposition process and typical growth parameters, the thin-film properties are ultimately affected by the resulting composition of the ternary compound. Accordingly, modifying the stoichiometry of ZTO in terms of controlling the amount of zinc and tin incorporation into the thin film has has been demonstrated to facilitate the systematic tuning of its electrical, optical, morphological and structural properties by various fabrication techniques such as sputtering [88–92], pulsed laser deposition [55,93] and solution processing [94–97]. Tin acts as mediator to suppress the formation of crystalline phases in ZTO grown at moderate temperatures, since pure ZnO typically turns out polycrystalline [58]. Further, the amount of tin affects the electron affinity of ZTO, ranging from 4.05 eV to 4.25 eV [99]. Fig. 1.2 exemplarily highlights the clear trend of the conductivity and the absorption behavior observed for a variation of the cation ratio of a ZTO thin film fabricated at room temperature. The compositional gradient has been obtained by pulsed laser deposition using a continuous composition spread approach [100]. A zinc-rich and tin-poor composition ratio contributes to a shift of the absorption edge toward higher photon energies, whereas tin-richer ZTO exhibits a distinct increase in conductivity. Higher amounts of undercoordinated Sn^{4+} ions are assumed to favor the overlap of associated vacant s orbitals, while simultaneously creating

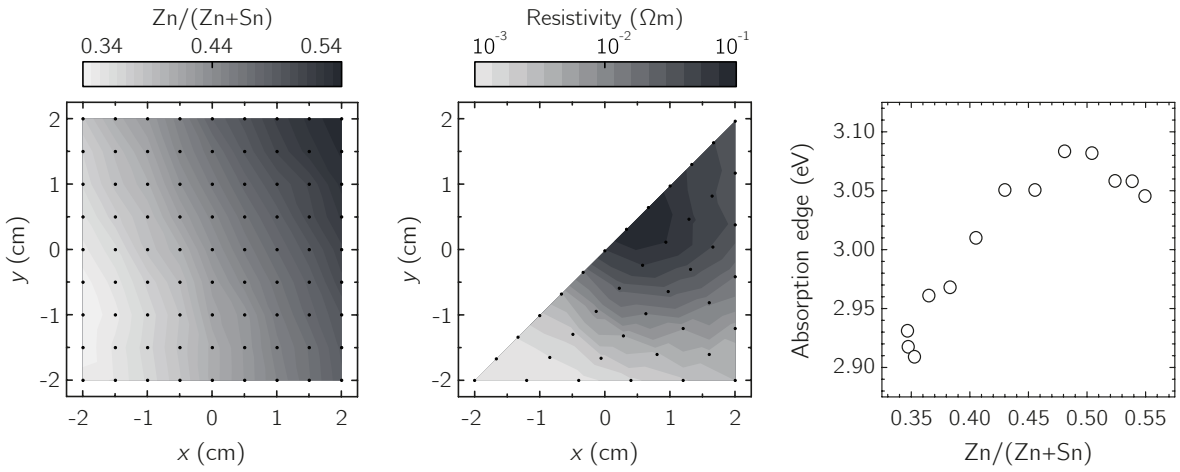


Figure 1.2: Grayscale representation of the spatial composition of a ZTO thin film determined by 81 EDX scans as well as an associated resistivity map and the absorption edge shift, both depicted for a zinc cation content variation between 34 % and 54 %. Based on data from Ref. [98].

deep defects levels within the band gap, causing a shift of the absorption edge toward lower photon energies. In the scope of the associated comprehensive study, multiple compositional gradients have been investigated, covering a total zinc content range from 8 % up to 78 % Zn/(Zn+Sn) [98]. Both the absorption edge and the resistivity increase considerably from 1.8 eV to 3.1 eV and $10^{-5}\,\Omega$m to $10^{3}\,\Omega$m upon incorporating more zinc into the thin film, respectively.

Similar to most amorphous oxide semiconductors, oxygen-poor growth promotes intrinsic doping and consequently accounts for the high conductivity observed in amorphous ZTO due to undercoordinated metal cations. Coordination defects in terms of undercoordinated metal cations typically create localized subgap defects that, when ionized, can form shallow donor states [10,101]. Consequently, the charge carrier density can be effectively tuned by controlling the rate of oxygen incorporation during thin-film deposition for a given cation composition ratio. Especially the formation of rectifying junctions has been demonstrated to be profoundly affected by the presence of oxygen at the interface [102–104].

The vast majority of previously reported electronic devices are restricted to the integration of amorphous ZTO as active channel material in metal-insulator-semiconductor field effect transistors (MISFETs) and usually rely on elevated processing temperatures during fabrication of at least 300°C in order to ensure proper functionality. First demonstrations regarding the implementation of amorphous ZTO as active channel material in transistors date back to 2005 [29]. Since then, numerous studies have followed with a focus on MISFETs containing amorphous ZTO grown by various deposition techniques [31,32,105–111] as well as associated integrated circuits [112–125]. Meanwhile, the metal-semiconductor field-effect transistor (MESFET) technology has been adapted for amorphous ZTO as an alternative approach to MISFETs, offering ease of fabrication and the device to operate at significantly lower power. MESFETs based on amorphous ZTO were initially demonstrated in 2017 and have soon after been realized by sputtering at room temperature without relying on any form of additional annealing treatment for the very first time [77,126]. Accordingly, being able to process ZTO based devices entirely at room temperature paved the way for applying common photolithographic patterning techniques involving thermally unstable resists, especially since ZTO already exhibits improved chemically stability in acidic and basic solutions compared to pure ZnO as well as a higher thermal stability in hydrogen environment than SnO_2 [89,127].

2 Flexible substrates

Nowadays, a wide variety of flexible substrate materials, including polymers, thinned glass and even paper, are being considered for applications in conformable electronics [128,129]. Apart from the device performance and bendability, manufacturing processes in particular set demanding requirements regarding the processability and properties of flexible substrates, such as stability, thickness and morphology. Paper represents a low-cost and disposable option, however, its high surface roughness in the order of several microns impedes the patterning of microelectronic structures to a certain extent. Flexible glass, thinned down to $\leq 50\,\mu m$, on the other hand, offers high processability but lacks mechanical stability due to its brittle nature that can only sustain small strains [130]. Consequently, polymers remain the most common choice as flexible substrate material, combining a high transparency with reasonable mechanical stability, light weight and a comparatively low surface roughness, as exemplified in Table 2.1. Many polymers, however, suffer from a poor solvent resistance as well as low glass transition temperatures around 150°C, limiting the maximum possible processing temperature and thus the amount of applicable deposition methods and materials eligible for device fabrication [131–133].

Polyimide represents one of the few exceptions with a glass transition temperature exceeding 350°C, providing high thermal resistance while maintaining mechanical stability as well as sufficient chemical resistance against common organic solvents and solutions involved in lithographic patterning procedures [134]. A drawback of conventional polyimide remains its deep yellowish appearance due to a poor optical transmittance between 30 % and 60 % between 400 nm and 700 nm [135]. However, among novel high temperature resistant polymers, considerable progress has been achieved regarding the synthesis of transparent, so-called colorless polyimide films, exhibiting a mean optical transmittance as high as 89 % in the visible spectral range [136].

Table 2.1: Comparison of various substrates commonly used for flexible electronic devices. Some listed values are only illustrative and might differ considerably for the same material depending on the substrate preparation technique.

Substrate material	Max. process temperature (°C)	Coeff. of therm. expansion (ppm/K)	Mean transmittance (400 nm - 700 nm) (%)	Surface roughness (nm)	Ref.
Polyimide (PI)	360	17 - 40	30 - 89	< 2	[130,135–137]
Polyethylene terephthalate (PET)	80	15 - 40	> 85	< 4	[135,138]
Polyethylene naphthalate (PEN)	150	13 - 20	> 85	< 2	[130,135–137]
Polydimethylsiloxane (PDMS)	150	> 300	> 90	< 1	[133,139]
Polyethersulfone (PES)	223	54 - 65	90	< 2	[135,140]
Polycarbonate (PC)	150	60 - 70	> 90	<2	[137,141]
Thinned glass	< 700	3	90	< 0.5	[130]
Paper	< 150	2 - 16	< 40	440 - 10^4	[142,143]

3 Device building blocks

3.1 Metal-semiconductor contacts

Close contact between semiconductors and metals does not necessarily result in an ohmic current-voltage relationship. Instead, a metal-semiconductor junction might exhibit rectifying properties depending on both the metal work function as well as the doping level of the semiconductor. Earliest observations and systematic investigations of such a nonlinear current-voltage behavior already date back to 1875 [144]. A first model considering the actual formation of a potential barrier at the contact interface has been developed by SCHOTTKY in 1938, giving the rectifying metal-semiconductor junction its today's most common designation Schottky contact [145,146]. Basic derivations and assumptions introduced in the following section briefly outline the descriptions provided in [147–149].

In general, metals and semiconductors differ in the position of their Fermi energies with respect to the vacuum level, given by the work functions $q\phi_{\mathrm{M}} > 0$ and $q\phi_{\mathrm{S}} > 0$, respectively [150]. Fig. 3.1 schematically illustrates the band alignment for the case of a metal spatially separated from an n-type semiconductor with $-e\chi_{\mathrm{S}}$ denoting the electron affinity, determined by the energetic distance between conduction band minimum and vacuum level, and $\phi_{\mathrm{n}} < 0$ being the potential difference between the Fermi level and the conduction band. Thus, the position of the Fermi level is given by

$$E_{\mathrm{F}} = E_{\mathrm{vac}} + e(\phi_{\mathrm{n}} + \chi_{\mathrm{S}}). \tag{3.1.1}$$

According to the Schottky-Mott model[1], a Schottky contact between a metal and an n-type semiconductor is formed if $|\phi_{\mathrm{M}}| > |\chi_{\mathrm{S}}|$ applies [146,152]. As soon as the metal and the semiconductor are brought in close contact, electrons within the conduction band of the semiconductor will occupy energetically more favorable states in the metal until the Fermi levels align, provided that the system is in a state of thermodynamic equilibrium. Consequently, space-charge regions with opposite signs form in the vicinity of the contact interface, whereas the equilibrium conditions in the bulk far off the junction prevail [153]. In order to maintain charge neutrality, the negative surface charge of the metal is compensated by the positive charge from the remaining ionized donor states in the semiconductor. Due to the high electron density in the metal conduction band, the position of the Fermi level does not change considerably upon charge exchange between metal and semiconductor, causing the space-charge region to predominantly extend into the semiconductor across the width w. Charge transport occurs until the diffusion current and the electric field induced drift current compensate. According to the energy band diagram of the Schottky contact depicted in Fig. 3.1, the bands on the semiconductor side bend by means of the voltage drop across the junction, given

[1] Considering an ideal contact, i.e. surface states shall be neglected [151].

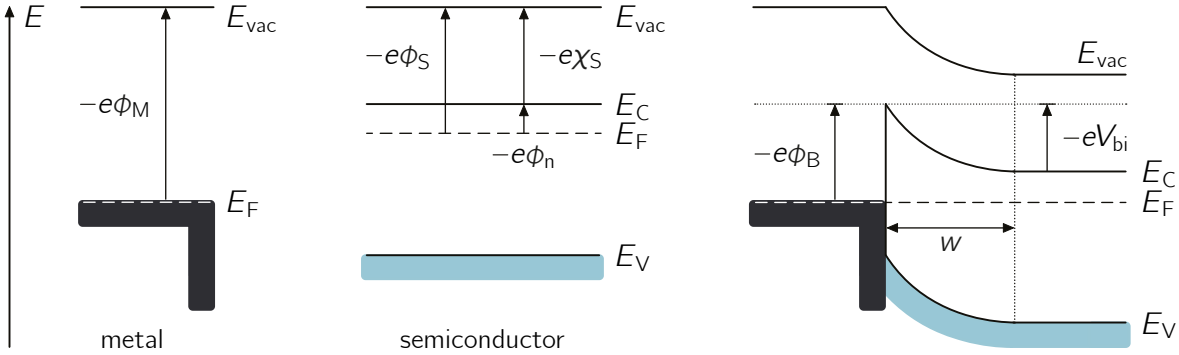


Figure 3.1: Schematic energy band diagrams of a metal and an n-type semiconductor both separated as well as in close contact, provided that $|\phi_\mathrm{M}| > |\chi_\mathrm{S}|$.

by the built-in potential $V_\mathrm{bi} = \phi_\mathrm{M} - \chi_\mathrm{S} - \phi_\mathrm{n}$. Thus, electrons in the semiconductor have to overcome a potential barrier of height $\phi_\mathrm{B} = \phi_\mathrm{M} - \chi_\mathrm{S} = V_\mathrm{bi} - \phi_\mathrm{n}$ to reach the metal surface, usually referred to as Schottky barrier.

Within the so-called abrupt approximation, the potential distribution of the junction perpendicular to the contact interface plane is described by the one-dimensional Poisson equation

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = -\frac{1}{\varepsilon_0\varepsilon_\mathrm{r}}\varrho(x) \tag{3.1.2}$$

with ϱ denoting the space-charge density and $\varepsilon_0\varepsilon_\mathrm{r}$ being the vacuum permittivity and the relative permittivity, respectively. In addition to abrupt boundaries of the space-charge region with the conditions $\phi(0) = -V_\mathrm{bi}$ and $\phi(w) = 0$, the semiconductor is assumed to have uniform doping and all donors in the depletion region are expected to be ionized, resulting in a space-charge density of $\varrho(0 \le x \le w) = eN_\mathrm{D}$. Outside of the space-charge region, the semiconductor is neutral, i.e. $\varrho(x > w) = 0$ and $\partial_x\phi(x > w) = 0$. Solving Eq. (3.1.2) yields a spatial electrostatic potential distribution with quadratic dependence on the position x as well as the associated equilibrium space-charge region width

$$w = \sqrt{\frac{2\varepsilon_0\varepsilon_\mathrm{r}}{eN_\mathrm{D}}\left(V_\mathrm{bi} - \frac{k_\mathrm{B}T}{e}\right)}. \tag{3.1.3}$$

A lowering of the built-in voltage by $k_\mathrm{B}Te^{-1}$ is taken into account by the Boltzmann approximation in terms of the thermal distribution related tail of the majority carriers in the space-charge region [147]. Applying an additional external voltage to the metal with regard to the semiconductor, such that $\phi(0) = -V_\mathrm{bi} + V$, causes a shift of the quasi Fermi level by eV. Consequently, reverse biasing of the junction contributes to further band bending, whereas forward biasing reduces the built-in potential until eventually the flat band condition $V = V_\mathrm{bi}$ applies and thus zero net space-charge remains in this region. Since the voltage dependence of w determines the capacitive behavior of the junction, the space-charge as well as the capacitance per unit area can be derived using a simple parallel-plate capacitor model, yielding $Q/A_0 = eN_\mathrm{D}w$ and $C/A_0 = \varepsilon_0\varepsilon_\mathrm{r}/w$, respectively.

As electrons approach the metal-semiconductor interface, the barrier height is affected by the potential associated with image charges build up in the metal [154]. An

electron facing the metal equipotential surface at position x in the semiconductor induces a charge with opposite sign at position $-x$ in the metal. The image charge exerts an attractive force on the electron, resulting in a voltage-dependent image-force-induced lowering of the barrier height, also referred to as Schottky effect. Further, nonidealities such as surface states have so far been neglected within the applied Schottky-Mott model. Especially covalent semiconductors tend to exhibit surface states distributed around mid-gap, usually caused by unsaturated bonds [155]. Donors of an n-type semiconductor, located close to the conduction band edge, will then donate electrons to deeper, i.e. energetically more favorable, unoccupied surface states rather than to the conduction band. A sufficiently high density of surface states might then already result in a band bending and thus the formation of a potential barrier in the vicinity of the semiconductor surface. Consequently, the Fermi level is pinned and does not change considerably upon bringing semiconductor and metal into close contact, regardless of ϕ_{M}. The dependence of the Schottky barrier height on the metal work function is given by the surface index $s = \partial\phi_{\mathrm{B}}/\partial\phi_{\mathrm{M}}$ with $0 \leq s \leq 1$, where $s = 0$ and $s = 1$ are defined as the Bardeen limit and the Schottky limit, respectively [156]. Increasing the ionicity of the semiconductor, i.e. larger electronegativity difference between constituent species of compounds, has been demonstrated to yield surface indices approaching $s \approx 1$ [157,158].

Ohmic contacts

Ohmic behavior is generally distinguished by a linear current-voltage relationship and thus provides uniform electrical conduction in either direction between metal and semiconductor. Ideally, the specific contact resistance $\rho_{\mathrm{c}} = (\partial j/\partial V)^{-1}_{V=0}$ - given by the reciprocal of the derivative of the current density with respect to the voltage drop across the contact interface evaluated at zero bias - is sufficiently low such that the voltage drop over the contact is negligible compared to the voltage drop across the active region of the semiconductor [159]. Both a reduction of the barrier height by choosing metals with suitable work functions as well as excessive extrinsic or intrinsic doping of the semiconductor favor the formation of an ohmic junction. Depending on the extent of the resulting barrier narrowing, the latter may then render tunneling a dominant charge transport mechanism.

Current transport mechanisms

Charge carrier transport across a metal-semiconductor junction is dominated by majority carriers, i.e. electrons or holes in case of n-type or p-type semiconductors, respectively [147]. Depending on the condition of both the charge carriers and the Schottky barrier, current transport under forward bias can be described by various mechanisms [160]. Thermionic emission of hot electrons above the barrier is usually important in case of intermediately doped semiconductors ($N_{\mathrm{D}} \leq 10^{17}\,\mathrm{cm}^{-3}$) at moderate temperatures of about 300 K [148]. Quantum mechanical tunneling of electrons through the barrier becomes a dominant transport mechanism for sufficiently thin barriers, i.e. at high doping according to $w \propto N_{\mathrm{D}}^{-1/2}$. Further basic transport processes include recombination in the space-charge region, diffusion of electrons in the space-charge region and injection of holes from the metal that diffuse and recombine

in the neutral region of the semiconductor. Additional edge leakage currents induced by sufficiently high electric fields and contact quality dependent trap induced interface currents might have to be considered as well. In case of amorphous ZTO based Schottky barrier diodes, however, thermionic emission is usually assumed to be the dominant charge carrier transport mechanism and associated theoretical models have been demonstrated to be suitable for describing and fitting experimental data [72,103].

In order to overcome a potential barrier of height $-e\phi_{\mathrm{B}} \gg k_{\mathrm{B}}T$, electrons require a thermal energy of at least $e(V_{\mathrm{bi}} - V)$, provided that the flat band condition is not reached, i.e. $V_{\mathrm{bi}} > V$. Accordingly, the thermionic emission current density is then given by

$$j = j_{\mathrm{s}} \exp\left(\frac{eV}{\eta k_{\mathrm{B}}T}\right)\left[1 - \exp\left(-\frac{eV}{k_{\mathrm{B}}T}\right)\right], \tag{3.1.4}$$

with j_{s} describing the saturation current density

$$j_{\mathrm{s}} = A^{*}\frac{m_{\mathrm{eff}}}{m_0}T^2 \exp\left(-\frac{\phi_{\mathrm{B},0}}{k_{\mathrm{B}}T}\right), \tag{3.1.5}$$

i.e. the maximum current in reverse direction, and $\phi_{\mathrm{B},0}$ being the equilibrium barrier height in the absence of externally applied electric fields [161]. $A^{*} = 4\pi\, e\, m_0\, k_{\mathrm{B}}^2\, h^{-3}$ and m_{eff} denote the Richardson constant and the effective electron mass, respectively. The dimensionless parameter $\eta \geq 1$ is referred to as ideality factor and represents a measure for the voltage dependence of the barrier height determined by

$$\eta = 1 + \frac{1}{e}\frac{\partial \Phi_{\mathrm{B}}}{\partial V}. \tag{3.1.6}$$

Considering the image force lowering effect on the barrier height induced by electrons moving from the semiconductor into the metal, the ideality factor is determined by

$$\eta_{\mathrm{img}} = 1 + \frac{1}{4V_{\mathrm{bi}}}\left(\frac{e^3 N_{\mathrm{D}}}{8\pi^2 \varepsilon_0^3 \varepsilon_{\mathrm{r}}^3}\right)^{0.25}. \tag{3.1.7}$$

Typically, η_{img} takes values ranging from 1.01 to 1.03 depending on the net doping concentration. Since electrons moving from the metal into the semiconductor have been demonstrated to affect the voltage dependence of the barrier height and thus the ideality factor as well, Eq. (3.1.4) simplifies to

$$j = j_{\mathrm{s}}\left[\exp\left(\frac{eV}{\eta k_{\mathrm{B}}T}\right) - 1\right] \tag{3.1.8}$$

and holds true for $V > 3k_{\mathrm{B}}Te^{-1}$ [161].

Nonidealities observed in current-voltage characteristics

Barrier height inhomogeneity

So far, the potential barrier has been assumed to be laterally homogeneous across the metal-semiconductor junction. However, nonideal Schottky diodes may exhibit fluctu-

ations in the barrier height due to either interface defects, rough surfaces or doping inhomogeneities. The contact interface can then be considered a parallel connection of multiple diodes, each with a different barrier height [162,163]. Assuming a Gaussian barrier height distribution yields

$$P(\phi_\mathrm{B}) = \frac{1}{\sqrt{2\pi}\Sigma} \exp\left(-\frac{(\bar{\phi}_\mathrm{B} - \phi_\mathrm{B})^2}{2\Sigma^2}\right) \tag{3.1.9}$$

with $\bar{\phi}_\mathrm{B}$ being the mean barrier height and Σ denoting the standard deviation of the height distribution [164]. The resulting total current density

$$j = \int P(\phi_\mathrm{B}) j_\phi(\phi_\mathrm{B})\,\mathrm{d}\phi_\mathrm{B} \tag{3.1.10}$$

takes into account the individual currents for each barrier height according to the distribution function. Consequently, charge transport occurs preferably along conduction paths with barrier heights lower than the mean barrier height, yielding an effective barrier height $\phi_\mathrm{B}^\mathrm{eff} < \bar{\phi}_\mathrm{B}$ in the absence of an externally applied voltage of

$$\phi_\mathrm{B}^\mathrm{eff} = \bar{\phi}_{\mathrm{B},0} - \frac{\Sigma_0^2}{2k_\mathrm{B}T}. \tag{3.1.11}$$

Since the barrier properties depend on the temperature, the external voltage as well as image charge effects, the effective barrier height ultimately affects the ideality factor according to [164]

$$\eta = \left(1 - \frac{1}{e}\frac{\partial\phi_\mathrm{B}^\mathrm{eff}}{\partial V}\right)^{-1} = \left(1 - \frac{1}{e}\frac{\partial\bar{\phi}_\mathrm{B}}{\partial V} + \frac{1}{2k_\mathrm{B}T}\frac{1}{e}\frac{\partial\Sigma^2}{\partial V}\right)^{-1}. \tag{3.1.12}$$

For small η close to unity, the effective barrier height exhibits a linear dependence on the ideality factor and can then be extrapolated to obtain the homogeneous barrier height [165–167].

Series and parallel resistances

The bias V applied to the Schottky contact in preceding descriptions differs from the actual external voltage V_ext by already considering the voltage drop across the semiconductor and the metal. In the following, the internal resistance of both the metal and the semiconductor as well as the contact resistance of the junction contribute to the total series resistance R_s of the device. The corresponding voltage drop ΔV across R_s depends on the current flowing through the junction, yielding a bias of

$$V = V_\mathrm{ext} - \Delta V = V_\mathrm{ext} - IR_\mathrm{s}. \tag{3.1.13}$$

Again, according to the barrier height inhomogeneity model, individual current paths can then be associated with a parallel connection of multiple diodes, each with a fixed barrier height and a series resistance [168]. Parasitic nondepletable current paths that contribute to the total current due to, for instance, surface or grain boundary conduction are further considered by a parallel ohmic resistance R_p.

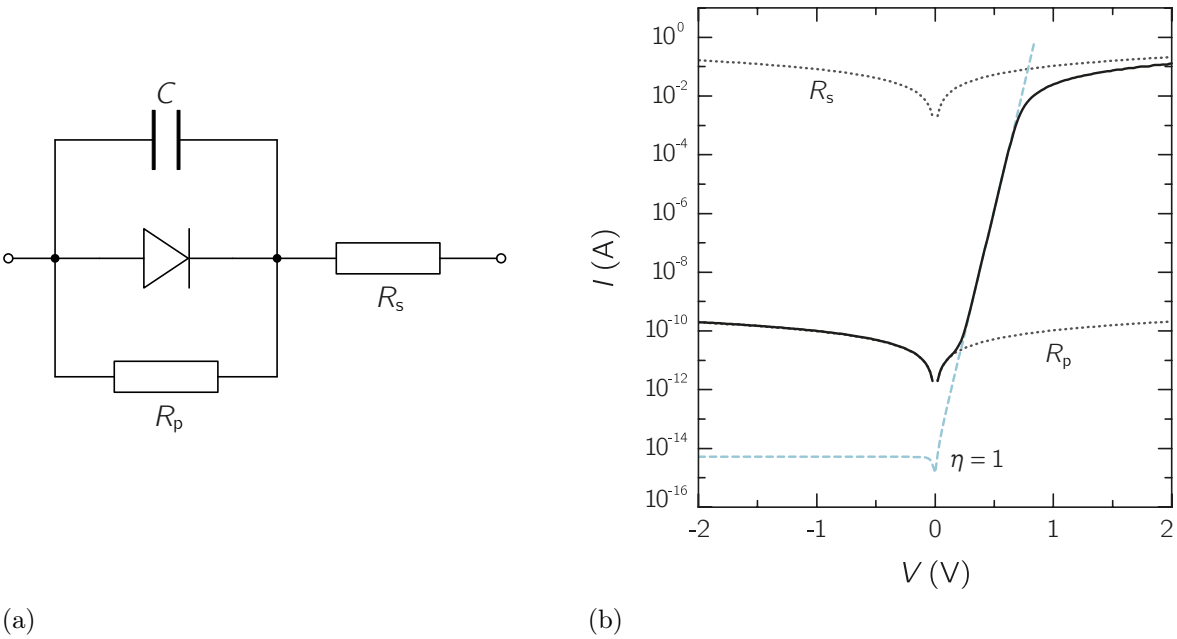
Real diodes

So far discussed junction nonidealities are schematically represented in the equivalent circuit diagram in Fig. 3.2 (a). An additional capacitance C connected in parallel to the ideal diode takes into account the space-charge region capacitance as well as any defect induced capacitances, responsible for charging and discharging processes during current-voltage measurements. Assuming that thermionic emission is the dominant charge transport mechanism, the current density $j = I/A_0$ in Eq. (3.1.8) can then be modified to

$$I = A_0 A^* \frac{m_{\mathrm{eff}}}{m_0} T^2 \exp\left(-\frac{\Phi_{\mathrm{B}}^{\mathrm{eff}}}{k_{\mathrm{B}} T}\right) \left[\exp\left(\frac{V_{\mathrm{ext}} - I R_{\mathrm{s}}}{\eta k_{\mathrm{B}} T}\right) - 1\right] + \frac{V_{\mathrm{ext}} - I R_{\mathrm{s}}}{R_{\mathrm{p}}} + I_{\mathrm{C}} \quad (3.1.14)$$

under consideration of the aforementioned nonidealities. Numerical solutions of the implicit equation Eq. (3.1.14) for characteristic diode parameters of $\eta = 1$, $\phi_{\mathrm{B}} = 1\,\mathrm{eV}$, $R_{\mathrm{s}} = 10\,\Omega$, $R_{\mathrm{p}} = 10^{10}\,\Omega$ a temperature of $T = 300\,\mathrm{K}$ and a contact area of $10^{-4}\,\mathrm{cm}^2$ are depicted in Fig. 3.2 (b). For amorphous ZTO, an effective mass of approximately $m_{\mathrm{eff}} = 0.3\,m_0$ has been estimated from experimental values for crystalline $ZnSnO_3$ thin films of $0.18\,m_0$ - $0.19\,m_0$ [169] and for Zn_2SnO_4 thin films of $0.23\,m_0$ - $0.26\,m_0$ [170] by assuming the effective mass to be slightly increased for amorphous thin films [62,171].

In case of reverse biasing, the current is clearly determined by the parallel resistance as well as the effective barrier height. A sufficiently low parallel resistance would consequently result in an ohmic characteristic. Forward biasing yields an exponential



(a) (b)

Figure 3.2: (a) Equivalent circuit diagram of a real diode including a series resistance R_{s}, a parallel resistance R_{p}, a capacitance C as well as the ideal diode. (b) Simulated current-voltage characteristic of a diode (solid line) according to Eq. (3.1.14) with $\eta = 1$, $\phi_{\mathrm{B}} = 1\,\mathrm{eV}$, $R_{\mathrm{s}} = 10\,\Omega$, $R_{\mathrm{p}} = 10^{10}\,\Omega$, $T = 300\,\mathrm{K}$, $m_{\mathrm{eff}} = 0.3\,m_0$ and a contact area of $10^{-4}\,\mathrm{cm}^2$. Additionally, the characteristics of R_{s} and R_{p} (dotted lines) as well as the ideal diode (dashed line), disregarding R_{s} and R_{p}, are depicted. Capacitive effects, considered by the charging current I_{C}, have been neglected.

behavior of the current for low voltages, whereas gradually increasing the voltage causes the current to transition into a linear dependence, limited by the series resistance. The exponential regime is affected by the ideality factor and the effective barrier height in terms of the slope and the horizontal shift along the voltage axis, respectively. Capacitive effects are considered by the charging current

$$I_{\mathrm{C}} = C\frac{\mathrm{d}V_{\mathrm{ext}}}{\mathrm{d}t} \tag{3.1.15}$$

in Eq. (3.1.14) and typically induce a shift of the zero-crossing of the characteristic. Since the integration time is kept fixed for every single measurement point during the voltage sweep, I_{C} is assumed to be constant due to $\mathrm{d}V/\,\mathrm{d}t = \mathrm{const}$.

3.2 Semiconductor heterojunctions

Obtaining a rectifying junction is, moreover, possible by establishing close contact between two suitable semiconductors with opposite charge carrier type. Different band gap energies and electron affinities then cause the formation of band discontinuities. Depending on the band alignment, *pn* heterojunctions are differentiated into either type-I heterostructures (straddling gap), type-II heterostructures (staggered gap) or type-III heterostructures (broken gap) [148]. Since the *n*-ZTO/*p*-NiO based devices investigated within the scope of this thesis exhibit a type-II configuration, the following descriptions are focusing on type-II heterojunctions.

As soon as both semiconductors are brought into contact, the concentration gradients of the associated majority carriers cause a diffusion current of electrons from the *n*- to the *p*-region and holes from the *p*- to the *n*-region in order for them to recombine. The stationary positive and negative ions induce an opposing electric field, resulting in the drift of the remaining free charge carriers until the Fermi levels on both sides align. Consequently, space-charge regions with opposite signs of width w_{n} and w_{p} form in the vicinity of the contact interface. Analogous to Eq. (3.1.3), the total space-charge region width $w = w_{\mathrm{n}} + w_{\mathrm{p}}$ is given by

$$w = \sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{r}}}{e}\left(\frac{N_{\mathrm{A}} + N_{\mathrm{D}}}{N_{\mathrm{A}}N_{\mathrm{D}}}\right)\left(V_{\mathrm{bi}} - V - \frac{2k_{\mathrm{B}}T}{e}\right)} \tag{3.2.1}$$

with N_{D} and N_{A} denoting the donor density in the *n*-type semiconductor and acceptor density in the *p*-type semiconductor, respectively [147]. According to $w_{\mathrm{n/p}} \propto (N_{\mathrm{D/A}})^{-0.5}$ the depletion zone will primarily extent further into the region of lower doping. Forward biasing the *pn* junction results in the continuous injection of majority carriers, i.e. electrons move from the *n*-contact into the *n*-region and holes move from the *p*-contact into the *p*-region. Electrons and holes then diffuse toward the contact interface, causing both carrier types to recombine due to the low hole and electron concentration on the *n*-side and *p*-side, respectively. Reverse biasing, on the other hand, accelerates electrons toward the *n*-contact and holes toward the *p*-contact and thus favors the expansion of the space-charge region.

3.3 Field-effect transistors

Field-effect transistors (FETs) comprise a wide variety of unipolar transistor types, all of which essentially operate according to the same physical principle and are thus typically distinguishable by either device geometry, doping or the material stacking order. Most commonly, however, the major FET types are subdivided into metal-insulator-semiconductor field-effect transistors (MISFETs), junction field-effect transistors (JFETs) and metal-semiconductor field-effect transistors (MESFETs). First basic concepts were initially proposed by LILIENFELD in 1925 and 1926 [172,173]. Due to persisting issues regarding impurities and surface effects, it was not until more than two decades later that the theoretical descriptions of a unipolar transistor have actually been implemented at the BELL LABS by BARDEEN and BRATTAIN [174]. Compared to bipolar devices, unipolar transistors are voltage-controlled and only majority carriers contribute to the current flow through the channel, offering faster switching dynamics, ease of fabrication as well as a broader range of suitable materials.

In its simplest form, a field-effect transistor consists of three terminals, generally referred to as source, gate and drain. Source and drain are separated by either an n-type or p-type semiconducting channel and form ohmic junctions. Current transport through the device is controlled by applying a voltage to the rectifying gate contact, which in turn modulates the electrical conductivity in the channel in terms of charge carrier accumulation and depletion. Ideally, the gate operates without power consumption. In reality, however, due to the gate capacitance a certain input power is required in order to switch the transistor, while the gate leakage current causes permanent power consumption [175]. The gate of MESFETs and JFETs consists of a Schottky diode and a pn heterodiode as described in Chapters 3.1 and 3.2, respectively, whereas MISFETs employ an insulator between metal gate contact and channel. Consequently, MISFETs exhibit a high dielectric breakdown strength and negligible gate leakage current while simultaneously drawing more input power and attaining limited switching speed due to charge carrier scattering at the insulator interface [176]. MESFETs and JFETs, on the other hand, typically reach much higher operation frequencies but usually suffer from significant gate leakage currents at large forward gate bias.

On behalf of using amorphous ZTO as channel material, the following assumptions are considered for an n-type[2] MESFET. JFETs can usually be described by the exact same formalism, provided that the gate material exhibits an essentially higher doping concentration with respect to the channel material, for instance by forming a p^+n heterojunction. At a source-drain voltage of $V_\mathrm{D} = 0\,\mathrm{V}$ and a source-gate voltage of $V_\mathrm{G} = 0\,\mathrm{V}$ with regard to the source terminal acting as common ground, the transistor is in equilibrium. The space-charge region width beneath the gate is then only determined by the built-in potential. Gradually increasing V_D causes electrons to move form source to drain through parts of the channel that are not yet depleted. Initially, the current starts to increase according to Ohm's law as illustrated by the linear region of the output characteristics in Fig. 3.3 (a). Continuously reverse biasing the gate-drain diode, however, results in the expansion of the space-charge region on the drain side of the channel. Assuming the gate length L to be large compared to the channel

[2]Derived equations can be adjusted for p-type channel FETs when charge, charge carrier density and doping density are exchanged accordingly

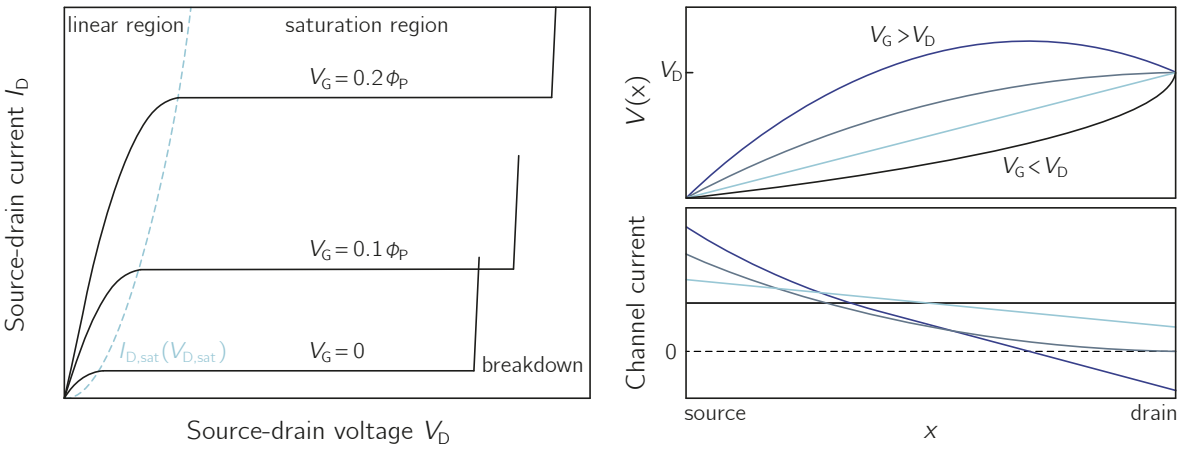


Figure 3.3: (a) Ideal output characteristics of an n-type depletion mode field-effect transistor based on [177]. (b) Influence of the gate voltage on the channel potential distribution $V(x)$ and the channel current, provided that $V_G > V_{bi} - \phi_P$ and $V_G > 0$. Adapted from Ref. [178].

thickness d and neglecting thermal effects, the width of the space-charge region at a certain position x between source and drain can be calculated by considering the abrupt approximation according to Eq. (3.1.3), yielding

$$w(x) = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_D}\left(V_{bi} - V_G + V(x)\right)}\,. \tag{3.3.1}$$

At the source end ($x = 0$) and the drain end ($x = L$) of the space-charge region, the total extent is then given by

$$w(0) = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_D}\left(V_{bi} - V_G\right)} \quad \text{and} \quad w(L) = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN_D}\left(V_{bi} - V_G + V_D\right)}\,. \tag{3.3.2}$$

Once the drain voltage approaches a certain drain saturation voltage $V_{D,sat}$, the channel is eventually pinched off by the space-charge region at the drain side, causing the drain current to transition from its linear regime into saturation, as indicated in Fig. 3.3 (a). The width of the space-charge region at drain then equals the channel width $d = w(L)$ for $V_{bi} - V_G + V_{D,sat} = \phi_P$ with ϕ_P denoting the pinch-off potential defined by

$$\phi_P = \frac{ed^2 N_D}{2\varepsilon_0\varepsilon_r}\,. \tag{3.3.3}$$

The pinch-off potential corresponds to the sum of all built-in and external voltages and thus denotes the potential difference between the top of the barrier and the channel-substrate interface, provided that the channel is fully depleted along its total width. Increasing V_D beyond $V_{D,sat}$ thus causes the drain current $I_D\,(V_D > V_{D,sat}) = I_{D,sat}$ to remain at its saturation level. Since no free charge carriers are left at the drain side, $V_D > V_{D,sat}$ does neither affect the potential distribution beneath the gate nor the spatial extent space-charge region. Excessive increase of the source-drain voltage, however, ultimately results in an avalanche breakdown of the device as illustrated in Fig. 3.3 (a).

Impact ionization then promotes the generation of electron-hole pairs, causing the drain current to increase rapidly.

In order to deplete the entire channel, the threshold voltage

$$V_{\mathrm{T}} = V_{\mathrm{bi}} - \phi_{\mathrm{P}} \tag{3.3.4}$$

has to be applied to the gate with respect to source. Depending on the extent of the space-charge region at $V_{\mathrm{G}} = 0\,\mathrm{V}$ and whether or not the channel is then able to conduct current between source and drain, the transistor operates either in depletion mode or enhancement mode, respectively. Further decrease of the gate voltage beyond $V_{\mathrm{G}} \leq V_{\mathrm{bi}} - \phi_{\mathrm{P}}$ causes the device to remain in the off-regime regardless of the applied source-drain voltage, as depicted in Fig. 3.4.

The current-voltage relationship of the aforementioned operation regimes can be derived by integrating the conductance of the channel along its lateral direction parallel to the substrate [177]. For the following derivations, current conservation along the channel is assumed, implying a negligible gate leakage current compared to the source-drain current [148]. Considering the drift current density for the neutral part of the channel

$$j_x = -e\mu N_{\mathrm{D}} \mathcal{E}_x = e\mu N_{\mathrm{D}} \frac{\partial V}{\partial x} \tag{3.3.5}$$

the channel current yields

$$I_{\mathrm{D}} = e\mu N_{\mathrm{D}} \frac{\partial V}{\partial x} W \left[d - w(x) \right]. \tag{3.3.6}$$

Provided that $V_{\mathrm{bi}} - V_{\mathrm{G}} + V_{\mathrm{D}} < \phi_{\mathrm{P}}$, the drain current is given by

$$I_{\mathrm{D}} = I_{\mathrm{P}} \left[\frac{3V_{\mathrm{D}}}{\phi_{\mathrm{P}}} - 2 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{G}} + V_{\mathrm{D}}}{\phi_{\mathrm{P}}} \right)^{3/2} + 2 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{G}}}{\phi_{\mathrm{P}}} \right)^{3/2} \right]. \tag{3.3.7}$$

The saturation current

$$I_{\mathrm{P}} = \frac{W}{L} \frac{e^2 \mu d^3 N_{\mathrm{D}}^2}{6\varepsilon_0 \varepsilon_{\mathrm{r}}} \tag{3.3.8}$$

is a constant and depends on material properties as well as the device geometry with W/L denoting the gate width-to-length ratio [147]. Once the channel is pinched off at the substrate interface by the space-charge region for $V_{\mathrm{bi}} - V_{\mathrm{G}} + V_{\mathrm{D,sat}} = \phi_{\mathrm{P}}$, the channel current becomes independent of V_{D} and saturates to

$$I_{\mathrm{D,sat}} = I_{\mathrm{P}} \left[1 - 3 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{G}}}{\phi_{\mathrm{P}}} \right) + 2 \left(\frac{V_{\mathrm{bi}} - V_{\mathrm{G}}}{\phi_{\mathrm{P}}} \right)^{3/2} \right]. \tag{3.3.9}$$

Taylor expansion of Eq. (3.3.9) around $V_{\mathrm{G}} = V_{\mathrm{T}}$ yields

$$I_{\mathrm{D,sat}} \approx \frac{3I_{\mathrm{P}}}{4\phi_{\mathrm{P}}} (V_{\mathrm{G}} - V_{\mathrm{T}})^2 \tag{3.3.10}$$

and facilitates the estimation of V_T by extrapolation of the linear relation obtained for $\sqrt{I_{D,sat}}$ in dependence on V_G.

As soon as V_G exceeds V_{bi}, the flat band condition applies and the space-charge region at the source vanishes, as illustrated in Fig. 3.4. Consequently, ohmic conduction occurs in the neutral part of the channel from source to the location in the channel where a potential of $V(x) = V_G - V_{bi}$ is reached. The rest of the channel can be treated as a transistor with reduced gate length, gate voltage and source-drain voltage due to the potential drop across the additional ohmic region [178]. Since the previously defined boundaries of the space-charge region are shifted, Eq. (3.3.7) and Eq. (3.3.9) are not defined anymore. Combining the current transport through both regions by assuming current conservation, the source-drain current can be described by

$$I_D = I_P \left[3\frac{V_{bi} - V_G + V_D}{\phi_P} - 2\left(\frac{V_{bi} - V_G + V_D}{\phi_P}\right)^{3/2} \right] + \frac{e\mu d N_D W}{L}(V_G - V_{bi}) \quad (3.3.11)$$

.

In saturation, i.e. $V_{bi} - V_G + V_D = \phi_P$, Eq. (3.3.11) simplifies to

$$I_{D,sat} = I_P + \frac{e\mu d N_D W}{L}(V_G - V_{bi}). \quad (3.3.12)$$

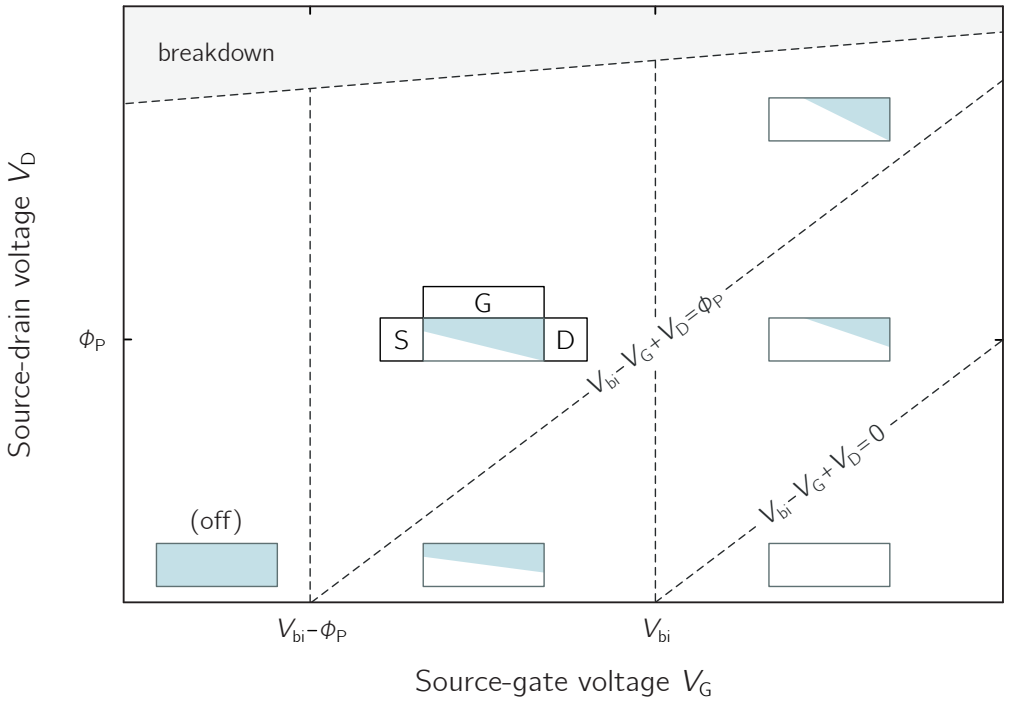


Figure 3.4: Extent of the space-charge region for different operation states of a field-effect transistor in dependence on both the source-gate voltage V_G and the source-drain voltage V_D. $\phi_P = V_{bi} - V_G + V_D$ and $\phi_P = V_{bi} - V_G$ denote the pinch-off condition at drain and source, respectively. The level of ϕ_P is determined by the intercept of the flat band condition $V_G = V_{bi}$ and the pinch-off condition at drain. Adapted from Ref. [178].

Once the space-charge region vanishes completely, the channel can be treated as a simple ohmic conductor, yielding

$$I_\mathrm{D} = \frac{e\mu d N_\mathrm{D} W}{L} V_\mathrm{D} . \tag{3.3.13}$$

The forward transconductance g_m of the transistor in the linear regime is given by

$$g_\mathrm{m} = \left.\frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}}\right|_{V_\mathrm{D}=\mathrm{const.}} = g_\mathrm{max}\left[\left(\frac{V_\mathrm{bi}-V_\mathrm{G}}{\phi_\mathrm{P}}\right)^{1/2} - \left(\frac{V_\mathrm{bi}-V_\mathrm{G}+V_\mathrm{D}}{\phi_\mathrm{P}}\right)^{1/2}\right] \tag{3.3.14}$$

with

$$g_\mathrm{max} = \frac{3I_\mathrm{P}}{\phi_\mathrm{P}} = \frac{e\mu d N_\mathrm{D} W}{L} \tag{3.3.15}$$

denoting the theoretical maximum of the transconductance. From Eq. (3.3.15), the field-effect mobility can be determined for given geometrical parameters if N_D is known. Often, the theoretical maximum of the forward transconductance is not reached due the considerable impact of gate leakage current at positive V_G, causing the field-effect mobility to underestimate the actual charge carrier mobility. As V_G approaches V_D under typical MESFET operation conditions, the contribution of the gate leakage current to the channel current becomes comparable to I_D. The potential distribution in the channel thus starts to get more flat near drain and I_D is reduced accordingly, as illustrated in Fig. 3.3 (b). Increasing V_G beyond V_D, however, induces a potential barrier in the channel that prevents current from further flowing between source and drain until eventually the current at the drain reverses and the gate leakage current dominates the overall channel current.

So far, the source-drain current was assumed to be zero at $V_\mathrm{G} \leq V_\mathrm{T}$ as a result of the channel being fully depleted of charge carriers. However, since the electron quasi Fermi level E_Fn extends into the space-charge region at both contacts, a nonzero charge carrier density of

$$n \approx N_\mathrm{C} \exp\left(\frac{E_\mathrm{Fn}-E_\mathrm{C}}{k_\mathrm{B}T}\right) \tag{3.3.16}$$

remains in the channel according to the Boltzmann approximation with N_C denoting the conduction band edge density of states. Due to the potential difference between source and drain under typical operation conditions, the quasi Fermi level at source is closer to E_C, causing a gradient of the free charge carrier density in the space-charge region [178]. The diffusion of associated charge carriers through the space-charge region yields the subthreshold current

$$I_\mathrm{T} = \gamma \frac{\varepsilon_0 \varepsilon_\mathrm{r} W}{d L_\mathrm{eff}} \frac{k_\mathrm{B}T}{e} D_\mathrm{n} \exp\left[\frac{e}{k_\mathrm{B}T}(V_\mathrm{G}-V_\mathrm{T})\right]\left[1-\exp\left(-\frac{e}{k_\mathrm{B}T}V_\mathrm{D}\right)\right] \tag{3.3.17}$$

where D_n is the electron diffusion coefficient and $1 \leq \gamma \leq 2$ denotes a constant describing the doping profile uniformity of the channel [179]. $L_\mathrm{eff} < L$ refers to an effective reduced gate length considering edge effects close to the contacts. The subthreshold current determines the slope of the transfer characteristic in the vicinity of V_T with exponential

dependence on V_G, since the gate voltage induces a potential barrier which in turn controls the electron injection from source into the depleted channel. Accordingly, the slope provides a lower limit for the voltage required to switch the transistor between off-state and on-state. Taking the reciprocal of the slope of the transfer characteristic in semilogarithmic representation yields the subthreshold swing

$$S = \left(\frac{\mathrm{d}(\log_{10} I_D)}{\mathrm{d}V_G} \right)^{-1} \tag{3.3.18}$$

with the theoretical minimum at room temperature of 60 mV/dec, given by the thermodynamic limit of $S = \ln(10) k_B T e^{-1}$ according to Eq. (3.3.17).

3.4 Digital circuit elements

First concepts of interconnecting several electronic circuits on what was back then already referred to as chips were proposed in 1958 and have soon after been implemented by the monolithic integration of multiple transistors on a single crystalline substrate [180,181]. Since then, the ability to incorporate transistors on a single chip has doubled roughly every 18 to 24 months according to Moore's law [182,183]. Both functionality and efficiency of integrated circuits thus improve with time due to increasing packing density as well as continuous reduction of the minimum feature size. Today's integrated circuit building blocks are based on the boolean binary system, implying that voltage signals take on one of at least two discrete levels [184]. Such digital circuits that essentially process or combine binary electronic signals in the desired manner are termed logic gates.

Among the most fundamental digital circuit building blocks is the NOT gate, commonly referred to as inverter. A simple inverter is basically a voltage divider comprising two transistors connected in series, as depicted by the inset in Fig. 3.5 (a). The voltage level of the binary output signal V_{OUT} is determined by the operation state of the input transistor, depending on the input voltage V_{IN} applied at the gate. In the depicted inverter configuration, both transistors are intended to be in depletion mode, i.e. $V_T < 0$. Source and gate of the load are shorted, causing V_G to be fixed at zero and the transistor to constantly remain in a conductive state. A supply voltage $V_{DD} > 0$ is applied at the drain of the load transistor with respect to the common ground, causing the output to take values of $0 \leq V_{OUT} \leq V_{DD}$. Ideally, the logic swing, i.e. the difference between high and low output level, covers the whole supply voltage range. For an input voltage of $V_{IN} \leq V_T$, the channel of the input transistor is fully depleted and thus has a large resistance compared to the load transistor. Consequently, the majority of V_{DD} drops across the input transistor, resulting in $V_{OUT} \approx V_{DD}$. By contrast, increasing the input voltage $V_{IN} > V_T$ beyond the threshold voltage causes the space-charge region in the channel to gradually vanish until eventually the output voltage approaches zero. Thus, an inverter yields a high output signal for a low input voltage and vice versa.

Fig. 3.5 illustrates the geometrical construction of the relation between V_{OUT} and V_{IN} from the output characteristics of the input transistor as well as the load transistor at $V_G = 0\,\mathrm{V}$. Since the source-drain voltage of both transistors add up to V_{DD} in accor-

dance with Kirchhoff's second law, the characteristic of the inverter is then determined by

$$V_{\mathrm{OUT}} = V_{\mathrm{D}}^{\mathrm{input}} = V_{\mathrm{DD}} - V_{\mathrm{D}}^{\mathrm{load}} \tag{3.4.1}$$

with the intersections of both output characteristics being connected by the current conservation equation

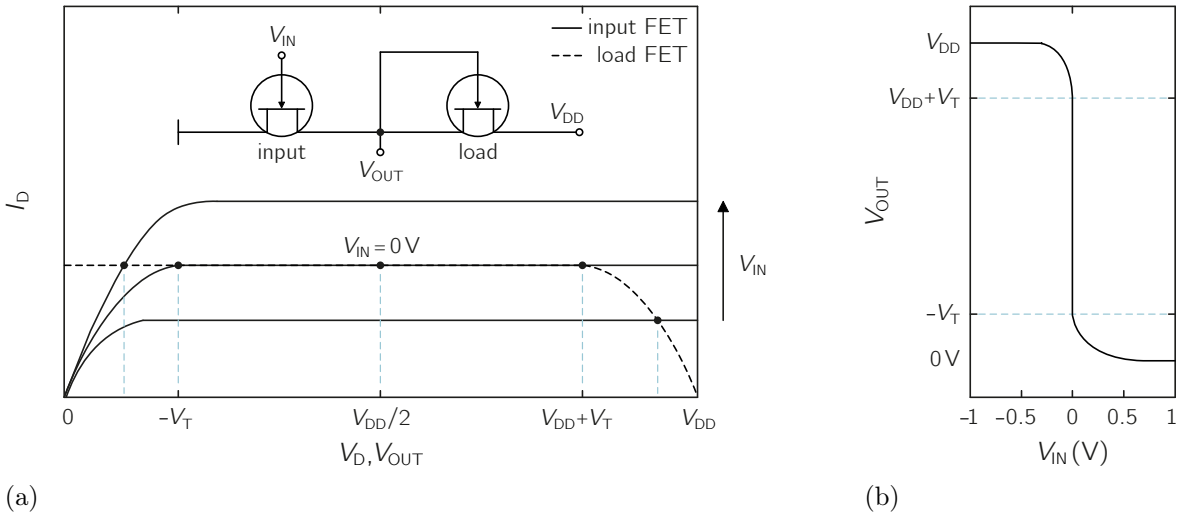
$$I_{\mathrm{D}}^{\mathrm{input}}\left(V_{\mathrm{IN}}, V_{\mathrm{D}}^{\mathrm{input}}\right) = I_{\mathrm{D}}^{\mathrm{load}}\left(0, V_{\mathrm{D}}^{\mathrm{load}}\right) \tag{3.4.2}$$

and assuming gate leakage current to be negligible. Between $V_{\mathrm{OUT}} = V_{\mathrm{DD}} + V_{\mathrm{T}}$ and $V_{\mathrm{OUT}} = -V_{\mathrm{T}}$, the steep transition of the ideal voltage transfer characteristic depicted in Fig. 3.5 (b) yields a discontinuity and the solution for $V_{\mathrm{IN}} = 0\,\mathrm{V}$ is thus not unique. The slope of the transition is described by the gain

$$g = -\frac{\partial V_{\mathrm{OUT}}}{\partial V_{\mathrm{IN}}} \tag{3.4.3}$$

with its maximum being commonly referred to as peak gain magnitude. Small variations of the input voltage around $V_{\mathrm{IN}} = 0\,\mathrm{V}$ thus induce a high amplification of the output signal, although the transition exhibits a pronounced nonlinearity. The required voltage to switch between high and low operation state is given by the uncertainty level, denoting the input voltage difference at both transition points where the gain equals unity. Beyond the transition regime with $g < 1$, the output level of an inverter is unambiguously defined.

For nonideal transistors, the drain current does not perfectly saturate once the chan-



(a) (b)

Figure 3.5: (a) Geometrical construction of an inverter characteristic from the output characteristics of the input and load transistor and (b) simulation of an associated ideal voltage transfer characteristic. The inset depicts the circuit schematic of a simple inverter model.

nel is pinched off, but rather still maintains a dependence on V_D. Eq. (3.3.9) can then be modified to

$$I_\mathrm{D,sat} = I_\mathrm{P}\left[1 - 3\left(\frac{V_\mathrm{bi} - V_\mathrm{G}}{\phi_\mathrm{P}}\right) + 2\left(\frac{V_\mathrm{bi} - V_\mathrm{G}}{\phi_\mathrm{P}}\right)^{3/2}\right] + \alpha(V_\mathrm{D} + V_\mathrm{T}) \tag{3.4.4}$$

with $\alpha(V_\mathrm{D} + V_\mathrm{bi} - \phi_\mathrm{P})$ being an empirical term describing the nonzero slope of the saturation current [185]. The saturation factor $\alpha = (\partial I_\mathrm{D,sat}/\partial V_\mathrm{D})\,|_{V_\mathrm{G}}$ is typically outlined in terms of an output resistance r_o^{-1}, modeling the linear dependence of $I_\mathrm{D,sat}$ on V_D [186]. Consequently, the voltage transfer characteristic of an inverter exhibits a finite slope at $V_\mathrm{IN} = 0\,\mathrm{V}$. Analogous to Eq. (3.4.2), the characteristic is then again determined by the current conservation equation

$$I_\mathrm{D,sat}^\mathrm{input}(V_\mathrm{IN}) + \alpha(V_\mathrm{OUT} + V_\mathrm{T}) = I_\mathrm{D,sat}^\mathrm{load}(0) + \alpha(V_\mathrm{DD} - V_\mathrm{OUT} + V_\mathrm{T}) \tag{3.4.5}$$

within the transition regime. Assuming the maximum gain to occur at $V_\mathrm{DD}/2$ close to $V_\mathrm{IN} \approx 0\,\mathrm{V}$, first-order Taylor expansion of Eq. (3.4.5) around $V_\mathrm{IN} = 0\,\mathrm{V}$ yields

$$V_\mathrm{OUT} = \frac{V_\mathrm{DD}}{2} - g_\mathrm{const} V_\mathrm{IN} \tag{3.4.6}$$

with g_const approximating a constant gain of

$$g_\mathrm{const} = \frac{1}{\alpha}\frac{3I_\mathrm{P}}{2\phi_\mathrm{P}}\left(1 - \sqrt{V_\mathrm{bi}/\phi_\mathrm{P}}\right) \tag{3.4.7}$$

for $-V_\mathrm{T} < V_\mathrm{OUT} < V_\mathrm{DD} + V_\mathrm{T}$ [185]. According to Eq.(3.4.7), increasing α reduces the maximum gain as the slope of the saturation current becomes steeper. Outside of the transition range, one of the transistors starts to operate in the linear regime while the other transistor remains in saturation, causing the gain to decrease rapidly.

Schottky diode FET logic

In order to cascade multiple logic gates, the output signal has to match the input of the subsequent device. Various unipolar logic families implement either complementary p-type and n-type transistors or enhancement mode and depletion mode transistors with compatible logic levels and power supply characteristics. Common technologies include for instance the complementary metal-oxide-semiconductor logic or the direct-coupled FET logic, both of which are somewhat difficult to fabricate or not even accessible for most semiconductors. Since the simple inverter approach depicted in Fig. 3.5 is based on identical unipolar transistors operating in depletion mode, i.e. $V_\mathrm{T} < 0$, the output signal of $0 \leq V_\mathrm{OUT} \leq V_\mathrm{DD}$ and the required input voltage range are not compatible. A suitable technology has been adapted from the GaAs MESFET technology, originally demonstrated in 1974, by adding Schottky diodes to the inverter configuration to adjust the input voltage range by means of the voltage drop over the diodes [187–189].

The corresponding circuit schematic of a Schottky diode FET logic (SDFL) inverter is depicted in Fig. 3.6. DRV and PU denote the input and load transistor of the simple inverter and are in the following referred to as driving transistor and pull-up transistor,

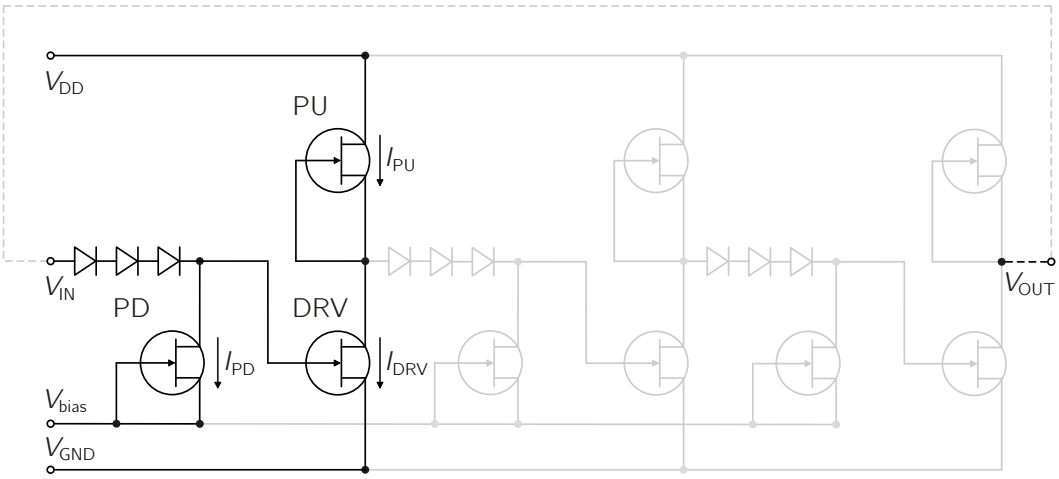


Figure 3.6: Circuit schematic of cascaded SDFL inverters with the output of each inverter connected to the input of the subsequent inverter. DRV, PU and PD denote the driving transistor, pull-up transistor and pull-down transistor, respectively. The dashed gray line indicates a feedback loop, converting the series connection of an odd number of inverters into a ring oscillator.

respectively. At the input of the driving transistor, a certain amount of Schottky barrier diodes as well as an additional pull-down transistor are added. The potential drop across the diodes adjusts V_{IN} such that the gate voltage at the driving transistor is reduced to $V_{\mathrm{G}} = V_{\mathrm{IN}} - V_{\mathrm{shift}}$ in order for the transition point of the inverter characteristic to shift toward higher input voltages. A negative supply voltage of $V_{\mathrm{bias}} \leq (-V_{\mathrm{OL}} + V_{\mathrm{T}})$ is applied at the source of the pull-down transistor with V_{OL} denoting the low output level of the inverter to ensure the depletion mode transistor to constantly operate in saturation due to source and gate being shorted. The pull-down transistor thus serves as constant current source for the diodes and further supplies the current required to discharge the load capacitance of the subsequent gate when the inverter output level is low [186]. Similar to the simple inverter depicted in Fig. 3.5 (a), the voltage transfer characteristic can be constructed geometrically from the output characteristics. For a gate voltage of $(V_{\mathrm{IN}} - V_{\mathrm{shift}}) \leq V_{\mathrm{T}}$, the channel is fully depleted and for $V_{\mathrm{G}} = 0\,\mathrm{V}$, the saturation current I_0 flows through the driving transistor. Typically, a SDFL circuit is designed such that the pull-down transistor has a reduced gate width of, for instance, $3W_{\mathrm{PD}} = W_{\mathrm{PU}} = W_{\mathrm{DRV}}$ compared to the otherwise identical pull-up and driving transistor [186]. The current through the pull-up transistor is then given by $I_{\mathrm{PU}} = I_{\mathrm{DRV}} + I_{\mathrm{PD}}$ with $I_{\mathrm{PD}} = \frac{1}{3} I_0$. Consequently, the output characteristic of the pull-up transistor is shifted by $-\frac{1}{3} I_0$ with respect to the output characteristics of the driving transistor. Further, the maximum output voltage is limited by the forward bias dropping across the diodes, including the gate diode of the subsequent inverter. This assumption is valid as long as the dimensions of associated diodes are in the same order of magnitude and can thus be considered equivalent to a certain extent. Depending on whether the SDFL configuration for level shifting is added at the input or at the output of the inverter, the voltage transfer characteristic is then either shifted toward positive input voltages or toward negative output voltages, respectively.

By applying the output signal of an inverter chain to its input as illustrated in Fig. 3.6, the feedback loop causes the output signal to oscillate between its high and low level, provided that the total number of cascaded inverters is odd. The associated application is referred to as ring oscillator and essentially converts a DC supply voltage into an AC output signal. Each inverter stage contributes to a propagation delay which is mostly determined by the total number of inverter stages as well as the switching speed of the driving transistors. In order for oscillations to occur, the supply voltage of the pull-up transistor V_{DD} with respect to the common ground has to be higher than the level shift provided by the voltage drop V_{shift}. Further, the negative supply voltage at the pull-down transistor is required to be at least equal or less than $V_{\mathrm{bias}} \leq (-V_{\mathrm{OL}} + V_{\mathrm{T}})$. Notably, a ring oscillator initiates oscillations due to thermal noise of the system and thus does not require an external input signal.

As the signal passes through the loop of $2k+1$ ($k \in \mathbb{N}$) cascaded inverters, each inverter stage induces a phase shift of π/k. After two full cycles, the output level has reached its initial state with a total phase shift of 2π, yielding an oscillation frequency of

$$f = \frac{1}{2\sum_k \tau_k} \tag{3.4.8}$$

where τ_k denotes the gate delay of a single inverter. The total time delay per inverter stage can be approximated by

$$\tau = \frac{C_{\mathrm{G}} \Delta V}{I_{\mathrm{PU}}} F \tag{3.4.9}$$

with C_{G} and F being the driving gate capacitance and the fan-out, respectively [190,191]. ΔV denotes the voltage swing which is present at the input of each inverter, describing the lower and upper boundary of V_{G} determined by V_{bias} and the amount of level shift per diode, respectively, provided that the dimensions of the gate diode and the level shifting diodes are in the same order of magnitude. The fan-out corresponds to the total number of gate inputs simultaneously driven by the output of another single inverter stage. Thus, in order to switch the driving transistor, the maximum charging current available to provide the gate charge $q = C_{\mathrm{G}} \Delta V$ is limited by I_{PU}/F. In case of the exemplary SDFL circuit depicted in Fig. 3.6, the fan-out for each inverter is $F = 1$. For a k-stage ring oscillator, Eq. (3.4.8) can then be modified to

$$f = \frac{1}{2k\tau^{F=1}}. \tag{3.4.10}$$

Since the supply current for charging and discharging of the subsequent gate is limited by the constant saturation current provided by the pull-up and pull-down transistor, the oscillation frequency of an SDFL ring oscillator does not depend on V_{DD}. Typically, an additional inverter for signal outcoupling is connected to the output of the ring oscillator, increasing the fan out of the last inverter of the loop to $F = 2$. Consequently, the single stage delay time is given by

$$\tau^{F=1} = \frac{1}{2(k+1)f} \tag{3.4.11}$$

due to $(k-1)$ inverter with $F = 1$ and one inverter with $F = 2$ in the circuit [191].

III

Experimental techniques

4 Device fabrication processes

4.1 Magnetron sputtering

Sputtering belongs to the most widespread and versatile physical vapor deposition techniques for the fabrication of metals as well as semiconductor thin films and dielectrics. Contemporary industrial applications particularly take advantage of the high process scalability combined with high deposition rates. Essentially, sputtering is based on the ejection of target material due to momentum transfer of accelerated energetic species - usually positive ions - generated by glow discharge. Consequently, a vapor flux consisting of the removed particles is launched toward a rotatable substrate which is commonly mounted opposite to the target to maintain uniform conditions of the vapor flux in terms of direction and distribution, as illustrated in Fig. 4.1.

The kinetic energy of the bombardment ions is typically provided by the potential drop between the plasma and the target surface. A key metric to characterize the sputtering event in terms of effectiveness is the sputter yield, describing a measure of the erosion due to ion irradiation defined by the ratio between the average number of sputtered atoms per incident ion. At low ion energies below the surface binding energy of the target material, the sputter yield is magnitudes less than unity, since only adsorbed molecular species or at most loosely bound target atoms can be removed [192]. Once the energy of the sputtering ion exceeds the surface binding energy, sufficient momentum transfer is provided in order for bonds in the target to break due to multiple collision events inside the target material. Dislodged atoms then in turn trigger further recoil collision cascades which eventually result in the ejection of surface atoms and secondary electrons from the target. Nowadays standard sputtering setups

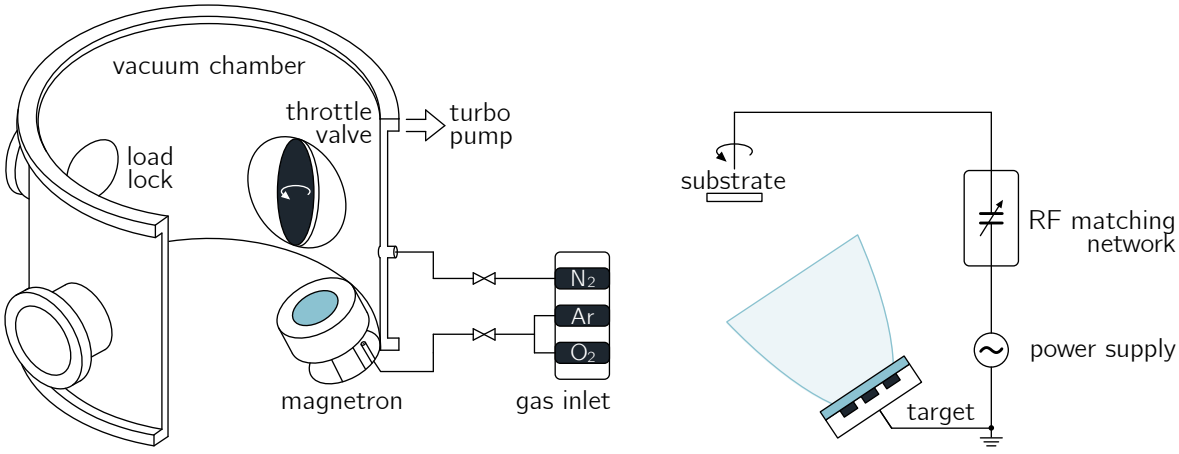


Figure 4.1: Schematic view of an RF sputtering setup with magnetrons arranged at the bottom of the vacuum chamber in a 30° angle with respect to the sample holder, rotating above the target.

deploy magnetrons behind the target source, consisting of permanent magnets often arranged in a circular configuration. Magnetrons are usually engineered such that the closed-loop magnetic field lines run parallel to the target in order to confine secondary electrons and thus increase their path lengths directly above the target surface. As a consequence, the maximized probability of ionizing collisions yields a much higher plasma density and increases both the overall deposition flux as well as the growth rate accordingly.

Since common DC sputtering is restricted to electrically conducting targets, the deposition of compound semiconductors or dielectrics from insulating targets requires a radio frequency (RF) source and associated impedance-matching hardware. The typical frequency supplied to the electrodes is 13.56 MHz. Alternating the polarity of the target cathode prevents charge buildup on the surface caused by the constant plasma current. The RF power couples to the electron motion in the plasma, increasing their path lengths and yielding an improved ionization rate as well as a higher plasma density. As a consequence, the plasma can be maintained at even lower pressures compared to DC magnetron sputtering, resulting in a more direct pathway for the ejected target particles due to fewer collisions with the background gas.

Owing to its chemical inertness and low cost, the ionized gas used for bombardment is typically Ar^+ [192]. Adding a reactive gas to the plasma such as molecular oxygen or nitrogen enables the formation of compounds and provides control over the stoichiometry of the deposited thin film. Chemical reactions between sputtered target species and ionized reactive gases then occur on the substrate surface or already within the plasma. The stoichiometric target transfer can be manipulated even further by applying an additional electric field between target cathode and substrate anode such that sputtered ions or compound gas ions are either accelerated toward the substrate or decelerated, depending on the respective charge state.

ZTO thin films have been fabricated using a long-throw magnetron sputtering system from Mantis Deposition ltd with a target-to-substrate distance of 25 cm [67]. In comparison, the mean free path of sputtered target species is about 1 cm to 10 cm within the applied deposition pressures range of 10^{-3} mbar to 10^{-2} mbar. Hence, larger droplets and clusters can be filtered or even completely thermalized due to collisions with gas atoms and other particles, enabling sputtered material to eventually reach the substrate either by diffusion or along the paraxial direction [193]. Consequently, the deposition rate decreases whereas sputter-induced damage at the substrate surface is reduced substantially, improving both the surface roughness and the thickness uniformity of the thin film. The large target-to-substrate distance further prevents unintentional heating effects caused by the plasma and thus favors the deposition of homogeneous amorphous thin films at room temperature [194].

4.2 Photolithographic patterning

Lithography has been the most predominant method of patterning nanoscale features for semiconductor thin-film technology in modern microelectronic industry. Although the optical resolution of traditional photolithography is inherently limited by the wavelength of the deployed light source, various resolution enhancement techniques have been developed to enhance the minimum resolvable feature size even further [195].

State-of-the-art lithography is thus considered the technical limiter regarding further advances in feature size reduction, affecting both the device speed and the occupied on-chip area. Within the scope of this thesis, either a SÜSS MicroTec MJB3 mask aligner with a mercury vapor lamp ($\lambda = 436\,\mathrm{nm}$) or a configurable μMLA maskless aligner direct-writing system from Heidelberg Instruments with an UV LED ($\lambda = 365\,\mathrm{nm}$) was used for device structuring.

Patterns are generated by selectively exposing a photosensitive polymer to UV irradiation, and by subsequently removing selected areas through dissolution in an appropriate solvent. Ideally, the remaining coating has the exact shape of the intended pattern in the sample plane and thus protects the covered parts of the substrate from the deposition of further material, etching or ion implantation. The general sequence of processing steps of a typical photolithography procedure is schematically depicted in Fig. 4.2.

Prior device patterning on flexible substrates, DuPont Kapton E polyimide foil has been cleaned by sonication in acetone and isopropyl alcohol to remove any contaminants and was then preshrunk in vacuum atmosphere at 200°C for 24 h [196].

(I) For the vast majority of performed photolithography processes, a thin layer of positive photoresist AZ1505 from MicroChemicals has been applied onto the substrate surface. Spin coating at 6000 rpm for 25 s yields a resist thickness of approximately 500 nm. Usually, the sample is prebaked at 110°C for 120 s before the resist is eventually exposed to UV light through a prepatterned photo mask.

(II) Exposed parts of the positive photoresist are removed in an AZ351B developer solution, followed by rinsing, drying and postbaking the sample at 110°C for 120 s.

(III) During deposition of the desired material it is necessary for the resist patterns to stay intact. Since most photoresists degrade at temperatures above 150°C, the sputtering process of each constituent device layer was invariably executed at room temperature.

(IV) Residual resist covered with the semiconductor is stripped off the substrate by ultrasonic cleaning in N-methyl-2-pyrrolidone until the semiconductor remains only where the resist had been dissolved beforehand. After a final cleaning in acetone and isopropyl alcohol, the sample is dried and prepared for a subsequent photolithography process.

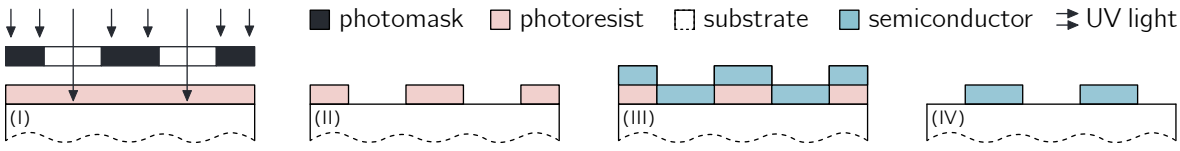


Figure 4.2: Schematic depiction of a typical photolithographic pattering procedure of semiconductor mesa structures: (I) exposure of photoresist to UV light through a prepatterned photomask, (II) development of the resist, (III) semiconductor deposition and (IV) removal of the residual resist by a common lift-off process involving organic solvents.

5 Characterization methods

5.1 Electrical conductivity and Hall effect

To generally classify the fabricated ZTO thin films regarding their electrical properties, combined Hall effect and resistivity measurements were performed. In particular, the Van-der-Pauw method has been used to determine the resistivity ρ, the charge carrier density N and the charge carrier mobility μ_{H}. Apart from a closed isotropic layer with homogeneous thickness as well as comparatively small contact areas with respect to the total thin film size, this approach does not impose any geometrical requirements and thus facilitates the investigation of arbitrary sample shapes [197]. Using the Van-der-Pauw four-point probing principle as depicted in Fig. 5.1 (a), two resistance measurements are conducted to determine $R_{\mathrm{AB,CD}} = V_{\mathrm{CD}} {I_{\mathrm{AB}}}^{-1}$ and $R_{\mathrm{BC,DA}} = V_{\mathrm{DA}} {I_{\mathrm{BC}}}^{-1}$ by applying a current between respective neighboring ohmic contacts. With the thin film thickness d being the only input parameter, the resistivity is then calculated using the relation

$$\rho = \frac{\pi d}{\ln 2} \frac{R_{\mathrm{AB,CD}} + R_{\mathrm{BC,DA}}}{2} f_{\mathrm{vdp}}, \tag{5.1.1}$$

where $0 < f_{\mathrm{vdp}} \leq 1$ denotes the Van-der-Pauw correction function given by the ratio of both resistances [197].

The Hall effect is based on the fact that charge carriers, moving in a conducting medium, are deflected by the Lorentz force caused by an external magnetic field [198]. As soon as an electric field $\vec{\mathcal{E}} = -q^{-1}\vec{F}$ is applied to a semiconductor, the associated exerted force accelerates charge carriers until their velocity saturates due to scattering processes at the crystal lattice or atoms. With m_{eff} denoting the effective mass and τ_{r}

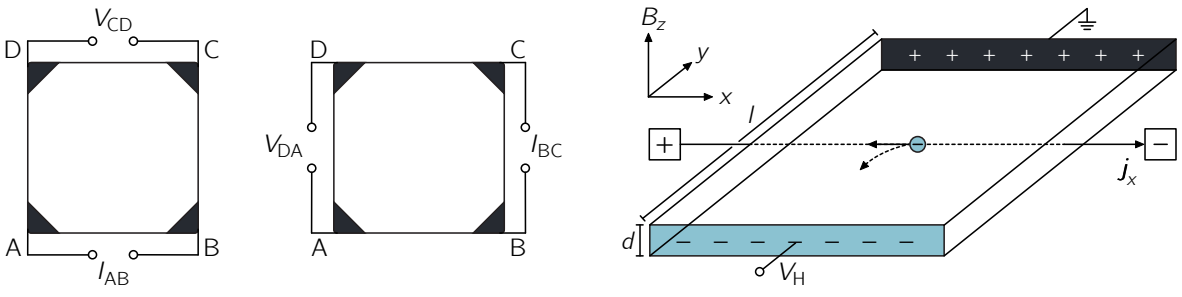


Figure 5.1: (a) Schematic illustration of the Van-der-Pauw four-point probing principle to determine $R_{\mathrm{AB,CD}}$ and $R_{\mathrm{BC,DA}}$. (b) Deflection of charge carriers, contributing to a current density j_x, by the Lorentz force exerted by an external magnetic field B_z. Both electrons and holes are deflected toward the $-y$ direction due to opposite signs of q and j_x.

corresponding to the relaxation time, i.e. the mean duration between two scattering events, the drift velocity v_d and drift mobility μ_d are related by

$$\vec{v}_\mathrm{d} = \frac{q\tau_\mathrm{r}\vec{\mathcal{E}}}{m_\mathrm{eff}} = \mu_\mathrm{d}\vec{\mathcal{E}} \quad . \tag{5.1.2}$$

Considering the average over the relaxation times given by the Hall scattering factor $r_\mathrm{H} = \langle\tau_\mathrm{r}^2\rangle/\langle\tau_\mathrm{r}\rangle^2$, the drift and Hall mobility are connected by $r_\mathrm{H}\mu_\mathrm{d} = \mu_\mathrm{H}$. According to Ohm's law $\vec{j} = \rho^{-1}\vec{\mathcal{E}}$ with a current density of $\vec{j} = qN\vec{v}_\mathrm{d}$, the resistivity can then be described by

$$\rho = \frac{1}{qNr_\mathrm{H}\mu_\mathrm{d}} = \frac{R_\mathrm{H}}{\mu_\mathrm{H}} \tag{5.1.3}$$

with $R_\mathrm{H} = (qN)^{-1}$ denoting the Hall coefficient. The sign of μ_d or R_H determines whether electrons ($q = -e$, $N = n$) or holes ($q = e$, $N = p$) are the dominant carrier type. Applying an additional stationary magnetic field $\vec{B} = (0,0,B_z)$ perpendicularly to the electric field $\vec{\mathcal{E}} = (\mathcal{E}_x,0,0)$ causes a deflection of charge carriers with $j_x = qNv_x$ in $-y$ direction by the Lorentz force $F_y = -qv_xB_z$, as schematically illustrated in Fig. 5.1 (b). Consequently, the charge accumulation induces an electric field $\mathcal{E}_y$, often referred to as Hall field. In equilibrium, the force exerted by $\mathcal{E}_y$ on the charge carriers equals the Lorentz force

$$F_y + q\mathcal{E}_y = -qv_xB_z + q\mathcal{E}_y = -\frac{j_xB_z}{qN} + \frac{qV_\mathrm{H}}{l} \tag{5.1.4}$$

with l denoting the sample length and $V_\mathrm{H} = R_\mathrm{H}j_xlB_z$ being the measurable built-up Hall potential. During nowadays commonly performed combined conductivity and Hall measurements based upon the Van-der-Pauw method, the Hall coefficient

$$R_\mathrm{H} = \frac{d}{B_z}\left(R_{\mathrm{AC,BD}_{(B_z=0)}} - R_{\mathrm{AC,BD}_{(B_z\neq 0)}}\right) \tag{5.1.5}$$

is determined by supplying two opposing contacts with a current and measuring the resulting voltage drop across the two residual contacts both with and without externally applied magnetic field in order to compensate the effect of the external magnetic field on the electric potential [197]. Permutations of the possible contact measurement configurations yield the overall resistivity as well as an average Hall coefficient to then determine N and μ_H according to Eq. (5.1.3).

5.2 Static and dynamic current-voltage measurements

Electrical characterization of devices has been performed using a SÜSS MicroTec PA200 wafer prober system as well as an Agilent 16442A test fixture, both connected to an Agilent 4155C Semiconductor Parameter Analyzer. The latter was predominantly used for static current-voltage (I-V) measurements and quasi-static capacitance voltage measurements, since the maximum sampling frequency for time-resolved analysis is restricted to 12.5 kHz. Automatically characterizing sample batches containing large ensembles of individually designed device patterns was feasible due to

a MATLAB based software developed by Dr. Fabian Klüpfel[3] to control and align the wafer prober sample stage [199]. Electrical contact to samples is established through height-adjustable tungsten needle probes with a tip radius of 7 µm. The usually examined voltage range of $< 20\,\mathrm{V}$ allows a maximum recordable compliance current of $10^{-2}\,\mathrm{A}$ and lower resolution limit of $10^{-12}\,\mathrm{A}$. *I-V* characteristics have been fitted using a MATLAB based software provided by Dr. Daniel Splith[3] to calculate associated parameters and evaluate larger data sets.

Frequency-dependent voltage and current responses in terms of time traces are recorded using a HANDYSCOPE HS3 oscilloscope from TIEPIE ENGINEERING with up to 100 MSa/s sampling, 50 MHz bandwidth and $\pm\,12\,\mathrm{V}$ output supply voltage. For signal outcoupling of investigated integrated circuits, a high input impedance ($10\,\mathrm{M\Omega} \parallel 0.1\,\mathrm{pF}$) active probe by GGB INDUSTRIES INC. has been connected to the oscilloscope input.

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IV

Cumulative part

6 Comparison of all-oxide transparent field-effect transistors

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All-Oxide Transparent Thin-Film Transistors Based on Amorphous Zinc Tin Oxide Fabricated at Room Temperature: Approaching the Thermodynamic Limit of the Subthreshold Swing

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Thin-film transistors (TFTs) based on transparent amorphous oxide semiconductors (TAOSs) have become essential building blocks for a broad range of electronics, since TAOSs facilitate large-scale fabrication at moderate temperatures and hence feature compatibility with flexible substrates. An emerging indium-free alternative to the widely commercially exploited indium gallium zinc oxide (IGZO) is amorphous zinc tin oxide (ZTO); however, according to previous reports, achieving acceptable performance of ZTO-based devices fabricated at temperatures below 300 °C is still challenging to date. Here, key properties of the first all-oxide and fully transparent metal-semiconductor field-effect transistors (MESFETs), metal-insulator-semiconductor field-effect transistors (MISFETs) and junction field-effect transistors (JFETs) based on amorphous ZTO are compared, employing PtO_x, HfO_y, and *p*-type NiO as gate, respectively. All individual layers have been deposited exclusively at room temperature and do not require any additional postdeposition annealing to obtain sufficient device functionality. Demonstrated TFTs exhibit reasonable current on/off ratios of over six orders of magnitude with subthreshold swings as low as 61 mV dec^{-1} at room temperature. Transistor characteristics have been recorded for several weeks to study performance consistency over time and are further investigated regarding their stability under bias stress.

1. Introduction

Within the last two decades, transparent semiconducting oxides (TSOs) considerably regained interest attributed to their unique quality of combining fairly high conductivity with reasonable optical transparency in the visible spectral range, owing to their large bandgap (>3 eV). Amongst the by far most intensively studied TSOs are ZnO, SnO_2, Ga_2O_3, and In_2O_3 as well as several related compound materials and alloy systems, due to their broad application potential in the field of optoelectronic devices.[1–3] Especially transparent amorphous oxide semiconductors (TAOSs) have emerged into a thriving distinct area of research over the last few years, and since then, the field has grown rapidly toward, for instance, novel thin-film transistor (TFT) backplanes for next-generation flat-panel displays.[4,5] Alongside their high transparency, TAOSs exhibit a superior, at least tenfold higher free-carrier mobility compared to conventional amorphous silicon thin films and allow homogeneous large-scale deposition at sufficiently low temperatures, enabling the fabrication of transparent devices on flexible substrates. The by far most mature and already widely commercially exploited representative indium gallium zinc oxide (IGZO); however, contains scarce elements such as indium which innovative research is attempting to substitute by material systems consisting of abundant cations only.[6] One suitable candidate that meets these requirements and gained popularity particularly in the recent couple of years is amorphous zinc tin oxide (ZTO). ZTO is composed of earth-abundant, nontoxic elements only and exhibits, in addition to its optical transparency, a reasonably high free-carrier mobility with reported values up to 12.7 cm^2 V^{-1} s^{-1} in case of ZTO thin films fabricated at room temperature.[7]

The first TFTs implementing amorphous ZTO as channel material have been reported by Chiang et al. back in 2005, followed by numerous studies on ZTO-based TFTs or rather metal-insulator-semiconductor field-effect transistors (MISFETs), fabricated using various deposition methods.[8–13] According to previous reports, however, the realization of MISFETs based on amorphous ZTO, including transparent devices, has up to date exclusively been limited to deposition at elevated temperatures or postdeposition annealing treatment in order to achieve sufficient functionality.[8,14–16] As alternatives to MISFET structures, metal-semiconductor field-effect transistors (MESFETs), implementing an *n*-ZTO/AgO_x Schottky barrier diode as gate contact, have been reported by

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Dang et al. in 2017. Requiring a growth temperature of 400 °C and additional annealing at 525 °C, the resulting ZTO-based MESFETs exhibited a current on/off ratio of 1.1×10^5 and a subthreshold swing as low as 310 mV dec^{-1}.[17] Recently, we reported the first MESFETs as well as junction field-effect transistors (JFETs) based on room-temperature-fabricated amorphous ZTO, implementing an *n*-ZTO/PtO_x Schottky barrier diode and an *n*-ZTO/*p*-NiO heterodiode as gate contact, respectively.[18–20] Despite deposition at room temperature and no additional annealing, except for photolithography-related baking steps at 90 °C for no more than 90 s, the presented devices achieved remarkable current on/off ratios up to 8.6 orders of magnitude and subthreshold swings as low as 124 mV dec^{-1}. MESFETs and JFETs are generally capable of faster switching and operation at lower voltages, although MISFETs exhibit significantly lower gate leakage current.[21] However, regarding fail-safety and device reliability, the preparation of the gate dielectric is the most critical part during MISFET fabrication, since it needs to be thin but highly insulating in order to ensure low power consumption while maintaining low leakage current and has to be grown at low temperatures, possibly room temperature with scalable techniques to reduce fabrication costs.

Alternative scalable approaches to substitute conventional a-Si and IGZO TFTs include, for instance, a-ZnON thin films or carbon nanotube-based devices. While a-ZnON exhibits high free-carrier mobilities in the order of 10^2 cm^2 V^{-1} s^{-1}, corresponding thin films lack transparency in the visible range as well as sufficient processing reliability.[22] Carbon nanotubes, on the other hand, are transparent due to their low thickness and exhibit a reasonable free-carrier mobility; however, usually a more complex sample preparation and higher processing temperatures are required compared to the presented ZTO-based TFTs.[23]

Here, we report on the realization of the first all-oxide and fully transparent MESFETs, MISFETs, and JFETs based on amorphous ZTO thin films, deposited exclusively at room temperature and without additional thermal annealing treatment. Demonstrated devices have been compared regarding their DC performance and are further investigated in terms of stability under negative bias stress as well as performance consistency over several weeks.

2. Results and Discussion

Investigated all-oxide ZTO-based field-effect transistors consist of symmetric ring structures with a front-gate geometry deposited on top of a planar amorphous ZTO thin film serving as channel layer. A photographic image of transparent MESFET, MISFET, and JFET samples as well as an associated laser-scanning microscopy image of MESFET structures are depicted in **Figure 1**. The gate length of all FETs was fixed at $L = 10$ µm while the gate width W ranges from 470 to 2360 µm, depending on the particular circumference of each ring structure. An optical transmission spectrum, including all individual layers that have been employed in the demonstrated device structures, is displayed in **Figure 2**a. Corresponding schematic cross sections through a MESFET, MISFET, and JFET devices, illustrating the basic material stacking order, are depicted in Figure 2b. The ZnO : 4 wt.% Ga_2O_3 (GZO) thin films, serving as ohmic source and drain contacts and as gate capping, as well as the ZTO channel exhibit an average transmittance in the visible spectral range of 83%. In combination with HfO_y as gate insulator, complete MISFET structures composed of a ZTO/HfO_y/GZO layer sequence show a mean transmittance of 81% between 380 and 780 nm, as denoted by the dotted line in the optical transmission spectrum. The PtO_x layer of the Schottky barrier diode exhibits the overall lowest average transmittance in the visible range of 57%. At 780 nm, PtO_x reaches a transmittance of 79%; however, for the green and blue spectral range, a significant decrease in transmission is observed. In order to enhance the transparency of PtO_x-based MESFETs, Frenzel et al. proposed an alternative approach to transparent circuitry by successfully decreasing the thickness of the PtO_x gate contact down to 50 Å for ZnO/PtO_x MESFETs.[24] However, the thickness of PtO_x plays a vital role in suppressing the leakage current in ZTO/PtO_x Schottky barrier diodes, since a thicker PtO_x layer provides a larger oxygen reservoir.[25] Hence, the resulting trade-off between device transparency and performance of ZTO-based MESFETs has to be taken into account.

Exemplary static room temperature current–voltage characteristics of a ZTO-based MESFET, MISFET, and JFET with gate widths and gate lengths of $W = 470$ nm and $L = 10$ nm, respectively, are depicted in **Figure 3**a. For a better clarity, only the voltage sweep direction from positive to negative gate voltages

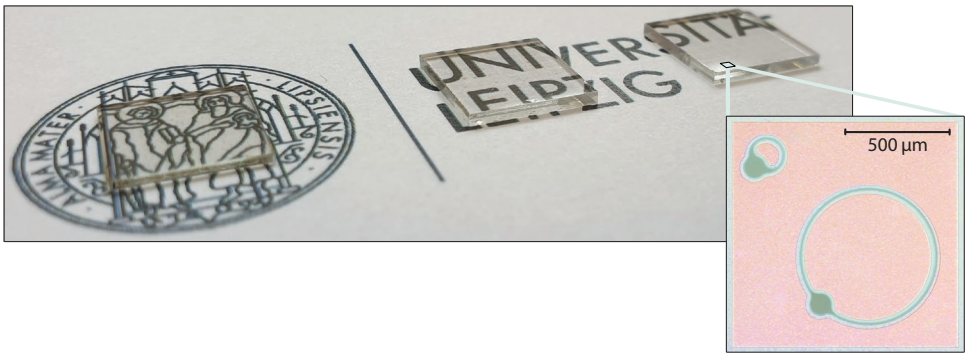

Figure 1. Photographic image of transparent samples containing all-oxide MESFETs, JFETs, and MISFETs based on amorphous ZTO (background: printed logo of the Universität Leipzig) as well as an exemplary corresponding laser-scanning microscopy image of MESFET structures. Gate contacts appear greenish due to thin film interference of superimposed ZTO/PtOx/GZO layers.

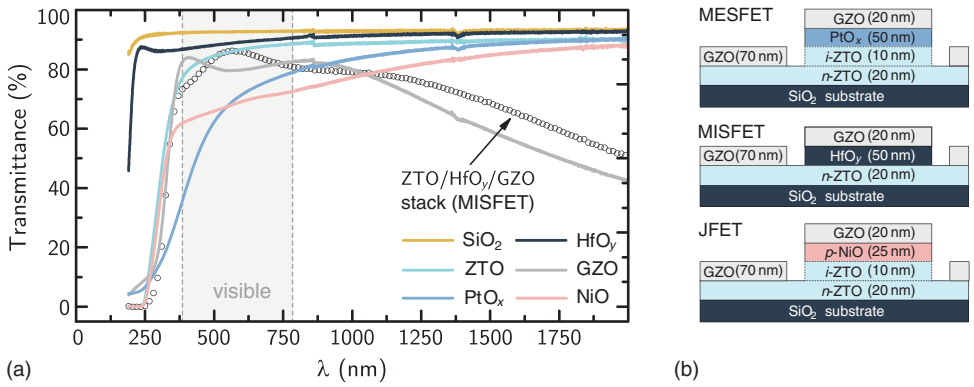

Figure 2. a) Optical transmission spectrum including all individual layers that have been employed in MESFET, JFET, and MISFET devices. The dotted line corresponds to a ZTO/HfOy/GZO layer sequence and represents a MISFET sample, exhibiting a mean transmittance of 81% in the visible spectral range. b) Illustration of the basic material stacking order and the respective schematic cross section through the investigated FET structures.

is displayed. The source–drain voltage was fixed at V_D = 2 V. Each transistor type exhibits a clear field effect with a current on/off ratio as high as 6.2, 4.8, and 4.9 orders of magnitude for the MESFET, MISFET, and JFET, respectively, and can be switched within a similar voltage range of less than 3 V due to their subthreshold swing of 99, 362, and 112 mV dec^{-1}. All devices are normally-on with threshold voltages of –0.05 and –0.1 V for the MESFET and JFET, respectively. A slightly larger threshold voltage of MESFETs indicates a higher built-in voltage of the Schottky barrier diode compared to the *pn* heterodiode of JFETs.[19] The MISFET, on the other hand, exhibits the lowest threshold voltage of –0.7 V due to the voltage drop across the gate insulator. Properties of corresponding device ensembles are collected within histograms in Figure 3b. All three FET types provide a similar on-current density in the order of 1–10 mA cm^{-2} for V_G = 1 V, which is limited by the resistivity of the ZTO channel and the amount of leakage current over the gate diode. While the MESFET shows the overall highest current on/off ratio and smallest subthreshold swing, the MISFET exhibits a significantly lower gate leakage current for $V_G > 0$ V and hence has the largest on-current density. In comparison to the MESFET, however, the off-current density of the MISFET is relatively high, which can most likely be attributed to fabrication-induced shunt resistances between source and gate contact. The ZTO/NiO JFET exhibits a current on/off ratio similar to the MISFET due to its high gate leakage current. Compared to the MESFET, the gate current of the *pn* heterodiode is already dominating the drain current at an applied gate voltage of ≈0.5 V. This is due to the fact that metal-oxide thin films tend to exhibit a porous and pitted structure when

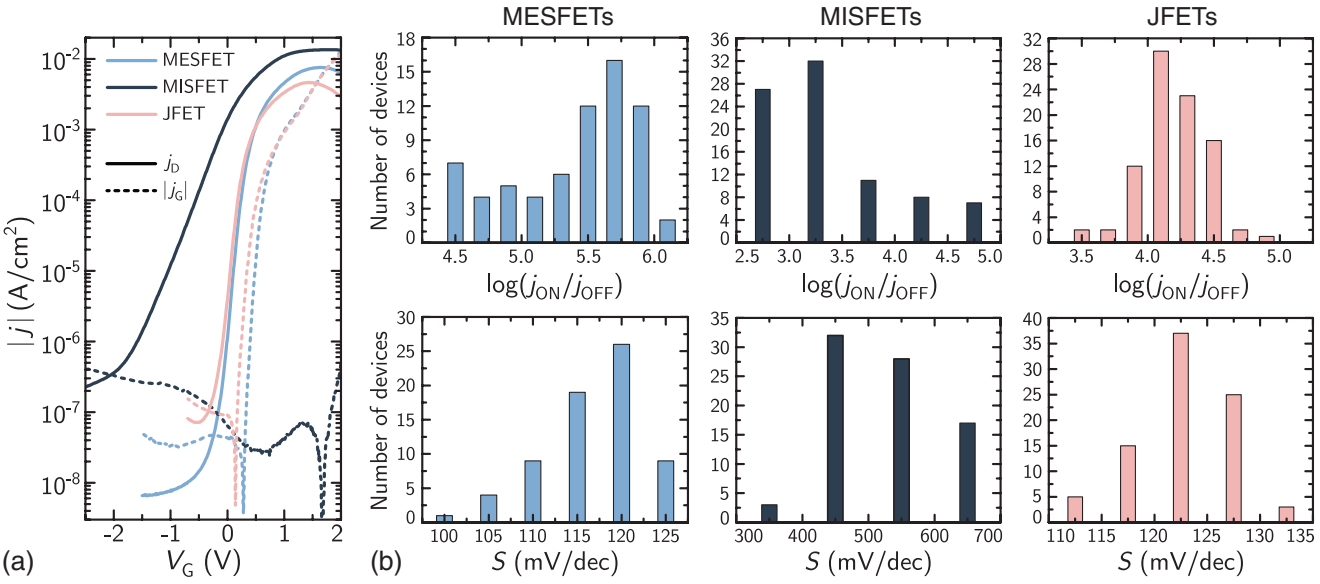

Figure 3. a) Room temperature transfer characteristics (solid lines) and associated gate leakage currents (dashed lines) of a ZTO-based MESFET, MISFET, and JFET (scanning direction from positive to negative gate voltages) and b) histograms displaying current on/off ratios and subthreshold swings of corresponding device ensembles with gate width-to-length ratios varying from 47 to 236. The source–drain voltage was fixed at 2 V.

deposited by pulsed laser deposition at room temperature under a fairly high oxygen partial pressure (here 0.1 mbar).[26] The resulting formation of pinholes in the NiO layers hence remarkably enhances the probability of shunt-induced leakage currents through the gate. Increasing the thickness of the NiO layer by approximately a factor of three to 80 nm yielded an improved and rather constant leakage current for $V_G < 0$ V, as has been reported for ZTO-based JFETs.[19]

The field-effect mobility of each transistor has been estimated by calculating the transconductance g_m from the transfer characteristics depicted in Figure 3a. Considering the channel resistance R_S, the forward transconductance can be expressed by $g_m^{-1} = g_{max}^{-1} + R_S$, where g_{max} is the theoretical maximum of the transconductance, given by the channel conductivity.[27] Since $R_S = \rho L_R / (W d)$ is determined by the part of the channel between gate electrode and both ohmic contacts (here L_R = 30 µm), the field-effect mobility has been estimated according to

$$\mu_{FE} = \frac{g_{max}}{end}\left(\frac{L + L_R}{W}\right) \quad (1)$$

Using the transconductance of the MESFET, MISFET, and JFET of 8.04, 12.68, and 6.69 µS, respectively, Equation (1) yields a field-effect mobility of 2.9, 4.9, and 2.4 cm^2 V^{-1} s^{-1}. μ_{FE}, however, underestimates the free-carrier mobility of 7.6 cm^2 V^{-1} s^{-1}, determined for the ZTO channel by Hall effect measurements, especially in case of the MESFET and JFET, and thus should be considered a lower mobility limit, since g_{max} cannot be reached due to the impact of increasing leakage current occurring for positive gate voltages. Although the demonstrated FETs based on TAOSs are generally intended to operate at low power, breakdown attempts have been performed by biasing the source–gate diode and the channel up to maximum 5 V. Recorded transfer characteristics of a MESFET, MISFET and JFET before and after applying a source–gate voltage of $V_G = -5$ V and a source–drain voltage of $V_D = 5$ V are compared within Figure S1 in the Supporting Information. Characteristic FET parameters such as the current on/off ratio, the subthreshold swing and the threshold voltage remain approximately unaltered. However, all three FET types exhibit a slight decrease in on-current and simultaneously in off-current triggered by biasing of the gate diode, as can be observed during negative bias treatment.[25]

In order to investigate the long-term stability and performance consistency of the demonstrated MESFETs, MISFETs, and JFETs, the as-deposited device characteristics depicted in Figure 3a have been recorded for additional 63 d under equivalent conditions. The temporal evolution of associated characteristic FET parameters is displayed in **Figure 4**. Regarding performance consistency, the MESFET and JFET undergo a slight drop in current on/off ratio after 14 d from 6 and 5 to 5.5 and 4.5 orders of magnitude, respectively. However, both devices recover after a few weeks, while the MESFET even exhibits $\log(j_{ON}/j_{OFF})$ = 6.5 orders of magnitude and thus exceeds its initial value after 49 d attributed to an improvement of the gate diode resulting in a reduced leakage current. The MISFET shows a decrease in current on/off ratio from 4.7 to 4 orders of magnitude after seven days due to an increased gate leakage current. The simultaneous increase of the subthreshold swing from 362 to 579 mV dec^{-1} is accompanied by a shift of

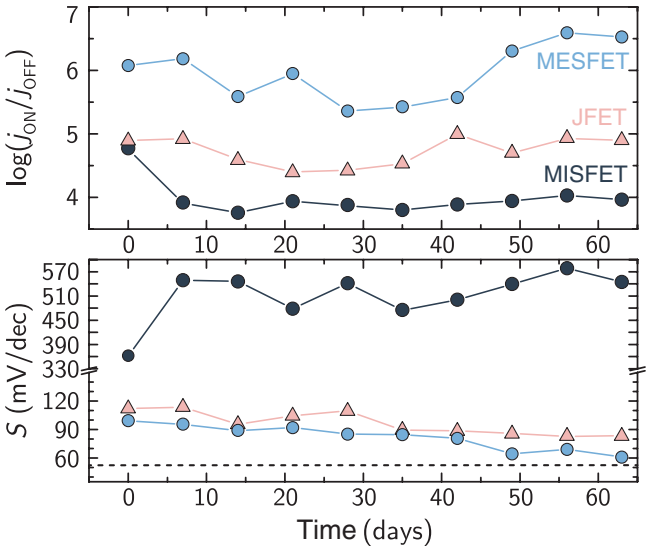

Figure 4. Evolution of characteristic FET parameters of the ZTO-based MESFET, MISFET, and JFET over a period of 63 d, extracted from transfer characteristics recorded under equivalent conditions. Corresponding as-deposited transfer characteristics are compared in Figure 3a. The dashed line represents the thermionic limit of the subthreshold swing at $T = 293$ K according to Equation (2).

the turn-on voltage from $V_G = -2$ to -3 V. Repeated measurements of transfer characteristics, however, result in stable FET properties within the studied time period of 63 d. Meanwhile, the subthreshold swing of both the MESFET and JFET significantly improves over time and, in case of the MESFET, even approaches the thermodynamic limit

$$S_{min} = \frac{k_B T}{q}\ln(10) \approx 58\ \text{mV dec}^{-1}\ \text{at}\ 293\ \text{K} \quad (2)$$

(derived for MESFETs by Liang et al.[28]), achieving record values for ZTO-based FETs as low as 61.1 mV dec^{-1} at room temperature (here $T = 293$ K).

Analogous to Schultz et al., the effect of negative bias stress on the performance of a ZTO-based MESFET has been investigated.[25] The evolution of a transfer characteristic and corresponding FET properties over a period of 15 h is depicted in **Figure 5**. During NBT, −2 V has been applied to the source–gate diode for 300 s while simultaneously the source–drain potential was set to 0 V to prevent current flow from gate to drain. Subsequent to the NBT, transfer characteristics have been recorded and the cycle has been repeated once per hour. A small decrease of the off-current can be observed with each NBT cycle, due to an improvement of the gate diode, resulting in a slightly increased current on/off ratio. Further, a small shift of the threshold voltage of 100 mV toward negative gate voltages along with an increase of the subthreshold swing from 113 to 132 mV dec^{-1} is observed. The improved off-current is related to an enhanced diffusion of oxygen from the PtO_x layer toward the ZTO channel interface, where it saturates undercoordinated cation bonds.[25] Changes of FET characteristics and corresponding parameters are expected to saturate when interface-near cations are fully coordinated or the oxygen

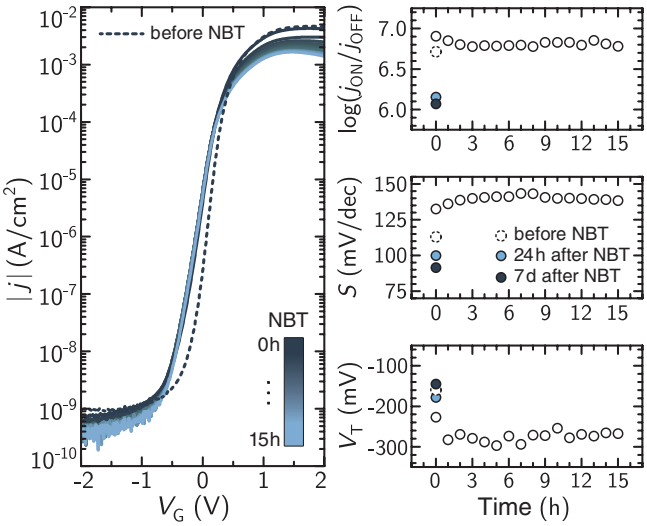

Figure 5. Evolution of transfer characteristics of a ZTO-based MESFET and associated FET parameters after repetitive negative bias treatment over a period of 15 h. The source–drain voltage for measurements of transfer characteristics after each NBT cycle was fixed at 2 V.

reservoir in the PtO_x layer is eventually exhausted. This phenomenon has been found to be similar to naturally occurring, oxygen-diffusion-driven aging processes of ZTO/PtO_x-based devices.[18,25] Despite the continuous minor changes of the on- and off-current with each cycle, the subthreshold swing and threshold voltage seem to be unaffected by repeating the NBT process. 24 h later, the subthreshold swing and threshold voltage started to recover from the exerted bias stress and eventually approached their initial values, as depicted in Figure 5. Repeated measurements after one week even show an improved subthreshold swing, reaching values as low as 91 mV dec^{-1}. After the NBT procedure, however, the current on/off ratio dropped from initially 6.7 to ≈6.1 orders of magnitude. This slight decrease might be attributed to a stress-induced accelerated aging process and is consistent with observed aging-related performance changes of associated MESFETs after 14 d, as displayed in Figure 4.

3. Conclusion

All-oxide and fully transparent MESFETs, MISFETs, and JFETs based on amorphous, room-temperature fabricated ZTO, implementing a PtO_x gate, a *p*-NiO gate and HfO_y as gate insulator, respectively, have been compared regarding their DC characteristics. Investigated devices remain functional during the studied time of ten weeks and showed consistent performance under the impact of bias stress. PtO_x/ZTO-based MESFETs turn out to be the most promising of the three FET types with current on/off ratios over six orders of magnitude and excellent subthreshold swings as low as 61 mV dec^{-1} at room temperature, whereas the JFETs and MISFETs exhibit comparatively large gate leakage currents, most likely due to fabrication-induced shunts within the associated *p*-NiO gate contact and HfO_y gate insulator, respectively. Even though, the performance of the MISFETs slightly degraded after a few days, the MESFETs and JFETs significantly improve over time. However, the choice of the gate type certainly depends on the desired device applications: although the presented MISFETs exhibit fairly low gate leakage current, a more promising dynamic behavior is generally expected in case of MESFETs and JFETs since carrier scattering processes at the channel–insulator interface do not have to be taken into account.[21,29] Moreover, MESFETs and JFETs usually operate at lower supply voltages compared to MISFETs due to the absent gate dielectric.

The presented results prove the feasibility of all-oxide and fully transparent field-effect transistors from earth-abundant elements based on amorphous ZTO, even though the fabrication process of each individual layer has been restricted to room temperature and completed devices did not require additional thermal annealing treatment to obtain sufficient device functionality. Moderate processing temperatures further facilitate the transfer of ZTO-based devices from rigid glass substrates to thermally unstable, flexible substrates, paving the way for low-cost transparent and bendable applications with promising dynamic properties.[20,30]

4. Experimental Section

The 20 nm thin n-ZTO channel layers with a cation composition of 1:1 Zn:Sn have been deposited on 10 × 10 mm^2 SiO_2 substrates by radio frequency (RF) long-throw magnetron sputtering at room temperature using a single ceramic target.[31] A comparatively large target-to-substrate distance of 25 cm was chosen to enable homogeneous growth and to reduce the impact of droplet impingement as well as high-energetic particles in order to minimize sputter-induced damage. The radio frequency power and chamber pressure were kept constant at 70 W and 10^{-3} mbar, respectively. X-ray diffraction and reflectivity measurements have been conducted to confirm amorphous growth and to determine individual thin film thicknesses. In order to investigate the actual transparency of single constituent layers as well as whole devices, transmission measurements have been carried out using a PerkinElmer Lambda 19 spectrometer.

Device structures of MESFETs, MISFETs, and JFETs have been patterned using photolithography with a lift-off process; thus, samples have been exposed to maximum temperatures of 90 °C for no more than 90 s in order to develop photo resist structures. The basic material stacking order of the three transistor types is schematically depicted in Figure 1b. Since previous investigations on ZTO-based FETs indicated the formation of a highly conductive ZTO layer close to the substrate, inhibiting sufficient depletion of the channel, the sputtering process was ignited in an oxygen-rich atmosphere of 25/30 sccm O_2/Ar.[18,19] Subsequently, a conductive ZTO channel layer has been deposited on top of the intrinsic buffer layer. Source and drain contacts consist of ZnO : 4 wt% Ga_2O_3 (GZO) with a nominal thickness of ≈70 nm grown by pulsed laser deposition at room temperature using a single ceramic target. Prior to the gate fabrication, ≈10 nm thin intrinsic ZTO layer (*i*-ZTO) has been deposited on top of the active channel to reduce the leakage current through the gate diode by saturation of under-coordinated cation bonds due to a transfer of oxygen at the channel interface.[20,32] The individual gate contacts have been fabricated in a single final step: MESFETs, MISFETs and JFETs employ a 50 nm PtO_x layer, 50 nm of HfO_y as gate insulator, and a 25 nm *p*-type NiO thin film, respectively. PtO_x and HfO_y have been deposited at room temperature by RF long-throw magnetron sputtering from a metallic and ceramic target, respectively, and NiO has been grown at room temperature by pulsed laser deposition. Due to the low hole mobility of the NiO thin film, it was not possible to determine the hole concentration by performing Hall

effect measurements. Thus, the *p*-type character of NiO has qualitatively been confirmed by performing Seebeck measurements.[33] Eventually, all gate contacts were capped with a 20 nm thin GZO layer to ensure a homogeneous electric potential distribution.

Electrical properties of the ZTO thin films such as the free-carrier density and mobility of $n = 4.2 \times 10^{17}$ cm^{-3} and $\mu = 7.6$ cm^2 V^{-1} s^{-1}, respectively, have been obtained by conducting Hall effect measurements in Van-der-Pauw geometry at room temperature with a magnetic field of 0.4 T. Static current–voltage characteristics were recorded using an Agilent 4155C semiconductor parameter analyzer and a SÜSS wafer prober system.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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All-Oxide Transparent Thin-Film Transistors Based on Amorphous Zinc Tin Oxide Fabricated at Room Temperature: Approaching the Thermodynamic Limit of the Subthreshold Swing

Oliver Lahr, Michael S. Bar, Holger von Wenckstern, and Marius Grundmann*

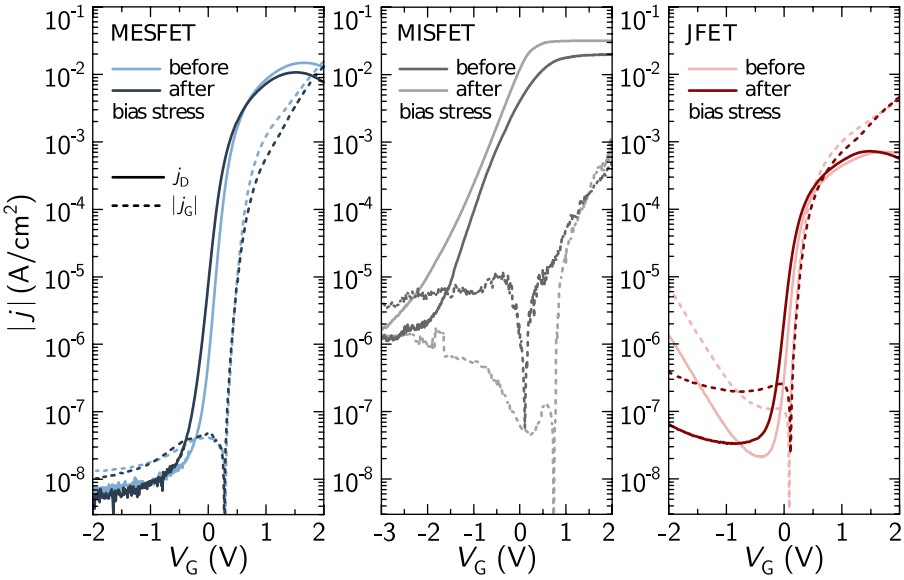

Figure S1. Room temperature transfer characteristics of a MESFET, MISFET and JFET before and after recording transfer characteristics under a bias stress of V_G = – 5V and V_D = 5, applied to the source-gate diode and the channel, respectively.

7 State-of-the-art integrated circuitry

The content of this section has been published in the following three manuscripts:

Oliver Lahr, Zhipeng Zhang, Frank Grotjahn, Peter Schlupp, Sofie Vogt, Holger von Wenckstern, Andreas Thiede and Marius Grundmann

Full-Swing, High-Gain Inverters Based on ZnSnO JFETs and MESFETs

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Low-Voltage Operation of Ring Oscillators Based on Room-Temperature-Deposited Amorphous Zinc-Tin-Oxide Channel MESFETs

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Full-Swing, High-Gain Inverters Based on ZnSnO JFETs and MESFETs

Oliver Lahr, Zhipeng Zhang, Frank Grotjahn, Peter Schlupp, Sofie Vogt, Holger von Wenckstern, Andreas Thiede, and Marius Grundmann

***Abstract*— Metal–semiconductor and junction n-channel field-effect transistors (MESFETs and JFETs) have been fabricated on glass substrates using room temperature deposited amorphous zinc–tin oxide (ZTO) channel layers. Characteristics of transistors and inverter circuits are compared. Best FET devices exhibit ON-to-OFF current ratios over eight orders of magnitude, subthreshold swings as low as 250 mV/dec and field-effect mobilities of 5 cm^2/Vs. Furthermore, all devices show long-term stability over a period of more than 200 days. Inverters fabricated using either MESFETs or JFETs exhibit remarkable peak gain magnitude values of 350 and voltage uncertainty levels as low as 260 mV for an operating voltage of 5 V. A Schottky diode FET logic (SDFL) approach is applied to shift the switching voltage which is a requirement for cascading of inverters for realization of ring oscillators.**

***Index Terms*— FET integrated circuits, inverters, junction field-effect transistor (JFET), metal–semiconductor field-effect transistor (MESFET), Schottky diode FET logic (SDFL), semiconductor device reliability, transparent amorphous oxide semiconductors, zinc–tin oxide (ZTO).**

I. Introduction

AMORPHOUS oxide semiconductors (AOS), consisting of heavy metal cations, exhibit remarkable transport properties and can be deposited at temperatures compatible with flexible and organic substrates [1], [2]. The AOS indium–gallium–zinc oxide (IGZO) is already commercially exploited; however, there are efforts to substitute this material by compounds that consist of abundant cations only [3]. One promising candidate is amorphous semiconducting zinc–tin oxide (ZTO) since it consists of abundant elements only. Room-temperature deposited amorphous ZTO exhibits a fairly short wavelength absorption edge, making it transparent in the visible spectral range, as well as a high free carrier mobility up to 12.6 cm^2/Vs [4]. Several metal–insulator semiconductor field-effect transistors (MISFETs) based on ZTO have already been reported [5]–[10]. However, MISFETs and related integrated circuits require an additional fabrication step and usually suffer from higher operating voltages due to the voltage drop across the gate insulator. Recently, properties of ZTO-based metal–semiconductor field-effect transistors (MESFETs) were published [11], [12]. Their key advantage, compared to previously reported ZTO-based MISFETs, is the higher field-effect mobility resulting in a higher current, transconductance, and transit frequency of the devices [13].

A major drawback of logic circuit approaches comprising inverter structures based on only depletion-type transistors is that their output voltage range does not cover the voltage range needed to switch a subsequent inverter. The simple inverter approach results in positive output voltages only, while negative voltages are necessary to switch the driving transistor. Therefore, sufficient level shifting of the output voltage is required. Concerning oxide-based inverter circuits, the Schottky diode FET logic (SDFL) approach was reported for ZnO-based inverters comprising MESFETs [14], [15] and an adaptation implementing p-n diodes in the case of JFET-based inverters [13], [16].

For AOS, publications on MESFET and JFET devices cover only reports on IGZO-based MESFETs [17]–[20], IGZO-based JFETs [21], [22] and ZTO-based MESFETs [11], [12]. In this work, we compare and discuss properties of n-channel ZTO/PtO_x/Pt MESFETs and ZTO/NiO JFETs as well as properties of SDFL inverter structures comprising these MESFETs or JFETs, respectively.

II. Mask Layout and Operation Principle

The layout of our SDFL inverter is depicted in the photographic image of Fig. 1. It consists of FET DRV being the driving transistor, FET PU being the pull-up or load transistor and FET PD being the pull-down transistor along with two level-shifting diodes. The terminal V_{GND} is the common ground, V_{DD} supplies the operating voltage, V_{OUT} is the output voltage, and V_{bias} is the operating voltage of the pull-down FET. Three terminals are available for the input voltage V_{IN}: D_0 input without level-shifting diodes, D_1 (D_2) input including one (two) level-shifting diode(s) allowing to shift the output signal.

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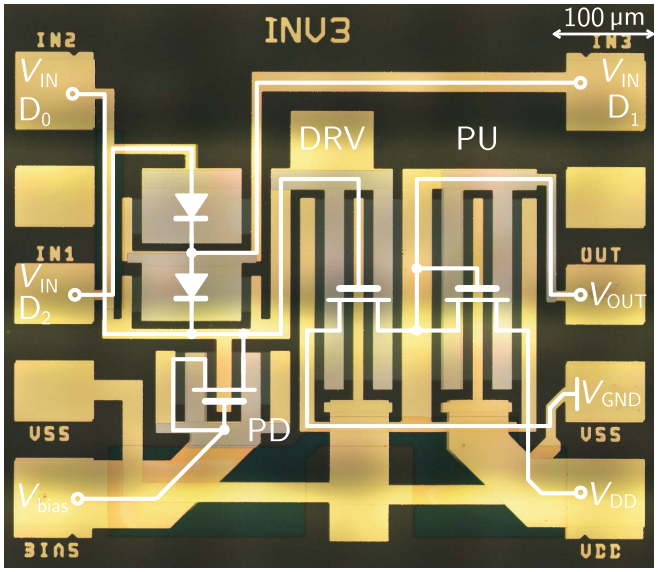

Fig. 1. Microscopic image with overlayed circuit schematic of an SDFL inverter consisting of three transistors. PU: pull-up FET; DRV: driving FET; and PD: pull-down FET.

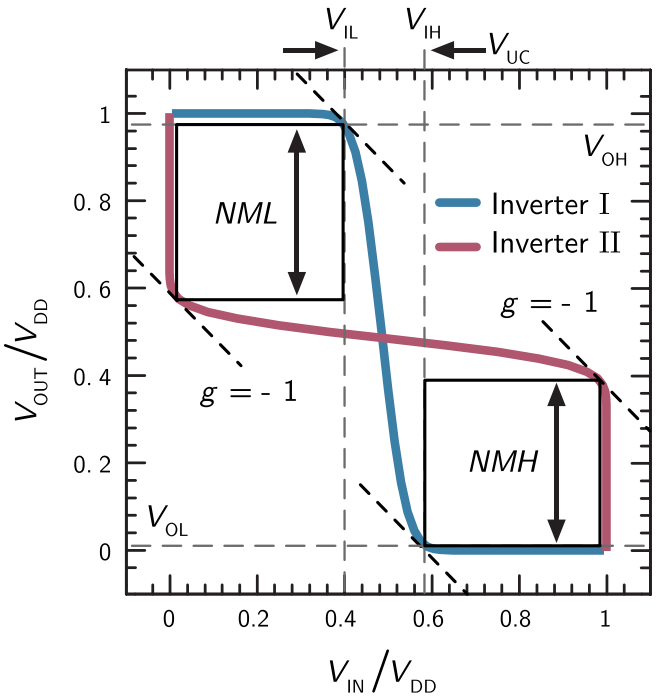

Fig. 2. Butterfly representation of two cascaded inverters used to define characteristic inverter parameters. V_{IL} and V_{IH} (V_{OL} and V_{OH}) are input (output) voltages for which the VTC of inverter I (blue solid line) has slope $g = -1$ (gray dashed lines), the difference $V_{IH} - V_{IH} \equiv V_{UC}$ defines the uncertainty voltage. The red line depicts the characteristic (mirrored at the line connected points $V_{IN}/V_{DD} = 1$ and $V_{OUT}/V_{DD} = 1$) of cascaded inverter II. The noise margins correspond to the side length of the largest square that can be drawn into the wings of the butterfly plot.

Two metallization layers are provided in this technology allowing realizing multi-gate transistors. In order to show the feasibility of this process, all transistors in the inverter design are realized with two gate fingers; 20-μm gate length and 10-μm distance between gate and drain–source edges are used. The gate width per finger is 185 μm for the active and load transistor of the inverter stage. Diodes, either Schottky barrier diodes or p-n heterojunctions, are based on the transistor layout style with drain and source shorted. The same mask set was used to realize MESFET- and JFET-based inverters, since the operation principle of the presented inverter circuit is equivalent, regardless whether MESFETs or JFETs are employed.

Important parameters that can be extracted from a voltage transfer characteristic (VTC) of an inverter are highlighted in the butterfly plot of Fig. 2 showing the characteristic of an inverter I (blue solid line) and that of an inverter II (red solid line) to be connected to the output of inverter I. First, the VTC of inverter I is considered. There are two points in its VTC with slope $g = -1$. The corresponding input (output) voltages are labeled V_{IL} (V_{OH}) and V_{IH} (V_{OL}). For $V_{IN} < V_{IL}$, the output voltage of inverter I corresponds to the high state ($V_{OUT} \geq V_{OH}$) or a logic 1. For $V_{IN} > V_{IH}$, the output voltage of inverter I corresponds to the low state ($V_{OUT} \leq V_{OL}$) or a logic 0. The voltage range, in which the logical state of the inverter is not well defined is $V_{UC} = V_{IH} - V_{IL}$ and called uncertainty level. The difference $V_{OH} - V_{OL}$ is called logic swing corresponding in the ideal case, for which $V_{OH} = V_{DD}$ and $V_{OL} = 0$, to V_{DD}. Another important property of an inverter is the peak gain magnitude (*pgm*) being the absolute value of steepest slope around the switching voltage. For an ideal inverter, the *pgm* is infinite. For the butterfly plot, the characteristic of inverter II in Fig. 2 is obtained by exchange of the x- and y-axes (for inverter II V_{IN} is on the y-axis and V_{OUT} is on the x-axis). This representation allows to read off the output of inverter II for any given input voltage to inverter I. As long as V_{IN} of inverter I is below V_{IL}, the output voltage of inverter II is below V_{OL}. In other words, for any voltage $V_{IN} < V_{IL}$ input to inverter I, the logic state of inverter II is well defined and zero. Therefore, one defines a noise margin for low-voltage output NML $= V_{IL} - V_{OL}$ which is indicated in Fig. 2 by the vertical arrow in the left wing of the butterfly plot. In analogy, one defines a noise margin for high-voltage output NMH $= V_{OH} - V_{IH}$ which is indicated in Fig. 2 as well.

III. Experimental Section

Amorphous ZTO thin films were deposited at room temperature (RT) in a long-throw magnetron sputtering system from Mantis Deposition. The chamber base pressure is about 6×10^{-7} mbar, the target-substrate distance is with 25 cm comparatively large which reduced the impact of high energetic particles. In addition, a large target substrate distance enables droplet-free growth of homogeneous thin films on large area substrates. The growth rate is significantly lower than in standard sputtering systems, which is, however, not an issue for thicknesses required for thin-film transistor fabrication. We used a ceramic ZTO target (33 wt.% ZnO, 67 wt.% SnO_2) with a purity of 99.9%; a radio frequency power of 70 W was applied during thin film growth. Prior to deposition, the target was presputtered for 10 min. The ZTO channel layers with nominal thickness of 22 nm were grown on 10 mm $\times$ 10 mm SiO_2 substrates (from Crystal GmbH).

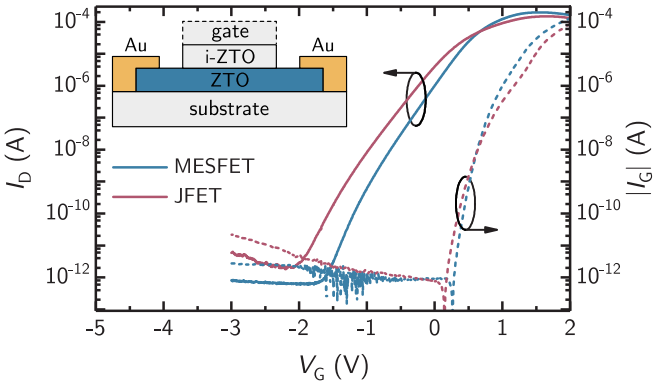

Fig. 3. Transfer and diode characteristic of the best MESFET and JFET (scanning direction from negative to positive gate voltages). Dashed lines: source–gate characteristics. Inset: schematic cross section of the ZTO-FET structure. V_D of 2 V was used for all measurements.

The thin films were patterned by photolithography. We used AZ 1514H as photoresist, requiring baking for 90 s at 110 °C, and AZ 351B (both from MICROCHEMICALS) as developer. The ZTO mesa structures were deposited in a two-step process. First, sputtering was done in a 25/30-sccm O_2/Ar flow atmosphere for 12 min and subsequently in a pure 30-sccm Ar flow for 7 min [12]. Liftoff with N-methyl-2-pyrrolidon was performed in an ultrasonic bath. For ohmic source and drain contacts, an adhesive layer consisting of about 10-nm-thick Pt was primarily sputtered in an Ar atmosphere and subsequently an about 50-nm-thick Au layer was deposited.

For vertical insulation between conduction lines at crossings [see Fig. 1] of inverter devices we used an about 200-nm-thick Si_3N_4 layer grown by plasma-enhanced chemical vapor deposition (PECVD) at 90 °C. To improve the adhesion of the Si_3N_4 layer on the metallic circuit paths, first, an approximately 30-nm HfO_2 layer was sputtered. To remove an incorporation of hydrogen within the nitride insulating layer during the PECVD process, the sample was kept in a vacuum chamber for 12 h at a working pressure of about 10^{-5} mbar. Subsequently, a second HfO_2 coating layer was sputtered on top of the Si_3N_4 layer.

Schlupp *et al.* [3], [23] showed that a thin semi-insulating ZTO layer below the gate contact is capable of strongly decreasing the leakage current of ZTO-based diodes. Therefore, prior to the deposition of the gate contact, an approximately 10-nm thin semi-insulating ZTO layer was sputter-deposited on the ZTO channel layer (see inset of Fig. 3) in a 25/5-sccm O_2/Ar flow atmosphere. The gate contacts of MESFETs consist of 50-nm-thick reactively sputtered PtO_x with a 20-nm-thick Pt-capping layer [24]. Completed devices were not passivated and stored under ambient conditions. For JFET-based devices, an approximately 80-nm-thick NiO gate contact was deposited by pulsed laser deposition at RT and capped with a thin sputtered Au layer [25]. Due to the small hole mobility of the associated NiO layer, it was not possible to determine its hole density with the used Hall measurement setup. Hence, the p-type character was qualitatively confirmed by Seebeck measurements [26].

All measurements were carried out at room temperature without ambient light. Transfer characteristics of FETs were acquired with an integration time of 20 ms per point, the voltage increment was 5 mV. The VTCs of the inverters were measured with an integration time of 0.64 ms per point and a voltage increment of 2 mV.

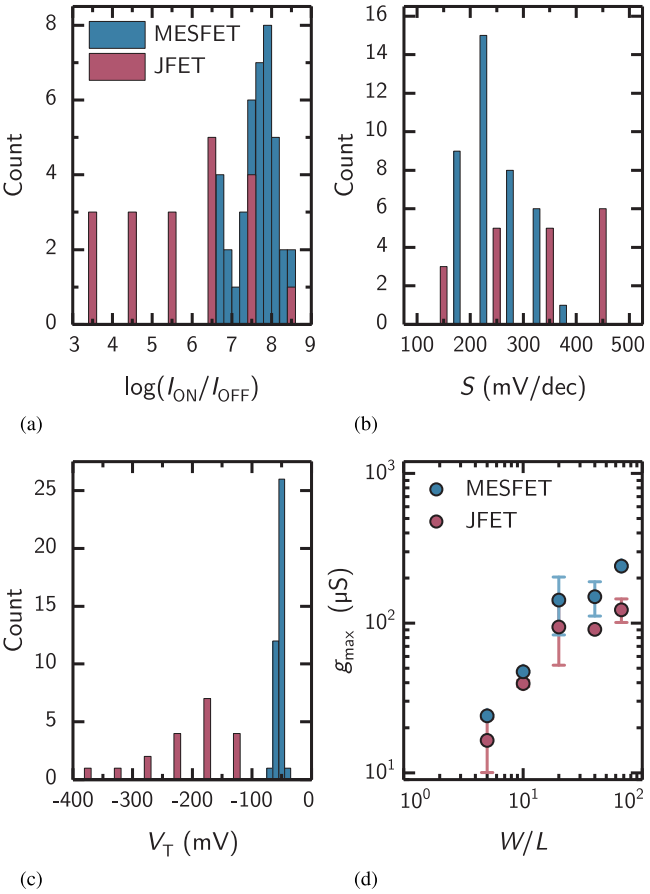

Fig. 4. Histogram of (a) ON-to-OFF current ratio, (b) subthreshold swing S, (c) threshold voltage V_T and (d) W/L scaling behavior of the transconductance g_{max} of ZTO MESFETs and JFETs. V_D of 2 V was used for all measurements.

IV. Results and Discussion

A. Properties of MESFETs and JFETs

Room-temperature transfer characteristics of the best MESFET and JFET are depicted in Fig. 3. Both devices exhibit a clear field effect with ON-to-OFF current ratios of about eight orders of magnitude. The subthreshold swing S and threshold voltage V_T of the MESFET (JFET) are 242 (229) mV/dec and −54 (−224) mV, respectively. The field-effect mobility calculated from the transfer characteristic in the linear region was 5 and 2 cm^2/Vs for the MESFET and JFET, respectively [27]. The mobility results were confirmed by calculations using the net doping density determined from quasi-static capacitance voltage measurements. Concerning the transfer characteristics, it should be noted that the gate leakage current starts to dominate the drain current at applied gate voltages of approximately −1.5 V (−2 V) in case of the MESFET (JFET), which is a common phenomenon for both transistor types. The properties of device ensembles are collected within the histograms of Fig. 4(a)–(d). In average,

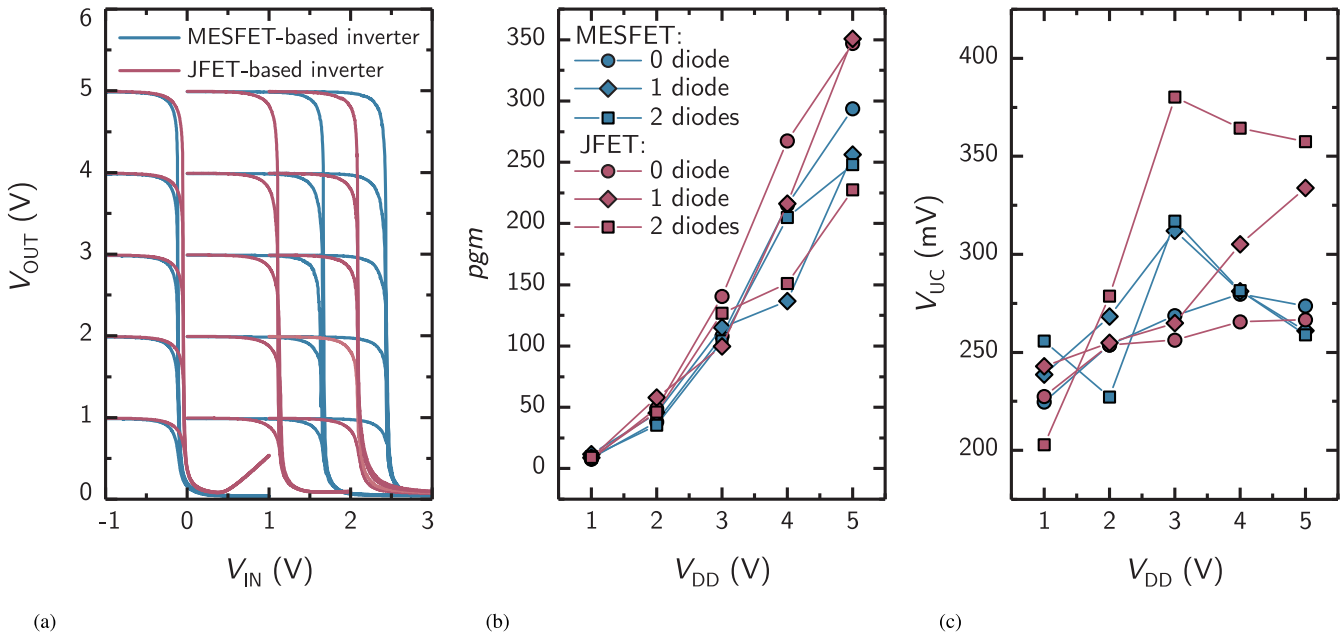

Fig. 5. (a) VTCs of ZTO inverters realized with JFETs or MESFETs using the device design as shown in Fig. 1. Dependence of (b) *pgm* and (c) V_{UC} on V_{DD} for no, one or two level-shifting diodes.

the ON-to-OFF current ratios are for the MESFETs slightly larger and the sub-threshold swings are slightly lower than for the JFET device ensemble. Furthermore, the threshold voltage is significantly higher for the MESFETs indicating that the built-in voltage of the Schottky barrier gate diode is higher than the built-in voltage of the p-n heterodiode gate contact.

Previously reported MESFETs based on ZTO exhibit maximum ON-to-OFF current ratios of 1.8×10^6 and subthreshold swings as low as 124 mV [11], [12]. The results here presented on ON-to-OFF current ratios are as high as those reported for MISFETs with additionally annealed channels at 500 °C [28].

In Fig. 4(d), the scaling behavior of the maximal transconductance g_{max} is depicted for devices with various gate lengths L from 3 to 40 μm and a constant gate width W of 200 μm, resulting in W/L ratios between 5 and 67. The transconductance increases linearly with increasing W/L as expected for channels obtained from the same thin film. Repeated measurements after a period of 200 days prove the long-term stability of the characterized devices concerning their electrical properties and performance. The mean ON-to-OFF current ratio for MESFETs decreases from 7.6 to 6.1 orders of magnitude, while remaining constant for JFET devices with 6.0 orders of magnitude. The average subthreshold swing improves over time for our MESFETs (JFETs) from 241 mV/dec (320 mV/dec) to 210 mV/dec (315 mV/dec). In addition, the threshold voltages partly decrease down to −400 mV (−600 mV).

B. Properties of ZTO Inverters

VTCs of an inverter realized with MESFETs and JFETs, respectively, are depicted in Fig. 5(a) for operating voltages V_{DD} between 1 and 5 V. For $V_{IN} < -0.25$ V, the output voltages correspond for both inverter types to V_{DD} and for $V_{IN} > 0.2$ V the output voltage is close to 0 V. Both device types exhibit full swing. The switching voltages are higher for the JFET-based inverters due to the slightly different threshold voltages of the transistors. We have determined the peak gain magnitude [see Fig. 5(b)], the uncertainty level [see Fig. 5(c)] as well as the noise margins for low (*NML*) and high (*NMH*) input voltage. For all inverters investigated here (level shift not considered), V_{UC} is below 280 mV. The MESFET- and JFET-based inverter exhibit a *pgm* of 294 and 347 at an operating voltage of 5 V, respectively. The higher *pgm* values of the JFET-based inverter can be attributed to the slightly lower slope of the saturation current for the driving and pull-up FET in the case of our JFETs [16], [29].

For cascading of the inverters, a sufficient level shifting of the output voltage is required. We employ the SDFL approach implementing PtO_x/ZTO Schottky barrier diodes in case of the MESFET-based inverters or NiO/ZTO p-n heterodiodes in case of the JFET-based inverters for level shifting. In Fig. 5(b) and (c), we depict the *pgm* and V_{UC} for different V_{DD} of inverters without level-shifting diodes and for inverters connected to one or two level-shifting diodes. The uncertainty level is higher for inverters with level shifting; however, a value of 380 mV is not exceeded for V_{DD} up to 5 V. The *pgm* is independent of the number of level-shifting diodes implemented making both FET types highly suited for cascading within, e.g., ring oscillators. The level shift is larger for the Schottky barrier diodes than for the NiO/ZTO p-n diodes (this is in accordance with the higher threshold voltage observed for the MESFETs). For the MESFET- and JFET-based inverters, the total shift for two diodes is 2.6 and 2.1 V, respectively.

It should be noted that, in both cases, the level shift per diode V_{shift} varies with changing the total number of level-shifting diodes [see Fig. 5(a)]. One reason for this might

TABLE I
COMPARISON OF ZTO-BASED INVERTERS. PROPERTIES OF THE MESFET- AND JFET-BASED INVERTERS ARE PROVIDED FOR THE CASE WITHOUT LEVEL-SHIFTING DIODES. DEPL: DEPLETION TYPE TRANSISTOR. ENH: ENHANCEMENT-TYPE TRANSISTOR. SWCNT: SINGLE WALL CARBON NANOTUBE: SiZTO: SILICON-DOPED ZTO, PHT: POLY-3-HEXYLTHIOPHENE. THE RESULTS IN BRACKETS DENOTE THE VALUES FOR AN OPERATING VOLTAGE OF 5 V

T_{process} (°C)	ZTO FET type	FET 1	FET 2	V_{DD} (V)	V_{UC} (V)	pgm	pgm/V_{DD} (V^{-1})	ref.
450	MISFET	ZTO depl	ZTO enh	10	1.87	10.6	1.1	[8]
–	MISFET	ZTO depl	ZTO enh	10	1.4	9	0.9	[30]
500	MISFET	ZTO enh	ZTO enh	60	> 10	9.9	0.2	[9]
500	MISFET	p-P3HT	n-ZTO	40	> 5	9	0.2	[31]
500	MISFET	p-SWCNT	n-ZTO	4	> 0.6	17.1	4.3	[32]
500	MISFET	ZTO enh	ZTO depl	15	> 0.5	23.2	1.6	[33]
500	MISFET	ZTO enh	SiZTO depl	10	2.4	25.2	2.5	[34]
RT	MESFET	ZTO depl	ZTO depl	3	0.13	119	39.7	[12]
RT	MESFET	ZTO depl	ZTO depl	3 (5)	0.26 (0.27)	108 (294)	58.8	this work
RT	JFET	ZTO depl	ZTO depl	3 (5)	0.25 (0.26)	141 (347)	69.4	this work

be the voltage drop across the voltage divider consisting of a certain amount of level-shifting diodes and the PD FET. On the other hand, the deviations in V_{shift} can be attributed to the contact between conduction path and level-shifting diode in this device layout. The conduction path consists of Au, however, its connection to the level-shifting diode consists of the whole gate-stack, comprising i-ZTO/PtO_x/Pt. As a result, this might prevent an ideal ohmic behavior between these conduction paths.

Hence, for a given number of level-shifting diodes (here one or two) the operating voltage V_{DD} resulting in similar NML and NMH (with desired values of about $V_{\mathrm{DD}}/2$) is different for the MESFET- and JFET-based inverters. In the present case, the optimal driving voltage is about 3 V (5 V) for one (two) level-shifting Schottky diodes and 4 V for two level-shifting p-n diodes. The characteristic parameters of the devices depicted in Fig. 5 are summarized in Table I together with pgm values and uncertainty levels. For $V_{\mathrm{DD}} = 3$ V, the MESFET- (JFET-)based inverter exhibits a pgm of 108 (141). For our devices, we obtain for $V_{\mathrm{DD}} = 5$ V values of $V_{\mathrm{IL}} = 2.29$ V ($V_{\mathrm{IL}} = 1.93$ V) and $V_{\mathrm{IH}} = 2.55$ V ($V_{\mathrm{IH}} = 2.29$ V) for the MESFET- (JFET-)based inverter using two level-shifting diodes.

In Table I, we also compare the parameters deduced for our devices to that of inverters discussed in the literature. The inverters reported here were fabricated at the lowest processing temperature and exhibit by far the highest gain despite operating at lowest supply voltage.

V. CONCLUSION

We have presented properties of amorphous ZTO-based MESFETs and JFETs that were entirely fabricated at temperatures below 110 °C. For both FET types, the maximum ON-to-OFF current ratio was about eight orders of magnitude and the subthreshold swing was as low as 242 mV/dec (229 mV/dec) for the MESFET (JFET). The investigation of ensembles of MESFETs and JFETs showed that in average MESFETs have slightly higher ON-to-OFF current ratios, lower subthreshold swings and higher maximum transconductances. The JFETs exhibit long-term stability after a period of more than 200 days concerning their performance, while in case of the MESFETs, a decrease in current ON-to-OFF ratio as well as reduced threshold voltages are observed. Using both FET types, inverters were fabricated and exhibited values of the peak gain magnitude and the uncertainty level of 294 (347) and 273 mV (266 mV) for MESFETs (JFETs) operating at 5 V. In order to cascade such inverters, level shifting is necessary and was realized here in an SDFL approach. Our inverters displayed stable pgm and V_{UC} values under operation with level shift. Overall, the SDFL design is a promising approach to realize ring oscillators comprising ZTO-based MESFETs or JFETs. In addition, other types of logic gates can be fabricated by simply modifying the featured circuit layout. Since the presented devices were fabricated at temperatures below 110 °C, the realization of bendable circuits is feasible, making ZTO a promising material for green circuitry as well as transparent and even flexible devices.

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ABSTRACT

Recent advances in the field of integrated circuits based on sustainable and transparent amorphous oxide semiconductors (AOSs) are presented, demonstrating ultrahigh performance operating state-of-the-art integrated inverters comprising metal–semiconductor field-effect transistors (MESFETs) with amorphous zinc tin oxide (ZTO) as a channel material. All individual circuit layers have been deposited entirely at room temperature, and the completed devices did not require undergoing additional thermal annealing treatment in order to facilitate proper device functionality. The demonstrated ZTO-based MESFETs exhibit current on/off ratios of over 8 orders of magnitude a field-effect mobility of 8.4 $cm^2\ V^{-1}\ s^{-1}$, and they can be switched within a voltage range of less than 1.5 V attributed to their small subthreshold swing as low as 86 mV $decade^{-1}$. Due to adjustments of the circuit layout and, thus, the improvement of certain geometry-related transistor properties, the associated Schottky diode FET logic inverters facilitate low-voltage switching by exhibiting a remarkable maximum voltage gain of up to 1190 with transition voltages of only 80 mV while operating at low supply voltages ≤3 V and maintaining a stable device performance under level shift. To the best of our knowledge, the presented integrated inverters clearly exceed the performance of any similar previously reported devices based on AOS, and thus, prove the enormous potential of amorphous ZTO for sustainable, scalable low-power electronics within future flexible and transparent applications.

I. INTRODUCTION

Recent developments in the field of active thin-film technology have advanced beyond use in common active-matrix flat-panel display backplanes toward manifold applications, such as photovoltaics and wireless communication systems, as well as memory and sensor elements. Conventionally deployed polycrystalline and amorphous silicon, however, struggles to keep up with the continuously growing demand for scalable electronics operating at higher frequencies, especially when future trends aim for developing mechanically flexible and transparent multifunctional thin-film devices with low power consumption.[1,2] These unique requirements can currently be satisfied using predominantly ZnO-based amorphous oxide semiconductors (AOSs), in particular, indium gallium zinc oxide (IGZO). However, the increasing scarcity and cost of indium and gallium in the context of their high criticality triggered recent efforts to substitute IGZO with the alloy systems composed of naturally abundant elements.[3]

An emerging, yet by far less mature, alternative is amorphous zinc tin oxide (ZTO), since ZTO comprises only earth-abundant as well as non-toxic elements, and it exhibits high transparency in the visible spectral range and facilitates fabrication at room temperature with free-carrier mobilities exceeding 10 $cm^2\ V^{-1}\ s^{-1}$.[4] The first successful integration of ZTO as an active channel material in metal–insulator–semiconductor field-effect transistors (MISFETs) already dates back to 2005, followed by numerous studies reporting on either the sputtered or the solution-processed ZTO thin films and the corresponding devices, such as inverters and ring oscillators.[5] Nonetheless, the majority of previously published results involve high processing temperatures of ZTO or additional

thermal post-deposition annealing treatment to obtain proper device functionality.

As an alternative approach to conventional MISFETs, Dang *et al.* demonstrated the first metal–semiconductor field-effect transistors (MESFETs) based on ZTO in 2017, exhibiting subthreshold swings of only 180 mV decade^{-1} and consequently enabling low-voltage switching due to the absence of a gate dielectric.[6] Even though MISFETs maintain a significantly lower gate leakage current, MESFETs are overall capable of low-voltage operation as well as faster switching, since carrier scattering processes at the channel–insulator interface do not have to be taken into account and, thus, are more suitable for high-frequency applications. Recently, we demonstrated the first room-temperature-fabricated integrated circuits and ZTO-based FETs with even lower subthreshold swings of 61 mV decade^{-1}, approaching the thermodynamic limit and exhibiting high current on/off ratios over 8 orders of magnitude.[7–9] Even though no additional annealing was performed, the corresponding inverters attained full swing and high gain of 347 using a supply voltage of 5 V.

To facilitate potential cascading of multiple inverters containing only unipolar transistors, we used the Schottky diode FET logic approach (SDFL) to obtain a compatible output voltage range required to switch a subsequent inverter. Compared to the complementary metal-oxide-semiconductor (CMOS) logic, based on *p*-type and *n*-type FETs, or direct-coupled FET logic (DCFL), using enhancement and depletion mode transistors, the SDFL inverter requires only one deposition step to prepare both channels of the transistors simultaneously. By employing an improved circuit layout regarding the geometry and, thus, the properties of associated transistors, the presented integrated inverters were capable of exhibiting ultrahigh performance, demonstrating a remarkable, highest yet reported maximum voltage gain of 1190 with a uncertainty level of only 80 mV for a supply voltage of 3 V, resulting in a peak gain magnitude per volt of $pgm/V_{DD} = 397\ V^{-1}$.

II. EXPERIMENTAL

Devices and circuits have been patterned using photolithography with a conventional lift-off process and, thus, were exposed to maximum baking temperatures of 110 °C for no longer than 60 s, required to develop photo-resist structures. ZTO thin films with a cation composition of 1:1 Zn:Sn have been deposited on 10 × 10 mm^2 SiO_2 substrates at room temperature by long-throw radio frequency (RF) magnetron sputtering using a single ceramic target. The sputtering process was ignited in an oxygen-rich atmosphere, inducing oxygen incorporation during thin film growth in order to prevent the formation of a highly conductive electron accumulation layer close to the ZTO-substrate interface that inhibits sufficient depletion of the channel.[7] Subsequently, a conductive ZTO thin film has been deposited on top of the 10 nm thin intrinsic buffer layer ($\rho \gg 10^3\ \Omega$ m). A large target-to-substrate distance of 25 cm has been chosen to enable homogeneous growth and to reduce sputter-induced damage.[10] Information on the layer thickness of ZTO channels have been obtained by performing x-ray reflectivity measurements.

Source and drain contacts consist of ~50 nm Au, deposited by DC sputtering at room temperature. Prior to the gate fabrication, another thin intrinsic ZTO layer has been deposited on top of the active channel to reduce the leakage current through the gate diode by saturating under-coordinated cation bonds due to a transfer of oxygen near the channel surface.[11,12] The metal contacts of the Schottky diodes required for level shifting and transistor gate contacts, consisting of 50 nm PtO_x with a Pt capping layer, have been fabricated in a single deposition process by long-throw RF magnetron sputtering at room temperature. A corresponding schematic cross section through a MESFET, illustrating the basic material stacking order, is depicted Fig. S1(a) in the supplementary material. As a final step, the Pt capping layers of each *i*-ZTO/PtO_x/Pt stack have been directly connected to associated underlying Au conduction paths, for instance, at the inverter input or output, by 10 nm DC sputtered Au in order to obtain ideal ohmic behavior [Fig. S1(b) in the supplementary material].[8] Since the Schottky diodes and unipolar transistor structures are patterned simultaneously, the employed SDFL approach requires the same amount or even less processing steps (five photolithography steps in the present case) compared to the conventional CMOS layout, where the deposition of *n*-type and *p*-type semiconductors, as well as the often required additional thermal annealing step has to be taken into account.

Static current–voltage characteristics were recorded using an *Agilent* 4155*C* semiconductor parameter analyzer and a *SÜSS* wafer prober system. The electrical properties of ZTO thin films have been determined by performing Hall effect measurements in the Van-der-Pauw geometry at room temperature.

III. RESULTS AND DISCUSSION

A. Properties of ZTO-based MESFETs

Static room-temperature transfer characteristics and the corresponding absolute gate leakage currents $|I_G|$ of ZTO/PtO_x-based MESFETs with varying channel thickness d are depicted in Fig. 1. The source–drain voltage was fixed at 2 V for all measurements. The investigated devices contain multi-gate structures with gate lengths of $L = 3\ \mu$m and a total gate width of $W = 400\ \mu$m. A schematic cross section through a MESFET, illustrating the basic material stacking order, is displayed in Fig. S1(a) in the supplementary material. The corresponding electrical properties of each ZTO channel, determined by Hall effect measurements, as well as the associated characteristic transistor parameters are compared within Table I. All MESFETs exhibit a clear field effect with current on/off ratios as high as 8 orders of magnitude and can be switched on and off within a low gate voltage range $\Delta V_G < 2.5$ V, given by the difference between the threshold voltage and the on-voltage, where I_D saturates. By increasing the channel thickness from 9 nm to 13 nm, a significant increase in the on-current, and thus, the maximum transconductance g_{max} from 8 μS to 525 μS is observed, since g_{max} is limited by the channel resistivity and by the leakage current over the gate diode. Simultaneously, the off-current shifts from 8×10^{-13} A ($d = 9$ nm) to 3×10^{-9} A ($d = 13$ nm) due to an increased amount of leakage current flow over the gate diode for gate voltages $V_G \leq -1$ V. All the investigated devices are normally on with the threshold voltages V_T ranging from −380 mV ($d = 13$ nm) to −80 mV ($d = 9$ nm). As expected, V_T shifts toward more negative source–gate voltages with increasing the channel thickness. Consequently, the lowest

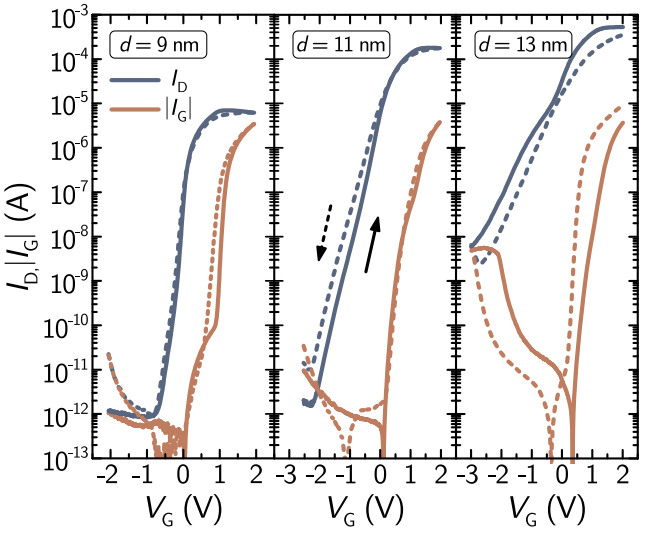

FIG. 1. Room-temperature transfer characteristics (teal) and the corresponding gate leakage currents $|I_G|$ (orange) of ZTO/PtO$_x$-based MESFETs with varying channel thickness d, as labeled. The source–drain voltage was fixed at V_D = 2 V for all measurements. Solid and dashed lines correspond to the voltage sweep direction from negative to positive gate voltages and vice versa, respectively.

subthreshold swing S of 86 mV decade^{-1} is obtained for the MESFET with the lowest channel thickness of 9 nm. A slight dependency of V_T on the voltage sweep direction as well as a crossing of I_D around V_G = 0 V is observable for the majority of measured transistors. This hysteresis is likely to be attributed to the localized states close to the ZTO/PtO$_x$ interface, acting as charge traps.[13] An estimation of the field-effect mobility μ_{FE} was done using the maximum transconductance g_{max}, determined by the channel conductivity and calculated from the transfer characteristics displayed in Fig. 1. The expression $\mu_{FE} = g_{max}L/(endW)$ yields a field-effect mobility of 1.5 cm^2 V^{-1} s^{-1} (d = 9 nm), 6.8 cm^2 V^{-1} s^{-1} (d = 11 nm), and 8.4 cm^2 V^{-1} s^{-1} (d = 13 nm), where e, n, d, and W denote the elementary charge, the charge carrier concentration, the channel thickness of the MESFET, and the gate width, respectively. However, μ_{FE} of only 1.5 cm^2 V^{-1} s^{-1} clearly underestimates the corresponding Hall mobility of 6.7 cm^2 V^{-1} s^{-1} since g_{max} cannot be reached due to limiting effects induced by the increasing gate leakage current occurring for V_G > 1.5 V.

B. Comparison of state-of-the-art inverters based on amorphous ZTO

Figure 2(a) schematically illustrates the circuit layout of an SDFL inverter that is investigated in the present study. The input of the basic inverter configuration, containing a driving (DRV) transistor, responsible for switching, and a pull-up (PU) transistor as load with source and gate shorted, is connected to an additional pull-down (PD) transistor with $\left(\frac{W}{L}\right)_{PD} = \frac{1}{3}\left(\frac{W}{L}\right)_{DRV}$ and three forward-biased n-ZTO/i-ZTO/PtO$_x$/Pt Schottky barrier diodes with an individual area of 450 μm^2 for level shifting in terms of voltage drops across the diodes. V_{GND} = 0 V and V_{DD} denote the constant operating voltages, applied to the ground potential and to the drain side of the PU transistor, respectively. While the DRV transistor has to be provided with a gate voltage $V_G = V_{IN}$ in the range of at least $-V_T \le V_{IN} \le V_{DD} + V_T$ to switch between high and low output levels, the PD transistor is supplied with a negative voltage V_{bias} and serves as a constant-current supply for the diodes. A level shift configuration is necessary to obtain a compatible output voltage range in order to enable the cascading of multiple inverters, for instance, required within ring oscillators or related interconnected logic circuit applications.[14] The geometry ratio between the DRV transistor and the PU transistor is $\beta = (W/L)_{DRV}/(W/L)_{PU}$ = 0.5 for all investigated inverters.

Exemplary voltage transfer characteristics (VTCs) of an SDFL inverter based on MESFETs with a channel thickness of 9 nm and W/L = 67 are depicted in Fig. 2(b). The VTCs approach the applied supply voltages V_{DD} between 1 V and 3 V, and thus, exhibit full swing, even while operating under level shift with up to three diodes connected to the input. V_{bias} was fixed at −2 V, causing the PD transistor to constantly operate in saturation. The VTCs exhibit a shift of the output signal toward positive input voltages by means of the voltage drop V_{shift} across the ZTO/PtO$_x$ diodes. V_{shift} is strongly dependent on the thickness of the ZTO layer, resulting in a voltage shift per diode of 0.3 V, 0.7 V, and 1.5 V for d of 9 nm, 11 nm, and 13 nm, respectively. A slight dependence on the voltage sweep direction is observed for the case without the level shift (not shown); however, the hysteresis of the output voltage remains below 20 mV and can further be reduced by increasing the integration time during the input voltage modulation. Important figures of merit to evaluate the performance of inverters are the maximum gain or the peak gain magnitude $pgm = \max|\partial V_{OUT}/\partial V_{IN}|$ and the uncertainty level V_{UC}, also referred to as the transition voltage, defined as the input voltage difference between the transition points of a VTC where the absolute value of the gain equals unity.

The V_{DD}-dependence of pgm values as well as V_{UC} for all three inverters based on MESFETs with varying channel thicknesses of

TABLE I. Characteristic parameters of ZTO-based MESFETs, depicted in Fig. 1, as well as the electrical properties of the corresponding ZTO channels with various thicknesses d determined by Hall effect measurements at room temperature.

d (nm)	μ_H (cm^2 V^{-1} s^{-1})	n (cm^{-3})	log(I_{ON}/I_{OFF})	S (mV decade^{-1})	g_{max} (μS)	μ_{FE} (cm^2 V^{-1} s^{-1})	V_T (mV)	V_D (V)
9	6.7	2.8×10^{17}	6.9	86	8	1.5	−80	2
11	7.8	1.1×10^{18}	8.1	285	168	6.8	− 180	2
13	8.8	2.2×10^{18}	5.2	526	525	8.4	− 380	2

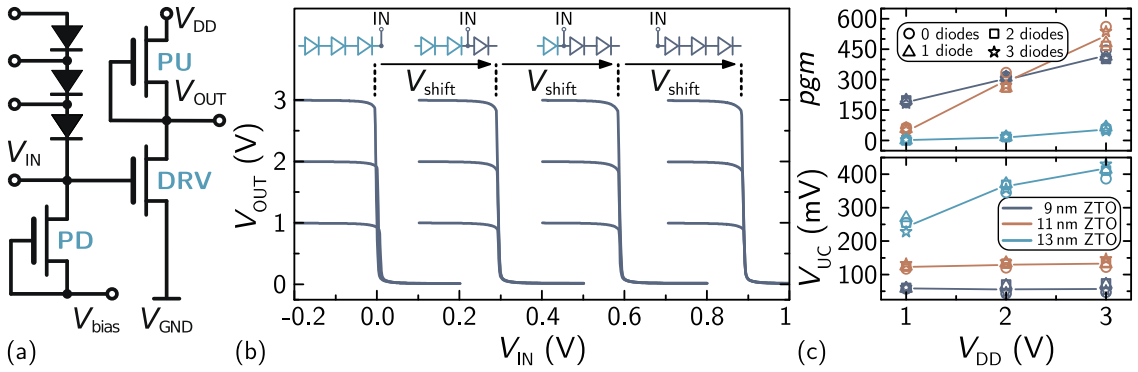

FIG. 2. (a) Schematic basic circuit layout of an SDFL inverter, employing a pull-down transistor (PD) and three ZTO/PtO$_x$ Schottky barrier diodes for the level shifting of the output signal. DRV and PU denote the driving transistor and pull-up transistor, respectively. (b) VTCs of a ZTO-based SDFL inverter without and with a series connection of up to three level-shifting diodes, comprising MESFETs with a channel thickness of 9 nm as well as W/L = 67, and operating at supply voltages V_{DD} between 1 V and 3 V. (c) Behavior under level shift and V_{DD}-dependence of *pgm* values, as well as uncertainty levels (transition voltages) of inverters based on the MESFETs depicted in Fig. 1.

9 nm, 11 nm and 13 nm is depicted in Fig. 2(c) for the case with and without the level shift. All SDFL inverters exhibit reasonable performance stability under level shift; only slight deviations of the *pgm* are observed at V_{DD} = 3 V for a channel thickness of 11 nm. As expected, the *pgm* is clearly dependent on V_{DD} and increases for higher supply voltages. V_{UC}, on the other hand, seems to be unaffected by varying V_{DD}, except for a channel thickness of 13 nm, where the uncertainty level increases from 250 mV (V_{DD} = 1 V) to 400 mV (V_{DD} = 3 V). The highest *pgm* of 560 (V_{DD} = 3 V) is obtained for the inverter with a ZTO channel thickness of 11 nm, while the lowest uncertainty level of 56 mV results for the MESFET-based inverter with a 9 nm ZTO channel, since the corresponding transistors exhibit the by far lowest subthreshold swing and highest threshold voltage. It should be noted that among the three SDFL inverters, the one based on MESFETs with the highest channel thickness of 13 nm, and consequently with the lowest threshold voltage of −380 mV does not quite approach the low output level of 0 V and exhibits a voltage swing of 2.75 V at V_{DD} = 3 V. This is due to the fact that the low threshold voltage causes the PU transistor to increasingly operate in saturation at higher I_D. Consequently, V_{DD} divides over both DRV transistor and PU transistor, even though V_{DD} is supposed to entirely drop across the PU transistor for $V_{IN} \gg 0$ V. Furthermore, the lower V_T for MESFETs with the highest channel thickness explains the smaller gain and the larger transition voltage compared to the other devices with threshold voltages closer to zero. The overall high gain and low transition voltage obtained for the presented inverters results from the high threshold voltage of the MESFETs approaching 0 V as well as the excellent current saturation behavior of $I_{D,sat}$. As soon as V_{DD} is larger than $2|V_T|$, the maximum gain occurs at $V_{DD}/2$ close to $V_{IN} \approx 0$ V and is then determined by the saturation behavior of the drain current of both DRV and PU transistor, given by

$$I_{D,sat} = I_P\left[1 - 3\frac{V_{bi} - V_{IN}}{V_P} + 2\left(\frac{V_{bi} - V_{IN}}{V_P}\right)^{3/2}\right] + \alpha(V_D - V_P + V_{bi}), \quad (1)$$

where the second summand corresponds to an empirical term, describing the non-zero slope of $I_{D,sat}$ with increasing V_D for non-ideal devices.[15,16] In the literature, $\alpha = \partial I_{D,sat}/\partial V_D|_{V_G}$ is often outlined in terms of a finite output resistance r_o^{-1}, modeling the linear dependence of $I_{D,sat}$ on V_D.[17] Thus, V_T close to zero and low α are favorable to obtain high gain within a narrow transition voltage regime.

Recently, we demonstrated the first ZTO-based SDFL inverters comprising ZTO/PtO$_x$ MESFETs, operating at V_{DD} = 3 V with a maximum gain as high as 108 and a transition voltage of 270 mV.[8] Since the previously employed active ZTO channel layers exhibited similar electrical properties compared to the here presented devices, the significant improvement of the inverters with voltage gains exceeding 1000 and V_{UC} below 100 mV is consequently related to performance-enhancing adaptations regarding the circuit layout and the transistor geometry. Unlike the conventional MISFETs, where the source and drain contacts overlap the gate at the edges due to the often preferred bottom-gate layout, MESFETs have a gap between gate and source/drain contacts, denoted by the length Z of the exposed parts of the channel. Z contributes considerably to the series resistances of the channel $R_S = \rho Z/(Wd)$, lowering both the effective drain voltage by $2V_S$ and the gate voltage by V_S due to the voltage drop $V_S = R_S I_D$ across R_S.[35] A decrease of Z from 10 μm to 5 μm for the DRV, PU, and PD transistors, implemented in the presented inverters, consequently yields a significant increase in g_{max}, and thus, a higher current on/off ratio. The smaller voltage drop across Z = 5 μm increases the effective V_D and V_G compared to the transistors with Z = 10 μm. As a result, V_T slightly shifts toward higher gate voltages and an improved subthreshold swing is observable, both of which are desirable to obtain high-gain inverters operating at low voltages. Additionally, a decrease of α from 11 nA/V to 4 nA/V (W/L = 10) by reducing Z from 10 μm to 5 μm is notable. The same applies to higher W/L ratios due to the lowered transconductance and the increased effective channel length for $V_D > V_G - V_T$.[17] Exemplary output characteristics, illustrating the geometry-dependency of α according to Eq. (1), are depicted in Fig. 3 for W/L ranging from 5 to 67.

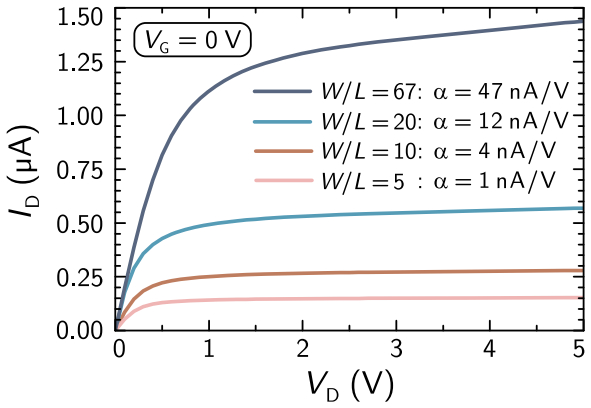

FIG. 3. Output characteristics of MESFETs with various W/L ratios and a channel thickness of 11 nm, recorded at 0 V gate bias. α denotes the non-zero slope of the saturation drain current with increasing V_D, extracted by a linear fit of $I_{D,sat}$.

The previously reported SDFL inverters exhibited a dependence of V_{shift} on the total amount of level-shifting diodes, resulting in a reduction of V_{shift} with an increase in the number of diodes connected to the input.[8] To further improve the former inverter layout, the Pt capping layer of the corresponding gate contacts has been connected to their associated underlying conduction paths using a thin Au layer to bypass the *i*-ZTO buffer as well as PtO_x in order to obtain ideal ohmic connections between conduction paths and gate contacts [Fig. S1(b) in the supplementary material]. The conduction path crossings between V_{DD}, V_{GND}, and V_{bias} have been removed as well to reduce the amount of parasitic capacitances present in the former circuit layout, and thus, to favor the operation at lower voltages (Fig. S2 in the supplementary material).[8] Eventually, the inverters with the adapted circuit layout have been fabricated and are compared regarding the impact of different W/L ratios ($Z = 5$ μm) on the device performance. The resulting *pgm* values and V_{UC} of an SDFL inverter based on MESFETs with a channel thickness of $d = 11$ nm and varying W/L between 5 and 67 are displayed in Fig. 4. A significant improvement of the *pgm* and V_{UC} for lower W/L ratios is observed. The associated drain current saturation behavior in dependence on W/L is depicted in Fig. 4(a) for an ensemble of 20 MESFETs and the corresponding exemplary output characteristics are compared in Fig. 3. Decreasing W/L from 67 to 5 yields a noticeable improvement of α from 47 nA/V to 1 nA/V. The inverters with $W/L = 5$ exhibit a superior voltage gain as high as 1190, and simultaneously an uncertainty level of only 80 mV, which are, to the best of the authors' knowledge, the highest yet reported *pgm* and lowest V_{UC} values for inverters based on any amorphous oxide semiconductor. It should be noted that a slight shift of the VTC toward larger input voltages in the range of 7 μV–30 μV, attributed to the geometry ratio of $\beta = 0.5$, as well as a small dependency on the voltage sweep direction are observable, resulting from the hysteresis of the MESFETs, as depicted in Fig. 1.

To put the obtained results into context, the key properties of all previously published ZTO-based inverters are compared within Table II. The ZTO channels have either been fabricated by RF sputtering or using inkjet-printing and solution-processing techniques. Alongside often required high operating voltages, the majority of the so far reported ZTO-based inverters rely on fabrication-method-related deposition at elevated temperatures exceeding 150 °C or additional thermal annealing to obtain functional devices. A more comprehensive comparison of more than 200 AOS-based inverters reported in the literature has been provided by Schlupp *et al.*[34] To further facilitate performance comparability, the figure of merit pgm/V_{DD} is compared in Fig. 5 for all the devices listed in Table II. The inverters presented in this study attain the highest yet reported *pgm* per V_{DD} of 397 V^{-1}, and thus, represent current state-of-the-art ZTO-based devices.

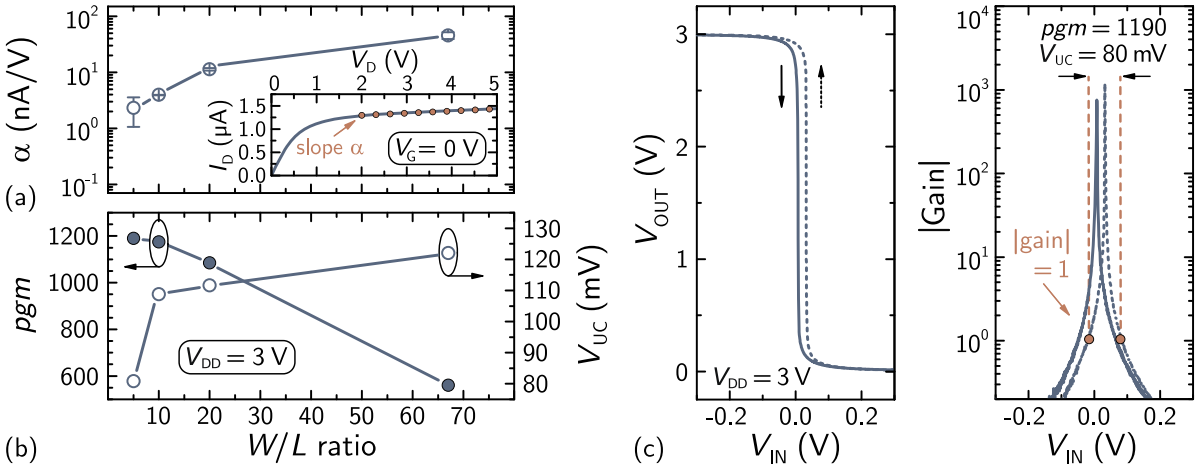

FIG. 4. (a) Impact of the transistor geometry ratio on the drain current saturation behavior as a function of V_D, described by the non-zero slope α and extracted for an ensemble of 20 MESFETs with various W/L. The deviations of α are denoted by the error bars. (b) Dependence of the *pgm* and V_{UC} on the W/L ratio for SDFL inverters implementing MESFETs with a channel thickness of 11 nm, using an operating voltage of $V_{DD} = 3$ V. (c) VTC and the corresponding voltage gain of the best inverter for $V_{DD} = 3$ V, based on MESFETs with $W/L = 5$ and $\alpha = 1$ nA/V.

TABLE II. Comparison of so far published results on ZTO-based inverters. Logic types: CMOS (complementary metal-oxide-semiconductor); SDFL (Schottky diode FET logic); DCFL (direct-coupled FET logic); NMOS (*n*-type metal-oxide-semiconductor). $T_{process}$ corresponds to the maximum temperature during either the deposition process of the ZTO channel or during post-deposition thermal annealing treatment [(RT) room temperature]. Boldface values correspond to the results reported in this work, representing current state-of-the-art inverters based on amorphous oxide semiconductors.

Method	FET type	Logic type	$T_{process}$ (°C)	V_{DD} (V)	*pgm*	V_{UC} (V)	Year	References
RF-sputtered	MISFET	DCFL	425	10	10.6	1.87	2009	18
Inkjet-printed	MISFET	NMOS	500	10	2[a]	>10[a]	2010	19
Sol.-processed	MISFET	DCFL	500	60	9.9	>10[a]	2011	20
RF-sputtered	MISFET	DCFL	425	10	9	1.4	2011	21
Sol.-processed	MISFET	CMOS	500	40	9	>5[a]	2013	22
Inkjet-printed	MISFET	CMOS	200	3	22.8	0.3[a]	2014	23
Inkjet-printed	MISFET	CMOS	500	4	17.1	0.5[a]	2014	24
Inkjet-printed	MISFET	CMOS	500	5	9.3	2[a]	2014	25
Sol.-processed	MISFET	DCFL	500	15	23.2	1[a]	2015	26
Inkjet-printed	MISFET	CMOS	500	5	34[a]	0.5[a]	2015	27
RF-sputtered	MISFET	DCFL	500	10	25.2	2.4	2015	28
Sol.-processed	MISFET	NMOS	350	2.5	11	0.28	2017	29
RF-sputtered	MISFET	NMOS	300	10	3.5	4[a]	2018	30
RF-sputtered	MISFET	NMOS	150	5	5	0.5[a]	2018	31
RF-sputtered	MESFET	NMOS	RT	3	119	0.13	2018	7
RF-sputtered	MESFET	SDFL	RT	5	294	0.27	2019	8
RF-sputtered	JFET	SDFL	RT	5	347	0.26	2019	8
RF-sputtered	MESFET	SDFL	RT	5	83	0.5	2019	14
RF-sputtered	MISFET	CMOS	300	20	4.2	>10[a]	2019	32
Sol.-processed	MISFET	NMOS	520	5	12.1	0.96	2020	33
RF-sputtered	JFET	NMOS	RT	3	464	0.13	2020	34
RF-sputtered	MESFET	SDFL	**RT**	**3**	**1190**	**0.08**	2020	**This work**

[a]Quantitative values have been estimated from figures.

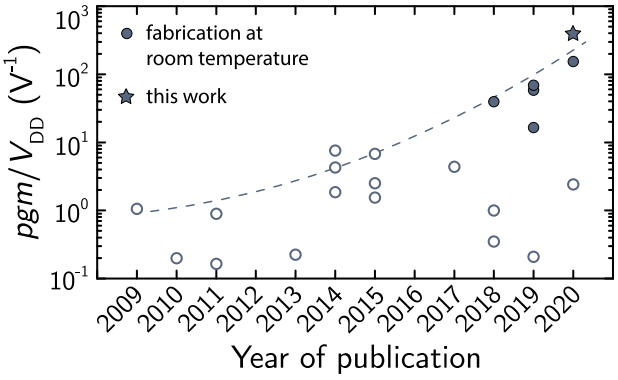

FIG. 5. Comparison of the figure of merit pgm/V_{DD} for the entirety of ZTO-based inverters published so far. Filled symbols correspond to the inverters employing ZTO thin films that have been deposited at room temperature and did not undergo additional thermal annealing to accomplish sufficient device functionality. The dashed line corresponds to the temporal evolution of the overall highest pgm/V_{DD} values per year.

IV. CONCLUSION

The capability of amorphous ZTO to obtain state-of-the-art, ultrahigh-performing integrated inverters based on MESFETs has been demonstrated. Furthermore, all individual implemented thin film layers have been fabricated entirely at room temperature and did not require undergoing post-deposition thermal annealing in order to facilitate sufficient device functionality. To provide the possibility of cascading multiple inverters based on unipolar devices, the SDFL approach has been deployed to maintain a compatible output voltage range by integrating additional ZTO-based Schottky diodes for level shifting.

MESFETs with different ZTO channel thickness have been compared regarding their DC performance, exhibiting current on/off ratios of over 8 order of magnitude and a field-effect mobility of up to 8.4 $cm^2\ V^{-1}\ s^{-1}$. The presented devices operate at low voltage and exhibit a subthreshold swing as low as 86 mV $decade^{-1}$ due to the absence of a gate dielectric. The associated ZTO-based inverters attain remarkable voltage gain of up to 1190 for a supply voltage of 3 V and can be switched within an input transition voltage range of only 80 mV. In contrast, the inverters based on amorphous IGZO so far do not exceed a maximum gain of 226 (V_{DD} = 3 V), while requiring a processing temperature of at least 225 °C.[36] Comparing the figure of merit pgm/V_{DD} with the entirety of the so far published results on the ZTO-based inverters yields the highest yet achieved value for maximum gain per supply voltage of 397 V^{-1} in the case of the here demonstrated devices.

Overall, our results exemplify the enormous potential of amorphous ZTO-based integrated circuits as a promising indium-free

alternative to widely commercially exploited IGZO, even though the conventional IGZO-based transistors and the related integrated circuits are, in addition, typically annealed at temperatures above 150 °C to enhance the device performance. Restriction to room temperature deposition further facilitates the transfer of devices from rigid to thermally unstable, flexible substrates, paving the way for novel transparent, bendable circuitry and sustainable, low-cost applications with reasonable dynamic capability based on amorphous ZTO.

SUPPLEMENTARY MATERIAL

See the supplementary material for a schematic illustration of the basic material stacking order employed in the demonstrated devices as well as laser-scanning microscopy images depicting the circuit design of the presented integrated inverters. Figure S1—Illustration of (a) the basic material stacking order of a ZTO-based MESFET and (b) the schematic cross section through the DRV/PU/PD FET, including an additional Au capping required to bypass the *i*-ZTO/PtO_x layers in order to ensure ideal ohmic behavior between gate contacts and the underlying Au conduction paths. A distance between the conduction path and the channel of 20 μm was chosen to compensate any potential misalignment during photolithographic patterning. Figure S2—Microscopic image of (a) the here presented integrated SDFL inverter layout and (b) the former circuit design,[8] implementing the conduction path crossings insulated by a 200 nm HfO_y layer that appears bluish and yellowish due to thin film interferences. (c) Depiction of the corresponding SDFL circuit schematic of both inverters.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Ultrahigh-performance integrated inverters based on amorphous zinc tin oxide deposited at room temperature

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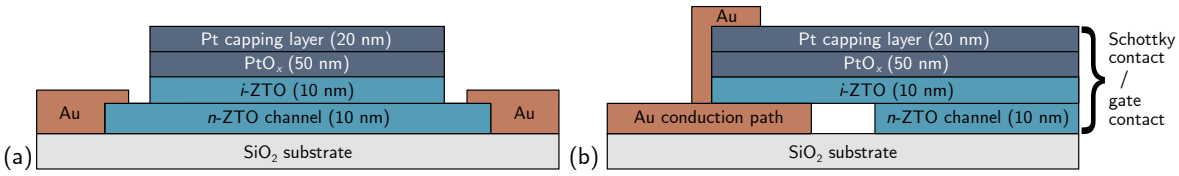
Supporting Information



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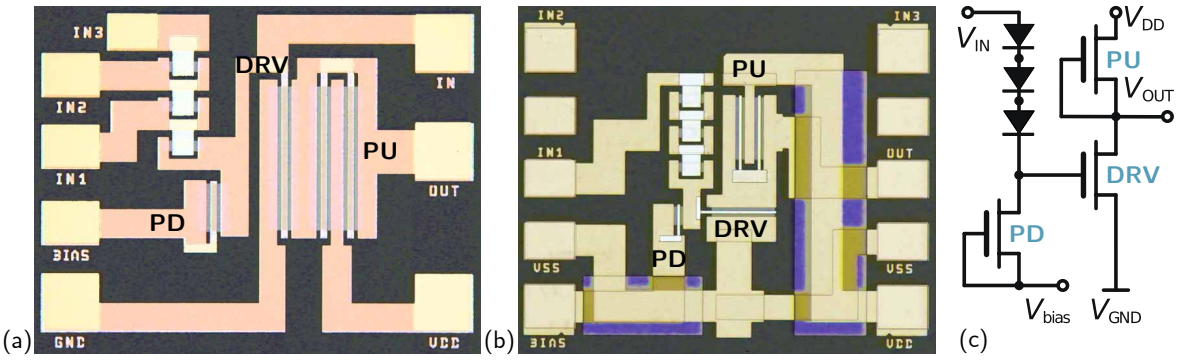

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Low-Voltage Operation of Ring Oscillators Based on Room-Temperature-Deposited Amorphous Zinc-Tin-Oxide Channel MESFETs

Oliver Lahr, Sofie Vogt, Holger von Wenckstern, and Marius Grundmann*

Schottky diode FET logic (SDFL) ring oscillator circuits comprising metal-semiconductor field-effect transistors (MESFETs) based on amorphous zinc-tin-oxide (ZTO) *n*-channels are presented. The ZTO channel layers are deposited entirely at room temperature by long-throw magnetron sputtering. Best MESFETs exhibit on/off current ratios as high as 8.6 orders of magnitude, a sub-threshold swing as low as 250 mV dec^{-1}, and a maximum transconductance of 205 µS. Corresponding inverters show peakge gain magnitude (*pgm*) values of 83 with uncertainty levels as low as 0.5 V at an operating voltage of 5 V. Single stage delay times down to 277 ns are measured for three-stage ring oscillators, corresponding to oscillation frequencies as high as 451 kHz. Oscillations are observed at operating voltages as low as 3 V. These results prove the feasibility of room-temperature-deposited, amorphous semiconducting oxide based integrated circuits with SDFL layout. The presented approach provides more efficient as well as fail-safe device fabrication and similar oscillation frequencies at significantly lower operating voltages compared to conventional, high-temperature processed logic circuits based on insulating gates.

1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) exhibit remarkable transport properties despite their disordered structure.[1] Additionally, their high transparency in the visible range associated with the possibility of large-area deposition at low temperatures enables the cost-efficient fabrication of transparent and even bendable circuits. For instance, the TAOS indium-gallium-zinc-oxide (IGZO) is already commercially exploited, however, ongoing research is targeting toward replacing elements such as indium and gallium by abundant elements.[2] One promising material for sustainable, green circuitry is the TOAS zinc-tin-oxide (ZTO) since it can be deposited at room temperature (RT) enabling the low-cost fabrication of transparent, flexible circuits.[3,4]

So far, several ZTO-based metal-insulator field-effect transistors (MISFETs) and related inverters have been reported in the literature, however, those devices required a deposition at elevated temperatures or post-growth annealing processes in order to perform well.[5–7] Reports on associated integrated circuits comprising ZTO MISFETs are restricted to thin film transistor (TFT) logic technology, based on depletion and enhancement transistors, as well as complementary metal oxide semiconductor logic technology, requiring compatible p-type and n-type FETs. Further, an additional fabrication step is necessary for the preparation of the gate insulator. Such MISFETs and related integrated circuits usually require high operating voltages due to the voltage drop across the insulator as well as a limited switching speed due to carrier scattering at the channel-insulator interface.[8] Previously reported ZTO-based ring oscillators, consisting of five or seven stages, exhibited oscillation frequencies between 0.85 and 800 kHz at operating voltages ranging from 5 to 60 V.[9–11] Single stage delay times, resulting in oscillation frequencies compatible with an ISM band, have so far not been reported for ZTO-based ring oscillators.

Recently, first metal-semiconductor field-effect transistors (MESFETs) and simple inverter circuits, comprising depletion-type MESFETs based on room temperature-deposited ZTO channel layers, have been reported.[12,13] Concerning device performance and fabrication efficiency, the absent gate insulator in case of MESFETs enables improved switching behavior as well as more fail-safe and faster processing. However, in case of inverters consisting of depletion-type FETs only, a shifting of the output signal is necessary to cover the voltage range required for switching a subsequent inverter. In the current work, we employ the Schottky diode FET logic (SDFL) approach that facilitates a sufficient level shift of the inverters output signal to enable a successful cascading of a series connection of inverters (see **Figure 1**). Since the SDFL layout consists of unipolar devices only, transistor channels can be deposited using a single photolithographic patterning process.

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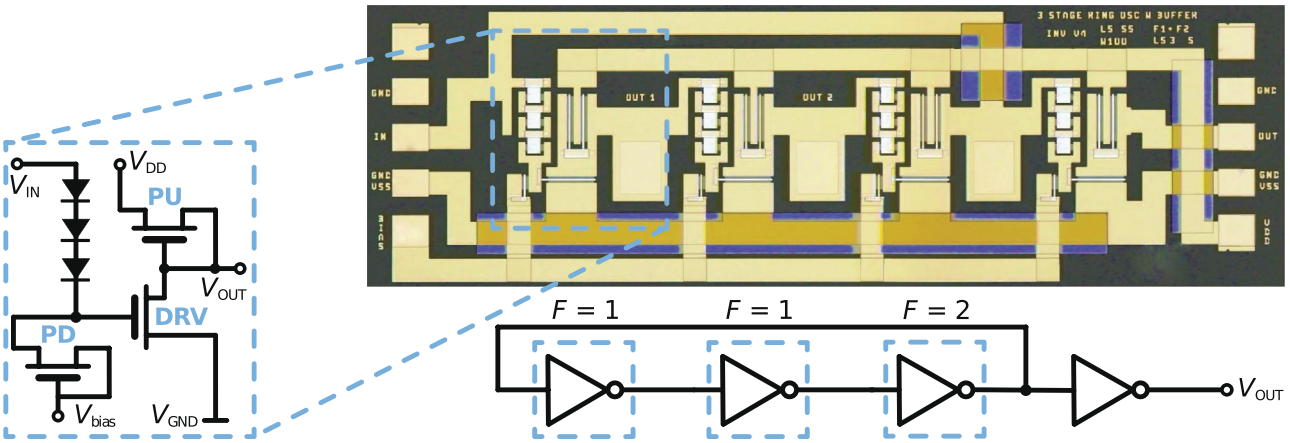

Figure 1. Microscopic image and the corresponding circuit schematic of a three-stage ring oscillator including an additional inverter for signal out-coupling as well as the basic circuit schematic of an SDFL inverter stage. *F* denotes the fan-out of the respective stages. DRV, PU, and PD mark the driving transistor, pull-up transistor, and pull-down transistor, respectively. Insulating HfO_2 layers between conduction path crossings appear orange and bluish due to thin film interference.

2. Results and Discussion

The static RT current–voltage characteristics of a ZTO-based MESFET as well as a schematic cross section through a MESFET sample, illustrating the basic material stacking order, are depicted in **Figure 2**. The gate width W and gate length L are 200 µm and 3 µm, respectively. Figure 2a displays the transfer characteristic as well as the gate leakage current for both voltage sweep directions. The MESFET exhibits a clear field effect with an on/off current ratio of 8.6 orders of magnitude and can be switched on and off within a voltage range of 3 V. The obtained sub-threshold swing and maximum transconductance are 250 mV dec^{-1} and 205 µS, respectively. A channel mobility of ≈1.8 cm^2 V^{-1} s^{-1} has been calculated using the relation $\mu = g_{max}L/(eWnd)$. g_{max} denotes the maximum transconductance derived from the transfer characteristic and the free-carrier density of $n = 4.3 \times 10^{18}$ cm^{-3} was determined by Hall effect measurements. It should be noted the channel mobility clearly underestimates the free-carrier mobility of $\mu_H = 5.4$ cm^2 V^{-1} s^{-1}, obtained from Hall effect measurements, and hence has to be understood as a lower mobility limit, since the maximum transconductance cannot be determined due to the influence of gate leakage currents for positive gate voltages. The investigated MESFETs are normally-on with threshold voltages ranging from −0.6 to −0.3 V. Further, all investigated devices show a hysteresis of the drain current, especially for low gate voltages. The transfer characteristics obtained for different bias sweep directions cross around V_G = 0 V. This dependence on the sweep direction can be attributed to localized states at the interface between the amorphous channel and the gate contact acting as charge traps. A similar effect has already been reported for ZnO-based junction field-effect transistors (JFETs) with amorphous $ZnCo_2O_4$ gates.[14,15]

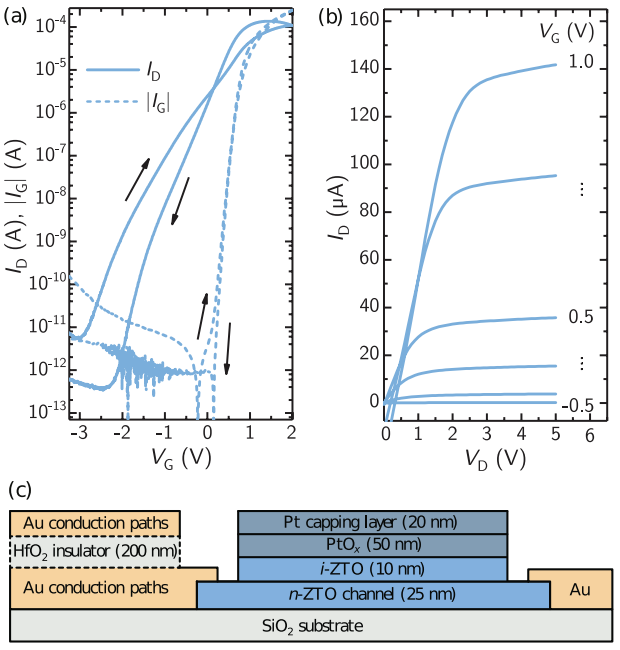

Figure 2. Room temperature current–voltage characteristics of a typical ZTO-based MESFET device with a gate width-to-length ratio of W/L = 200 µm/3 µm. a) Transfer characteristic and the corresponding gate leakage current, each for a voltage sweep direction from negative to positive and vice versa. b) Output characteristics for various gate voltages V_G. c) Depicts a schematic cross section through a MESFET sample visualizing the basic material stacking order that is present in all investigated devices.

Corresponding output characteristics for various gate voltages are depicted in Figure 2b. It is notable that the current does not fully saturate with further increasing the source-drain voltage. At V_G = 0 V, which corresponds to the operational state of the pull-down transistor and pull-up transistor within the SDFL circuits (see Figure 1), the drain current increases with a slope of 0.15 µA V^{-1}. The shift of the output characteristic for V_G > 0.5 V is caused by an increased leakage current flow over the gate diode and is a common phenomenon for MESFETs.

An essential step toward the realization of ring oscillators are investigations on the cascadability of the respective inverters. Here, we employ the SDFL approach that has already been

successfully demonstrated for ZTO-based inverters comprising depletion-type MESFETs and JFETs.[16] To achieve compatible output and input voltage levels, our SDFL circuits implement PtO_x/*i*-ZTO/ZTO Schottky barrier diodes for shifting of the output voltage by means of a voltage drop across the diodes in order to switch a subsequent inverter. In addition to these diodes, the level shift configuration contains a transistor with its gate and source shorted, as depicted in Figure 1. This transistor is supplied with a negative operating voltage V_{bias} and acts as constant-current bias source for the level shifting diodes, hence the denotation pull-down transistor.

Voltage transfer characteristics (VTCs) of a ZTO-based SDFL inverter without and with three level shifting diodes are depicted in **Figure 3**a for operating voltages V_{DD} between 1 and 6 V. The pull-down transistor was supplied with a negative voltage of $V_{bias} = -2$ V for all measurements. The gate width and length of the associated driving and pull-up transistor are 100 µm and 5 µm, respectively, while the pull-down transistor has a gate width-to-length ratio of 30 µm/5 µm. For negative input voltages, the output voltage approaches V_{DD}. In the on-state of the driving transistor, the output voltage is still 0.5 V rather than the expected ground potential of 0 V. This can be attributed to the low threshold voltage, causing the pull-up transistor to increasingly operate in the saturation regime at higher I_D. Consequently, V_{DD} partly drops across the pull-up transistor and the driving transistor, resulting in a decreased logic swing. Full-swing ZTO-based inverters with sufficient level shift have previously been achieved using MESFETs and JFETs with threshold voltages approaching 0 V.[16] However, a decreased logic swing does not affect the cascadability of SDFL inverters as long as the total level shift V_{shift} is sufficiently high. Further, the output voltage of the VTCs without level shift starts to increase once V_{IN} exceeds 0.8 V due to current flow over the forward-biased gate diode. Characteristic parameters of the VTCs such as the peak gain magnitude (*pgm*), that is, the maximum gain, and the uncertainty level V_{UC} are depicted in Figure 3a and have been determined for various operating voltages. The *pgm* can be calculated as $\max|\partial V_{OUT} / \partial V_{IN}|$. V_{UC} is defined as the difference between both input voltages, where the gain equals –1. The presented inverter exhibits a *pgm* and V_{UC} (level shift not considered) of 83 and 0.5 V for $V_{DD} = 5$ V, respectively. Regarding the shifted VTCs in Figure 3a, a total voltage shift of $V_{shift} = 2.25$ V is obtained for three level shifting diodes. In this case, the *pgm* slightly decreases to 75, whereas V_{UC} remains 0.5 V at an operating voltage of 5 V. Previously reported ZTO-based SDFL inverters, comprising MESFETs, exhibited a remarkable *pgm* of 294 at $V_{DD} = 5$ V.[16] This significant discrepancy in maximum gain can be attributed to the voltage dependency of the saturation current of the pull-up transistors and driving transistor at $V_G = 0$ V for our devices (see Figure 2b).[17,18]

Furthermore, we investigated the cascadability of our SDFL inverters within inverter chains consisting of four series-connected stages. Each SDFL inverter stage consists of three diodes for level shifting. For cascading of these inverters, V_{IN} was applied at the input of the first inverter while V_{OUT} was measured at the output of the last inverter stage. The corresponding VTCs are depicted in Figure 3b for various operating voltages and exhibit the expected inverting behavior. V_{DD} ranges from 3 to 5 V and V_{bias} was fixed at –2 V. Due to an observed level shift of approximately $V_{shift} = 2.5$ V, operating voltages of $V_{DD} \leq 2.5$ V result in incompatible output driving voltages that do not match the input voltage range. Hence, a successful cascading with inverting behavior was only achieved for operating voltage of $V_{DD} > V_{shift}$. As expected, it was also observed that the VTCs become significantly steeper the more inverter stages are connected within the chain. In case of four series-connected inverters, the *pgm* increases up to 700 while simultaneously uncertainty levels as low as 0.08 V are obtained for $V_{DD} = 5$ V.

Measured frequencies as a function of V_{DD} as well as the typical time trace of a three-stage ZTO-based SDFL ring oscillator are depicted in **Figure 4**. The FET geometry of W/L = 100 µm/5 µm is analogous to the presented inverter circuits. A

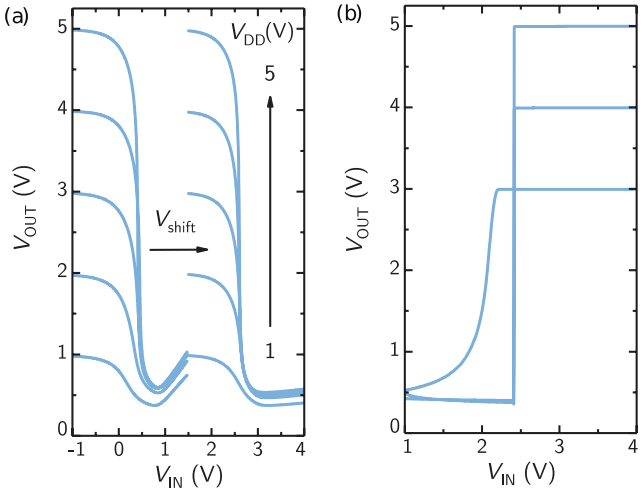

Figure 3. a) VTCs of an SDFL inverter with no level-shifting diodes as well as three level-shifting diodes based on the circuit schematically depicted in Figure 1. The gate width-to-length ratio of the driving transistor and pull-up transistor is 100 µm/5 µm. The operating voltage of the pull-down transistor is fixed at $V_{bias} = -2$ V, while the pull-up transistor is supplied with operating voltages ranging from 1 to 5 V. b) Associated VTCs of an inverter chain consisting of four SDFL inverters. Three-level shifting diodes are implemented at the input of each inverter to adjusting the output driving voltage in order to switch the subsequent inverters.

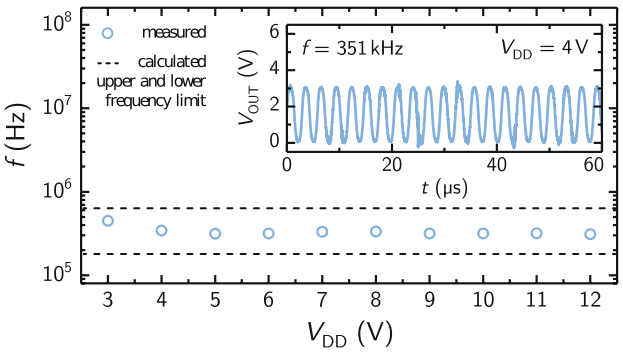

Figure 4. Oscillation frequencies of a typical ZTO-based three-stage ring oscillator dependent on the applied operating voltage V_{DD}. The dashed lines mark the expected frequency range that was calculated based on related FET and inverter parameters, using Equation (1). The inset displays an example for a measured time trace of a ring oscillator at V_{DD} = 4 V, exhibiting an oscillation frequency of 351 kHz with an output voltage ranging from 0 to 3.2 V.

maximum oscillation frequency of 451 kHz is observed at V_{DD} = 3 V, corresponding to single stage delay times of 277 ns. Oscillations start to occur at a minimum operating voltage of 3 V, which is attributed to the voltage drop V_{shift} across the level shifting diodes. For $V_{DD} < V_{shift}$, no oscillations are observed since the output voltage range does not match the input voltage range of the subsequent inverter. Within the operating voltage range of approximately $V_{shift} < V_{DD} < V_{shift} + 1$ V, a shift in the frequency can be observed for most of the investigated devices, which has also been reported for ZnO-based SDFL ring oscillators.[19] For $V_{DD} \geq V_{shift} + 1$ V, the observed frequencies of ≈350 kHz stay constant as expected for SDFL circuits, since the supply current is limited by the pull-up and pull-down transistors which operate in saturation and act as constant current sources.

Klüpfel et al. developed an analytical model to estimate the single stage delay time τ_D based on easily obtainable FET and inverter quantities.[19] τ_D was calculated using the relation

$$\tau_D = \frac{\Delta V C_G}{I_{PU}} F \quad (1)$$

where C_G, I_{PU}, and F are the driving gate capacitance, the saturation current of the pull-up FET, and the fan-out, respectively.[19] $\Delta V = V_{shift}/N_{diode} - V_{bias}$ denotes the voltage swing which is present at the input of each driving gate. N_{diode} is the number of implemented level shifting diodes. If the previous inverter within the cascaded chain drives F gates, the maximum supply current available for recharging of gate capacitances is I_{PU}/F. Since the presented ring oscillator circuits consist of (N–1) inverter stages with $F = 1$ and one inverter stage with $F = 2$ (see Figure 1), the oscillation frequency can be estimated by the relation $f = (2(N+1)\tau_D{}^{F=1})^{-1}$.[19]

The results in terms of expected maximum and minimum oscillation frequencies are represented by the dashed lines in Figure 4. The scattering of calculated frequencies results from variations of the device properties across the sample. C_G was constant and ≈15 pF and ΔV was determined from the VTCs of the corresponding inverters. I_{PU} ranged from 50 to 200 µA, resulting in estimated oscillation frequencies between 170 and 670 kHz. The slight deviations in observed frequencies for various V_{DD} can be attributed to the saturation current dependence on the source-drain potential.

3. Conclusion

In summary, we have realized ring oscillators comprising MESFETs based on room-temperature-deposited amorphous zinc-tin-oxide. Oscillation frequencies up to 451 kHz with single stage delay times of 277 ns have been observed for three-stage ring oscillators with W = 100 µm and L = 5 µm at V_{DD} = 3 V and V_{bias} = −2 V. Demonstrated ring oscillators operated at voltages as low as 3 V, which is significantly lower compared to previously reported high-temperature processed, ZTO-based three-stage ring oscillators, exhibiting similar single stage delay times at V_{DD} between 8 and 60 V.[9,10] In case of amorphous IGZO, similar single stage delay times have been achieved for TFT-based ring oscillators, operating at V_{DD} between ≈8 and 80 V.[20–25]

Since the single stage delay time of SDFL circuits is strongly dependent on device layout parameters, high-frequency circuits at low operating voltages based on amorphous semiconducting oxides are feasible. By scaling down the gate length by a factor of 10 (leading to a gate length of 0.5 µm) using state-of-the-art photolithographic patterning techniques, an increase of oscillation frequencies up to 100 times higher is expected due to the linear dependency of the gate length on the driving gate capacitance as well as the total driving current. To operate in the desired ISM band frequency range of for instance 13.56 MHz, a reduction of the gate length to ≈0.4 µm (under otherwise constant device parameters) is necessary.

Overall, the presented results prove that room-temperature-deposited amorphous ZTO is a suitable candidate for more cost-efficient, sustainable green circuitry, and an indium-free and gallium-free alternative to the commercially exploited, far more mature amorphous representative IGZO. Furthermore, it was shown that low-temperature-processed ZTO thin films and associated integrated circuits can compete with previously reported high-temperature-treated devices concerning their performance. Additionally, room-temperature-deposited of entire device structures offers the possibility of utilization of organic substrates, allowing the realization and investigation of flexible and even transparent integrated circuits.

4. Experimental Section

The integrated circuits presented in this study comprise MESFETs based on amorphous *n*-ZTO channels fabricated by radio frequency, long-throw magnetron sputtering. To ensure amorphous growth, the ZTO thin films were deposited at RT using a ceramic target with a 33 wt% ZnO and 67 wt% SnO_2 composition.[4] A comparatively large target-to-substrate distance of 25 cm was chosen to prevent the impingement of high energetic particles and droplets allowing growth of homogeneous thin films without sputter induced damage. All thin films were deposited on 10×10 mm^2 SiO_2 substrates. Since all thin films were deposited at RT, photolithography was used for patterning of transistor structures as well as inverters and ring oscillator circuits.

Previous investigations on ZTO-based MESFETs indicated the formation of a highly conductive layer at the interface close to the substrate, preventing a sufficient depletion of the channels.[13] Thus, ZTO mesa structures were deposited in two steps: first the sputtering process was ignited in a 25/30 sccm O_2/Ar flow atmosphere and subsequently an ≈13 nm thick conductive ZTO layer was sputter-deposited under pure argon flow, resulting in a nominal thickness of 25 nm. The basic material stacking order that was present in all investigated devices is illustrated in **Figure 2**c. The channel fabrication step was followed by the deposition of source and drain contacts, using DC-sputtered Au. Between the two necessary SDFL design-related metallization steps, a 200 nm thick insulating HfO_2 layer was deposited at RT. This insulating layer has also been used to realize multi-gate FET structures, that were implemented in inverters and ring oscillator circuits to increase the maximum current flow through the channel. The gate contact was deposited in a single final step. Reactive sputtered PtO_x with a Pt capping was used as gate material to reduce the free-carrier density close to the ZTO/PtO_x interface due to a saturation of under-coordinated cation bonds via transfer of oxygen from PtO_x to ZTO.[26] The resulting increase in depletion layer width leads to a decrease in tunneling current through the gate diode. Schlupp et al. showed that an additional thin intrinsic ZTO layer (*i*-ZTO) between channel and gate contact significantly enhances this effect without affecting the device properties otherwise.[2,27] Hence, an ≈10 nm thin *i*-ZTO layer was sputtered underneath the gate contact and on top of the conducting ZTO channel in a 25/5 sccm O_2/Ar atmosphere

prior to the deposition of the PtO_x/Pt gate contact. Eventually, all gate contacts and their corresponding conduction paths were shorted by a final deposition of a thin Au layer in order to obtain ideal ohmic behavior within the circuits.

Current–voltage measurements and quasi-static capacitance-voltage measurements were carried out using an *Agilent* 4155*C* semiconductor parameter analyzer to obtain static current–voltage characteristics and the driving gate capacitance C_G, respectively. The capacitance values, necessary for calculating the single stage delay times of the presented ring oscillators, were estimated for gate voltages between 0 and –0.5 V where the capacitance was nearly constant. All measurements were performed in the dark at ambient temperature. Electrical parameters of the ZTO channel layers such as the free-carrier concentration of $n = 4.3 \times 10^{18}$ cm^{-3} and a free-carrier mobility of $\mu_H = 5.4$ cm^2 V^{-1} s^{-1} were determined by Hall effect measurements. Voltage oscillations of the presented ring oscillators were recorded using a *Tiepie Engineering Handyscope HS3* oscilloscope. For signal outcoupling, a high input impedance active probe by GGB Industries Inc. was used to connect the output of ring oscillators to the input of the oscilloscope.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

abundant, ring oscillators, Schottky diode FET logic, transparent amorphous oxide semiconductors, zinc-tin-oxide

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8 Mechanically flexible devices

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Mechanical Stress Stability of Flexible Amorphous Zinc Tin Oxide Thin-Film Transistors

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Due to their low-temperature processing capability and ionic bonding configuration, amorphous oxide semiconductors (AOS) are well suited for applications within future mechanically flexible electronics. Over the past couple of years, amorphous zinc tin oxide (ZTO) has been proposed as indium and gallium-free and thus more sustainable alternative to the widely deployed indium gallium zinc oxide (IGZO). The present study specifically focuses on the strain-dependence of elastic and electrical properties of amorphous zinc tin oxide thin-films sputtered at room temperature. Corresponding MESFETs have been compared regarding their operation stability under mechanical bending for radii ranging from 5 to 2 mm. Force-spectroscopic measurements yield a plastic deformation of ZTO as soon as the bending-induced strain exceeds 0.83 %. However, the electrical properties of ZTO determined by Hall effect measurements at room temperature are demonstrated to be unaffected by residual compressive and tensile strain up to 1.24 %. Even for the maximum investigated tensile strain of 1.26 %, the MESFETs exhibit a reasonably consistent performance in terms of current on/off ratios between six and seven orders of magnitude, a subthreshold swing around 350 mV/dec and a field-effect mobility as high as 7.5 $cm^2V^{-1}s^{-1}$. Upon gradually subjecting the transistors to higher tensile strain, the channel conductivity steadily improves and consequently, the field-effect mobility increases by nearly 80 % while bending the devices around a radius of 2 mm. Further, a reversible threshold voltage shift of about −150 mV with increasing strain is observable. Overall, amorphous ZTO provides reasonably stable electrical properties and device performance for bending-induced tensile strain up to at least 1.26 % and thus represent a promising material of choice considering novel bendable and transparent electronics.

Keywords: zinc tin oxide, amorphous oxide semiconductor, flexible electronics, transparent electronics, sustainable, abundant, MESFETs, thin-film transistors

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1 INTRODUCTION

With the rapid evolution of active-matrix flat-panel display technology, significantly advanced by the replacement of commonly deployed silicon by indium gallium zinc oxide (IGZO) approximately a decade ago, amorphous oxide semiconductors (AOS) have considerably gained interest leading to the development of a distinct, thriving research area (Hosono, 2018). The continuously growing demand for scalable electronics, requiring low power consumption and high-frequency operation capability, however, has triggered recent efforts to substitute scarce materials such as IGZO by

compounds comprising earth-abundant elements only. Amorphous zinc tin oxide (ZTO) represents such a viable choice regarding a more sustainable and cost-efficient approach to transparent as well as bendable electronics, attributed to the possibility of room-temperature fabrication combined with its reasonably high charge carrier mobility exceeding $10\,cm^2V^{-1}s^{-1}$ for thin-films deposited at room temperature (Schlupp et al., 2013).

Even though ZTO appears to be a suitable candidate for use in flexible device building blocks, the vast majority of previously published issues covering ZTO based devices primarily report metal-insulator field-effect transistors (MISFETs) fabricated on rigid substrates. Only a few flexible devices implementing ZTO have so far been demonstrated, including MISFETs fabricated between 180°C and 300 °C and junction field-effect transistor (JFET) based inverters (Jackson et al., 2005; Jackson et al., 2006; Fernandes et al., 2018; Lee et al., 2018; Schlupp et al., 2020). Over the past couple of years, JFET and especially metal-semiconductor field-effect transistor (MESFET) technology has proven to be a viable approach to obtain high-performance ZTO based electronics providing both low-power operation and fabrication at room temperature (Dang et al., 2017; Vogt et al., 2018; Lahr et al., 2019a; Lahr et al., 2020a). Further, the successful implementation of amorphous ZTO within integrated circuits such as logic inverters and ring oscillators yielded a remarkable voltage gain as high as 1190 as well as single stage delay times as low as 277 ns, respectively, rendering amorphous ZTO a reasonable competitor within the scope of future AOS based electronic applications (Lahr et al., 2019b; Lahr et al., 2020b).

This study focuses on evaluating the effect of bending-induced strain on the properties of amorphous ZTO thin-films as well as the limits to excessive bending stress on the performance of ZTO based MESFETs. Performing force-distance measurements with bent samples enabled the *in-situ* investigation of the elastic behavior of ZTO in dependence on the induced strain. Additionally, the effect of residual compressive and tensile strain on the electrical properties of ZTO thin-films has been determined by Hall effect and conductivity measurements at room temperature, while the sample was subjected to bending-induced mechanical stress in between measurements. Finally, the performance of ZTO/PtO_x based MESFETs and associated transistor parameters have been studied regarding their stability under tensile strain up to $\varepsilon = 1.26\,\%$, corresponding to a bending radius of 2 mm.

2 MATERIALS AND METHODS

ZTO thin-films with a cation composition ratio of 1:1 Zn:Sn have been deposited by RF magnetron sputtering on 50 μm thick polyimide substrates using a single ceramic target. To maintain compatibility with the limited thermal stability of common organic substrates, the deposition temperature has been restricted to room temperature while the processing temperatures associated with photoresist developing during photolithographic patterning did not exceed 110 °C. Prior device fabrication, 50 µm thick polyimide substrates (DUPONT KAPTON E and KOLON CPI) were preshrunk under vacuum atmosphere at 200 °C for 24 h and have then been sonicated in acetone and isopropanol (Münzenrieder et al., 2011). Photolithographic patterning has been performed using a HEIDELBERG µMLA direct laser writing lithography system with AZ 1514H photoresist and AZ 351B developer (both from MICROCHEMICALS), followed by a conventional ultrasonic lift-off process using N-methyl-2-pyrrolidon.

The ZTO sputtering process has been ignited in oxygen-rich atmosphere to grow a 10 nm thin intrinsic layer (*i*-ZTO) underneath the conductive *n*-ZTO channel in order to compensate electron accumulation at the interface by inducing oxygen incorporation and thus enabling sufficient channel depletion (Vogt et al., 2018). Ohmic source and drain contacts consist of 30 nm DC sputtered Au. MESFET gates have been deposited in a single final step, comprising 10 nm *i*-ZTO as well as 150 nm PtO_x capped with 30 nm Pt. Again, the thin semi-insulating *i*-ZTO layer between channel and gate significantly improves the device performance in terms of reducing the gate leakage current by saturating under-coordinated cation bonds due to oxygen transfer in the vicinity of the channel surface. Despite being intrinsically undoped and thus way less conductive $\rho > 10^3\,\Omega m$), the *i*-ZTO layer, however, does not induce a conduction band offset. In fact, the ZTO/*i*-ZTO contact forms rather an n/n^- type of junction with decreasing net doping density toward the metal interface. Previous investigations of corresponding Schottky barrier diodes yield the effective barrier height to be independence of *i*-ZTO being embedded between ZTO and PtO_x (Schlupp et al., 2015; Schlupp et al., 2017).

Electrical properties of ZTO thin-films have been determined by Hall effect measurements at room temperature. Static current-voltage measurements were recorded using a SÜSS P200 wafer prober system and a LAKESHORE MODEL 8425 probe station each connected to an AGILENT 4155C semiconductor parameter analyzer. Force spectroscopy have been performed with a PARK SCIENTIFIC XE150 atomic force microscopy (AFM) system using a DD-ACTA Si probe coated with polycrystalline boron-doped diamond (spring constant $40\,Nm^{-1}$, tip radius < 150 nm). Amorphous growth and the thickness of ZTO has been confirmed by X-ray diffraction and X-ray reflectivity measurements, respectively.The minimum bending-induced strain

$$\varepsilon = \frac{z - z_{neutral}}{R} \tag{1}$$

for corresponding radii R has been calculated by estimating the location of the neutral plane $z_{neutral}$ within the entire material stack of height z (Heremans et al., 2016). $z_{neutral}$ takes into account the individual thickness of constituent layers as well as their corresponding approximate Young's modulus of 2.8, 110, 60, 126 and 140 GPa for polyimide, ZTO, Au, PtO_x and Pt, respectively (Salvadori et al., 2003; Jain et al., 2013). In the following, the neutral plane has been assumed to be constant throughout the sample, even though its position slightly shifts across the sample plane due to the lateral thickness differences of the investigated devices. Further, **Eq. 1** neglects the residual strain - remaining from previous bending events - within the constituent device layers (Townsend et al., 1987).

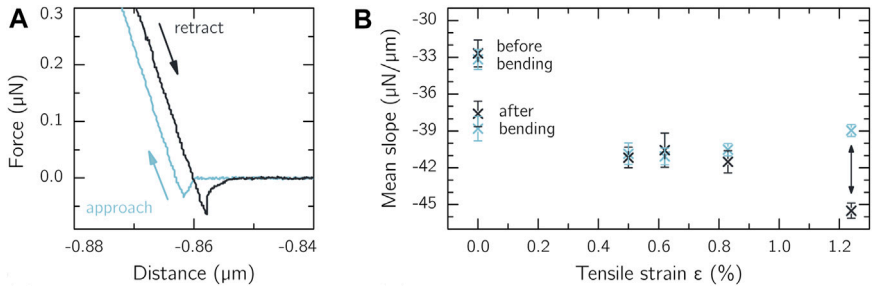

FIGURE 1 | (A) Exemplary force-distance characteristic acquired by force spectroscopy via AFM of an unbent (ε = 0 %) amorphous 24 nm thick ZTO thin-film sample grown on a flexible polyimide substrate, indicating an elastic deformation behavior **(B)** Tensile-strain-dependent mean slopes derived from the approaching and retracting curves of eight separately performed force-distance measurements per bending radius across the ZTO sample. ε has been calculated according to **Eq. 1** for bending radii ranging from 5 mm down to 2 mm.

3 RESULTS AND DISCUSSION

3.1 Elasticity of Amorphous ZTO

In order to investigate the impact of bending induced strain on the mechanical properties of amorphous ZTO, force-distance curves of 24 nm thick ZTO thin-films, deposited on polyimide substrates, have been recorded via force spectroscopy using AFM to monitor the tip-sample interactions via perpendicular cantilever deflection. Respective exemplary force-distance curves of ZTO are depicted in **Figure 1A**. While the cantilever approaches the sample down to a few nanometers of separation between tip and surface, the prevailing attractive van der Waals forces cause the tip to snap into contact, as indicated by the observed minimum of the effective force. Once the tip is in close contact with the thin-film, repulsive Pauli interaction dominates the observed characteristic of the approaching curve, as the scanner further extends toward the sample. At a certain predetermined force setpoint, the scanner starts to retract the tip from the sample. Consequently, the cantilever will bend toward the surface due to attractive adhesive forces, given by the second observed minimum in **Figure 1A**. During further withdrawal of the scanner, the tip detaches from the surface as the elastic constant of the cantilever overcomes the adhesive forces between tip and sample (Cappella and Dietler, 1999).

Figure 1B depicts the strain-dependence of the mean slopes - determined for both the approaching and retraction curves - out of eight force-distance measurement points per bending radius equally distributed across a sample area of 1 μm^2. Starting with the unbent state ε = 0 %, the investigated bending radii have been gradually reduced from R = 5 mm down to R = 2 mm in steps of 1 mm, corresponding to a tensile strain of 0.5 % up to 1.24 %, respectively. By subjecting the sample to a strain up to $\varepsilon \leq 0.83$ %, the resulting higher steepness of the mean slopes clearly suggests an increased stiffness of ZTO. Comparing the slope after the bending procedures with the initial measurement, the sample maintains its slightly higher stiffness, which is probably attributed to residual strain effects and the ZTO thin-film not being fully relaxed during the repeated measurement in its unbent state. The strain-independence of the slopes up to a bending radius of 3 mm, regardless of the scanning-direction, indicates only an elastic deformation of the ZTO thin-film. Further increasing the tensile strain beyond 0.83 %, results in a plastic deformation, since both slopes deviate considerably. ZTO starts to become softer as the tip advances further into the sample, given by the decreased slope of the approaching curve. The absolute value of the mean slope of the retraction curve, however, increases significantly due to compression of the surface by the cantilever tip, causing the thin-film to deform irreversibly. Comparing the mean slopes before and after the bending procedure suggests that the total stress exerted on ZTO causes a substantial amount residual strain to remain in the thin-film. Note that the observed plastic deformation results from combined tensile strain and probing-induced stress; thus the ZTO thin-film might not necessarily undergo plastic deformation across the whole sample but rather in the vicinity of the measurement points.

Figure 2A depicts the exerted probing stress in terms of the attractive tip-sample pull-on force as well as the corresponding adhesion force, calculated for a tip contact area of approximately $7 \times 10^{-14}\,m^2$ and the maximum adhesive force given by the minima of the approaching and retraction curve, respectively. Both stresses appear to be strain-independent and are rather determined by thin-film material itself, as further verified by comparing the initial results with a repeated measurement for the unbent case in **Figure 2B**, after the sample has been exposed to mechanical bending stress. Hence, the force exerted on the sample surface by the cantilever was approximately the same for all measurements. A similar adhesive tip-sample relationship has also been observed regardless whether the ZTO thin-film has been deposited on polyimide or on a quartz glass substrate.

3.2 Strain-Dependence of Electrical Properties

Conductivity as well as Hall effect measurements based on the van der Pauw configuration have been performed at room temperature to gain further insight to what extent bending-induced residual strain affects the electrical properties of amorphous ZTO thin-films. Therefor, 14 nm of ZTO were grown on two $10 \times 10\,mm^2$ polyimide substrates, exhibiting a resistivity of $2 \times 10^{-3}\,\Omega m$, a free-carrier concentration of $4 \times 10^{18}\,cm^{-3}$ and a charge-carrier mobility of $7.2\,cm^2V^{-1}s^{-1}$. Both samples have then been subjected to either compressive or tensile

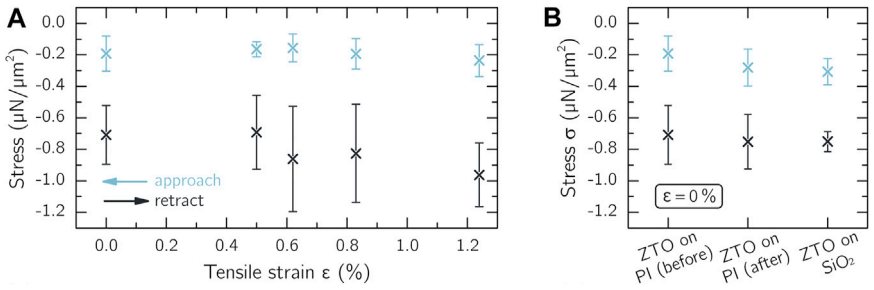

FIGURE 2 | (A) Strain-dependence of the mechanical stress exerted on the ZTO thin-film by the cantilever tip in terms of attractive pull-on force (snap-in) as well as adhesion force per cantilever tip area of $7{\cdot}10^{-14}\,m2$ during the force-distance measurements **(B)** Comparison of the stress exerted by the cantilever tip on ZTO thin-films deposited on quartz glass as well as on polyimide (PI) substrates before and after the bending the sample (ε = 0 %).

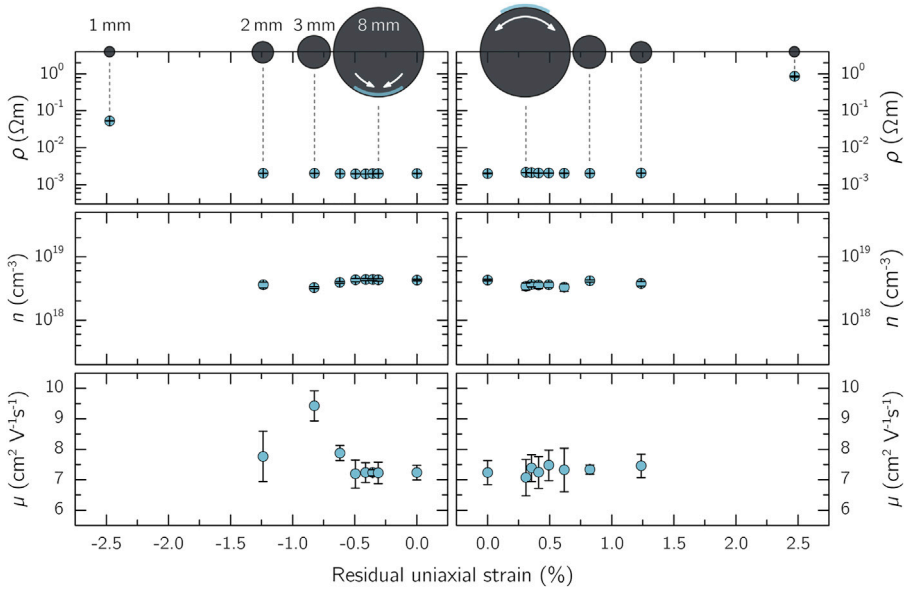

FIGURE 3 | Resistivity, free-carrier concentration and charge-carrier mobility of amorphous ZTO thin-films as a function on the residual compressive and tensile strain, remaining in the sample upon bending to radii ranging from 8 mm down to 1 mm. Beyond ε =±1.24 %, the Hall effect results were not clearly evaluable due to alternating signs of the Hall coefficients.

bending for 10 s in between measurements, while the radius was gradually reduced from 8 to 1 mm. A side-by-side comparison of associated electrical thin-film properties is given in **Figure 3**. Overall, the vast majority of the obtained electrical properties are unaffected by the residual strain regardless of the chosen bending radius between 8 and 2 mm. The duration of each Hall measurement of about 15 min per bending cycle appears to be sufficiently enough relaxation time for the ZTO thin-film to compensate possible effects of residual strain. An increased charge-carrier mobility from approximately $8\,cm^2V^{-1}s^{-1}$–$9.5\,cm^2V^{-1}s^{-1}$ is observable for compressive strain of −0.83 % and presumably associated with the remaining influence of residual strain in the ZTO layer. However, as the mobility decreases to its initial value for ε = − 1.24 %, these changes turn out to be reversible.

For strain exceeding ±1.24 %, only resistivity data are shown, since the corresponding Hall effect results are not clearly evaluable due to alternating signs of the Hall coefficients. As soon as the strain approaches ε = ± 2.5 %, a significant increase of the resistivity of up to more than two order of magnitude is notable for both compressive and tensile strain, which is most likely associated with the ZTO surface starting to become brittle. Consequently, bending the sample around 1 mm causes the surface to be permanently damaged, resulting in irreversible changes of the electrical properties. Note that Hall effect measurements are generally very sensitive to disturbances of the thin-film homogeneity and excessive bending the sample eventually causes the polyimide substrate to plastically deform as well by and to maintain its bent shape which might affect the measurement in general regardless of the condition of ZTO layer. A direct comparison between the impact of excessive compressive and tensile strain, being responsible for plastic deformation, yields a much more pronounced effect of the tensile strain on

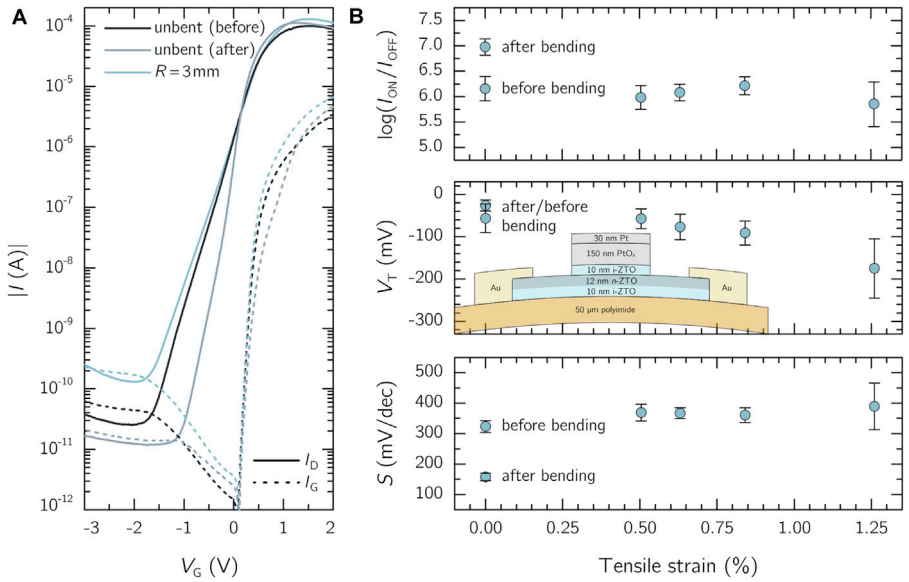

FIGURE 4 | (A) Exemplary static transfer characteristics and associated gate leakage current of a ZTO/PtO$_x$ based MESFET recorded for a bending radius of 3 mm as well as before and after the bending procedures including radii ranging from 5 mm down to 2 mm.The strain has been applied parallel to the channel, i.e., to the current flow direction. The source-drain voltage was fixed at 2 V and the gate width and length are 200 µm and 2 µm, respectively. For better clarity, only the scanning direction from positive to negative gates voltages are shown **(B)** Strain-dependence of the associated current on/off ratio, subthreshold swing and threshold voltage, determined from transfer characteristics of ZTO based MESFETs. For ε =0 %, the transistor parameters before and after the whole bending procedure are depicted. The inset schematically depicts the basic material stacking order of a MESFET with corresponding layer thicknesses.

the overall condition of the surface and thus the electrical properties of the ZTO thin-film. Similar observations have been made for flexible IGZO based transistors, where the device performance is usually more affected by bending-induced tensile strain (Heremans et al., 2016; Billah et al., 2017).

3.3 Performance Durability of Flexible ZTO Based Devices

Static current transfer characteristics of a typical ZTO/PtO$_x$ based MESFET are depicted in **Figure 4A**, recorded for various bending radii ranging from 5 to 2 mm and with a fixed source-drain voltage of 2 V. Corresponding strain values have been calculated by estimating the location of the neutral plane along the gate-channel layer stack according to **Eq. 1**. However, note that the overall induced strain within the ZTO channel is larger at the uncovered parts of the channel between gate and source/drain terminal. During the measuring process, the samples remained in the bent state for at least 10 minutes and the strain has been applied parallel to the channel, i.e., to the current flow direction. The gate width W and length L of all transistors are 200 µm and 2 µm, respectively. The 12 nm ZTO channel exhibits a free-carrier concentration of 1.5×10^{18} cm^{-3} and a charge-carrier mobility of 7.5 cm^{2}V^{-1}s^{-1}. Respective transistor parameters derived from the transfer characteristics are given in **Figure 4B**. All MESFETs exhibit a current on/off ratio between six and seven order of magnitude and can be switched between on and off state within a similar gate voltage range of less than 2.5 V, attributed to their subthreshold swing of about 350 mV/dec. As expected, a clear

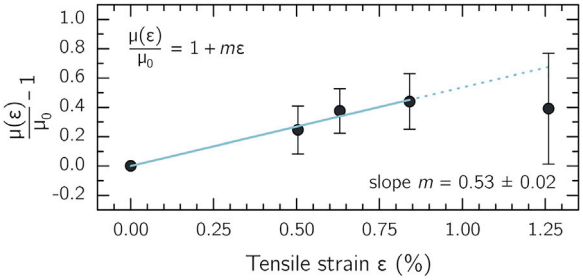

FIGURE 5 | Strain-dependence of the normalized field-effect mobilities calculated from the transfer characteristics of ZTO based MESFETs according to **Eq. 2**.

dependence of the channel conductivity on the tensile strain is observable, considering the doubling of the maximum on-current up to 0.3 mA. Consequently, the maximum transconductance improves from initially 109 µS to roughly 220 µS (ε = 1.26 %) for a bending radius of 2 mm. Further, the threshold voltage exhibits a distinct normally-on shift of about 150 mV toward negative gate voltages with increasing the tensile strain. A similar trend is observable for IGZO based transistors and originates from the increased channel conductivity under tensile strain (Münzenrieder et al., 2011; Petti et al., 2014). After reflattening the sample, the investigated MESFETs are fully operational and the negative V_T is reversed. The transistors show no visible cracks even after multiple tensile bending to radii of 2 mm. However, the unbent MESFETs exhibit a reduced

gate leakage current and thus an increase of the current on/off ratio to seven orders of magnitude as well as an improved subthreshold swing of 150mV/dec after the whole bending procedure.

Associated strain-dependent normalized field-effect mobilities calculated from the transfer characteristics using

$$\mu = \frac{L}{W}\frac{g_{\max}}{end} \tag{2}$$

are shown in **Figure 5**, where $g_{\max}$, e and d denote the maximum transconductance, the elementary charge and the channel thickness, respectively. As expected, the channel conductivity increases upon subjecting the devices to tensile bending stress and consequently, an improvement of the field-effect mobility of almost 80 % from 4.2 $cm^2V^{-1}s^{-1}$–7.5 $cm^2V^{-1}s^{-1}$ has been observed. According to Heremans *et al.*, the change of the charge-carrier mobility for moderate levels of mechanical strain can be described by $\mu(\varepsilon)\mu_0^{-1} = (1 + m\varepsilon)$, where $\mu(\varepsilon)$ and μ_0 corresponds to the mobility in bent and flat condition, respectively, and m denotes an empirical proportionality constant (Heremans et al., 2016). For tensile strain, ε is positive, whereas the sign of m certainly depends on the channel material itself. For amorphous oxide semiconductors such as IGZO based transistors, obtained m values are usually positive and have found to be ranging from +1.4 to +2.7 (Münzenrieder et al., 2013; Tripathi et al., 2015). Linear regression of the strain-dependent field-effect mobilities calculated for the presented ZTO MESFETs yields $m = 0.53 \pm 0.02$, indicating a less sensitive device operation under tensile bending compared to IGZO.

4 CONCLUSION

Amorphous ZTO thin-films have been investigated regarding their performance stability under strain induced by bending around radii ranging from 8 mm down to 1 mm. Force spectroscopy of bent ZTO samples yield no significant effect on the elastic properties of ZTO up to a tensile strain of 0.83 % (R = 3 mm). By exceeding that value, however, the ZTO thin-film starts to plastically deform. Additionally, the impact of residual compressive and tensile strain on the resistivity, the free-carrier concentration as well as the charge-carrier mobility of ZTO has been compared after the samples have been subjected to bending in between Hall-effect and conductivity measurements. Again, the electrical properties appear to be unaffected by the internal strain up to $\varepsilon = \pm 1.24$ % (R = 2 mm). Further increasing the tensile and compressive strain to 2.5 % causes the ZTO surface to become brittle and the resistivity to irreversibly increase by at least two orders of magnitude. Lastly, the operation of ZTO based MESFETs has been investigated while bending the sample around radii between 5 mm and 2 mm. Even up to highest applied tensile strain of 1.26 %, a reasonably stable device performance in terms of a current on/off ratio around six to seven orders of magnitude, a subthreshold swing of 350 mV/dec and a field-effect mobility as high as 7.5 $cm^2V^{-1}s^{-1}$ is observable. Gradually increasing the tensile strain results in a reversible negative V_T shift of approximately 150 mV as well as a steady improvement of the channel conductivity and consequently an increase of the field-effect mobility of almost 80 %. After reflattening the sample, the MESFETs are fully functional and no visible cracks across the transistor structures are observable.

To further improve the transistor performance stability for smaller bending radii, a device passivation or even full sample encapsulation, e.g., with polyimide in the order of the substrate thickness, should shift the neutral plane into the center of the transistor channel to minimize the total induced strain. Nevertheless, the presented results demonstrate a sufficient durability of amorphous ZTO and less sensitive device operation behavior compared to IGZO when being subjected to mechanical stress in terms of bending-induced compressive and tensile strain and thus render ZTO a promising candidate for future bendable electronic applications.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

AUTHOR CONTRIBUTIONS

OL prepared the samples and performed the electrical characterization. MS conducted AFM measurements and assisted with data evaluation. OL drafted the manuscript; MS, HvW and MG helped discussing results, commented on the manuscript during its preparation and approved the final version.

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V

Summary and outlook

Within the scope of this dissertation, the ongoing development progress of amorphous oxide semiconductor based electronics has been further advanced toward the realization and optimization of novel amorphous zinc tin oxide (ZTO) based devices, including transparent thin-film technology, state-of-the-art digital integrated circuitry as well as conformable flexible electronics. Amorphous ZTO thin films have been fabricated by radio frequency long-throw magnetron sputtering at room temperature without undergoing any sort of post-deposition annealing treatment in order to maintain compatibility with common photolithographic patterning as well as thermally unstable flexible organic substrates. Additionally, the operation of MISFETs, JFET based logic inverter circuits as well as ring oscillators is demonstrated for the very first time for amorphous ZTO thin films prepared at room temperature.

Starting with the most fundamental device building blocks, amorphous ZTO is demonstrated a viable option as active channel material in various types of field-effect transistors. Key properties of MESFETs with a PtO_x/n-ZTO gate, JFETs based on p-NiO/n-ZTO heterodiodes and MISFETs implementing HfO_2 as gate dielectric are compared in terms of performance and long-term stability [C1]. The all-oxide transistor approach additionally facilitates to realize devices fully transparent in the visible spectral range. For source and drain electrodes as well as the gate capping layers, a thin highly conductive gallium zinc oxide oxide layer has been deposited by pulsed laser deposition. According to transmission spectroscopy measurements, completed devices exhibit a mean transmittance up to 81 % between 380 nm and 780 nm. All FETs can be operated within a similar supply voltage range of less than 3 V and remain fully functional over the course of the studied time period of 10 weeks. ZTO based MESFETs obtain the highest current on/off ratio of over 6 orders of magnitude and an excellent subthreshold swing of 61 mV/dec, being close to the thermodynamic limit of about 58 mV/dec at 293 K. Additionally, MESFETs further exhibit stable performance as well as full recovery under negative bias stress and overall turn out to be the most promising devices among the three investigated FET types.

Owing to their reasonably high field-effect mobility and low-voltage operation capability, MESFETs and JFETs based on amorphous ZTO are subsequently investigated regarding their suitability in basic digital integrated circuit building blocks [C2,C3]. The Schottky diode field-effect transistor logic (SDFL) has been adapted for simple ZTO based inverters in order to facilitate the cascading of multiple inverters based on unipolar depletion mode transistors of the same charge carrier type by adjustment of the input and output signals regarding their logic compatibility. Associated MESFET and JFET based SDFL inverters are demonstrated to maintain stable functionality while operating under level shift conditions. The design of SDFL circuits is optimized in terms of improving geometry-related transistor properties such as the threshold voltage and drain current saturation behavior as well as reducing the impact of layout related parasitic capacitances in order to enhance the efficiency of ZTO based inverters. Consequently, a remarkable maximum amplification gain as high as 1190 combined with a transition voltage of 80 mV is obtained for an operation voltage of 3 V, exceeding the performance of any similar previously reported devices based on amorphous oxide semiconductors.

Taking a step toward more advanced integrated circuits, MESFET based SDFL inverters are subsequently cascaded in terms of a ring oscillator feedback loop by directly connecting both the output and input terminal of a three stage inverter chain [C4]. An oscillation frequency up to 451 kHz with a single stage delay time of 277 ns is observed for an operation voltage of 3 V, corresponding to the switching speed of a single MESFET gate of roughly 3.6 MHz. As expected, the oscillation frequency does not exhibit a dependence on the supplied operation voltage, since the maximum supply current for charging and discharging each gate is limited by the saturation current of associated MESFETs. Observed delay times are further in reasonable agreement with calculated data derived from a model based on easily accessible transistor parameters.

Ultimately, amorphous ZTO thin films were deposited on flexible polyimide foil in addition to rigid glass substrates to determine the elastic and electrical properties of ZTO in dependence on external stress induced by mechanical bending for radii ranging from $r = 8\,\mathrm{mm}$ to $r = 1\,\mathrm{mm}$ [C5]. Force-distance measurements are performed across the sample surface using a conventional atomic force microscope and yield no significant effect of tensile bending on the elasticity of amorphous ZTO up to a strain of 0.83 % ($r = 3\,\mathrm{mm}$). Exceeding a strain of 0.83 %, however, causes ZTO to plastically deform. The free charge carrier density, the charge carrier mobility and the resistivity are determined by Hall effect measurements at room temperature to examine the impact of residual tensile and compressive strain on the electrical properties of amorphous ZTO thin films. Up to a strain of $\pm 1.24\%$ ($r = 2\,\mathrm{mm}$), the electrical properties remain unaffected, whereas approaching a strain of $\pm 2.5\%$ with the smallest bending radius of 1 mm causes the resistivity to irreversibly increase by more than 3 orders of magnitude. As a consequence, ZTO thin films become brittle and visible cracks start to appear at the surface. Associated Hall measurements are not reliably evaluable due to alternating signs of the Hall coefficients. Further, current-voltage measurements of MESFETs fabricated on polyimide are recorded during mechanical tensile bending using radii between 5 mm and 2 mm. In accordance with the electrical properties of corresponding ZTO thin films, the MESFETs maintain a reasonably stable performance even for the highest strain of 1.26 % in terms of current on/off ratios of over 6 orders of magnitude and a subthreshold swing of about 350 mV/dec. An increase of the forward transconductance from 109 µS to 220 µS is observable with increasing tensile strain and most likely attributed to a decrease of the inter-cation distance during tensile bending. Consequently, the field-effect mobility increases from initially $4.2\,\mathrm{cm^2V^{-1}s^{-1}}$ to $7.5\,\mathrm{cm^2V^{-1}s^{-1}}$. After reflattening the samples, no visible cracks are observable across the transistor structures and the MESFETs remain fully functional.

In conclusion, amorphous ZTO has been demonstrated a sustainable and low-cost yet viable material for transparent and mechanically flexible basic device building blocks and digital integrated circuit elements, even though the deposition processes of constituent device layers during the development of this thesis have been restricted to room temperature exclusively. Nevertheless, various presented devices, such as inverters and ring oscillators, have achieved state-of-the-art like performance not only in accordance with previous reports related to ZTO but amorphous oxide semiconductor based electronics in general.

Outlook

Aside from the most obvious way of significantly enhancing the performance of devices by further reducing the minimum feature size, soft annealing should be considered to increase the field-effect mobility due to structural relaxation and perhaps to improve the overall spatial homogeneity of ZTO thin films [200,201]. Soft annealing refers to a temperature range compatible with photolithographic patterning related resists, typically below 150°C, as well as common flexible organic substrates.

So far, in order to guarantee proper functionality of presented devices, amorphous ZTO thin films have been encapsulated by thin semi-insulating, oxygen-rich ZTO layers at the substrate and gate interface [126]. As a consequence, oxygen diffusion in the vicinity of the contact interfaces reduces the leakage current considerably and thus favors the overall channel depletion capability of amorphous ZTO based field-effect transistors due to saturation of undercoordinated cation bonds. However, choosing an appropriate argon-oxygen mixture as sputtering atmosphere might gain more control over both the high charge carrier concentration at the surface as well as the doping uniformity and thus may improve the device reliability accordingly. In-depth information regarding the doping profile can then be gathered using, for instance, space-charge region spectroscopic methods such as thermal admittance spectroscopy and deep level transient spectroscopy. For ZTO based devices to maintain long-term stability far beyond the investigated time frames, either channel passivation of even complete device encapsulation should then be considered as well.

To minimize the induced strain of flexible devices during mechanical bending, the neutral plane of the material stack is required to be located ideally in the center of the device. However, since the substrate is usually the thickest layer, it almost entirely determines the overall induced strain. In order to shift the neutral strain axis accordingly, the device should be encapsulated using a layer with similar thickness and Young's modulus as the substrate [202,203].

List of abbreviations and symbols

Abbreviation	Designation
AC	alternating current
AOS	amorphous oxide semiconductor
DC	direct current
DRV	driving transistor
FET	field-effect transistor
IGZO	indium gallium zinc oxide
JFET	junction field-effect transistor
LCD	liquid crystal display
MESFET	metal-semiconductor field-effect transistor
MISFET	metal-insulator-semiconductor field-effect transistor
OLED	organic light-emitting diode
PD	pull-down transistor
PU	pull-up transistor
RF	radio frequency
SDFL	Schottky diode FET logic
UV	ultraviolet
ZTO	zinc tin oxide

Symbol	Constant	Numerical Value (SI units)
e	elementary charge	1.602×10^{-19} (C)
ε_0	vacuum permittivity	8.854×10^{-12} ($\mathrm{F \cdot m^{-1}}$)
h	Planck constant	6.626×10^{-34} ($\mathrm{J \cdot s}$)
k_B	Boltzmann constant	1.381×10^{-23} ($\mathrm{J \cdot K^{-1}}$)
m_0	electron mass	9.109×10^{-31} (kg)

Symbol	Definition
A_0	contact area
A^*	Richardson constant
α	slope of the saturation source-drain current
B	magnetic field
C	capacitance
C_G	gate capacitance
χ_S	semiconductor electron affinity
d	(channel) thickness
D_n	electron diffusion coefficient
E_C	conduction band edge energy
E_F	Fermi level
$E_\mathrm{F,n}$	electron quasi Fermi level
E_V	valence band edge energy
E_vac	vacuum level
$\mathcal{E}$	electric field
ε_r	relative permittivity
f	frequency
f_vdp	Van-der-Pauw correction function
F	fan-out, force
ϕ	potential
ϕ_B	Schottky barrier height
$\phi_\mathrm{B}^\mathrm{eff}$	effective Schottky barrier height
$\phi_\mathrm{B,0}$	equilibrium Schottky barrier height
$\bar{\phi}_\mathrm{B}$	mean Schottky barrier height
ϕ_M	metal work function
ϕ_P	pinch-off potential
ϕ_S	semiconductor work function
g	gain
g_m	forward transconductance
g_max	maximum forward transconductance
η	ideality factor
η_img	ideality factor considering image force effects

Symbol	Definition
I	current
I_{C}	charging current
I_{D}	source-drain current
$I_{\mathrm{D,sat}}$	saturation source-drain current
I_{P}, I_0	saturation current
j	current density
j_{s}	saturation current density
l	length
L	gate length
L_{eff}	effective gate length
λ	wave length
m_{eff}	effective electron mass
μ	charge carrier mobility
μ_{d}	drift mobility
μ_{H}	Hall mobility
n	electron density, principal quantum number
N	charge carrier density
N_{A}	acceptor concentration
N_{C}	conduction band edge density of states
N_{D}	donor concentration
p	hole density
P	Gaussian distribution
q	charge
Q	space-charge
r_{H}	Hall scattering factor
r_{o}	output resistance
R	resistance
R_{H}	Hall coefficient
R_{p}	parallel ohmic resistance
R_{s}	series ohmic resistance
ρ	resistivity
ρ_{c}	specific contact resistance
ϱ	space-charge density

Symbol	Definition
s	surface index
S	subthreshold swing
Σ	standard deviation
t	time
T	temperature
τ	single stage gate delay
τ_r	relaxation time
v	velocity
v_d	drift velocity
V, V_ext	external voltage
V_bi	built-in potential
V_bias	negative supply voltage
V_D	source-drain voltage
V_DD	positive supply voltage
$V_\mathrm{D,sat}$	saturation source-drain voltage
V_G	source-gate voltage
V_H	Hall potential
V_IN	input voltage
V_OL	low output level of an inverter
V_OUT	output voltage
V_shift	level shift
V_T	threshold voltage
w	space-charge region width
W	gate width

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Publication List

[C1] O. Lahr, M. S. Bar, H. von Wenckstern and M. Grundmann: *All-Oxide Transparent Thin-Film Transistors Based on Amorphous Zinc Tin Oxide Fabricated at Room Temperature: Approaching the Thermodynamic Limit of the Subthreshold Swing*. Advanced Electronic Materials **6**, 10, p. 2000423 (2020). doi:10.1002/aelm.202000423

[C2] O. Lahr, Z. Zhang, F. Grotjahn, P. Schlupp, S. Vogt, H. von Wenckstern, A. Thiede and M. Grundmann: *Full-swing, high-gain inverters based on ZnSnO JFETs and MESFETs*. IEEE Transactions on Electron Devices **66**, 8, pp. 3376–3381 (2019). doi:10.1109/ted.2019.2922696

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OL conceived and drafted the manuscript, prepared the samples and carried out the electrical characterization. MB assisted with lithographic patterning and data evaluation. Transmission measurements have been performed by Ulrike Teschner (Universität Leipzig). Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2).

Oliver Lahr, Zhipeng Zhang, Frank Grotjahn, Peter Schlupp, Sofie Vogt, Holger von Wenckstern, Andreas Thiede and Marius Grundmann

Full-Swing, High-Gain Inverters Based on ZnSnO JFETs and MESFETs

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The manuscript was conceived by HvW and drafted by OL and HvW. Devices, circuits and photolithography masks have been designed by FG. Samples have been prepared by OL and Monika Hahn (Universität Leipzig). Electrical characterization of devices was performed by OL and ZZ and associated data have been evaluated by OL. Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-1) and (GR 1001/31-2) and by AT within SSP 1796 (TH 829/12-1). The work was further partly supported by "Europäische Fonds für Regionale Entwicklung (EFRE)" within Project COSIMA under grant SAB 100282338.

Oliver Lahr, Holger von Wenckstern, and Marius Grundmann

Ultrahigh-performance integrated inverters based on amorphous zinc tin oxide deposited at room temperature

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OL conceived and drafted the manuscript, designed the circuits and prepared the samples. All measurements including data evaluation and interpretation have been conducted by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Figures and images have been prepared by OL. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2).

Oliver Lahr, Sofie Vogt, Holger von Wenckstern, and Marius Grundmann

Low-Voltage Operation of Ring Oscillators Based on Room-Temperature-Deposited Amorphous Zinc-Tin-Oxide Channel MESFETs

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OL conceived and drafted the manuscript. Sample preparation as well as all measurements including data evaluation and interpretation have been conducted by OL. Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-1) and (GR 1001/31-2).

Oliver Lahr, Max Steudel, Holger von Wenckstern, and Marius Grundmann

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OL conceived and drafted the manuscript, prepared the samples and carried out the electrical characterization. Atomic force microscopy measurements and evaluation of associated data have been performed by MS. Figures have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2)

Curriculum vitae

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Zusammenfassung nach §11 (4) der Promotionsordnung

Zusammenfassung der Dissertation

Toward Sustainable Transparent and Flexible Electronics with Amorphous Zinc Tin Oxide

der Fakultät für Physik und Geowissenschaften der Universität Leipzig

eingereicht von

M. Sc. Oliver Lahr

angefertigt am

Felix-Bloch-Institut für Festkörperphysik

Juli 2022

Starting roughly one decade ago, the gradual replacement of common silicon based electronics by amorphous oxide semiconductors (AOSs) has triggered a rapid evolution as well as the ongoing advancement of flat-panel display technology [1]. Compared to covalent a-Si, AOSs with strong ionicity typically feature a unique electronic structure that combines both a high conductivity and optical transparency in the visible spectral range, while still maintaining a high charge carrier mobility in spite of being amorphous. Back then, the continuously growing demand for scalable electronics, operating at high frequencies and requiring low power consumption, was met by the AOS indium gallium zinc oxide (IGZO), especially since future trends tend to aim toward the development of transparent and mechanically flexible multifunctional devices [2,3]. However, the fact that industrially established metal oxide compounds often contain scarce and highly expensive elements such as indium and gallium has led to recent efforts to substitute materials such as IGZO by alloy systems featuring naturally earth-abundant elements only [4].

A promising, yet far less intensively investigated alternative is the sustainable, low-cost and nontoxic amorphous zinc tin oxide (ZTO) system. ZTO thin films can be fabricated at room temperature and exhibit a high charge carrier mobility of about $10\,\mathrm{cm^2V^{-1}s^{-1}}$ [5,6]. First ZTO based electronic devices have already been demonstrated in 2005, followed by numerous studies presenting predominantly metal-insulator-semiconductor field-effect transistors prepared at elevated temperatures of at least 300°C [7]. It was not until more than ten years later that the more accessible metal-semiconductor field-effect transistor (MESFET) approach has been adapted for amorphous ZTO, generally facilitating higher switching frequencies and significantly less supply voltage to operate [8]. Since then, MESFETs and junction field-effect transistors (JFETs) as well as associated simple inverter circuits have been demonstrated, both based on amorphous ZTO thin films deposited at room temperature [9,10].

Within the scope of this dissertation, the previous development and optimization progress of ZTO based devices has been further advanced toward multiple directions, including state-of-the-art digital integrated circuitry, fully transparent devices and conformable flexible electronics, all of which are fabricated at moderate temperatures by industrially relevant fabrication methods to highlight the immense potential of ZTO.

Amorphous ZTO is demonstrated a viable option as active channel material in fundamental types of field-effect transistors such as MESFETs with a PtO_x gate, JFETs based on p-NiO/n-ZTO heterojunctions as well as MISFETs implementing HfO_2 as gate dielectric [C1]. The all-oxide device approach, fabricated by a combination of radio frequency long-throw magnetron sputtering and pulsed laser deposition processes at room temperature, yields fully transparent transistors with a mean transmittance up to 81 % (380 nm - 780 nm). All devices can be operated within a similar supply voltage range of less than 3 V and exhibit a current on/off ratio as high as 6 orders of magnitude. MESFETs and JFETs exhibit an excellent subthreshold swing as low as 61 mV/dec, being close to the thermodynamic limit. Presented devices further maintain their properties for the investigated time period of 10 weeks.

Owing to their fast-switching capability and low-voltage operation, MESFETs and JFETs based on amorphous ZTO are subsequently investigated regarding their suitability in basic digital integrated circuit building blocks. The Schottky diode FET logic (SDFL) has been adapted in order to facilitate the cascading of multiple inverters based on unipolar depletion mode transistors of the same charge carrier type by adjusting input and output signals regarding their logic level compatibility [C2,C3]. ZTO based SDFL inverters exhibit a sufficient voltage shift of the input signal while maintaining stable performance. Not only do presented SDFL inverters exhibit a peak performance in terms of a maximum amplification gain as high as 1190 combined with a transition voltage of 80 mV but, further, can be considered current state-of-the-art with respect to any previously reported similar devices based on amorphous oxide semiconductors, despite of ZTO being prepared at room temperature. Associated SDFL inverters are then successfully integrated within a feedback loop to obtain ring oscillator circuits and gain insights into the high-frequency properties of amorphous ZTO based MESFETs. Ring oscillators exhibit an oscillation frequency as high as 451 kHz for an operation voltage of 3 V, corresponding to a single stage delay of 277 ns or a MESFET operation frequency of 3.6 MHz [C4].

Ultimately, amorphous ZTO thin films are fabricated on flexible polyimide foil to determine the elastic and electrical properties of ZTO while being subjected to external stress induced by mechanical bending for radii ranging from $r = 8$ mm to $r = 1$ mm [C5]. Force-distance measurements yield no noticeable change of the elastic properties up to a tensile strain of 0.83 % ($r = 3$ mm). Exceeding that value causes the ZTO thin films to plastically deform. Electrical thin-film properties in terms of free charge carrier density, charge carrier mobility and resistivity are determined by Hall effect measurements in dependence on residual tensile as well as compressive strain and are unaffected up to a strain of ± 1.24 % ($r = 2$ mm). Further decreasing the bending radius to 1 mm causes the ZTO thin-film surface to become brittle and the resistivity to irreversibly increase by more than 3 order of magnitude. Current-voltage characteristics of associated MESFETs are recorded during tensile bending using radii between 5 mm and 2 mm. While all investigated devices maintain stable current on/off ratios and subthreshold swings, a clear improvement of the channel conductivity from 109 µS to 220 µS with increasing the tensile strain is observable, corresponding to a shift of the field-effect mobility from 4.2 $cm^2V^{-1}s^{-1}$ to 7.5 $cm^2V^{-1}s^{-1}$. After reflattening the samples, no visible cracks are observable across the transistor structures and the MESFETs remain fully functional.

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Publication List of the Author

The publications [C1]-[C5] are part of this cumulative dissertation. Brief descriptions of own contributions to each publication are given below.

[C1] Oliver Lahr, Michael S. Bar, Holger von Wenckstern and Marius Grundmann
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OL conceived and drafted the manuscript, prepared the samples and carried out the electrical characterization. MB assisted with lithographic patterning and data evaluation. Transmission measurements have been performed by Ulrike Teschner (Universität Leipzig). Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2).

[C2] Oliver Lahr, Zhipeng Zhang, Frank Grotjahn, Peter Schlupp, Sofie Vogt, Holger von Wenckstern, Andreas Thiede and Marius Grundmann
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The manuscript was conceived by HvW and drafted by OL and HvW. Devices, circuits and photolithography masks have been designed by FG. Samples have been prepared by OL and Monika Hahn (Universität Leipzig). Electrical characterization of devices was performed by OL and ZZ and associated data have been evaluated by OL. Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-1) and (GR 1001/31-2) and by AT within SSP 1796 (TH 829/12-1). The work was further partly supported by "Europäische Fonds für Regionale Entwicklung (EFRE)" within Project COSIMA under grant SAB 100282338.

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OL conceived and drafted the manuscript, designed the circuits and prepared the samples. All measurements including data evaluation and interpretation have been conducted by OL. Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2).

[C4] Oliver Lahr, Sofie Vogt, Holger von Wenckstern, and Marius Grundmann
Low-Voltage Operation of Ring Oscillators Based on Room-Temperature-Deposited Amorphous Zinc-Tin-Oxide Channel MESFETs
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OL conceived and drafted the manuscript. Sample preparation as well as all measurements including data evaluation and interpretation have been conducted by OL. Figures and images have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-1) and (GR 1001/31-2).

[C5] Oliver Lahr, Max Steudel, Holger von Wenckstern, and Marius Grundmann
Mechanical Stress Stability of Flexible Amorphous Zinc Tin Oxide Thin-Film Transistors
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OL conceived and drafted the manuscript, prepared the samples and carried out the electrical characterization. Atomic force microscopy measurements and evaluation of associated data have been performed by MS. Figures have been prepared by OL. All authors critically discussed and revised the manuscript during its preparation and approved the final version. Project funding was acquired by HvW and MG within the framework of the DFG Schwerpunktprogramm SPP 1796 "High Frequency Flexible Bendable Electronics for Wireless Communication Systems (FFlexCom)" (GR 1001/31-2).

Collaborations and Third-Party Services

Collaborations within Universität Leipzig, Felix Bloch Institute of Solid State Physics, Semiconductor Physics Group:

- Daniel Splith provided the software to evaluate IV and CV measurements
- Fabian Klüpfel provided a software for the wafer prober system to automatically measure sample batches containing multiple devices
- Jörg Lenzner and Daniel Splith performed SEM measurements
- Max Steudel performed AFM measurements
- Monika Hahn and Michael Bar assisted with photolithography
- Philipp Storm and Michael Bar introduced me to the PLD setup
- Sofie Vogt and Anna Reinhardt introduced me to the sputtering setup
- Stefan Hohenberger and Michael Lorenz introduced me to the XRR and XRD measurement setup
- Ulrike Teschner performed transmission spectroscopy measurements
- Zhipeng Zhang provided some measurement data of ZTO device characteristics
- Within the scope of this dissertation, the master thesis of Max Steudel has been supervised
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External collaborations

- First photolithography mask containing various advanced device structures have been designed by Frank Grotjahn, Institut für Elektrotechnik und Informationstechnik, Universität Paderborn
- Polyimide substrates have been prepared and kindly provided by Niko Münzenrieder, Faculty of Science and Technology, Free University of Bozen-Bolzano, Italy
- ToF-SIMS measurements have been performed and evaluated by Susanne Selle and Stephan Gierth at Fraunhofer-Institut für Mikrostruktur von Werkstoffen und Systemen (IMWS), Halle

Supervisors

This thesis has been supervised by Prof. Dr. Marius Grundmann and PD Dr. habil. Holger von Wenckstern.

Institutes

This dissertation has been developed between February 2019 and July 2022 at

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Selbstständigkeitserklärung

Hiermit versichere ich, dass die vorliegende Disseration mit dem Titel

"Toward Sustainable Transparent and Flexible Electronics with Amorphous Zinc Tin Oxide"

selbstständig verfasst und ausschließlich unter Zuhilfenahme der ausgewiesenen Hilfsmittel angefertigt wurde. Alle Stellen, welche im Wortlaut oder dem Sinn nach veröffentlichten beziehungsweise noch unveröffentlichten Quellen entnommen wurden, sind eindeutig als solche kenntlich gemacht. Ich versichere, dass außer den von mir in der Dissertation genannten keine weiteren Personen bei der geistigen Erstellung der vorliegenden Arbeit beteiligt waren und ich insbesondere nicht die Hilfe eines Promotionsberaters in Anspruch genommen habe. Weiterhin erkläre ich, dass keine weiteren Personen von mir oder in meinem Auftrag weder unmittelbar noch mittelbar geldwerte Leistungen für Arbeiten erhalten haben, die im Zusammenhang mit dem Inhalt der vorgelegten Dissertation stehen. Ich versichere, dass die vorgelegte Arbeit weder im Inland noch im Ausland in gleicher oder in ähnlicher Form in einer anderen Prüfungsbehörde zum Zwecke einer Promotion oder eines anderen Prüfungsverfahrens vorgelegt und in ihrer Gesamtheit noch nicht veröffentlicht wurde. Darüber hinaus erkläre ich, dass ich bisher keine erfolglosen Promotionsversuche unternommen habe.

Leipzig, den 22.07.2022

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Oliver Lahr