

Online Research @ Cardiff

This is an Open Access document downloaded from ORCA, Cardiff University's institutional repository: <https://orca.cardiff.ac.uk/id/eprint/158987/>

This is the author's version of a work that was submitted to / accepted for publication.

Citation for final published version:

Chen, Jinlei, Wang, Sheng ORCID: <https://orcid.org/0000-0002-2258-2633>,
Liang, Jun ORCID: <https://orcid.org/0000-0001-7511-449X>, Navaratne,
Rukshan and Ming, Wenlong ORCID: <https://orcid.org/0000-0003-1780-7292>
2023. Decentralized control for multi-terminal cascaded medium-voltage
converters considering multiple crossovers. IEEE Transactions on Power
Delivery 10.1109/TPWRD.2023.3268829 file

Publishers page: <http://dx.doi.org/10.1109/TPWRD.2023.3268829>
<<http://dx.doi.org/10.1109/TPWRD.2023.3268829>>

Please note:

Changes made as a result of publishing processes such as copy-editing, formatting and page numbers may not be reflected in this version. For the definitive version of this publication, please refer to the published source. You are advised to consult the publisher's version if you wish to cite this paper.

This version is being made available in accordance with publisher policies.

See

<http://orca.cf.ac.uk/policies.html> for usage policies. Copyright and moral rights for publications made available in ORCA are retained by the copyright holders.



Decentralized Control for Multi-terminal Cascaded Medium-Voltage Converters Considering Multiple Crossovers

Jinlei Chen, Sheng Wang, *Member, IEEE*, Jun Liang, *Senior Member, IEEE*,
Rukshan Navaratne and Wenlong Ming, *Member, IEEE*

Abstract— Decentralized control with multiple droop characteristics can significantly improve the accuracy of power flow in medium-voltage direct-current (MVdc) networks. However, multiple crossovers caused by different control characteristics can lead to the drifts of power and voltage and instability issues. When this type of control is implemented in the cascaded three-level neutral-point-clamped (C3L-NPC) converters, on one hand, the mechanism of such the power and voltage drifts was not investigated. On the other hand, power control accuracy, dc voltage balancing across submodules (SMs) and multiple crossovers should all be considered, which requires suitable control methods. To address the challenges, firstly, the mechanism behind the power and dc voltage drifts is analyzed. Secondly, a control scheme is presented to improve the power control accuracy and dc voltage balancing and concurrently, to avoid the multiple crossovers. This is achieved by suitable droop gain design and adding a secondary power compensator. The presented control scheme is verified in MATLAB/Simulink simulation and experimentally validated in a three-terminal MVdc testbed. Results show that the accuracy of steady-state power flow is improved by 15% due to the elimination of multiple crossovers, while the power accuracy at dynamics improved by 13% with the secondary power compensator.

Index Terms-- Medium-voltage direct-current (MVdc), cascaded three-level neutral-point-clamped (C3L-NPC) converter, decentralized control, multiple crossovers.

NOMENCLATURE

C3L-NPC	Cascaded three-level neutral-point-clamped.
MVdc	Medium-voltage direct-current.
MMC	Modular-multilevel converter.
DSOs	Distribution system operators.
ESS	Energy storage system.
PLL	Phased-locked loop

This work was supported in part by the EPSRC Supergen Energy Networks Hub under grant EP/S00078X/1 and in part by the EPSRC Sustainable Urban Power Supply through Intelligent Control and Enhanced Restoration of AC/DC Networks under grant EP/T021985/1. (Corresponding author: Wenlong Ming).

J. Chen, S. Wang, J. Liang and R. Navaratne are with the School of Engineering, Cardiff University, Cardiff, CF24 3AA, U.K. (e-mail: ChenJ111, WangS9, LiangJ1 and NavaratneR@cardiff.ac.uk).

W. Ming is with the School of Engineering, Cardiff University, Cardiff, CF24 3AA and also with the Compound Semiconductor Applications Catapult, Newport, NP108BE, U.K. (e-mail: wenlongming@ieee.org)

LPF	Low-pass filter
V, I, P	Magnitudes of voltage, current and power.
v, i, p	Instantaneous voltage, current and power.
<i>A. Subscripts</i>	
i and j	the i^{th} and j^{th} converters.
d and q	the d -axis and q -axis components on the synchronous coordinate frame.
dc	Direct-current components.
<i>B. Superscripts</i>	
*	Reference value.

I. INTRODUCTION

THE decentralized control strategies are promising to be widely used in the medium-voltage direct-current (MVdc) systems [1]–[3]. The power feeding and voltage support can be automatically shared by power converters thus improving the voltage and power regulation, and meanwhile, decreasing the risk of system failures compared with the centralized control. Traditional decentralized control such as the power versus voltage droop method usually adopts a single droop slope [4]. This slope is typically shallow (e.g. 5%) and thus exhibits a characteristic of a voltage source more than a current source. In this case, the accuracy of power control is significantly impacted by any dc voltage disturbance. A slight dc voltage offset (ΔV_{dc}) that may be caused by errors of sensors will cause a huge mismatch of power flow (ΔP) (see Fig.1(a)). Further increasing the slope of the droop will mitigate the inaccuracy but could lead to voltage instability in dynamic events (e.g. change of loads), which actually imposes greater threats to the MVdc systems.

The decentralized control with multiple droop characteristics is a popular solution to precisely control the power while well stabilize the system in dynamic events, which is shown in Fig. 1(b). It features a steep droop (k_{droop2}) in the narrow region around the desired operating point [5]. Due to the steep droop slope, the accuracy of power control is thus significantly improved as the power is much less sensitive to voltage disturbance with k_{droop2} . Hence, the droop curve within the narrow region features the current source characteristics. If

there is a large power disturbance which forces the operation point beyond the narrow band, control of dc link voltage should be prioritized to ensure stable operation of the system at the expense of reducing the power control accuracy. This is achieved by using smaller droop slopes k_{droop1} and k_{droop3} to make the voltage less sensitive to such disturbance.

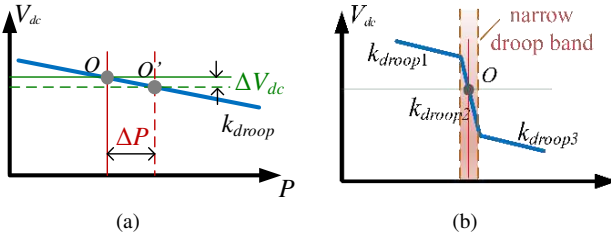


Fig. 1. Decentralized control characteristics in power versus voltage ($P-V_{dc}$) droop. (a) Conventional control with single droop characteristics. (b) Improved control with multiple droop characteristics.

The multiple-slope based decentralized control have been reported in [6]-[11]. In [6]-[9], different types of droop control and margin control which are commonly used in dc distribution networks are introduced. In [10], an improved coordinated control strategy of multi-terminal dc systems was presented by combining the double stage voltage margin and undead-band voltage droop methods. Thus, the power and voltage variations are restrained. In [11], the droop curves are flexibly adjusted instead of using a constant slope. Both current sharing and dc voltage are improved simultaneously. Despite the advantages of multiple-slope control, the concerns of consequent adverse effects also arise. The interactions between converter stations with different control types may exist. The interactions can lead to the condition of multiple crossovers where more than one possible operating points would arise. This may result in the shift of dc voltage and unintended power imbalances at converter stations. Such multiple crossovers were reported in limited resources presented by industry and projects in Europe [12], [13]. In [12], the adverse effects caused by the multiple crossovers were first revealed for two-terminal high-voltage direct-current (HVDC) applications. Such a phenomenon will arise when one converter operates with constant power control and the other with current versus voltage droop ($I_{dc} - V_{dc}$) control. In [13], the multiple crossovers resulting from another typical control strategy combination – constant current control and power versus voltage droop ($P - V_{dc}$) control were studied. The constant current control has been mostly used in the dc/dc converters [14]-[16]. Although it has not been widely used for dc/ac converters, however, since a ‘multi-vendor’ supply chain is considered in the future and each manufacturer has created their own control concepts, it is worth considering different types of control characteristics [17]. The effects of multiple crossovers caused by interactions between $P - V_{dc}$ droop control and current control have been experimentally assessed through a modular-multilevel converter (MMC) based HVDC link [13]. Also, a guideline on how to select a suitable droop slope to avoid the multiple crossovers were therein given.

However, a few research gaps have yet to be closed. First, the mechanism of the power and voltage drifts caused by the multiple crossovers remains unexplored. Second, although

multiple crossovers can be avoided by reducing the droop slope following the guideline in [13], this sacrifices the advantage of the steep droop slope as discussed—the power control accuracy at dynamics is decreased when the system is subjected to a perturbation in either dc voltage or dc current. Third, apart from the above, dc voltage balancing across submodules (SMs) is another understudied issue for cascaded dc/dc and dc/ac converters, in which dc sides are made in series connection [18], [19]. These types of converters are suitable for MVdc applications due to their affordability of high dc link voltage. Among the cascaded converters, C3L-NPC converters are a promising candidate, which have been adopted in the UK’s first MVDC demonstration project (ANGLE-DC) in North Wales [20]-[22]. When the droop methods are employed to the converters with dc series connection, the smaller the slope is in Fig. 1, the better the dc voltage balancing would be, at the sacrifice of accuracy of power control [19], [23]. Thus, how to find a control solution that balances these three factors is a challenge.

This paper investigates the multiple crossovers when using constant I_{dc} and $P - V_{dc}$ multiple slope-based decentralized control in the C3L-NPC converter based MVdc system. To address aforementioned challenges, the mechanism of the power and voltage drifts caused by the multiple crossovers are first analyzed. It is found that the normal operating point is unstable in the presence of multiple crossovers. Then, the selection method for the droop gain is presented based on consideration of multiple crossovers between different converters and dc voltage balancing in each C3L-NPC converter. Also, a secondary power compensator is proposed to guarantee the accuracy of power flow. Therefore, the multiple crossovers are avoided, and meanwhile, the voltage balancing and power flow are well controlled. The presented solution has been verified through simulation and experimental tests on a three-terminal MVdc testbed scaled down from the real ANGLE-DC project. By using the presented methods, the accuracy of power at steady state has been improved by 15% due to the elimination of multiple crossovers, and meanwhile, the dc voltage balancing is well achieved. At dynamic changes of dc current, the power accuracy has been improved by 13% with a secondary power compensator.

II. CONTROL STRUCTURE FOR THREE-TERMINAL C3L-NPC CONVERTERS

In this section, the C3L-NPC converters in the ANGLE-DC MVdc demonstration project are selected for analysis. First, the configuration of C3L-NPC converters is introduced. Then, two potential challenges are presented – one is the power and voltage drifts caused by the interactions due to the multiple crossovers. The other is the impact of the droop slope on the occurrence of multiple crossovers, power control accuracy and dc voltage balancing performance across SMs within C3L-NPC converters.

A. C3L-NPC Converters in ANGLE-DC Project

The C3L-NPC converters were adopted in the ANGLE-DC MVDC link due to the low cost without sacrificing much the performance compared to MMCs. C3L-NPC converters for MVdc applications since then have become an attractive to

distribution system operators (DSOs) [20]. Fig. 2 shows the topology of a C3L-NPC converter. There are $2N$ 3L-NPC SMs cascading together, N on the positive pole and another half on the negative pole. A resistive grounding is connected in shunt at the midpoint of the cascaded SMs to configure a bipolar system. The dc side of each SM is connected in series to establish a demanded medium-level dc voltage. Two sets of Yd11 isolation transformers are connected in parallel at the ac side.

As more renewable energies are integrated into the power networks in the future, such a point-to-point power MVdc link could be extended to a multi-terminal system [24]. For example, incorporating an energy storage system (ESS) in the MVdc distribution system can improve the quality, efficiency and reliability of the MVdc transmission system [24]. In terms of the converter station 3 in Fig. 2, the dual active bridge (DAB) based dc/dc converters or multilevel ac/dc converters can be used to for renewable energy collections or connections to other distribution networks. This converter may operate as a dc current source. However, there are potential adverse interaction effects due to the coupling of different converter stations.

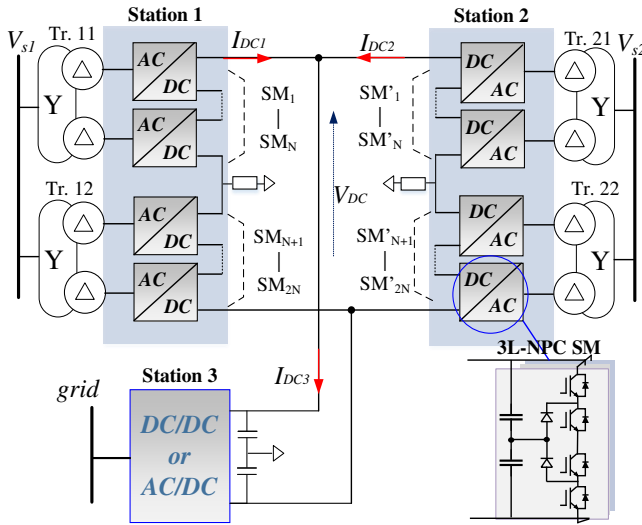


Fig. 2. C3L-NPC converter based three-terminal MVdc link.

B. Multiple crossovers between different Converters

The multiple crossovers may exist in a multi-terminal system, where I_{dc} control and $P-V_{dc}$ droop control are adopted in different converter stations. In this paper, the three-terminal system in [24] is used for study and is depicted in Fig. 2, where Station 3 adopts the constant I_{dc} control and C3L-NPC converter stations (Stations 1 and 2) adopt the $P-V_{dc}$ control. The multiple crossovers have been displayed in Fig. 3, where the red line represents the curve of the constant current control, and the blue line represents the merged curve of the droop control of two C3L-NPC converter stations. It can be seen in Fig. 3(a) that there are no multiple crossovers between I_{dc} and $P-V_{dc}$ control if power flow is positive (the positive directions are defined as the directions of red arrows in Fig. 2). There is only one operating point (O) in steady state.

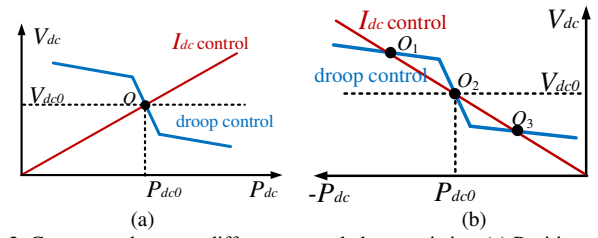


Fig. 3. Crossovers between different control characteristics. (a) Positive power flow condition. (b) Negative power flow condition.

However, multiple crossovers may exist if the direction of power flow is reversed (see 3(b)). There are three intersection points denoted as O_1 , O_2 and O_3 . The adverse impacts caused by the multiple crossovers can be the deviations of the voltage and power from the desired operating points, thus deteriorating the performance of system or even making the system fall into collapse. The detailed analysis of the multiple crossings is presented in Section III.

C. Voltage Balancing of SMs with a Droop-controlled Converter

Droop-based voltage balancing control is widely adopted in the cascaded converters as there is no communication required between SMs [19], [25]–[27]. Thus, the fault-tolerant operation of system can be achieved. The $P-V_{dc}$ droop control can contribute to the voltage balancing across SMs if each SM uses a $P_i - V_{dci}$ droop controller, where P_i and V_{dci} is the power and dc voltage of the i^{th} SM [23]. The voltage balancing with droop control is shown in Fig. 4. To equalize the power sharing amongst SMs, the power and voltage references (P_{i0} and V_{dci0}) of each SM are set as $P_{i0} = \frac{P_0}{2N}$ and $V_{dci0} = \frac{V_{dc0}}{2N}$, where P_0 and V_{dc0} are given references of the converter and $2N$ is the number of cascaded SMs. Due to the droop characteristic, the dc voltage balancing between SMs can be automatically achieved [23]. For example, if dc voltage of a SM is decreased from V_{dci0} to V_{dci1} after suffering from a disturbance, the power is also decreased according to the droop curve. Thus, the dc voltage can restore to V_{dci0} with the decreased power output.

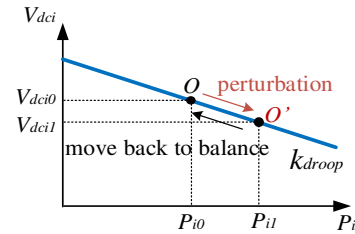


Fig. 4. Droop-based voltage balancing control within SMs.

As discussed above, it is concluded that a larger droop gain is beneficial to accuracy of power control whereas a smaller droop gain can avoid multiple crossings and mitigate voltage imbalance. Thus, only by optimizing the droop gain is not sufficient to meet all the desired performance. To address this challenge, a suitable control method is presented in Section IV. It should be noted that these potential issues and presented solutions also apply to other types of cascaded converters with dc sides in series connections, since they present similar output characteristics.

III. ANALYSIS OF THE MULTIPLE CROSSINGS DUE TO DIFFERENT CONTROL CHARACTERISTICS

As previously shown in Fig. 3(b), interaction between I_{dc} and $P-V_{dc}$ droop creates multiple crossovers (O_1 , O_2 and O_3). Initial observation shows that the operating points will be either located at O_1 or O_3 in steady-state and O_2 is an unstable point. The mechanism of this phenomenon was not yet investigated.

To fully study the mechanism, two cases are discussed corresponding to the disturbances caused by dc current and dc voltage. Assume Stations 1 and 3 initially operates at O_2 (see Fig. 5). Fig. 5(a) and 5(b) show the shift of the operating point during the change of dc current and voltage respectively.

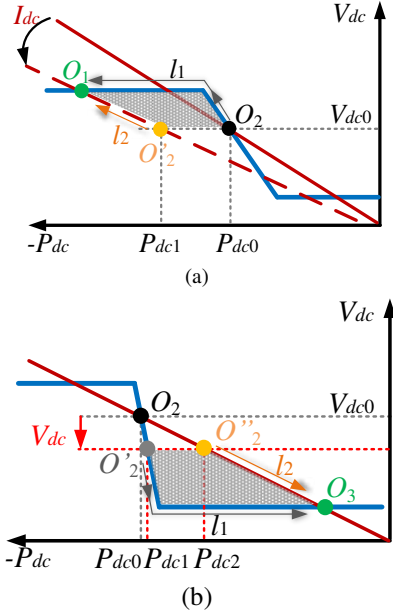


Fig. 5. Power and voltage drifts under a disturbance (the definitions of the red and blue curves are same as those in Fig. 3). (a) The case under a dc current disturbance. (b) The case under a dc voltage disturbance.

In Fig. 5(a), the dc current of Station 3 is slightly increased, represented by the change of the dc current curve from the red solid line to the red dashed line. Following this, the operating point of the Station 3 jumps immediately from O_2 to a new point O_2' . The operating point of Stations 1 is maintained at O_2 in transient. The power P_{dc1} at O_2' then has a greater absolute value than the power P_{dc0} at O_2 . This means that the power absorbed by the Station 3 from ac to dc side is larger than the power output from dc to ac side in Station 1. The dc link capacitor will be charged according to the power balance equation defined as (1).

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = P_{drp,1} - P_{i_{dc},3} \quad (1)$$

where C_{dc} is the equivalent dc link capacitance, $P_{drp,1}$ is the power of Station 1 and $P_{i_{dc},3}$ is the power of Station 3.

Consequently, the dc voltage is increased. The operating point of Station 3 will then move in the direction of arrow \vec{l}_2 , while the operating point of Station 1 moves in the direction of arrow \vec{l}_1 . The absorbed power at the dc side remains larger than the output power until operating points reach at O_1 , where the system becomes stable at an undesired voltage level.

In Fig. 5(b), a perturbation results in slight drop of dc voltage which is represented by change from the grey dashed horizontal line to the red dashed horizontal line. Following this, the operating point of Station 1 jumps from O_2 to O_2' , while the operating point of Station 3 jumps to O_2'' . As $P_{i_{dc},3} > P_{drp,1}$, the dc link capacitor is discharged according to (1) and the dc voltage decreases. Similarly, the operating point of Station 3 will then move following \vec{l}_2 , while that of Station 1 will move following \vec{l}_1 . The absorbed power at the dc side remains lower than the output power until O_3 is reached. Thus, the system is stabilized at another unwanted voltage level.

Through the above analysis, it is validated that the operating point O_2 is unstable whenever a slight disturbance exists in the system. It may shift to O_1 or O_3 depending on the disturbance. Such adverse effects need to be addressed to allow the system to operate at O_2 and to increase its immunity to any disturbance.

IV. PRESENTED DECENTRALIZED CONTROL SCHEME

A. Decentralized Control Schematic

To improve the performance of dc voltage balancing and power control accuracy, and concurrently to mitigate the multiple crossovers, an improved control method is proposed. Fig. 6(a) and (b) show the control schematics of C3L-NPC SMs and the dc/dc converter in Station 3 (see Fig. 2), respectively. For the droop control in Fig. 6(a), the desired operating points ($P_{0,i}$, $Q_{0,i}$ and $V_{dc0,i}$) of SMs are given by a high-level controller. Each SM controller works at the $P_i - V_{dci}$ droop control mode, so the external characteristic of the converter station is also exhibited as the droop control. A droop gain k_{droop} is used in the $P_i - V_{dci}$ droop controller. Output signals from the droop controller are the current references which are sent to the current controller performed at the dq frame. A PLL is used for grid frequency synchronization. The constant current control for the current-controlled converter in Station 3 is depicted in Fig. 6(b). As can be seen, a closed-loop current controller is used to control the inductor current to trace the given reference. As the k_{droop2} in the narrow band (see Fig. 1) is the cause behind the multiple crossovers, the optimal design for k_{droop2} is particularly presented in this section. The k_{droop1} and k_{droop3} adopt a normal droop setting with a 5% slope [28]. It is noted that droop parameter in Fig. 6 only stands for k_{droop2} while k_{droop1} and k_{droop3} are omitted for simplicity.

B. Droop Gain Selection

1) *Droop gain selection considering the multiple crossovers:* As shown in Fig. 5, the slope of droop curve in the narrow band should be less than the slope of dc current curve to avoid the intersections.

The conclusion can be extended to multi-terminal conditions, assuming that there are m stations with droop control and l stations with dc current control [13]. According to the power balance, there is:

$$\sum_{i=1}^m P_{drp,i} = \sum_{j=1}^l P_{i_{dc},j} \quad (2)$$

where $P_{drp,i}$ and $P_{i_{dc},j}$ are the power processed by the converter

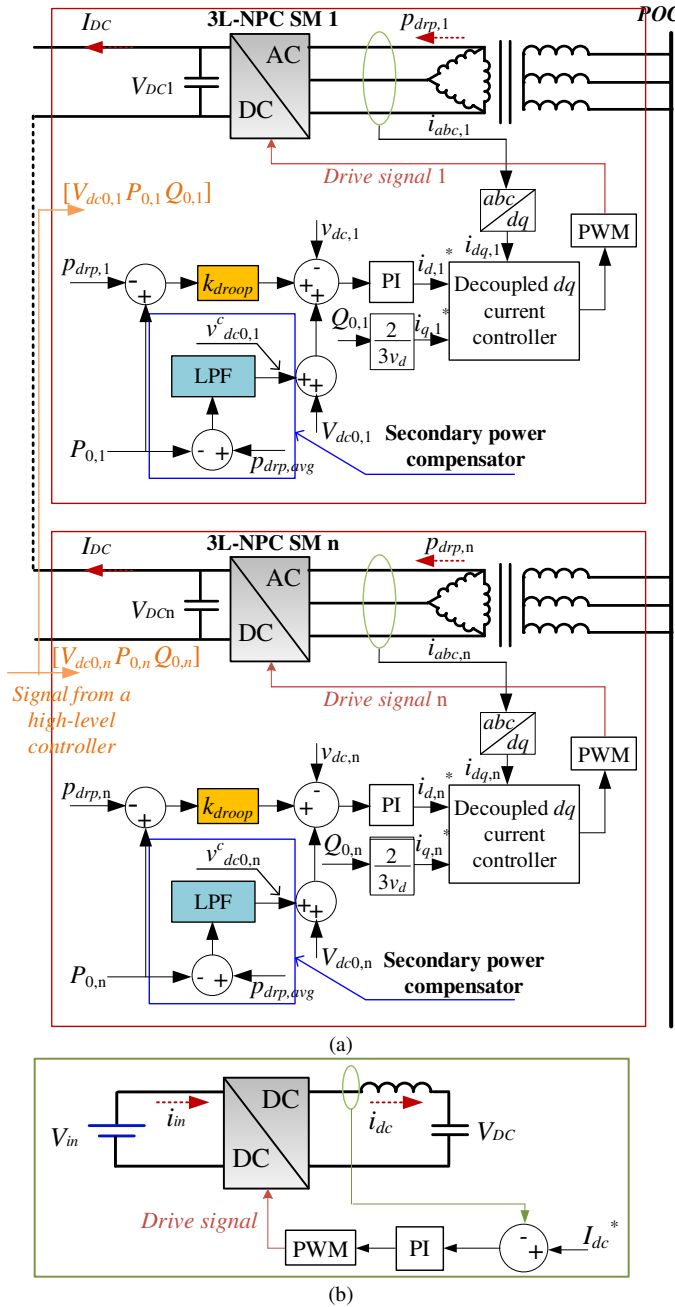


Fig. 6. The decentralized control schematic of the system. (a) Droop control for C3L-NPC converters. (b) DC current control for dc/dc converters.

stations with droop control and dc current control, respectively. $P_{drp,i}$ and $P_{i_{dc},j}$ are represented as:

$$P_{drp,i} = \frac{-1}{k_{droop}} (v_{dc,i} - V_{dc0,i}) + P_{0,i} \quad (3)$$

$$P_{i_{dc},j} = v_{dc,j} i_{dc,j} \quad (4)$$

Substituting (3) and (4) into (2), we can obtain:

$$\sum_{i=1}^m \frac{-1}{k_{droop}} (v_{dc,i} - V_{dc0,i}) + P_{0,i} = \sum_{j=1}^l v_{dc,j} i_{dc,j} \quad (5)$$

As the converter stations share a common dc bus, $v_{dc,i} = v_{dc,j}$ is obtained if the cable impedance is omitted. To find the slope of the merged control characteristics of all VSCs with the V_{dc} - P droop and the VSCs in current control mode, the

derivative of (5) is taken with respect to $v_{dc,i}$, yielding:

$$\frac{\partial \left(\sum_{i=1}^m \frac{-1}{k_{droop}} (v_{dc,i} - V_{dc0,i}) + P_{0,i} \right)}{\partial v_{dc,i}} = \frac{\partial \left(\sum_{j=1}^l v_{dc,j} i_{dc,j} \right)}{\partial v_{dc,i}} \quad (6)$$

By solving (6), the following relationship is obtained as

$$\sum_{i=1}^m \frac{-1}{k_{droop}} = \sum_{j=1}^l i_{dc,j} \quad (7)$$

In steady-state, $\sum_{j=1}^l i_{dc,j} = \sum_{i=1}^m i_{dc,i} = \sum_{i=1}^m \frac{P_{0,i}}{V_{dc0,i}}$ is obtained. Thus, to avoid the multiple crossovers, k_{droop} should be selected as $k_{droop} < \frac{m}{\left| \sum_{j=1}^l i_{dc,j} \right|} = \frac{m}{\left| \sum_{i=1}^m \frac{P_{0,i}}{V_{dc0,i}} \right|}$.

2) *Droop gain selection considering the dc voltage balancing*: The selection of k_{droop} should also consider the dc voltage balancing performance, otherwise the system may become unstable. To select a suitable k_{droop} , the system model including the main circuits and control parts is developed. It is assumed that components of all SMs have identical parameters and that slight differences due to manufacturing tolerances are omitted. The total power/voltage of converter and the individual dc voltage of SMs can be independently controlled as an input-series-output-parallel converter [29]. Thus, a single SM is chosen for tuning the droop gain.

The state-space representation of the i^{th} SM considering the current control loop is:

$$\frac{d}{dt} \begin{bmatrix} \Delta x_{id,i} \\ \Delta x_{iq,i} \\ \Delta i_{di} \\ \Delta i_{qi} \\ \Delta v_{dci} \end{bmatrix} = \mathbf{A} \begin{bmatrix} \Delta x_{id,i} \\ \Delta x_{iq,i} \\ \Delta i_{di} \\ \Delta i_{qi} \\ \Delta v_{dci} \end{bmatrix} + \mathbf{B} \lambda \begin{bmatrix} \Delta i_{di}^* \\ \Delta i_{qi}^* \\ \Delta v_{dci} \end{bmatrix} \quad (8)$$

In the adopted notation, ' Δ ' stands for perturbed variables. i_{di}^* is the reference of active current, i_{qi}^* is the reference of reactive current, i_{dc} is the dc link current, i_{di} is the d -axis current, i_{qi} is the q -axis current, and v_{dci} is the dc voltage. $x_{id,i}$ and $x_{iq,i}$ are the outputs of the integral action of the current PI controller. The matrices \mathbf{A} and \mathbf{B} and their derivation processes are referred to equation (1), Section II-D in [23]. $\lambda = \text{diag} \left(\frac{3V_s}{2}, \frac{3V_s}{2}, 1 \right)$ is a diagonal matrix, where V_s is the RMS value of grid voltage.

The transfer function of Δi_{di}^* to Δv_{dci} is given as

$$\Delta v_{dci} = \frac{[\mathbf{C}_1 (s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}']}{G_1(s)} \Delta i_{di}^* = G_1(s) \Delta i_{di}^* \quad (9)$$

where $\mathbf{C}_1 = [0 \ 0 \ 0 \ 0 \ 1]$. \mathbf{B}' has a dimension of 5×1 , representing the first column vector of $\mathbf{B}\lambda$. With use of the droop controller, there are

$$\begin{aligned} \Delta i_{di}^* &= G_{PI}(s) (\Delta v_{dci}^* - \Delta v_{dci}) \\ &= G_{PI}(s) (-k_{droop} (\Delta p_{drp,i} - \Delta p_{0,i}) + \Delta v_{dc0,i} - \Delta v_{dci,i}) \end{aligned} \quad (10)$$

$$\Delta p_{drp,i} = \frac{3V_s}{2} \Delta i_{di} \quad (11)$$

$$\Delta i_{di} = \frac{[\mathbf{C}_2 (s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}']}{G_2(s)} \Delta i_{di}^* = G_2(s) \Delta i_{di}^* \quad (12)$$

where $\mathbf{C}_2 = [0 \ 0 \ 1 \ 0 \ 0]$. $\Delta v_{dc0,i} = \frac{\Delta v_{dc0}}{2N}$ and $\Delta p_{0,i} =$

$\frac{\Delta p_0}{2N}$ are selected to achieve the dc voltage and power balancing. $G_{PI}(s) = \frac{K_{pvb}s + K_{ivb}}{s}$ is the outer-loop PI controller. Combining (9)–(12), the closed-loop transfer function of $\Delta v_{dc0,i}$ to Δv_{dci} for the i^{th} SM is obtained as

$$G_{vb}(s) = \frac{\Delta v_{dci}}{\Delta v_{dc0,i}} = \frac{G_{PI}(s)G_1(s)}{1 + 1.5k_{droop}V_sG_{PI}(s)G_2(s) + G_{PI}(s)G_1(s)} \quad (13)$$

The open-loop transfer function corresponding to (11) is

$$G_{vb_open}(s) = \frac{G_{PI}(s)G_1(s)}{1 + 1.5k_{droop}V_sG_{PI}(s)G_2(s)} \quad (14)$$

When k_{droop} is increased, the closed-loop poles' trajectories of $G_{vb}(s)$ are shown in Fig. 7. The main circuit and controller parameters used in the modelling are listed in Table I and II.

TABLE I. PARAMETERS OF EACH C3L-NPC SM

Power rating S	2.5 kVA	DC link voltage V_{DC}	90 V
RMS value of AC grid voltage	415 V	Transformer ratio	Y-415 V/Δ-41.5 V
L inductance	0.5 mH	DC capacitance	5400 μF

TABLE II. CONTROL PARAMETERS OF SMS

Proportional parameter of d -axis current controller	100	Integral parameter of d -axis current controller	20
Proportional parameter of q -axis current controller	100	Integral parameter of q -axis current controller	20
Proportional parameter of dc voltage balancing controller	6.8	Integral parameter of dc voltage balancing controller	1000

Fig. 7(a) shows the trajectories of three dominant closed-loop poles (λ_1, λ_2 and λ_3) under positive power flow while Fig. 7(b) shows the zoom-in view where the threshold of the k_{droop} that makes system stable is displayed. The real part represents the exponential rate of decay, while the imaginary part represents the oscillation frequency. The left-half plane with negative real part denotes the stable region. The system will become unstable if the poles locate on the right-half plane. It can be seen that the dominant pole λ_3 will move to the right half s-plane (unstable region) with increase of k_{droop} . As shown in Fig. 7(b), the λ_3 reaches zero when k_{droop} is 0.0402, which is the threshold value of k_{droop} that makes the system stable.

Fig. 8 shows the Bode diagram of $G_{vb_open}(s)$. In the Bode diagram, k_{droop} are changed from 0.008 to 0.038 to test the system performance under different droop slopes. As can be seen, $G_{vb_open}(s)$ has a lower bandwidth with increase of k_{droop} , which can affect the dc voltage balancing performance. Although dc voltage balancing can be improved with higher bandwidth using a smaller droop gain, the advantages of multiple-droop characteristics will be sacrificed. Thus, $k_{droop} = 0.023$ is selected as the optimal gain K_{droop_opt} , which achieves a suitable trade-off between dc voltage balancing and multiple-droop characteristics.

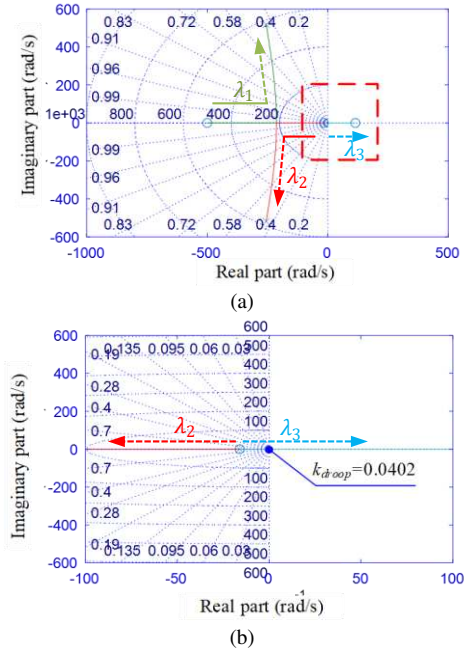


Fig. 7. Closed-loop poles' trajectories in equation (13) as k_{droop} increases. (a) Dominant poles' trajectories. (b) Zoom-in view of dominant poles' trajectories.

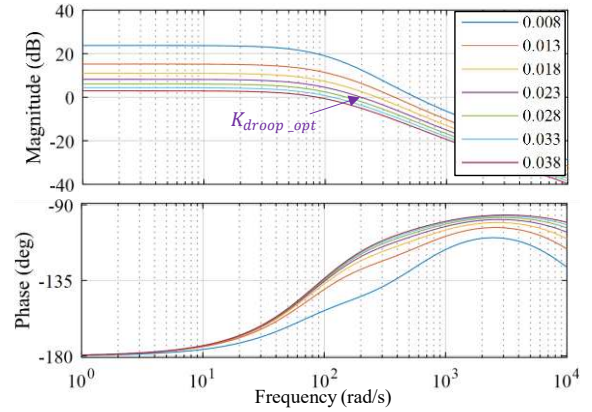


Fig. 8. Bode diagram of $G_{vb_open}(s)$ under different k_{droop} .

To further verify the selected K_{droop_opt} , the root locus under uncertainties of component parameters is tested. The dc capacitance and ac inductance change from 80% to 120% of the nominal value, and the corresponding trajectories of dominant poles are shown in Fig. 9(a) and Fig. 9(b), respectively. It can be seen that the imaginary parts of λ_1 and λ_2 are obviously decreased as dc capacitance increases, while the poles have a slight change with increase of inductance. Nevertheless, for both cases, the dominant poles remain locating at the left-half s plane, which indicates the robustness of the system to parameter uncertainties.

Therefore, to avoid multiple crossovers and to concurrently achieve dc voltage balancing, the k_{droop} of the narrow band should be selected as the lowest value of the result obtained from (7) and the threshold value in Fig. 7.

$$k_{droop} = \min \left(\frac{m}{\left| \sum_{j=1}^l i_{dc,j} \right|}, K_{droop_opt} \right) \quad (15)$$

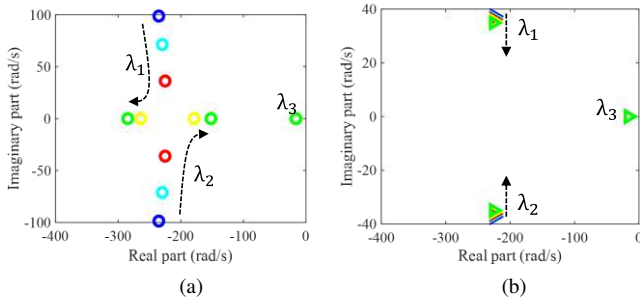


Fig. 9. Trajectories of dominant poles under uncertainties of dc capacitance and ac inductance. (a) Change of dc capacitance from 80% to 120% of the nominal value. (b) Change of ac inductance from 80% to 120% of the nominal value.

C. Secondary Power Compensator

Since a smaller droop gain is used to avoid multiple crossovers, a potential large power offset may occur under the dynamic change of dc current. This reduces the accuracy of power control and sacrifices the advantages of using the narrow band in the piecewise droop control. In this section, a secondary power compensator is presented to compensate the potential large power offset. First, the mathematical model of the second power compensator is derived. Then, analyses are performed to justify the rationality of the adopted power compensator. It is indicated that the power compensation can be achieved without affecting the dynamics of droop control loop by using the LPF and suitably designing the controller gain. Finally, the transfer function of the system from input to output is derived for controller parameter tuning and stability analysis.

As shown in the blue rectangular in Fig. 6, the secondary power compensator is embedded in each SM. It consists of a proportional gain k_{comp} and an LPF. The desired operating point $P_{0,n}$ is compared with the average power of SMs, the error is mitigated by k_{comp} through the feedback control loop. The LPF is used to filter the noises of the power. Also, the dynamics of the power compensator is decreased due to the use of LPF, so that the power compensating loop and the droop loop can be decoupled. The compensation term $v_{dc0,i}^c$ is superposed to $v_{dc0,i}$ to mitigate the drift of power flow. $v_{dc0,i}^c$ is obtained from a LPF and given as

$$\Delta v_{dc0,i}^c = k_{comp} \frac{1}{\tau s + 1} (\Delta p_{drp,avg} - \Delta p_{0,i}) \quad (16)$$

$$\Delta p_{drp,avg} = \frac{\sum_{i=1}^n \Delta p_{drp,i}}{n} \quad (17)$$

where k_{comp} is the proportional gain of the compensator, τ is the time constant of the LPF and $p_{drp,avg}$ is the average power of all SMs. It is noted that the $p_{drp,avg}$ in Fig. 6 is sent by the high-level controller, so there is a slight time delay. This delay is around 2 ms with Modbus based communication,

which can be omitted since the bandwidth of the power compensator loop is much lower. Thus the dynamics due to the communication delay has been omitted in the model. After adding the compensator, Δi_{di}^* in (10) is expressed as

$$\begin{aligned} \Delta i_{di}^* &= G_{PI}(s) (\Delta v_{dc,i}^* - \Delta v_{dc,i}) \\ &= G_{PI}(s) \left(-k_{droop} (\Delta p_{drp,i} - \Delta p_{0,i}) \right. \\ &\quad \left. + \Delta v_{dc0,i} + \frac{k_{comp}}{\tau s + 1} (\Delta p_{drp,avg} - \Delta p_{0,i}) \right. \\ &\quad \left. - \Delta v_{dc,i} \right) \end{aligned} \quad (18)$$

Combining (9), (11), (12) and (18), we can obtain the sensitivity of $\Delta p_{drp,i}$ to $\Delta v_{dc,i}$ by setting $\Delta p_{0,i}$ and $\Delta v_{dc0,i}$ to zero. The sensitivity of $\Delta p_{drp,i}$ to $\Delta v_{dc,i}$ in each SM is shown in (19). Summing up all equations in (19) yields the sensitivity of the total output power (Δp_{drp}) to the dc link voltage (Δv_{dc}) which is shown in (20).

$$\begin{cases} \Delta v_{dc,1} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)} \left(k_{droop} \Delta p_{drp,1} - \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg} \right) \\ \Delta v_{dc,2} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)} \left(k_{droop} \Delta p_{drp,2} - \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg} \right) \\ \Delta v_{dc,n} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)} \left(k_{droop} \Delta p_{drp,n} - \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg} \right) \end{cases} \quad (19)$$

$$\begin{aligned} \Delta v_{dc} &= \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)} \sum_{i=1}^n \left(k_{droop} \Delta p_{drp,i} - \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg} \right) \\ &= \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)} \left(k_{droop} - \frac{k_{comp}}{\tau s + 1} \right) \Delta p_{drp} \end{aligned} \quad (20)$$

In (20), due to the low-pass filtering effect of $\frac{k_{comp}}{\tau s + 1}$, the power compensator has little impact on the sensitivity of the power against dc voltage and hence, the droop characteristic is still determined by k_{droop} .

The k_{comp} can be reasonably selected by studying the transfer function of the secondary power compensating loop. Combining (9), (11), (12) and (18), the relationship between Δp_{i0} and $\Delta p_{drp,i}$ is given in (21) at the bottom of this page.

Combining all equations in (21) yields (22). By rearranging (22), the closed-loop transfer function of Δp_0 to Δp_{drp} is obtained as

$$G_P(s) = \frac{\Delta p_{drp}}{\Delta p_0} = \frac{3V_s G_{PI}(s) G_2(s) (k_{droop} - \frac{k_{comp}}{\tau s + 1})}{2(1 + G_1(s)G_{PI}(s)) + 3V_s G_{PI}(s) G_2(s) (k_{droop} - \frac{k_{comp}}{\tau s + 1})} \quad (23)$$

The open-loop transfer function corresponding to (21) is

$$G_{P,open}(s) = \frac{3V_s G_{PI}(s) G_2(s) (k_{droop} - \frac{k_{comp}}{\tau s + 1})}{2(1 + G_1(s)G_{PI}(s))} \quad (24)$$

The closed-loop pole trajectory with increase of k_{comp} is shown in Fig. 10.

$$\begin{cases} \Delta p_{drp,1} = \frac{3V_s G_{PI}(s) G_2(s)}{2(1+G_1(s)G_{PI}(s))+3k_{droop}V_s G_{PI}(s)G_2(s)} (\Delta p_{10} (k_{droop} + \frac{k_{comp}}{\tau s + 1}) + \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg}) \\ \Delta p_{drp,2} = \frac{3V_s G_{PI}(s) G_2(s)}{2(1+G_1(s)G_{PI}(s))+3k_{droop}V_s G_{PI}(s)G_2(s)} (\Delta p_{20} (k_{droop} + \frac{k_{comp}}{\tau s + 1}) + \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg}) \\ \Delta p_{drp,n} = \frac{3V_s G_{PI}(s) G_2(s)}{2(1+G_1(s)G_{PI}(s))+3k_{droop}V_s G_{PI}(s)G_2(s)} (\Delta p_{n0} (k_{droop} + \frac{k_{comp}}{\tau s + 1}) + \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg}) \end{cases} \quad (21)$$

$$\sum_{i=1}^n \Delta p_{drp,i} = \frac{3V_s G_{PI}(s) G_2(s)}{2(1+G_1(s)G_{PI}(s))+3k_{droop}V_s G_{PI}(s)G_2(s)} (\sum_{i=1}^n \Delta p_{i0} (k_{droop} + \frac{k_{comp}}{\tau s + 1}) + n \frac{k_{comp}}{\tau s + 1} \Delta p_{drp,avg}) \quad (22)$$

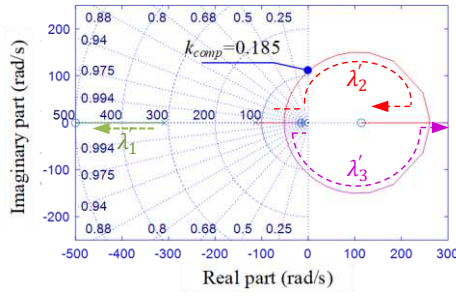


Fig. 10. Closed-loop poles' trajectories in equation (23) as k_{comp} increases.

As can be seen in Fig. 10, a pair of conjugate poles will move to the right half s-plane when k_{comp} is greater than 0.185. Thus the k_{comp} should be selected less than the upper bound. To decouple the dynamics between the secondary power compensating loop and the droop control loop, the response speed of the secondary power compensating loop should be 5–10 times slower than that of the droop control loop. The open loop Bode diagram of the secondary power compensator ($G_{p_open}(s)$) with $k_{comp} = 0.085$ is shown in Fig. 11. The cut-off frequency of $G_{p_open}(s)$ is 20 rad/s, which has 1/10 times the bandwidth of the droop control loop (by comparing the red solid line and green dashed line in Fig. 11). Thus, the dynamics of the two control loops can be decoupled. Therefore, $k_{comp} = 0.085$ is used for the case study of simulation in Section V.

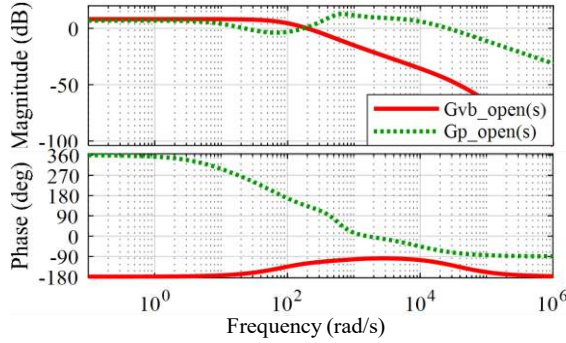


Fig. 11. Bode plots of $G_{vb_open}(s)$ and $G_{p_open}(s)$ with $k_{comp} = 0.085$, $\tau = 0.1$.

V. SIMULATION AND EXPERIMENTAL STUDIES

A. Simulation Verification

The simulation is conducted in MATLAB/Simulink for the three-terminal system shown in Fig. 2, including two C3L-NPC converters (Stations 1 and 2) and a converter operated as a controllable current source (Station 3). Both C3L-NPC converter stations work under $P - V_{dc}$ droop control while the converter station 3 under dc current control. To verify the presented methods, three studies are performed:

- *Study 1:* The droop control is implemented without optimized tuning of droop gain (see Fig. 12).
- *Study 2:* The droop control is implemented with optimized tuning of droop gain by considering multiple crossovers and dc voltage balancing across SMs (see Fig. 13).
- *Study 3:* The second power compensator is added to improve the power flow accuracy (see Fig. 14 and Fig. 15).

The power and voltage references of the droop controller for all the case studies (Fig. 12 to Fig. 15) are $P_0 = 10$ kW and $V_{dc0} = 360$ V, respectively. The dc current reference for the dc current-controlled converter is set as $I_{dc0} = 55$ A. Considering the potential overshoot at the start-up stage, the dc current references are modified using ramp functions with slopes of 137.5 A/s to achieve a smooth dynamic behavior, as opposed to step changes. The minimum voltage is set as 280 V (70 V for each SM). When dc voltage falls below 280 V, the control mode is switched to constant dc voltage control so that the dc voltage is maintained at 280 V.

Figs. 12 to 15 show the dc current output from the converter station 3 and the dc voltage and power of the C3L-NPC converter of Stations 1 and 2. Fig. 12 shows the case of multiple crossovers when k_{droop} of the narrow band is 0.06, which is less than the value defined in (15). In Fig. 12(a), the dc current can track the reference with a slight error. Due to the multiple crossovers, the operating points of power and dc voltage deviate from the given references. In Fig. 12(b), the power shifts from the setting point by around 2.8 kW. In Fig. 12(c), the dc voltage decreases to the minimum voltage (280 V) according to the droop curve.

Fig. 13 shows that the multiple crossovers are eliminated when k_{droop} is properly selected as $k_{droop} = 0.023$. As seen in Fig. 13(b) and (c), the operating power and voltage are much closer to the references compared with Fig. 12. The error of 0.7 kW in active power is caused by the steady-state error of controller rather than the multiple crossovers. Also, the dc voltage across SMs is balanced well, as shown in Fig. 13(d).

Fig. 14 shows the accuracy of power flow is deteriorated under dynamic change of dc current when the secondary power compensator is not used. In Fig. 14(a), the current reference of the current-controlled converter has a slight change from 55 A to 40 A after 0.7s. Since a smaller k_{droop} is used, the power flow become higher sensitive to a perturbation in dc current. As a consequence, a power drift of 4 kW arises in Fig. 14(b), which proves that the power control accuracy of the narrow band becomes worse.

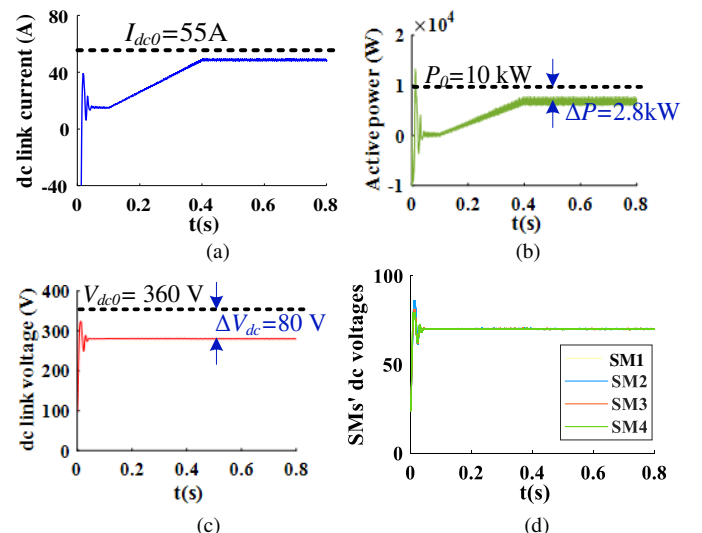


Fig. 12. Multiple crossovers when k_{droop} is 0.06. (a) dc current. (b) total power. (c) dc link voltage. (d) SMs' dc voltages.

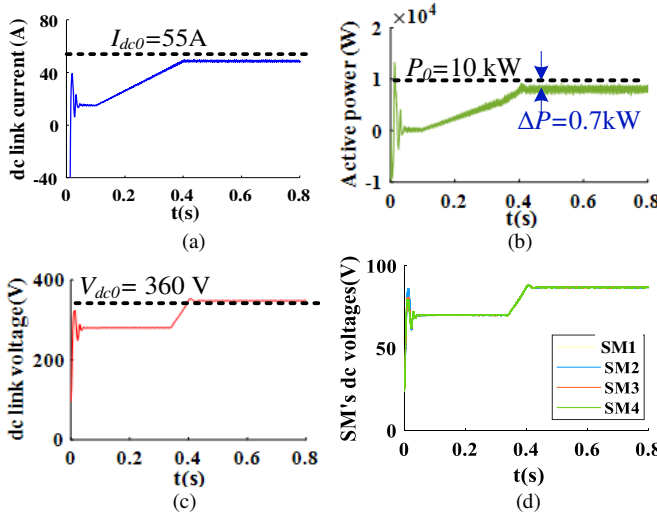


Fig. 13. No multiple crossovers when k_{droop} is 0.023. (a) dc current. (b) total power. (c) dc link voltage. (d) SMs' dc voltages.

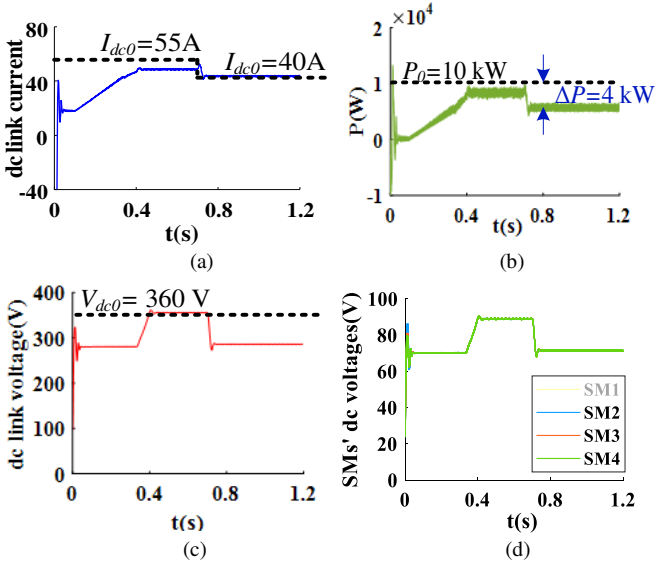


Fig. 14. Power drift under dynamic change of dc current without using secondary power compensating controller. (a) dc current. (b) total power. (c) dc link voltage. (d) SMs' dc voltages.

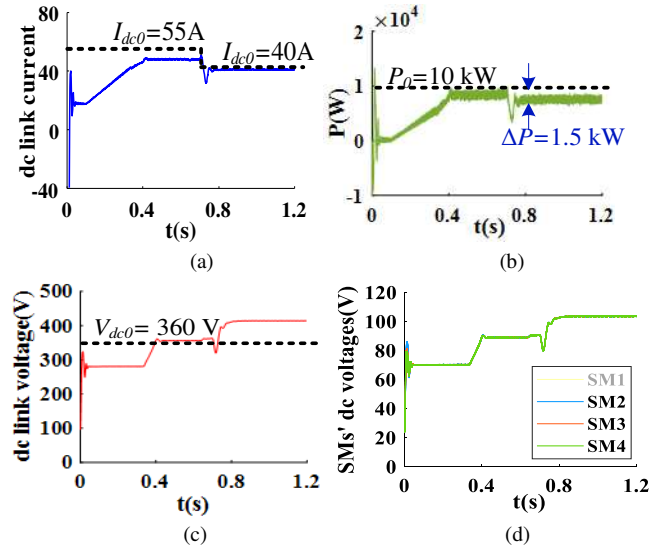


Fig. 15. Improved power control accuracy with using secondary power compensating controller. (a) dc current. (b) total power. (c) dc link voltage. (d) SMs' dc voltages.

Fig. 15 shows the improved performance after implementing the secondary power compensator. As can be seen, although the dc current drops down, the power can be nearly restored to the desired value by increasing the dc voltage (see Fig. 15(c) and (d)). Thus, the secondary compensating loop is useful for the application where an accurate power control is required.

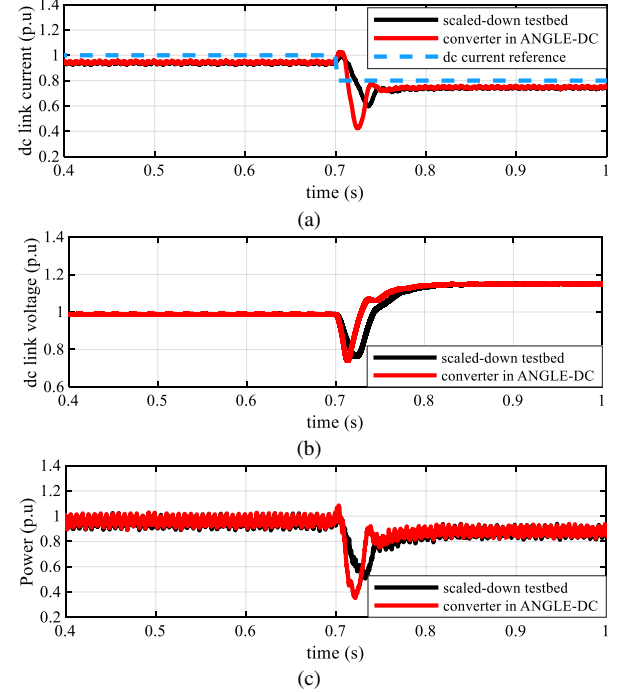


Fig. 16. Comparisons between scaled-down converters and full-scale converters in ANGLE-DC project under per-unit values. (a) dc link current. (b) dc link voltage. (c) active power.

The comparisons between scaled-down C3L-NPC converters and full-scale converters in ANGLE-DC project under per-unit values are shown in Fig. 16. In time 0.7 s, the reference of dc current has a step change from 1 p.u. to 0.8 p.u. The dc voltage and power have a transient drop as a consequence. Due to the effect of the power compensator, the power will increase and restore to around 0.85 p.u. after time 0.75 s. The scaled-down and full-scale simulation have similar performance with a slight mismatch in dynamic response.

B. Experimental Validation

The presented control schemes were experimentally validated using a three-terminal MVdc testbed consisting of two C3L-NPC converter stations and a dc power supply. The hardware configuration of the system is shown in Fig. 17.

The C3L-NPC converters were a scaled-down physical replica of the ANGLE-DC MVdc converters to accurately emulating the real system response [23]. For each C3L-NPC converter station, two 3L-NPC SMs were cascaded to build a 180 V dc link voltage, with each SM is operated at 90 V. A power amplifier (PA-3*3000-AB/260/2G) is used to establish the ac voltage (415 V/50 Hz) for the C3L-NPC converter stations. The dc power supply is EA-PS 9200-25 rated at 1.5 kW. The dc power supply is operated in current source mode to provide desired dc current. Since the operation conditions of the two C3L-NPC converters are identical, only the measurements

of one C3L-NPC converter are presented in the results.



Fig. 17. Three-terminal MVdc configuration, including two C3L-NPC converter stations and a dc power supply operated at current-controlled mode.

Fig. 18 shows the waveforms under multiple crossings. The references of each C3L-NPC converter station are set as $P_0 = 750$ W and $V_{dc0} = 180$ V, and the current of dc power supply is adjusted from 0 to around 8.3 A. A set of comparative tests was conducted to verify the selection of k_{droop} with and without considering multiple crossovers. As the threshold is $\frac{2}{8.3} = 0.24$, a k_{droop} larger than the threshold (e.g., $k_{droop} = 0.36$) and a k_{droop} smaller than the threshold (e.g., $k_{droop} = 0.072$) are selected for case studies in Figs. 18 and 19. In Fig. 18(a), due to the existence of multiple crossings, the dc voltage of each SM at steady state is 80 V, which is 10 V less than the given voltage. In Fig. 18(b), the steady-state power is around 1.25 kW, which is 0.25 kW less than the given value.

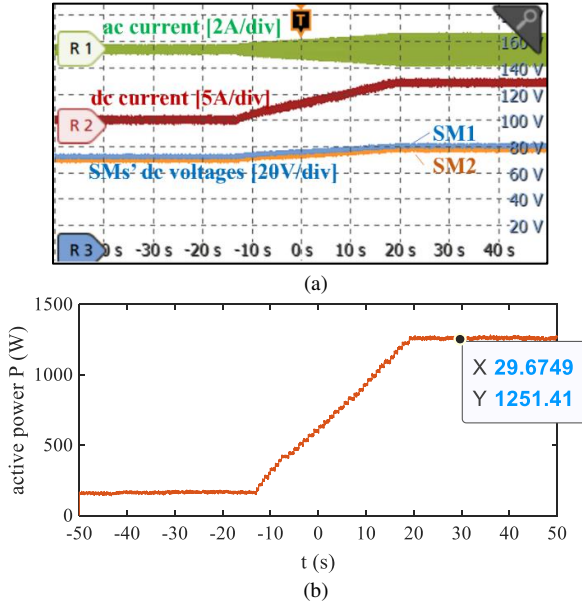


Fig. 18. Waveforms when k_{droop} is set to 0.36. (a) Currents and dc voltages. (b) Output power from dc power supply.

The multiple crossings are avoided in Fig. 19 when k_{droop} decreases to 0.072, less than 0.24. As seen in Fig. 19(a) and (b), the drifts of dc voltage and power are effectively mitigated and thus the desired operating point is achieved. Compared with the Fig. 18(b), the steady power has been improved by around 15%. Also, the SMs' dc voltages are well balanced.

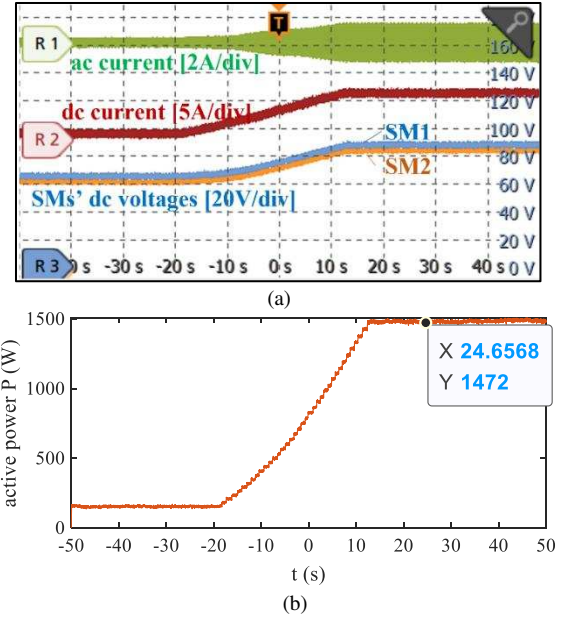


Fig. 19. Waveforms when k_{droop} is set to 0.072. (a) Currents and dc voltages. (b) Output power from dc power supply.

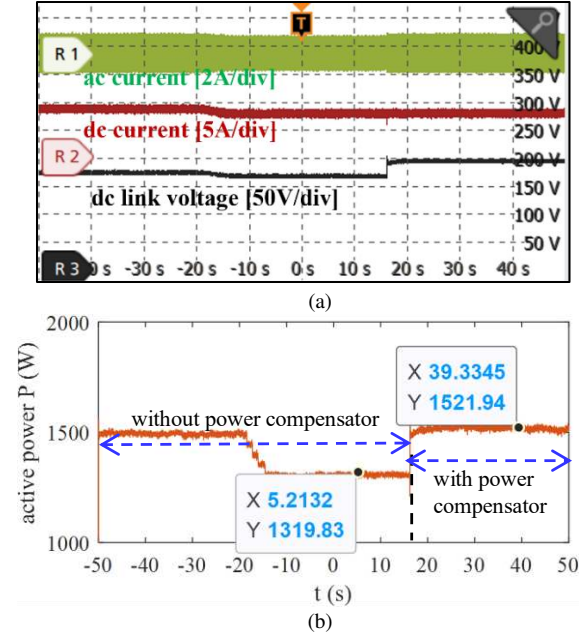


Fig. 20. Waveforms under dc current change, with and without secondary power compensator. (a) Currents and dc voltage. (b) Output power from dc power supply.

Fig. 20(a) shows the deterioration of accuracy of power flow under dynamic changes of dc current and the improved performance after enabling the secondary power compensator. The dc current changes from around 8 A to 7.2 A after time -20 s. Consequently, there is a 200 W power drift (see Fig. 20(b)) due to a dynamic change of dc current without using the secondary power compensator. To pursue an accurate power control performance, the secondary power compensating controller is enabled after time 16 s. The power quickly restores to the similar level of the original operating point. In Fig. 20(b), the power control accuracy has been improved by about 13% through comparing the power with and without using the power compensator under the change of dc current after time -20 s. As

dc voltage is inevitably increased, the overvoltage protection should be considered according to the requirements in real applications. From the perspective of power accuracy, the presented methods are validated to be effective.

VI. CONCLUSION

Multiple crossovers may exist in a multi-terminal MVdc system with decentralized control. This can cause significant voltage and power drifts, raising concerns of safe operation of the system. This paper first analyzed the voltage and power drifts in the multiple crossovers. Then, a suitable control scheme was presented to avoid the multiple crossovers and concurrently, to achieve dc voltage balancing across SMs and the accuracy of power flow for C3L-NPC converters.

Multiple crossovers may appear when C3L-NPC converters adopt the voltage–power droop control while another converter adopts the constant dc current control. Through analysis on the physical mechanism, the normal operating point is unstable in multiple crossovers, and may move away due to a disturbance. This leads to large power and voltage drifts, which are not desired in practical applications.

Decreasing the droop gain is beneficial for both eliminating multiple crossovers and improving dc voltage balancing performance, but this is at the cost of decreasing the accuracy of power flow. To address such a trade-off, in the first step, the droop gain was properly selected by considering the multiple crossovers and dc voltage balancing performance. The small-signal analysis is used to design the droop gain to achieve satisfactory bandwidth and phase margin. In the second step, a secondary power compensator was used to ensure the accuracy of power control. Thus the power restores to the given reference after suffering from a disturbance such as a dynamic change of dc current. The theoretical analyses and presented control methods have been verified by MATLAB simulation and also experimentally validated using a 1.5 kW three-terminal MVdc testbed, which is down scaled from the ANGLE-DC project.

REFERENCES

- [1] S. Faddel, A. A. Saad, T. Youssef and O. Mohammed, "Decentralized Control Algorithm for the Hybrid Energy Storage of Shipboard Power System," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 720-731, Mar. 2020.
- [2] X. Chen et al., "A Novel Virtual Resistor and Capacitor Droop Control for HESS in Medium-Voltage DC System," *IEEE Trans. Power Syst.*, vol. 34, no. 4, pp. 2518-2527, July 2019.
- [3] A. Eggi, S. Karagiannopoulos, S. Bolognani and G. Hug, "Stability Analysis and Design of Local Control Schemes in Active Distribution Grids," *IEEE Trans. Power Syst.*, vol. 36, no. 3, pp. 1900-1909, May 2021.
- [4] P. Simiyu et al., "Adaptive Droop Control of Multi-Terminal MVDC Distribution Network for High Solar PV Penetration," in *2018 2nd IEEE Conf. EI2*, 2018, pp. 1-6.
- [5] T.K. Vrana, J. Beerten, R. Belmans, O.B. Fosfo, "A classification of DC node voltage control methods for HVDC grids," *Electr. Power Syst. Res.*, vol. 103, pp. 137-144, Oct. 2013.
- [6] M. S. Golsorkhi and M. Savaghebi, "A Decentralized Control Strategy Based on V-I Droop for Enhancing Dynamics of Autonomous Hybrid AC/DC Microgrids," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9430-9440, Aug. 2021.
- [7] F. Chen, R. Burgos, D. Boroyevich, J. C. Vasquez and J. M. Guerrero, "Investigation of Nonlinear Droop Control in DC Power Distribution Systems: Load Sharing, Voltage Regulation, Efficiency, and Stability," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9404-9421, Oct. 2019.
- [8] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna and P. Rodriguez, "A Generalized Voltage Droop Strategy for Control of Multiterminal DC Grids," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 607-618, Jan.-Feb. 2015.
- [9] L. Zhang et al., "Modeling, control, and protection of modular multilevel converter-based multi-terminal HVDC systems: A review," *CSEE J. Power Energy Syst.*, vol. 3, no. 4, pp. 340-352, Dec. 2017.
- [10] L. Bibaya, C. Liu and G. Li, "An Improved Coordinated Control Strategy of VSC-MTDC Distribution Network," in *2018 2nd IEEE Conf. EI2*, Beijing, China, 2018, pp. 1-7.
- [11] S. Liu, J. Zheng, Z. Li, R. Li, W. Fang, X. Liu, "Distributed Piecewise Droop Control of DC Microgrid with Improved Load Sharing and Voltage Compensation," in *Proc. 2019 IEEE ICDCM*, Japan, May 2019, pp. 1-6.
- [12] C. Barker, R. Whitehouse, J. Liang, S. Wang, "Risk of multiple crossover of control characteristics in multi-terminal HVDC," *IET Gener. Transm. Distrib.*, vol. 10, pp. 1353-1360, 2016.
- [13] J. Chen et al., "Demonstration of Converter Control Interactions in MMC-HVDC Systems," *Electron.*, vol. 11, no. 2, 2022.
- [14] M. Borage, S. Tiwari and S. Kotaiah, "LCL-T Resonant Converter With Clamp Diodes: A Novel Constant-Current Power Supply With Inherent Constant-Voltage Limit," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 741-746, April 2007.
- [15] R. G. Retegui, M. Benedetti, M. Funes, P. Antoszczuk and D. Carrica, "Current Control for High-Dynamic High-Power Multiphase Buck Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 614-618, Feb. 2012.
- [16] Z. Lin et al., "A Novel Single-Input Multi-output DC/DC Converter With Constant Current Mode Operation," in *31st conf. AUPEC*, 2021, pp. 1-5.
- [17] C. Barker, R. Whitehouse, S. Wang and J. Lang, "Risk of Multiple Crossover of Control Characteristics in Multiterminal HVDC," in *11th IET Int. Conf. ACDC*, Birmingham, 2015, pp. 1-7.
- [18] T. Fang et al., "Control Scheme to Achieve Multiple Objectives and Superior Reliability for Input-Series-Output-Parallel LCL-Type Grid-Connected Inverter System," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 214-224, Jan. 2020.
- [19] W. Chen and G. Wang, "Decentralized Voltage-Sharing Control Strategy for Fully Modular Input-Series-Output-Series System with Improved Voltage Regulation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2777-2787, May 2015.
- [20] M. Urizarbarrena, "ANGLE-DC - 2015 Network Innovation Competition", NIC final submission document, 2015. [Online]. Available: <https://www.ofgem.gov.uk/ofgem-publications/97841/anglesubmission-pdf>
- [21] T. Joseph, J. Liang, G. Li, A. Moon, K. Smith and J. Yu, "Dynamic control of MVDC link embedded in distribution network: — Case study on ANGLE-DC," in *IEEE Conf. EI2*, 2017, pp. 1-6.
- [22] G. Abeynayake, G. Li, T. Joseph, J. Liang and W. Ming, "Reliability and Cost-Oriented Analysis, Comparison and Selection of Multi-Level MVdc Converters," *IEEE Trans. Power Del.*, vol. 36, no. 6, pp. 3945-3955, Dec. 2021.
- [23] J. Chen, W. Ming, C. E. Ugalde-Loo, S. Wang and N. Jenkins, "Analysis and Mitigation of DC Voltage Imbalance for Medium-Voltage Cascaded Three-Level Neutral-Point-Clamped Converters," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4320-4336, Apr. 2022.
- [24] R. Sarrias-Mena, L. M. Fernández-Ramírez, C. A. García-Vázquez, C. E. Ugalde-Loo, N. Jenkins and F. Jurado, "Modelling and control of a medium-voltage DC distribution system with energy storage," in *2016 IEEE Int. Conf. ENERGYCON*, 2016, pp. 1-6.
- [25] W. Chen, X. Jiang, W. Cao, J. Zhao, W. Jiang and L. Jiang, "A Fully Modular Control Strategy for Input-Series Output-Parallel (ISOP) Inverter System Based on Positive Output-Voltage-Amplitude Gradient," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2878-2887, Apr. 2018.
- [26] W. Chen, G. Wang, X. Ruan, W. Jiang, and W. Gu, "Wireless input voltage-sharing control strategy for input-series output-parallel (ISOP) system based on positive output-voltage gradient method," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6022-6030, Nov. 2014.
- [27] G. Xu, D. Sha, and X. Liao, "Decentralized inverse-droop control for input-series-output-parallel DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4621-4625, Sep. 2015.
- [28] C. D. Barker and R. S. Whitehouse, "Further developments in autonomous converter control in a multi-terminal HVDC system," in *10th IET Int. Conf. ACDC*, Birmingham, 2012, pp. 1-6.
- [29] X. Ruan, et al., "Control Strategy for Input-Series-Output-Parallel Converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1174-1185, Apr. 2009.



Jinlei Chen received the B.Eng. and M.Eng. Degrees in automation from Shandong University, Jinan, China, in 2015 and 2018, respectively, and the Ph.D. degree in electrical engineering with Cardiff University, Cardiff, U.K. He has been a Research Assistant with Cardiff University, Cardiff, U.K. since 2018, and a visiting Research Fellow with Compound Semiconductor Applications (CSA) Catapult, U.K. since 2022. His research interests include control of medium-voltage dc power converters and modeling of compound semiconductor devices.



Sheng Wang (M'17) received the B.Eng. degree from both Cardiff University, U.K. and North China Electric Power University, China in 2011. He received the Ph.D. degree from Cardiff University, U.K., in 2016. Between 2013–2014, 2016–2018 and 2018–2020, he was a Research Assistant, a Research Associate and a KTP Associate with Cardiff University, U.K. Since 2020, he has been a Lecturer with the School of Engineering, Cardiff University. He is the Vice-Chair of IEEE PELS

UK&I Chapter and Research Fellow at Compound Semiconductor Applications (CSA) Catapult. His current research interests include active gate drivers, power electronic devices, wide-bandgap semiconductors, control and protection of HVDC and MVDC.



Jun Liang (M'02-SM'12) received the B.Sc. degree from Huazhong University of Science and Technology, Wuhan China in 1992, and the M.Sc. and Ph.D. degrees from China Electric Power Research Institute, Beijing China in 1995 and 1998 respectively. From 1998 to 2001, he was a Senior Engineer with China Electric Power Research Institute. From 2001 to 2005, he was a Research Associate at Imperial College, London, UK. From 2005 to 2007, he was a Senior Lecturer at the University of

Glamorgan, Wales UK. Currently, he is a Professor at the School of Engineering, Cardiff University, Wales UK. His research interests include DC technologies, power electronics, power system stability control, and renewable power generation.



Rukshan Navaratne obtained his PhD in Aerospace Engineering at Cranfield University and currently working as a Reader and Leading the Aerospace Propulsion Research at Cardiff University. Before joining academia, he has spent much of his career working as an Engineer, Project Manager and Senior Executive in aerospace industry. His current research

focuses on the development of novel electric propulsion systems, electrical machine modelling, and design optimisation of advanced novel propulsion systems. Rukshan use variety of numerical and experimental tools and techniques to develop propulsion technologies from initial conception through increasing levels of technology readiness with a constant view towards commercialization and real-world use. Also, he is a consultant to several local and international organisations. Rukshan is a Chartered Engineer and Member of IMechE (UK), ASME, and AIAA.



Wenlong Ming (M'16) received the B.Eng. and M.Eng. Degrees in Automation from Shandong University, Jinan, China, in 2007 and 2010, respectively. He received the Ph.D. degree in Automatic Control and Systems Engineering from the University of Sheffield, Sheffield, U.K., in 2015. He is the winner of the prestigious IET Control & Automation Doctoral Dissertation Prize in 2017. He has been a Senior Lecturer of Power Electronics at Cardiff University, U.K., since August 2020 and a Senior Research Fellow funded by Compound Semiconductor Applications (CSA) Catapult, U.K., for 5 years since April 2020.

He was with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA in 2012 as an academic visiting scholar. He has (co-)authored more than 60 papers published in leading journals or refereed IEEE conferences. His research interests focus on packaging, characterisation, modelling and applications of wide-bandgap compound semiconductor power devices.