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A Test Platform for Dependability Analysis of SoCs Exposed to EMI and Radiation

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Abstract With the IEC 62.132 proposal, the roadmap for standardization of Electromagnetic (EM) immunity measurement methods has reached a high degree of success. The same understanding can be taken from the MIL-STD-883 H for Total Ionizing Dose (TID) radiation. However, no effort has been made to measure the behavior of electronics operating under the combined effects of both, EM noise and TID radiation. For the reasons pointed out, the combined-effect measurements should be mandatory when dealing with Systems-on-Chip (SoCs) devoted to critical applications. In this paper, we present a configurable platform devoted to perform combined tests of EM immunity and TID radiation of SoCs according to the international standards.

Keywords System-on-Chip · Electromagnetic Interference · Total-Ionizing Dose Radiation · Testing Platform

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1 Introduction

With the widespread use of wireless technology-based embedded systems, the environment in which electronic systems have to operate is becoming increasingly hostile. As consequence of technology scaling, Integrated Circuits' (ICs) supply voltage is continuously decreasing, reaching less than 1 V for the IC core and less than 2 V for the periphery and the I/O pads. This scenario reduces noise margins and increases circuit susceptibility to Electromagnetic (EM) noise [5, 13], which exposes the circuit to transient faults and consequently reduces the system reliability [2, 11].

Furthermore, for critical applications—such as military, aerospace or biomedical—reliability assurance to Total Ionizing Dose (TID) radiation is always a key-issue for the success of products on the market. Trapping of positive charges in oxide regions causes TID effects on CMOS integrated circuits, for deep-submicron circuits, the main TID effects are the increase of leakage currents and the change in current–voltage characteristics of the devices. Both effects are due to charges getting trapped in shallow trench insulators [4, 6]. The variation of devices' electrical characteristics leads to variations of parameters of the circuits, namely, leakage current increase, noise margin degradation and propagation delay increase. For very high doses, a permanent functional failure of the circuit can be observed [4].

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In the past works presented in literature, these concerns have been considered and treated as independent events and consequently, engineers certificate electronic systems to Electromagnetic Interference (EMI) or TID radiation. In the best case, systems are tested regarding both, but never taking into account the combined consequences as one phenomenon may take effect on the other. For instance, assuming that a given part of an embedded system - hardware or software—for space application is certified by a set of EMI tests according to specific standards. After a given period of time operating in the field, it is impossible to ensure that this part will still perform properly according to the same set of EMI standards, considering that a certain level of TID has been cumulated over the system. The equivalent holds true for the reverse, it is at least doubtful that separated certification can ensure that the part will operate properly in a given radiation environment under exposure of high noise levels of EMI.

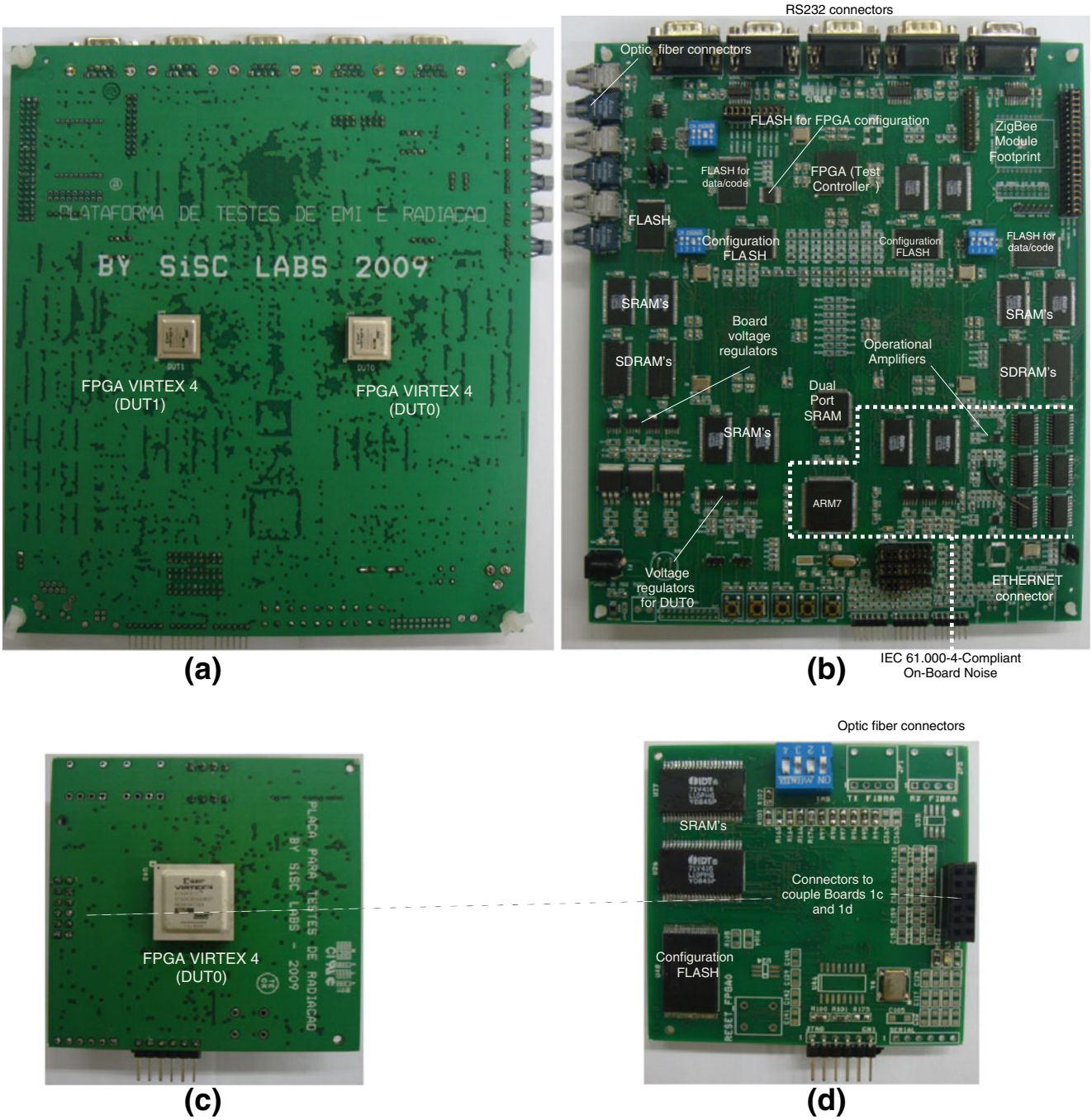


Fig. 1 Platform: 8-layer board for EM immunity tests: (**a**) Top; (**b**) Bottom; 6-layer board for TID tests: (**c**) Top; (**d**) Bottom

In this paper, we present a configurable platform suitable for combined tests of EMI and TID radiation measurements of embedded systems. At this point, the platform is used to characterize the combined effects, in order to identify the SoC's reliability level under such environmental conditions. The platform has been developed in order to attend the most representative international standards for measurements on ICs and embedded systems regarding EMI: IEC 62.132-2 (for radiated noise), IEC 61.0004-17 and IEC 61.0004-29 (for conducted noise) and regarding TID: 1019.8 method for TID Test Procedure of MIL-STD-883 H.

The remainder of this paper is organized as follows: *Section 2* describes the platform, including the hardware and the programming interface used to configure the boards and monitor the system under test. This section also describes the international standards for which the platform was designed in compliance with. *Section 3* describes the test environment and how the board is connected to the various devices. To illustrate the platform's utilization, *Section 4* presents the case study developed based on a Plasma microprocessor. With the obtained case results, *Section 5* performs the reliability analysis of the Plasma microprocessor operating in different environments with combined EMI and TID radiation. Finally, *Section 6* summarizes the conclusions of the work.

2 The Platform

The platform's hardware is based on two specific complementary boards. The first one is an 8-layer board devoted to EM immunity tests, depicted in Fig. 1a and b. More precisely, two types of EM immunity tests can be performed:

- *Radiated Noise Immunity Test (RNIT)*, which is carried out in a Gigahertz Transverse Electromagnetic Cell (GTEM Cell) according to the IEC 62.132-2 standard [8];
- *Conducted Noise Immunity Test (CNIT)*, following the IEC 61.000-4-17 standard for ripple on power supply lines [9] and IEC 61.000-4-29 standard for voltage dips, voltage variations and short interruptions on the DC port of electronic systems [7].

The second board is a 6-layer board, depicted in Fig. 1c and d, dedicated to the 1019.8 method for TID Test Procedure of MIL-STD-883 H. Note that Fig. 1 presents details of these two boards. In both boards, the most important component is the Xilinx Virtex 4 FPGA, part number XC4VFX12-10SF363, used to map the SoC under evaluation.

Thus, the platform is designed to evaluate different applications under one test condition related to two regarding EM immunity and TID radiation, respectively. In more detail, the three tests the platform considers are:

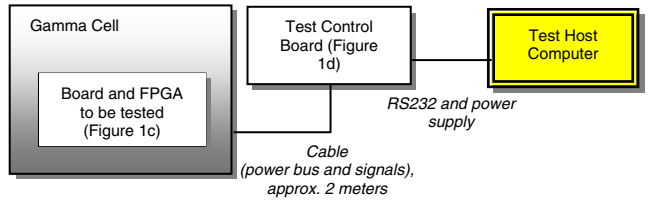


Fig. 2 Configuration for TID radiation test

2.1 Radiated Noise Immunity Test (RNIT)

The board's side shown in Fig. 1a is called the *test side*, while the other side is denominated the *glue-logic side*. During RNIT campaigns, the board is placed inside a metallic shielding box with an upward opening, where the *test side* is exposed to radiated noise, while the *glue-logic side* remains protected against the EMI by the shielding box. By adopting this configuration, it is possible to ensure that only the SoC prototyped into the two FPGAs on the *test side* will be radiated with EM noise, while the remaining logic required for test control will be protected inside the shielding box. The remaining logic is comprised of test vectors generator and compressor, clock generators, reference data for FPGA configuration, board voltage regulators, logic responsible for test monitoring and external environment communication-support ICs and connectors (optical fiber, serial RS232, Ethernet connectors), among other components.

2.2 Conducted Noise Immunity Test (CNIT)

The EM immunity test board can also perform CNIT for the SoC prototyped on the two FPGAs' *test sides*. For this purpose, an ARM7 processor, able to generate Power Supply Disturbances (PSDs) according to the two previously mentioned IEC standards for CNIT and capable of monitoring the system during the execution of both EM immunity evaluations, is integrated on the 8-layer board. Moreover,

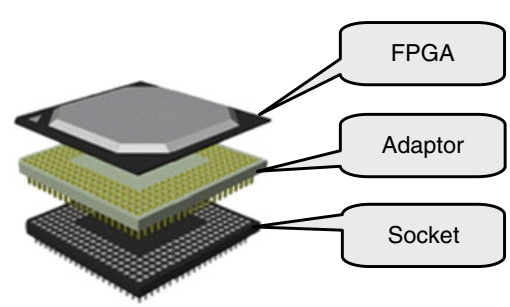


Fig. 3 Mounting the FPGA on boards for EM and TID immunity tests

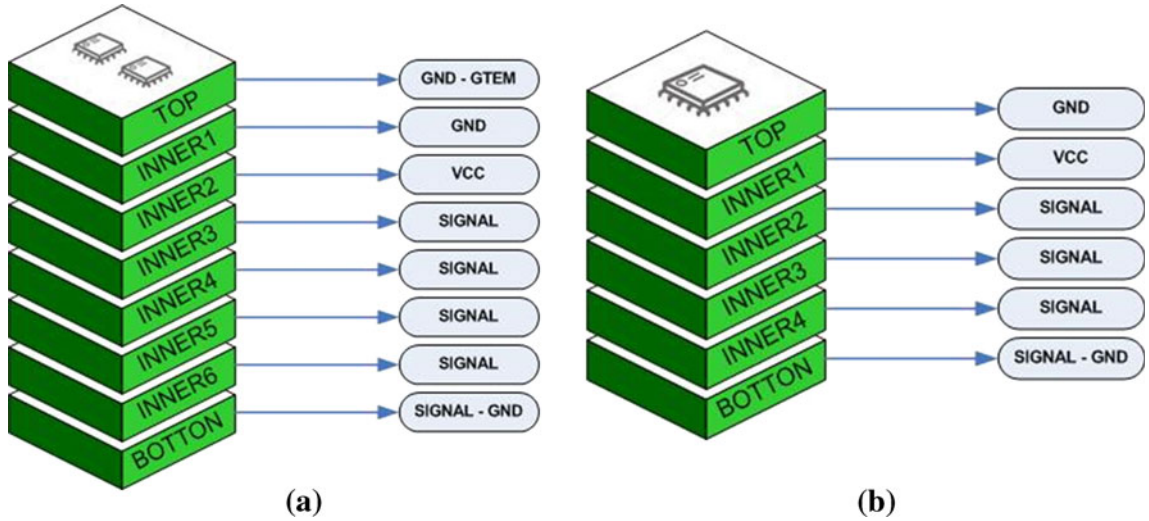


Fig. 4 Layer distribution for: (**a**) EM immunity board, and (**b**) TID immunity board

the noise generator has SRAM memories, six operational amplifiers and 6 12-bit Digital-to-Analog Converters (DACs), as shown in the board's bottom right side in Fig. 1b. Thus, the ARM7 processor executes a code that controls the V_{dd} voltage provided to FPGA0 and FPGA1. More precisely, the processor sends a 12-bit digital signal to the DACs, which are connected to the inputs of the operational amplifiers, while the operational amplifiers' outputs are connected to the V_{dd} input ports of FPGA0 and FPGA1. In this manner, it is possible to generate and individually inject any type of noise into the core, the periphery and the pad rings of FPGA0 and FPGA1.

It is worth noting that based on this infrastructure it is possible to perform not only individual immunity tests for radiated or conducted EMI, but also combine both experiments into a single test session. For many critical embedded systems, this combined-test scenario may represent the most realistic condition to "mimic" the harsh environments that they will operate in.

2.3 TID Radiation Test (TIDRIT)

The board for TIDRT depicted in Fig. 1c and d is in fact composed of two separate boards that are joined by connectors on their backsides. The board of Fig. 1c is the one that is placed inside the vacuum chamber of the Gamma cell described in the next section. The board seen in Fig. 1d contains the *glue logic* necessary to control the test, to monitor the FPGA during the session in real-time, in order to provide power-supply to the FPGA under test and to communicate with the remotely placed test host (PC) computer. Figure 2 summarizes such scenario.

It should be stated that the FPGAs seen in Fig. 1a and c are the same. The FPGA is mounted on these boards by means of a socket and an adaptor, as depicted in Fig. 3. The socket is soldered onto the board, whereas the adaptor is soldered onto the ball-grid array (BGA) of the FPGA. In order to perform TID testing, the FPGA is placed on board as shown in Fig. 1c. Once the test session is accomplished, the FPGA is removed from this board and placed on the board's socket as shown in Fig. 1a, in order to proceed with EM immunity tests. The radiated FPGA can be placed in any of the two sockets. During the EM immunity test sessions, the other socket is used to place a non-irradiated FPGA to be used as *Gold Reference*. In this manner, the combined test can be performed in both directions, from the TID radiation to the EM immunity test and vice-versa.

Table 1 Preferred range of test levels and durations for voltage dips on the V_{dd} input power port (IEC 61.000-4-29)

Test Type	Test Level (%)	Duration (s)
Voltage Dips	40, 70 or *X*	0.01
		0.03
		0.1
		0.3
		1
		X

Table 2 Preferred range of test levels and durations for ripple on the V_{dd} input power port (IEC 61.000-4-17)

Test Type	Level	Percentage of the nominal DC voltage
Ripple	1	2
	2	5
	3	10
	4	15
	Y	*Y*

To conclude the description of the platform's hardware, it is worth mentioning the distribution of signals and power over the boards' several layers. According to IEC recommendations for designing test boards, the layer functionality of these boards shown in Fig. 4 is adapted. High-sensitivity and high-frequency signals are carried on the inner layers, which are involved by power (*Gnd* and V_{dd}) planes preferring to place the *Gnd* plane exterior to the V_{dd} plane. It is important to highlight that V_{dd} and *Gnd* need to be parallel planes in order to construct a "natural" decoupling capacitor for the sensitive signals flowing in the board's inner layers. Finally, it is important that a *Gnd* plane is placed on the *test side* of the board. This plane is connected with the *Gnd* line of the GTEM cell in order to prevent floating nodes which cause unwanted currents flowing between the GTEM cell and the system under test. These currents may not only damage board electronics, but may cause altered experimental results.

The platform's software was developed for *Microsoft Windows* operating systems. Through this software, the user may configure the FPGAs, download software for the ARM7 processor, monitor the system during EM or TID immunity tests and configure noise to be injected into the FPGAs V_{dd} input ports.

Basically, any kind of noise waveform can be generated on-board and applied not only to the FPGAs, but also to the SRAMs, the SDRAMs, the Flash Memory or any combination of these ICs. The platform is configured to generate noise on V_{dd} according to the IEC. 61.000-4-17 standard (for ripple on V_{dd} power rail), the 61.000-4-29 standard (for voltage dips, voltage transients and short interruptions), as well as the 61.000-4-17 standard (for ripple on V_{dd} power rail). Table 1 shows the details regarding test levels and durations. The frequency at which noise can be injected into the FPGA's V_{dd} pins may range from 1 Hz to 120 KHz, with a duty cycle, which can vary from 10 % to 90 %. The noise

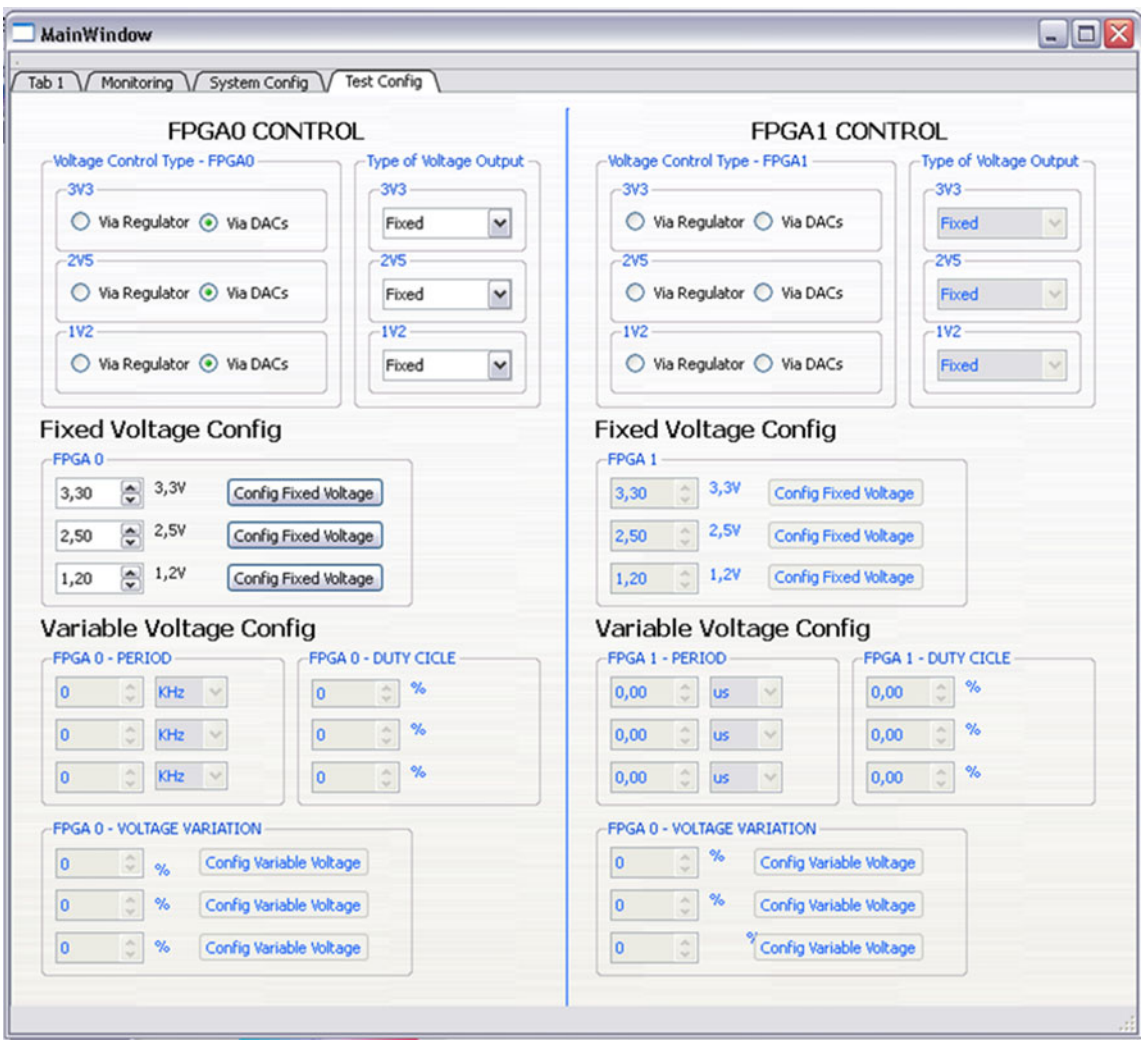


Fig. 5 Programming interface of the platform: screenshot of the configuration environment to perform tests according to the IEC standards 61.000-4-17 and 61.000-4-29

amplitude may vary from 0 % to 100 % using the nominal V_{dd} as reference.

Table 1 summarizes the preferred voltage test levels and durations for voltage dips stated in the IEC 61.000-4-29 standard. A X represents an open value and shall be selected by the product committee [7] to be as representative as possible for the circuit operating conditions. One or more of the test levels and durations specified in this table may be chosen to certificate the product. It is worth noting that for modern nanotechnologies, with a V_{dd} equal to or lower than 1 V, voltage dips of less than 10 % (i.e., X=10 %) should be assumed. In nano-circuits, on-chip IR-drop and ground bounce may create supply voltage fluctuations, which became one of the most important concerns of IC designers.

Table 2 shows the preferred voltage test levels and durations for ripple noise on the *DC input power port* for immunity tests according to the IEC 61.000-4-17 standard [9]. The Y parameter in this table assumes the same function as X in Table 1, an open value and shall be selected by the product committee [7] to be as representative as possible for the circuit operating conditions.

There is also an on-board temperature sensor that can be read by the ARM7 processor in real-time. Figure 5 presents the platform's configuration screen used to define the noise waveform parameters before the injection into the V_{dd} pin of FPGA 0 and FPGA 1.

Fig. 7 Radiation source used for gamma irradiations at the *Centro Atómico Ezeiza*, from the *Comisión Nacional de Energía Atómica, Argentina*

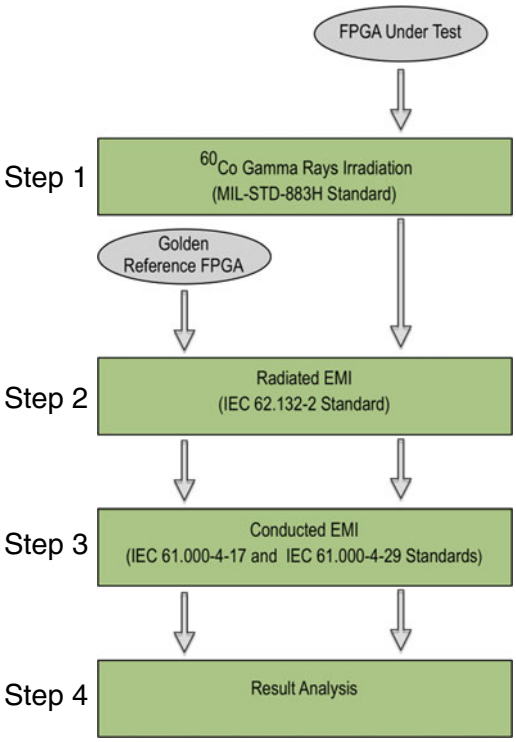


Fig. 6 Flow diagram of the experiments performed in order to evaluate the combined effects of EMI and TID radiation

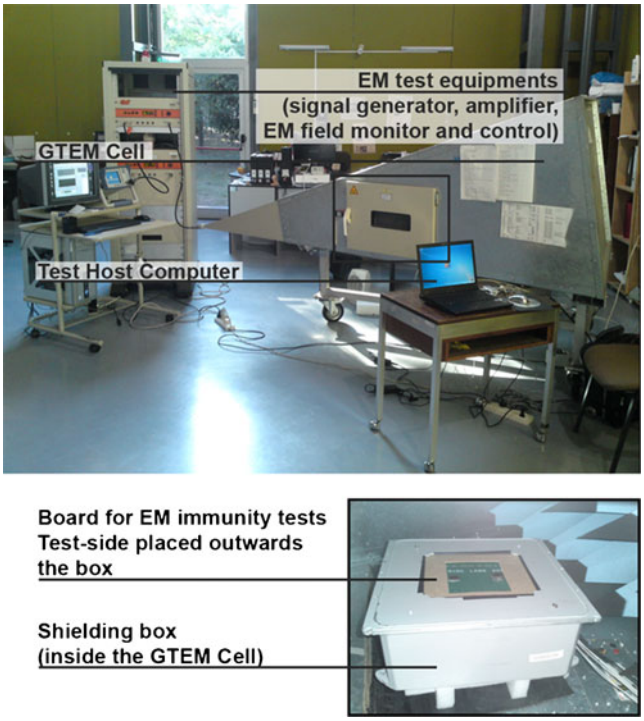


Fig. 8 Environment for radiated EM immunity measurements at the *Instituto Nacional de Tecnología Industrial (INTI)*

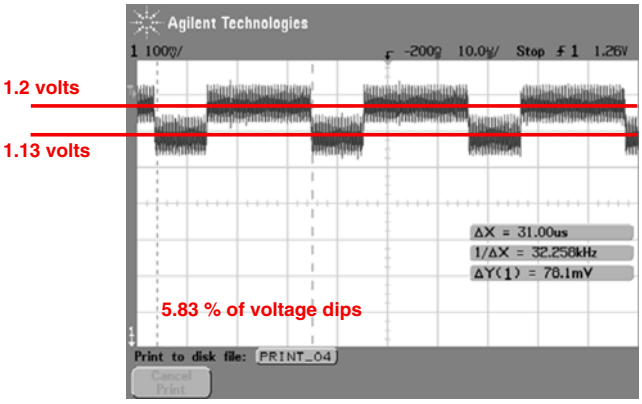


Fig. 9 Oscilloscope print screen for the conducted EMI injected at the FPGAs input power pins according to IEC 61.000-4-29 standard

3 Test Environment, Procedures and Standards

In the following, the environment and procedures according to the above-mentioned standards for EM immunity and TID tests are described in more detail. Thus, in order to evaluate the combined effects of EMI and TID radiation on embedded systems, a set of experiments has been performed according to the flow diagram presented in Fig. 6.

In the here reported experiments, four Virtex-4 (XC4VFX12-10SF363) FPGAs from the same lot have been irradiated using 60Co gamma rays source in different doses in *Step 1*. The gamma ray irradiations have been performed following the standardized 1019.8 method for TIDRT of the MIL-STD-883 H standard. The radiation source used during these experiments is the Gamma Cell shown in Fig. 7. Basically, the Gamma Cell allows a uniform irradiation of the samples when they are physically placed on known isodose surfaces. The irradiations have been performed at room temperature and with a dose rate of 0.75rads(Si)/s. Silver-chromate dosimeters have been employed to measure the TID [10]. To evaluate how different levels of TID affect the FPGA's EM immunity, several FPGAs can be irradiated to a wide span of doses. Several works reported that FPGAs fabricated in deep-submicron CMOS processes are able to withstand TID levels of a few hundreds of krads [3, 4, 12, 14]. Before gamma irradiation, electrical performance tests have to be made on each FPGA to guarantee their functionality in their original state. During gamma irradiation, the FPGAs are mounted on the board described in Section 2 and shown in Fig. 1c and d, while functioning as close as possible to real operating conditions. Figure 6 summarizes the steps to be taken.

In *Step 2*, the FPGAs exposed to different doses of TID radiation are submitted to Radiated EMI. These FPGAs are mounted on the 8-layer board, which is placed inside the shielding box which itself is inserted into the Gigahertz Transversal Electromagnetic Mode (GTEM) Cell, shown in Fig. 8. Specifically, the RNITs have been performed in the GTEM cell of the *Instituto Nacional de Tecnología Industrial (INTI)*, in Buenos Aires, Argentina. Test conditions according to the IEC 62.132-2 standard have been adopted. In more detail, the conditions can be stated as follows:

- *EM field range:* from 10 to 220 V/m;
- *Radiated signal frequency range:* [150KHz–3 GHz] (extended IEC 62.132-2);
- Signal modulation format: AM/FM 80 %.

In *Step 3* of the flow diagram presented in Fig. 6, CNITs have been performed in order to understand how TID radiation can affect the susceptibility of the FPGA when voltage dips according to IEC 61.000-4-29 are injected to the supply line of the FPGA under test. Figure 9 shows the waveform of the applied voltage dips with further detail. In order to measure the FPGAs' degree of susceptibility, we step-by-step decreased the nominal V_{dd} from 1.2 V until observing an erroneous output.

Finally, in the flow diagram's *Step 4* the obtained results are analyzed. It is important to highlight that, depending on the experiments purpose, radiated and conducted EMI experiments are performed immediately using the FPGAs already exposed to gamma rays irradiation. Alternatively, test engineers may prefer to apply worst-case bias conditions to the FPGAs during a given period of time for post irradiation anneals [16] before performing EM immunity measurements. In the latter case, it is worth remarking that special care has to be taken to ensure that all the samples will hold equal anneal times between the end of the TID irradiation and the beginning of the EM immunity tests. This will ensure that the different EM test results observed in the different FPGAs are due to TID level variations and not to different anneal times.

Table 3 TID deposited on the four FPGAs

FPGA0 (krads)	FPGA1 (krads)*	FPGA2 (krads)*	FPGA3 (krads)*	FPGA4 (krads)*
0	5.6	51.9	111.0	216.0

*dose rate: 0.75 rads/s

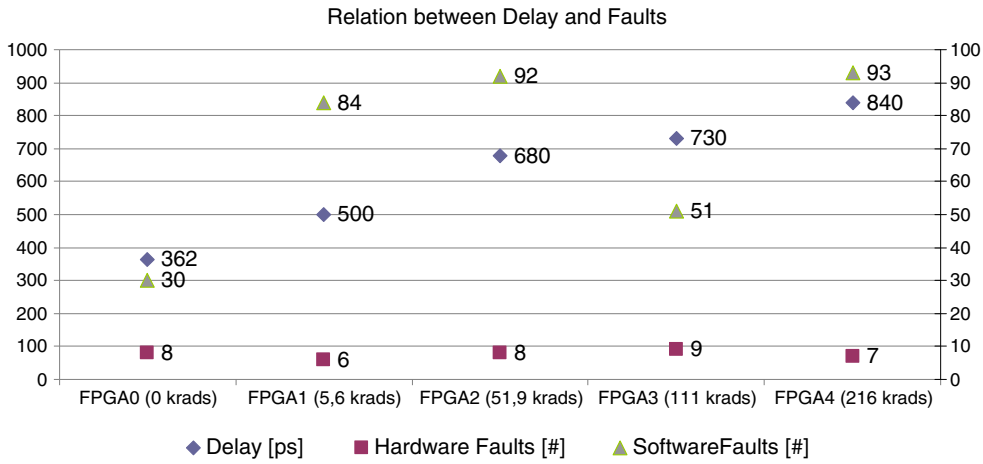


Fig. 10 Experimental results showing the relationship between TID, delay and number of fault occurrences in the FPGAs

4 Case-Study

In order to evaluate the platform, we adopted a case study based on a Plasma Microprocessor. Two independent experiments were carried out. The first one runs a Matrix Multiplication (MM) directly on the microprocessor, while the second runs a Test Program (TP) composed of various tasks that exploit different resources of the adopted Real-Time Operating System (RTOS). The experiments are described in more detail below.

4.1 Experiment 1: 10×10 Matrix Multiplication

A SoC based on the Plasma microprocessor[1] running a 10×10 MM code was implemented. In addition to the processor, we designed a chain containing 10,000 inverters. Four Virtex FPGAs, similar to the one depicted in Fig. 1c, were configured for both circuits and submitted to different doses of TID radiation as depicted in Table 3. It is important to highlight, that FPGA0 is the reference device that was not irradiated and therefore serves as the *Golden Reference*. For this experiment, the MM code was fully stored in the FPGA's internal block RAMs. Additionally, the inverter's chain input and output have been directly connected to the FPGA I/O pins to allow precise *delay* versus *TID* measurements on the FPGA.

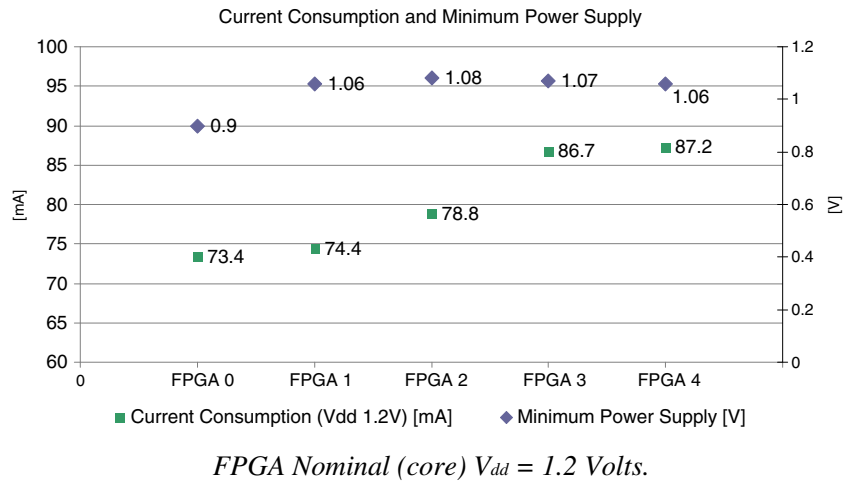
The radiation source used was the gamma cell depicted in Fig. 7. The experiment followed the standardized 1019.8 method and has been applied at room temperature with a dose rate of 0.75 rads/s. To achieve different radiation doses the FPGAs under test remained under radiation for different time periods. In more detail, FPGA1 remained for a few hours, while FPGA4 was radiated for 5 days. Silver-chromate dosimeters were used to measure the TID. Two hours after stopping the radiation process, the following measurements were performed for each FPGA:

1. The delay of the inverter's chain;
2. The static current consumption of the FPGA;
3. The minimum core V_{dd} required by the FPGAs to properly run the Plasma microprocessor. Figures 10 and 11 summarize the results of these measurements;
4. The number of faults occurring in the Plasma processor when running the MM code under radiated EMI. This measurement was carried out with the board seen in Fig. 1a and b attached to the shielding box, inside the GTEM cell, as depicted in Fig. 8. Each of the five FPGAs was exposed to radiated EMI during a period of 8 h. These measurements were carried out in compliance with the IEC international 62.132-2 standard (extended) according to the following parameters mentioned in Section 3.

We classified the faults observed in the Plasma processor when running the MM code under EMI into: *Hardware Faults* and *Software Faults*. While the former type makes reference to those faults affecting the logic used to configure the FPGA, the latter one reflects the number of faults corrupting the MM code execution. Faults affecting the FPGA configuration logic were detected by performing the *readback* operation of the component.

In Figure 10, it is possible to observe that the delay is monotonically increasing for increasing TID radiation. FPGA4 shows a 232 % higher delay than the not-irradiated FPGA0. Regarding the fault occurrence during the test session in the GTEM cell, FPGA0 was affected

[1] The Plasma microprocessor is a Von Neumann 32-bit RISC architecture that can be downloaded from the public domain www.opencores.org. The Plasma is implemented in VHDL and has, with exception of the load/store instruction, an instruction set compatible to the MIPS architecture.



FPGA Nominal (core) V_{dd} = 1.2 Volts.

Fig. 11 Experimental results showing the current consumption and the minimum core V_{dd} supported by the FPGAs

by 38 faults: 30 software faults affecting user data registers and 8 hardware faults affecting the FPGA0 configuration registers. The four irradiated FPGAs demonstrated an average of about 88 fault occurrences. This is an increase of 230 % with respect to the *Golden Reference*. It is important to highlight that the delay increases only the occurrence of software faults. The number of faults affecting the FPGA's hardware parts remains approximately constant. About 8 faults per FPGA can be independently observed for each TID level deposited on the components.

Figure 11 shows the static current consumption of the four irradiated FPGAs as well as the value for the gold reference. This figure summarizes the minimum V_{dd} required by the FPGAs to properly execute the Plasma processor and its MM code during the EM immunity tests in the GTEM cell. The results illustrated in this figure demonstrate two aspects that below are described in more detail.

1. FPGA core's static current consumption increases as a function of the accumulated dose of radiation. More precisely, from 73.4 mA for FPGA0 to 87.2 mA for FPGA4.
2. The FPGA becomes more sensitive to V_{dd} reduction: with a minimum value ranging between 0.9 V for FPGA0 and 1.06 V for FPGA4. Note also that the minimum V_{dd} tolerated for the four irradiated FPGAs settles in between 1.06 and 1.09 V (with an arithmetic average of 1.068 V). This means that the minimum V_{dd} necessary for the irradiated FPGAs to properly run the Plasma processor with its application is roughly similar, independent of the accumulated dose. Therefore, to ensure correct Plasma operation in the irradiated FPGAs under EMI exposure, the V_{dd} provided to these components should be at least 18.67 % higher than the minimum V_{dd} measured for the *Golden Reference*.

4.2 Experiment 2: RTOS Executing Different Tasks

For the second experiment, the TP whose block diagram is shown in Fig. 12, was developed. The TP was executed under the control of the Plasma's RTOS.[2] During the execution of the TP, 8 tasks access and update the value of a global variable, which is protected by a semaphore. Additionally, another global variable is accessed by an interrupt. The 8 tasks were appointed to the following different priorities: 1, 2, 3, 4, 1, 2, 3 and 4, respectively. The interrupt has been assigned the maximum priority. For this experiment, after TID deposition, each of the FPGAs was exposed to conducted EMI during a period of 8 h, after having suffered TID deposition already. Table 4 summarizes the observed RTOS fault indications during BM1 execution.

The experiment features fault injection campaigns that were generated according to the IEC 61.000-4-29 international standard by applying voltage dips to the core V_{dd} pins of the four irradiated FPGAs as well as the *Golden Reference*. The nominal core V_{dd} is 1.2 V. During the experiment, the IC peripheries remained at normal voltage levels, i.e., 3.3 V or 2.5 V. During the test session, voltage dips were randomly injected into the FPGA's V_{dd} pins at a frequency of 25.68 kHz and consisted of dips of 5.83 % of the nominal V_{dd}. For larger voltage dips, the loss of the hardware configuration for FPGA3 (111 krads) was observed. It is worth noting that FPGA4 (216 krads) permanently failed to run the TP and the Plasma's RTOS even at nominal V_{dd}, i.e., the

[2] The Plasma's RTOS adopts the preemptive scheduling algorithm with priority support and provides a basic mechanism able to detect faults that cause misbehavior of the RTOS's essential services, such as stack overflow and timing violations. This mechanism is implemented by a function named *assert()*, which is called every time a RTOS service is run. When the argument of the *assert()* function is false, the RTOS sends an error message through the standard output. Therefore, more RTOS services are solicited by a given application program, higher is RTOS capability to detect faults.

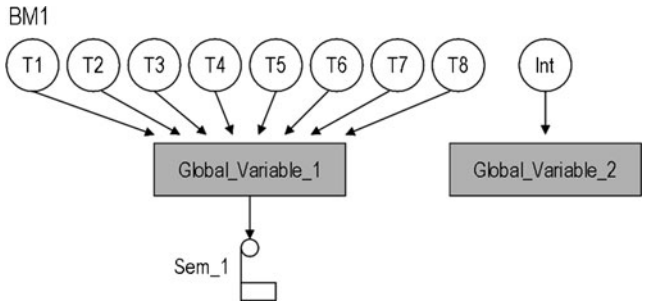


Fig. 12 Block diagram of the Test Program (TP) executed by the Plasma processor under the RTOS control. The whole system was run inside the irradiated FPGAs during conducted EMI tests

Plasma processor was downloaded to FPGA4, but the RTOS was not able to start. It is our understanding, that the use of the RTOS forced parts of the processor to be activated. These parts had not been used during Experiment 1, since the processor was running MM code without RTOS. With the activation of these parts by the RTOS execution, different critical paths were excited, whose timing response was violated due to the accumulated radiation.

5 Reliability Analysis

The experimental values obtained in the previous section will be used hereafter to estimate the reliability of the Plasma processor operating in EM environment after different accumulated radiation doses. With this purpose, we consider the following statements, which are also similarly assumed in [1]:

1. The probability of a number of faults occurring in a fixed period of time with a known average rate is independent of the time since the last event. (Poisson distribution).
2. System errors are statistically independent.

Therefore, the reliability of a system can be given by:

$$R(t) = e^{-\lambda t} \tag{1}$$

where λ is the failure rate and t represents the time parameter. Based on the experimental results depicted in the previous section, λ can be computed for the five FPGAs as shown in Tables 5 and 6. For instance, FPGA1's user logic has an estimated failure rate of 0.75 errors per hour when the component is running the Plasma processor with the MM code in an irradiated EMI environment, as defined by the IEC 62.132-2 international standard. This, for example could refer to an EM field hanging between 10 and 220 V/m, a radiated signal frequency range between 150 kHz and 3 GHz as well as a signal modulation format at AM/FM 80 %.

Table 4 Number of faults observed during TP execution

FPGA0	FPGA1	FPGA2	FPGA3	FPGA4
0	356	692	708	*

* The Plasma processor has been downloaded to FPGA4, but the RTOS did not start.

Based on Eq. (1), the mean time to failure (MTTF) of the Plasma processor operating in EM-noise environment after cumulating TID can be calculated for two situations: when the processor is directly running the application (Experiment 1, for irradiated EMI) and when the processor is running the application under the control of the RTOS (Experiment 2, for conducted EMI). Thus, the integration of the reliability function results in the MTTF equations:

$$MTTF = \int_0^{\infty} R(t)\, dt \tag{2}$$

$$MTTF = \left[\frac{-e^{-\lambda t}}{\lambda}\right]_0^t \tag{3}$$

>Figure 13 shows the reliability of the system described in the Experiment 1 as a function of TID and EMI. The system reliability was computed considering the combined fault occurrence of *configuration* and *user logic*. Figure 14 depicts the RTOS's reliability as a function of the TID and EMI during Experiment 2. Tables 7 and 8 present the MTTF, given in hours for the Plasma-based system, both experiments are presented. The values in Figs. 13 and 14 were obtained from computing Eq. (1) as a function of the time t and the failure rates λ as depicted in Tables 5 and 6, respectively. In the following, Tables 7 and 8 were built up by computing Eq. (3) as a function of the time t, as well as the failure rates λ as depicted in Tables 5 and 6.

By analyzing Figs. 13 and 14 as well as Tables 7 and 8, one can draw the following conclusions:

a) As observed in Fig. 13, FPGA3 is slightly more robust to EMI than FPGAs 1 and 2, even though it received a higher TID than FPGAs 1 and 2. Nevertheless, it should be noted that the same test procedure was used to verify the functional behavior of these components when operating in EMI environment. The only difference among the FPGAs is the manufacturing lot: FPGA3 is from a different lot than FPGAs 0, 1, 2 and 4. Thus, it is our understanding that process variations may have a considerable impact on the tolerance level of an IC to TID radiation.[3]

[3] It should be noted that as postulated in the literature [15], the accumulated radiation (TID) on ICs has as consequence the reduction of the MOS transistor threshold voltage (V_{th}). This phenomenon gradually reduces the (I_{DS}) current drive capability of pMOS transistors and increases the one for nMOS devices. From this, the IC is more prone to suffer from timing (delay) faults.

Table 5 λ computation for the five FPGAs during Experiment 1, for irradiated EMI

Failure Rate (errors per hour)	FPGA0	FPGA1	FPGA2	FPGA3	FPGA4
λ for user logic faults	3.75	10.50	11.5	6.38	11,63
λ or configuration logic faults	1.00	0.75	1.00	1,13	1.00
λ for combined (configuration+user) faults	4.75	11.30	12.50	7.50	12.65

b) The radiation effect on the FPGA reliability degradation is remarkable for the first tenths of deposited krads. This reasoning can be easily observed in Fig. 13 for FPGA0 (*Golden Reference*) against FPGA 1 (5.6 krads), FPGA2 (51.9 krads) and FPGA4 (216. krads), and in Fig. 14 for FPGA0 (*Golden Reference*) against FPGA2 and FPGA3 (111 krads).
c) When the FPGA operates in conducted EMI environment, the MTTF for the *user logic* degrades 2.5 times for a radiated component (MTTF arithmetic mean for FPGAs 1, 2, 3 and 4) in comparison to a radiation-free component (FPGA0), whereas the MTTF of the *configuration logics* remains quite constant independently from radiation that is deposited on the IC (Table 7).
d) When the FPGA operates in conducted EMI environment, the average MTTF for radiated FPGAs (1, 2, 3, and 4) degrades 2.2 times with respect to the one for a non-radiated component (FPGA0), as seen in the last line of Table 7. When the FPGA operates in radiated EMI environment, the mean MTTF for radiated FPGAs (1, 2 and 3) degrades from a theoretical "α" to a mean value of 0.015 (i.e., one fault at every 54 s, in average), as shown in Table 8.

6 Conclusion

A configurable platform for combined tests of EM immunity and TID radiation of prototype embedded systems has been presented. The platform attends the following international standards: IEC 62.132-2 (for radiated EMI), IEC 61.0004-17 and IEC 61.0004-29 (for conducted EMI) and 1019.8 method for TID Test Procedure of MIL-STD-883 H.

The hardware part of the platform is composed of two boards: the first one has been designed for radiated and conducted EM noise measurements, while the second board has been designed for performing TID procedure. The software part is based on an interface used by the designer to configure both boards by one side, and to monitor the system under test online, by the other side. The software part is also responsible for formatting measurement results and generating summary fault dependability reports.

To illustrate the platform's operation, a case study based on the Plasma soft-core processor running with and without the Plasma RTOS has been presented. After depositing different radiation doses on the FPGAs, the system has been exposed to radiated and conducted EMI. The failure rate has been extracted from the practical experiments.

The performed combined tests demonstrate that TID radiation increases the delay, which may lead to functional faults due to the fact that the FPGA running the application does not meet the expected timing constraints. Furthermore, the experiments demonstrate that the power consumption increases with the radiation dose applied to the FPGA.

The results indicate that the stand-alone evaluation of EM immunity is not able to guarantee a reliable execution of the FPGA's functionality if the component is supposed to operate in harsh environment exposed to TID. It is important to highlight that the reliability of safety-critical applications has to be guaranteed in an environment that closely imitates the reality. Therefore, evaluating the combined effects of TID radiation and EMI is the only solution to properly foresee the reliability of an FPGA.

In more detail, the presented experiments are able to evaluate such combined effects. They show that the fault occurrence for FPGAs subject to TID radiation and EMI are significantly higher than for FPGAs that suffered from EMI exposition only. Furthermore, the combined effects of TID and EMI increased FPGA susceptibility to power supply voltage transients. Compared to the *Golden Reference*, a non-irradiated FPGA, TID-exposed FPGAs needed a substantially higher minimum supply voltage to function properly when operating in EMI environment.

Consequently, the stand-alone evaluation of EM immunity is not able to represent real environments where this type of components has to operate. Only a combined test can guarantee realistic predictions for the embedded system's reliability.

Table 6 λ computation for the five FPGAs during Experiment 2, for conducted EMI

Failure Rate (errors per hour)	FPGA0 (Gold Ref)	FPGA1 (5.6 krads)	FPGA2 (51.9 krads)	FPGA3 (111 krads)	FPGA4 (216 krads)
λ	0	44.5	86.5	88.5	—

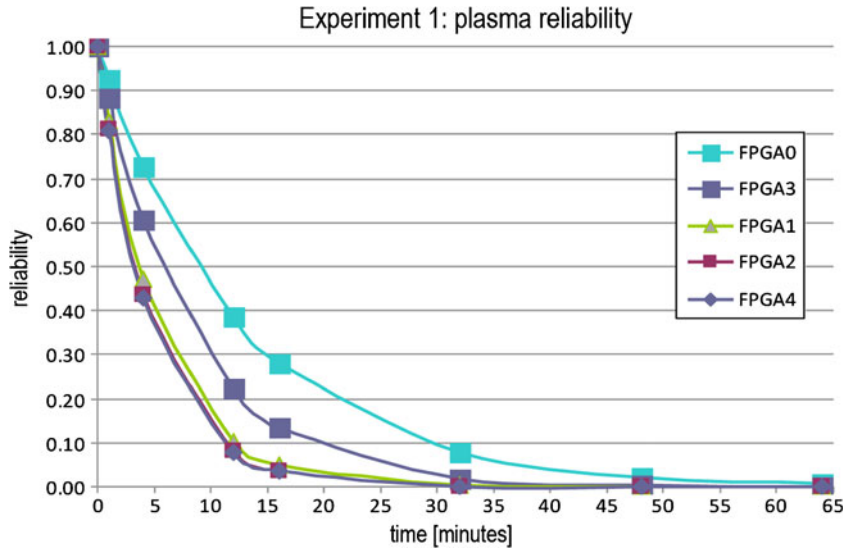


Fig. 13 Plasma reliability for Experiment 1

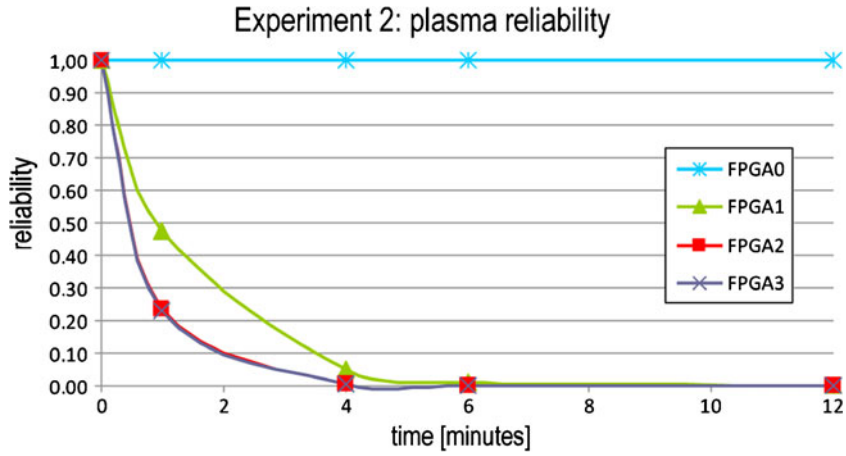


Fig. 14 Plasma reliability for Experiment 2

Table 7 MTTF for the Plasma processor (Experiment 1)

	FPGA0 (Gold Ref)	FPGA1 (5.6 krads)	FPGA2 (51.9 krads)	FPGA3 (111 krads)	FPGA4 (216 krads)
MTTF for user logic	0.267	0.095	0.087	0.157	0.086
MTTF for configuration logic	1.000	1.333	1.000	0.885	1.000
MTTF for combined (configuration+ user) faults	0.211	0.088*	0.080*	0.133*	0.079*

*average value: 0.095

Table 8 MTTF for the Plasma processor (Experiment 2)

	FPGA0 (Gold Ref)	FPGA1 (5.6 krads)	FPGA2 (51.9 krads)	FPGA3 (111 krads)	FPGA4 (216 krads)
MTTF	α	0.022*	0.012*	0.011*	—

*average value: 0.015

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References

1. Argyrides C, Chipana RD, Vargas F, Pradhan DK (2011) "Reliability Analysis of H-Tree RAM Memories Implemented with BICS and Parity Codes for Multiple-Bit Upset Correction", *IEEE Transactions on Reliability*, Issue 99
2. Ben Dia S, Ramdani R, Sicard E (2006) Electromagnetic compatibility of integrated circuits – Techniques for low emission and susceptibility, Springer
3. Cochran DJ, Buchner SP, Sanders AB, LaBel KA, Carts MA, Poivey CF, Oldham TR, Ladbury RL, O'Bryan MV, Mackey SR (2008) Compendium of Recent Total Ionizing Dose Results for Candidate Spacecraft Electronics for NASA. *2008 IEEE Radiation Effects Data Workshop,* 5–10
4. Dodd PE, Shanneyfelt MR, Schwank JR, Felix JA (2010) Current and future challenges in radiation effects on cmos electronics. IEEE Trans on Nuclear Science 57(4):1747–1763
5. Freijedo J, Costas L, Semião J, Rodríguez-Andina JJ, Moure MJ, Vargas F, Teixeira IC, Teixeira JP (2010) Impact of power supply voltage variations on FPGA-based digital systems performance. Journal of Low Power Electronics 6:339–349
6. Hughes HL, Benedetto JM (2002) Radiation effects and hardening of MOS technology: Devices and circuits. IEEE Trans Nuclear Science 50(3):500–521
7. IEC 61.000-4-29: Electromagnetic compatibility (EMC) – Part 4–29: Testing and measurement techniques – Voltage dips, short interruptions and voltage variations on d.c. input power port immunity tests, First Edition, 2000–01. (www.iec.ch)
8. IEC 62132–2, Ed. 1: Integrated Circuits – Measurement of Electromagnetic Immunity, 150KHz to 1 GHz – Part 2: Measurement of Radiated Immunity - TEM Cell Method. This part of IEC 62132 is to be read in conjunction with IEC 62132–1. (www.iec.ch)
9. IEC Stds. 61.000-4-17: Electromagnetic compatibility (EMC) – Part 4–17: Testing and measurement techniques – Ripple on d.c. input power port immunity test, Edition 1.2, 2009–01. (www.iec.ch)
10. ISO/ASTM51401 - Standard Practice for Use of a Dichromate Dosimetry System. ASTM International, West Conshohocken, PA, 2003
11. Perez R (1997) Signal integrity issues in ASIC and FPGA design, *International Symposium on Electromagnetic Compatibility – EMC'97* 334–339
12. Quinn H, Graham P, Krone J, Caffrey M, Rezgui S (2005) Radiation-induced multi-bit upsets in SRAM-based FPGAs. IEEE Trans on Nuclear Science 52(6):2455–2461
13. Semião J, Freijedo J, Moraes M, Mallmann M, Antunes C, Benfica J, Vargas F, Santos M, Teixeira IC, Rodríguez-Andina JJ, Teixeira JP, Lupi D, Gatti E, Garcia L, Hernandez F (2009) Measuring clock-signal modulation efficiency for systems-on-chip in electromagnetic interference environment, *10th IEEE Latin American Test Workshop (LATW'09)*
14. Smith F, Mostert S (2007) Total ionizing dose mitigation by means of reconfigurable FPGA computing. IEEE Trans on Nuclear Science 54(4):1343–1349
15. Srour JR, McGarrity JM (1988) Radiation Effects on Microelectronics in Space. *Proceedings of IEEE* 76(11)
16. US Department of Defense - Test Method Standard Microcircuits MIL-STD-883 H. February 2010

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