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RESEARCH ARTICLE

A Fault-Tolerant Cascaded Switched-Capacitor Multilevel Inverter for Domestic Applications in Smart Grids

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ABSTRACT Cascaded multilevel inverters (MLIs) generate an output voltage using series-connected power modules that employ standard configurations of low-voltage components. Each module may employ one or more switched capacitors to double or quadruple its input voltage. The higher number of switched capacitors and semiconductor switches in MLIs compared to conventional two-level inverters has led to concerns about overall system reliability. A fault-tolerant design can mitigate this reliability issue. If one part of the system fails, the MLI can continue its planned operation at a reduced level rather than the entire system failing, which makes the fault tolerance of the MLI particularly important. In this paper, a novel fault location technique is presented that leads to a significant reduction in fault location detection time based on the reliability priority of the components of the proposed fault-tolerant switched capacitor cascaded MLI (CSCMLI). The main contribution of this paper is to reduce the number of MLI switches under fault conditions while operating at lower levels. The fault-tolerant inverter requires fewer switches at higher reliability, and the comparison with similar MLIs shows a faster dynamic response of fault detection and reduced fault location detection time. The experimental results confirm the effectiveness of the presented methods applied in the CSCMLI. Also, all experimental data including processor code, schematic, PCB, and video of CSCMLI operation are attached.

INDEX TERMS Cascaded, fault, fault-tolerant, multilevel inverter, reliability, smart grid, switched-capacitor.

NOMENCLATURE

S11,S12,S21,S22,S23	Identification of modules switches, *S*nm is the switch of number n from module m, n=Switch number, m= module number.
T1, T2, T3, T4	Identification for inverter H-bridge switches, H-bridge switch number of n.
C11,C21	Switched capacitor identification, *C*nm is switched-capacitor of number n from module m, n=Switched-capacitor number, m=module number.
λ_P	Failure rate (Failures/(10^6(h))).
T_J	Junction Temperature (°C).

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t_0-t_{13}	Time for each pulse of the steps (s).
V_{ab}	Voltage across the H-bridge circuit (V).
$MTTF$	Mean Time to Failure (h).
λ_b	Base Failure Rate (Failures/(10^6(h))).
π_T	Temperature Factor.
π_A	Application Factor.
π_Q	Quality Factor.
π_E	Environment Factor.
π_S	Electrical Stress Factor.
π_C	Contact Construction Factor.
π_{CV}	Capacitate Factor.
V_S	Voltage Stress Ratio (V).
S	Ratio of Operating to Rated Voltage.
N_{level}	Level numbers of the inverters.
ΔV	Voltage difference between the reference voltage and actual voltage (V).

I. INTRODUCTION

Multilevel inverters are becoming very popular due to their high power and voltage capacities and their ability to be used in renewable energy applications [1], [2] and smart grids [3]. By using a large number of cells or modules combined with switched DC capacitors in the structure of multilevel inverters, the demanded pulses can be generated without using multiple transformers. As the number of modules or cells in the structure of multilevel inverters increases, the probability of faults also increases [4]. As a result, reliability and safety have become the major challenges of MLI inverters [5]. A fault in any of these modules or cells can distort the output voltage and current of the multilevel [5]. Therefore, fault detection and identification of the faulty unit becomes essential. Rapid fault detection and identification of the failed parts can prevent further damage. Failures in MLIs are usually due to semiconductor switch failures, which depend on the operating parameters of the converter, including voltage and current, as well as environmental conditions [6].

Several strategies for fault detection and fault localization have been proposed in recent years. In some of these strategies, such as the extended state observer and adaptive observer [3], [7], [8], the longest time to locate the faulty switch is about 150 ms, which increases the time of the fault detection process for a large number of modules. The Kalman filter is another fault detection strategy that can identify the fault location within 100 ms [9], where fault detection is based on the estimated current compared to the actual current. The fault location is determined based on the voltage difference between the healthy and faulty modules. However, the difference between the capacitor voltage of the healthy and faulty modules may be too small to detect the fault location. Convolutional neural networks can also be used to detect and locate faults in the modules. These methods require many calculations, which increase the amount of computation and analysis of the parameters, thus increasing the complexity of the system. The work [10] has increased the cost and complexity of the multilevel inverter by using additional hardware with 7 sampling channels. The research [11] suggests using an adaptive linear neuron algorithm and recursive least squares algorithm to detect and locate the fault. However, this method requires many calculations and a large number of estimation units for the voltage of the capacitors. In [5], a 7-level fault tolerant multilevel inverter is presented where the faulty switch is detected using the suggested dedicated method, and the redundant switch is replaced by the faulty switch. The work [5] is simulated using MATLAB, and the results show that by replacing the redundant IGBTs, the total harmonic distortion (THD) is reduced to 18%. In [12], an Entropy of Wavelet Packets (EWP) - Support Vector Machine (SVM) based method is presented which is able to find the open circuit fault of IGBTs in less than 0.33 ms with 99.7% accuracy.

The main challenges of fault detection and localization are as follows:

1) low speed of fault detection and localization [11],
2) the number of calculations is high and the number of sampling sensors is large [10],
3) no verification and analysis of the short-circuit fault, while the semiconductors are shorted after the failure of the connection and most of the faults are of the short-circuit type, and the probability of short-circuit happening is much higher for semiconductors conditions [6], and
4) some sensors are invasive and affect the performance of the circuits [9].

One of the gaps in fault detection is the shortage of research on the use of electronic component reliability, which is applied in this article. The main objective of this paper is to present a fault detection and fault localization approach for a multilevel inverter that can be extended to other similar inverters.

Evaluating the reliability of the components can help to find the location of the fault more quickly. In other words, the shorter the lifetime of a component, the more probable it is that it will fail. It is possible to set a priority for fault location detection and increase its speed by evaluating the reliability of each component.

The key contributions are as follows:

i. The occurrence of a short circuit fault in some switches leads to the formation of a short circuit in the presence of the input power supply. With the presented fault detection method, the healthy switch of the path is turned off in less than 60 microseconds, which prevents further faults and damages from occurring to the circuit.
ii. The reduction of the fault detection time is achieved by prioritizing the reliability of the different components.
iii. For fault detection and localization, only one voltage sensor is used.
iv. The voltage sensor used is an isolated sensor, which is a non-invasive circuit.
v. The worst and most common type of failure in semiconductor components is the short-circuit failure [10],

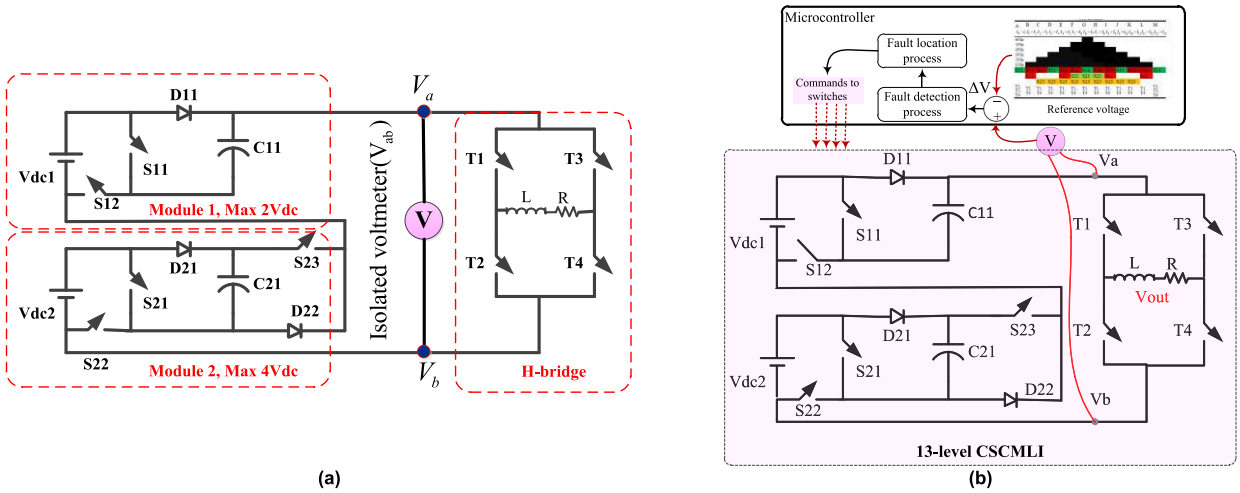

FIGURE 1. a) Structure of the proposed 13-level CSCMLI [13] and b) the function diagram of the fault detection and fault location method.

which causes serious damage to the system, therefore this research focuses on the short-circuit failure of the components.

This paper is a continuation of our previous work [13], which includes more details on the operation of the proposed multilevel inverter (MLI). This 13-level CSCMLI inverter is shown in Figure 1(a). This switched capacitor cascaded MLI (CSCMLI) consists of two modules and an H-bridge circuit to change the load voltage polarity. The first module can generate a maximum of 2Vdc and the second module is capable of generating a maximum of 4Vdc. Overall, this converter includes 9 switches, two switched capacitors, and three diodes. This CSCMLI is a fault-tolerant inverter. Due to the occurrence of the fault type in each switch, the number of output voltage levels reduces, but the inverter can keep working.

This article contains the following sections: The fault detection method is explained in Section II. Section III examines the component reliability calculations, and Section IV identifies the fault location based on the module component reliability prioritization. Section V presents the experimental results of the presented methods. Section VI discusses the obtained results. In Section VII, the open questions are mentioned, and finally, in Section VIII, the conclusions are presented.

II. FAULT DETECTION

To detect the fault, voltage sensing is performed at the output of the modules and before the H-bridge circuit at points a and b, which is shown in Figure 1(a). Also, the function diagram of fault detection and location is shown in Figure 1(b). The sampled voltage is compared online with the reference voltage in the processor, and the difference value is labeled as ΔV. Considering the voltage fluctuations of the capacitors due to charging and discharging and the voltage drop caused by the diodes and MOSFETs of the path, the allowable ΔV ranges to 5V. The voltage difference between the sampled voltage and the reference voltage in the range of 5V means that the modules are working correctly and therefore no faults occur. If a fault occurs within one of the MOSFETs, the ΔV value will be outside the allowable band, indicating the occurrence of faults in the modules. The performance of the inverter in normal mode and fault mode is simulated in MATLAB software. In the experimental test, when the fault is detected, the inverter is shut down to avoid damage to other parts, but in the simulation status, the operation of the inverter is not stopped, thus the inverter continues to operate after the occurrence of the fault to observe the V_{ab}, the ΔV, and the load voltage. Before the fault occurs, the ΔV value is in the range of 5 volts, which indicates that the inverter is working properly. When a fault occurs in one of the switches, the ΔV value exceeds 5 volts, indicating a fault in the circuit. Due to the short circuit fault in switches S11 and S12, the load voltage drops from 13 to 9 levels, which are shown in Figure 2 and Figure 3. If a fault occurs in one of the switches S21, S22, and S23, the waveform of the load voltage is distorted. In this case, the inverter can continue to operate by changing the switching algorithm, but the output voltage will be reduced. The focus of this paper is on fault detection and fault location. The presentation switching algorithm for the fault-tolerant operation of the inverter will be presented in future research.

III. RELIABILITY EVALUATION OF THE MODULES' COMPONENTS

The lower the reliability of a component, the more probably it is to fail in the electronic system. Reliability calculations can be used to increase the speed of the fault location process. In this section, the reliability of all components is calculated first, and then the priority of fault location is presented based on reliability. In other words, the lower the reliability value of a component, the higher the priority of the fault detection process for that component. The MIL-HDBK-217

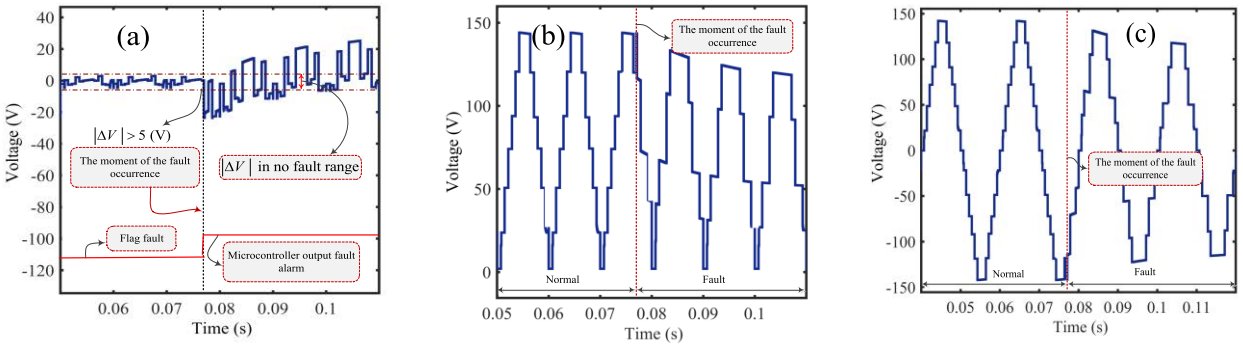

FIGURE 2. Occurrence of a fault on S11 and CSCMLI operation after the fault has occurred, a) the voltage of ΔV, b) Vab and c) the load voltage.

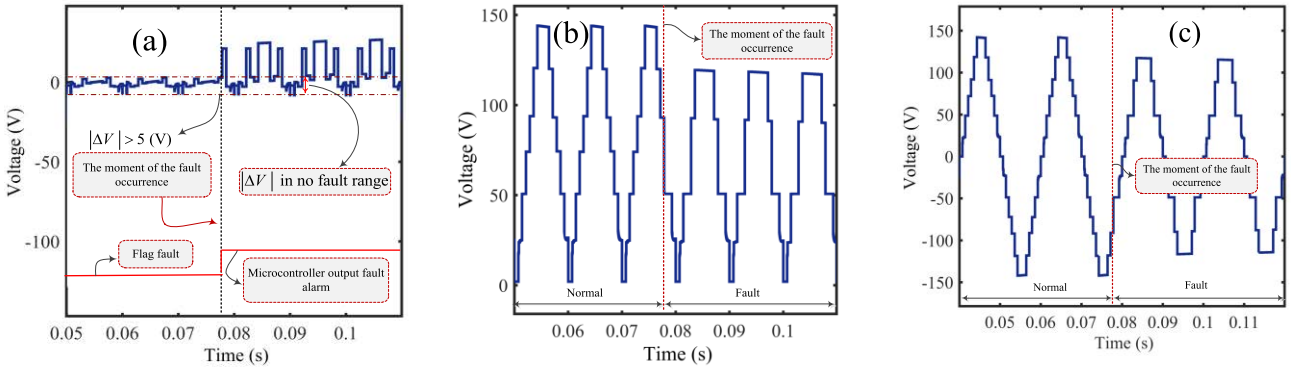

FIGURE 3. Occurrence of a fault on S12 and CSCMLI operation after the fault has occurred, a) the voltage of ΔV, b) Vab and c) the load voltage.

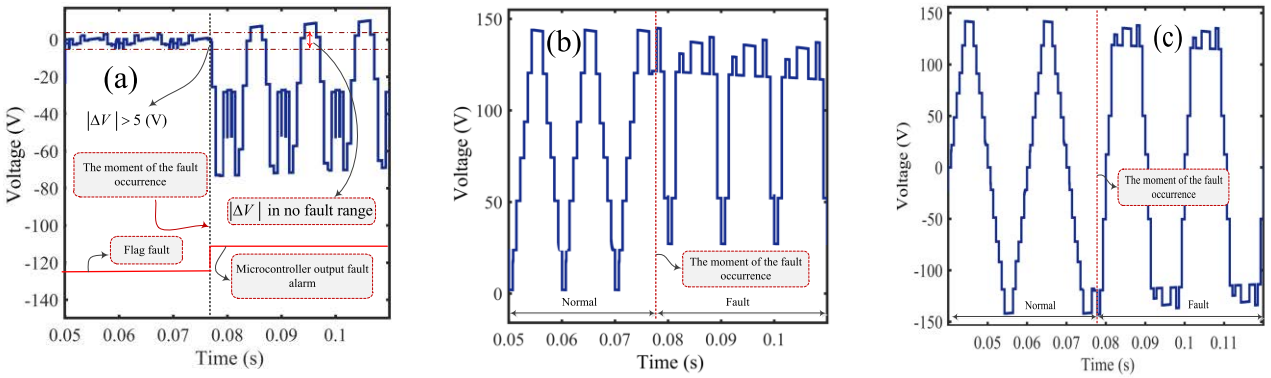

FIGURE 4. Occurrence of a fault on S21 and CSCMLI operation after the fault has occurred, a) the voltage of ΔV, b) Vab and c) the load voltage.

standard is used to evaluate the reliability of electronic components [14]. This standard describes how to calculate the failure rate considering the performance of the system under different environmental conditions. In papers [15], [16], MIL-HDBK-217 was also used for the reliability assessment of electronic components.

Equation (1) expresses the MTTF value based on the failure rate. Equations (2) and (3) specify how to evaluate the failure rate of MOSFETs. Equations (4) to (7) show the failure rate calculation of diodes, and (8) to (10) show the failure rate calculation of capacitors. Figure 7 shows the MTTF change curve of the mentioned components as a function of the changes in their respective variables.

$$\text{MTTP} = \frac{10^6}{\lambda_P} \tag{1}$$

$$\lambda_{p,\text{mosfet}} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \tag{2}$$

$$\pi_T = e^{(-1925(\frac{1}{T_J+273} - \frac{1}{298}))} \tag{3}$$

$$\lambda_{p,\text{diode}} = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E \tag{4}$$

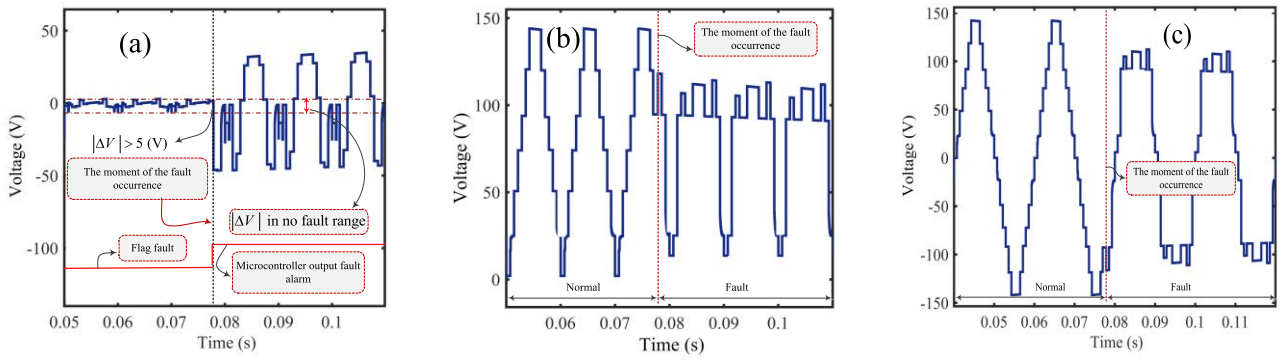

FIGURE 5. Occurrence of a fault on S22 and CSCMLI operation after the fault has occurred, a) the voltage of ΔV, b) Vab and c) the load voltage.

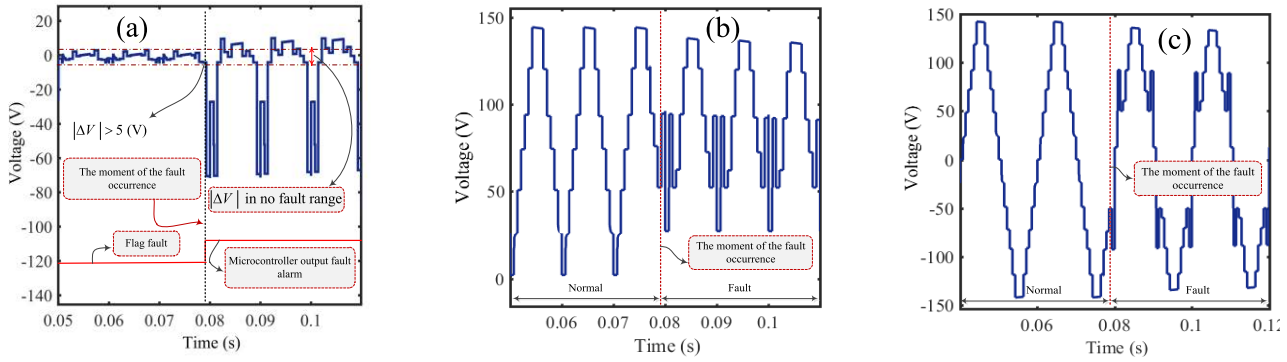

FIGURE 6. Occurrence of a fault on S23 and CSCMLI operation after the fault has occurred, a) the voltage of ΔV, b) Vab and c) the load voltage.

$$\pi_T = e^{(-3091(\frac{1}{T_J+273}-\frac{1}{298}))} \quad (5)$$

$$\pi_S = V_S^{2.43} \quad (6)$$

$$V_S = \frac{\text{Voltage Applied}}{\text{Voltage Rated}} \quad (7)$$

$$\lambda_{p,\text{capacitor}} = \lambda_b \pi_{CV} \pi_Q \pi_E \quad (8)$$

$$\lambda_b = 0.00254\left[\left(\frac{S}{0.5}\right)^3 + 1\right] e^{\left(5.09\left(\frac{T_J+273}{378}\right)^5\right)} \quad (9)$$

$$\pi_{\text{CV}} = 0.34C^{0.18} \quad (10)$$

Based on the above relationships, the MTTF value and failure rate of the components of the modules are evaluated. According to the results from Table 1, MOSFETs have the lowest MTTF compared to capacitors and diodes. Also, among the switches, the S23 switch has the lowest MTTF value, and the failure rate of this switch is higher than the other switches. All three switches S11, S21, and S22 are in the same power range, resulting in the same MTTF. Therefore, it is possible to determine their priority at the same MTTF value by considering the different power flowing from the switches [14], Ch. 6, pp: 9-11]. Table 1 also shows the flowing power of all switches. According to this, it is evident that switch S21, which transfers the highest power, has the highest failure rate among the three switches and is more likely to fail than the other two switches. Similarly, switch S11, with a flowing power of 170 W, has a higher failure rate than switch S22, with a power of 56 W. And finally, S12 with a lower MTTF has a lower failure rate compared to all MOSFETs.

IV. FAULT LOCATION BASED ON RELIABILITY PRIORITIZATION

The reliability of the different components of the modules was calculated in the previous section. It was taken into account that MOSFETs have lower MTTF. Therefore, the failure probability for the switches is very high compared to the capacitors and diodes of the modules. For this reason, the fault location method was applied only to the switches due to their high failure probability. According to the reliability table of MOSFETs (Table 1), switch S23 has the lowest MTTF and the three switches S11, S21, and S22 have the same MTTF. And finally, switch S12 has a high MTTF compared to the other switches, and since it also has a low power rate, the probability of failure is lower than the other switches.

According to the differences in MTTF and power flow of the switches, four test situations were considered based on prioritization, and the test duration in each condition was set to 100 microseconds, which are shown in Table 2. In condition A, switch S23 is tested, in conditions B, and C switches S11, S21, and S22 are tested, and finally in condition D, switch S12 is tested. In all these situations, V_{ab} is measured

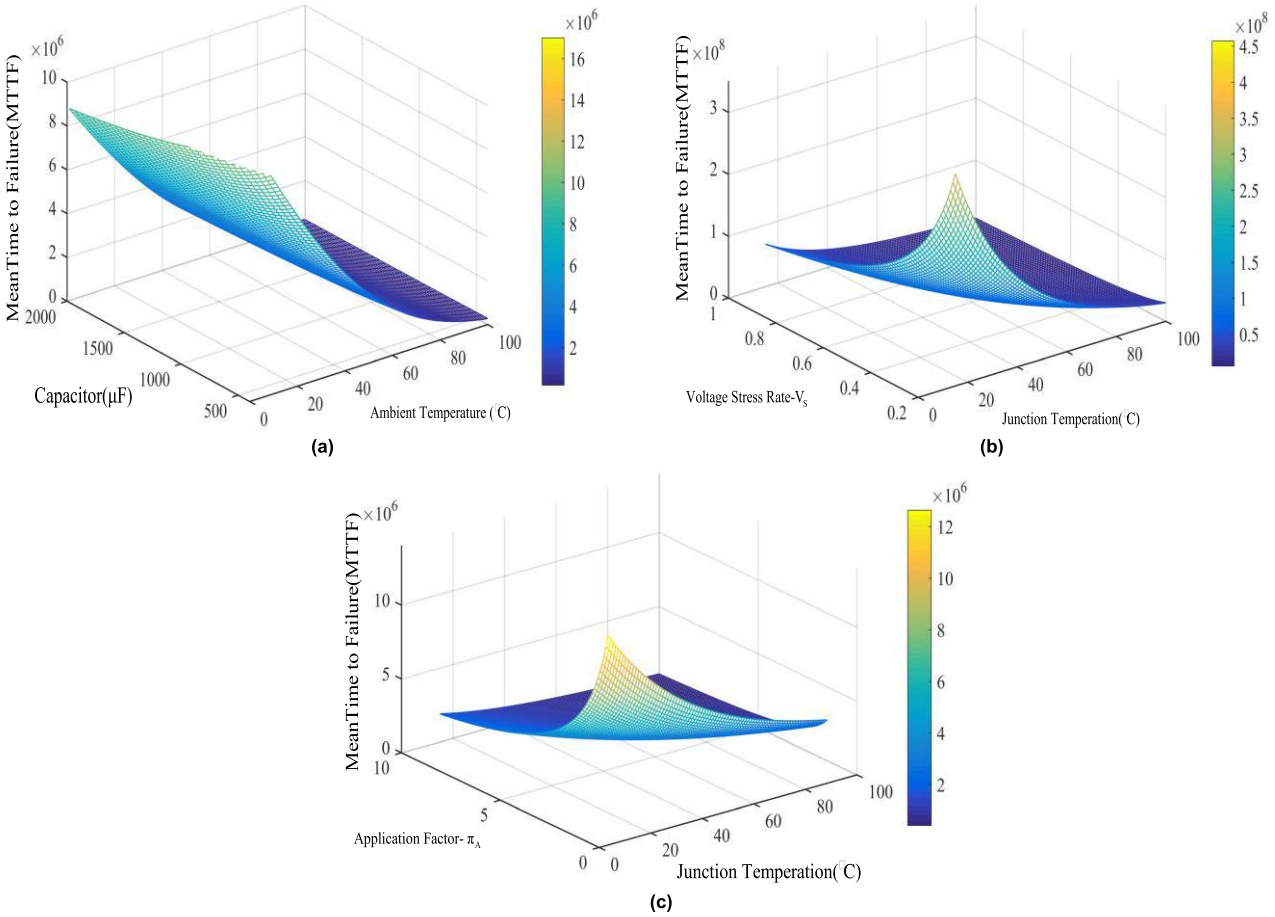

FIGURE 7. Mean time to failure of a) aluminum capacitor, b) diode, and c) MOSFET.

as shown in Figure 8, and the fault location is determined based on the state of the device under test and the values obtained from the measurement. In all four of the above conditions, switches T1 and T3 are turned on to discharge the energy stored in the inductive load and prevent current flow to modules. The conditions are as follows:

A. CONDITION A

In condition A, all switches are switched off. In this case, five different voltages can be generated at the output of the modules.

In the A1 state, when only switch S23 is shorted, two power sources are connected in series with a capacitor according to the topology of the modules, and a 2 V_{dc} output is generated. The power source is VDC2 and the capacitor is C11, which produces a voltage of 2 V_{dc} at the output. In the A2 state, shorting switches S11, and S23 causes two power sources VDC1, VDC2, and capacitor C11 to be connected in series, producing a 3 V_{dc} voltage at the output of the modules. In the A3 state, shorting switches S22, and S23 causes power supply VDC1 to be connected in series with capacitor C21, resulting in a voltage of 4 V_{dc} at the output of the modules. In addition, shorting switches S12, S22, and S23 causes capacitors C11, and C21 to be connected in series, resulting in a voltage of 4 V_{dc} at the output of the modules. In the A4 state, shorting switches S21, and S23 causes power supplies VDC1, VDC2, and capacitor C21 to be connected in series, resulting in a voltage of 5 V_{dc} at the output of the modules. Also, shorting S11, S22, and S23 causes the two capacitors C11, C21, and the power source VDC1 to be connected in series, resulting in a voltage of 5 V_{dc} at the output, and in state A5, shorting switches S11, S21, S23 will cause them to be connected in series. There are two power sources VDC1, VDC2, and capacitors C11, and C21 that produce a voltage of 6 V_{dc} at the output of the modules. In the above five states, the short circuit of switch S23 causes a voltage at the output, and depending on whether other switches are damaged, they produce a different voltage at the output. Consequently, in state A, the generation of a voltage at the output indicates a short circuit in MOSFET S23.

B. CONDITION B

In condition B, only switch S23 is on and the other switches are off. In this situation, four different voltages can be generated at the output of the modules, and the generation of each voltage indicates the short circuit of each switch. In state B1,

TABLE 1. Evaluation of the failure rate and MTTF of the components based on MIL-HDBK-217.

	Power	λ_b	π_T	π_A	π_Q	π_E	π_{CV}	π_S	π_C	λ_p	MTTF
S23	297	0.012	3.7	10	5.5	1	-	-	-	2.442	409500
S21	201	0.012	3.7	8	5.5	1	-	-	-	1.9536	511876
S11	170	0.012	3.7	8	5.5	1	-	-	-	1.9536	511876
S22	56	0.012	3.7	8	5.5	1	-	-	-	1.9536	511876
S12	36	0.012	3.7	4	5.5	1	-	-	-	0.9768	1023751
C11	-	0.046	-	-	10	1	1.51	-	-	0.6946	1439678
C12	-	0.028	-	-	10	1	1.24	-	-	0.3472	2880184
D11	-	0.069	8	-	5.5	1	-	0.054	2	0.16394	6099644
D12	-	0.069	8	-	5.5	1	-	0.054	2	0.16394	6099644
D22	-	0.069	8	-	5.5	1	-	0.054	2	0.16394	6099644

TABLE 2. Proposed fault location method based on reliability priority.

Condition		S11	S12	S21	S22	S23	T1	T2	T3	T4	V_{ab}	Description
A	A1	0	0	0	0	0	1	0	1	0	$2V_{dc}$±5V	Short Circuit S23 or Short Circuit S12, S23
	A2	0	0	0	0	0	1	0	1	0	$3V_{dc}$±5V	Short Circuit S11, S23
	A3	0	0	0	0	0	1	0	1	0	$4V_{dc}$±5V	Short Circuit S22, S23 or Short Circuit S12, S22, S23
	A4	0	0	0	0	0	1	0	1	0	$5V_{dc}$±5V	Short Circuit S21, S23 or Short Circuit S11, S22, S23
	A5	0	0	0	0	0	1	0	1	0	$6V_{dc}$±5V	Short Circuit S11, S21, S23
B	B1	0	0	0	0	1	1	0	1	0	$3V_{dc}$±5V	Short Circuit S11
	B2	0	0	0	0	1	1	0	1	0	$4V_{dc}$±5V	Short Circuit S22 or Short Circuit S22, S12
	B3	0	0	0	0	1	1	0	1	0	$5V_{dc}$±5V	Short Circuit S21 or Short Circuit S21, S12
	B4	0	0	0	0	1	1	0	1	0	$6V_{dc}$±5V	Short Circuit S11, S21
C	C1	0	0	1	0	1	1	0	1	0	$4V_{dc}$±5V	Short Circuit S22 or Short Circuit S12, S22
	C2	0	0	1	0	1	1	0	1	0	$6V_{dc}$±5V	Short Circuit S11
D	D1	1	0	1	0	1	1	0	1	0	$4V_{dc}$±5V	Short Circuit S12, S22
	D2	1	0	1	0	1	1	0	1	0	$5V_{dc}$±5V	Short Circuit S12

the short circuit of S11 causes two power supplies VDC1, and VDC2 to be connected in series with capacitor C11, resulting in a voltage of 3 V_{dc} at the output of the two modules. In state B2, the short circuit of S22 causes power supply VDC1 to be connected in series with capacitor C21, resulting in a voltage of 4 V_{dc} at the output of the modules ($V_{ab} = 4\ V_{dc}$). Moreover, the short circuit of switches S22 and S12 causes two capacitors C11, and C21 to be connected in series, resulting in a voltage of 4 V_{dc} at the output of the modules. In state B3, shorting switch S21 causes the two power supplies to be connected in series with capacitor C21, resulting in a voltage of 5 V_{dc} at the output of the modules. In state B4, shorting switches S11, and S21 causes the two power supplies VDC1, and VDC2 to be connected in series with the two capacitors C11, and C21 resulting in a voltage of 6 V_{dc} at the output.

C. CONDITION C

In condition C, switches S23 and S21 are turned on, and two different voltages are generated as a result of the faulty switches. In the C1 condition, the shorting of switch S22 causes capacitor C21 to be connected in series with power supply VDC1, producing a voltage of 4 V_{dc} at the output. Also, shorting switches S22 and S12 causes both capacitors C11 and C21 to be connected in series, resulting in a voltage of 4 V_{dc} at the output. In state C2, shorting switch S11 causes capacitors C11 and C21 to be connected in series with current

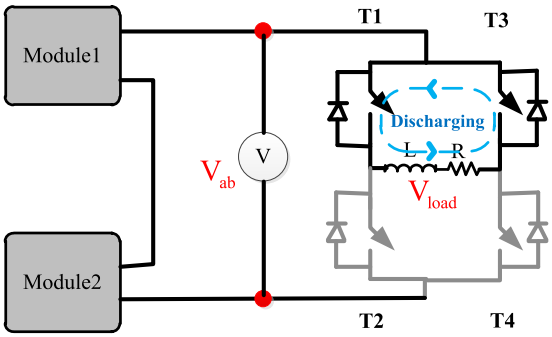

FIGURE 8. Vab position on the CSCMLI.

sources VDC1 and VDC2, resulting in a voltage of 6 V_{dc} at the output.

D. CONDITION D

In condition D, the switches S11, S21, and S23 are open. In this condition, the failure of these switches causes two different output voltages to be generated. In state D1, shorting switches S12, and S22 causes two capacitors C11, and C21 to be connected in series, producing a voltage of 4 V_{dc} at the output, and in state D2, shorting only switch S12 causes two capacitors C11, and C21 to be connected in series with the source VDC2, which produces a voltage of 5 V_{dc} at the output. From the results of Table 2, a Boolean algebra for debugging can be derived such as (11) to (15).

$$\text{Short Circuit S11} = \text{A2} + \text{A5} + \text{A6} + \text{A9} + \text{A11} \quad (11)$$

$$\text{Short Circuit S12} = \text{A12} + \text{A13} \quad (12)$$

$$\text{Short Circuit S21} = \text{A5} + \text{A8} + \text{A9} \quad (13)$$

$$\text{Short Circuit S22} = \text{A3} + \text{A7} + \text{A10} + \text{A12} \quad (14)$$

$$\text{Short Circuit S23} = \text{A1} + \text{A2} + \text{A3} + \text{A4} + \text{A5} \quad (15)$$

V. EXPERIMENTAL RESULTS

In this section, fault detection and fault location detection are performed for the inverter presented in [13]. For this purpose, five different scenarios were considered, each scenario representing a fault that occurred in a switch. It should be noted that the multi-level inverter modules have five switches and the five scenarios are all proposed scenarios of the short circuit fault in the inverter. By default, we do not know which switch is burned out, and the fault location should be determined based on Table 2 according to the reliability priorities. After all the switches are off, the inverter then needs to reach a steady state, which takes 50 microseconds. After that, the algorithm to detect the fault location is implemented in the circuit. Based on Table 2, Condition A is executed first, then Condition B and the other conditions until the location of the burnt switch is determined. It should be noted that when the fault is detected, all switches except T1 and T3 are turned off. Turning on switches T1 and T3 is done to discharge the energy stored in the inductive load. At the time of the fault, there is a difference between the voltage across the load and the V_{ab}, the reason for this difference is that the energy stored in the inductive load is discharged in switches T1, and T3, which is shown in Figure 8.

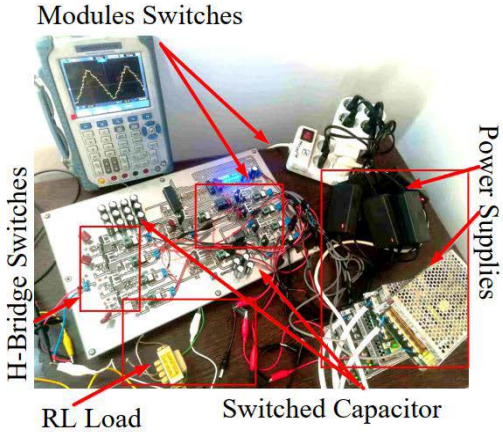

FIGURE 9. Experimental setup test.

A. SCENARIO 1: S11 SHORT CIRCUIT FAULT

In this scenario, the switch S11 is shorted and the fault detection and fault location determination are performed. Figure 10 shows the time of fault occurrence, fault detection, and fault location detection. Figure 10 shows the Vab waveform where the fault occurs in the 6th cycle, and after 60 microseconds, the fault is detected and the shutdown command is released immediately. By implementing the condition-A switching algorithm, the voltage output became zero, which is shown in Figure 10(b). The zero voltage in condition A does not correspond to any of the desired outputs in Table 2, so condition B is tested. The processor then allows the system to rest for 50 microseconds to reach a steady state until condition B is encountered in the circuit. According to Table 2, when condition B is implemented and Vab becomes equal to 3 Vdc (Vab = 3 Vdc), it means that switch s11 is damaged. It took 360 microseconds from the time the fault occurred until it was located.

B. SCENARIO 2: S12 SHORT CIRCUIT FAULT

In this scenario, the switch S12 is shorted. In this case, the operation of the circuit is shown in Figure 11. First, condition A is executed after the short-circuit detection. Since the $V_{ab} = 0$ in this condition, condition B is tested, and in this situation, the $V_{ab} = 2\ V_{dc}$. Then, the condition of C is checked, which results in the generation of a voltage of 5 V_{dc}, due to the mismatch between the conditions of A and B in Table 2, finally, the condition of C is checked, which generates a voltage of 5 V_{dc}, indicating that the S12 switch is damaged.

C. SCENARIO 3: S21 SHORT CIRCUIT FAULT

Figure 12 shows the time of occurrence of the short circuit, the fault detection, and the fault location detection. The detection of the fault location in this scenario is similar to the detection of the fault location in the first scenario. The only difference is that in the implementation of the algorithm for

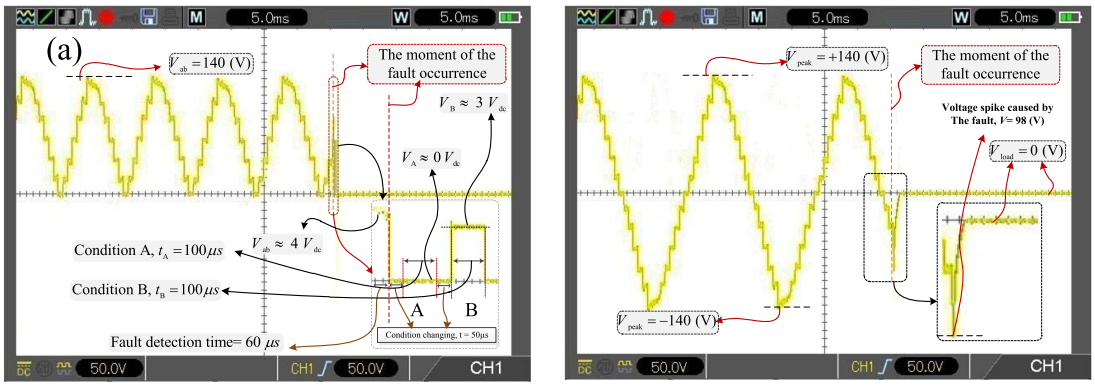

FIGURE 10. Experimental results of S11 short circuit, scenario 1, a) V_{ab} and b) V_{out} across the load.

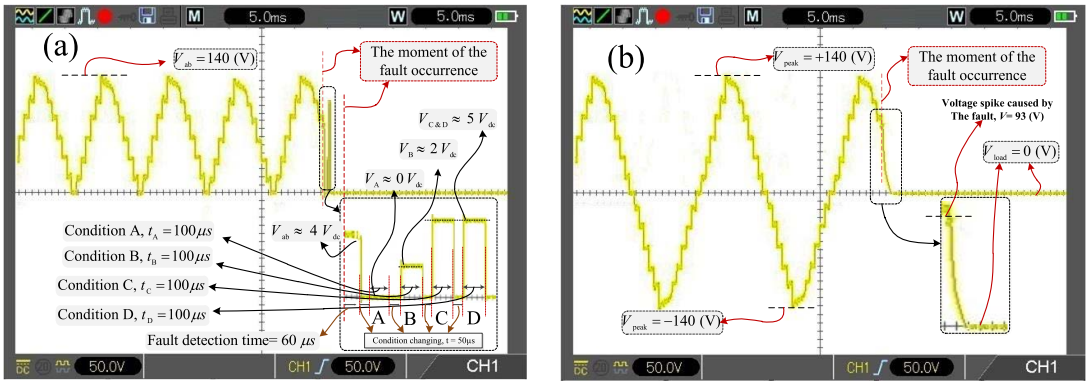

FIGURE 11. Experimental results of S12 short circuit, scenario 1, a) V_{ab} and b) V_{out} across the load.

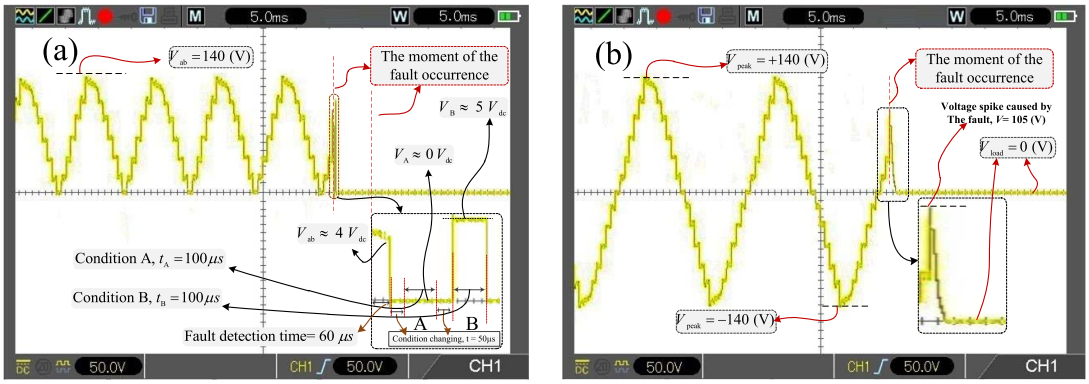

FIGURE 12. Experimental results of S21 short circuit, scenario 1, a) V_{ab} and b) V_{out} across the load.

condition B, it is detected that the switch S21 is shorted by observing the $V_{ab} = 5\ V_{dc}$.

D. SCENARIO 4: S22 SHORT CIRCUIT FAULT

Figure 13 also shows the time of occurrence of a short circuit, fault detection, and fault location detection. Similar to the first and third scenarios, the voltage in condition A is zero, but when the algorithm is implemented, the voltage in condition B is detected as $V_{ab} = 4\ V_{dc}$ which means the short circuit fault of switch S22.

E. SCENARIO 5: S23 SHORT CIRCUIT FAULT

In this scenario, S23 is short-circuited. The results of shorting switch S23 are shown in Figure 14. In this case, a voltage of 2 V_{dc} is observed in the V_{ab} voltage ($V_{ab} = 2\ V_{dc}$) in condition A, which indicates that switch S23 is shorted.

VI. DISCUSSION

The results of the experimental test show that the approximate duration of fault detection is between 40 and 60 microseconds. The duration of fault detection also depends

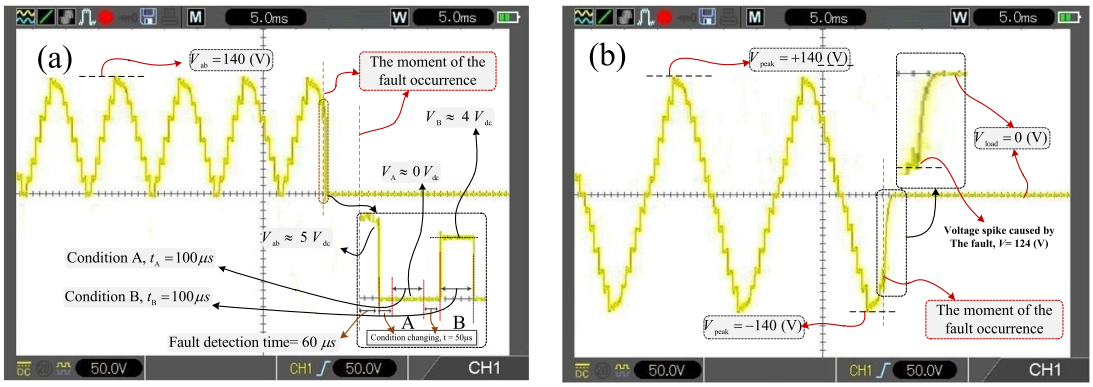

FIGURE 13. Experimental results of S22 short circuit, scenario 1, a) V_{ab} and b) V_{out} across the load.

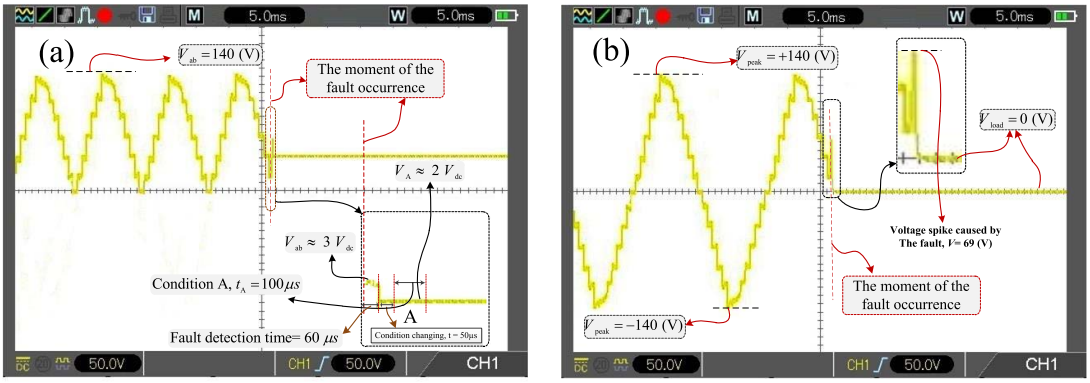

FIGURE 14. Experimental results of S23 short circuit, scenario 1, a) V_{ab} and b) V_{out} across the load.

TABLE 3. Comparison of the proposed method with similar methods.

	Fault detection /Method	Fault location ability	Advantages and disadvantages
[5]	THD measurement Normalized voltage Factor	THD measurement Normalized voltage Factor	+ Replace the faulty circuit with a redundant circuit, high reliability. - Not tested on the actual circuit, does not meet the required power of the load
[6]	Extended state observer (ESO)	Extended state observer (ESO)	+ Low computational complexity, and relatively fast fault detection. - Decreasing detection speed by increasing the number of modules.
[12]	EWP-SVM based method	EWP-SVM based method	+ Low computational complexity, and relatively fast fault detection. - One additional current sensor is required.
[10]	Convolutional Neural Networks	Convolutional Neural Networks	+ average identification probability of 0.997 in less than 100-ms. - High computational complexity, and a high number of sampling channels.
[9]	Estimated state variables, Kalman Filter	Kalman Filter	+ Optimal estimation, ability to detect multiple fault locations. - High computational complexity, large number of sensors.
[17]	based on FFT	Fast Fourier transform	+ High detection accuracy based on FFT analysis. -Low speed, high computational complexity.
Pro.	An improved normalized voltage reference	A method based on reliability	+ Fast, No complexity. - One additional sensor is required.

on which conditions of A, B, C, and D the fault is detected. As stated in the previous section, the primary criterion was the reliability of the switches. The minimum time for detecting the fault location is 210 microseconds concerning the short-circuit fault of switch S23 and the maximum time for detecting the fault location concerning switch S12, which is shown in Figure 11. In Table 3, a comparison is made between the presented approach, and the fault detection and fault location methods reported in other articles. Compared to the other presented methods, the proposed method has a low computational volume and a high speed compared to other methods. According to the presented algorithm based

TABLE 4. Comparison of 9-level fault-tolerant inverter with similar 9-level multilevel inverters.

Topology	N_L	Nsw	N_d	N_{dc}	N_C	TSV	Gain	Voltage Boosting
[18]	9	12	0	1	2	5.5	2	Yes
[19]	9	11	0	1	2	5	2	Yes
[20]	9	10	0	1	2	7.5	2	Yes
[21]	9	17	1	1	4	7.25	1	No
[22]	9	12	0	1	3	6	4	Yes
[23]	9	9	0	1	2	6.25	4	Yes
[24]	9	12	0	2	1	6	1	No
[25]	9	8	3	1	3	6.25	4	Yes
[26]	9	10	0	1	2	5.5	2	Yes
[20]	9	11	1	1	2	11	2	Yes
[27]	9	10	2	1	2	9	2	Yes
[28]	9	10	2	1	4	9	3	Yes
[29]	9	8	3	1	3	5.75	4	Yes
[30]	9	12	0	2	1	8	2	Yes
[31]	9	9	2	1	2	5.75	2	Yes
[32]	9	8	2	1	2	4.36	2	Yes
[33]	9	17	5	1	4	12.25	4	Yes
[34]	9	12	0	1	2	5.25	4	Yes
Proposed	9	9	3	2	2	6	2	Yes

on prioritization by reliability, it is possible to detect the fault location in a shorter time. Also, when the switch burnout leads to the generation of the maximum voltage of 4Vdc in the output, the inverter becomes 9-level. Table 4 shows the comparison between the inverter in normal operation and the 9-level faulty inverter with similar new multilevel items.

As shown in Table 4, the proposed CSCMLI seems to have fewer components compared to similar MLIs, even after the occurrence of a fault. For example, the number of switches in this fault-tolerant 9-level MLI is still less than other items. The other parameters of the provided inverter are also in a good condition compared to other inverters.

VII. CONCLUSION

The quickness of fault detection and fault localization is extremely important in a fault-tolerant inverter. The occurrence of a fault can lead to the occurrence of faults in other parts of the inverter, and the faster the fault is detected, the less the inverter will be damaged. In this article, the fault was detected in less than 60 microseconds using a non-invasive analog method, and the location of the fault was also determined using a new method that incorporates the reliability and lifetime of electronic components. The time for fault location was less than 360 μs in the worst case. By calculating the reliability of electronic components, the probability of a fault occurrence of the components can be estimated. As a result, the duration of fault location could be reduced. The practical implementation of the presented methods confirms their applicability.

VIII. OPEN QUESTIONS

This article is a continuation of the 13-level inverter [13], where one of the open issues was the investigation of the fault tolerance of CSCMLI, and this article has tried to investigate this issue to some extent. There are still many issues related to the study of this inverter that will be investigated in the future. Some of these issues can be summarized as follows:

1- The proposed multilevel inverter can continue to operate at a lower voltage only if one or more electronic parts of the module circuits are damaged, but if any of the H-bridge circuit switches are damaged, the inverter will be completely destructed. Therefore, one of the open solutions is to find solutions to increase the reliability and lifetime of H-bridge switches.

2- Is it possible to use other switches with higher reliability instead of MOSFETs in the H-bridge circuit?

3- Another open question is the use of artificial intelligence methods based on a neural network to detect the fault location in the presented inverter. It is necessary to check whether other methods have a higher speed than the currently presented method in this inverter or not.

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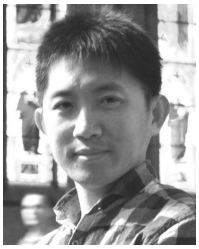

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