DEEP LEVEL TRANSIENT SPECTROSCOPY MEASUREMENTS OF GaAsBi/GaAs

by

Zenan Jiang
B. Sc., Tsinghua University, 2007

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

In the Department
of
Physics

SIMON FRASER UNIVERSITY

Summer 2010

APPROVAL

Name:	Zenan Jiang
Degree:	Master of Science
Title of Thesis:	Deep level transient spectroscopy measurements of GaAsBi/GaAs
Examining Committee:	Dr. J. Steven Dodge Chair
	Dr. Patricia Mooney, Senior Supervisor
	Dr. Simon Watkins, Supervisor
	Dr. Karen Kavanagh, Supervisor
	Dr. Mike Thewalt, Internal Examiner
Date Approved:	June 24, 2010

Declaration of
Partial Copyright Licence

Abstract

Bismuth incorporation in GaAs produces a much larger reduction in the band gap than In or Sb alloying, for the same increase in lattice constant. However, Bi is incorporated only at growth temperatures (T_g) < 400 °C, making deep level defects a concern. GaAsBi layers, GaAs layers and *p-i-n* structures having a 50 nm GaAsBi quantum well with bismide fraction ≤ 5% in the center of the intrinsic layer were grown by molecular beam epitaxy in the temperature range 285-580 °C. Deep level transient spectroscopy (DLTS) measurements of GaAsBi and GaAs Schottky diodes show several different traps. Similarly, DLTS spectra from the *p-i-n* devices vary with the growth conditions and the bismide fraction. The trap concentrations were found to be ≤ 5×10^{15} cm^{-3}, consistent with reported photoluminescence and electroluminescence measurements of the GaAsBi *p-i-n* structures. The possible identity of some of the traps is discussed.

Acknowledgements

I would like to thank the following individuals: Dan Beaton, Ryan Lewis and Dr. Tom Tiedje in UBC/Uvic for growing the samples used in this experiment, Xudong Chen for teaching me how to use the DLTS system, Alberto Basile for discussing the experiments and simulations with me, Dr. Simon Watkins and Dr. Karen Kavanagh for their comments and advice to this work, my parents, Kejun and Yuee for always supporting any of my decisions, and finally, Dr. Pat Mooney, my supervisor, who was always had helpful advice or suggestions when I had problems.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

III-V compound semiconductors and their alloys contain elements from column IIIA and column VA of the periodic table. The ratio between atoms from each column is 1:1. Many III-V semiconductors have a direct band gap. Consequently, these semiconductors have higher electron mobility than Silicon, which makes them useful in high frequency electronics such as hetero-junction bipolar transistors and power amplifiers. The variety of III-V compound semiconductors and their ternary or quaternary alloys provide a wide range of band gap energies, which is particularly useful when a specific band gap energy is required. These properties lead to applications of III-V semiconductors in photonic devices such as laser diodes, optical detectors, and solar cells.

Bismuth is the heaviest element in group V of the periodic table, and has been largely neglected in device fabrication. Incorporating a small amount Bi into GaAs reduces the band gap significantly without causing much lattice mismatch strain, which makes the material useful for hetero-junction devices such as multi-junction solar cells, bipolar transistors, and light emitting diodes. However, to grow $GaAs_{1-x}Bi_x$ alloy requires non-standard growth conditions; specifically a very low substrate temperature and a ratio of As/Ga flux of 1. Due to these non-standard growth conditions, the formation of deep level defects is a major concern.

This research focuses on the characterization of deep level defects in $GaAs_{1-x}Bi_x$. $GaAs_{1-x}Bi_x$ Schottky diodes, *p-i-n* diodes having a thin intrinsic $GaAs_{1-x}Bi_x$ quantum well with bismide fraction up to 4.7%, and GaAs Schottky diodes grown by molecular beam epitaxy were measured with deep level transient spectroscopy (DLTS). Chapters 2 and 3 of this thesis present an overview of the properties of semiconductors and semiconductor diodes. Chapter 4 describes the DLTS technique and the equipment used in our measurements. The electrical and optical properties as well as the growth of $GaAs_{1-x}Bi_x$ alloy are introduced in Chapter 5. The following three chapters present the experimental data, results and analysis.

Chapter 2

Semiconductor physics and defects

It is very important to understand the band structure and carrier transport in semiconductors in order to study the properties of defects. In this chapter, an overview of semiconductor physics is presented, as well as the behaviour of deep level defects in equilibrium. Section 2.1 is based on Chapters 1-5 in Reference 1, and other sections are from Chapter 1 in Reference 2, Chapter 5 in Reference 3, and Chapter 7 in Reference 4.

2.1 Physical properties of semiconductors

2.1.1 Energy bands and band gap

The electrons of a single isolated atom, interacting with the core potential and other electrons occupy a discrete set of energy levels and form atomic orbitals with a certain energy. When semiconductor atoms are brought together to form a crystal, orbitals from different atoms overlap with each other, more for outer-shell levels and less for inner ones. Interactions between electrons from different atoms cause the original energy levels to split into discrete levels. A large number of energy levels with little energy difference form essentially continuous bands of energy, which are called allowed bands, with energy gaps between these

bands. Electrons are no longer limited within a single atom, but rather move over the entire crystal. The electrons are distributed in allowed energy bands separated by band gaps.

The highest energy band that is occupied is known as the valence band and the lowest unoccupied band is the conduction band. The energy difference between the top of valence band, E_V, and the bottom of conduction band, E_C, is the band gap E_g. Semiconductors usually have band gap energy between 0 and 6 eV. Generally, intrinsic semiconductor materials are not conductive when the temperature is 0 K. However, electrons in the valence band can be excited to conduction band at room temperature, which results in a non-zero intrinsic carrier concentration.

An electron is emitted from the valence band to the conduction band thermally and becomes a quasi-free particle, leaving an unoccupied level behind. Another electron in the valence band may fill the unoccupied state and generate another unfilled level. The missing electron is considered a positive charge or "hole" that is free to move in the valence band. It is helpful to explain the motion of the vast concentrations of electrons in the valence band with a low concentration of holes. Unlike most of the metals, where the only charge carriers are electrons, electrons and holes both commonly conduct electricity in semiconductors.

If electrons transit from one band to another band without momentum changing, which means that the top of the valence band and the bottom of the conduction band are at the same $\vec{k}$ value, this material is a direct band gap material, such as GaAs. Other materials, like Si or GaP, with conduction band minimum and valence band maximum along different $\vec{k}$ value have an indirect band gap.

2.1.2 Carrier concentration and Fermi level

One of the most important properties of a semiconductor is that it can be doped with different types and concentrations of impurities to vary its conductivity. When these impurities are ionized, they provide free carriers and leave the ions behind which results in an electric field inside the semiconductor.

In intrinsic silicon, for example, each atom shares four valence electrons with four neighbours, forming covalent bonds. If a substitutional phosphorous atom with five valence electrons replaces a silicon atom, four of the electrons are involved in the covalent bonds that hold the crystal atoms together, and the extra electron is donated to the lattice and becomes a carrier, as shown in Fig. 2.1(a). The phosphorous atom is called a "donor". A semiconductor doped with donor impurities is an *n*-type material. Similarly, when a silicon atom is replaced by a boron atom, a positive carrier is created, as shown in Fig. 2.1(b). The boron atom is called an "acceptor", and the silicon doped with acceptors is *p*-type.

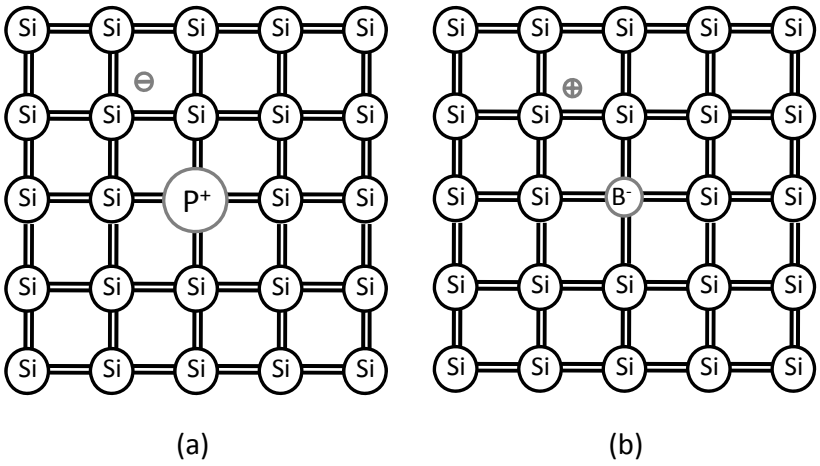


Figure 2.1 Diagram of a two-dimensional lattice with (a) a donor atom and (b) an acceptor atom. [Adapted from Fig. 4.3 and Fig. 4.4 in Ref. 1]

The motion of electrons in a crystal lattice is different from that of free electrons in the vacuum state. The movements of carriers may be affected by external forces, as well as the internal forces produced by ions and other electrons. Since it is difficult to consider every internal force, the effective mass m^* is introduced, and the motion of carriers in a crystal under an external force can be interpreted with a semi-classical Newton's law: $\vec{F}_{ext} = m^* \vec{a}$.

In a non-degenerately doped semiconductor, applying Boltzmann statistics as an approximation, the carrier concentration at thermal equilibrium can be expressed as [1]

$$n = N_C(T)\exp\left(-\frac{E_C - E_F}{kT}\right), \tag{2.1}$$

$$p = N_V(T)\exp\left(-\frac{E_F - E_V}{kT}\right), \tag{2.2}$$

where N_C and N_V are the effective density of states in the conduction and valence bands and E_F is the Fermi energy level. Electrons in the crystal lattice follow the Fermi-Dirac Distribution,

$$f_F(E) = \frac{1}{1+\exp\left(\frac{E - E_F}{kT}\right)}. \tag{2.3}$$

In Equation (2.3), $f_F(E)$ represents the probability of a state with energy E being occupied by an electron. The Fermi level E_F is the energy for which the probability of the state being occupied is equal to 1/2.

When impurities are introduced into a semiconductor crystal, not all dopants are ionized, depending on the energy needed to remove the electron from the impurity atoms and the temperature (Equation 2.1 and 2.2). Figure 2.2 shows the position of the Fermi level in *n*-type and *p*-type semiconductors and the impurity levels.

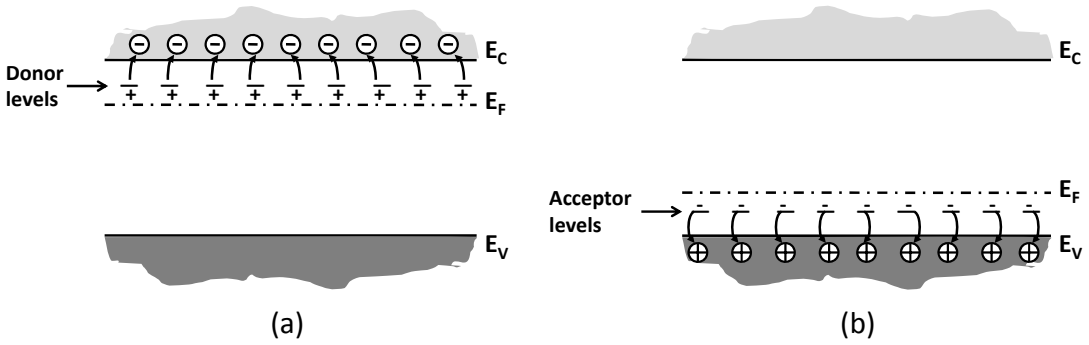


Figure 2.2 Impurity level and Fermi level of an (a) *n*-type and a (b) *p*-type semiconductor. [Adapted from Fig. 4.12 in Ref. 1]

2.1.3 Mobility and carrier transport

If the electric field inside the semiconductor is constant, the current density can be written as

$$\left|J_n\right| = \sigma\left|\vec{E}\right|, \tag{2.4}$$

where $\left|\vec{E}\right|$ is the electrical field strength and σ is conductivity of the semiconductor.

Electrons have a constant average drift velocity when the electric field is constant.

$$\left|\overline{v}_d\right| = \mu_n\left|\vec{E}\right|, \tag{2.5}$$

and μ_n is defined as the mobility of electrons in the semiconductor.

Hence, in a semiconductor with both electrons and holes, the conductivity is

$$\sigma = ne\mu_n + pe\mu_p, \tag{2.6}$$

where n and p is the electron and hole concentration, respectively, and μ_p is the mobility of holes.

Carriers can only be accelerated while they are drifting between two scattering events. So, mobility is related to the mean free path of the carriers. Increasing temperature and having a larger effective mass will shorten the mean free path of the carrier, and reduce the mobility. In addition, the doping concentration is another factor related to the mobility. In general, mobility decreases with increasing impurity concentration because the scattering by impurities shortens the mean free path of the carriers.

When the carrier concentration in a semiconductor is non-uniform, carriers diffuse until equilibrium is achieved. The diffusion current density is

$$J_n = eD_n \frac{dn}{dx}, \tag{2.7}$$

for electrons in one dimension, where D_n is called the electron diffusion coefficient. Similarly, the hole diffusion current density is

$$J_p = eD_p \frac{dp}{dx}, \tag{2.8}$$

where D_p is the hole diffusion coefficient.

Now, four possible independent current components are in a semiconductor and the total current density in three dimensions is given by

$$\vec{J} = en\mu_n \vec{E} + ep\mu_p \vec{E} + eD_n \vec{\nabla} n - eD_p \vec{\nabla} p \,. \tag{2.9}$$

Here, the mobility terms indicate the carrier motion as a result of an electric field, and the diffusion coefficient represents the effect of a density gradient. The two parameters are not independent of each other. Due to Einstein relation,

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e}, \tag{2.10}$$

with k the Boltzmann constant, and T the temperature.

2.2 Semiconductor defects

An ideal single crystal does not contain any defects or impurities, and all atoms in the crystal lattice are in equilibrium. Real materials are not ideal and perfect. Impurities added to vary the conductivity and contaminants may all break the periodicity of the crystal lattice and may introduce energy levels in the semiconductor band gap.

Point defects involve only one or several atoms, such as impurities, either dopants (added intentionally) or contaminants (added unintentionally). Interstitial impurities, usually with a small atom radius such as H and Li, exist in the intervening space between crystal atoms (Fig. 2.3 (a)). Substitutional defects replace atoms at lattice points (Fig. 2.3 (b) and (c)). These impurities have similar orbital configurations of valence electrons as semiconductor atoms, as III and V groups doped in Si and Ge, or II and VI groups in III-V compounds. Another type of point defect is a missing atom of the host crystal, a vacancy. In a compound semiconductor, a group III atom may be located on a group V lattice site, or vice versa and this is known as an anti-site defect. These defects are shown in Fig. 2.4.

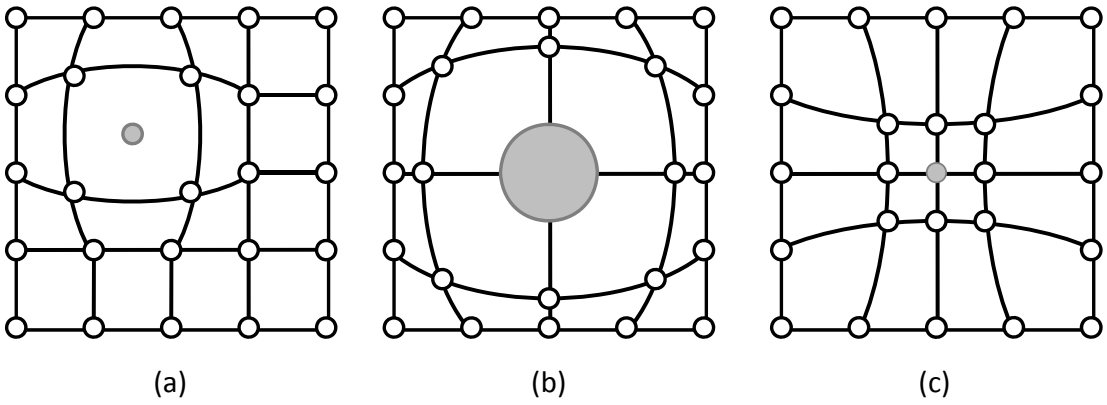


Figure 2.3 Impurity defects (a) small atom interstitial; (b) and (c) substitutional atoms.

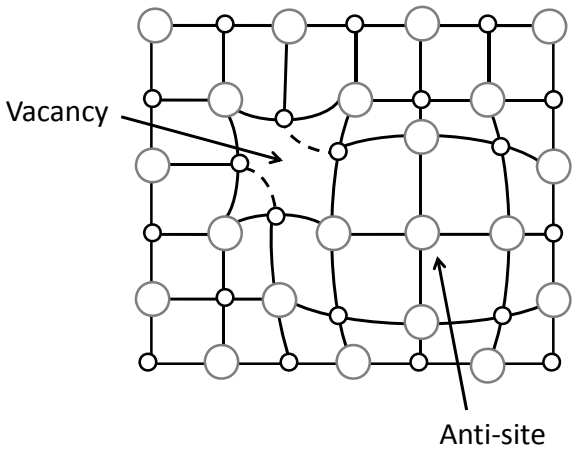


Figure 2.4 Vacancy and anti-site defects.

In semiconductors there are two kinds of defects which have completely different characteristics and effects: those that introduce levels which have quite a small energy difference from the bottom of the conduction band or the top of the valence band are called “shallow defects”, and determine type and conductivity of a semiconductor; others that introduce levels which are deep in the band gap, are called “deep levels”, as shown in Fig. 2.5. Vacancies, interstitials, dislocations, and anti-sites in compound semiconductors and other defects may also introduce levels in the band gap.

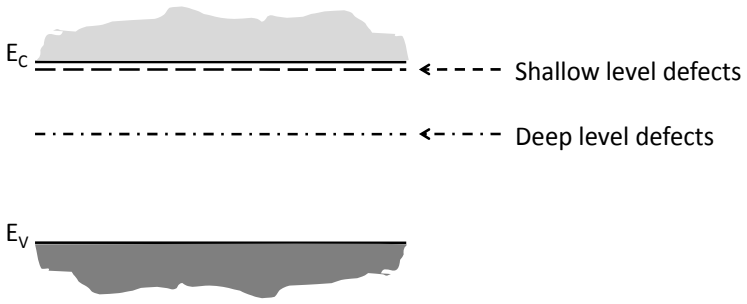


Figure 2.5 Shallow levels and deep levels for electrons in an *n*-type semiconductor.

Deep levels have important effects in semiconductor materials and devices. First, deep levels that are close to mid-gap may form effective recombination centers that increase the rate at which electrons and holes recombine, and therefore shorten the lifetime of carriers. Meanwhile, because the energy difference between deep levels and allowed bands is smaller than the band gap, it is easier to excite carriers from deep levels to conduction or valence bands and generate electron-hole pairs.

To improve the quality of semiconductor materials and devices, it is necessary to understand the nature and effects of deep level defects, in order to make use of their advantages sufficiently and reduce their harmfulness.

2.3 Deep levels in the band gap

There are no allowed energy levels inside the band gap in an *ideal* semiconductor. As discussed in the previous section, some states with a very small energy difference from the conduction or valence band edge are shallow levels, whereas other states that are deep in the band gap are deep levels, which can behave as traps or generation-recombination centers, depending on the temperature and energy levels. As in GaAs, shallow defects have energy levels within a few tens of meV from the respective band edges, whereas deep defects typically reside within the middle third of the band gap energy.

2.3.1 Carrier capture and emission

There are mainly two types of dynamic behaviour at a deep level, namely the capture and emission processes for electrons or holes. The following figure (Fig. 2.6) shows electron and hole traps and a recombination center.

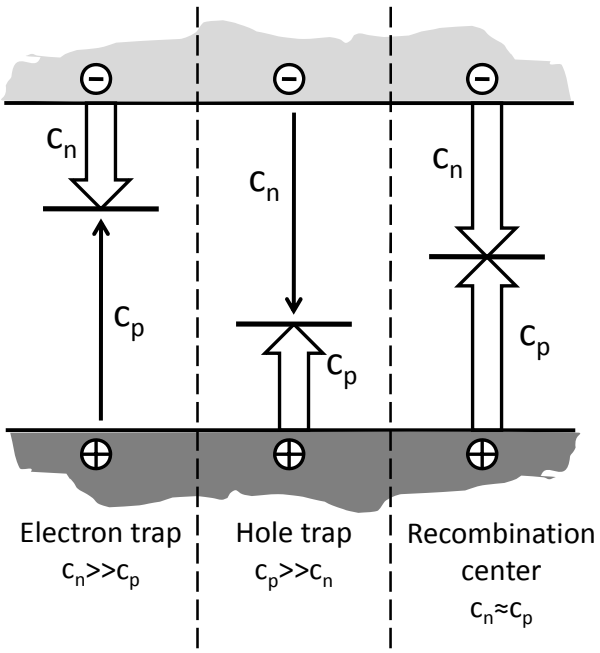


Figure 2.6 Definition of an electron trap, a hole trap and a recombination center. The four arrows show the processes of a trap capturing electrons and holes from the conduction and the valence bands. The width of the arrows indicates that relative size of c_n and c_p.

The capture process is characterized by the capture cross section. Consider that a flux of n electrons per unit volume with root mean square thermal velocity $\langle v_n \rangle$ is captured by a certain concentration of identical deep level centers with a capture cross section σ_n, this will give c_n, the capture rate per empty state (in the unit of s^{-1}), as

$$c_n = \sigma_n \langle v_n \rangle n, \tag{2.11}$$

where n is the electron concentration. A similar expression can be written for the capture rate of holes onto occupied states as

$$c_p = \sigma_p \langle v_p \rangle p. \tag{2.12}$$

The electron emission rate per occupied state e_n and hole emission rate per empty state e_p, represent the number of carriers emitted from a certain concentration of identical deep centers per unit time. The emission rates are mainly intrinsic properties of the deep level itself, independent of the doping, whereas the capture rate is dependent on both the deep level and the doping of the material.

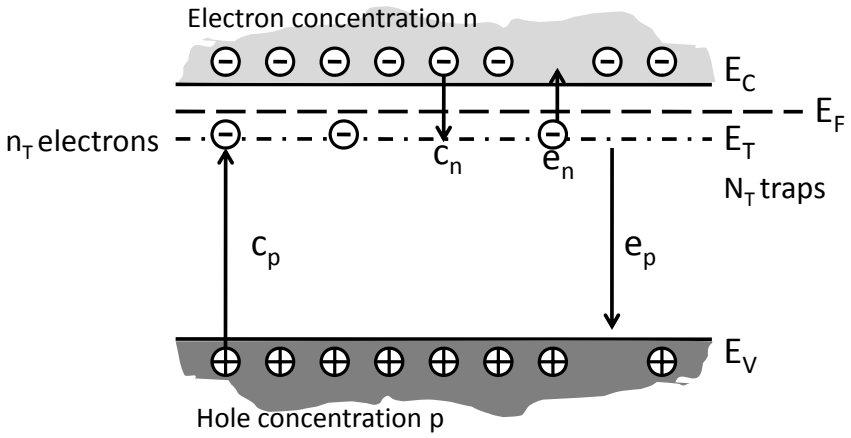


Figure 2.7 Electron and hole capture and emission processes for a trap with energy level E_T and density N_T containing a density n_T of electrons. E_F is the Fermi level of the semiconductor, n and p are the electron and hole concentrations in the conduction band and valence band. The initial state of each transition is shown. [Adapted from Fig. 7.1 in Ref. 4]

Consider an *n*-type material with a deep level that may be occupied by an electron or hole. The occupancy of the state is determined by the competition of both emission and capture processes. In Fig. 2.7, electrons are emitted and holes captured at the states occupied with electrons, while holes are emitted and electrons captured at empty states. Define N_T as the total concentration of deep level states, and n_T the concentration of states occupied by electrons. In a short interval Δt, the net change of electron occupancy is

$$\Delta n_T = (c_n + e_p)\Delta t(N_T - n_T) - (e_n + c_p)\Delta t n_T, \tag{2.13}$$

Here, $\left(N_T - n_T\right)$ is the concentration of empty states. When N_T is small compared to the net doping, the free carrier concentration is considered unchanged by this process, and c_n and c_p are given by Equations (2.11) and (2.12) with constant n and p. Therefore, the net rate of change is

$$\frac{dn_T}{dt} = (c_n + e_p)(N_T - n_T) - (e_n + c_p)n_T. \tag{2.14}$$

The solution to this differential equation is

$$n_T(t) = n_T(0)e^{-\frac{t}{\tau}} + \frac{c_n + e_p}{c_n + e_p + e_n + c_p} N_T\left(1 - e^{-\frac{t}{\tau}}\right), \tag{2.15}$$

where $n_T(0)$ is the concentration of electron occupied states at $t = 0$, and time constant

$$\tau = \left(c_n + e_p + e_n + c_p\right)^{-1}. \tag{2.16}$$

For $n_T(0) = 0$, when deep levels are all empty initially,

$$n_T(t) = \frac{c_n + e_p}{c_n + e_p + e_n + c_p} N_T\left(1 - e^{-\frac{t}{\tau}}\right); \tag{2.17}$$

whereas for $n_T(0) = N_T$, when all deep states are occupied initially [4],

$$n_T(t) = \frac{e_n + c_p}{c_n + e_p + e_n + c_p} N_T e^{-\frac{t}{\tau}}. \tag{2.18}$$

If the deep level concentration is comparable to the free carrier concentration, then n and p are no longer constant and other equations for $n(t)$ and $p(t)$ are needed to solve Equation (2.14).

2.3.2 Deep levels in thermal equilibrium

In thermal equilibrium, the occupacy of a deep level is constant, as determined by the constant relative value of the trap energy and Fermi level. The capture and emission processes must satisfy the principle of detailed balance, which in this case means the rates of electrons captured and emitted must be equal, as must be the rates of holes. If not, carriers could transfer from one band to the other when the trap occupancy remains the same. For instance, an electron could first be excited from valence band to the trap level, and then emitted to conduction band. The occupation of the trap is still the same while the number of electrons in conduction band increases. The detailed balance condition requires

$$e_n n_T = c_n (N_T - n_T), \tag{2.19}$$

and $c_p n_T = e_p (N_T - n_T)$. (2.20)

Hence, in thermal equilibrium, we have

$$\frac{n_T}{N_T} = \frac{c_n}{c_n + e_n} = \frac{e_p}{c_p + e_p}. \tag{2.21}$$

The occupancy of the deep level is described by the Fermi-Dirac distribution at equilibrium. For a deep state at energy E_T with degeneracy g_0 when empty and g_1 when occupied by an electron, the occupancy is

$$n_T = \frac{N_T}{1 + \frac{g_0}{g_1} \exp\left(\frac{E_T - E_F}{kT}\right)}. \tag{2.22}$$

The degeneracy of a state means how many different ways a state is occupied by an electron (as g_1) or a hole (as g_0).

Combining Equation (2.21) and (2.22), for electrons,

$$\frac{e_n}{c_n} = \frac{g_0}{g_1} \exp\left(\frac{E_T - E_F}{kT}\right), \tag{2.23}$$

and for holes,

$$\frac{e_p}{c_p} = \frac{g_1}{g_0} \exp\left(\frac{E_F - E_T}{kT} \right). \tag{2.24}$$

Clearly, when $g_0 = 1$ and $g_1 = 1$, $c_n > e_n$, $e_p > c_p$, and the state is empty if E_T is above Fermi level; whereas $e_n > c_n$, $c_p > e_p$, and the state is occupied if E_T is below Fermi level.

According to Equation (2.1), the free electron concentration at equilibrium is

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT} \right), \tag{2.25}$$

Substituting Equation (2.11) and (2.25) into (2.23), one can obtain the result for e_n:

$$e_n(T) = \sigma_n \langle v_n \rangle \frac{g_0}{g_1} N_C \exp\left(-\frac{E_C - E_T}{kT} \right). \tag{2.26}$$

Similarly,

$$e_p(T) = \sigma_p \langle v_p \rangle \frac{g_1}{g_0} N_V \exp\left(-\frac{E_T - E_V}{kT} \right). \tag{2.27}$$

We see that the emission rate of a deep level is primarily described by the capture cross section and the energy difference from the appropriate band. Although these relations were derived for a semiconductor in thermal equilibrium, they are also used in other situations. One such situation is discussed in section 4.1.

2.3.3 Majority and minority traps

The general behaviour of a deep state is complicated, because both emission and capture processes of two kinds of carriers have to be taken into consideration. Hence, there are in total four kinds of traps, electron traps in *n*-type material, hole traps in *n*-type material, electron traps in *p*-type material and hole traps in *p*-type material.

From Equation (2.26) and (2.27), the trap level that has equal emission rate $e_p = e_n$ for electrons and holes has the energy E_1 as

$$E_1 = \frac{E_C + E_V}{2} + \frac{kT}{2} \ln\left(\frac{\sigma_p \langle v_p \rangle g_1 / g_0 N_V}{\sigma_n \langle v_n \rangle g_0 / g_1 N_C} \right). \tag{2.28}$$

The precise energy of the level, given by Equation (2.28), depends on the level itself and the intrinsic properties of the material. It is typically located close to mid-gap. Levels with $E_T > E_1$, that is $e_n > e_p$ are more likely to capture/emit electrons from/to the conduction band, and are called "electron traps"; while levels with $E_T < E_1$ which is $e_p > e_n$ are called "hole traps".

The emission rate is related to the trap energy, and the capture rate as well as the position of Fermi level, which depends on the doping concentration. Therefore, all the traps can be sorted into the four categories, shown in Table 2.1.

Table 2.1 Dominant processes and equilibrium occupancy for electron and hole traps in *n*- and *p*-type materials. p_T is the concentration of the unoccupied trap states. [4]

	Material	
Trap type	*n*-type $E_F > E_T$ $c_n > e_n$ $e_p > c_p \approx 0$	*p*-type $E_F < E_T$ $c_p > e_p$ $e_n > c_n \approx 0$
Electron $E_T > E_1$ $e_n \gg e_p$	(majority trap) $c_n > e_n \gg e_p > c_p \approx 0$ $n_T = \frac{c_n}{c_n + e_n} N_T = N_T$	(minority trap) $c_p > e_p,\ e_n > e_p,\ c_n \approx 0$ $p_T = N_T$
Hole $E_T < E_1$ $e_n \ll e_p$	(minority trap) $c_n > e_n,\ e_p > e_n,\ c_p \approx 0$ $n_T = N_T$	(majority trap) $c_p > e_p \gg e_n > c_n \approx 0$ $p_T = N_T$

For an electron trap in an *n*-type material, the table shows that $c_n > e_n \gg e_p > c_p \approx 0$, which means it is easier to capture and emit electrons than holes, and more likely to be occupied with electrons. The situation would be similar for hole traps in *p*-type material. Therefore, the concentration of occupied states is usually nearly the total trap concentration. In these situations, the majority carriers dominate the dynamic behaviour of the levels, which are termed majority traps. For an electron trap in *p*-type material, the electron capture process can be neglected (since $n \approx 0$). However, both electron and hole emission as well as hole capture may be involved in the exchange of carriers with both bands and the equilibrium occupancy. This is similar for a hole trap in *n*-type material. These traps are described as minority traps, with trap energy closer to the minority band edge.

2.4 Summary

In this chapter, the physical properties of semiconductors were presented, such as energy bands, Fermi levels, carrier transport, and defects in semiconductors. The properties of deep level defects in equilibrium as well as the capture and emission of carriers were also discussed.

Chapter 3

Semiconductor junctions

p-n junctions and Schottky diodes are commonly used semiconductor devices. Usually, a one-sided *p-n* junction, in which the doping on one side is about two orders of magnitude larger than the other, or a Schottky diode is preferred for DLTS measurements. The band diagram, current-voltage and capacitance-voltage characteristics of these two devices are discussed in this chapter. This discussion is based on Chapters 7-9 in Reference 1 and Chapters 2-3 in Reference 2.

3.1 *p-n* junctions

A *p-n* junction is a single-crystal material with one region doped with acceptor impurities and the adjacent region doped with donor atoms. The interface where the two regions meet is called the junction. The theory of *p-n* junctions is a foundation of semiconductor device physics. *p-n* junctions are of great importance both in understanding other more complicated semiconductor devices and for electronic applications. Depending on the doping profile, device geometry and other relevant factors, a *p-n* junction can perform various functions and is widely used.

Figure 3.1 shows the *p-n* junction schematically. When the impurity concentration in a semiconductor changes abruptly at the junction, an abrupt junction is obtained. For

simplicity, an abrupt *p-n* junction with constant equal doping concentrations N_d and N_a throughout the semiconductor is used as an example here.

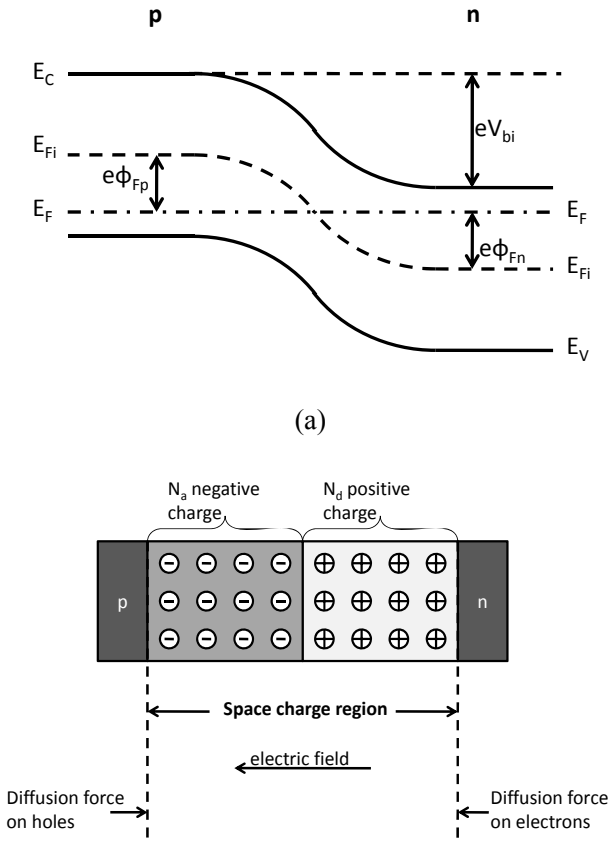


Figure 3.1 An abrupt *p-n* junction: (a) energy band diagram; E_C , E_V , E_{Fi} are conduction band energy, valence band energy and intrinsic Fermi level of the semiconductor, respectively. ϕ_n and ϕ_p are the potential difference between Fermi level and intrinsic Fermi level in *n*- and *p*-side, respectively. V_{bi} is the built-in potential. x_n and x_p are the depletion width in each side of the junction; and (b) the space charge region. [Adapted from Fig. 7.2 and Fig. 7.3 in Ref. 1]

3.1.1 Depletion region

When putting two semiconductors of different types together, due to the carrier concentration gradient near the junction, electrons from *n*-type and holes from *p*-type materials will diffuse across the junction leaving positive donor ions on the *n*-side and negative acceptor ions on the *p*-side. This region with ionized donors and acceptors is called the "space charge region", as shown in Fig. 3.1 (b). The ions form a built-in electric field causing carriers to drift in the opposite direction to the diffusion direction until a steady state is reached. The space charge region is also called a "depletion region", since this region is depleted of free carriers. Outside the depletion region the material is neutral, the same as independent *n*- or *p*-doped semiconductors.

When a steady state is reached in the space charge region, the Fermi energy is the same on both sides of the junction. This leads to the bending of the conduction and valence bands and creates an electrical potential difference. This potential difference maintains the balance of majority carriers in one side with minority carriers in the other side, i.e., the balance of drift and diffusion. From the band diagram in Fig. 3.1(a), we see that a built-in barrier is established between the *n*- and *p*-region, with a barrier height

$$V_{bi} = \left|\phi_{Fn}\right| + \left|\phi_{Fp}\right| = \frac{kT}{e}\ln\left(\frac{N_a N_d}{n_i^2}\right) = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right), \tag{3.1}$$

where $V_T = \frac{kT}{e}$.

The built-in potential is created by the charges in the depletion region, with the relationship between electric field and charge density determined by Poisson's equation,

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon} = -\frac{dE(x)}{dx}, \tag{3.2}$$

where ϕ is the electric potential, E is the electric field, ρ is the charge density, and ε is the dielectric constant.

Solving Equation (3.2), assuming uniform doping, one can obtain the width of the depletion region on each side of the junction x_n and x_p. Therefore, the total width of the depletion region W, is

$$W = x_n + x_p = \left\{ \frac{2\varepsilon_s V_{bi}}{e} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2} . \tag{3.3}$$

The width of the space charge region is related to the doping concentration on both sides of the junction. For a one-sided *p*-*n* junction, in which the doping on one side is significantly higher than on the other side, the depletion region is almost all located on the lower doped side of the junction.

3.1.2 Capacitance-voltage characteristics

When a reverse-bias voltage is applied to the diode, the Fermi level on the *n*-side of the junction is lower than the Fermi level on the *p*-side. The applied electric field is in the same direction as the internal electric field, thus increasing the total potential barrier. Almost all the reverse voltage is applied across the space charge region, since the electric field in the neutral *p*- and *n*-regions is essentially zero.

$$V_{total} = V_R + V_{bi} . \tag{3.4}$$

Figure 3.2 shows a *p*-*n* junction diode with a reverse-bias voltage V_R.

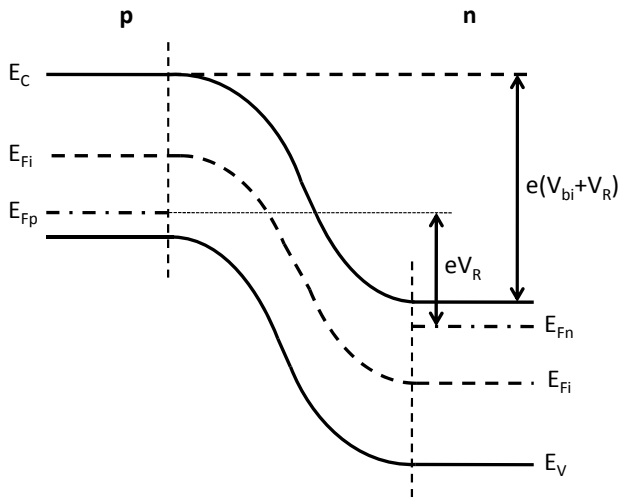


Figure 3.2 Energy band diagram of a *p-n* junction under reverse bias V_R, where E_{Fn} and E_{Fp} are Fermi levels of the *n*-type and *p*-type semiconductor, respectively. [Adapted from Fig. 8.1(b) in Ref. 1]

The edges of the depletion region extend farther into the semiconductor with increasing reverse bias. Substituting for V_{bi} in Equation (3.3) with V_{total}, the total space charge width is

$$W = \left\{ \frac{2\varepsilon(V_{bi} + V_R)}{e} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2} . \tag{3.5}$$

The junction capacitance per unit area is defined as

$$C' = \frac{dQ'}{dV_R} , \tag{3.6}$$

where $dQ' = eN_d dx_n = eN_a dx_p$.

Thus, $C' = \frac{dQ'}{dV_R} = \frac{eN_d dx_n}{dV_R} = \left\{ \frac{e\varepsilon N_a N_d}{2(V_{bi} + V_R)(N_a + N_d)} \right\}^{1/2} .$ (3.7)

The junction capacitance is related to the materials and diode properties: ε (the dielectric constant of the material), V_{bi} (the difference of intrinsic Fermi levels), N_a, N_d, (the *p*-type and *n*-type doping concentrations) and the applied voltage. If Equation (3.7) is compared to Equation (3.5), the junction capacitance per unit area can be rewritten as

$$C' = \frac{\varepsilon}{W}, \tag{3.8}$$

which is the same as for a parallel plate capacitor. C-V measurements are a standard method of determining the built-in potential and, for a one-sided abrupt *p*-*n* junction, the doping concentration on the lightly-doped side of the junction [1].

3.1.3 Current-voltage characteristics

The total current in the *p*-*n* junction consists of two parts. One is the ideal diffusion current, and the other is generation-recombination current. In general, for a large forward-bias voltage, the diffusion current dominates, while the recombination dominates for a low forward-bias voltage.

3.1.3.1 Diffusion current

At zero-bias, carriers on the *p*- and *n*-sides of the junction are in equilibrium. The drift and diffusion currents are equal. When a forward voltage V_a is applied across the junction, V_a is almost all dropped across the depletion region, since the resistance of this region is much larger than of the neutral *p*- and *n*-doped semiconductors. The forward bias V_a is in the opposite direction to the built-in potential and reduces the electric field, causing the barrier height to be decreased to $e\left(V_{bi} - V_a\right)$, as shown in Fig. 3.3. Also, the amount of space charge decreases as the width of depletion region becomes narrower. The drift current related to the electric field in the depletion region is reduced. Hence, a net diffusion of carriers occurs, with electrons diffusing from the *n*-side to the *p*-side, and holes from the *p*-side to the *n*-side, thus generating excess carriers on both sides of the deletion region. This process is called minority

carrier injection because the carriers injected are both minority carriers in the region they go into. These excess carriers diffuse across the junction, and the material returns to equilibrium after several diffusion lengths.

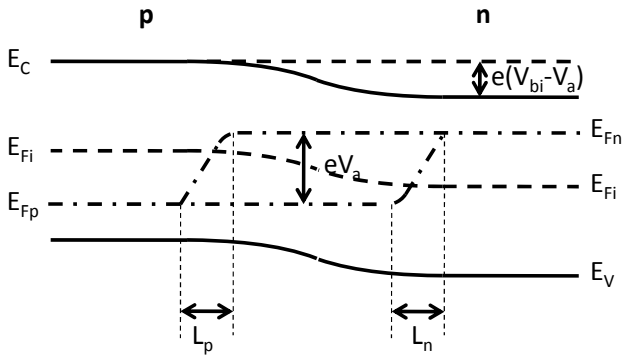


Figure 3.3 Depletion region of a *p*-*n* junction at forward bias V_a, where E_{Fn} and E_{Fp} are Fermi level of the *n*-type and *p*-type semiconductor, respectively. L_n and L_p are diffusion length of minority carriers in each side of the junction. [Adapted from Fig. 8.3(b) in Ref. 1]

The ideal diffusion current density for a *p*-*n* junction, including both the flow of majority and minority carriers, is given by

$$J_d = J_s\left[\exp\left(\frac{eV_a}{kT}\right)-1\right], \tag{3.9}$$

where J_s is the diode reverse saturation current,

$$J_s = \frac{eD_p p_{n0}}{L_p}+\frac{eD_n n_{p0}}{L_n}. \tag{3.10}$$

3.1.3.2 Generation-recombination current

In a real *p*-*n* junction generation and recombination of carriers may occur. With forward applied bias, electrons and holes are injected into the space charge region and recombine resulting in a recombination current. There are several physical mechanisms of recombination. The common cause is defects in the crystal structure, which can create energy levels in the band gap and form effective recombination centers. Fig. 3.4 shows the band diagram of a *p*-*n* junction at forward bias when recombination happens.

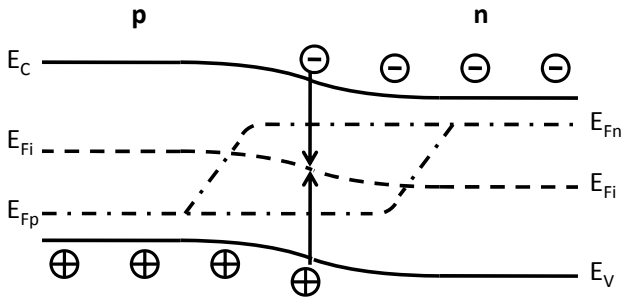


Figure 3.4 Electron-hole pair recombination in depletion region of a *p*-*n* junction under forward bias [1]. E_{Fn} and E_{Fp} are Fermi level of the *n*-type and *p*-type semiconductor, respectively. [Adapted from Fig. 8.18 in Ref. 1]

The recombination rate of the excess carriers in the depletion region is described by SRH theory [1, 2], as

$$|R| = \frac{np - n_i^2}{\tau_p (n + n') + \tau_n (p + p')}, \tag{3.11}$$

where n and p are carrier concentrations, n' and p' are excess carrier concentrations, n_i is the intrinsic carrier concentration, and τ_n and τ_p are the lifetimes of electrons and holes. The recombination current density can be written as

$$J_{rec} = \int_0^W e|R|\,dx = \frac{eWn_i}{2\tau_0}\exp\left(\frac{eV_a}{2kT}\right) = J_{r0}\exp\left(\frac{eV_a}{2kT}\right), \tag{3.12}$$

and $J_{r0} = \dfrac{eWn_i}{2\tau_0}$, where τ_0 is the excess minority carrier lifetime. So, the total current density in forward bias is

$$J_{total} = J_d + J_{rec} = J_s\left(\exp\left(\frac{eV_a}{kT}\right) - 1\right) + J_{r0}\exp\left(\frac{eV_a}{2kT}\right), \tag{3.13}$$

In general, the total forward current density in a *p*-*n* junction diode is written as

$$J = J_s\left[\exp\left(\frac{eV_a}{nkT}\right) - 1\right],\ 1 < n < 2\,. \tag{3.14}$$

with $n = 1$ at high forward bias when the drift current dominates and $n = 2$ at low bias when the recombination current dominates.

Similarly, in reverse bias, the concentration of carriers in the depletion region is nearly zero. When an electron-hole pair is generated, carriers will be pulled apart to the *p*- or *n*-side of the junction, forming generation current in the junction that is also a part of the current in reverse bias, as shown in Fig. 3.5. The generation current density can be written as

$$J_{gen} = \int_0^W e|G|\,dx = \int_0^W e\frac{n_i}{\tau_n + \tau_p}\,dx = \frac{eWn_i}{2\tau_0} = J_{r0}\,, \tag{3.15}$$

where G is the generation rate. This process is shown in Fig. 3.5. The total current density in reverse bias is

$$J_{total} = J_d + J_{gen} = J_s + J_{r0}\,. \tag{3.16}$$

The reverse current is dominated by the generation current at room temperature for *p*-*n* junctions, in general.

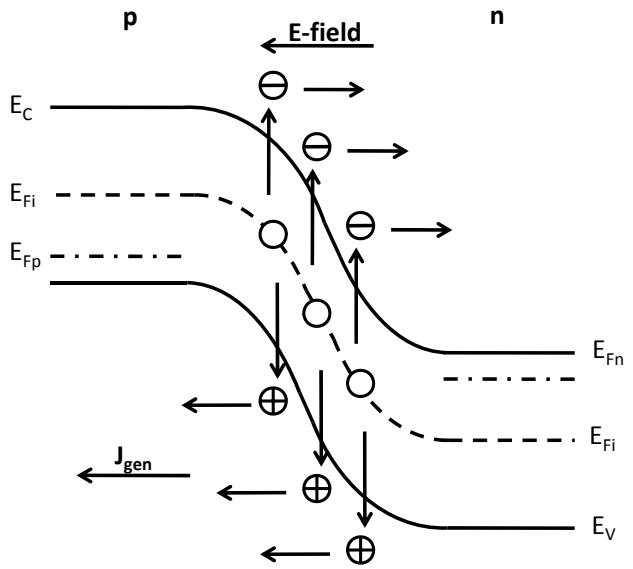


Figure 3.5 Electron-hole pair generation in the depletion region of a *p*-*n* junction under reverse bias. E_{Fn} and E_{Fp} are the quasi-Fermi level of the *n*-type and *p*-type semiconductors, respectively. J_{gen} is the generation current. [Adapted from Fig. 8.17 in Ref. 1]

A Schottky diode consists of a metal-semiconductor junction instead of a junction of two semiconductors with different doping types or concentrations. If the device is made with an *n*-type semiconductor, only electrons play a significant role in normal operation of the device. So the Schottky diode is called "majority carrier" device, and there is no recombination of *n*- and *p*-type carriers. Figure 3.6 is an energy band diagram of an *n*-type Schottky diode.

When a metal makes contact with a semiconductor, they share the same vacuum level, which are the energy levels of free electrons that escape from the metal or the semiconductor. We assume that the work function, which is the energy difference between the Fermi level and the vacuum level, of the metal is higher than that of the semiconductor. Thus, before equilibrium, the Fermi level of the semiconductor is higher than the metal, causing electron to flow into the metal side, lowering the potential of the metal and increasing that of the

semiconductor. Similar to a one-sided abrupt *p*-*n* junction, the bending of the semiconductor bands close to the junction creates a depletion or space charge region in the semiconductor at equilibrium.

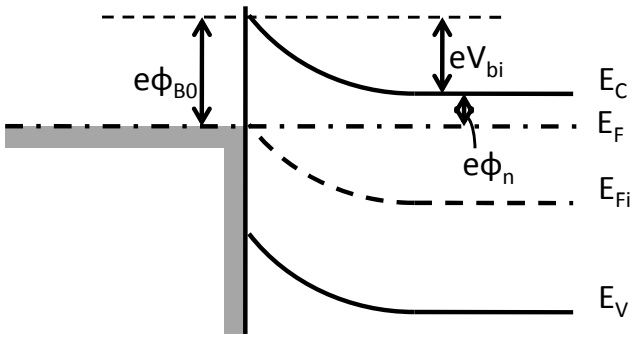


Figure 3.6 Energy band diagram of an *n*-type Schottky diode, where E_C, E_V, E_{Fi} are the conduction band energy, valence band energy and intrinsic Fermi level of the *n*-type semiconductor, respectively, ϕ_{B0} is the ideal barrier height in the metal side, and V_{bi} is the built-in potential in the semiconductor side. [Adapted from Fig. 9.1(b) in Ref. 1]

3.2.1 C-V characteristics

For a uniformly doped *n*-type Schottky diode, as well as a one-sided *p*-*n* junction with $N_a \to \infty$ and $x_p \to 0$, the depletion region is all in the *n*-type semiconductor. From Equation (3.3), the space charge width of a Schottky diode reduces to

$$W \approx \left\{ \frac{2\varepsilon(V_{bi} + V_R)}{eN_d} \right\}^{1/2}, \tag{3.17}$$

and the capacitance can be written as

$$C' \approx \left\{ \frac{e\varepsilon N_d}{2(V_{bi} + V_R)} \right\}^{1/2}. \tag{3.18}$$

Equation (3.18) may be manipulated to give

$$\left(\frac{1}{C'} \right)^2 = \frac{2(V_{bi} + V_R)}{e\varepsilon N_d}, \tag{3.19}$$

which shows that the inverse capacitance squared is linear with applied reverse voltage. The slope is related to the doping concentration and the built-in potential can be calculated with the horizontal intercept. As shown in Fig. 3.6, the Schottky barrier height is slightly larger than the built-in potential,

$$\phi_{B0} = V_{bi} + \phi_n, \tag{3.20}$$

where ϕ_{B0} is the energy difference between the conduction band and the Fermi level in the semiconductor, which depends on the doping level.

Therefore, the doping concentration on the lightly doped side of one-sided abrupt *p-n* junction diodes can be obtained by measuring the capacitance-voltage profile, as can the doping on the semiconductor side of Schottky barrier diodes.

3.2.2 I-V characteristics

The current transport in a metal-semiconductor junction is mainly due to majority carriers, and is determined by the barrier height. Electrons in the semiconductor that have energy higher than the built-in potential can flow into the metal, while electrons in the metal side which have higher energy than the barrier can pass over the barrier and reach the semiconductor. This process is described by thermionic emission theory. The net current density is defined by the net electron flux.

For Schottky diodes, the total current expression is

$$I = I_s\left[\exp\left(\frac{eV_a}{kT}\right)-1\right], \tag{3.21}$$

and the reverse saturation current $I_s = AA^*T^2\exp\left(\frac{-e\phi_{Bn}}{kT}\right)$, with A the diode area, A^* the effective Richardson constant and ϕ_{Bn} the barrier height.

Although the ideal current-voltage relationship of the Schottky diode is of the same form as that of the *p-n* junction, the magnitudes of the saturation current are different from each other. The form of the two saturation currents comes from different current mechanisms. The saturation current of a *p-n* junction is determined by the diffusion of minority carriers, while the reverse current in a Schottky barrier is from the thermionic emission of majority carriers over a potential barrier.

The generation current of a Schottky diode in reverse bias is similar to that of a *p-n* junction. As discussed in section 3.1.3.2, the dominant current in reverse bias for a *p-n* junction is the generation current at room temperature. In general, the reverse current of a Schottky barrier is several orders of magnitude higher than that of a *p-n* junction. This shows that the generation current of a Schottky diode is much lower than the reverse saturation current, and can be neglected.

3.3 Summary

To summarize, the band structure, current-voltage and capacitance-voltage characteristics of two devices, *p-n* junctions and Schottky barrier diodes, were presented. The Schottky barrier diodes are what we measured with DLTS. The other device we measured, the *p-i-n* diode, has a more complicated structure. The DC characteristics of *p-i-n* diodes will be interpreted by analogy with those of *p-n* junctions.

Chapter 4

Deep level transient spectroscopy (DLTS)

In order to study electronic states deep in the semiconductor band gap, a technique which monitors the capacitance of a semiconductor diode was employed. In 1974 Lang developed deep level transient spectroscopy (DLTS) to characterize deep levels in semiconductors [5]. The DLTS technique is used to study an energy level in the band gap in the space charge region of a Schottky barrier or a *p-n* junction by observing the transient capacitance from an initial state when the trap levels are occupied to the steady state when they are empty. To study majority carrier traps, either a Schottky diode or a one-sided abrupt *p-n* junction is preferred. A *p-n* junction or illumination is needed to detect minority carrier traps. The description of the capacitance transient is based on Chapter 7 in Reference 4. The discussion of the DLTS technique is based on References 5-8. For simplicity, I will describe the technique using an *n*-type Schottky diode as an example.

4.1 Capacitance transient

As shown in Fig. 4.1(a), in the absence of an applied bias voltage, deep level states in neutral *n*-type material are occupied by electrons since the trap energy level is below the Fermi level.

When a reverse bias V_R is applied to the diode, the depletion width is increased from $W(0)$ to $W(V_R)$ from the surface, as shown in Fig. 4.1(b).

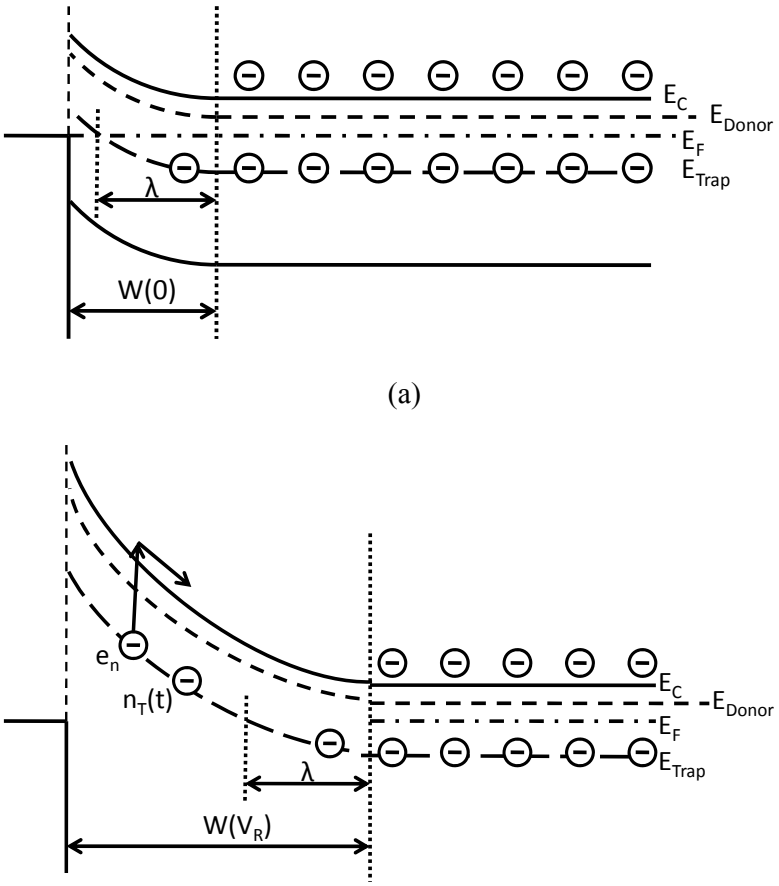


Figure 4.1 Conduction band diagram: (a) at zero bias; (b) at reverse bias V_R. The arrows show that electrons are emitted from the trap level to the conduction band and then swept out of the depletion region. [Adapted from Fig. 7.5 in Ref. 4]

From Equation (3.8), the increased depletion width when a reverse bias voltage is applied results in a decrease in the diode capacitance. Free electrons are swept out of the depletion region and, as the value of n in the region between $W(V_R)$ and $W(0)$ becomes zero, the capture rate decreases as well and the traps empty by thermal emission of the electron to the semiconductor conduction band. The emitted electrons are swept out of the depletion region by the electric field, causing an increase in capacitance. When the reverse bias voltage is removed, the empty traps are filled by electrons again. Because of the bending of the energy bands near the Schottky interface, the region of trap occupacy near the interface varies as the difference between the trap energy and the Fermi level. In Fig. 4.1, the transition distance λ representing the difference between the width of the depletion region and the width of the region where the traps are unoccupied, i.e. where the trap energy is above the Fermi level, is given by

$$\lambda = \left\{ \frac{2\varepsilon}{e^2 N_d} \left(E_F - E_T \right) \right\}^{1/2}. \tag{4.1}$$

During the emission process, the net space charge density is

$$\rho(t) = e\left(N_d + N_T - n_T(t) \right), \tag{4.2}$$

So from Equation (3.18), replacing the charge density eN_d by $\rho(t)$, the time-dependent capacitance immediately after a constant reverse bias voltage is applied is

$$C(t) = A\left\{ \frac{e\varepsilon\left(N_d + N_T - n_T(t) \right)}{2(V_{bi} + V_R)} \right\}^{1/2} = C(\infty)\left\{ 1 - \frac{n_T(t)}{N_d + N_T} \right\}^{1/2}, \tag{4.3}$$

where A is the diode area, and

$$C(\infty) = A\left\{ \frac{e\varepsilon\left(N_d + N_T \right)}{2(V_{bi} + V_R)} \right\}^{1/2}, \tag{4.4}$$

is the final steady state capacitance.

In the case of $N_T, n_T << N_d$, a Taylor expansion of $C(t)$ can be done and thus the change in capacitance can be written as

$$\frac{\Delta C(t)}{C(\infty)} = \frac{C(t) - C(\infty)}{C(\infty)} = -\frac{1}{2}\frac{n_T(t)}{N_d}. \tag{4.5}$$

From Fig. 4.1, we know that the states are always occupied in the region λ. The net space charge density is only changed in the region of $(W - \lambda)$. Taking this into consideration, Equation (4.5) is written as

$$\frac{\Delta C(t)}{C(\infty)} = \frac{C(t) - C(\infty)}{C(\infty)} = -\frac{1}{2}\left\{\frac{(W(V_R) - \lambda)^2 - (W(0) - \lambda)^2}{W^2(V_R)}\right\}\frac{n_T(t)}{N_d}, \tag{4.6}$$

From Equation (2.18), with $c_n, e_p, c_p \approx 0$, the transient response is

$$\frac{\Delta C(t)}{C(\infty)} = -\frac{1}{2}\left\{\frac{(W(V_R) - \lambda)^2 - (W(0) - \lambda)^2}{W^2(V_R)}\right\}\frac{N_T}{N_d}\exp(-e_n t). \tag{4.7}$$

The capacitance increases exponentially with time as carriers are emitted from the traps thermally.

4.2 Deep level transient spectroscopy

Deep Level Transient Spectroscopy (DLTS) is an experimental method for studying carrier traps in semiconductors. Deep level parameters such as the thermal emission activation energy and the capture cross section are obtained as well as trap concentrations. The DLTS technique has high sensitivity for trap concentrations, about 10^{-4} times the doping concentration of the semiconductor, typically as low as 10^{12} cm^{-3}.

4.2.1 DLTS Technique

Figure 4.2 shows how the capacitance transient is generated. When a reverse-bias voltage is applied across a Schottky diode, with depletion width W, the charge in the depletion region is contributed by both ionized impurities (shallow states) and deep level (defect) states. As discussed in the previous section, deep states are unoccupied by electrons within the region of $(W-\lambda)$.

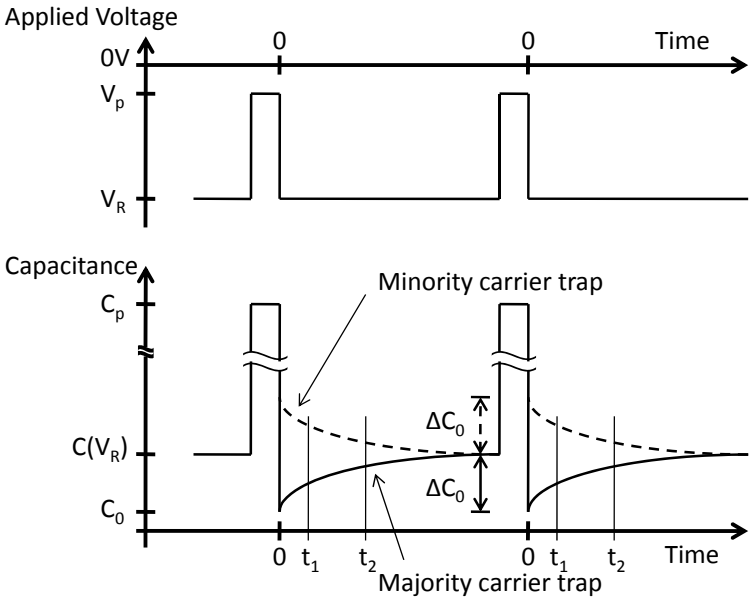


Figure 4.2 Applied voltage and corresponding capacitance transient. [Adapted from Fig. 4 in Ref. 5]

When a higher bias voltage pulse is applied, the depletion width decreases and there is a corresponding increase in the depletion capacitance. The deep states below the Fermi level are filled by electron capture during the pulse. After the pulse, when the voltage returns to reverse bias, electrons trapped in the deep level states partly counteract the positive charge in the shallow ionized donor states. The reverse bias sweeps out the free electrons and therefore

increases the width of the depletion region, and the capacitance decreases accordingly. As electrons are emitted from trap states, the width of depletion region become slightly smaller and the junction capacitance goes back to the previous steady state value.

From Equation (4.7), the capacitance transient can be written as

$$\Delta C(t) = \Delta C_0 e^{-e_n t}, \tag{4.8}$$

where $\Delta C_0 = \Delta C\left(t=0\right) = -\frac{1}{2}\left\{\frac{\left(W(V_R)-\lambda\right)^2 - \left(W\left(V_p\right)-\lambda\right)^2}{W^2\left(V_R\right)}\right\}\frac{N_T}{N_d}C\left(V_R\right)$ (4.9)

is the capacitance difference between $t=0$ and the steady state value when electron emission is completed, as shown in Fig 4.2, and V_p is the filling pulse voltage. Note that, since the carrier emission rate is an exponential function of the sample temperature and the trap energy, as shown in Equation (2.26), the capacitance transient is exponentially dependent on these two parameters as well.

The DLTS technique makes use of the temperature dependence of $e_n(T)$ and employs a "rate window" to determine the emission rate from the capacitance transient, which is described here as the double boxcar method [5].

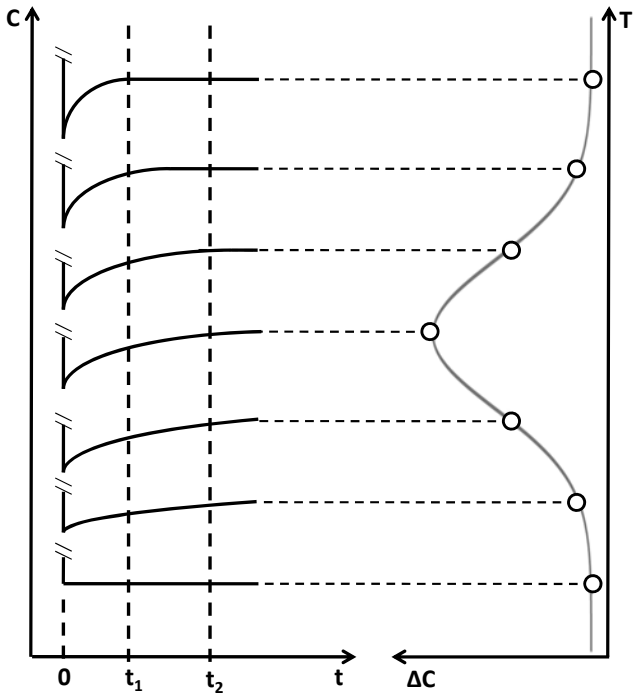


Figure 4.3 Capacitance transient and $S(T)$ vs. T . [Adapted from Fig. 6 in Ref. 5]

In a common DLTS system, the transient capacitance signal is sampled with two gates set at times t_1 and t_2 after the filling pulse and produces an output signal that is the difference between the two capacitance values. The output signal which is given by an exponential capacitance transient is

$$S(T) = C(t_2) - C(t_1) = g\Delta C_0 \left\{ \exp(-e_n t_1) - \exp(-e_n t_2) \right\}, \qquad (4.10)$$

where g is the calibration factor taking account of the gain of the system and $t = 0$ is at the beginning of the capacitance transient, i.e., at the end of the filling pulse. $S(T)$ varies as the emission rate e_n changes with temperature, as shown in Fig. 4.3.

In order to determine the maximum of $S(T)$, Equation (4.10) is differentiated with respect to τ ($\tau = 1/e_n$), and the maximum occurs when $\frac{dS(T)}{d\tau} = 0$. So, assuming $T = T_m$ at the peak output, the time constant is

$$\tau(T_m) = \tau_{ref} = \frac{t_2 - t_1}{\ln(t_2 / t_1)}, \tag{4.11}$$

and the emission rate is $e_n(T_m) = \frac{\ln(t_2 / t_1)}{t_2 - t_1}$, (4.12)

when $S(T)$ is a maximum.

The two sampling times t_1 and t_2 define an time constant τ_{ref}, which gives the emission rate window $\tau_{ref} = 1/e_n$ or $1/e_p$ of the instrument. When the emission rate of the trap is equal to the rate window of the instrument as the temperature is varied, the output is a maximum. The signal $S(T)$ versus temperature is called a DLTS spectrum. If there are several trap levels in the band gap, each has a maximum at a different temperature T_m for the same t_1 and t_2. Hence, there will be several peaks corresponding to different T_m in a single spectrum, easily showing the different trap states. For the same state, if a second rate window is chosen, the temperature of the maximum shifts. Therefore, we can choose a series of t_{1j}, t_{2j} ($j = 1, 2, 3\cdots$) to get a series of DLTS peaks, as shown in Figure 4.4. The T_{mj} are obtained from DLTS spectra, where the emission rate is known for each preset rate window.

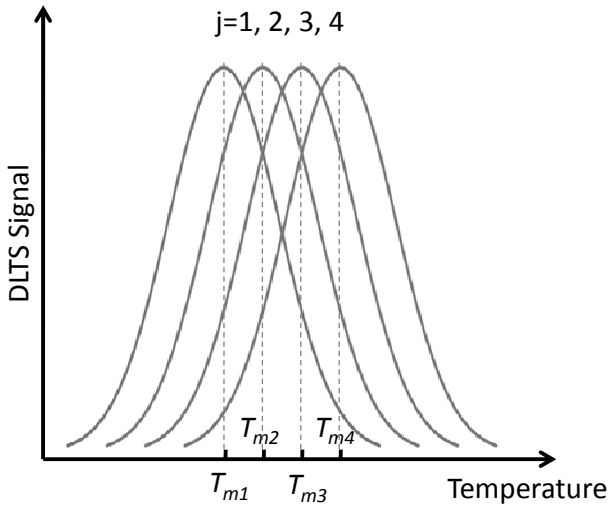


Figure 4.4.4 DLTS spectra taken with different "rate windows". [Adapted from Fig. 7 in Ref. 5]

4.2.2 Determination of the trap density and emission activation energy

The emission rate of carriers from a deep state in this case is described by Equations (2.26) and (2.27), although the system is not in equilibrium.

For electron traps in the p^+-n junction,

$$e_n(T) = \sigma_n \langle v_n \rangle \frac{g_0}{g_1} N_C \exp\left(-\frac{E_A}{kT}\right), \tag{4.13}$$

where the activation energy E_A, a main parameter to describe a deep level, is defined as

$E_A = E_C - E_T$, or $E_A = E_T - E_V$ for holes.

We have

$$\langle v_n \rangle = \left(\frac{3kT}{m_e^*}\right)^{\frac{1}{2}}, \tag{4.14}$$

where m_e^* is the effective mass of electrons, and

$$N_C = 2M_C\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}}, \tag{4.15}$$

where M_C is the number of conduction band minima.

Therefore, $e_n(T) = \gamma T^2 \sigma_n \exp\left(-\frac{E_A}{kT}\right)$, (4.16)

and $\gamma = 2\sqrt{3}M_C(2\pi)^{\frac{3}{2}} k^2 m_e^* h^{-3} g_0/g_1$ is a constant.

Rearranging Equation (4.16) we find that $\ln\frac{e_n}{T^2}$ versus $\frac{1}{T}$ should be linear.

$$\ln\frac{e_n}{T^2} = \ln\gamma\sigma_n - \frac{E_A}{k}\frac{1}{T}, \tag{4.17}$$

with the slope proportional to E_A and the intercept related to σ_n. Hence, the activation energy and capture cross section of a deep level can be determined from an Arrhenius plot, which is often known as the signature of the deep level.

From Equation (4.10), the peak height of DLTS signals is proportional to ΔC_0. A dimensionless parameter β is defined as

$$t_2 = \beta t_1, \tag{4.18}$$

then when the DLTS signal is at peak value, Equation (4.10) is written as

$$S(T_m) = g\Delta C_0\left\{\exp\left(-\frac{\ln\beta}{\beta-1}\right) - \exp\left(-\frac{\beta\ln\beta}{\beta-1}\right)\right\}. \tag{4.19}$$

Substituting Equation (4.19) into (4.7),

$$\frac{S(T_m)}{C(V_R)} \propto \frac{\Delta C_0}{C(V_R)} = -\frac{1}{2}\frac{N_T}{N_d}\left\{\frac{(W(V_R)-\lambda)^2 - (W(V_p)-\lambda)^2}{W^2(V_R)}\right\}, \qquad (4.20)$$

when $N_T << N_d$, and the interval between two filling pulses are long enough for carriers that are trapped to fully emit. Thus the mean trap concentration of the trap levels in the depletion region is obtained.

4.3 SULA deep level spectrometer

A block diagram of the SULA Technologies Deep Level Spectrometer is shown in Fig. 4.5. The capacitance meter employs a 1 MHz test signal. It can tolerate a maximum forward current of 30 mA during the filling pulse, and requires a reverse leakage current of <100 μA to give an accurate value of the capacitance.

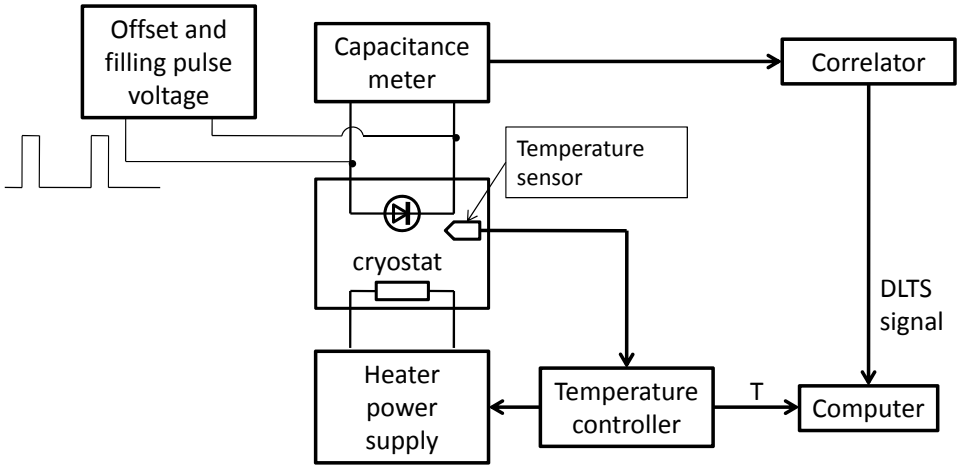


Figure 4.5 Block diagram of the SULA DLTS system. [9]

The sample is placed in a liquid nitrogen cryostat and can be scanned in the range of 78 K to 500 K. The sample temperature is measured and controlled by a Lakeshore Model

331 temperature controller. An "initial delay" (ID), which is the time between the back edge of the filling pulse and the starting point of the first sampling time, is set on the instrument and the two sampling times are $t_1 = 2.8ID$ and $t_2 = 7.0ID$ (Figure 4.6).

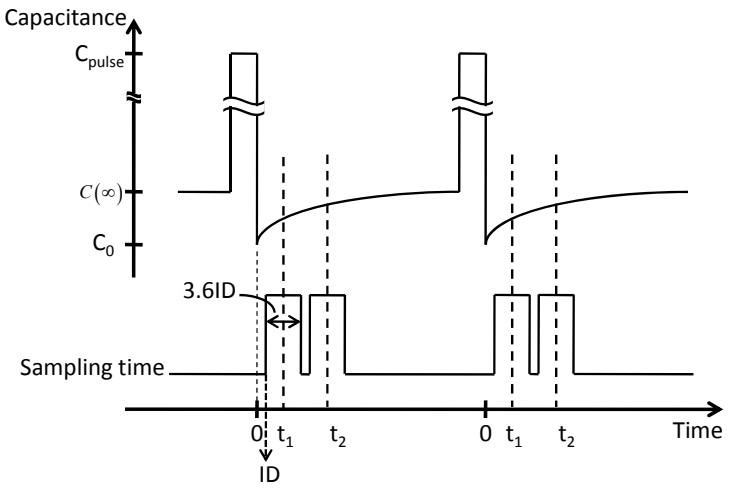


Figure 4.6 Initial delay and sampling time in SULA system. [9]

From Equation (4.18), $\beta = 2.5$. The reference time constant $\tau_{ref} = 4.3ID$. [9]

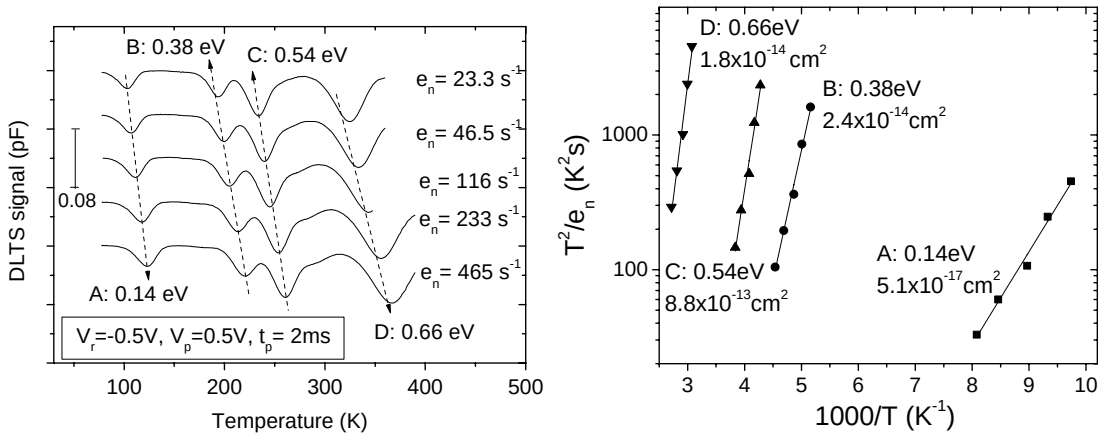
Therefore, for our system,

$$\frac{S(T_m)}{C(V_R)} = -\frac{1}{6}\frac{N_T}{N_d}\left\{\frac{(W(V_R)-\lambda)^2 - (W(V_p)-\lambda)^2}{W^2(V_R)}\right\}, \tag{4.21}$$

and the trap concentration is

$$N_T = 6N_d\left|\frac{S(T_m)}{C(V_R)}\right|\left\{\frac{W^2(V_R)}{(W(V_R)-\lambda)^2 - (W(V_p)-\lambda)^2}\right\}. \tag{4.22}$$

Figure 4.7 shows an example of the DLTS spectra and the Arrhenius plots of an *n*-type GaAs Schottky sample grown at 390 ºC [10]. Here, majority carrier traps are plotted as negative peaks. The spectra show four electron traps having activation energies of 0.14 eV, 0.38 eV, 0.54 eV, and 0.66 eV, respectively.



(a) (b)

Figure 4.7 (a) DLTS spectra of five different rate windows, with all measurement parameters shown in the plot. The signals are offset for clarity; (b) Arrhenius plot of the spectra, with the activation energy and capture cross section shown for each trap.

4.4 Summary

The DLTS technique was introduced in this chapter, as well as the equipment we used for the experiments. In addition, the method to calculate the activation energy, capture cross section and the trap concentration from DLTS spectra was presented. Basically, this is the standard way by which we obtain the results that are presented in Chapters 6-8.

Chapter 5

Properties of $GaAs_{1-x}Bi_x$ alloys

Great effort continues to be devoted to exploring novel semiconductor alloys in order to meet the growing demands of new technologies. Intensive studies have been done to understand the properties of III-V-N alloys [11-17]. Introducing bismuth, the heaviest element in group V, into III-V semiconductors was initially designed to compensate strain in III-V-N alloys [18]. Because of the semi-metallic character of III-Bi compounds, it is expected that III-V-Bi materials may lead to lower band gap alloys [18, 19].

5.1 Epitaxial growth of $GaAs_{1-x}Bi_x$

Bismuth was first incorporated into GaAs in 1998 using metal organic chemical vapour deposition (MOCVD) [20, 21], and quite recently was also successfully grown by molecular beam epitaxy (MBE) [22-27]. These publications show that introducing Bi to grow dilute $GaAs_{1-x}Bi_x$ induces a strong reduction of the band gap energy at a small bismuth fraction, and is therefore useful for many possible applications [18, 28].

It is very difficult to incorporate Bi into the GaAs lattice. To grow $GaAs_{1-x}Bi_x$ epi-layers requires a very low substrate temperature and much lower As_2 flux than the standard GaAs growth conditions [20, 22, 26]. The normal growth temperature for bismide incorporation is $< 400\ ^0C$, which results in a low surface mobility of atoms. The As/Ga flux ratio is 1:8 when

growing GaAs, while it is about 1:1 when growing bismide, which results in a Ga rich environment. Because of the low As pressure, Ga and Bi tend to form droplets on the surface of the epi-layers. An SEM image of a droplet is shown in Fig. 5.1. The Ga/Bi droplet has a diameter about 0.5-1 μm. These droplets may result in very rough surfaces that may cause problems for devices.

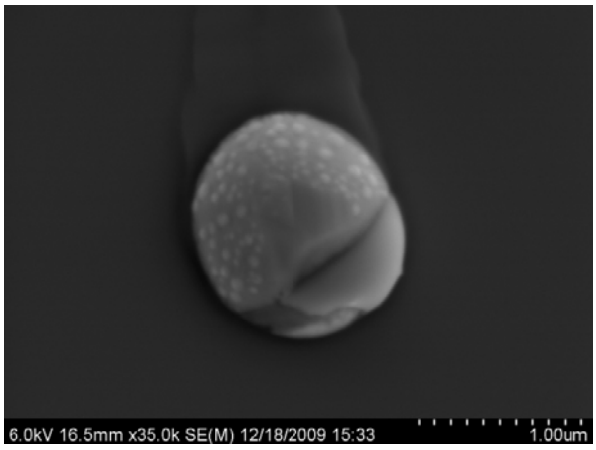
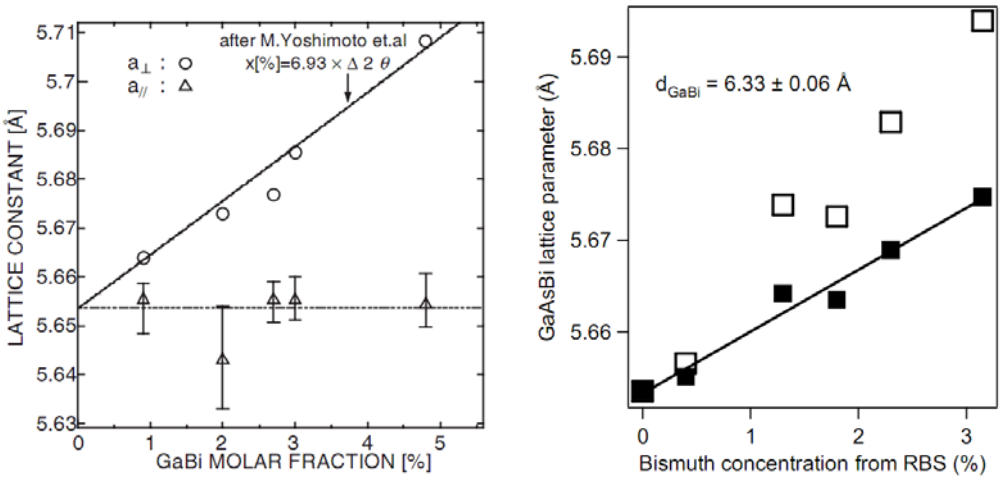


Figure 5.1 Droplet formed on the surface of $GaAs_{1-x}Bi_x$ epi-layer. Energy dispersive X-ray measurements show that this droplet is formed from both Ga and Bi. [29]

5.2 Lattice mismatch

Since the binary compound GaBi has not yet been synthesized, its crystal structure, lattice constant and band gap energy are still unknown [30]. A calculated value of the lattice constant of GaBi is 6.324 Å assuming a zinc-blende phase using the local-density approximation [18]. Hence, the lattice mismatch of GaBi with respect to GaAs would be about 12%. Due to the large size of the bismuth atom, it is important to investigate the lattice constant of dilute Bi in GaAs.

For MBE grown $GaAs_{1-x}Bi_x$ samples, the lattice parameter of dilute $GaAs_{1-x}Bi_x$ with $x < 5\%$ has been measured by x-ray diffraction (XRD), and the bismide composition was determined by Rutherford Backscattering Spectroscopy (RBS). It was found that the lattice parameter versus bismide composition is linear when $x < 5\%$ [22]. Fig. 5.2 gives the lattice constant of $GaAs_{1-x}Bi_x$ layers with bismide fraction below 5% layers on GaAs grown in two groups. In Fig. 5.2 (a), the in-plane and out-plane lattice constants of $GaAs_{1-x}Bi_x$ are given, indicating that the $GaAs_{1-x}Bi_x$ lay on GaAs is pseudomorphic [31, 32]. In Fig. 5.2 (b), the parameters for pseudomorphic GaAsBi films and free standing films by correcting the x-ray data for the tetragonal distortion using the elastic constants of GaAs are also given. Assuming that Vegard's law works for all x between 0 and 1, the estimated lattice constant for GaBi based on the data points in Fig. 5.2 (b) is 6.33 Å [22], consistent with the calculated value.

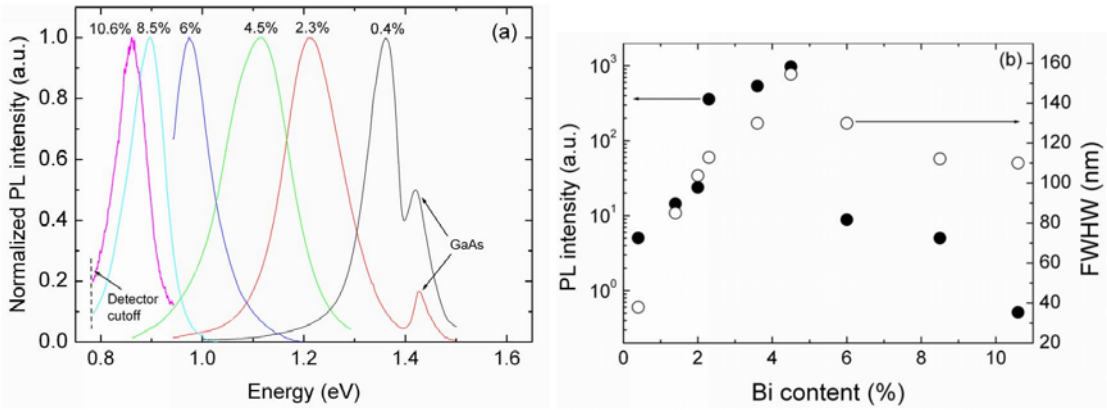


(a) (b)

Figure 5.2 (a) Lattice constant perpendicular and parallel to surface of $GaAs_{1-x}Bi_x$ epi-layers as a function of GaBi fraction [Fig. 3 in Ref. 32]. (b)Lattice parameter of the pseudomorphic (open square) and free standing (filled square) $GaAs_{1-x}Bi_x$ alloys as a function of the Bi concentration [Fig. 2 in Ref. 22]. The lattice parameters are from XRD measurements and the Bi concentrations are from RBS.

5.3 Band gap of $GaAs_{1-x}Bi_x$

Similar to N in GaAs, a small amount of Bi in GaAs reduces the band gap significantly, much more than introducing In or Sb with the same lattice mismatch strain [21, 33, 34]. The room temperature photoluminescence (PL) of $GaAs_{1-x}Bi_x$ samples with bismide composition from 0.4% to 10.6% is shown in Fig. 5.3 [25]. The PL peak shifts to lower energy with increasing bismide fraction. The PL intensity and FWHM both have a maximum value at ~4.5% bismide. The enhancement of PL intensity with increased bimide is quite unexpected [25]. Based on the PL measurements, the change in band gap of bismide is about -83 meV/%Bi as shown in Fig. 5.4, -88 meV/%Bi after the correction for the epitaxial strain [34].



(a) (b)

Figure 5.3 (a) Normalized PL spectra of $GaAs_{1-x}Bi_x$ samples showing the energy of the emitted light, and (b) the Bi concentration dependence of the PL intensity and FWHM. [Fig. 1 in Ref. 25]

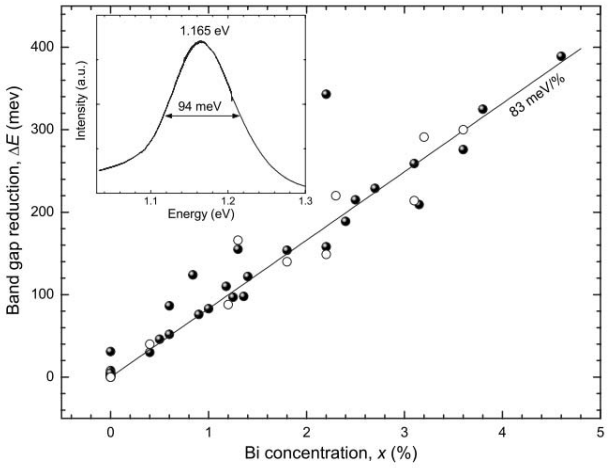


Figure 5.4 Band gap energy reduction of $GaAs_{1-x}Bi_x$ with respect to that of GaAs from room temperature photoluminescence and electroreflectance. The inset shows a 300 K PL spectrum for x = 2.3%. [Fig. 4 in Ref. 23]

Figure 5.5 shows the band gap energy variation with respect to lattice constant of III-V semiconductors and their alloys. Although less than the change of band gap at -200 meV/% for incorporating nitride into GaAs at low N concentration [11, 35], it is clearly shown in Fig. 5.5 that the effect of bismide on band gap reduction is much larger than for InGaAs or GaAsSb alloys with the same increase in lattice constant [22, 36, 37].

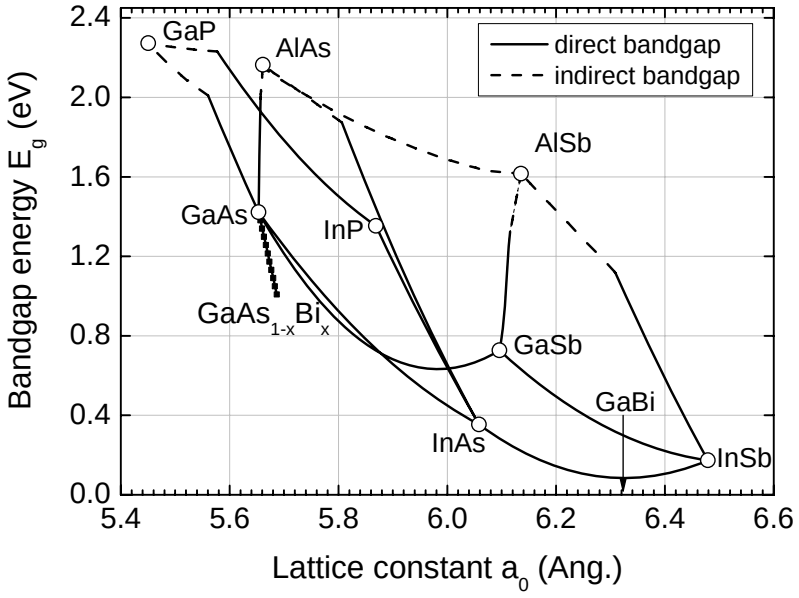


Figure 5.5 Lattice constant vs. band gap energy of various III-V semiconductors. The dotted line is for $GaAs_{1-x}Bi_x$. [The lattice constant of GaBi is from Ref.18; Data of GaAsBi alloy are from Ref. 22; and the data for the other III-V materials are based on Ref. 38]

The effect of the strain produced by growth of $GaAs_{1-x}Bi_x$ on a GaAs substrate is to split the light and heavy hole valence bands [34]. The temperature dependence of the band gap of dilute bismide reported is almost identical and the band gap reduction coefficient of the alloy is almost the same as GaAs [34]. The temperature sensitivity of the band gap of GaAsBi alloy shows a weak dependence with bismide fraction up to 3.1% [33, 34].

A mathematical expression has been established for the band gap energies as a function of the alloy composition of dilute bismide alloys [18, 25, 39]. Here the band gap energy for GaBi is -1.45 eV according to first principle calculations, assuming that the zinc-blende phase has the lowest energy [18, 30, 40]. For the ternary system of $GaAs_{1-x}Bi_x$ with $x < 13\%$, the relationship is

$$E_g = xE_{GaBi} + (1-x)E_{GaAs} - bx(1-x), \qquad (4.1)$$

where E_{GaAsBi}, E_{GaBi}, and E_{GaAs} are the band gap energies of $GaAs_{1-x}Bi_x$, GaBi, and GaAs, respectively. The bowing parameter $b(x) = \alpha/(1+\beta x)$ is dependent on Bi concentration [41], with $\alpha \approx 9.5$ and $\beta \approx 10.4$ [25].

Some theoretical studies of the electronic properties of dilute $GaAs_{1-x}Bi_x$ have been done [18, 30, 40]. The calculations agree well with the experimental results for the band gap reduction. They also show that the spin-orbit splitting is enhanced by incorporating Bi, due to the strong localization of the valence band states at Bi sites. In contrast to GaAsN, introducing Bi distorts the valence band energy instead of the conduction band [30, 42]. Two major theories are reported for the origin of the valence band maximum (VBM) in $GaAs_{1-x}Bi_x$ at this energy. One is that it is derived from a Bi bound state which is 180 meV above the VBM of GaAs [18], while the other idea is that it is derived from the VBM of GaAs, and Bi forms a resonant state below the VBM [23, 30, 43]. Based on experimental results recently, and also by consideration of the isolated Bi energy level in GaP [44] and InP [45], the latter explanation appears to be more realistic [23, 46]. A schematic drawing of the band structure of dilute GaAsN and GaAsBi is shown in Fig. 5.6.

Theoretically, for adding nitrogen into GaAs, only the electron mobility is impacted, since nitrogen modifies the conduction band; while on the other hand, only the hole mobility is expected to be changed for dilute bismide alloy because bismuth modifies the valence band [47]. The electron mobility of $GaAs_{1-x}Bi_x$ layers for x up to 2.5% was measured [48]. The degradation of electron mobility of $GaAs_{1-x}Bi_x$ with $x \leq 1.2\%$ is negligible. However, at higher Bi composition, $x \geq 1.6\%$, some degradation is observed. They attribute it to Bi segregation or non-optimal growth. Meanwhile, the hole mobility of $GaAs_{1-x}Bi_x$ layers was also measured. However, the reduction of hole mobility of $GaAs_{1-x}Bi_x$ is not as strong as that of the electron mobility in GaAsN [49].

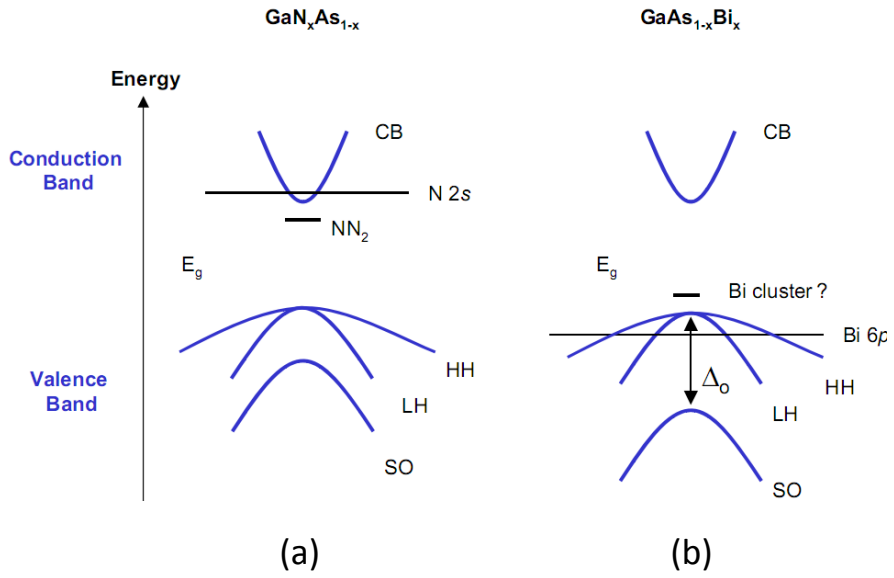
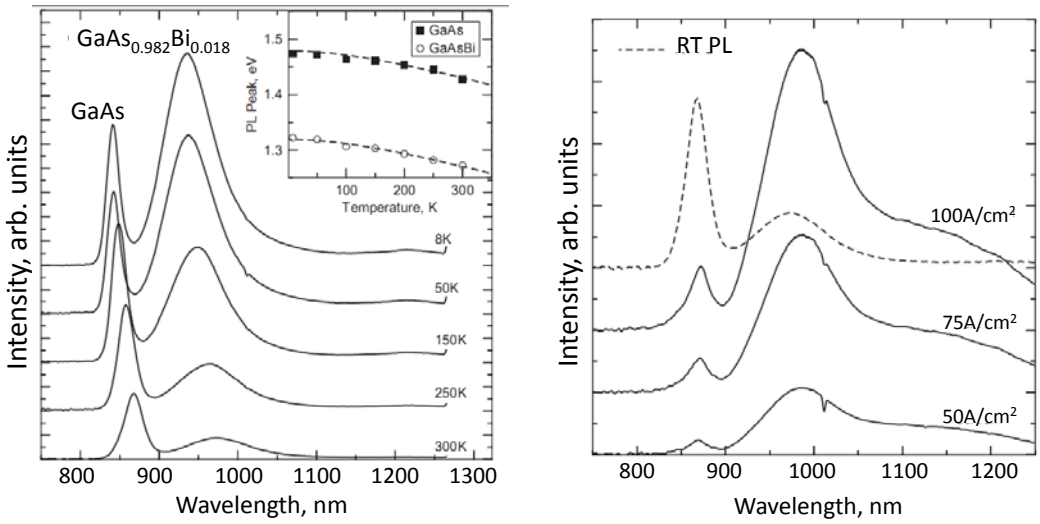


Figure 5.6 Schematic illustration of band structure of (a) GaNAs and (b) GaAsBi, showing conduction band (CB), heavy hole valence band (HH), light hole valence band (LH) and split-off band (SO). [Fig. 1 of Ref. 47]

5.4 Applications

Strong electroluminescence (EL) has been observed from $GaAs_{1-x}Bi_x$ *p-i-n* diodes with 1.8% [24] and 4.7% bismide [50]. These GaAsBi *p-i-n* diodes have a symmetric structure with *n*-type and *p*-type doped GaAs layers on each side of a 100nm-thick intrinsic region having a thin (~50 nm) $GaAs_{1-x}Bi_x$ quantum well located in the center. The doped *p*-type and *n*-type GaAs layers were both grown at standard temperature, about 550 ^{0}C. The growth temperature of all the three intrinsic layers is at low temperature, about 300 ^{0}C. The PL spectra of the sample with 1.8% bismide are shown in Fig. 5.7 (a), and the EL spectra in Fig. 5.7 (b) are from the same sample. The strong EL spectra indicate that the GaAsBi material may be useful for manufacturing light emitting diodes. Comparing this device with a similar *p-i-n* structure with 3x5 nm InGaAs quantum wells separated by 15 nm GaAs grown at 580 ^{o}C, the

EL intensity of the InGaAs *p-i-n* diode is about 100 times higher than that of the $GaAs_{0.082}Bi_{0.018}$ diode at the same injection current. It is known that having multiple quantum wells is more efficient for light emission. Therefore, it is expected that the *p-i-n* diodes with three similar $GaAs_{0.082}Bi_{0.018}$ quantum wells could have higher intensity than the present structure. On the other hand, defects in $GaAs_{1-x}Bi_x$ may be another reason for the lower EL intensity than the InGaAs layers [24].



(a) (b)

Figure 5.7 (a) PL spectra for a $GaAs_{1-x}Bi_x$ *p–i–n* structure with x = 1.8%. The inset shows the peak emission energies as a function of temperature for both the GaAs and $GaAs_{1-x}Bi_x$ peaks. (b) EL spectra for a $GaAs_{1-x}Bi_x$ *p-i-n* structure with x = 1.8% for various injection current densities at 300 K. Room temperature PL is shown for comparison. [Fig. 2 and Fig. 3 of Ref. 24].

Dilute bismide alloys have many potential applications. The observed electroluminescence and photoluminescence of $GaAs_{1-x}Bi_x$ shows that it is a candidate for solid state lasers [51] and high efficiency multi-junction solar cells [52-55]. Using dilute bismide as the base of a heterojunction bipolar transistor for its smaller band gap compared to

GaAs is expected to reduce power consumption [56, 57]. The strong spin-orbit splitting in the valence band makes the material useful for spintronics devices [58]. $GaAs_{1-x}Bi_x$ is also a promising material for THz optoelectronic devices [26]. In addition, co-doping of N and Bi in GaAs makes another potential alloy for 1 eV band gap material lattice matched to GaAs. The strains caused by N and Bi can compensate each other and can possibly improve the crystal quality. The strong band gap reduction of both dilute Bi and N can change the band gap with less N and Bi, which may improve the optical properties of the material [18].

5.5 Summary

$GaAs_{1-x}Bi_x$ alloys with bismide composition $x \leq 5\%$ show good optical properties. However, there are some concerns. Droplet formation caused by the low As/Ga ratio growth environment leads to poor surface morphology and may limit the layer thickness for applications of these alloys. The low T_g may result in low surface mobility of atoms during the growth and therefore high concentrations of defects may be present in the crystal. With all these factors, it is important to investigate the deep level defects in the $GaAs_{1-x}Bi_x$ alloy.

Chapter 6

DLTS on $GaAs_{1-x}Bi_x$ Schottky diodes

As discussed in Chapter 4, the preferred samples for DLTS measurements are Schottky diodes or one-sided abrupt *p*-*n* junctions. In these samples the location of the defects and whether they are electron or hole traps is clear, since the depletion region is located in a single layer and the majority carrier is known. To investigate deep level defects in $GaAs_{1-x}Bi_x$ layers, Schottky diodes were fabricated and tested with DLTS measurements.

The $GaAs_{1-x}Bi_x$ layers were grown on GaAs (001) substrates by molecular beam epitaxy (MBE) at the University of British Columbia (UBC) and University of Victoria by Professor T.Tiedje's group. The layer structure is shown in Fig. 6.1. A lightly *p*-doped epitaxial $GaAs_{1-x}Bi_x$ layer was grown at low temperature, about 380 ºC, on top of a thick heavily *p*-doped GaAs buffer layer grown at standard temperature, 550 ºC on a *p*-type GaAs substrate. These samples were characterized at UBC by x-ray diffraction (XRD) to determine the layer thickness and bismide fraction. Hall measurements of $GaAs_{1-x}Bi_x$ epi-layers on semi-insulating GaAs substrates were grown to calibrate the doping concentration and the growth rate before growing the DLTS samples. Metal contacts were deposited on top of the wafer through a metal shadow mask and also on the back side of the wafer as a blanket film at UBC. The top contact is a Schottky contact, and the bottom contact is a large area tunnel

barrier, which serves as an ohmic contact. The Schottky diodes were characterized by I-V and C-V measurements to confirm that the samples were suitable for DLTS measurements.

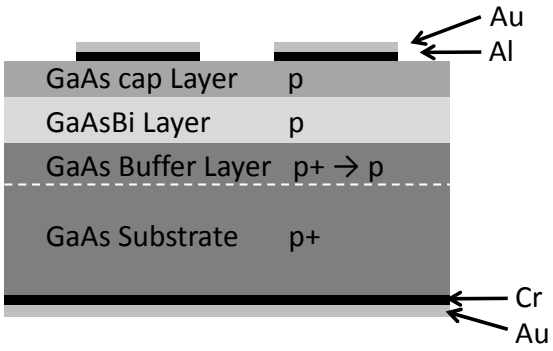


Figure 6.1 Schematic structure of the $GaAs_{1-x}Bi_x$ Schottky diodes.

Initially, Cr/Au Schottky contacts were used for *p*-type $GaAs_{1-x}Bi_x$ layers, and Cr/Au was also used in the back-side contact. Unfortunately, the I-V measurements showed that all $GaAs_{1-x}Bi_x$ samples had current at reverse voltages that is too large for DLTS measurements. Four different methods of surface processing were performed on the 3.4% Bi sample r2179 (sample r2179a to r2179d in Table 6.1), before metal contact deposition, in order to improve the I-V properties. However, none actually reduced the leakage current. The Schottky samples tested by I-V and C-V are listed in Table 6.1.

To reduce the reverse leakage current, the Schottky metal was changed to Al/Au for the most recent four samples [59]. The leakage current was reduced by about an order of magnitude with the new Schottky contacts. Adding a thin GaAs cap layer on top of the $GaAs_{1-x}Bi_x$ layer was also found to reduce the reverse leakage current, as can be seen in Table 6.2. Samples r2187 and r2206 with a GaAs cap layer and Al/Au contacts have a leakage current low enough to be measured with the SULA DLTS system, but the other two samples that do not have a GaAs cap layer are too leaky, even with Al/Au contacts.

Table 6.1 List of $GaAs_{1-x}Bi_x$ Schottky samples.

Sample #	Description	% Bi	Metal contact	GaAsBi layer thickness (nm)	Growth temperature (^{0}C)	Notes
r2165	p-GaAsBi	2.9	Cr/Au	300	390	
r2179a	p-GaAsBi	3.4	Cr/Au	430	380	
r2179b	p-GaAsBi	3.4	Cr/Au	430	380	
r2179c	p-GaAsBi	3.4	Cr/Au	430	380	
r2179d	p-GaAsBi	3.4	Cr/Au	430	380	
r2187	p-GaAsBi	4.1	Cr/Au	310	370	GaAs cap layer ~30nm
r2206	p-GaAsBi	3.0	Cr/Au	350	370	
r2165	p-GaAsBi	2.9	Al/Au	300	390	
r2179	p-GaAsBi	3.4	Al/Au	350	380	
r2187	p-GaAsBi	4.1	Al/Au	310	370	GaAs cap layer ~30nm
r2206	p-GaAsBi	3.0	Al/Au	350	370	GaAs cap layer~15nm

Table 6.2 Comparison of the built-in potential and leakage current of *p*-type $GaAs_{1-x}Bi_x$ Schottky samples having Al/Au and Cr/Au contacts.

Sample #	%Bi	GaAs cap layer (nm)	V_{bi} Al (V)	V_{bi} Cr/Au (V)	I @ -1V Al (μA)	I @ -1V Cr/Au (μA)
r2165	2.9	0	0.43	--	-280	-1×10^4
r2179	3.4	0	0.28	--	-2170	$> -2 \times 10^4$
r2187	4.1	30	0.97	0.62	-6.72	-81.6
r2206	3.0	15	0.23	0.31	-39.6	-2×10^3

6.1 DLTS measurements on *p*-type $GaAs_{1-x}Bi_x$

6.1.1 *p*-$GaAs_{1-x}Bi_x$ with 4.1% Bi

A *p*-type $GaAs_{1-x}Bi_x$ Schottky diode (r2187) with 4.1% Bi grown at 370 °C, with nominal $GaAs_{1-x}Bi_x$ layer thickness of 310 nm, and GaAs cap layer thickness of about 30 nm. I-V and

C-V results are summarized in Table 6.3. DLTS measurements were performed on two different diodes, and one majority carrier peak was detected. The DLTS spectra at an emission rate of 465 s^{-1} are shown in Fig. 6.2 for both diodes. Notice that the peak is very broad and the shape of it does not look like a typical DLTS peak for a single energy level. It was hard to fit the curve by multiple peaks because the signal is noisy and the total number of traps is unknown. Assuming the broad peak is a single trap, the trap concentration, activation energy and capture cross section are given in Table 6.4.

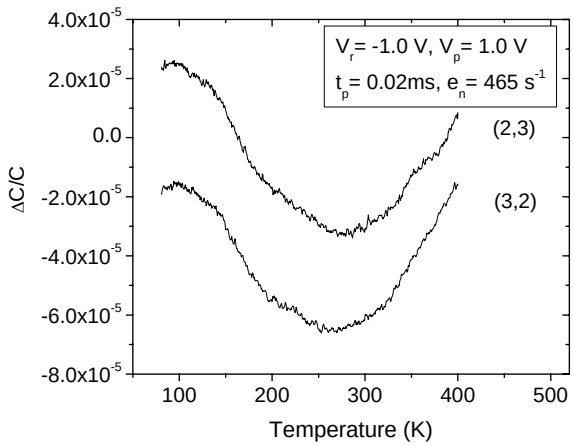


Figure 6.2 DLTS data taken from two different diodes on sample r2187, with all parameters shown on the graph. The signals are offset for clarity.

Table 6.3 Summary of results from I-V and C-V measurements of two diodes on 4.1% Bi sample. The built-in potential, the doping concentration, the leakage current at -1 V, and the depletion width at 0 V are given.

Diode	V_{bi} (V)	N_a (cm^{-3})	I @ -1V (μA)	W @ 0V (nm)
r2187-(2,3)	0.98	2.2×10^{17}	-2.70	78
r2187-(3,2)	1.01	2.0×10^{17}	-3.44	84

Table 6.4 Activation energy, capture cross section and trap concentration calculated assuming a single trap for both diodes.

Diode		r2187-(2,3)	r2187-(3,2)
Trap A	E_A (eV)	0.36 ± 0.02	0.36 ± 0.02
	σ (cm^2)	5.0 x10^{-18}	1.2 x10^{-17}
	N_T (cm^{-3})	4.6 x10^{14}	2.7 x10^{14}

6.1.2 *p*-$GaAs_{1-x}Bi_x$ with 3.0% Bi

A *p*-type $GaAs_{1-x}Bi_x$ Schottky diode (r2206) with 3.0 % Bi was grown at 370 °C, with a nominal $GaAs_{1-x}Bi_x$ layer thickness of 350 nm and a GaAs cap layer thickness of approximately 15 nm. I-V and C-V results are summarized in Table 6.5. DLTS measurements were performed on two different diodes on the chip with Cr/Au contacts and two other diodes on the second chip with Al/Au contacts. The DLTS spectra for an emission rate of 465 s^{-1} are shown in Fig. 6.3 for all four diodes.

Similar to the 4.1% bismide layer, one majority carrier peak was detected. Fitting the spectra with multiple peaks was not successful. The parameters of the traps are calculated assuming the signal of each diodes is a single peak. The Fermi level in this sample is about 0.11 eV above the valence band and normally traps this close to the Femi level would not be detected. The estimated trap concentration, activation energy and capture cross section are shown in Table 6.6, although the small activation energy and capture cross section numbers all seem unphysical.

Table 6.5 Summary of results on each diode in sample r2206. The built-in potential, doping concentration, leakage current at -1 V, depletion width at 0 V, and respective defect concentration are given. (Note – Al/Au contacts are a different chip than the Cr/Au contacts.)

Diode	V_{bi} (V)	N_a (cm^{-3})	I @ -1V (μA)	W @ 0V (nm)
r2206-Cr-(2,1)	0.33	1.3×10^{17}	-1.1×10^{3}	64
r2206-Cr-(3,2)	0.35	1.1×10^{17}	-1.0×10^{3}	70
r2206-Al-(2,3)	0.55	1.3×10^{17}	-8.52	75
r2206-Al-(3,4)	0.54	1.4×10^{17}	-37.2	73

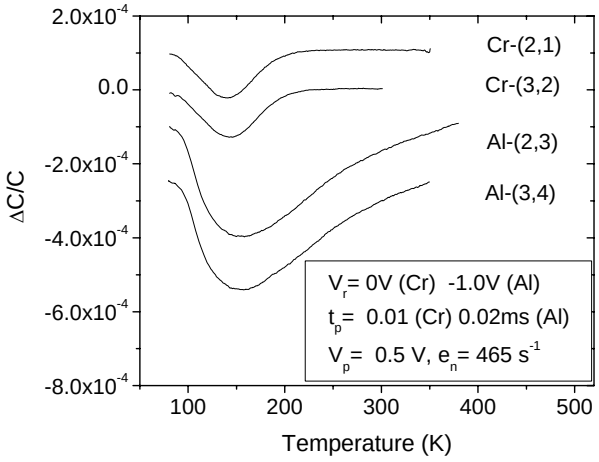


Figure 6.3 DLTS data taken from four different diodes on sample r2206, with all parameters shown on the graph. The signals are offset for clarity.

Table 6.6 Activation energy, capture cross section, and trap concentration calculated by assuming a single trap for all devices.

Diode		r2206-Cr-(2,1)	r2206-Cr-(3,2)	r2206-Al-(2,3)	r2206-Al-(3,4)
Trap A	E_A (eV)	0.12 ± 0.02	0.09 ± 0.05	0.15 ± 0.03	0.12 ± 0.02
	σ (cm^2)	7.1×10^{-20}	5.8×10^{-21}	3.3×10^{-19}	2.5×10^{-20}
	N_T (cm^{-3})	1.0×10^{14}	1.5×10^{14}	6.8×10^{14}	6.0×10^{14}

6.2 Surface morphology

Optical images (Fig. 6.4) of the $GaAs_{1-x}Bi_x$ layers show that these layers have very rough and pitted surfaces, presumably due to the formation of metal droplets on the surface during MBE growth at Ga/As ratios close to 1. Atomic force microscopy (AFM) of this sample shows that some of the pits are about 100 nm in depth (Fig. 6.5). Some other pits are about 230 nm deep, almost the same as the total $GaAs_{1-x}Bi_x$ layer thickness of the $GaA_{0.96}Bi_{0.04}$ layer (sample r2187). The actual depth of the pits could be even larger, if the AFM tip does not reach the bottom of the pit.

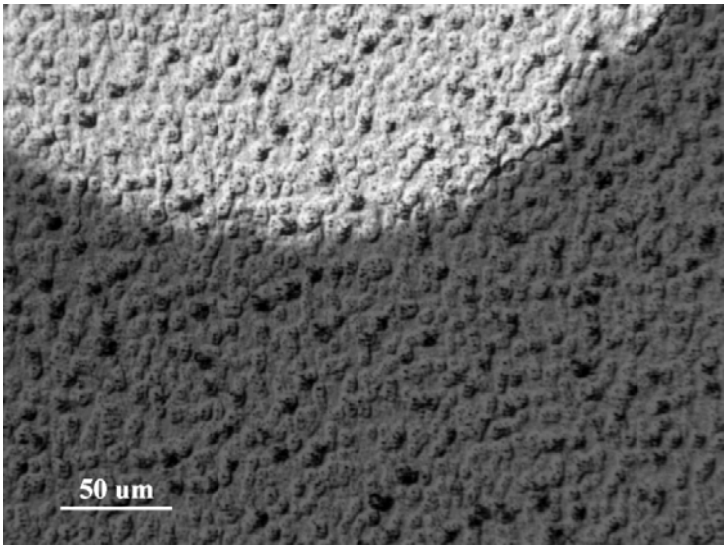
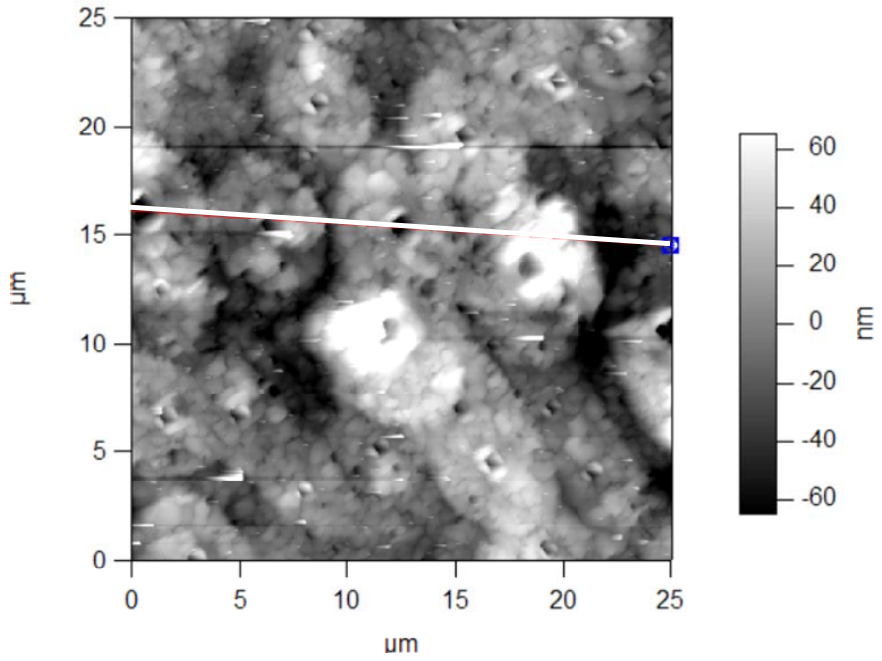
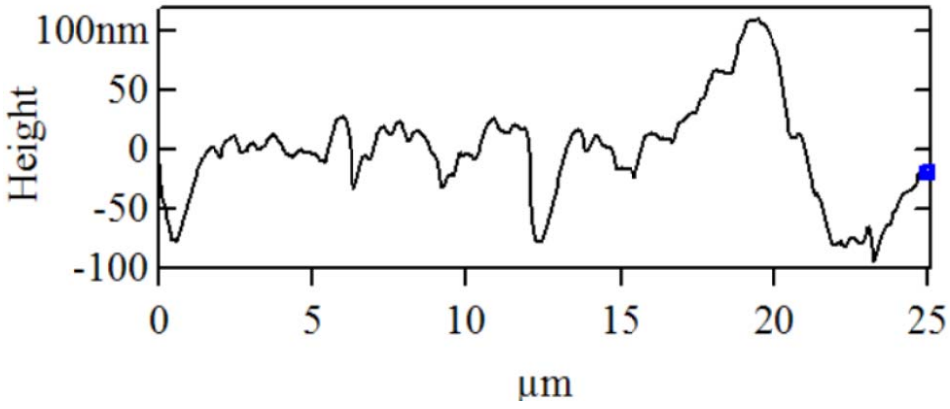


Figure 6.4 Optical image of the (001) surface of the *p*-$GaAs_{1-x}Bi_x$ sample with 4.1% Bi. The light area is the edge of the Schottky contact. The surface appears to be mounds with black centers.



(a)



(b)

Figure 6.5 AFM picture of $GaAs_{1-x}Bi_x$ sample r2187with 4.1% Bi: (a) surface shows many mounds with black pits in the center, similar to Fig. 6.4; (b) the height scanned along the white line in (a), shows that the pits are about 1 um wide and 100 nm deep. [60]

Because of these pits, the thickness of the epi-layer over the contact area is not uniform. Moreover, we do not even know if the metal is contacting the semiconductor everywhere within the area. The poor surface morphology probably causes the poor I-V characteristics and the unphysical DLTS signals. In this case, the calculated values of the activation energy and trap concentration are not reliable. However, carriers can move horizontally in the layer, so the mobility [49] as well as optical measurements [25] can be performed on similar $GaAs_{1-x}Bi_x$ layers.

Another interesting thing we noticed about these $GaAs_{1-x}Bi_x$ Schottky diodes is that measuring the I-V characteristics with the light on and off gives the same result. In contrast, other GaAs Schottky samples exhibit a photo response, behaving as solar cells, in which photons generate additional current in the devices. This may be another indication of the poor quality of these $GaAs_{1-x}Bi_x$ Schottky samples.

6.3 Summary

Unfortunately, little information about deep level defects could be obtained from the GaAsBi Schottky samples, because of the problem of droplet formation during epitaxial growth. However, the DLTS data does indicate the presence of traps in concentrations on the order of $5x10^{14}$ cm^{-3}.Therefore, in order to obtain better information about defects in $GaAs_{1-x}Bi_x$, it was decided to attempt DLTS measurements on the *p-i-n* structures that had been fabricated for measurements of $GaAs_{1-x}Bi_x$ electroluminescence. These *p-i-n* structures have a thin, nominally 50 nm, $GaAs_{1-x}Bi_x$ quantum well in the *i*-layer and droplet formation is believed to be much less severe when only a thin $GaAs_{1-x}Bi_x$ layer is grown.

Chapter 7

Deep level defects in GaAs

In chapter 6 it was shown that $GaAs_{1-x}Bi_x$ Schottky diodes are not suitable for DLTS measurements. Therefore, DLTS measurements were performed on the *p-i-n* diodes with a thin $GaAs_{1-x}Bi_x$ quantum well fabricated for EL and PL measurements, discussed briefly in chapter 5. These *p-i-n* diodes have a symmetric layer structure, consisting of two doped GaAs layers grown under standard conditions and two intrinsic GaAs layers grown at approximately 300 °C in addition to the $GaAs_{1-x}Bi_x$ quantum well. Therefore, the defects existing in the GaAs layers must be ruled out, if the traps in $GaAs_{1-x}Bi_x$ are to be determined. We needed to investigate the traps in both *n*-type and *p*-type GaAs grown at standard and low temperature as well as GaAs layers grown at lower temperature in order to try to distinguish the traps in GaAs from those in $GaAs_{1-x}Bi_x$. The structure of the GaAs Schottky diodes is shown in Fig. 7.1. Similar to the GaAsBi Schottky diodes, a lightly *n*- or *p*-doped GaAs layer was grown on top of an *n*- or *p*-type GaAs substrate, after a thick heavily *n*- or *p*-doped GaAs buffer layer. The contact to the top layer is a Schottky contact, and the contact to the heavily doped substrate, is a large area tunnel barrier, which serves as an ohmic contact.

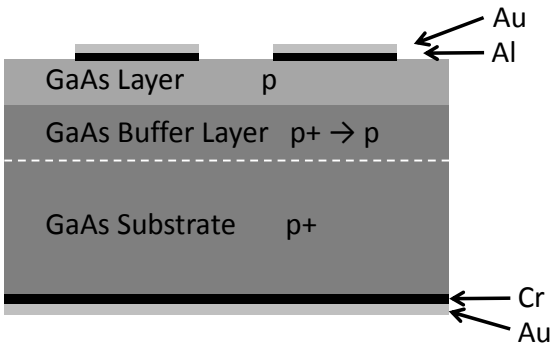


Figure 7.1 Diagram of the sample structure of a *p*-type GaAs Schottky diode. The structure for *n*-type samples is similar but with *n*-type doping.

Several GaAs Schottky diodes were measured some time ago by other group members, including *p*-type GaAs layers grown at 560 °C, 450 °C and 350 °C and *n*-type layers grown at 550 °C and 390 °C. Details are discussed in section 7.1. Several additional GaAs sample were fabricated more recently, including *n*-type and *p*-type layers grown at 310 °C, comparable to the growth temperature for the intrinsic layers in the *p*-*i*-*n* diodes. As well, an *n*-type sample was grown at standard conditions using solid Si as the dopant source for comparison with the previous *n*-type samples which were grown using $SiBr_4$ as the dopant source. The *p*-type dopant source was CBr_4.

7.1 Summary of previous DLTS results for GaAs

7.1.1 Hole traps in *p*-type GaAs layers

Table 7.1 shows the properties of the *p*-type GaAs Schottky samples measured previously. From the spectra in Fig. 7.2 and Table 7.2, we see that one hole trap is present in all the *p*-type samples, with an activation energy of 0.57 eV. The trap concentration is higher, about 2-5 $x10^{14}$ cm^{-3} in the samples grown at 550 °C, which is the standard growth

temperature, and at 450 ºC, but much lower, in the 2-5 x10^{12} cm^{-3} range in the samples grown at 350 ºC.

Table 7.1 Properties of the *p*-type GaAs Schottly diodes measured previously.

Sample #	Growth temperature (ºC)	N_a (cm^{-3})	V_{bi} (V)	I @ -1V (uA)	Metal Contact
r1729	560	5.5 x10^{16}	0.53	-1.75	Cr/Au
r1730	450	4.9 x10^{16}	0.44	-26	Cr/Au
r1838	350	1.8 x10^{16}	0.46	-45	Cr/Au
r1840	350	4.8 x10^{16}	0.44	-98	Cr/Au

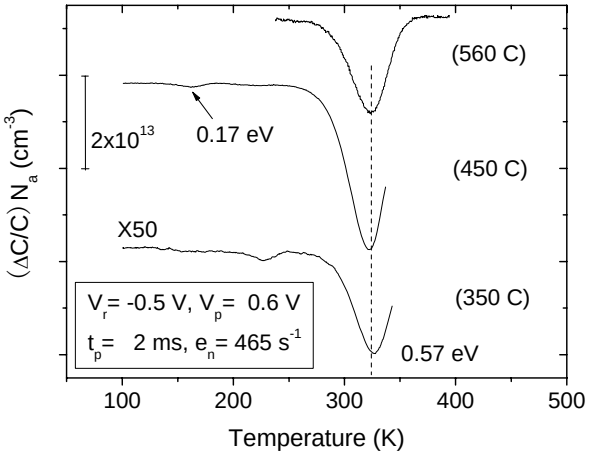


Figure 7.2 Comparision of DLTS spectra of the *p*-GaAs Schottky diode with different growth temperatures. The signals are offset for clarity.

Table 7.2 Hole traps found in the previously measured *p*-type GaAs Schottky diodes.

Sample #		r1729	r1730	r1838	r1840
T_g (°C)		560	450	350	350
E_A=0.17eV	N_T (cm^{-3})		3.2×10^{13}		
	σ (cm^2)				
E_A=0.57eV	N_T (cm^{-3})	2.2×10^{14}	5.4×10^{14}	4.5×10^{12}	2.1×10^{12}
	σ (cm^2)			3.7×10^{-16}	3.8×10^{-16}

7.1.2 Electron traps in *n*-type GaAs layers

Two *n*-type GaAs Schottky samples were also measured previously. The diode properties determined from I-V and C-V measurements are shown in Table 7.3, and the DLTS spectra are shown in Fig. 7.3. For convenience, we label the four traps in the sample grown at 390 °C as ES1 (0.66 eV), ES2 (0.54 eV), ES3 (0.38 eV), and ES4 (0.14 eV), and name the tiny trap observed in the sample grown at 550 °C as ES5 (0.32 eV).

Table 7.3 Summary of the *n*-type GaAs Schottly diodes.

Sample #	Growth temperature (°C)	N_d (cm^{-3})	V_{bi} (V)	I @ -1V (uA)	Metal Contact
r1866	550	1.6×10^{16}	0.69	-0.11	Cr/Au
r1867	390	4.1×10^{16}	0.78	-0.11	Cr/Au

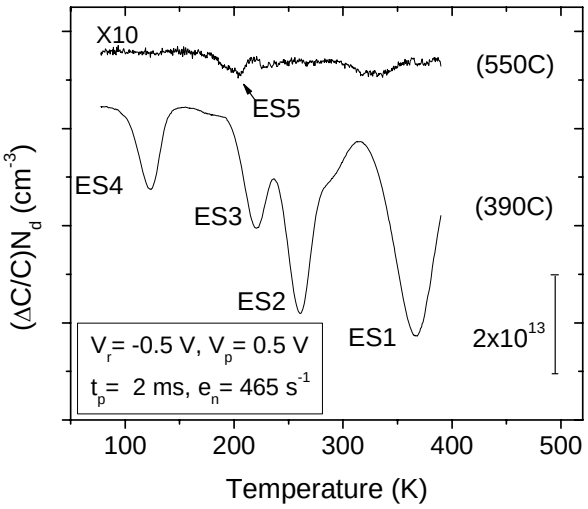


Figure 7.3 DLTS spectra from *n*-GaAs Schottky diode grown at different temperatures. The signals are offset for clarity.

Table 7.4 Electron traps found in the previously measured *n*-type GaAs Schottky diodes.

Sample #		r1866	r1867
T_g (°C)		550	390
E_A=0.14eV (ES4)	N_T (cm^{-3})		1.1×10^{14}
	σ (cm^2)		5.1×10^{-17}
E_A=0.32eV (ES5)	N_T (cm^{-3})	2.2×10^{12}	
	σ (cm^2)	2.4×10^{-15}	
E_A=0.38eV (ES3)	N_T (cm^{-3})		1.8×10^{14}
	σ (cm^2)		2.4×10^{-14}
E_A=0.54eV (ES2)	N_T (cm^{-3})		3.1×10^{14}
	σ (cm^2)		8.8×10^{-13}
E_A=0.66eV (ES1)	N_T (cm^{-3})		3.4×10^{14}
	σ (cm^2)		1.8×10^{-14}

From Table 7.4, we see that there are no traps at concentration higher than 3 x10^{12} cm^{-3} in the *n*-type GaAs layers grown at standard temperature (550 °C and above). However, many traps were found in the samples fabricated at low temperature, at concentrations of about 3 x10^{14} cm^{-3}.

7.2 *n*-type GaAs grown at 580 °C

This is an *n*-type GaAs layer grown at 580 °C, which is the standard growth temperature for *n*-type GaAs in the MBE system. The nominal epi-layer thickness is 600 nm. The Schottky contact is Cr/Au. Results of I-V and C-V measurements are summarized in Table 7.5. DLTS measurements were performed on two diodes. The DLTS spectra at an emission rate of 465 s^{-1} are shown in Fig. 7.4 for both diodes. No peaks were found in the tested devices, up to the detection limit for the trap concentration of 1 x10^{12} cm^{-3} for this sample. We conclude that there are no electron traps with concentration higher than 1x10^{12} cm^{-3} in this sample and the trap concentration is therefore lower than for the earlier similar *n*-type sample where the doping source was $SiBr_4$.

Table 7.5 Properties of *n*-type Schottky diodes grown at standard conditions using solid Si as the doping source. The built-in potential, doping concentration, leakage current at -1 V, and depletion width at 0 V are given.

Diode	V_{bi} (V)	N_d (cm^{-3})	I @ -1V (uA)	W @ 0V (nm)
r1948-(2,4)	0.81	4.4 x10^{17}	0.22	158
r1948-(4,2)	0.81	4.5 x10^{17}	0.10	155

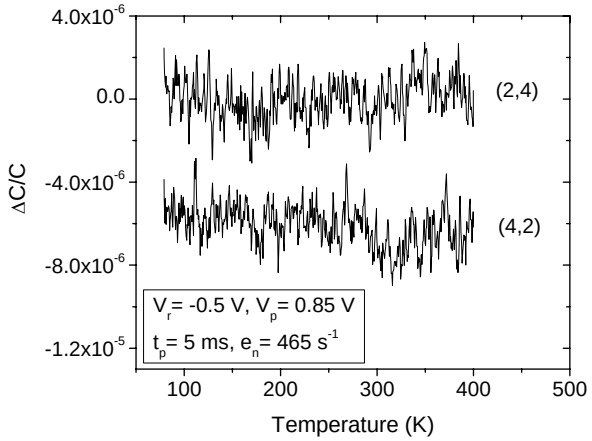


Figure 7.4 DLTS data taken from two different GaAs Schottky diodes fabricated on *n*-type GaAs grown at standard conditions at 580 °C using solid Si as the dopant source with all parameters shown. The signals are offset for clarity.

7.3 GaAs layers grown at 310 °C

Both *n*-type and *p*-type samples were grown at 310 °C, which is much lower than the standard growth temperature used for GaAs in the MBE system but is close to the growth temperature of the intrinsic layers in the *p-i-n* diodes. Sample r2232 is an *n*-type sample with an Al/Au Schottky contact. I-V measurements showed that the leakage current is about 0.22 mA at -1 V, which is too large for DLTS measurements with the SULA system. Sample r2231 is a *p*-type GaAs layer with nominal thickness of 520 nm. The Schottky contact is Al/Au. The sample was first evaluated by I-V and C-V measurements and the results are given in Table 7.6. It appears that the capacitance varies little, only about 5 pF, when the applied voltage was scanned from -3 V to 0 V. From a linear fit to the $1/C^2$ vs. V data of diode (2,3) near 0V bias, shown in Fig. 7.5, a doping of 2 x10^{17} cm^{-3}, much higher than the nominal doping of 3 x10^{16} cm^{-3} from Van der Pauw measurements of a layer grown at the

same temperature, and a non-physical value of the built-in potential (~10 V) are obtained. The expected built-in potential of Al on *p*-type GaAs is about 0.69 V [59]. Assuming a barrier height of 0.7 eV, and the value of the zero bias depletion width calculated from the measured capacitance, the doping should be about 1.3 x10^{16} cm^{-3}, close to the expected value. From the C-V data for other diode that has a non-linear $1/C^2$ vs. V curve, the doping concentration is not uniform through the depletion region. This indicates two possibilities: (1) a non-uniform doped low T_g layer or (2) the low T_g layer thickness is less than the depletion width and the buffer layer is also probed in this bias voltage range. In the latter case, the thickness of the low T_g layer must be less than 300 nm, from the C-V measurements.

Table 7.6 Properties of *p*-type Schottky diodes fabricated from GaAs grown at 310 ºC. The built-in potential, doping concentration, leakage current at -1 V, and depletion width at 0 V are given.

Diode	V_{bi} (V)	N_a (cm^{-3})	I @ -1V (uA)	W @ 0V (nm)
r2231-(2,2)	10.5	1.9 x10^{17}	-21.2	285
r2231-(2,3)	11.4	2.1 x10^{17}	-0.16	281
r2231-(3,3)	10.2	1.9 x10^{17}	-26.2	282

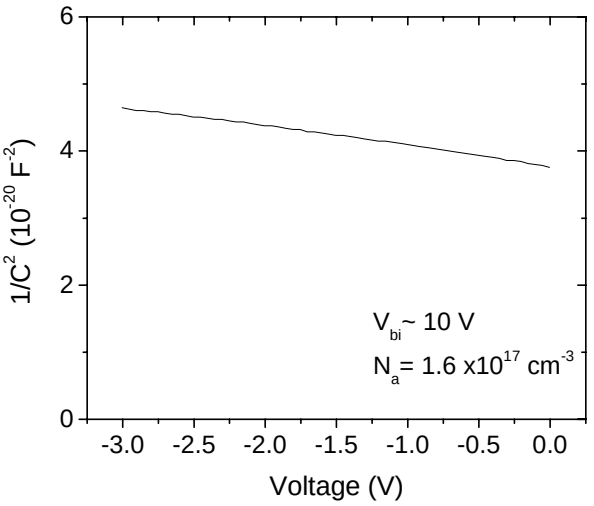


Figure 7.5 $1/C^2$ vs. V plot of device (2,3) of sample r2231.

DLTS measurements were performed on three different diodes, and two majority carrier traps were detected, labelled HS1 and HS2. The DLTS spectra at an emission rate of 465 s^{-1} are shown in Fig. 7.6 for all three diodes. Both traps were seen in all three tested devices, and the trap concentrations were similar, suggesting that these defects are homogeneously distributed in the sample. The defect concentration of HS1 could only be estimated, since the amplitude of HS1 is impacted by HS2 as well as a positive peak at higher temperature range. There is a large change in the peak height of HS2 when measured using different rate windows, and a smaller amplitude change in HS1, as shown in Fig. 7.7. This behaviour may be caused by a large reverse bias leakage current [61]. However, the current of r2231 is not large enough to cause such large changes. In addition, the activation energy of HS2 is higher than HS1 but the peak of HS2 is at a lower temperature, which shows that the capture cross section of HS2 must be much larger than that of HS1. It should be noticed that the capture cross section may be dependent on the temperature, i.e. $\sigma = \sigma_0 \exp\left(\Delta E_\sigma / kT\right)$. In this case, $E_A = E_\sigma + E_T$. This could then explain the large value in the activation energy of HS2, which

is much larger than $E_g/2$. This could also be the reason for the amplitude difference of traps at different rate windows. Results are summarized in Table 7.7.

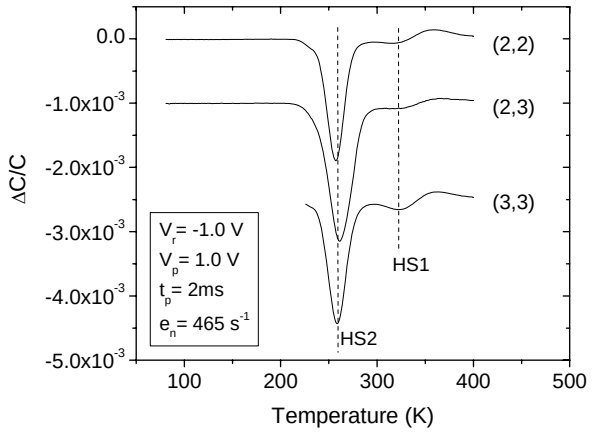


Figure 7.6 DLTS data taken from three different diodes on sample r2231, with all parameters shown. The signals are offset for clarity.

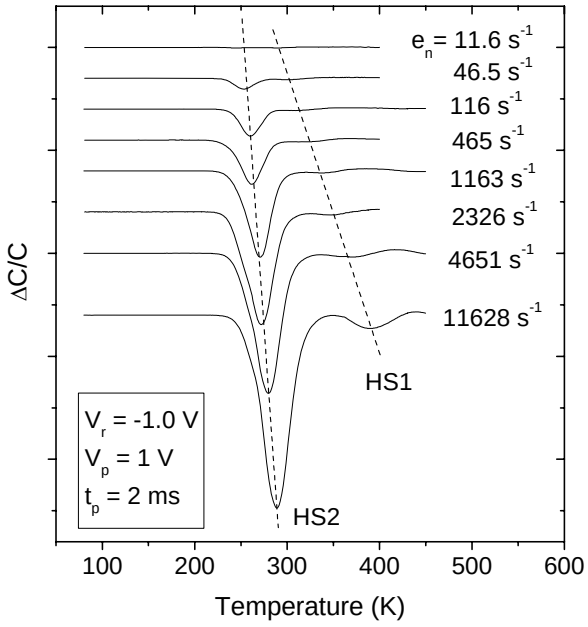


Figure 7.7 DLTS spectra of device (2,3) in sample r2231. The peak height of HS2 varies significantly with rate windows. The signals are offset for clarity.

Table 7.7 Activation energy, capture cross section and concentration calculated for the two traps observed in the DLTS spectra. The trap concentration for trap HS1 is approximate.

Diodes		r2231-(2,2)	r2231-(2,3)	r2231-(3,3)
Trap HS1	E_A (eV)	0.71 ± 0.05	0.48 ± 0.04	0.63 ± 0.03
	σ (cm^2)	1.5 x10^{-13}	3.0 x10^{-17}	4.3 x10^{-15}
	N_T (cm^{-3})	> 2 x10^{14}	8 x10^{14}	7 x10^{14}
Trap HS2	E_A (eV)	0.99 ± 0.09	0.86 ± 0.05	0.80 ± 0.05
	σ (cm^2)	2.8 x10^{-5}	3.9 x10^{-8}	4.0 x10^{-9}
	N_T (cm^{-3})	5.3 x10^{15}	1.2 x10^{16}	8.1 x10^{15}

The activation energy and capture cross section for HS1 were calculated using the temperature at the minimum of the peak. The overlap with HS2 at fast emission rates and the presence of the positive peak at high temperature causes a significant error in the peak height and position. This is indicated by the very large scatter in the calculated values of the activation energy and capture cross section of HS1 for the three devices. We also note that the value of the activation energy and capture cross section for HS2 in device (2,2) is significantly different from that measured in the other two diodes.

The peak HS1 found in the 310 °C *p*-type GaAs sample is at the same temperature position as the 0.57 eV hole trap in the other p-type Schottky samples, as shown in Fig. 7.8. Also, the capture cross section of HS1 is within about an order of magnitude as the capture cross section of this trap in the 350 °C *p*-type GaAs sample. This indicates that HS1 is likely the same hole trap as the 0.57 eV trap present in the other samples. Although the concentration of this trap was two orders of magnitude lower in the *p*-type GaAs layer grown at 350 °C, the HS1 trap concentration is as high as the high T_g samples. As mentioned in our discussion of the C-V measurements, it is possible that the thickness of the 310 °C is smaller than the depletion width and that high T_g buffer layer is also detected in the DLTS measurements. Therefore the HS1 defect may be located in the GaAs buffer layer grown at standard temperature but not in the layer grown at 310 °C. This interpretation would be consistent with the trend showing only a low concentration of this trap in GaAs grown at 350 °C. To verify this, another sample with a thicker low T_g layer should be prepared.

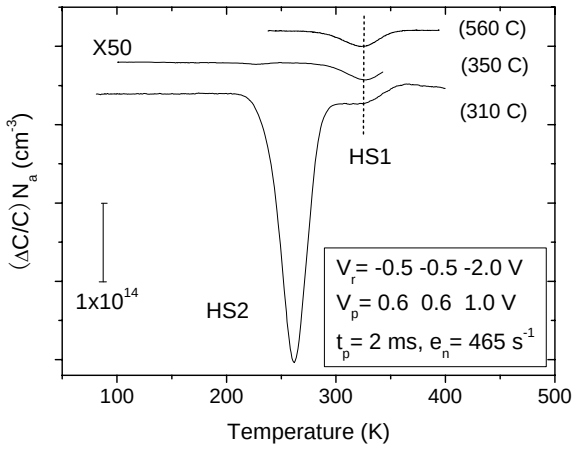


Figure 7.8 Comparision of DLTS spectra of *p*-GaAs layers grown at different temperatures. The signals are offset for clarity.

7.4 Discussion: defects in GaAs

All the defects found in these MBE-grown GaAs layers from UBC/UVic samples are listed in Table 7.8. Comparing these results with the literature work on *p*-type GaAs [62-66], a 0.57eV defect with a similar capture cross section has been consistently observed in GaAs when Fe had been diffused into the sample. This trap has therefore been associated with Fe impurities [63]. Another trap with similar activation energy of 0.54eV has been identified as the double donor state of the arsenic anti-site defect [67]. The single donor state of the arsenic anti-site, As_{Ga}, known as EL2 [68], is located about 0.75eV below the conduction band and is easily observed in *n*-type GaAs. The arsenic anti-site defect is uniquely identified by its persistent metastable behaviour upon optical illumination at low temperature [67]. However, this trap is not typically observed in MBE-grown GaAs and was not observed in our *n*-type samples, suggesting that Fe is a more likely candidate for this trap. No traps similar to HS2 have been found in the literature and its origin is unknown.

By looking in the literature [68], we find that the traps ES4 and ES2, observed in our GaAs layer grown at 390 °C, are commonly found in bulk and MBE grown material and are known as EL10 and EL4, respectively. Also, the 0.32 eV (labelled as ES5 here) defect found in *n*-type GaAs grown at standard T could be the trap EL7, which is also commonly observed in MBE GaAs [68]. Since all the GaAs samples were grown under As-rich conditions, the defects present are expected to be either the Ga vacancy or the As interstitial or their complexes [68-70]. Traps with properties similar to ES1 and ES3 could not be found in the literature to our knowledge.

Table 7.8 Summary of all traps in GaAs Schottky diodes measured.

Sample #		*p*-type					*n*-type		
		r1729	r1730	r1838	r1840	r2231	r1948	r1866	r1867
T_g (°C)		560	450	350	350	310	580	550	390
0.14eV (ES4)	N_T (cm^{-3})								1.1×10^{14}
	σ (cm^2)								5.1×10^{-17}
0.17eV	N_T (cm^{-3})		3.2×10^{13}						
	σ (cm^2)		N/A						
0.32eV (ES5)	N_T (cm^{-3})							2.2×10^{12}	
	σ (cm^2)							2.4×10^{-15}	
0.38eV (ES3)	N_T (cm^{-3})								1.8×10^{14}
	σ (cm^2)								2.4×10^{-14}
0.54eV (ES2)	N_T (cm^{-3})								3.1×10^{14}
	σ (cm^2)								8.8×10^{-13}
0.57eV (HS1)	N_T (cm^{-3})	2.2×10^{14}	5.4×10^{14}	4.5×10^{12}	2.1×10^{12}	8.2×10^{14}			
	σ (cm^2)	N/A	N/A	3.7×10^{-16}	3.8×10^{-16}	3.0×10^{-17}			
0.66eV (ES1)	N_T (cm^{-3})								3.4×10^{14}
	σ (cm^2)								1.8×10^{-14}
0.86eV (HS2)	N_T (cm^{-3})					1.2×10^{16}			
	σ (cm^2)					3.9×10^{-8}			

7.5 Summary

In conclusion, several different electrically active defects were observed in GaAs samples grown in the temperature range 310-580 °C. The trap observed in *p*-type samples grown at standard temperature may be related to Fe. The origin of the trap in high concentration observed in *p*-type GaAs grown at 310 °C is unknown. The four traps observed in *n*-type GaAs grown at 390 °C have also not been identified, although two of them have been frequently observed previously in MBE-grown GaAs. We note that an *n*-type sample grown at 310 °C could not be measured and that the diode characteristics of the *p*-type sample grown at 310 °C were poor. Therefore, additional work is needed to characterize deep levels in GaAs grown at temperatures below 400 °C. Nevertheless, the results presented here will serve as a basis for interpreting DLTS measurements of the *p*-*i*-*n* diodes presented in the following chapter.

Chapter 8

DLTS on GaAs and $GaAs_{1-x}Bi_x$ *p-i-n* structures

As was discussed in Chapter 6, the $GaAs_{1-x}Bi_x$ Schottky samples did not give reliable DLTS spectra. Hence, *p-i-n* structures having a thin $GaAs_{1-x}Bi_x$ quantum well at the center of the intrinsic layer, which had been fabricated at UBC for electroluminescence measurements, were also measured by DLTS to investigate deep level defects. This device is not ideal for DLTS measurements for several reasons. Because its structure is symmetric, it is difficult to tell the location of the deep states and it is not possible to know whether they are trapping electrons or holes. And it is hard to distinguish between traps in the GaAs layers or in the bismide layer. To help solve these problems, the GaAs Schottky samples discussed in Chapter 7 were measured as references. Also two GaAs *p-i-n* structures were fabricated at UBC as control samples, in order to help interpret the DLTS spectra of the $GaAs_{1-x}Bi_x$ *p-i-n* diodes.

Six *p-i-n* diodes with bismide fraction ranging from 0 to 4.7% were measured by DLTS. The layer structure is shown in Fig. 8.1 and the measured layer thicknesses and alloy compositions measured by XRD are given in Table 8.1. The $GaAs_{1-x}Bi_x$ *p-i-n* diodes have an *n*-type and *p*-type doped GaAs layer on each side of a nominally 100 nm-thick intrinsic layer having a 50 nm $GaAs_{1-x}Bi_x$ quantum well at the center. The doped *p*-type and *n*-type GaAs

layers were grown at standard temperature, about 550 °C. The growth temperature of the three intrinsic layers is about 300 °C. Ohmic contacts are Ti/Pt/Au on the *p*-type layer and Ni/Au-Ge/Au on the *n*-type substrate. For some samples, the growth was interrupted for about 10 minutes at the interface of the *n*-type GaAs layer and the first intrinsic GaAs layer, while the substrate temperature was decreased. For samples grown without this interrupt, the substrate temperature was ramped down during the growth of the first GaAs intrinsic layer.

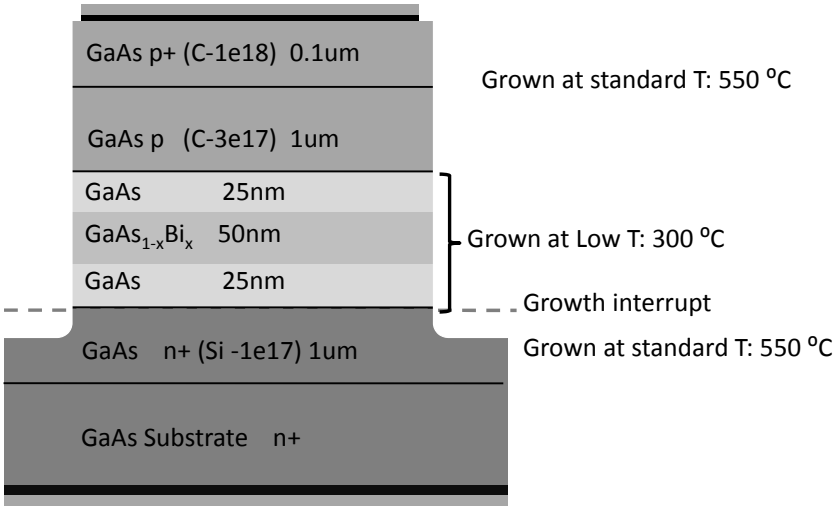


Figure 8.1 Schematic structure of $GaAs_{1-x}Bi_x$ *p-i-n* diode.

Table 8.1 List of GaAs and $GaAs_{1-x}Bi_x$ *p-i-n* structures measured by DLTS.

Sample #	% Bi	GaAsBi layer thickness (nm)	*i*-layer thickness (nm) GaAs/GaAsBi/GaAs	*i*-layer growth temperature (°C)	Growth interrupt
r1960	0	0	110	580	No
r2163	0	0	100	300	Yes
r1970	1.4	30-60	30/30-60/30	350	Yes
r1965	1.8	30	27/30/25	310	Yes
r2069	4.0	16	90/16/90	285	No
r2100	4.7	16	35/16/90	285	No

The measured leakage current at -1 V bias for all the *p-i-n* diodes was < 0.5 μA. As expected, the zero bias depletion width determined from C-V measurements was found to be larger than the nominal width of the intrinsic layer for all the diodes tested. The standard analysis of the C-V data used for Schottky or one-sided abrupt *p-n* diodes is not valid for the *p-i-n* diodes. Thus, the built-in potential and doping concentration of these samples were not determined. The defect concentrations were calculated using the nominal doping concentrations in the *p*-type and *n*-type doped layers, which were determined from GaAs and $GaAs_{1-x}Bi_x$ calibration layers. The data for the sample with 4.0% Bi looks quite different from the others and therefore results for this sample are not included here.

When measuring with DLTS, standard initial settings were used for all samples: an offset voltage of -1 V, a filling pulse of 20 ms, a period of 200 ms, and filling pulse voltages in the range of 0 V to 1.5 V. The DLTS spectra shown were taken using an emission rate of 465 s^{-1}. The defect concentrations were calculated when the corresponding peak was saturated. If there was no indication of saturation at the filling pulse voltage of 1.5 V, the peak height at 1.5 V was calculated providing a lower limit for the trap concentration. Equation (4.22) on page 44 was used to calculate the trap concentrations in Schottky diodes or one-sided *p-n* junctions. However, in the case of symmetric *p-n* junctions, the depletion width extends equally into the *n*-type and *p*-type regions and doping concentration in the lightly doped material (N_d or N_a) is replaced by $N_a N_d / (N_a + N_d)$, as shown in Equation (3.5) on page 24. The nominal doping concentration and the net carrier concentration of each *p-i-n* diode are summarized in Table 8.2. Therefore, the trap concentration in the *p-i-n* diodes was calculated using

$$N_T = 6\frac{N_a N_d}{N_a + N_d}\frac{S(T_m)}{C(V_R)}\left\{\frac{W^2(V_R)}{\left(W(V_R)-\lambda\right)^2-\left(W(V_p)-\lambda\right)^2}\right\}. \qquad (8.1)$$

Table 8.2 Nominal doping concentration and net charge density of *p-i-n* diodes.

Diode	% Bi	Nominal N_d (cm^{-3})	Nominal N_a (cm^{-3})	$N_a N_d / (N_a + N_d)$ (cm^{-3})
r1960	0	1.1×10^{17}	3.2×10^{17}	8.2×10^{16}
r2163	0	1.9×10^{17}	3.0×10^{17}	1.2×10^{17}
r1970	1.4	1.1×10^{17}	3.2×10^{17}	8.2×10^{16}
r1965	1.8	1.1×10^{17}	3.2×10^{17}	8.2×10^{16}
r2100	4.7	1.3×10^{17}	1.5×10^{17}	7.0×10^{16}

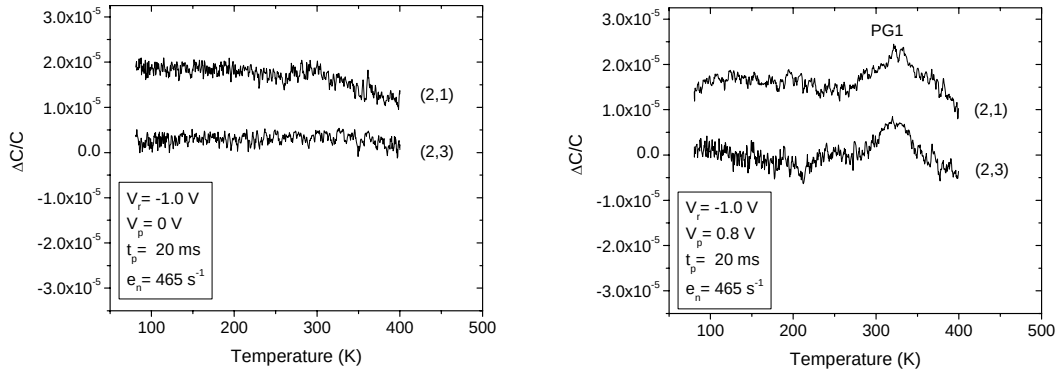
8.1 GaAs *p-i-n* diodes

Two GaAs *p-i-n* diodes were fabricated and measured in order to detect defects in the GaAs doped and intrinsic layers. The doped *p*-type and *n*-type GaAs layers were both grown at standard temperature, around 580 ^{0}C. However, the growth temperature of the intrinsic GaAs layer was different for the two samples; specifically, it was the standard temperature of 580 ^{0}C for sample r1960, and a low temperature of 300 ^{0}C, which is similar to the temperature used for growing the intrinsic layers in the *p-i-n* samples containing bismide, was used for sample r2163.

8.1.1 GaAs *p-i-n* with all layers grown at 580 °C (sample r1960)

The GaAs high T_g (HT_g) *p-i-n* sample was grown at 580 °C. DLTS measurements were performed on two different diodes, with the filling pulse voltage at 0 V and 0.8 V. The DLTS spectra are shown in Fig. 8.2 for both diodes. Comparing Fig. 8.2 (a) and (b), we see that, with 0 V filling pulse, i.e. with no injection current through the intrinsic layer, no peaks are found; while a weak positive peak (PG1) is seen when there is injection current with the filling pulse voltage at 0.8 V. As discussed above, it cannot be determined whether electrons or holes are majority carriers. Therefore the trap concentrations and capture cross sections for each trap are calculated as both an electron and a hole trap. The activation energy and capture cross section calculated may include some extra uncertainties (±0.01 eV of E_A and

$\pm 1 \times 10^{-21}$ cm^2 of σ) caused by the ~±5 K errors of defining the peak position and the amplitude because of the noisy spectra. Detailed results are shown in Table 8.3.



(a) (b)

Figure 8.2 DLTS data taken from two different diodes on GaAs HT_g, with (a) filling pulse voltage at 0 V and (b) filling pulse voltage at 0.8 V. The signals are offset for clarity.

Table 8.3 Activation energy, capture cross section and concentration of each trap found in the GaAs HT_g sample.

Diode		r1960-(2,1)	r1960-(2,3)
PG1	E_A (eV)	0.63 ± 0.04	0.57 ± 0.05
	σ (cm^2)	1.4×10^{-13} (e) 6.7×10^{-15} (h)	1.5×10^{-14} (e) 6.7×10^{-15} (h)
	N_T (cm^{-3})	2.6×10^{13} (e) 1.5×10^{13} (h)	2.3×10^{13} (e) 1.4×10^{13} (h)

8.1.2 GaAs *p-i-n* with intrinsic layers grown at 300 °C (sample r2163)

Sample r2163 (GaAs LT_g) has the doped layers grown at 580 °C and the intrinsic layer grown at 300 °C. DLTS measurements were performed on three different diodes and the spectra are

shown in Fig. 8.3. The spectra for diode r2163-(1,3), is different from the spectra for the other two diodes at all three filling pulse conditions, indicating that the sample is not homogeneous. This lateral in-homogeneity may arise from the substrates, which are not device quality. Many DLTS peaks are present. There is a big positive peak (PG2) at about 370 K, and many peaks overlapping together below 300 K. When the filling pulse voltage is increased to 1.5 V, an additional negative peak (NG1) is seen at 230 K for diode (1,2) and (2,1), and at about 180 K for diode (1,3). Although the peak position is different, the amplitude of the negative peaks for the three diodes is almost the same. Detailed results for the two similar devices are given in Table 8.4.

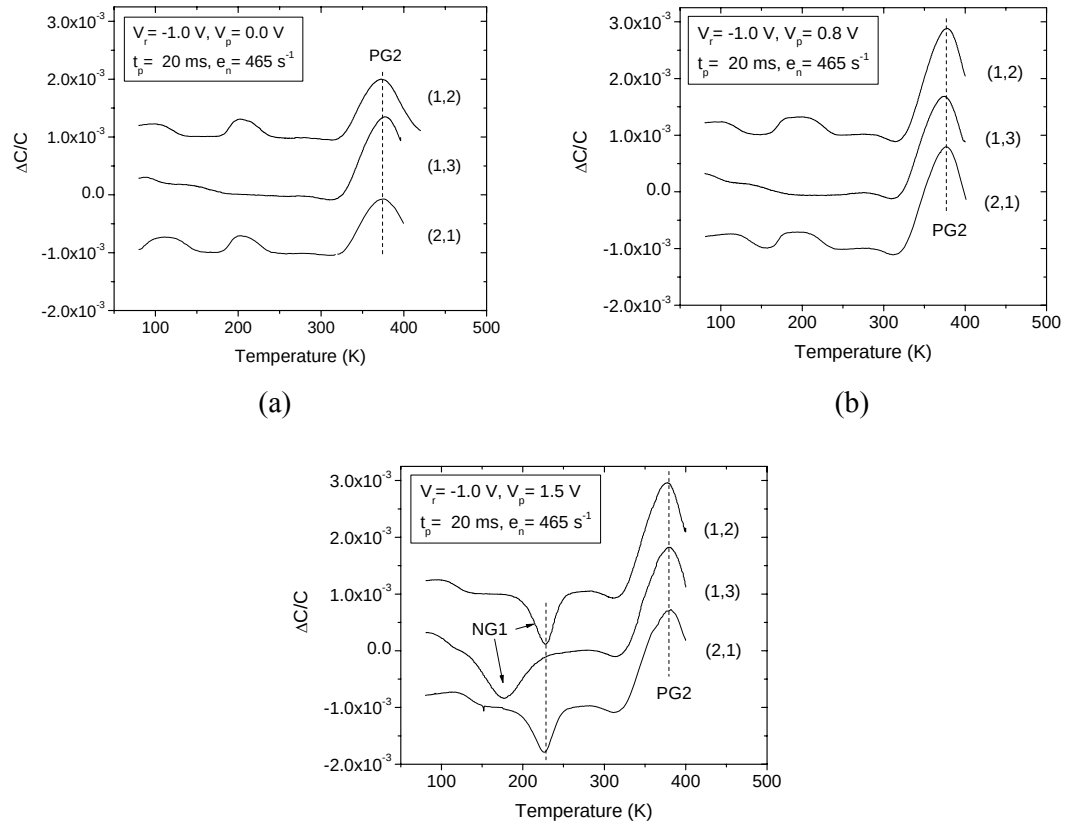


Figure 8.3 DLTS spectra of three diodes on GaAs LT_g, with (a) filling pulse voltage at 0 V; (b) filling pulse voltage at 0.8 V; and (c) filling pulse voltage at 1.5 V. The signals are offset for clarity.

Table 8.4 Activation energy, capture cross section and concentration of traps found in two similar diodes on the GaAs LT_g sample.

Diode		r2163-(1,2)	r2163-(1,3)	r2163-(2,1)
PG2	E_A (eV)	0.52 ± 0.03	0.42 ± 0.02	0.51 ± 0.04
	σ (cm^2)	2.0×10^{-16} (e) 1.0×10^{-17} (h)	8.6×10^{-17} (e) 4.3×10^{-18} (h)	1.1×10^{-16} (e) 5.6×10^{-18} (h)
	N_T (cm^{-3})	2.3×10^{15} (e) 2.1×10^{15} (h)	2.2×10^{15} (e) 2.0×10^{15} (h)	2.1×10^{15} (e) 1.8×10^{15} (h)
NG1	E_A (eV)	0.29 ± 0.01	0.09 ± 0.01	0.28 ± 0.01
	σ (cm^2)	8.9×10^{-17} (e) 4.5×10^{-18} (h)	2.3×10^{-20} (e) 1.1×10^{-21} (h)	7.5×10^{-17} (e) 3.8×10^{-18} (h)
	N_T (cm^{-3})	1.0×10^{15} (e) 9.5×10^{14} (h)	9.0×10^{14} (e) 8.1×10^{14} (h)	8.7×10^{14} (e) 7.9×10^{14} (h)

8.2 GaAs *p-i-n* diodes with a $GaAs_{1-x}Bi_x$ quantum well

8.2.1 $GaAs_{1-x}Bi_x$ quantum well with 1.4% Bismide (sample r1970)

Sample r1970 has a $GaAs_{1-x}Bi_x$ quantum well with 1.4% bismide. DLTS measurements were performed on two different diodes and the spectra are shown in Fig. 8.4. The two diodes give exactly the same spectra with 0 V and 0.8 V filling pulses; however, for V_p =1.5 V, a positive peak is seen for diode (1,3) around 100 K.

Many peaks are shown in the spectra, and all of them are majority carrier traps except for the positive signal at T < 100K for diode (1,3). There is always a big peak (NB1) at about 350 K, with and without injection current. When the filling pulse voltage is above 0 V, several additional peaks (NB2, NB3, NB4, NB5) occur. There is also a peak between NB2 and NB3, however, it is difficult to fit that peak or determine the peak temperature for most of the emission rates. Hence, no further analysis was done for this small peak. Detailed results are shown in Table 8.5.

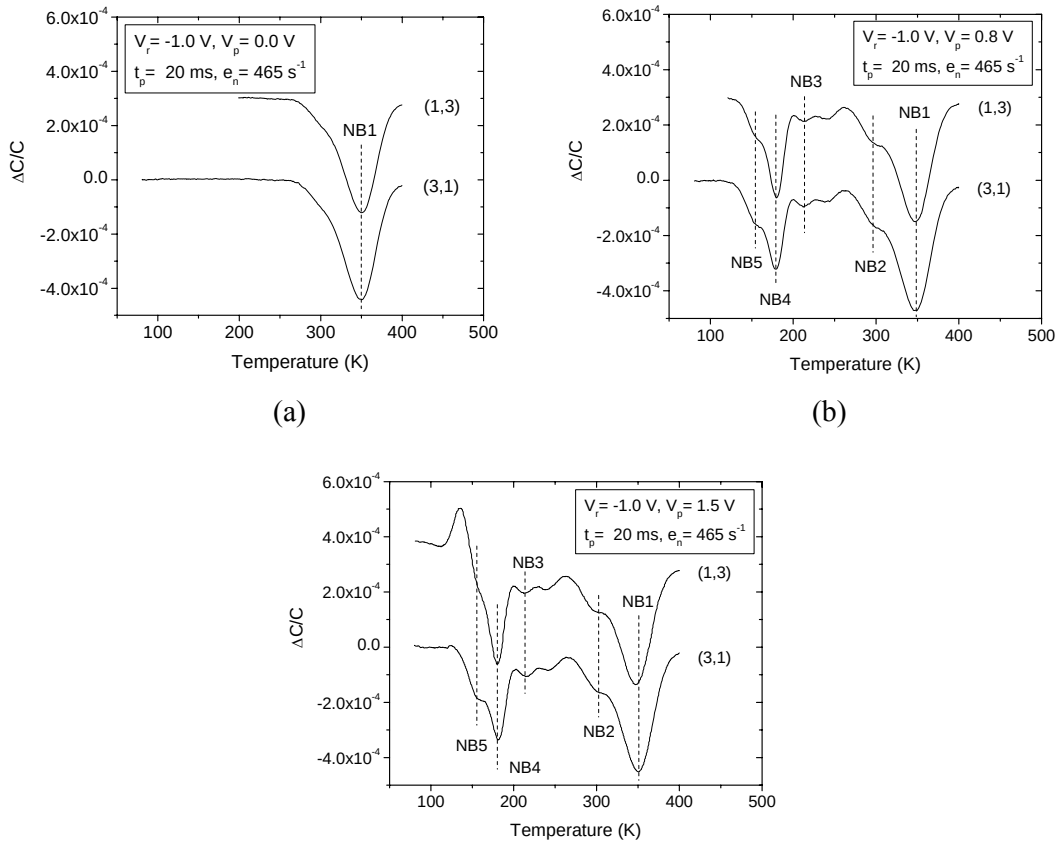


Figure 8.4 DLTS spectra of two diodes on the 1.4% Bi sample, with (a) filling pulse voltage at 0 V; (b) filling pulse voltage at 0.8 V; and (c) filling pulse voltage at 1.5 V. The signals are offset for clarity.

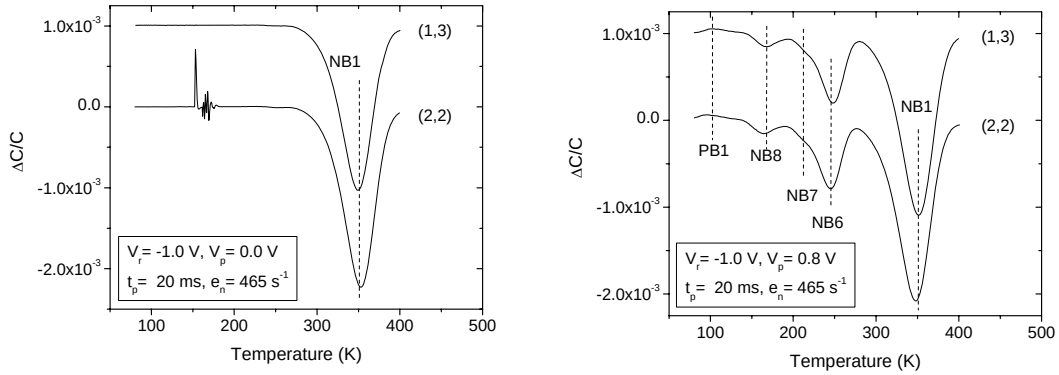
Table 8.5 Activation energy, capture cross section and concentration of each trap found in the 1.4% Bi sample.

Diode		r1970-(1,3)	r1970-(3,1)
NB1	E_A (eV)	0.63 ± 0.01	0.64 ± 0.01
	σ (cm^2)	2.4 x10^{-14} (e) 1.2 x10^{-15} (h)	2.8 x10^{-14} (h) 1.4 x10^{-15} (h)
	N_T (cm^{-3})	1.1 x10^{15} (e) 5.1 x10^{14} (h)	9.9 x10^{14} (e) 5.1 x10^{14} (h)
NB2	E_A (eV)	0.56 ± 0.01	0.56 ± 0.02
	σ (cm^2)	5.6 x10^{-14} (e) 2.8 x10^{-15} (h)	5.0 x10^{-14} (e) 2.5 x10^{-15} (h)
	N_T (cm^{-3})	3.7 x10^{14} (e) 1.7 x10^{14} (h)	3.4 x10^{14} (e) 1.7 x10^{14} (h)
NB3	E_A (eV)	0.37 ± 0.02	0.37 ± 0.01
	σ (cm^2)	2.7 x10^{-14} (e) 1.4 x10^{-15} (h)	2.2 x10^{-14} (e) 1.1 x10^{-15} (h)
	N_T (cm^{-3})	1.5 x10^{14} (e) 8.8 x10^{13} (h)	1.3 x10^{14} (e) 8.4 x10^{13} (h)
NB4	E_A (eV)	0.33 ± 0.01	0.33 ± 0.01
	σ (cm^2)	8.7 x10^{-14} (e) 4.3 x10^{-15} (h)	8.2 x10^{-14} (e) 4.1 x10^{-15} (h)
	N_T (cm^{-3})	4.9 x10^{14} (e) 3.1 x10^{14} (h)	3.9 x10^{14} (e) 2.6 x10^{14} (h)
NB5	E_A (eV)	0.32 ± 0.02	0.22 ± 0.02
	σ (cm^2)	1.9 x10^{-12} (e) 9.4 x10^{-14} (h)	9.5 x10^{-16} (e) 4.7 x10^{-17} (h)
	N_T (cm^{-3})	1.9 x10^{14} (e) 1.2 x10^{14} (h)	1.5 x10^{14} (e) 9.9 x10^{13} (h)

8.2.2 $GaAs_{1-x}Bi_x$ quantum well with 1.8% Bismide (sample r1965)

Sample r1965 has a $GaAs_{1-x}Bi_x$ quantum well with 1.8% bismide. DLTS measurements were performed on two different diodes and the spectra are shown in Fig. 8.5. The two diodes give exactly the same spectra with all filling pulse voltages. With filling pulse voltage above 0.8 V, the DLTS signals are almost the same as that of 0.8 V.

In total five peaks are shown in the spectra. Four of them are majority carrier traps and one is a minority carrier trap appearing at about 90 K. There is also a big peak (same peak as NB1 in r1970) at about 350 K, with and without injection current. When the filling pulse voltage is above 0 V, several additional peaks (NB6, NB7, NB8, PB1) occur. Detailed results are shown in Table 8.6.



(a) (b)

Figure 8.5 DLTS spectra of two diodes on the 1.8% Bi sample, with (a) filling pulse voltage at 0 V and (b) filling pulse voltage at 0.8 V. The signals are offset for clarity.

Table 8.6 Activation energy, capture cross section and concentration of each trap found in the 1.8% Bi sample.

Diode		r1965-(1,3)	r1965-(2,2)
NB1	E_A (eV)	0.62 ± 0.02	0.63 ± 0.02
	σ (cm^2)	1.4 x10^{-14} (e) 7.0 x10^{-16} (h)	1.8 x10^{-14} (e) 8.9 x10^{-16} (h)
	N_T (cm^{-3})	6.0 x10^{15} (e) 2.9 x10^{15} (h)	6.7 x10^{15} (e) 2.9 x10^{15} (h)
NB6	E_A (eV)	0.41 ± 0.02	0.41 ± 0.01
	σ (cm^2)	7.3 x10^{-15} (e) 3.7 x10^{-16} (h)	8.4 x10^{-15} (e) 4.2 x10^{-16} (h)
	N_T (cm^{-3})	1.4 x10^{15} (e) 8.4 x10^{14} (h)	1.5 x10^{15} (e) 8.2 x10^{14} (h)
NB7	E_A (eV)	0.37 ± 0.02	0.36 ± 0.02
	σ (cm^2)	1.1 x10^{-14} (e) 5.4 x10^{-16} (h)	7.2 x10^{-15} (e) 3.6 x10^{-16} (h)
	N_T (cm^{-3})	4.3 x10^{14} (e) 2.3 x10^{14} (h)	4.3 x10^{14} (e) 2.6 x10^{14} (h)
NB8	E_A (eV)	0.25 ± 0.02	0.29 ± 0.02
	σ (cm^2)	3.8 x10^{-15} (e) 1.9 x10^{-16} (h)	4.7 x10^{-14} (e) 2.3 x10^{-15} (h)
	N_T (cm^{-3})	2.2 x10^{14} (e) 1.5 x10^{14} (h)	2.4 x10^{14} (e) 1.5 x10^{14} (h)
PB1	E_A (eV)	0.49 ± 0.06	0.32 ± 0.05
	σ (cm^2)	321 (e) 16.1 (h)	8.1 x10^{-6} (e) 4.0 x10^{-7} (h)
	N_T (cm^{-3})	1.7 x10^{14} (e) 9.2 x10^{13} (h)	1.2 x10^{14} (e) 7.6 x10^{13} (h)

8.2.3 $GaAs_{1-x}Bi_x$ quantum well with 4.7% Bismide (sample r2100)

Sample r2100 has a $GaAs_{1-x}Bi_x$ quantum well with 4.7% bismide. DLTS measurements were performed on four different diodes and the spectra are shown in Fig. 8.6. Three out of the four diodes give exactly the same spectra with all filling pulse voltages. However, diode (4,4) is different from the others. With a 0 V filling pulse, similar to the other two $GaAs_{1-x}Bi_x$

p-i-n samples, a large majority carrier peak (NB9) appears at about 340 K, but NB9 is not the same trap as NB1 in r1970 with 1.4% Bi and r1965 with 1.8% Bi. At least two positive peaks between 250 K and 300 K overlap together, which was not found in other GaAsBi *p-i-n* samples.

Focusing on the reproducible diodes (1,2), (1,4) and (2,3), when the filling pulse is above 0 V, the positive peaks become overwhelmed by the signal from majority carrier traps and the peak becomes negative (NB10). The amplitude of NB10 increases very fast with filling pulse voltage, and exceeds NB9 eventually. Only one positive peak at 0 V becomes negative with injection current for diode (4,4) and there is still a positive peak left. The two peaks in the spectra of other diodes may be three peaks actually, one positive and two negative, overlapping together. Nonetheless, this is only a guess and the analysis of these peaks assumes that there are only two negative peaks with injection. Detailed results are shown in Table 8.7.

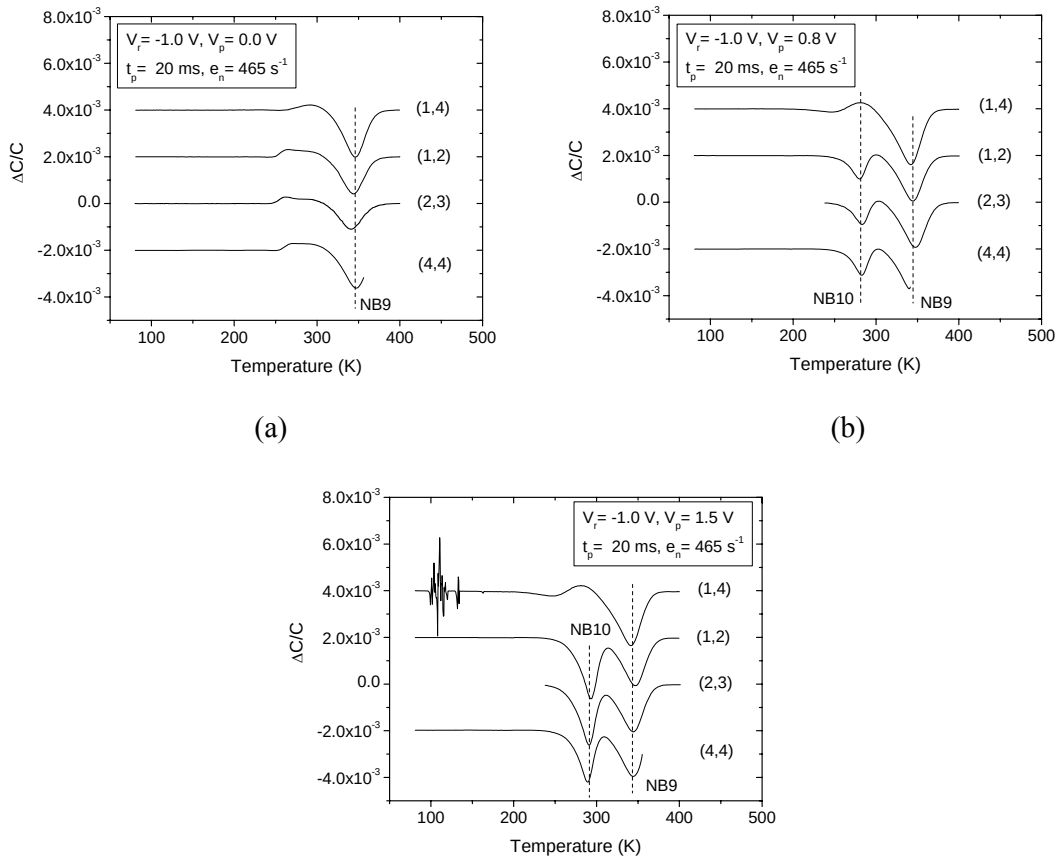


Figure 8.6 DLTS spectra of four diodes on the 4.7% Bi sample, with (a) filling pulse voltage at 0 V; (b) filling pulse voltage at 0.8 V; and (c) filling pulse voltage at 1.5 V. The signals are offset for clarity.

Table 8.7 Activation energy, capture cross section and concentration of each trap found in the 4.7% Bi sample.

Diode		r2100-(1,2)	r2100-(1,4)	r2100-(2,3)	r2100-(4,4)
NB9	E_A (eV)	0.73 ± 0.02	0.71 ± 0.01	0.71 ± 0.02	0.71 ± 0.03
	σ (cm^2)	7.3×10^{-13} (e) 3.7×10^{-14} (h)	5.2×10^{-13} (e) 2.6×10^{-14} (h)	4.2×10^{-13} (e) 2.1×10^{-14} (h)	3.9×10^{-13} (e) 1.9×10^{-14} (h)
	N_T (cm^{-3})	2.0×10^{15} (e) 1.8×10^{15} (h)	1.9×10^{15} (e) 1.8×10^{15} (h)	1.9×10^{15} (e) 1.7×10^{15} (h)	1.5×10^{15} (e) 1.4×10^{15} (h)
NB10	E_A (eV)	0.57 ± 0.01	0.51 ± 0.01	0.58 ± 0.01	0.60 ± 0.01
	σ (cm^2)	1.8×10^{-13} (e) 8.9×10^{-15} (h)	9.7×10^{-13} (e) 4.9×10^{-14} (h)	2.8×10^{-13} (e) 1.4×10^{-14} (h)	6.7×10^{-13} (e) 3.3×10^{-14} (h)
	N_T (cm^{-3})	2.6×10^{15} (e) 2.4×10^{15} (h)	1.7×10^{15} (e) 1.6×10^{15} (h)	2.2×10^{15} (e) 2.0×10^{15} (h)	1.6×10^{15} (e) 1.5×10^{15} (h)

8.3 Simulations of the *p-i-n* structures

Because these samples are essentially symmetrically-doped diodes consisting of three or five different epi-layers, interpreting the DLTS spectra obtained from them is difficult. The depletion region extends almost equally far into both the *n*- and the *p*-doped layers making it impossible to distinguish electron trapping in the n-layer from hole trapping in the *p*-type layer, since both processes are detected as majority carrier peaks in the DLTS spectrum. In addition, the background doping type in the *i*-layers is not known and thus which carrier is the majority carrier in those layers is also not known. Therefore, calculations of the band diagrams of the *p-i-n* diodes under various bias conditions have been employed to help interpret the DLTS results. These simulations were carried out using Nextnano [71, 72]. The main process of the simulation is to solve the Poisson equation (Equation (3.2) on page 22) to get a self-consistent potential and the quasi-Fermi level. We assume all the band parameters of GaAsBi are the same as those of GaAs, and also that the change in band gap occurs entirely at the valence band with E_V increasing by 83 meV/%Bi. The simulated structure is using the same layer thickness and doping as the 4.7% Bi sample.

The band diagram of the 1.8% and 4.7% bismide *p-i-n* samples under zero, reverse and forward bias were simulated. The layer parameters of the 4.7% bismide *p-i-n* sample were used for the simulation shown in Fig. 8.7.

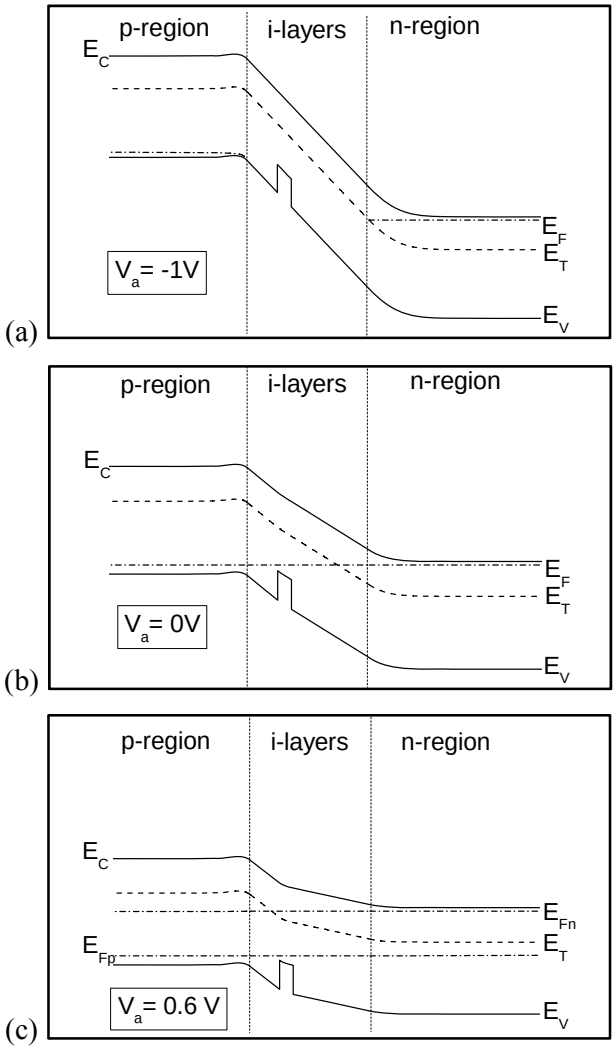


Figure 8.7 Simulation of the band diagram of the 4.7% Bi sample under applied voltage at (a) reverse bias, (b) zero bias, and (c) forward bias. An electron trap with $E_A = 0.46eV$ is shown for illustration. E_{Fn} and E_{Fp} are the quasi-Fermi levels when there is injection current.

We see from the above figure of the 4.7% Bi sample that although the depletion region extends into the *n*-type layer, electron traps with activation energy at 0.46 eV located in the *n*-layer are always filled when the applied voltage is -1 V. Thus, at an offset voltage of -1 V, the DLTS transient cannot come from traps deeper than 0.46 eV in the *n*-type layer. When 0 V bias is applied, some traps in the intrinsic layers are filled and shallower traps in the doped layers may be at least partially filled. With increasing forward bias, additional traps closer to the center of the intrinsic layer will be filled by electrons. The band diagram indicates that under our measurement condition, electron traps with activation energy greater than 0.46 eV will be detected only if they are located in the intrinsic layers. Similar conclusions can be obtained for hole traps. However, due to the heavier doping in the *p*-type layer, a hole trap with activation greater than 0.17 eV can be detected only when it is located in the intrinsic region. *This explains why no traps were observed in the HT_g GaAs p-i-n sample, although the 0.57 eV hole traps are observed in p-type GaAs grown at standard temperature.*

Table 8.8 The spatial location of deep levels than can be detected in the 4.7% *p-i-n* sample under these measurement conditions

Settings	Location of Electron traps	Location of Hole traps
V_R = -1 V; V_p = 0 V	$E_A \leq 0.46$ eV *n*-type and *i*-layers	$E_A \leq 0.17$eV *p*-type and *i*-layers
	$E_A \geq 0.46$ eV only in *i*-layers	$E_A > 0.17$ eV only in *i*-layers
V_R = -1 V; $V_p > 0$ V	Can fill shallower traps in all layers than when V_p = 0 V	Can fill shallower traps in all layers than when V_p = 0 V

8.4 Discussion of defects

To summarize, all the defects found in the *p-i-n* samples are listed in Table 8.9. Because the traps observed when there is no injection current are deep in the band gap, they must be located in the intrinsic GaAs layers grown at low temperature. The traps seen only when

there is injection current are likely located in the *i*-layers grown at about 300^0C; however, if they are shallow enough they could also be minority carrier traps located in the doped layers.

Table 8.9 Summary of traps found in *p-i-n* structures. The traps indicated by gray shading are seen only when there is injection current.

Sample			GaAs HT_g	GaAs LT_g	1.4% Bi	1.8% Bi	4.7% Bi
Majority Carrier Trap	0.22eV (NB5)	N_T (cm^{-3})			1.5×10^{14} (e) 9.9×10^{13} (h)		
		σ (cm^2)			9.5×10^{-16} (e) 4.7×10^{-17} (h)		
	0.29eV (NG1≠NB8)	N_T (cm^{-3})		1.0×10^{15} (e) 9.5×10^{14} (h)		2.4×10^{14} (e) 1.5×10^{14} (h)	
		σ (cm^2)		8.9×10^{-17} (e) 4.5×10^{-18} (h)		4.7×10^{-14} (e) 2.3×10^{-15} (h)	
	0.33eV (NB4)	N_T (cm^{-3})			3.9×10^{14} (e) 2.6×10^{14} (h)		
		σ (cm^2)			8.2×10^{-14} (e) 4.1×10^{-15} (h)		
	0.37eV (NB3=NB7?)	N_T (cm^{-3})			1.3×10^{14} (e) 8.4×10^{13} (h)	4.3×10^{14} (e) 2.3×10^{14} (h)	
		σ (cm^2)			2.2×10^{-14} (e) 1.1×10^{-15} (h)	7.2×10^{-15} (e) 3.6×10^{-16} (h)	
	0.41eV (NB6)	N_T (cm^{-3})				1.5×10^{15} (e) 8.2×10^{14} (h)	
		σ (cm^2)				8.4×10^{-15} (e) 4.2×10^{-16} (h)	
	0.56eV (NB2=NB10)	N_T (cm^{-3})			3.4×10^{14} (e) 1.7×10^{14} (h)		2.6×10^{15} (e) 2.4×10^{15} (h)
		σ (cm^2)			5.0×10^{-14} (e) 2.5×10^{-15} (h)		1.8×10^{-13} (e) 8.9×10^{-15} (h)
	0.63eV (NB1)	N_T (cm^{-3})			9.9×10^{14} (e) 5.1×10^{14} (h)	6.7×10^{15} (e) 2.9×10^{15} (h)	
		σ (cm^2)			2.8×10^{-14} (e) 1.4×10^{-15} (h)	1.8×10^{-14} (e) 8.9×10^{-16} (h)	
	0.73eV (NB9)	N_T (cm^{-3})					2.0×10^{15} (e) 1.8×10^{15} (h)
		σ (cm^2)					7.3×10^{-13} (e) 3.7×10^{-14} (h)
Minority Trap	0.32eV (PB1)	N_T (cm^{-3})				1.2×10^{14} (e) 7.6×10^{13} (h)	
		σ (cm^2)				8.1×10^{-6} (e) 4.0×10^{-7} (h)	
	0.52eV* (PG2)	N_T (cm^{-3})		2.3×10^{15} (e) 2.1×10^{15} (h)			
		σ (cm^2)		2.0×10^{-16} (e) 1.0×10^{-17} (h)			
	0.57eV (PG1)	N_T (cm^{-3})	2.3×10^{13} (e) 1.4×10^{13} (h)				
		σ (cm^2)	1.5×10^{-14} (e) 7.0×10^{-16} (h)				

* It is not clear why a minority carrier trap is observed without injection current.

8.4.1 GaAs *p-i-n* diodes

Based on the band diagrams from the simulation, the trap PG1 found in the high T_g GaAs sample is in the intrinsic GaAs layer. Comparing it with the defects found in Table 7.9, PG1 is possibly the 0.57 eV hole trap (HS1) in *p*-type GaAs, as can also be seen in Fig. 8.8, which compares the DLTS spectra from the GaAs Schottky diodes with the spectra for the GaAs and GaAsBi *p-i-n* diodes. Since this is a minority carrier trap, one may infer that electrons are the majority carrier in the intrinsic GaAs layer of the high T_g GaAs *p-i-n* sample. This is somewhat surprising since our collaborators had expected intrinsic GaAs grown under standard conditions to be *p*-type. An *n*-type intrinsic layer could result from a memory effect in the growth chamber, since the *n*-type layer is grown immediately prior to the intrinsic layer. If the intrinsic layer is also *n*-type in the sample with a low T_g GaAs *i*-layer, then all the positive peaks are due to hole traps and the negative peak NG1 is due to an electron trap. However, DLTS peaks similar to PG2 and NG1 have not been reported in GaAs to our knowledge.

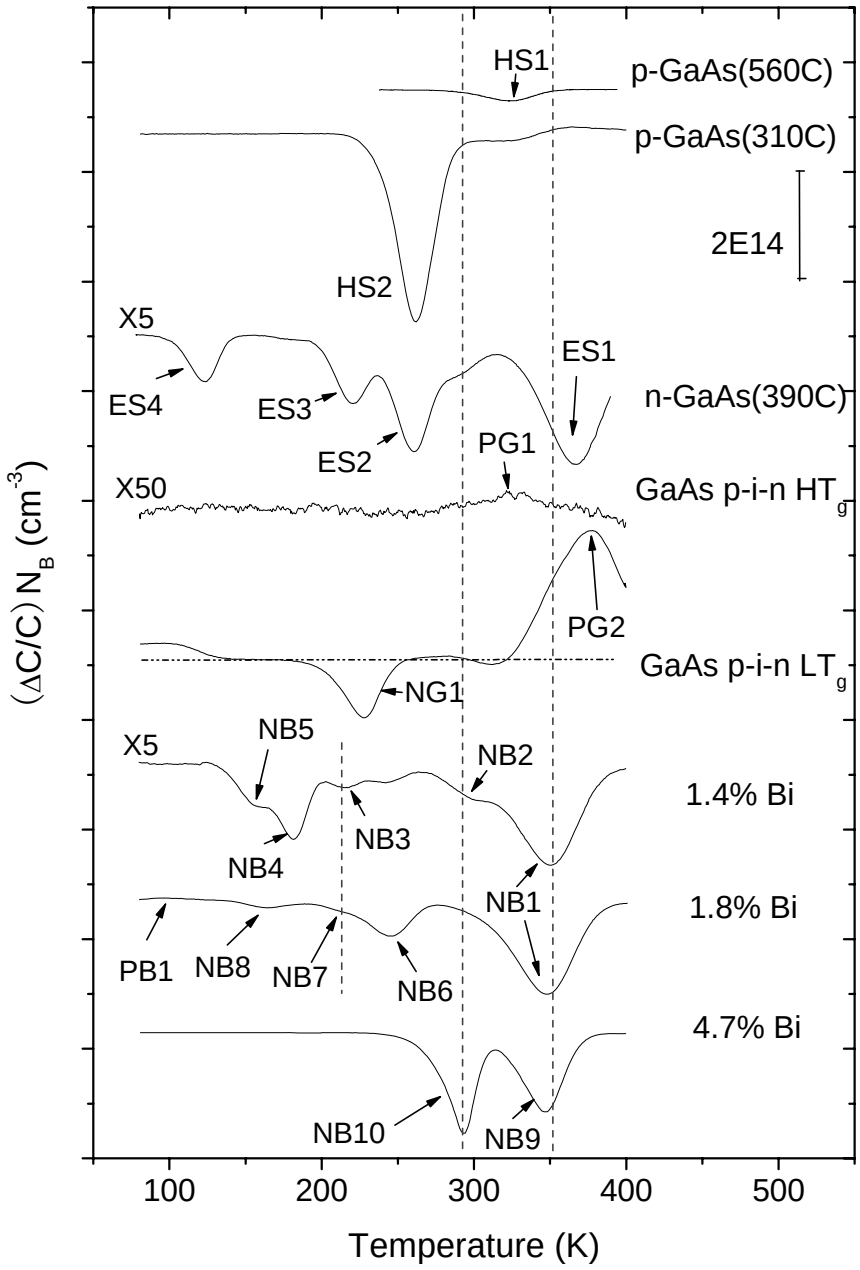


Figure 8.8 DLTS spectra of *p*-type Schottky diodes, *n*-type Schottky diodes and *p*-*i*-*n* structures taken at filling voltage at 1.5 V.

Although it was determined from the simulations that almost all the traps we found are located in the intrinsic layers, the exact location of each trap, whether it is in GaAs or $GaAs_{1-x}Bi_x$ layer, is still unknown. In addition, the majority and minority carrier in the intrinsic layers is not known; therefore, the carrier type of each trap is also not determined. However, some traps can possibly be identified.

Trap NB2 in the sample with 1.4% Bi and NB10 in the sample with 4.7% Bi may be the same trap and they have the same temperature as the little shoulder in the *n*-GaAs grown at 390 °C. By looking in the literature, NB2 and NB10 are quite similar to EL3 that is a point defect or a point-defect/impurity complex [68]. The concentration of EL3 trap varies in a wide range according to growth conditions and is easily decreased by annealing above 600 °C [68, 73].

The $GaAs_{1-x}Bi_x$ layer (and possibly a part of the intrinsic GaAs at the interface with GaAsBi) is grown in a Ga-rich environment, where the Ga_{As} anti-site is likely to form. GaAs grown at 600 °C under Ga-rich conditions has been investigated by DLTS and the second acceptor level of the Ga_{As} anti-site defect is at 0.71 eV with respect to the valence band [74]. Trap NB9 in the 4.7% Bi sample may be this hole trap (named HL2 in Ref. 61). However, if this is true, the majority carrier trap for the 4.7% bismide sample is a hole. If so, then NB10 must also be a hold trap and cannot be EL3 which is an electron trap.

From the comparison of the DLTS spectra in Fig. 8.8, the *p-i-n* diodes with a growth interrupt (GaAs *p-i-n* LT_g, 1.4% Bi, and 1.8% Bi samples) have many DLTS peaks at T < 200K, while the samples without a growth interrupt (GaAs *p-i-n* HT_g and 4.7% Bi sample) have no traps in this temperature range, suggesting that the growth interrupt may introduce these defects. We note that in the more recently grown structures the substrate temperature was ramped down during the growth of the first GaAs intrinsic layer and that a growth interrupt is therefore not necessary.

8.5 Estimated radiative and non-radiative recombination rates

All of the $GaAs_{1-x}Bi_x$ *p-i-n* samples show good photoluminescence and electroluminescence spectra, as shown in Fig. 5.6 and 5.7 for the 1.8% bismide sample. However, the luminescence intensity is about 100 times lower than that from an InGaAs/GaAs superlattice grown in the same chamber. This suggests that the defect concentrations observed by DLTS may be high enough to reduce light emission from these devices.

As discussed in section 3.1.3.2, with injection of excess carrier by light or electric field, electron and hole pairs are generated in the junction and then recombine radiatively or non-radiatively, emitting light or heat respectively. The probability that a particular electron in the conduction band recombines with a hole in the valence band is proportional to the hole concentration and vice versa for a hole in the valence band. Therefore, the radiative recombination rate R is proportional to the product of the electron and hole concentrations [75], that is,

$$R = Bnp = B\left(N_d + n'\right)\left(N_a + p'\right), \tag{8.2}$$

where n' and p' are the excess electron and hole concentration, respectively; and the constant B is called the radiative recombination coefficient. $B = 7\times10^{-10}\ cm^3/s$ for GaAs. The excess carriers are generated in pairs, so $n' = p'$. In *p-i-n* diodes, the generation and recombination process happens in the intrinsic layers of the diode, where $N_a = N_d = n_i << n' = p'$. Then Equation (8.1) is written as

$$R = Bn'^2. \tag{8.3}$$

The non-radiative recombination is described by SRH theory discussed in section 3.1.3.2 (page 27). Substituting the condition $N_a = N_d = n_i << n' = p'$ into Equation (3.11), the non-radiative recombination rate NR is written as

$$NR = \frac{np - n_i^2}{\tau_p(n+n') + \tau_n(p+p')} = \frac{1}{\tau_p + \tau_n} n', \tag{8.4}$$

where τ_p and τ_n are the lifetime of holes and electrons, respectively.

$$\frac{1}{\tau_n} = N_T \langle v_n \rangle \sigma_n, \tag{8.5}$$

and $$\frac{1}{\tau_p} = N_T \langle v_p \rangle \sigma_p, \tag{8.6}$$

with $\langle v_n \rangle$ and $\langle v_p \rangle$ the thermal velocity of carriers.

The electron-hole pair generation rate per unit volume is about $1x10^{22}$ cm^{-3}/s with a photon flux of $1x10^{18}$ cm^{-2} [76]. In the steady state, the radiative recombination rate is equal to the generation rate. Hence, from Equation (8.3) we estimate the excess carrier concentration as $n' = p' = 4 \times 10^{15} cm^{-3}$. This value of the excess carrier concentration together with the concentration and capture cross section values of the near mid-gap trap that has the highest concentration in the $GaAs_{1-x}Bi_x$ *p-i-n* diodes, NB1 in the 1.4% and 1.8% Bi sample and NB10 in the 4.7 % Bi sample, was used to calculate the probability of radiative recombination $\eta = R/(R + NR)$ [75]. Assuming these are electron traps or hole traps, the calculated radiative recombination efficiency for each sample is shown in Table 8.10.

Table 8.10 Radiative recombination efficiency of the three bismide *p-i-n* diodes assuming only the single trap which has the highest concentration and is near the mid-gap.

Sample	GaAsBi 1.4%	GaAsBi 1.8%	GaAsBi 4.7%
Electron trap	0.2% (NB1)	0.04% (NB1)	0.01% (NB10)
Hole trap	7% (NB1)	2% (NB1)	0.3% (NB10)

These values of the radiative efficiency are low. However, strong PL and EL has been observed for all these diodes. And radiative recombination is more likely to happen in the quantum well, which is the bismide layer in our case. This may indicate that the traps occurring in high concentration (NB1, NB4, NB6 and NB10) are located in the GaAs layers.

8.6 Summary

In this chapter, DLTS measurements of GaAs and $GaAs_{1-x}Bi_x$ *p-i-n* structures with bismide fraction up to 4.7% were presented. Many traps are found in the intrinsic GaAs and $GaAs_{1-x}Bi_x$ layers grown at low temperature, although the exact location and carrier type of each trap is unknown because of the complicated structure of these diodes. From the simulations of the band diagram, we conclude that all the traps we observed are located in the intrinsic layers. Trap PG1, seen in the GaAs HT_g sample, is likely to be HS1 in *p*-GaAs, which is evidence that the intrinsic GaAs layer could be slightly *n*-type. The *p-i-n* samples without a growth interrupt show no DLTS peaks at T < 200K, indicating that the growth interrupt may introduce defects. From estimates of the radiative and non-radiative recombination rates, it is clear that reducing the trap concentrations would considerably increase the radiative efficiency of these devices.

Chapter 9

Conclusions

In this study, deep levels in $GaAs_{1-x}Bi_x$ layers, GaAs layers and *p-i-n* structures containing an intrinsic $GaAs_{1-x}Bi_x$ quantum well with bismide fraction ≤ 5% were investigated using the DLTS technique. These are the first DLTS measurements of GaAsBi. The epitaxial layers were grown by MBE in the temperature range 285-580 °C by the Tiedje group. Due to poor surface morphology, the characteristics of the $GaAs_{1-x}Bi_x$ Schottky diodes were poor and the trap parameters obtained from the DLTS measurements of these samples are unphysical and not reliable. Therefore, *p-i-n* structures, some having a GaAs *i*-layer and some having a $GaAs_{1-x}Bi_x$ quantum well in the *i*-layer, were measured. In addition, several Schottky diodes fabricated from GaAs layers grown at different temperatures were also measured to help interpret the DLTS spectra of the *p-i-n* diodes.

Trap HS1 was found in both high and low T_g p-GaAs layers. A trap having similar properties was observed in GaAs samples after Fe diffusion, suggesting that it is likely related to Fe impurities [63]. Traps in *n*-type GaAs layers are observed only in low T_g samples. ES2, ES4 and ES5 are commonly seen in MBE grown GaAs, probably related to a Ga vacancy or an As interstitial [68-70].

DLTS spectra from the *p-i-n* diodes vary with the growth conditions and the bismide fraction from 0 to 4.7%. From simulations of the band diagram of these devices, it is concluded that all the traps observed are located in the intrinsic GaAs or $GaAs_{1-x}Bi_x$ layers

grown at ~300 ºC. The traps we found in the *p-i-n* structures are all in concentrations less than $7x10^{15}$ cm^{-3}, and PL and EL spectra showing emission from the $GaAs_{1-x}Bi_x$ layers have been obtained [24, 50]. This indicates that $GaAs_{1-x}Bi_x$ may be useful for a variety of high performance electronic and optoelectronic devices. However, device performance will very likely be improved, if the deep level defect concentrations can be reduced.

A device structure more suitable for DLTS measurements than these symmetric *p-i-n* diodes is needed to further investigate the defects in $GaAs_{1-x}Bi_x$ layers. Since the thick $GaAs_{1-x}Bi_x$ layers have a surface morphology problem due to droplet formation at these growth conditions, a one-sided *p-n* junction containing a thin $GaAs_{1-x}Bi_x$ quantum well on the lightly doped side may be a good choice for the next DLTS experiments. Continued investigation of GaAs layers gown at T < 400ºC would also be important, since device structures fabricated incorporating $GaAs_{1-x}Bi_x$ layers will likely also incorporate GaAs layers grown at the same temperature.

Bibliography

[1] D. A. Neamen. *Semiconductor Physics and Devices: Basic Principle*. McGraw-Hill Press, Third Edition, 2003.

[2] S. M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices*. John Wiley & Sons Ltd., Third Edition, 2007.

[3] Dieter K. Schroder. *Semiconductor Material and Device Characterization*. John wiley & Sons Ltd., Third Edition, 2006.

[4] P. Blood and J. W. Orton. *The Electrical Characterization of Semiconductors: Majority Carriers and Electron States*. Academic Press Inc., 1992.

[5] D. V. Lang. Deep-level transient spectroscopy: A new method to characterize traps in semiconductors. *Journal of Applied Physics*, 45: 3023-3032, 1974.

[6] G. Qin and M. Yan. Deep-level defects and deep-level transient spectroscopy. *Physics*, 14: 422-428, 1985.

[7] L. C. Kimerling, Influence of deep traps on the measurement of free-carrier distributions in semiconductors by junction capacitance techniques. *Journal of Applied Physics*, 45: 1839-1845, 1974.

[8] P. M. Mooney. Defect identification using capacitance spectroscopy. *Semiconductor and Semimetals*, 51B: 93-152, 1999.

[9] SULA Technologies, Deep Level Transient Spectrometer: User's Manual

[10] Xudong Chen, 2008. Private communication.

[11] Y. Zhang, B. Fluegel, M. C. Hanna, A. Mascarenhas, L. W. Wang, Y. L. Wang, and X. Wei. Impurity perturbation to the host band structure and recoil of the impurity state. *Physical Review B*, 68: 075210, 2003.

[12] A. Rubio and M. L. Cohen. Quasiparticle excitations in $GaAs_{1-x}N_x$ and $AlAs_{1-x}N_x$ordered alloys. *Physical Review B*, 51: 4343-4346, 1995.

[13] J. Neugebauer and C. G. Vandewalle. Electronic structure and phase stability of $GaAs_{1-x}N_x$alloys. *Physical Review B*, 51: 10568-10571, 1995.

[14] S. H. Wei and A. Zunger. Giant and composition-dependent optical bowing coefficient in GaAsN alloys. *Physical Review Letters*, 76: 664-667, 1996.

[15] J. D. Perkins, A. Mascarenhas, Y. Zhang, J. F. Geisz, D. J. Friedman, J. M. Olson, and S. R. Kurtz. Nitrogen-activated transitions, level repulsion, and band gap reduction in $GaAs_{1-x}N_x$ with $x<0.03$. *Physical Review Letters*, 82: 3312-3315, 1999.

[16] W. Shan, W. Walukiewicz, J. W. Ager, E. E. Haller, J. F. Geisz, D. J. Friedman, J. M. Olson, and S. R. Kurtz. Band anticrossing in GaInNAs alloys. *Physical Review Letters*, 82: 1221-1224, 1999.

[17] P. R. C. Kent and A. Zunger. Evolution of III-V nitride alloy electronic structure: the localized to delocalized transition. *Physical Review Letters*, 86: 2613-2616, 2001.

[18] A. Janotti, Su-Huai Wei, and S. B. Zhang. Theoretical study of the effects of isovalent coalloying of Bi and N in GaAs. *Physical Review B*, 65: 115203, 2002.

[19] M. A. Berding, A. Sher, A. B. Chen, and W. E. Miller. Structural properties of bismuth-bearing semiconductor alloys. *Journal of Applied Physics*, 63: 107-116, 1988.

[20] K. Oe and H. Okamoto. New semiconductor alloy $GaAs_{1-x}Bi_x$ grown by metal organic vapour phase epitaxy. *Japanese Journal of Applied Physics*, 37: L1283-L1285, 1998.

[21] K. Oe. Characteristics of semiconductor alloy $GaAs_{1-x}Bi_x$. *Japanese Journal of Applied Physics*, 41: 2801-2806, 2002.

[22] S. Tixier, M. Adamcyk, T. Tiedje, S. Francoeur, A. Mascarenhas, P. Wei, and F. Schiettekatte. Molecular beam epitaxy growth of $GaAs_{1-x}Bi_x$. *Applied Physics Letters*, 82: 2245-2247, 2003.

[23] S. Francoeur, S. Tixier, E.C. Young, T.Tiedje, and A. Mascarenhas. Bi isoelectronic impurities in GaAs. *Physical Review B*, 77: 085209, 2008.

[24] R.B. Lewis, D.A. Beaton, Xianfeng Lu, and T. Tiedje. $GaAs_{1-x}Bi_x$ light emitting diodes. *Journal of Crystal Growth*, 311: 1872-1875, 2009.

[25] Xianfeng Lu, D.A. Beaton, R. B. Lewis, T.Tiedje, and Yong Zhang. Composition dependence of photoluminescence of $GaAs_{1-x}Bi_x$ alloys. *Applied Physics Letters*, 95: 041903, 2009.

[26] V. Pacebutas, K. Bertulis, L. Dapkus, G. Aleksejenko, A. Krotkus, K. M. Yu, and W. Walukiewicz. Characterization of low-temperature molecular-beam-epitaxy grown GaBiAs layers. *Semiconductor Science Technology*, 22: 819-823, 2007.

[27] M. Yoshimoto, S. Murata, A. Chayahara, Y. Horino, J. Saraie, and K. Oe. Metastable GaAsBi alloy grown by molecular beam epitaxy. *Japanese Journal of Applied Physics*, 42: L1235-L1237, 2003.

[28] A. Mascarenhas, Y. Zhang, J. Verley, and M. J. Seong. Overcoming limitations in semiconductor alloy design. *Superlattices Microstructure*, 29: 395-404, 2001.

[29] R. B. Lewis, M. Masnadi-Shirazi, D. A. Beaton, M. J. Fryer, X. Lu, and T. Tiedje. Surface reconstructions and bismuth incorporation in $GaAs_{1-x}Bi_x$ Alloys. http://meetings.aps.org/link/BAPS.2010.MAR.W25.12, APS 2010.

[30] Yong Zhang, A. Mascarenhas, and L. W. Wang. Similar and dissimilar aspects of III-V semiconductors containing Bi versus N. *Physical Review B*, 155201, 2005.

[31] K. Oe and H. Asai. Proposal on a temperature insensitive wavelength semiconductor laser. *IEICE Transactions on Electronics*, E97-c: 1751-1759, 1996.

[32] Y. Takehara, M. Yoshimoto, W. Huang, J. Saraie, K. Oe, A. Chayahara, and Y. Horino. Lattice distortion of GaAsBi alloy grown on GaAs by molecular beam epitaxy. *Japanese Journal of Applied Physics*, 45: 67-69, 2006.

[33] J. Yoshida, T. Kita, O. Wada, and K. Oe. Temperature dependence of $GaAs_{1-x}Bi_x$ band gap studied by photoreflectance spectroscopy. *Japanese Journal of Applied Physics*, 42: 371-374, 2003.

[34] S. Francoeur, M. J. Seong, A. Mascarenhas, S. Tixier, M. Adamcyk, and T. Tiedje. Band gap of $GaAs_{1-x}Bi_x$, $0<x<3.6\%$. *Applied Physics Letters*, 82: 3874-3876, 2003.

[35] E. C. Young. *GaNAs and GaAsBi: Structural and electronic properties of two resonant state semiconductor alloys*. PhD Thesis, University of British Columbia, 2006.

[36] S. Adachi. *Physical properties of III-V Semiconductor Compounds,* chapter1 and chapter 4. John Wiley & sons, Ltd., 1992.

[37] M. Ferhat and A. Zaoui. Structural and electronic properties of III-V bismuth compounds. *Physical Review B*, 73: 115107, 2006.

[38] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan. Band parameters for III–V compound semiconductors and their alloys. *Journal of Applied Physics*, 89: 5815-5875, 2001.

[39] S. Tixier, S. E. Webster, E. C. Young, T. Tiedje, S. Francoeur, A. Mascarenhas, P. Wei, and F. Schiettekatte. Band gaps of the dilute quaternary alloys $GaN_xAs_{1-x-y}Bi_y$ and $Ga_{1-y}In_yN_xAs_{1-x}$. *Applied Physics Letters*, 86: 112113, 2005.

[40] D. Madouri, A. Boukra, A.Zaoui, and M. Ferhat. Bismuth alloying in GaAs: a first-principles study. *Computational Materials Science*, 43: 818-822, 2008.

[41] E. Iliopoulos, A. Adikimenakis, C. Giesen, M. Heuken, and A. Georgakilas. Energy bandgap bowing of InAlN alloys studied by spectroscopic ellipsometry. *Applied Physics Letters*, 92: 191907, 2008.

[42] R. Kudrawiec, M. Syperek, P. Poloczek, J. Misiewicz, R. H. Mari, M. Shafi, M. Henini, Y. Galvão Gobato, S. V. Novikov, J. Ibáñez, M. Schmidbauer, and S. I. Molina. Carrier localization in GaBiAs probed by photomodulated transmittance and photoluminescence. *Journal of Applied Physics*, 106: 023518, 2009.

[43] J. Shen, S. Y. Ren, and J. D. Dow. Relaxed-lattice model of isolated and paired isoelectronic traps in GaP. *Physical Review B*, 42: 9119-9126, 1990.

[44] F. Trumbore, M. Gershenzon, and D. Thomas. Luminescence due to the isoelectronic substitution of bismuth for phosphorus in gallium phosphide. *Applied Physics Letters*, 9, 4-6, 1966.

[45] P. Dean, A. White, E. W. Williams, and M. Astles. The isoelectronic trap bismuth in indium phosphide. *Solid State Communication*, 9: 1555-1558, 1971.

[46] R.N. Kini, A. Mascarenhas, R. france, and A. J. Ptak. Low temperature photoluminescence from dilute bismides. *Journal of Applied Physics*, 104: 113534, 2008.

[47] T. Tiedje, E. C. Young, and A. Mascarenhas. Growth and properties of the dilute bismide semiconductor $GaAs_{1-x}Bi_x$ a complementary alloy to the dilute nitrides *International Journal of Nanotechnology*, 5: 963-983, 2008.

[48] R. N. Kini, L. Bhusal, A. J. Ptak, R. France, and A. Mascarenhas. Electron Hall mobility in GaAsBi. *Journal of Applied Physics*, 106: 043705, 2009.

[49] D. A. Beaton, R. B Lewis, M. Masnadi-Shirazi, and T. Tiedje. Temperature dependence of hole mobility in $GaAs_{1-x}Bi_x$ alloys. *Unpublished paper*, 2010.

[50] R. B. Lewis, 2010. Private communiacation.

[51] T. Miyamoto, K. Takeuchi, F. Koyama, and K. Iga. A novel GaInNAs-GaAs quantum-well structure for long-wavelength semiconductor lasers. *IEEE Photonics Technology Letters*, 9: 1448-1450, 1997.

[52] Sarah R. Kurtz, D. Myers, and J. M. Olson. Projected performance of three- and four-junction devices using GaAs and GaInP. in *Proceedings of the 26th IEEE photovoltaics Specialist Conference*, 875-878, 1997.

[53] D.J. Friedman, J.F. Geisz, S.R. Kurtz, and J.M. Olson. 1-eV solar cells with GaInNAs active layer. *Journal of Crystal Growth*, 195: 409-415, 1998.

[54] J.F. Geisz, D.J. Friedman, J.M. Olson, S.R. Kurtz, and B.M. Keyes. Photocurrent of 1 eV GaInNAs lattice-matched to GaAs. *Journal of Crystal Growth*, 195: 401-408, 1998.

[55] Steven R. Kurtz, A.A. Allerman, E.D. Jones, J.M. Gee, J.J. Banas, and B.E. Hammons. InGaAsN solar cells with 1.0 eV band gap, lattice matched to GaAs. *Applied Physics Letters*, 74: 729-731, 1999.

[56] P. M. Asbeck, R. J. Welty, C. W. Tu, H. P. Xin, and R. E. Welser. Heterojunction bipolar transistors implemented with GaInNAs materials. *Semiconducor Science Technology*, 17: 898-906, 2002.

[57] K. L. Lew, S. F. Yoon, H. Wang, S. Wicaksono, J. A. Gupta, and S. P. McAlister. GaAsNSb-base GaAs heterojunction bipolar transistor with a low turn-on voltage. *Journal of Vacuum Science Technology B*, 24: 1308-1310, 2006.

[58] Ichiro Hase. Heterojunction bipolar transistor with a base layer that contains bismuth. US Patent #7,009,225, 2006.

[59] F. D. Auret and M. Nel. Deep level transient spectroscopy of hole defects in bulk-grown p-GaAs using Schottky barrier diodes. *Applied Physics Letters*, 48: 130-132, 1986.

[60] M. Gooyers, 2010. Private communication.

[61] M. C. Chen, D. V. Lang, W. C. Dautremont-Smith, A. M. Sergent, and J. P. Harbison. Effects of leakage current on deep level transient spectroscopy. *Applied Physics Letters*, 44: 790-792, 1984

[62] A. Mitonneau, G. M. Martin, and A. Mircea. Hole traps in bulk and epitaxial GaAs crystals. Electronics Letters, 13 : 666-668, 1977.

[63] D. V. Lang, and R. A. Logan. A study of deep levels in GaAs by capacitance spectroscopy. Journal of Electronic Materials, 4: 1053-1066, 1976.

[64] P. K. Bhattacharya, H.-J. Bühlmann, M. Ilegems, and J. L. Staehli. Impurity and defect levels in beryllium-doped GaAs grown by molecular beam epitaxy. Journal of Applied Physics, 53: 6391-6398, 1982.

[65] M. Kleverman, P. Omling, L-Å. Ledebo, and H. G. Grimmeiss. Electrical properties of Fe in GaAs. Journal of Applied Physics, 54: 814-819, 1983.

[66] I. Koslow. Study of defects in GaAsN. BSc honour thesis, University of British Columbia, 2006.

[67] J. Lagowski, D. G. Lin, T. P. Chen, M. Skowronski, and H. C. Gatos. Native hole trap in bulk GaAs and its association with the double-charge state of the arsenic antisite defect. Applied Physics Letters, 47: 929-931, 1985.

[68] G.M. Martin, A. Mitonneau, and A. Mircea. Electron traps in bulk and epitaxial GaAs crystals. Electronics Letters, 13: 191-193, 1977.

[69] D. V. Lang, A. Y. Cho, A. C. Gossard, M. Ilegems, and W. Wiegmann. Study of electron traps in *n*-GaAs grown by molecular beam epitaxy. Journal of Applied Physics, 47: 2558-2564, 1976.

[70] A. Mircea and A. Mitonneau. A study of electron traps in vapour-phase epitaxial GaAs. Applied Physics A: Material Sciences and Processing, 8: 15-21, 1975.

[71] Nextnano software, next generation 3D nano device simulator, Copyright © 1999-2008, Walter Schottky Institutes, http://www.nextnano.de/nextnano3/index.htm.

[72] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis, and P. Vogl. nextnano: General Purpose 3-D Simulations. IEEE Transactions on Electron Devices, 54: 2137-2142, 2007.

[73] A. Mircea, A. Mitonneau, L. Hollan, and A. Brière. Outdiffusion of deep electron traps in epitaxial GaAs. Applied Physics A: Material Sciences and Processing, 11: 153-158, 1976.

[74] P. Krispin, S. G. Spruytte, J. S Harris, and K. H Ploog. Origin and annealing of deep-level defects in p-type GaAs/Ga(As,N)/GaAs heterostructures grown by molecular beam epitaxy. Journal of Applied Physics, 89: 6294-6301, 2001.

[75] E. Fred Schubert. Light-emitting diodes, chapter 2. Cambridge University Press, Cambridge, 2003.

[76] T. Tiedje, 2010. Private communication.