High-performance solution-processed polymer ferroelectric field-effect transistors

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We demonstrate a rewritable, non-volatile memory device with flexible plastic active layers deposited from solution. The memory device is a ferroelectric field-effect transistor (FeFET) made with a ferroelectric fluoropolymer and a bisalkoxy-substituted poly(*p*-phenylene vinylene) semiconductor material. The on- and off-state drain currents differ by several orders of magnitude, and have a long retention time, a high programming cycle endurance and short programming time. The remanent semiconductor surface charge density in the on-state has a high value of 18 mC m^{-2}, which explains the large on/off ratio. Application of a moderate gate field raises the surface charge to 26 mC m^{-2}, which is of a magnitude that is very difficult to obtain with conventional FETs because they are limited by dielectric breakdown of the gate insulator. In this way, the present ferroelectric–semiconductor interface extends the attainable field-effect band bending in organic semiconductors.

A memory element based on the ferroelectric field-effect transistor (FeFET) is attractive because of its non-volatile data retention, small size, rewritability, non-destructive read-out, low-voltage operation and short programming time[1]. Its functionality arises from the attenuation of the charge carrier concentration in the semiconductor by the ferroelectric polarization of the gate insulator. Even though inorganic FeFETs have been studied for decades, a memory performance of any practical value has been achieved only in recent years[2–8]. The main problems that have arisen are charge trapping at the ferroelectric–semiconductor interface and the lack of thermal stability of the interface. This has prompted the use of insulating buffer layers between the semiconductor and ferroelectric to prevent charge injection and protect the semiconductor from the high-temperature annealing procedure that is required for inorganic ferroelectrics. Crucial device parameters for all memory devices are the on/off ratio, data retention time, programming cycle endurance and programming time. Current state-of-the-art inorganic FeFETs have on/off ratios up to 10^9, a retention time of 16 days and a programming time of 10^{-8} s (refs 5,8). This is promising, although the high production cost of this non-CMOS (complementary metal-oxide-semiconductor) technology may hinder widespread application.

Organic field-effect transistors are ideally suited for low-cost, low-performance logic circuit applications on flexible substrates[9]. There is currently a need for an electrically addressable non-volatile memory technology that can be put into organic integrated circuits[10,11]. An interesting option is to make organic FeFETs because of the similarity of the processing procedure and the advantages mentioned above. Small memory effects with an on/off ratio up to nine have been demonstrated by combining the inorganic ferroelectric $Pb(Zr,Ti)O_3$ with evaporated organic semiconductors pentacene and sexithiophene[12,13]. Recently, FeFETs with organic active layers have also been demonstrated, invariably with the use of evaporated pentacene as the semiconductor material[14–16]. Schroeder *et al.*[14] demonstrated an on/off ratio of 200 at 2.5 V gate bias, 30 at zero gate bias and a retention time of three hours. The programming time, estimated from the reported ferroelectric switching current duration, exceeds 200 ms. Unni *et al.*[15] obtained a similar on/off ratio and retention time.

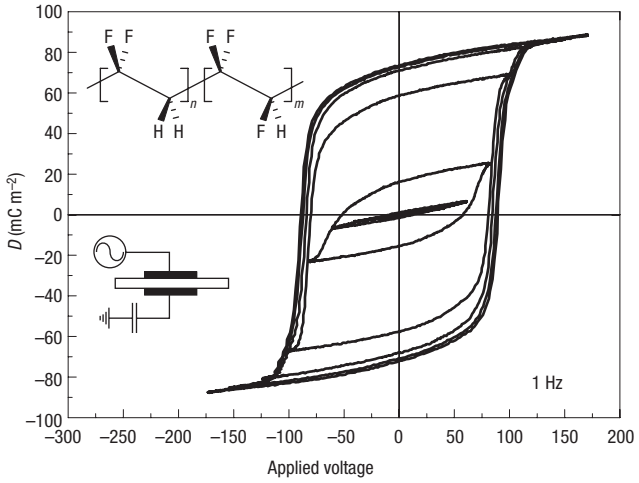

Figure 1 Ferroelectric hysteresis loops of a P(VDF/TrFE) polymer capacitor device. These were measured on a 1.7-μm-thick layer using a Sawyer–Tower circuit as shown in the inset at a 1-Hz applied voltage frequency. The chemical formula of P(VDF/TrFE) is shown in the all-trans configuration that defines its ferroelectric crystalline phase.

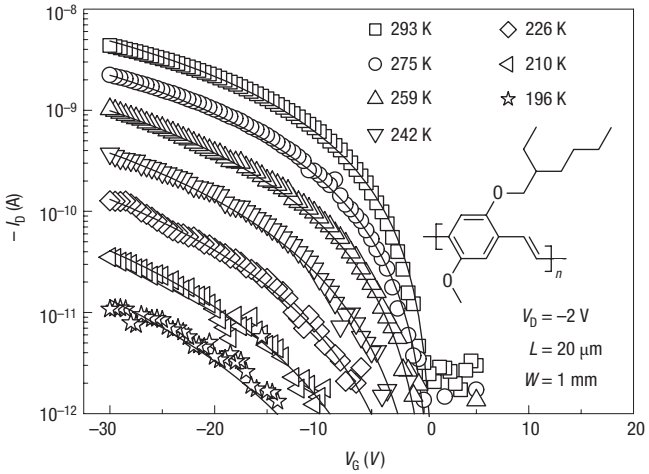

Figure 2 Transfer characteristics as a function of temperature of MEH-PPV FETs (symbols) and the modelling result (lines). The chemical formula of MEH-PPV, drain voltage V_D, source–drain gap width W and length L are included. The insulator capacitance per area C_i was 10 nF cm^{-2}.

Although both results were obtained with ferroelectric materials, neither report proves that the memory functionality is driven by ferroelectricity and not by a secondary effect such as charge trapping. This would have been demonstrated by, for example, a sudden rise in the drain current when the gate field reached the coercive field of the ferroelectric insulator layer. (The gate field applied in the transfer curve measurement by Unni *et al.* is much lower than the coercive field of their ferroelectric material[17]. Schroeder *et al.* do not mention the thickness of the gate insulator film or the coercive voltage.) The coercive field of a ferroelectric is where its hysteresis loop in a plot of charge displacement versus applied field, D–E, passes zero D, so it is the minimum field required to reverse the full ferroelectric polarization. Matsuo *et al.*[16] have reported the expected drain current increase at around the coercive voltage and a data retention time of a week, but the on- and off-states after this time differ only by a factor of 0.5.

Here we study high-performance solution-processed polymer FeFETs consisting of a poly(vinylidene fluoride/trifluoroethylene) (P(VDF/TrFE)) ferroelectric copolymer as gate insulator and poly[2-methoxy, 5-(2′-ethyl-hexyloxy)-*p*-phenylene-vinylene] (MEH-PPV) as a semiconductor. P(VDF/TrFE) is a wide-bandgap insulator and a ferroelectric material[17]. Its annealing temperature is 140 °C, which is compatible with flexible substrate materials such as polyimide[18]. MEH-PPV is a p-type semiconductor whose charge transport is characterized by site-to-site hopping[19]. Of the two polymers, only the PPV-polymer is not entirely air-stable. By sealing it properly, however, it can be made stable enough for commercial application, as shown by the use of PPV-polymers for LED displays in currently available products. The polymer FeFETs have a remanent on/off ratio of several orders of magnitude at zero gate bias, a long data retention time, a high programming cycle endurance and a short programming time. The high on/off ratio mainly originates from the large on-current in the semiconducting channel which is indicative of a large surface charge density ρ. This ρ value was determined by comparing the current response of non-ferroelectric and ferroelectric FETs, as previously proposed[20]. From this analysis we derive a remanent ρ value of 18 mC m^{-2}, which is one quarter of the remanent polarization of the ferroelectric. Application of a moderate gate field raises ρ to 26 mC m^{-2}, which exceeds the values accessible in conventional FETs, because they are limited by breakdown of the gate insulator at high fields.

First, the ferroelectric properties of the P(VDF/TrFE) copolymer are characterized. Figure 1 shows typical hysteresis loops for a capacitor at several voltages. The thickness of the P(VDF/TrFE) layer amounts to 1.7 μm, the coercive voltage is 90 V and the remanent polarization value is 74 mC m^{-2}. The voltage required to switch the ferroelectric polarization can be reduced to 5 V without loss of ferroelectric properties by decreasing the ferroelectric layer thickness[21].

As a next step, the field-effect properties of MEH-PPV are characterized using FETs with lithographically patterned gold electrodes and a standard polymer lithographic resist material as the gate dielectric[9]. Transfer curves (drain current I_D as a function of gate voltage V_G) at various temperatures are shown in Fig. 2. The field-effect mobility amounts to 2.4×10^{-4} cm^2 V s^{-1} at $V_G = -29$ V and room temperature. When the transistor is biased in the hole-accumulation mode ($V_G < 0$), the current can be described by a model based on hopping of charge carriers in an exponential density of states[19,22]:

$$I_D = \frac{WV_D\,\varepsilon_o\,\varepsilon_r\,\sigma_o}{Le}\left(\frac{T}{2T_o - T}\right) \times \sqrt{\frac{2k_B T_o}{\varepsilon_o\,\varepsilon_r}}\left[\frac{\left(\frac{T_o}{T}\right)^4 \sin\left(\pi\frac{T}{T_o}\right)}{(2\alpha)^3 B_c}\right]^{\frac{T_o}{T}} \times \left\{\sqrt{\frac{\varepsilon_o\,\varepsilon_r}{2k_B T_o}}\left[\frac{C_i\,(V_G - V_{so})}{\varepsilon_o\,\varepsilon_r}\right]\right\}^{\frac{2T_o}{T}-1} \quad (1)$$

with L and W the length and width of the channel, V_D the drain voltage, $\varepsilon_0\varepsilon_r$ the dielectric constant of the semiconductor, e the elementary charge, k_B the Boltzmann constant, T_0 the width of the exponential density of states for holes, B_c a critical number for

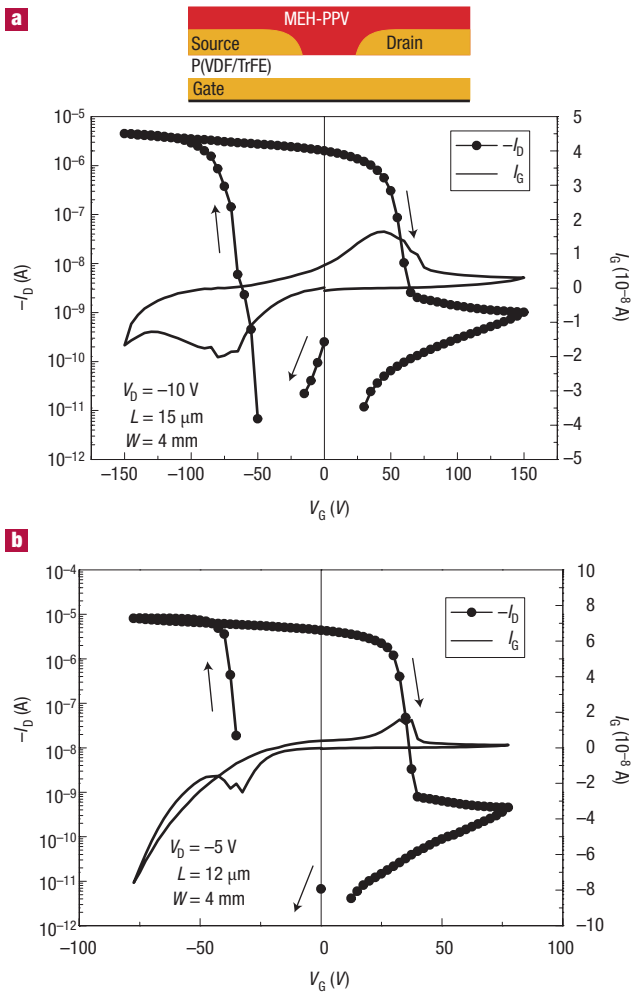

Figure 3 Hysteretic drain current as a function of gate voltage for polymer FeFETs. The ferroelectric layer thickness is 1.7 μm in **a** and 0.85 μm in **b**. The arrows show the clockwise hysteresis of the drain current consistent with accumulation and depletion of p-type charge carriers. The FeFETs had previously been brought into the off-state.

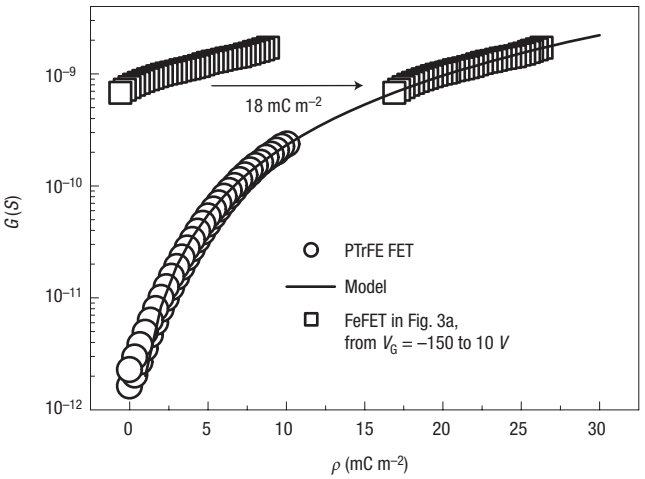

Figure 4 Channel conductance G versus surface charge density ρ for a PTrFE FET, the model derived from it and the method of calculating the remanent ρ in a polymer FeFET. G is defined as $(LI_D)/(WV_D)$, with drain current I_D, drain voltage V_D, source–drain gap length L and width W. The ρ values of the PTrFE FET are calculated by multiplying the measured C_i of 6.7 nF cm^{-2} with the applied gate voltage. The model curve was calculated using equation (1), the parameters derived from Fig. 2 and an adjusted σ_0 of 8.2×10^6 S m^{-1}. The FeFET data points are from Fig. 3a at gate voltages of –150 to 10 V, using a measured C_i of 5.9 nF cm^{-2}. The horizontal shift of 18 mC m^{-2} that is applied illustrates the method of obtaining the estimate for the remanent ρ value.

the onset of a percolating conduction path of 2.8, α^{-1} the effective overlap parameter between localized states, C_i the insulator capacitance per unit area of 10 nF cm^{-2}, and V_{so} the switch-on voltage. Using equation (1) to model the transfer characteristics yields $T_0 = 450$ K, $\alpha^{-1} = 9.3 \times 10^{-11}$ m, a conductivity pre-factor of $\sigma_0 = 2 \times 10^7$ S m^{-1} and a switch-on voltage $V_{so} = 0$ V (Fig. 2, solid lines).

Having characterized the ferroelectric properties of P(VDF/TrFE) and semiconductor properties of MEH-PPV, we combine the two in FeFETs. Figure 3 shows the transfer curves of two polymer FeFETs with a ferroelectric layer thickness of 1.7 and 0.85 μm. The application of a negative gate bias results in a sharp increase by several orders of magnitude of the channel current associated with hole accumulation and a remanent on-state current after bringing the bias back to zero. When compared with the previous FET experiment, the magnitude of this current suggests the presence of a high surface charge density in the semiconductor channel. Subsequently applying a positive gate bias results in current pinch-off and a remanent off-state. The remaining drain current after pinch-off closely mimics the gate current, which indicates that it is gate insulator leakage. The loops in Fig. 3 are symmetric in the sense that the voltage at which the drain current loop crosses –10^{-8} A either upwards or downwards is about the same (the slight asymmetries are consistent with the effect of the applied drain voltage[23]). These transition voltages are ±60 V in Fig. 3a and ±35 V in Fig. 3b, so they scale with the difference in ferroelectric layer thickness. The on/off ratio was 10^3 or higher for all the prepared devices.

Two features in Fig. 3a and b that prompt detailed explanation are the asymmetry of the gate current at high gate voltages and the non-closed drain current loop where the gate voltage returns to zero. The asymmetry arises because in accumulation the unpatterned semiconductor layer is a leakage path between the source–drain and gate electrodes. The non-closed loop is brought forth by the dielectric response of the gate insulator capacitance rather than the channel conductance. Because we use a shadow-mask technique for patterning the electrodes, the overlap of source–drain with gate is 30 times as large as the surface area of the channel, which results in a non-negligible dielectric displacement current of the insulator. As the gate voltage is brought from a positive value to zero, the gate current becomes slightly negative. This opposes normal leakage and is therefore a discharge current. The off-state current also changes sign because it is dominated by the same discharge and this causes the non-closed loop.

The surface charge density of the on-state of the FeFET can be estimated using the field-effect mobility of MEH-PPV and the measured on-state current at zero gate bias[20]. Applying the mobility parameters of equation (1) leads to a ρ value of 12 mC m^{-2} for the measurement in Fig. 3a. But such a direct comparison between this reference FET and the FeFET is not valid, because the charge carrier mobility in organic transistors decreases with increasing dielectric constant of the insulator[24]. The relative dielectric constant of the

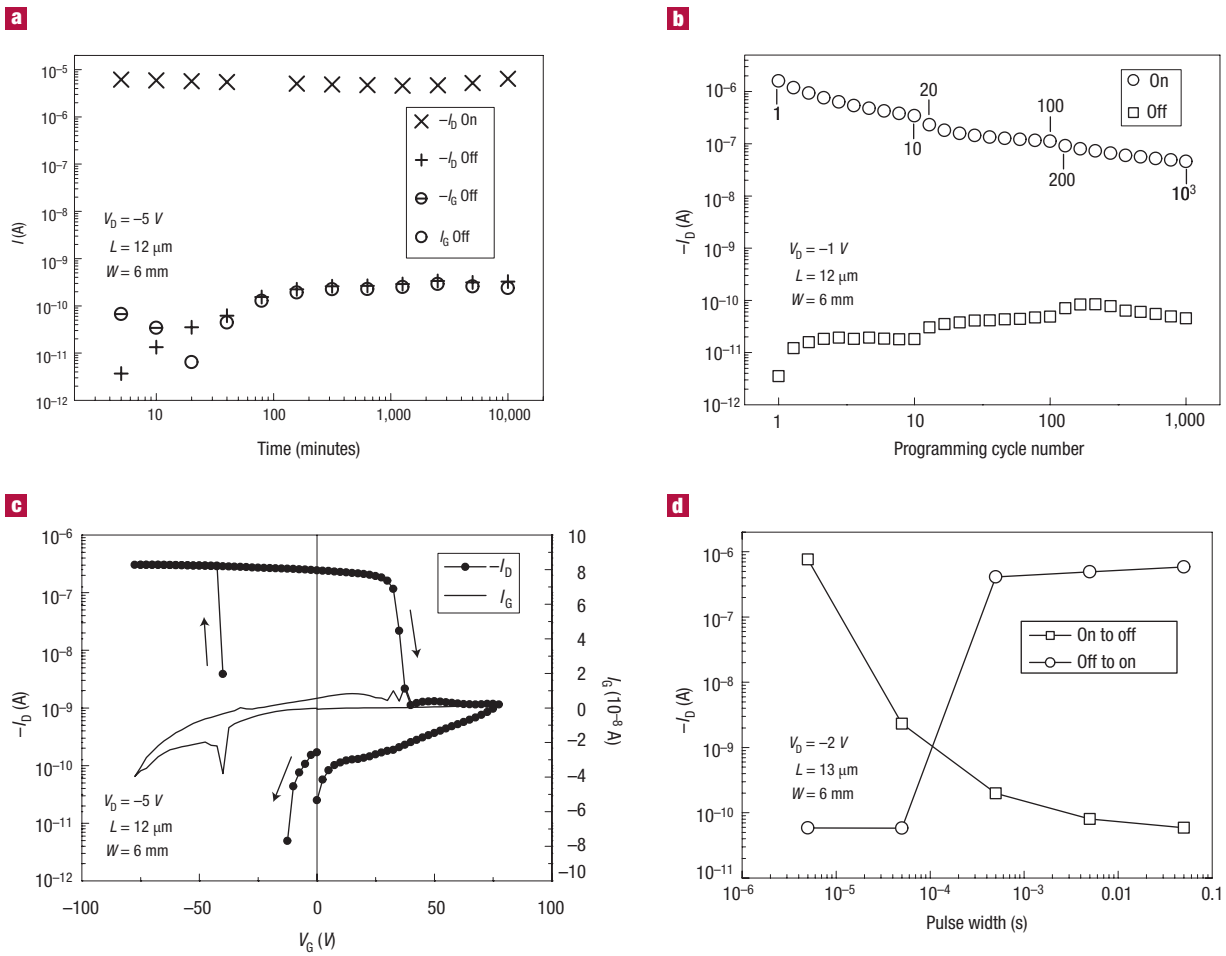

Figure 5 Data retention time, programming cycle endurance and programming time measurements. These measurements were done with a ferroelectric layer thickness of 0.85 μm. **a**, Data retention measurement obtained by programming the on- or off-state once and monitoring the drain current at zero gate bias for a week. The off-state gate current is included to explain the initial increase of the off-state drain current. The on-state gate current is insignificant with respect to the on-state drain current. Both states were attained with a gate voltage of ±77.5 V. **b**, The on- and off-state drain current at zero gate bias as a function of the number of applied gate voltage sweeps. The voltage sweep maxima were ±77.5 V. **c**, The hysteretic drain current response of the device in **b**, after the 1,000 programming cycles. **d**, Programming time measurements made by trying to change the on-state to an off-state or vice versa, with a ±85-V gate pulse of varying width. The *RC*-time of the circuit was 10^{-7} s.

gate insulator of the reference FET is 3.4 whereas the measured value for P(VDF/TrFE) was 11. To eliminate a possible mobility difference between the reference and the ferroelectric devices, non-ferroelectric FETs were made with polytrifluoroethylene (PTrFE) gate insulator. PTrFE is semicrystalline and highly polar just like the P(VDF/TrFE) copolymer, but its ferroelectric polarization is negligible[17]. Measurements of *D*–*E* curves for capacitors with a PTrFE insulator layer verified this lack of ferroelectricity. The similarity of PTrFE and P(VDF/TrFE) is also expressed in their equivalent relative dielectric constant of just above 10, as measured by impedance spectroscopy on capacitors. Figure 4 shows the good fit that was obtained for the PTrFE FET data using the model parameters obtained from the reference FET except that the conductivity prefactor σ_0 is lowered from 2×10^7 to 8.2×10^6 S m^{-1}. Such a reduction of a factor of two in the mobility closely corresponds to the decrease observed previously[24] for a dielectric constant increase from 4 to 10. Using the parameters from the PTrFE FET, the model predicts that the on-state drain current of 2 μA at zero gate bias in Fig. 3a requires a ρ of 18 mC m^{-2}. This calculation is illustrated in Fig. 4: the measured conductance values of the FeFET are shifted along the horizontal axis by 18 mC m^{-2} where they coincide with the model curve. The gate-voltage dependence of channel conductance G of the FeFET nicely follows the model curve, because of the equal dielectric constant of PTrFE and P(VDF/TrFE).

The field-effect mobility of the on-state in Fig. 3a can be obtained from the slope of the drain current at low gate biases, because there the polarization response is linear, as can be observed for the low-voltage loops in Fig. 1. The hopping-based model[19] predicts an increase in mobility when ρ is increased, because the additional charges on average start to occupy higher-energy sites and therefore require less energy for nearest-neighbour hopping transport. Using the measured C_i of 5.9 nF cm^{-2} of the FeFET we obtain a field-effect mobility of 1.3×10^{-3} cm^2 V^{-1} s^{-1}, which is five times as high as the 2.4×10^{-4} cm^2 V^{-1} s^{-1} for the data in Fig. 2 at –29 V gate bias. At the ρ value of 18 mC m^{-2} the model predicts an increase by a factor of 4 to a value of 9×10^{-4} cm^2 V^{-1} s^{-1}, close to the

measured value. This high field-effect mobility confirms the large estimate for ρ. Because of this high charge density, the on-state channel conductance is similar to or higher than those of earlier reported FeFETs with sexithiophene and pentacene, despite the fact that the mobility of MEH-PPV in conventional transistors is less than 1% of the mobility of these small molecules[12–16]. This also explains why the FeFETs with MEH-PPV have a much higher on/off ratio than reported so far.

It is important to realize that a ρ of 18 mC m^{-2} or more is only attainable in practice with ferroelectrics and high-permittivity dielectrics. Organic FET experiments are often done with thermally grown SiO_2 gate insulators with a typical thickness of 200 nm (ref. 22). These layers generally break down at 75–80 V, which is a field of 0.4 GV m^{-1}. With a C_i of 17 nF cm^{-2}, this corresponds to a maximum attainable ρ of about 13 mC m^{-2}. This is already less than that of the FeFET in the on-state at zero gate bias, but application of a moderate gate field of 90 MV m^{-1} raises ρ even further to 26 mC m^{-2}, as shown in Fig. 4.

A constraint for the operation of FeFETs is that the band-bending V_{bb} induced in the semiconductor should not be so large as to cause depolarization of the ferroelectric layer[25]. Under short-circuit conditions the depolarization field in the ferroelectric equals V_{bb} divided by the thickness of the ferroelectric. It is therefore theoretically possible that as the ferroelectric layer thickness is reduced to obtain low-voltage operation, the ferroelectricity will become unstable. To investigate this, we calculate V_{bb} in the semiconductor at a ρ of 18 mC m^{-2} using a recently developed model[26] together with the parameters that describe the PTrFE FETs. We derive a V_{bb} of 0.5 V which, together with the coercive field of 50 MV m^{-1} of P(VDF/TrFE), means that the depolarization field does not exceed the coercive field for ferroelectric layer thicknesses well below 100 nm. Low-voltage operational polymer FeFETs should therefore be attainable.

Figure 5 presents measurements of degradation and programming time, which are the critical parameters to compare with competing technologies. Figure 5a shows that the on-state is stable for a week whereas the off-current has an initial increase that stops after 1 day. This increase is largely due to an increased gate current and not due to the channel conductance, as shown by the similar increase of gate and drain current. As noted above, the gate current is much larger than that of the active area alone because of the relatively large overlap between source–drain and gate electrodes. The on/off ratio after a week is 10^4 and, apart from the initial off-state increase, is completely stable. Figure 5b shows a decline of the on-current of a pristine device when it is programmed many times, but even after 1,000 programming cycles the devices still have considerable drain-current hysteresis. This is demonstrated in Fig. 5c, which was measured after 1,000 programming cycles. Comparison of Fig. 5c with Fig. 3 shows that the only significant difference is the on-state current. Further experiments are required to explain the decline and to determine whether it can be prevented. Preliminary results with other spin-cast organic semiconductors show that a similar effect occurs there too. Figure 5d presents programming time measurements at an applied field where the ferroelectric in a capacitor switches fully in 0.3 ms (ref. 17). We monitored the switching current during the experiments using a small resistor connected in series, which confirmed this value for the switching time. Figure 5d demonstrates that the programming time is determined by the same number given that the on/off ratio reaches 10^3 within 0.5 ms. The observed asymmetry of the on/off transitions can be explained by the conductance of the semiconductor channel. At 50 µs, the on-state is much more affected by the programming pulse than the off-state because its conductance is higher. At 0.5 ms the roles are reversed, so the off-state disappears rapidly while the on- to off-state transition slows down. Altogether, the long data retention, high programming cycle endurance and short programming time strengthen the viability of this device architecture for non-volatile memory applications.

We suggest that the high performance of the present polymer FeFETs is induced by the lack of defects at the ferroelectric–semiconductor interface. Intermixing at polymer–polymer interfaces can be prevented by using dissimilar solvents for the two layers, making the interfaces abrupt and defect-free. Such defects can lead to the formation of interface charge traps which provide a secondary mechanism for memory applications[11], but they degrade FeFET performance[27]. Proof that surface traps do not affect the performance significantly is provided by the PTrFE FET measurement in Fig. 4. In that measurement the gate field is brought from 0 to 125 MV m^{-1} and back. This should fill the traps and lead to a significant switch-on voltage V_{so}. From comparison with the model curve in Fig. 4, which represents an ideal zero switch-on voltage FET, we can conclude that the trap charge density cannot be larger than 1 or 2 mC m^{-2}. This is insignificant in comparison with the 26 mC m^{-2} value reached in the FeFET.

We suggest that the short programming time, long memory retention and high programming cycle endurance combined with the low-cost deposition method make this device highly suitable for low-cost non-volatile memory applications.

METHODS

PREPARATION

Bottom-gate transistors and capacitors with gold electrodes were prepared on clean glass substrates. The bottom electrodes were applied by shadow-mask evaporation of a thin chromium adhesion layer and gold. Subsequently, polytrifluoroethylene (PTrFE) or poly(vinylidene fluoride/trifluoroethylene) (P(VDF/TrFE)) random copolymer with 65 mol% VDF was applied by spin casting from filtered 2-butanone solutions. These layers were annealed in a vacuum oven at 138 °C to enhance the crystallinity. A second gold layer was applied using shadow-mask evaporation to create a capacitor or a transistor; in the latter case using a wire to create a gap typically 20 µm wide between the source and drain electrode. Non-ferroelectric transistors consisting of lithographically patterned gold electrodes with a bottom-gate configuration and a polyvinylphenol-based standard lithographic resist material as the gate dielectric were also used as a reference[9]. Poly[2-methoxy, 5-(2′-ethyl-hexyloxy)-*p*-phenylene-vinylene] (MEH-PPV) polymer was spin-cast onto the layer stack from toluene solutions in a N_2-filled glovebox and annealed at 90 °C.

CHARACTERIZATION

Field-effect measurements on transistors were done in dark and vacuum using a Keithley 4200 semiconductor analyser. Polymer layer thicknesses were determined using a Dektak profilometer. For the dielectric characterization of capacitor devices, we used Sawyer–Tower charge displacement versus applied field (*D*–*E*) and impedance spectroscopy measurements using a Solartron 1260 impedance analyser. The results reported in Fig. 5d were obtained with the aid of an Agilent 8114A voltage pulse generator. The capacitance charge obtained by the pulses was removed by a short-circuit operation. During the programming operations of Fig. 5b and d, the source and drain electrodes were connected to 0 V, optionally by way of a small resistor.

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Competing financial interests

The authors declare that they have no competing financial interests.