ABSTRACT

Title of Document:	ON-CHIP THERMOELECTRIC HOTSPOT COOLING
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Increased power density and non-uniform heat dissipation present a thermal management challenge in modern electronic devices. The non-homogeneous heating in chips results in areas of elevated temperature, which even if small and localized, limit overall device performance and reliability. In power electronics, hotspot heat fluxes can be in excess of 1kW/cm^2. Although novel package-level and chip-level cooling systems capable of removing the large amounts of dissipated heat are under development, such "global" cooling systems typically reduce the chip temperature

uniformly, leaving the temperature non-uniformity unaddressed. Thus, advanced hotspot cooling techniques, which provide localized cooling to areas of elevated heat flux, are required to supplement the new "global" cooling systems and unlock the full potential of cutting-edge power devices. Thermoelectric coolers have previously been demonstrated as an effective method of producing on-demand, localized cooling for semiconductor photonic and logic devices. The growing need for the removal of localized hotspots has turned renewed attention to on-chip thermoelectric cooling, seeking to raise the maximum allowable heat flux of thermoelectrically-cooled semiconductor device hotspots.

This dissertation focused on the numerical and empirical determination of the operational characteristics and performance limits of two specific thermoelectric methods for high heat flux hotspot cooling: monolithic thermoelectric hotspot cooling and micro-contact enhanced thermoelectric hotspot cooling. The monolithic cooling configuration uses the underlying electronic substrate as the thermoelectric material, eliminating the need for a discrete cooler and its associated thermal interface resistance. Micro-contact enhanced cooling uses a contact structure to concentrate the cooling produced by the thermoelectric module, enabling the direct removal of kW/cm^2 level heat fluxes from on-chip hotspots. To facilitate empirical validation of on-chip thermoelectric coolers and characterization of advanced thin film thermoelectric coolers, it was found necessary to develop a novel laser heating system, using a high-power laser and short-focal length optics. The design and use of this illumination system, capable of creating kW/cm^2-level, mm-sized hotspots, will also be described.

ON-CHIP THERMOELECTRIC HOTSPOT COOLING

By

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Dedication

I dedicate this to my family: Mom, Dad, Liz, Chris, Julius, and Sarah.

Thank you for always supporting me.

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NOMENCLATURE

A_C	cross sectional area [m^2]
COP	coefficient of performance
e	elementary charge, 1.6 x 10^{-19} C
I	current [A]
k	thermal conductivity [W/(m-K)]
k_B	Boltzmann Constant, 1.38 x 10^{-23} J/K
L	element Thickness [m]
*m**	effective mass [kg]
n	carrier concentration [$1/m^3$]
PF	power factor [$W/(m-K^2)$]
Q	heat flow [W]
R	resistance [Ω]
S	Seebeck coefficient [V/K]
T	temperature [K or ºC]
TIM	thermal Interface Material
Z	thermoelectric fig. of merit [1/K]
ZT	thermoelectric fig. of merit

Greek Symbols

ΔT	temperature difference [K]
μ	carrier mobility [$m^2/(V-s)$]
ρ	electrical resistivity [Ω-m]

Subscripts

c	cold-side
elec	electrical
h	hot-side
max	current resulting in maximum temperature difference
Over	overshoot
Pulse	magnitude of current pulse
SC	"super cooling"
min	minimum transient temperature

1 Introduction

1.1 Introduction and Motivation

As electronic devices become smaller in size, increasing power density is not the only thermal management challenge that must be solved. The power dissipated by modern electronic packages is non-uniform, leading to areas of elevated temperature, known as hotspots. In many cases, the hotspot temperature, rather than the temperature of the majority of the device, limits performance and compromises reliability [1]-[4]. Thus, hotspot remediation can greatly improve a device's efficiency by either increasing the maximum performance or by reducing the amount of power required by the bulk cooling system. Power amplifiers, such as IGBTs and HEMTs, are examples of high power devices, which process and dissipate more energy than typical logic chips. In GaN based amplifiers, linear power dissipation in excess of 40W/mm has been demonstrated, however temperature related reliability concerns typically limit device power dissipation to less than 5W/mm [5], [6]. As an example, a typical transistor finger in a GaN based device with a footprint of 0.5μm x 50μm and dissipating 1 watt of power, results in a heat flux of 4 MW/cm^2 [7]!

While the hotspots have very high heat fluxes, the net power dissipated is still relatively small, on the order of only a few watts. However, as shown in Figure 1, the resulting temperature rise can be up to 100K [7]. Thus, a hotspot cooling solution only needs to be capable of removing a few watts of power in order to make a dramatic improvement in the thermal performance. Many novel bulk-cooling systems are being studied for removing the background heat fluxes in power electronics, however new

methods for providing high flux, localized cooling for the removal of hotspots are also required. Therefore, the research presented here had two main focuses: First, two on-chip thermoelectric hotspot cooling configurations were studied extensively in order to determine their capacity for cooling high intensity hotspots. Second, in order to test these novel thermoelectric cooling techniques, a methodology for testing thermoelectric device level performance by using a focused laser to create high heat flux hotspots was developed.

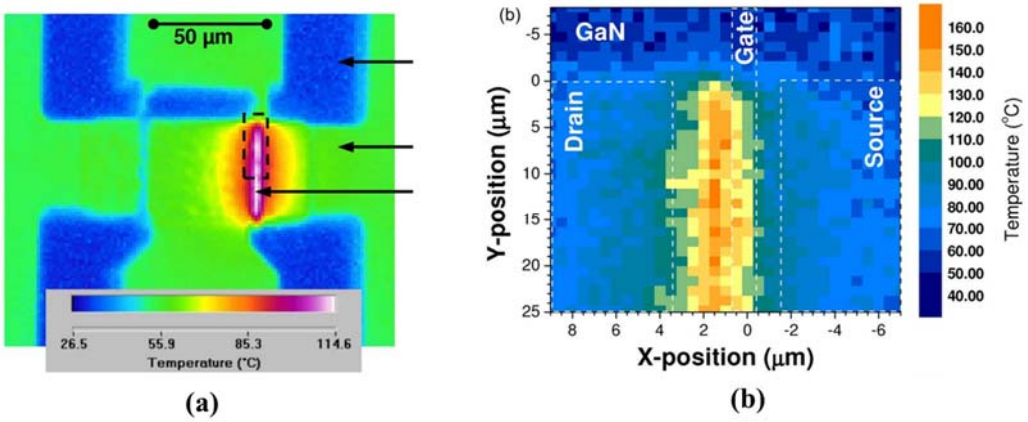


Figure 1. Temperature distribution near the gate of a AlGaN/GaN HFET power transistor captured by Sarua using a combined (a) infrared and (b) micro-Raman technique [7].

1.2 Objective and Scope of Work

The objective of this work was to demonstrate the ability of novel thermoelectric cooling configurations to cool kW/cm^2 level hotspots on silicon and silicon carbide substrates. Two on-chip thermoelectric cooling configurations, monolithic thermoelectric cooling and micro-contact enhanced thermoelectric cooling, were studied extensively using both numerical simulations and experimental demonstrations. Additionally, motivated by the need for high cooling flux thermoelectric modules and high heat flux hotspots for experimental demonstrations,

work was performed on characterization of thin film thermoelectric devices and creation of high heat flux hotspots on various substrates using a laser.

2 On Chip Thermoelectric Hotspot Cooling

2.1 Introduction, Physics, and Figure of Merit

At the macro-scale, thermoelectric coolers, or TECs, can be thought of as heat pumps, similar to the vapor compression cycles found in refrigerators, but relying on solid-state energy conversion and using no moving parts. However, thermoelectric devices generally have lower coefficients of performance (COP) than vapor compression cycles, resulting in a larger market share for vapor compression refrigerators in HVAC and refrigeration [8]. Thermoelectric devices can also be readily switched between heating and cooling mode, making them useful in temperature control applications, and some common commercial uses for thermoelectric modules include small beverage coolers, temperature controlled electronic enclosures, temperature control in photonic packages, and temperature cycling in DNA sequencing machines [9]-[12]. Some of the major thermoelectric manufactures are Laird Technologies, Marlow Industries, Ferrotec, and TE Technology Inc.

However, for the application of hotspot thermal management, thermoelectric cooling presents two major advantages over vapor compression. First, thermoelectric modules are scalable, meaning thermoelectric cooling does not requires a compressor, evaporator, or refrigerant, thus the devices can be made extremely small without concerns about how to shrink various components. Second, thermoelectric coolers have no moving parts, making them extremely reliable. Additionally, as will be discussed,

recent advances in novel thermoelectric materials are producing state of the art thermoelectric devices with high heat pumping capacities and improved COPs [13].

2.1.1 Thermoelectric effects and physics

Although thermoelectric coolers are often called Peltier devices, there are actually three thermoelectric effects to be considered. The Seebeck effect occurs under open circuit conditions and describes voltage generation due to a temperature gradient in a material. The Seebeck effect is the fundamental principle in thermocouple temperature measurements and thermoelectric power generation. As will be described in more detail below, the Peltier effect is essentially the reverse of the Seebeck effect, and describes the amount of heat carried by electrical carriers. Finally, the Thompson effect describes the heating or cooling that occurs when current flows through a material subjected to a temperature gradient. The contribution of the Thompson effect is typically much less than that of Peltier cooling or Joule heating, thus it is typically neglected in the analysis of thermoelectric devices [14].

As mentioned above, the Peltier effect describes the fact that the energy of charge carriers is material dependent. Thus, if a voltage causes electrons or holes to flow across the interface of two dissimilar materials, the charge carriers must absorb or reject energy into the material lattice. The heat pumped, in watts, by a single thermoelectric leg is equal to the Peltier cooling corrected by two parasitic effects, Joule heating and back conduction, as displayed in Equation 1 [14]. Figure 2(a) shows a thermoelectric couple consisting of two oppositely doped legs and it can be seen that as current flows through the circuit, heat is absorbed at the top surface and dissipated at the lower surface. As shown in Figure 2(b), a thermoelectric module is created by

connecting many thermoelectric couples electrically in series and thermally in parallel. Joule heating and conduction are irreversible effects and decrease the performance of a thermoelectric cooler [14]. From Equation 1, it can be seen that a larger Seebeck coefficient increases the Peltier cooling, while low electrical resistivity and thermal conductivity minimize parasitic effects. Advanced thermoelectric materials, which are designed to maximize Peltier cooling, with minimal parasitic losses, will be discussed in detail in the following sections.

$$Q_{net} = STI - \frac{1}{2}I^2R - K(T_h - T_c) \qquad (1)$$

$$R = \frac{\rho L}{A}$$

$$K = \frac{kA_c}{L}$$

S – Seebeck coefficient [V/K]

T – Absolute temperature [K]

I – Current [A]

ρ - Electrical resistivity [Ω-m]

L – Length [m]

k – Thermal conductivity [W/m*K]

A_c - Cross sectional area [m^2]

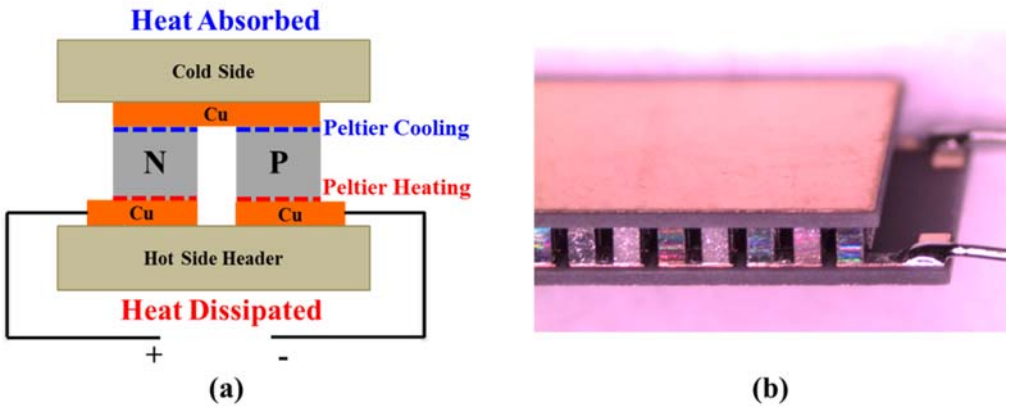


Figure 2. (a) Schematic of a thermoelectric device - a voltage is applied, resulting in current flow, which causes absorption of heat at the top surface (cold side) and rejection of heat at the bottom surface (hot side), and (b) an image of a typical thermoelectric module, consisting of many thermoelectric couples connected electrically in series and thermally in parallel.

Figure 3 shows a semiconductor block attached to two metallic contacts, each at a specified temperature and voltage. The Fermi distribution in each contact, as well as the band diagram for the semiconductor, is shown for three different cases. According to the Landaur-Boltzman expression, the flow of current is determined by three main parameters: Transmission (T), number of electron modes or channels (M), and the difference in Fermi levels (f_1-f_2).

The first case shown in Figure 3 is the flow of current due to an applied voltage. As can be seen, the applied voltage shifts the electrochemical potential in contact one up, such that electronics are supplied from contact 1 into the conduction band of the semi-conductor and flow through to contact 2. In the left column of the figure, it can be seen that the difference in Fermi distribution between the two contacts (f_1-f_2) has a peak in the conduction band of the semi-conductor, which provides the driving force for conduction.

The second case in the figure shows current flow due to an applied temperature difference, which is representative of thermoelectric power generation. Here, no external voltage is applied, so the electrochemical potential in contacts 1 and 2 are equal. However, temperature affects the shape of the Fermi distribution, so if contact 2 is very cold, its Fermi distribution will become a sharp step, as shown in the figure, and if contact 1 is warm, its Fermi distribution becomes a more gradual step.

In this case, the difference in Fermi distribution (f_1-f_2) has two peaks, one which drives the flow of electrons from left to right, and the other which drives electrons from right to left. Initially, it might seems that these two flows would cancel out, resulting in no net flow of current. However, current flow is also a function of the number of electron modes or channels in the semiconductor. As shown in the figure, the density of electron states increases with increasing energy in an n-type material, meaning an n-type material has more electron channels available at the Fermi level that is driving electron flow from left to right, resulting in a net flow of current. In p-type semi-conductors, the opposite is true, and there is a net flow of electrons from right to left, and in fact, this property is commonly used test if a semi-conductor is p-type or n-type.

The final case shows heat flow due to the application of an electrical voltage or current, representative of thermoelectric cooling. Similar to the first case, the application of an external voltage shifts up the Fermi distribution in contact 1. However, in this case the electrochemical potential remains just below the bottom of the semiconductor's conduction band, thus electrons must absorb energy from the surrounding material lattice in order to jump up into the conduction band. The electrons then flow through the semi-conductor and release energy into contact 2 as they drop

down from the conduction band. The Seebeck coefficient, S, is proportional to the amount of energy that the electrons must gain to jump from the Fermi level in contact 1 into the conduction band of the semi-conductor, which demonstrates a fundamental challenge in the engineering of advanced thermoelectric materials.

As previously discussed, Peltier cooling is directly proportional to the Seebeck coefficient, so large Seebeck coefficients are desirable for thermoelectric cooling. However, increasing the amount of energy that electrons must absorb to enter the conduction band of semi-conductor also increases the electrical resistivity, which produces additional parasitic Joule heating and can counteract the benefit of the additional Peltier cooling. Therefore, properties of thermoelectric materials must be carefully optimized for the application, and will be discussed in greater detail in Section 2.3.

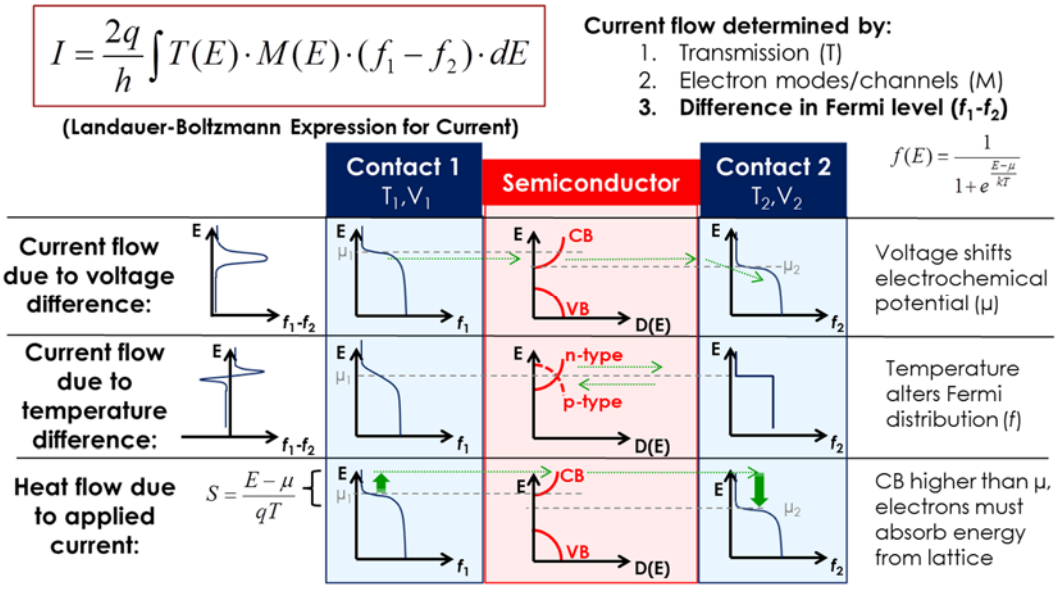


Figure 3. Description of current flow due to an applied voltage and temperature difference and heat flow due to an applied current.

2.1.2 Figure of Merit

The potential of thermoelectric materials is often evaluated using the figure of merit, Z, shown in Equation 2, with units of K^{-1}. Since Peltier cooling is proportional to temperature, ZT, which is Z multiplied with absolute temperature and is therefore dimensionless, is also used as a figure of merit [15]. In some thermoelectric configurations, such as the monolithic cooling configuration, thermal conductivity has a less direct correlation with hotspot cooling [15]. Thus, the power factor, shown in Equation 3, is a more appropriate figure of merit in these situations. As will be discussed in Section 2.6.1, Joule heating and back conduction are parasitic effects that degrade the amount of hotspot cooling that can be provided by a monolithic cooler. However, unlike a discrete module, in monolithic cooler, the thermoelectric material is also the substrate of the electronics that are being cooled, and, therefore, the thermal conductivity plays a more complex role, affecting both back conduction and heat spreading within the chip [15]. In depth discussion of the monolithic cooling configuration will be provided in Chapter 3.

$$Z = \frac{S^2}{\rho k} \quad [\mathrm{K}^{-1}]; \qquad ZT = \frac{S^2}{\rho k} T \tag{2}$$

Since thermoelectric coolers are effectively solid state heat pumps, COP is also an important parameter to evaluate. Based on the discussion in the previous section, the amount of heat pumped by two oppositely doped thermoelectric legs can be described by Equation 4 [15]. The electrical power consumed by the thermocouple consists of the energy dissipated as Joule heat and the power expended overcoming the Seebeck voltage, as shown in Equation 5 [15]. COP is simply the heat pumped divided

by the total energy consumed. Thus Equation 6 shows a relationship for the COP of a two leg thermoelectric couple [15].

$$PF = \frac{S^2}{\rho} \tag{3}$$

$$Q_{net} = \left(S_p - S_n\right)T_C I - \frac{1}{2} I^2 R - K(T_h - T_c) \tag{4}$$

$$P_{elec} = I^2 R + (S_p - S_n)(T_H - T_C)I \tag{5}$$

$$COP = \frac{Q_{net}}{P_{elec}} = \frac{\left(S_p - S_n\right)T_C I - \frac{1}{2} I^2 R - K(T_h - T_c)}{I^2 R + (S_p - S_n)(T_H - T_C)I} \tag{6}$$

2.2 Conventional Thermoelectric Materials and Modules

2.2.1 Conventional Thermoelectric Modules

A typical thermoelectric module consists of many of the thermoelectric couples described above, placed thermally in parallel and electrically in series. The couples are connected by copper traces and sandwiched between ceramic plates for mechanical support. When power is supplied to the device, the electrical energy is converted into thermal energy resulting in a net flow of heat through the device. Conventional thermoelectric devices have been previously used in specialized cases of electronics cooling. However, in addition to their low COP, conventional coolers also have a limited heat pumping capacity, making them unsuitable for high heat flux cooling applications. Therefore, recent research on advanced thermoelectric modules and materials has focused on the production of state-of-the-art devices with higher heat pumping capacities and improved COP.

As an example, Figure 4 shows a representative performance curve for a thermoelectric module. As can be seen in the figure, the maximum cooling flux that can be produced by this cooler is on the order of 100W/cm^2 and can be reached when there is no ΔT across the device. Conversely, the maximum ΔT of the device can only be reached when the device cooling flux is zero. Figure 4(b) displays the COP of the cooler as a function of cooling flux for various ΔTs. While the thermoelectric cooler can reach relatively high COP values at low cooling fluxes and low ΔTs, the COP decreases to values of less than one as the cooling flux or ΔT is increased to levels that would be the most useful for high heat flux hotspot cooling. Thus, research on advanced thermoelectric materials and modules focuses on both increasing the COP itself, as well as increasing the cooling flux at which the peak COP occurs[16]. Tabulated data on common commercially available thermoelectric modules are available in [15], [17].

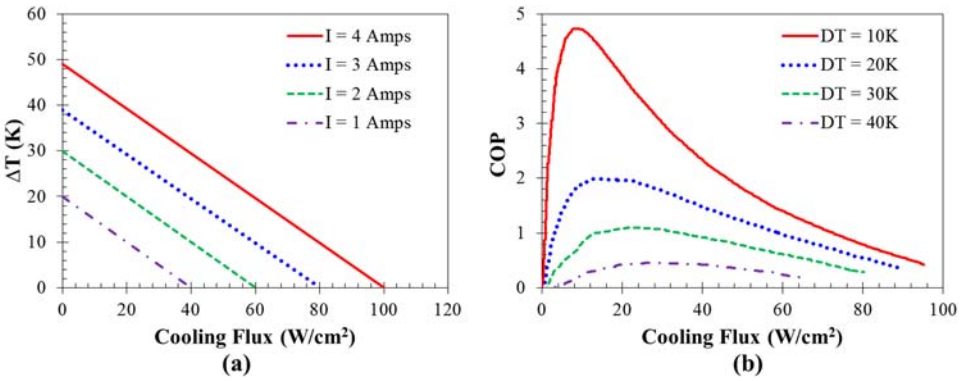


Figure 4. Representative thermal performance curves for a thermoelectric module. (a) Device ΔT as a function of cooling flux for several different current levels and (b) COP as a function of cooling flux for a variety of device ΔTs [18].

Ranjan *et al.* performed a numerical study with the goal of increasing the cooling flux and COP of thermoelectric modules by varying the angle of the thermoelectric legs to increase packing fraction and therefore performance[19]. As was

shown in Figure 4(b), the maximum COP for a thermoelectric module is typically reached at relatively small cooling fluxes, thus one objective of the study was not to just increase COP across the board, but rather to increase the cooling flux at which COP is maximized. Packing fraction is the ratio of the area occupied by active thermoelectric elements to the total footprint area of the thermoelectric module. Figure 5 shows the packing fraction and heat pumping as a function of thermoelectric leg angle for a leg height of 100μm. As the leg angle increases, more active thermoelectric area can be fit in the footprint area of the module, thus packing fraction increases and at large leg angles, where the thermoelectric elements are close to 90° from the traditional arrangement, packing fractions greater than one are possible. Due to the packing fraction enhancement, it can be seen that increasing the leg angle causes an increase in heat pumping at the maximum COP, particularly at large angles.

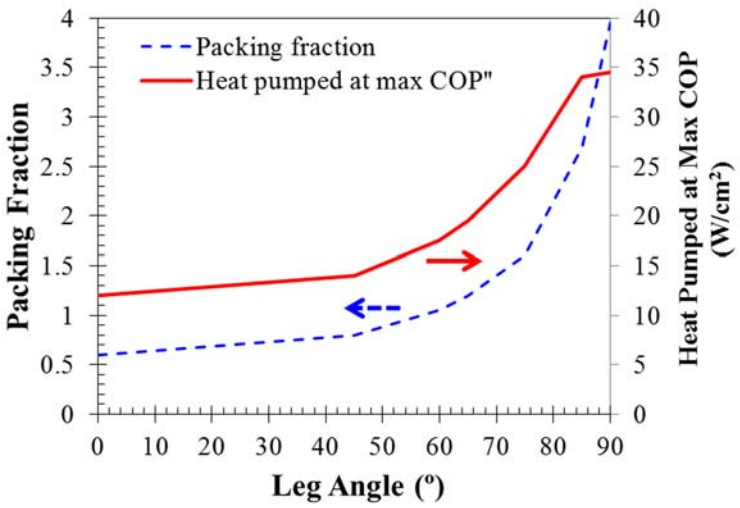


Figure 5. Dependence of packing fraction and cooling flux at maximum COP on element leg angle. It can be seen that packing fraction and heat pumped both increases with increasing leg angle [19].

Hodes performed multiple analytical studies on the optimization of element, or pellet, geometry in thermoelectric modules [20], [21]. An optimization was performed

with and without electrical contact resistance assumed at the metal-semiconductor interface and the relationship for the optimum element leg height, which maximizes heat pumping capacity for a given temperature difference, was derived. Element packing fraction was also considered and it was found that the maximum cooling flux varies linearly with packing fraction while varying inversely with electrical contact resistance. A relationship for the optimum leg height, which maximizes the coefficient of performance as a function of cooling flux, with electrical contact resistance considered, was also derived. Finally, the effect of element cross sectional area was studied and it was found that decreasing cross sectional area leads to a larger voltage drop and more power consumption by the TEC. Therefore, optimization of the pellet cross sectional area can be used to minimize electrical power losses [21].

2.2.2 Conventional Thermoelectric Materials

There are a variety of semiconductors used in thermoelectric modules. Commercially, the most common thermoelectric material is bismuth telluride (Bi_2Te_3), along with many related alloys including Sb_2Te_3, Bi_2Se_3, and Bi_4Te_6 [12], [22], [23]. Additionally, other semiconductors have been studied including silicon, germanium, and silicon and germanium based alloys. Figure 6 shows the variation in Seebeck coefficient and figure of merit, Z, of bismuth telluride as a function of composition. It can be seen that low concentrations of tellurium result in a positive Seebeck coefficient, while high concentrations lead to a negative Seebeck coefficient [23]. Figure 4(b) shows the figure of merit, which is a result of the combined behavior of the Seebeck coefficient, electrical resistivity, and thermal conductivity, as a function of telluride concentration. This paper will focus on thermoelectric materials that are optimized for

use in temperature ranging from 20ºC to 500ºC. However, there are many thermoelectric materials available for specialized applications, ranging from cryogenic temperatures to high temperature waste heat recovery [9], [24].

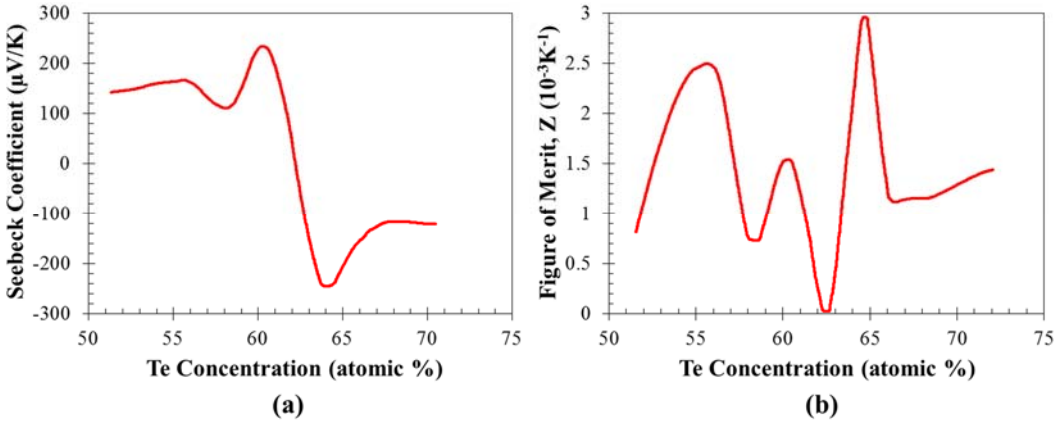


Figure 6. Dependence of (a) Seebeck coefficient and (b) figure of merit, Z, on Te concentration for BiTe [17], [23].

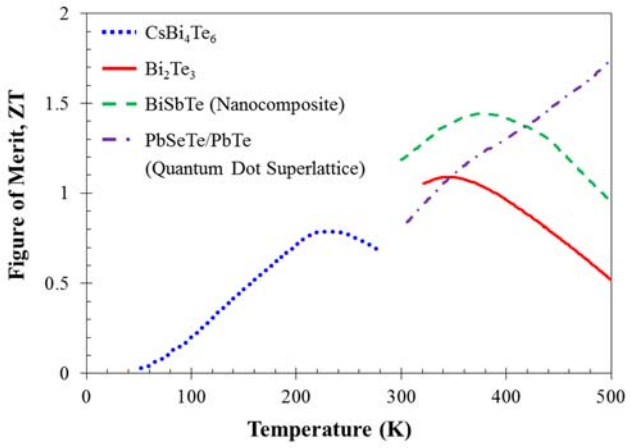


Figure 7. Figure of merit, ZT, of conventional and nanostructured thermoelectric materials as a function of temperature [17], [23].

2.3 Advanced Thermoelectric Materials

2.3.1 Superlattice Thermoelectric Materials

The performance of a thermoelectric device is determined by the material properties, as shown in Equation 1. Therefore, for improving the performance of a

thermoelectric cooler it is desirable to engineer new thermoelectric materials which have larger Seebeck Coefficient (S), smaller thermal conductivities (k), and smaller electrical resistivity (ρ) [25]. The majority of advanced thermoelectric materials are made of superlattice structures, consisting of alternating layers of two different materials, which are capable of increasing Seebeck coefficient while decreasing thermal conductivity, by reducing phonon transport in thebulk materials and at the interfaces, relative to bulk materials, resulting in improved Z values [26].

2.3.2 Reduction in Thermal Conductivity

A major challenge in the production of high Z thermoelectric material is decoupling the three thermoelectric properties of interest. For example, thermal conductivity is inherently linked to electrical conductivity by the Weidemann-Franz law [10]. Thus, it is difficult to increase the electrical conductivity (decreasing the resistivity), without also increasing the thermal conductivity. Thermal conductivity is composed of an electrical contribution and a lattice contribution, where the electrical contribution is the thermal energy carried by electrons and the lattice contribution is thermal energy transmitted through the lattice as vibrations, also known as phonons. Any attempt to decrease the electrical contribution of thermal conductivity will obviously lead to an increase in electrical resistivity, thus superlattice structures typically reduce the thermal conductivity of a material by suppressing the lattice contribution to thermal conductivity as much as possible, while leaving electron flow unaffected [27]-[30].

The numerous interfaces in a superlattice structure impede through-plane thermal transport by scattering and reflecting phonons, resulting in a decreased thermal

conductivity relative to the bulk material [31]. As suggested by Equation (1), the lower thermal conductivity of superlattice lattice thermoelectric materials impedes back conduction of heat, improving the heat pumping and maximum ΔT of thermoelectric modules. As will be discussed in more detail, there are also planer thermoelectric configurations, where heat is pumped laterally rather than vertically, as is typical in a thermoelectric module. In the case of planer thermoelectric coolers, the in-plane thermal conductivity also influences thermal performance.

Although phonons do not need to cross multiple interfaces when traveling in-plane through a superlattice structure, it has been determined that the in-plane thermal conductivity of superlattice structures is also reduced below bulk values. Chen performed an analytical study on the effect of superlattice structures on in-plane thermal conductivity and determined that the thickness of the individual repeating layers, as well as the quality of the interfaces between the layers, plays a crucial role in determining the overall thermal conductivity of the structure [31]. Figure 8 shows the predicted in-plane thermal conductivity of a GaAs/AlAs superlattice, compared with experimental results obtained by Yu *et al.* and Yao *et al.* [32], [33]. It can be seen that the bulk material has the highest thermal conductivity and that if the interfaces between the layers are assumed to be perfectly specular, the in-plane thermal conductivity remains near that of the bulk value for all layer thicknesses. However, if the interface between the layers is assumed to be diffuse, the thermal conductivity is greatly reduced, especially at small layer thickness where interface effects dominate. The diffuse reflections at each interface scatter phonons, thus resulting in the reduced thermal conductivity, even in the in-plane direction.

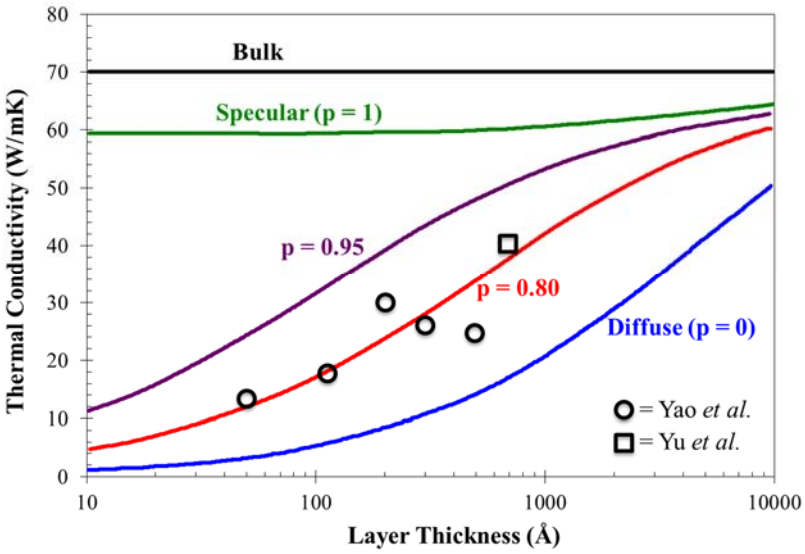


Figure 8. In-plane thermal conductivity of a GaAs/AlAs superlattice. Here, p is the interface scattering parameter, where p = 1 and p = 0 correspond to a perfectly specular and perfectly diffuse interface condition, respectively [31]-[33].

2.3.3 Increase in Seebeck Coefficient

The Seebeck coefficient can also be increased in superlattice structures, thus improving thermoelectric performance. However, as was the case with thermal conductivity, there are tradeoffs to consider [34]. For example, Equation 7 shows a relationship for the Seebeck coefficient, where n is the carrier concentration and m^* is the effective mass of the carrier [10]. It can be observed that a lower carrier concentration, n, produces a larger Seebeck coefficient. However, Equation 8 shows a relation for electrical resistivity, where it is clear that decreasing the carrier concentration increases resistivity, thus offsetting some of the benefit seen in Seebeck coefficient [10]. As was discussed, thermal conductivity is also directly linked to electrical conductivity. As shown in Figure 9 for Bi_2Te_3, the carrier concentration of a given material needs to be optimized to provide the ideal balance of the three thermoelectric material properties in order to maximize Z [10].

$$S = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n} \right)^{\frac{2}{3}} \quad (7)$$

$$\rho = \frac{1}{ne\mu} \quad (8)$$

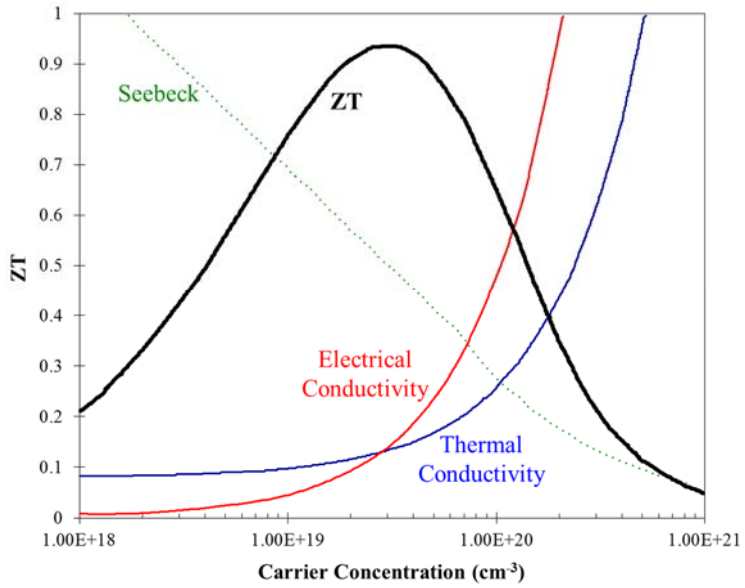


Figure 9. General behavior of Seebeck coefficient, electrical conductivity, and thermal conductivity as a function of carrier concentration for Bi_2Te_3. It can be seen that there is an optimum balance of the competing thermoelectric effects, which maximizes ZT [10].

2.4 Thin-Film Thermoelectric Cooling

In order to cool the high heat flux hotspots found in power electronics, it is necessary to maximize the cooling flux that can be provided by thermoelectric modules. In addition to improving the properties of thermoelectric materials, as was discussed in the previous section, reducing the thickness of the thermoelectric elements used in a module can increase the maximum achievable heat pumping [35]. Equation 9 shows a relation for the maximum heat pumping capacity of a thermoelectric device, where *l* is the thickness of the thermoelectric elements [35].

It is clear that reducing l increases the maximum heat pumping capacity; however there is a limit to this benefit. As the thermoelectric elements become thinner and thinner, parasitic effects at the interfaces begin to dominate, limiting device performance [35]. Additionally, as the thermoelectric element thickness is reduced, the thermal resistance between the hot side and cold side of the thermoelectric device also decreases; hence the increased cooling flux is achieved at the expense of reduced maximum ΔT across the module. Figure 10 shows the cooling power for bulk, miniature, and thin film thermoelectric devices as a function of cold side temperature [36]. As suggested by Equation 9, reducing the thickness of the thermoelectric legs by an order of magnitude results in an increase in cooling flux of approximately one order of magnitude.

$$q_{\max} = \frac{1}{l}\left[\frac{S^2 T_{cold-side}^2}{2\rho} - k\left(T_{hot-side} - T_{cold-side}\right)\right] \tag{9}$$

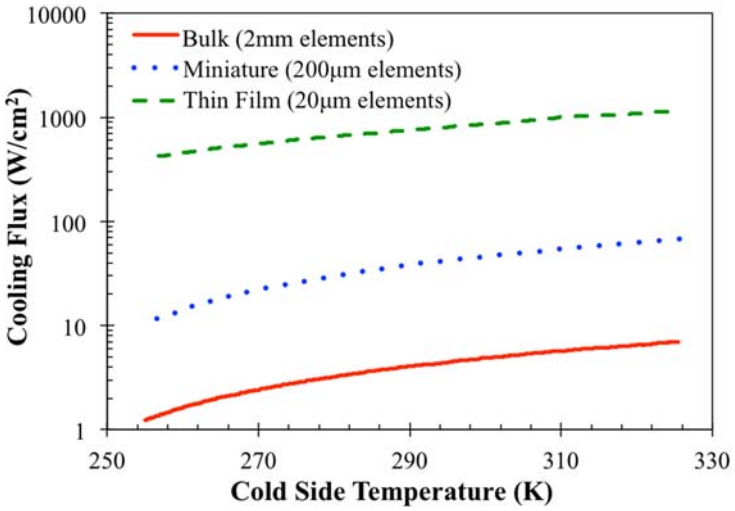


Figure 10. Cooling flux as a function of cold side temperature for three element thickness for a BiTe alloy based thermoelectric device. It is clear that thinner elements result in larger cooling fluxes [36].

2.4.1 Freestanding Thin Film Thermoelectric Cooling

In 2001, Venkatasubramanian *et al.* created Bi_2Te_3/Sb_2Te_3 thin film superlattice thermoelectric elements composed of approximately 2000 individual layers with thicknesses as small as 10Å. The thin film thermoelements were capable of providing maximum cooling fluxes of 700W/cm^2 and 585W/cm^2 at temperatures of 353K and 298K, respectively [37]. It should be noted that these values are for a free standing device and effective integration into an overall thermal management system, including efficient heat removal from the hot side of the device, would be required for optimum hotspot cooling performance [38].

Harman *et al.* created PbSeTe quantum dot superlattice structures using molecular beam epitaxy and performed device level testing at room temperature [39]. The quantum dot superlattice samples had measured Seebeck coefficients of -208 to -219μV/K and corresponding ZT values of 1.3 to 1.6 at 300K. Single PbSeTe thermoelectric legs were tested using the test fixture shown in Figure 11, where the hot junction is attached to a heat sink and the circuit is completed with a gold wire. It was found that a maximum ΔT of 43.7K, at an applied current of 650mA, could be achieved in this configuration. As a reference, Harman also tested a traditional $(BiSb)_2(SeTe)_3$ leg, with comparable dimensions, in the same test fixture and achieved a ΔT of 30.8K.

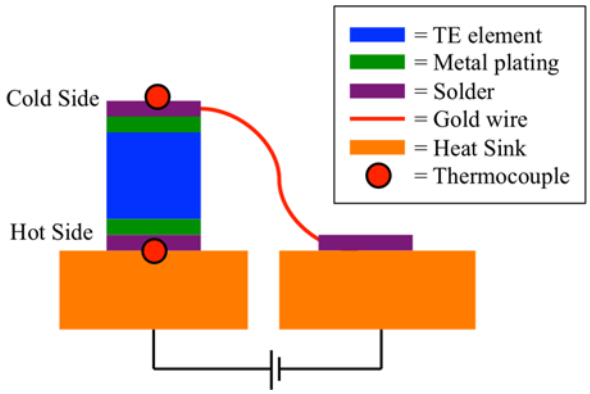


Figure 11. Schematic of the experimental setup used by Harman for testing of a single PbSeTe thermoelectric leg [39].

Bulman *et al.* fabricated thin film superlattice BiTe thermoelectric elements and were able to experimentally measure the Seebeck coefficient, which ranged from 489 to 633 μV/K (p-type), for the samples [40]. Figure 12 shows the ΔT across the device as a function of applied current for three slightly different cooler configurations, all of which utilize the superlattice BiTe. It can be seen that device level temperature differences of up to 54.4K could be achieved. Additionally, embedded thermocouples were used to measure the internal ΔT, which was found to be larger than the external ΔT, with values up to 68.8K. Finally, maximum element and device level cooling fluxes of 715 and 128W/cm^2, respectively, were measured.

As discussed in Section 2.1, the footprint of a thermoelectric device is made up of many thermoelectric elements with space between them, and the ratio of the active thermoelectric area to the total footprint of the device is described by the packing fraction. Devices typically have packing fractions of less than 50%, thus, as seen in Bulman's results, the device level cooling flux is significantly lower than the element level flux. Table I summarizes the thermoelectric coolers discussed in this section, along with other recent novel devices.

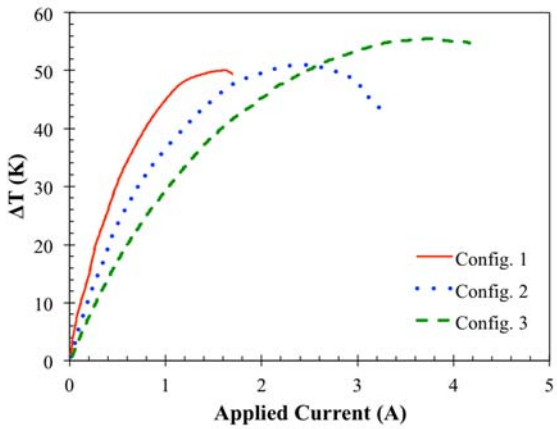


Figure 12. Device ΔT as a function of applied current for three superlattice BiTe based coolers fabricated by Bulman *et al.* [40].

Table I. Summary of recently fabricated free standing thin film thermoelectric coolers.

Researcher and Year	Classification	Materials	ZT	Max Cooling (at ΔT = 0) [W/cm^2]	Max ΔT (at Q=0) [K]
Venkatasubramanian *et al.* – 2001 [37]	Superlattice	Bi_2Te_3/ Sb_2Te_3	2.4 (@ 300K)	700 (@353K) *Element level*	32 (@ 300K)
Harman *et al.* – 2002 [39]	Superlattice/ Quantum Dot	PbSeTe/ PbTe (n)	2 (@ 300K)	Not reported	43.7 (@ 300K)
Semenyuk – 2006 [41]	Thin Bulk Device	Bi_2Te_3	1.1 (@ 350K)	132 (@ 350K) *Device level*	92 (@ 350K)
Bulman *et al.* – 2006 [40]	Superlattice	Bi_2Te_3	0.75 (@ 300K)	128 (@ 300K) *Device level* 715 (@ 300K) *Element level*	55 (@ 300K)
Goncalves *et al.* – 2007 [42]	Thin Film (flexible)	Bi_2Te_3 (n) Sb_2Te_3 (p)	0.86 (n) 0.49 (p)	Not reported	5 (@300K)
Jovanovic *et al.* – 2009 [43]	Quantum Well Thin Film	Si/SiGe	~7 (@ 350K)	Not reported	Not reported

2.4.2 Hotspot Cooling Using Thin Film Thermoelectric Coolers

The previous section outlined recent progress made in device level fabrication and testing of freestanding thin film thermoelectric coolers. Recent research has also explored thermoelectric devices integrated into an electronic system to cool hotspots [44]-[46]. Chau *et al.* performed an exploratory numerical study into the feasibility of using embedded thermoelectric devices for cooling hotspots in electronic substrates [47]. In this study, a 2.5mm x 2.5mm thin film thermoelectric cooler, with a total thickness of 100µm, was used to cool a 400µm x 400µm hotspot located at the center of a silicon chip, as shown in the schematic in Figure 13. The hotspot dissipated 3W of power, resulting in a 1,875W/cm^2 heat flux, while the rest of the chip had a background heat flux of 100W/cm^2. Chau *et al.* explored four different TEC placements consisting of embedding the TEC in the heat spreader, attaching the TEC to the bottom of the heat spreader, attaching the TEC to the top of the die, and embedding the TEC in the die. It was found that the thermoelectric cooler was capable of reducing the maximum hotspot temperature by 16K when a current of 6 amps was applied to the device. Additionally, it was determined that the maximum hotspot temperature was fairly insensitive to TEC placement, varying less than 2K between the different configurations.

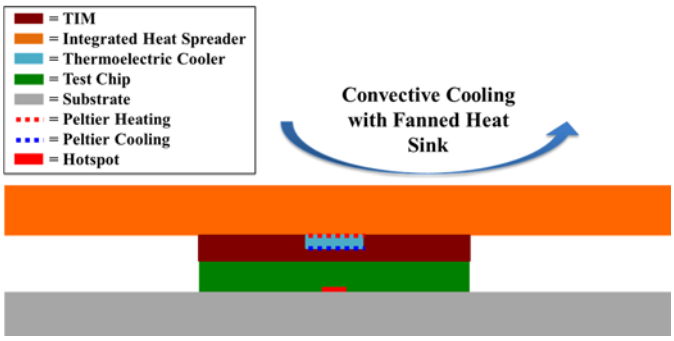


Figure 13. Schematic of a typical thin film thermoelectric hotspot cooling test setup, consisting of a test chip with a hotspot in the center [35], [47]-[49].

Ramanthan *et al.* also performed modeling, which studied the ability of an embedded thermoelectric device to cool a hotspot [48]. Similar to the Chau study, a thermoelectric cooler and integrated heat spreader were attached to a die with a thermal interface material and the integrated heat spreader was cooled using a heat sink. The die was 1cm x 1cm and dissipated a background heat flux of 100W/cm^2 with a 500µm x 500µm hotspot at the center, consisting of a heat flux of 800W/cm^2 [48]. The thermoelectric cooler was centered over the hotspot and had a footprint of 3mm x 3mm, with element leg heights ranging from 5µm to 30µm. Figure 14 shows the maximum hotspot temperature as function of power supplied to the thermoelectric cooler, with and without electrical contact resistance, for two different ZT values. Figure 15 shows the maximum hotspot temperature as a function of thermoelectric leg height, also for two different ZT values. It can be seen that there for a given ZT, there is an optimum input power and leg height, which maximizes hotspot cooling.

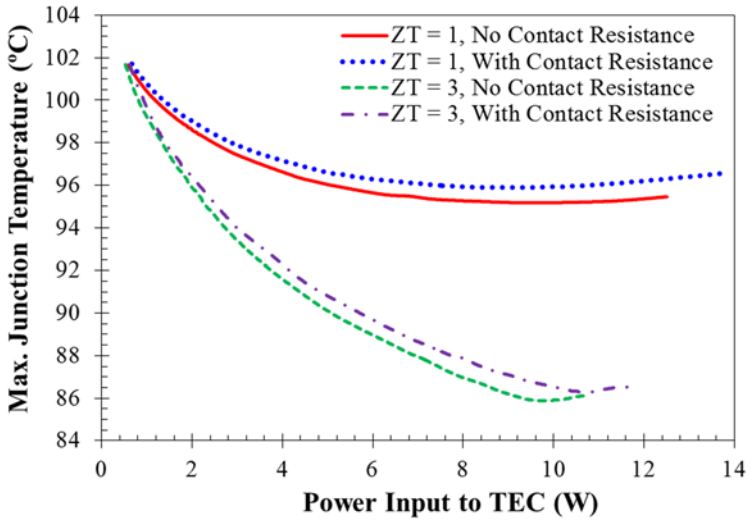


Figure 14. Maximum junction temperature as function of input power for a theoretical TEC with ZT = 1 and ZT = 3. It is clear the high ZT device produces a significant enhancement in cooling of the junction temperature [48].

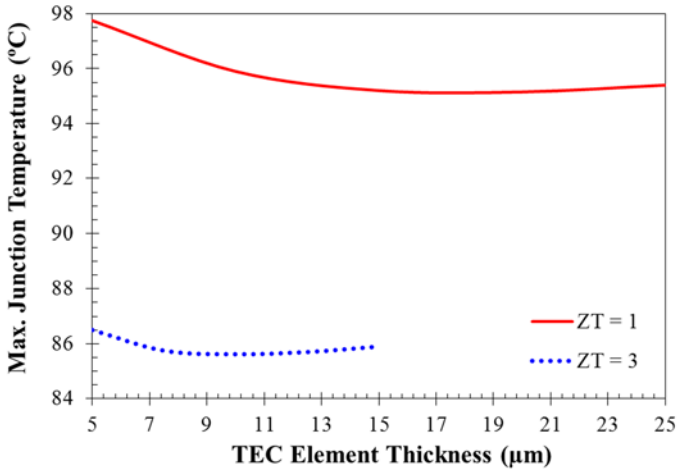


Figure 15. Dependence of maximum junction temperature on thermoelectric element thickness for a TEC with ZT = 1 and ZT = 3. It is clear the high ZT device produces a significant enhancement in cooling of the junction temperature [48].

Chowdhury *et al.* fabricated a thin film thermoelectric module, which consisted of elements that ranged from 5 to 8 microns thick, and had a total device thickness of approximately 100µm [35]. The thin film cooler was grown directly on an integrated heat spreader, which provided a path for heat to be removed from the hot side of the thermoelectric device, as well as mechanical stability. The device consisted of a 7x7 array of p-n thermoelectric couples occupying a footprint of 3.5mm x 3.5mm. The cooler and integrated heat spreader were attached to the backside of a silicon test vehicle, similar to the set up shown in Figure 13, and a background heat flux of 43W/cm^2 and a 400µm x 400µm hotspot with a heat flux of 1250W/cm^2 were applied [35].

Figure 16 shows the hotspot temperature as a function of current applied to the thermoelectric device. It should be noted that the results include 'passive cooling,' which occurred due to the TEC's higher effective thermal conductivity compared to the thermal interface material (TIM) that it replaced. It can be seen that the model with

electrical and thermal contact resistances agrees well with experimental results and that the presence of thermal contact resistance degrades hotspot cooling performance more severely than electrical contact resistance. Typically, the parasitic effect of thermal contact resistance becomes more severe at higher hotspot heat fluxes, thus good thermal contact between the cooler and chip is vital for effective hotspot cooling. In addition to the case shown, several other thin film thermoelectric devices were tested and were capable of providing on-demand hotspot cooling of up to 9.6K [35].

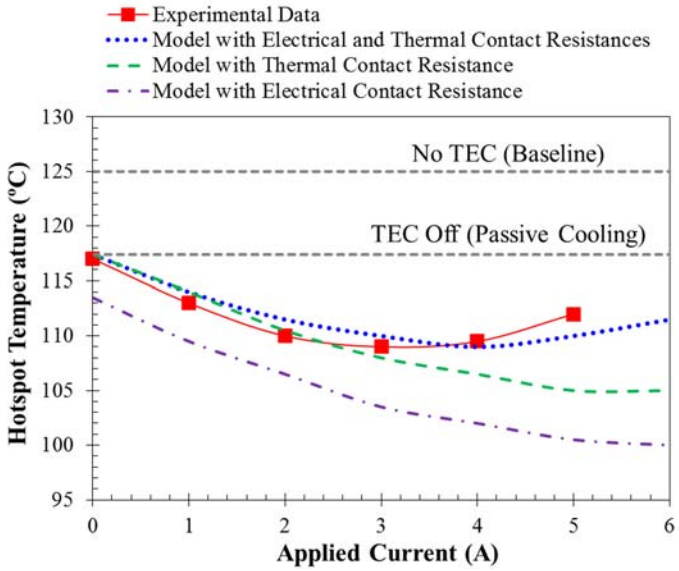


Figure 16. Numerically and experimentally obtained hotspot temperature as a function of applied current for a thin film thermoelectric device with an integrated heat sink. The higher conductivity of the TEC relative to the TIM results in 8K of passive cooling even when the device is off. When the optimum current is supplied, the thermoelectric modules produces up to 9.6K of on-demand cooling [35].

Gupta *et al.* performed a numerical study on thermoelectric hotspot cooling, similar to the Chowdhury study discussed above. As was the case in the Chowdhury study, it was found that the thermal contact resistance between the TEC and the substrate and the electrical contact resistance between the thermoelectric elements and the metal traces are critical parameters in determining the performance of a device [49].

Figure 17 shows the hotspot temperatures calculated by Gupta *et al.* as a function of current with and without thermal and electrical contact resistances. Electrical contact resistances ranging from $10^{-11}\Omega\text{-m}^2$ to $10^{-10}\Omega\text{-m}^2$ and thermal contact resistances from $1\text{x}10^{-6}\text{m}^2\text{K/W}$ to $8\text{x}10^{-6}\text{m}^2\text{K/W}$ were considered in this study, and values of $10^{-11}\Omega\text{-m}^2$ and $10^{-6}\text{m}^2\text{K/W}$ were used for electrical and thermal interface resistances, respectively, in the case shown. It can be seen that without contact resistance, the thermoelectric cooler can provide approximately 12K of hotspot cooling, but when thermal and electrical contact resistances are present, the hotspot cooling is reduced to 5.5K.

An energy analysis of operation of the thin film thermoelectric cooler was also performed, as shown in Figure 18. In this situation, COP is defined as the ratio of the amount of energy removed from the hotspot to the amount of energy supplied to the thermoelectric cooler. As can be seen in Figure 18(a), the largest COP occurs at small currents, and decreases as the current magnitude is increased. Figure 18(b) shows the amount of heat entering the cold side of the thermoelectric cooler and the amount of electrical power being supplied to the device as a function of current. It should be noted that due to spreading, the thermoelectric device removes heat from the area immediately around the hotspot as well as from the hotspot itself, thus the amount of power being absorbed at the cold side of the thermoelectric module, Q_{in}, is a different quantity than the amount of energy being removed from the hotspot. Increasing the current causes parabolic behavior in Q_{in}, with a maximum value around 12 amps, and causes the amount of power consumed by the thermoelectric device to increase exponentially. Gupta *et al.* also performed extensive numerical simulations on transient operation of the thermoelectric cooler, which will be discussed in Section 7.

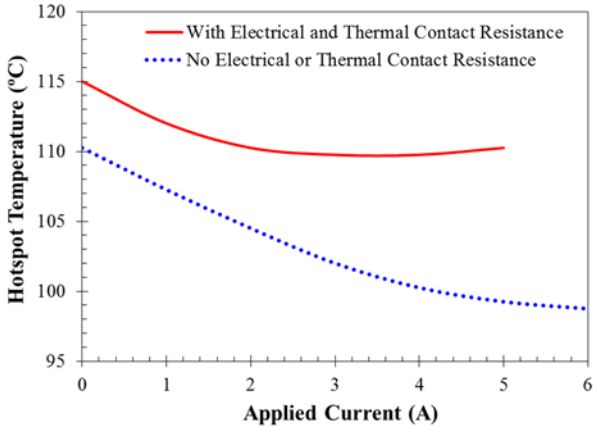


Figure 17. Hotspot temperature as a function of current, with and without contact resistances. The thermal and electrical contact resistances reduced the hotspot cooling by over 10K [49].

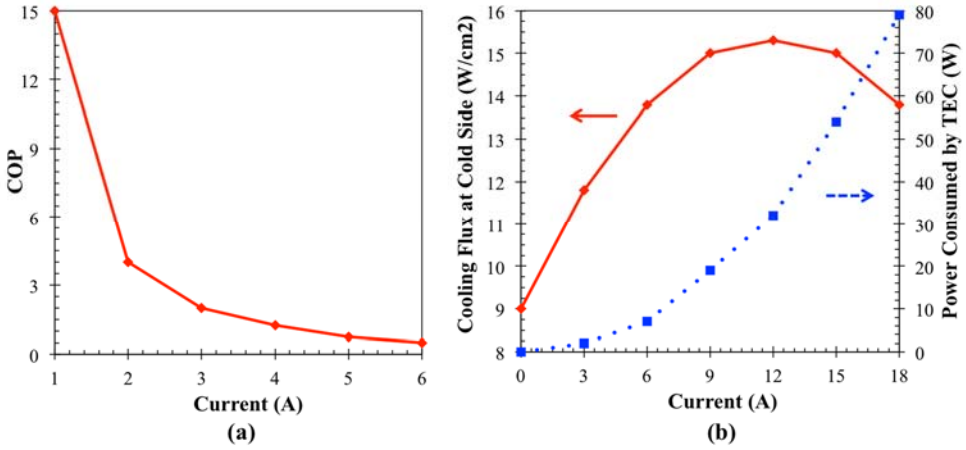


Figure 18. Dependence of (a) COP and (b) cooling flux and power consumed on applied current for a thermoelectric device. The COP is quite low at the current that produces the maximum cooling flux [49].

Wang *et al.* explored the potential of using a hybrid thermal management system, consisting of a liquid cooled cold plate and an embedded thin film thermoelectric cooler, for isothermalization of an insulated gate bipolar transistor (IGBT) chip [50]. Figure 19 shows a schematic of the cooling system, which includes an IGBT chip with a uniform heat flux ranging from 100W/cm^2 to 200W/cm^2. The IGBT is soldered to a direct bond copper (DBC) substrate, which is attached to a liquid

cooled cold plate. In this example, the TEC is embedded in the lower copper layer of the DBC substrate; however an alternative configuration, with the TEC embedded in the liquid cooled cold plate, was also studied.

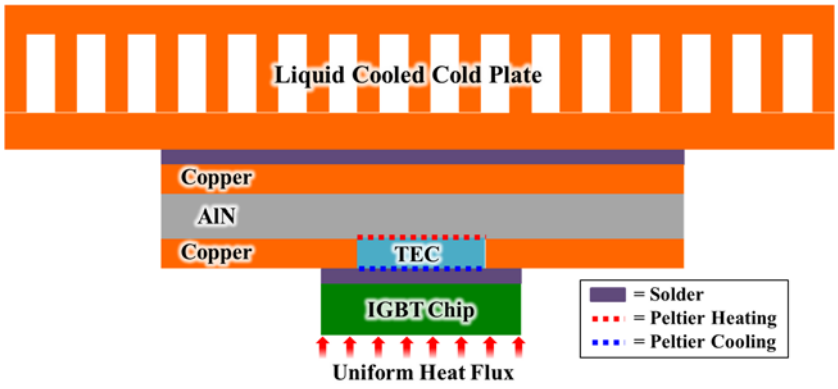


Figure 19. Schematic of the IGBT chip and thermal management system tested by Wang *et al.* [50].

While there is not a discrete hotspot with an elevated heat flux, the power dissipation by the multiple transistors constituting the IGBT chip creates a parabolic temperature distribution, with the maximum at the center, as can be seen in Figure 20. Therefore, similar to the other thermoelectric hotspot cooling studies discussed in this section, the thin film thermoelectric cooler was used to reduce the temperature rise at the center of the IGBT, thus reducing the amount of work that needed to be done by the liquid cooled cold plate. Figure 20 shows a case where the IGBT is dissipating a uniform heat flux of 100W/cm^2 and a superlattice thermoelectric cooler, consisting of a 16 x 16 array of elements, is being used. It can be seen that increasing the current supplied to the TEC increases the temperature reduction at the IGBT and that a current of approximately 5.5 amps results in the most isothermal temperature distribution. Additionally, the fact that larger currents can further reduce the temperature of the center portion of the IGBT suggests that even higher heat fluxes could be removed.

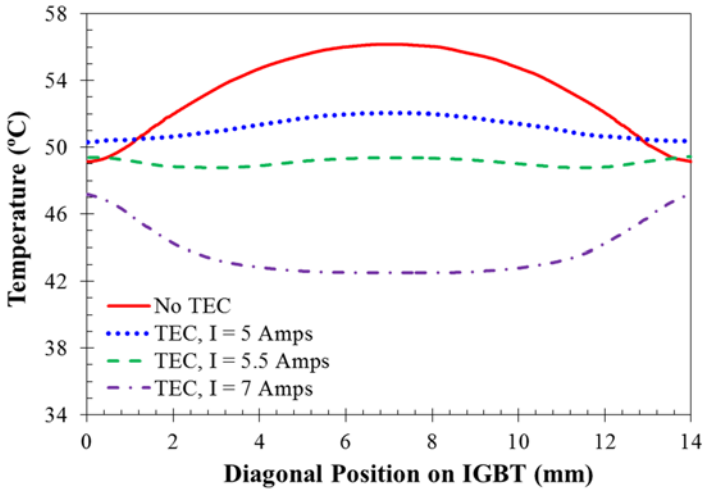


Figure 20. Temperature distribution along the bottom of the copper layer in the DBC substrate attached to the IGBT chip for various applied currents [50].

Figure 21 shows the temperature distribution along the bottom of the IGBT chip as function of applied current for the configuration with the TEC embedded in the base of the liquid cooled cold plate, with the IGBT dissipating 100W/cm^2. Even with the thermoelectric cooler farther away from the heat source, it can be seen that the TEC greatly reduces the spatial temperature variation in the chip. In order to further improve the cooling performance of the TEC embedded in the cold plate, trenches in the DBC substrate were proposed in order to reduce lateral heat spreading and concentrate the thermoelectric cooling onto the center of the IGBT chip. Finally, it was reported that using the liquid cold plate – thermoelectric cooler hybrid system, 94% of the temperature non-uniformity could be removed when the IGBT was dissipating 100W/cm^2 and 91% of the temperature non-uniformity could be removed when the IGBT was dissipating 200W/cm^2. Table II summarizes the thin film hotspot cooling studies discussed in this section.

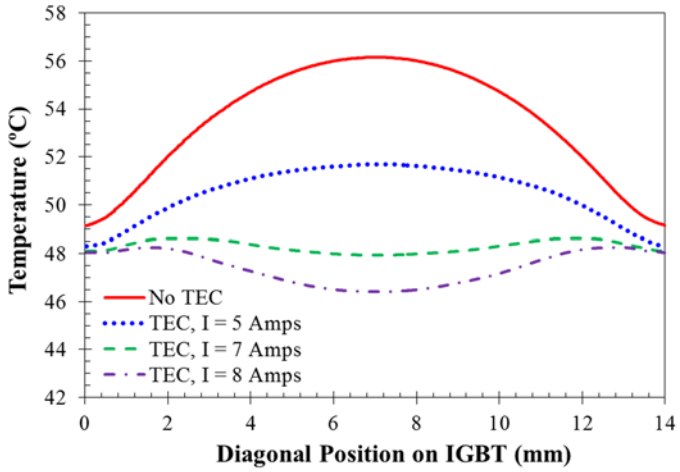


Figure 21. Temperature distribution along the bottom of the copper layer in the DBC substrate attached to the IGBT chip for various TEC currents, when the TEC is embedded in the bottom of the liquid cooled cold plate [50].

Table II. Summary of recent thin film thermoelectric hotspot cooling studies.

Researcher and Year	Classification	Materials	Hotspot Heat Flux [W/cm^2]	Max Hotspot ΔT [K]	Hotspot Size [μm^2]
Chau *et al.* – 2006 [47]	Thin Film	Not reported – Theoretical	1875	16	400x400
Ramanathan *et al.* – 2006 [48]	Superlattice/ Thin Film	Not reported – Theoretical	800	17	500x500
Chowdhury *et al.* – 2009 [35]	Superlattice/ Thin Film	Bi_2Te_3/Sb_2Te_3 (p), $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ (n)	1300	15	400x400
Gupta *et al.* – 2011 [49]	Superlattice/ Thin Film	Bi_2Te_3	1250	15	400x400
Wang *et al.* – 2013 [50]	Superlattice and Thin Bulk	Bi_2Te_3 (Bulk and superlattice)	N/A	N/A	N/A

2.5 Transient Thermoelectric Cooling

2.5.1 Freestanding Transient Thermoelectric Cooling

Transient, or pulsed, thermoelectric cooling has been an area of considerable interest due to the potential to achieve cold junction temperature reductions beyond what is possible in steady state operation [51]-[53]. As discussed, Peltier cooling is a surface effect, which occurs at the interface of the semiconductor and the metal at the cold junction of the thermoelectric circuit. Joule heating, on the other hand, is a volumetric effect, which is generated throughout the semiconductor and metal volume. Due to the spatial disparity in the origin of these two effects, it takes time for the volumetric joule heating to diffuse to the cold junction. Therefore, short periods of Peltier cooling with minimal parasitic Joule heat are possible, resulting in temperature reductions beyond what is possible under steady state operation. Transient operation of thin film thermoelectric coolers is also advantageous due to the relatively fast thermal response time, typically ranging from microseconds to milliseconds [11], [54].

Figure 22 shows the typical temperature response of a thermoelectric cold junction when a short current pulse is applied. Peltier cooling occurs immediately at the cold junction, resulting in the initial rapid decrease in temperature, often referred to as transient "super cooling." The cold junction reaches a minimum transient temperature and then begins to rise, due to the diffusion of Joule heating created throughout the volume of the device. Even after the current pulse magnitude is stepped back down, excess Joule heat continues to diffuse to the cold junction, resulting in a post-pulse overshoot temperature. After reaching the peak overshoot temperature, the cold junction of the device begins to settle back to the original steady state temperature.

As will be presented in this section, the magnitude, duration, and profile of the current pulse, as well as the geometry of the device, all have an effect on the overall transient behavior.

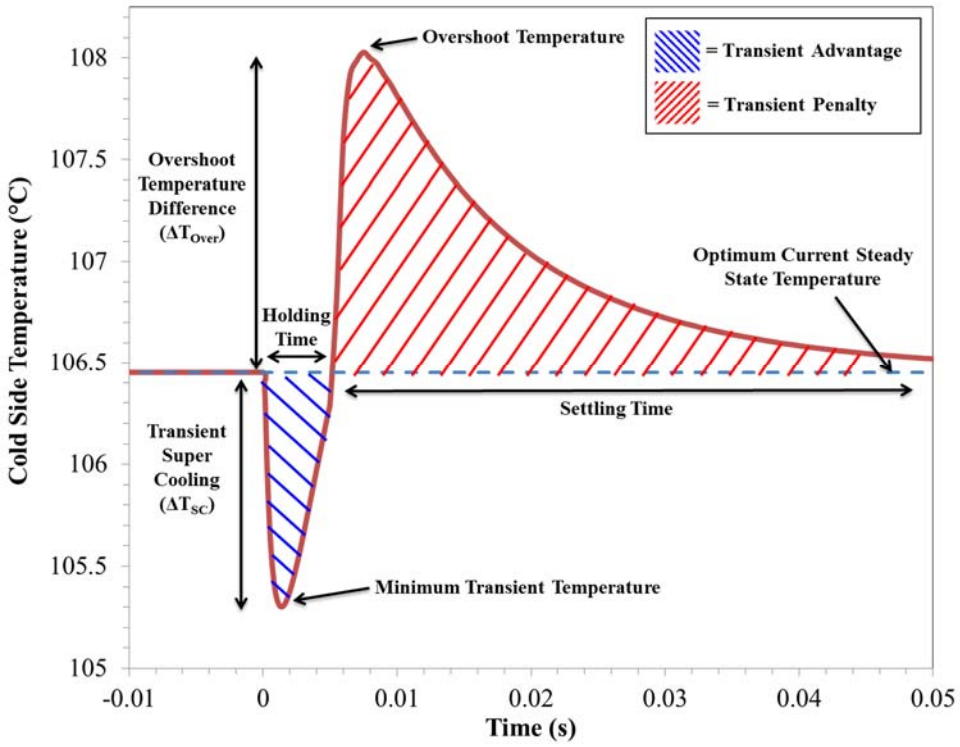


Figure 22. Typical temperature response of the cold side of a thermoelectric device to a current pule, with important metrics labeled [55].

Snyder *et al.* fabricated a thermoelectric device consisting of an n-type $Bi_2Te_{2.85}Se_{0.15}$ and a p-type $Bi_{0.4}Sb_{1.6}Te_3$ element connected with a copper foil, creating a cold junction, as shown in [56]. The hot side of the device was attached to an isothermal heat sink, which could be adjusted to temperatures ranging from -30ºC to 55ºC. Each thermoelectric leg was 5.8mm tall and had a cross section of 1mm x 1mm and a thermocouple with a diameter of 25µm was soldered to the cold junction to measure temperature. The device was initially supplied with the optimum steady state current, I_{max}, which produced the maximum ΔT in steady state operation. The current

was then stepped up to I_{pulse}, a value 2.5 times greater than I_{max}, for a short period, before being stepped back down to I_{max}.

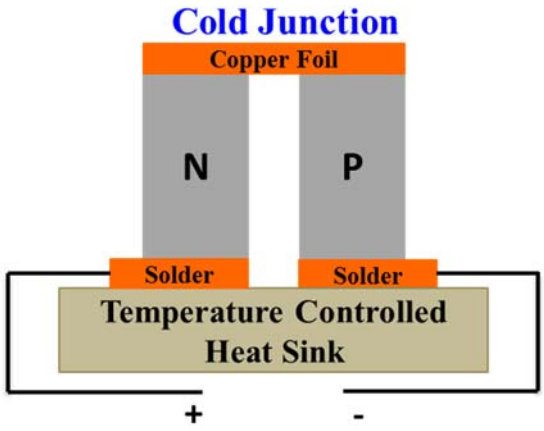


Figure 23. Schematic of the thermoelectric couple used by Snyder *et al.* for transient behavior characterization [56].

The resulting temperature response at the cold junction of the thermoelectric couple was similar to that shown in Figure 22, consisting of an initial burst of Peltier cooling during the pulse, followed by an increase in temperature due to Joule heating after the current pulse. The magnitude of the pulse current, I_{pulse} was varied and it was found that increasing I_{pulse} generally led to more rapid and larger initial temperature reduction, as shown in Figure 24. However, it can be seen that there are diminishing returns, and after a P of approximately 4, increasing the current pulse magnitude only causes slightly more cooling. Additionally, since increasing I_{pulse} increases the amount of Joule heating produced, the post pulse overshoot temperature increased with increasing pulse magnitude.

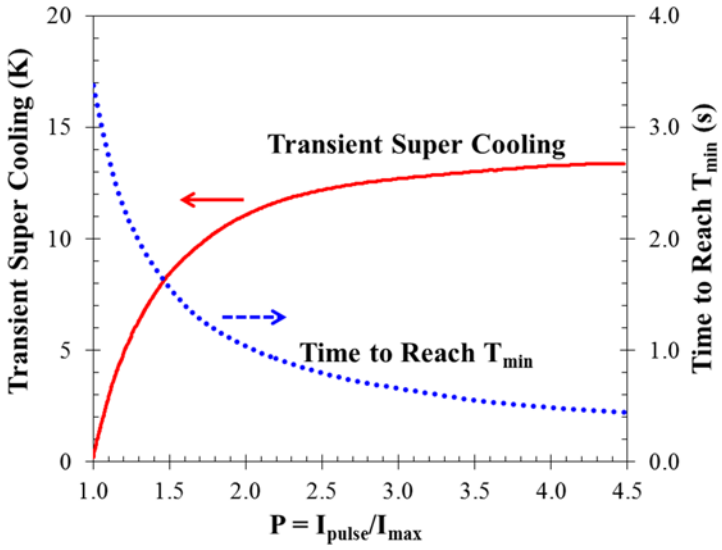


Figure 24. Dependence of transient "super cooling" and time to minimum temperature on applied current magnitude. Large currents cause a larger and more rapid temperature decrease [56].

Yang *et al.* also performed an extensive study on transient thermoelectric cooling, consisting of a numerical model and an experimental validation [57]. The numerical results were compared with theoretical models and results similar to Snyder *et al.* were found, such as larger current pulse magnitudes leading to larger initial temperature reductions, but with diminishing returns. It was theorized that varying the cross sectional area of the thermoelectric elements, thus altering the thermal resistance for Joule heat to flow to the hot and cold junctions, could be exploited in order to improve the transient performance of thermoelectric device.

A narrower cross sectional area near the cold junction would increase the thermal resistance for Joule heat to conduct to the cold side, however a narrower area also produces additional Joule heating. Therefore, a balance of Joule heating and conductive thermal resistance determines transient behavior. Figure 25 shows the cold junction temperature and normalized holding time as a function of the ratio of hot side

cross sectional area to cold side cross sectional area, for a tapered thermoelectric leg. The holding time is normalized against a cylindrical thermoelectric leg with a cross section equal to the average cross section of the tapered element. It can be seen that when the cold side area is larger, the holding time, meaning the amount of time the temperature is below the steady state value, is maximized, but there is very little temperature reduction. Conversely, when the hot side area is larger, holding time is reduced, but larger temperature reductions are possible.

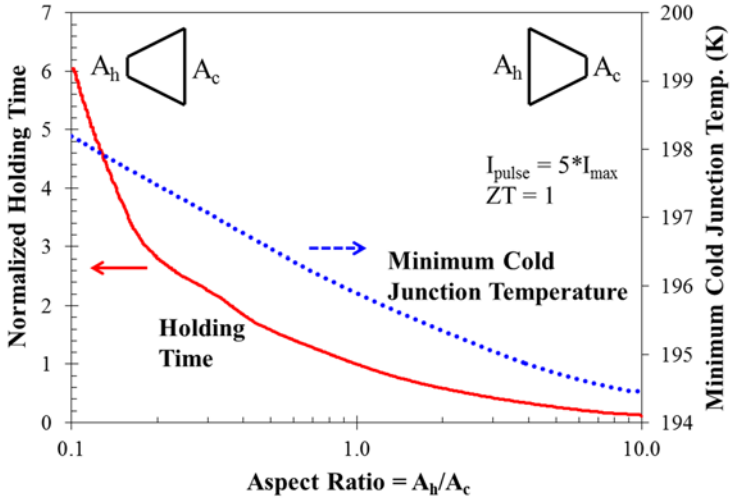


Figure 25. Dependence of holding time and minimum cold junction temperature on of the ratio of hot side to cold side cross sectional area. Larger hot side areas result in increased temperature reductions, but also reduce the holding time [57].

Similar to Snyder *et al.*, Yang *et al.* carried out a transient thermoelectric experiment, consisting of a single thermoelectric couple, made of two Bi_2Te_3 legs electrically connected with a copper sheet. The thermoelectric legs were 6mm tall, with a cross sectional area of 1mm x 1mm and the copper sheet was 3.5mm x 2.5mm, with a thickness of 35μm. Figure 26(a) shows an image of the thermoelectric couple tested by Yang *et al.* and Figure 26(b) displays the experimental results. The temperature of the cold junction is shown as a function of time when current magnitudes of 2, 3, 4,

and 5 times the optimum steady state current are applied. Good agreement with the numerical model was found and, as previously discussed, larger pulse currents resulted in more rapid and larger temperature reductions, but also caused larger post pulse overshoot temperatures.

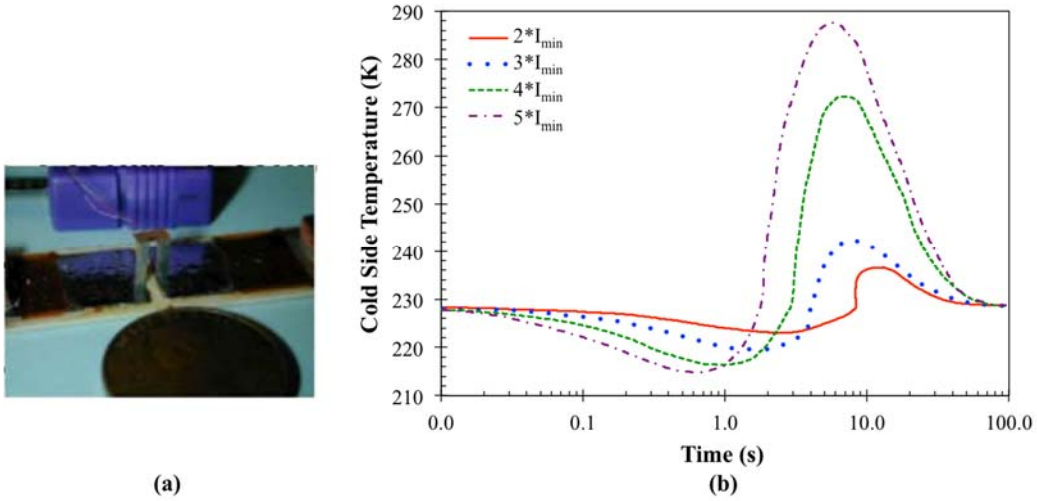


Figure 26. (a) Image of experimental thermoelectric couple and (b) transient temperature response to several different magnitude current pulses. Larger current pulses result in larger and more rapid temperature reduction, but also lead to increased overshoot temperature rise [57].

All of the current pulses discussed up to this point have been square pulses, consisting of step changes in current; however more complex current pulse profiles are possible. Thonhauser *et al.* numerically studied the effect of alternative pulse shapes on the transient behavior of a thermoelectric cooler [58]. Similar to previous studies, a single thermoelectric couple, consisting of an n and a p-type leg was used in the model. The thermoelectric elements were assumed to be made of Bi_2Te_3, with a ZT of 1, and have a thickness of 200μm. Figure 27(a) shows the alternate current pulse profiles considered in the study. The current pulse duration was 500μs and the maximum pulse magnitude is 11.7 times that of the steady state optimum current for all the cases.

Figure 27(b) shows the temperature response at the cold junction of the thermoelectric device as a function of time for the various current pulse shapes. It can be seen that a step change in current is actually the least efficient current shape and alternative profiles, such as $P \alpha t^3$, produce comparable reductions in temperature at the cold junction, with significantly less post pulse overshoot temperature rise. Other profiles, such as the $P \alpha t^{1/3}$, produce longer duration decreases in cold side temperature than the t^3 case, however they also result in larger post pulse temperature overshoots. From these results, it is clear that certain current profiles result in more efficient cooling with sustained temperature reductions and minimal temperature rise after the pulse.

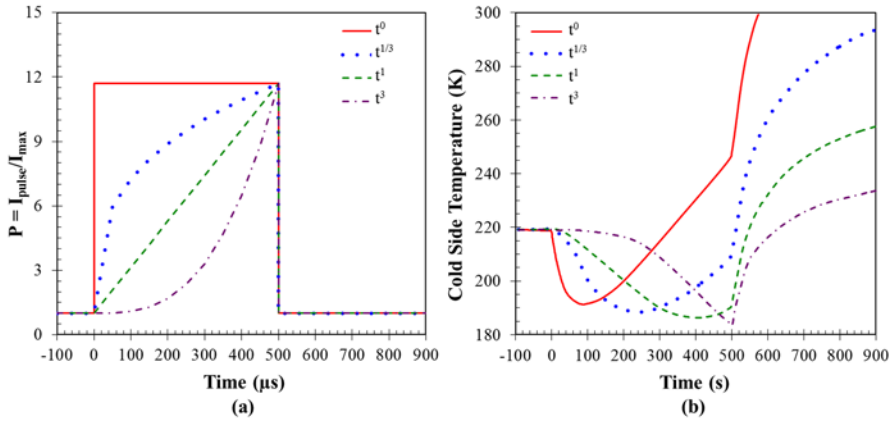


Figure 27. (a) Applied current profile and (b) transient temperature response at the cold junction of a thermoelectric couple when each current pulse profiles is applied for a duration of 500μs. The step current results in the largest temperature rise after the current pulse [58].

2.5.2 Transient On Chip Cooling Thermoelectric Cooling

The previous section focused on transient thermoelectric behavior of freestanding devices and provided insight into the physics involved in transient thermoelectric cooling, consisting of the temporal and spatial interplay of Peltier cooling and Joule heating. However, the transient behavior of a thermoelectric cooler

embedded in a thermal management system for dynamic cooling of an electronic device is of particular engineering interest. Gupta *et al.* performed numerical simulations on transient cooling using a 100µm thick superlattice thermoelectric cooler embedded in a configuration similar to that shown in Figure 13.

The thermoelectric device was used to cool a 400µm x 400µm hotspot with a heat flux of 1250W/cm^2 and it was found that pulsed operation could provide an additional 6K to 7K of hotspot cooling, beyond what is possible in steady state [49]. Similar to the previously discussed studies, I_{max} is the current that maximizes steady state hotspot cooling, and is equal to 3 amps in this example, while I_{pulse} is the magnitude of the current pulse. Figure 28 shows the applied current profile and the corresponding hotspot temperature response and it can be seen that the hotspot temperature behavior is analogous to the behavior at the cold junction of a freestanding thermoelectric cooler discussed is the previous section.

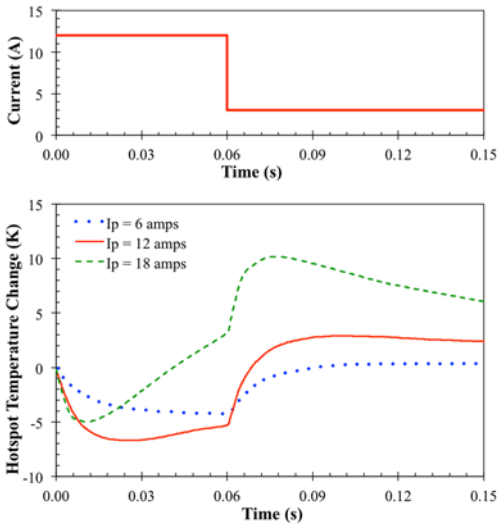


Figure 28. Applied current profile and hotspot temperature over time when three different magnitude current pulses are applied to an embedded thermoelectric cooler [49].

When the current pulse is first activated, there is a burst of Peltier cooling, resulting in an initial decrease in hotspot temperature. However, the elevated current produces excess Joule heating, which drives up the temperature of the hotspot after the pulse. Increasing the current pulse magnitude from 6 amps to 9 amps increases the temperature reduction at the hotspot, but after a current of approximately 12 amps, increasing the current magnitude farther actually reduces the amount of transient hotspot "super cooling". There is also an inflection point in the hotspot temperature response curve at 0.06 seconds. The sudden increase in slope is due to the current magnitude being stepped back down from I_{pulse} to I_{max}, which reduces the amount of Peltier cooling. The Joule heating created during the pulse continues to diffuse to the hotspot, thus the reduction in Peltier cooling with continued Joule heat conduction, causes the sharp increase in hotspot temperature.

Similar to the results discussed for a free standing thermoelectric device, Figure 29 shows the time to reach the minimum temperature, the maximum transient reduction in hotspot temperature, and the post-pulse overshoot temperature rise as a function of pulse magnitude. Over the range shown, increasing the current magnitude causes larger and more rapid hotspot temperature reductions, however there are diminishing returns and the overshoot temperature increases exponentially with larger currents.

In thin film devices, interface resistances begin to play a dominant role and limit performance more than bulk properties. Therefore, the effect of electrical and thermal contact resistance, at the thermoelectric element to metal interface was also studied. Figure 30(a) shows the maximum hotspot temperature reduction and the post pulse overshoot temperature as function of thermal resistance for a pulse magnitude of 12

amps and a duration of 0.04 seconds. Increased thermal resistance significantly degrades the ability of the thermoelectric cooler to reduce the hotspot temperature and results in modest increases in overshoot temperature. Similarly, as shown in Figure 30(b), large electrical contact resistances generate additional Joule heating, leading to less hotspot cooling and larger overshoot temperatures.

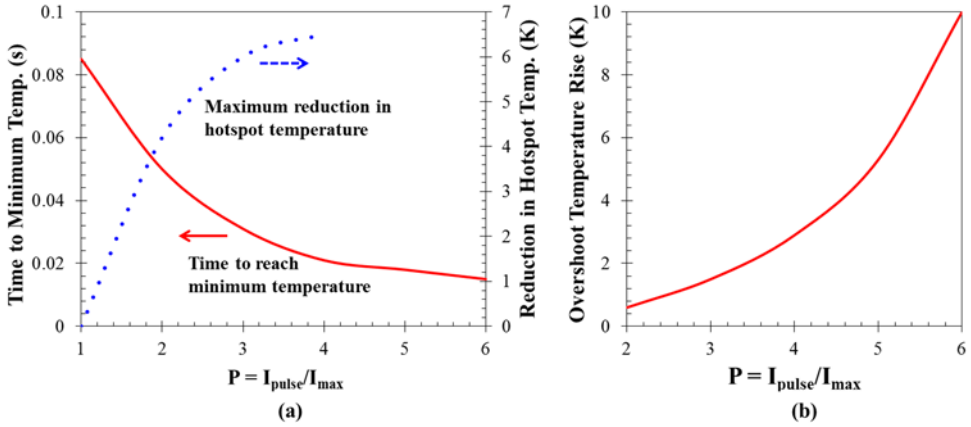


Figure 29. Dependence of (a) time to reach minimum hotspot temperature, maximum reduction in hotspot temperature and (b) post pulse hotspot temperature rise on current pulse magnitude [49].

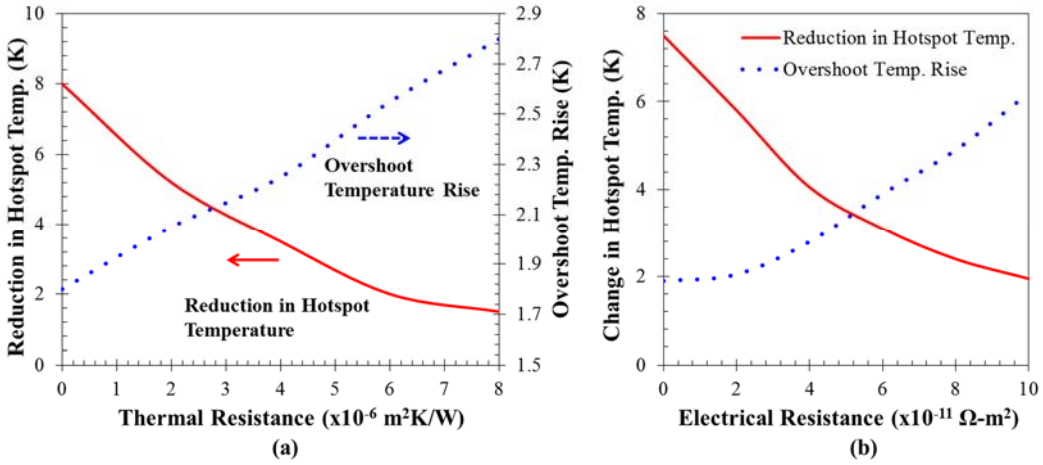


Figure 30. Hotspot temperature reduction and post pulse hotspot temperature rise as a function of (a) thermal resistance and (b) electrical resistance [49].

3 Monolithic Thermoelectric Cooler

3.1 Introduction and Motivation

The monolithic configuration is a novel approach to thermoelectric cooling, in which there is no discrete thermoelectric module; rather, the semiconductor substrate itself is used as a leg in the thermoelectric circuit [59], [60]. Figure 31 shows a top and section view of a monolithic cooler, with the active electronic components on the bottom of the substrate, producing the background and hotspot heat fluxes. A layer of metallization is deposited on the top of the substrate, such that if a voltage is applied, current flows from the larger outer electrode to the smaller center electrode. The current becomes concentrated at the center electrode, producing localized Peltier cooling, thus the center electrode is referred to as the 'microcooler.'

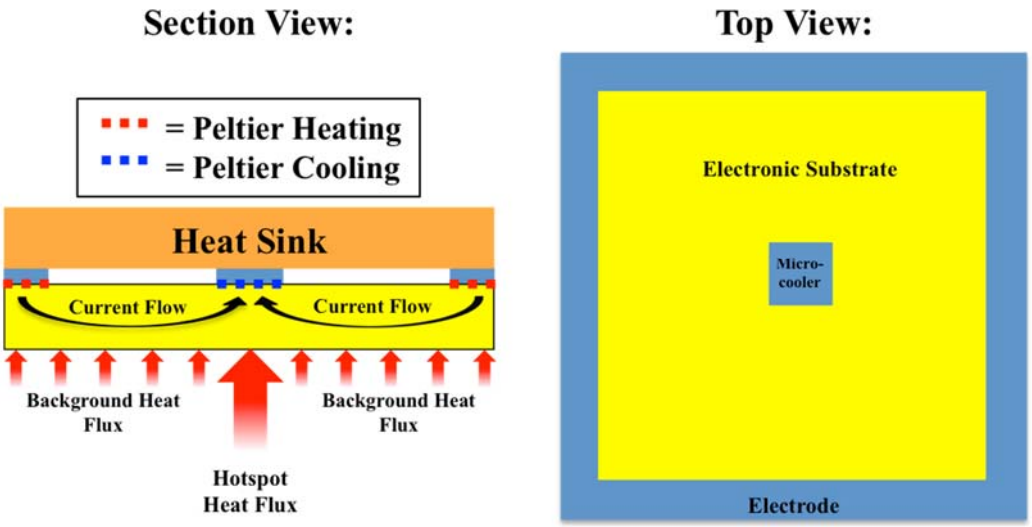


Figure 31. Section and top view (heat sink removed for clarity) of the monolithic cooling configuration. Current flows from the outer ring electrode to the center electrode creating localized Peltier cooling at the center of the chip [55].

As discussed, when a discrete thermoelectric cooler is used for hotspot temperature reduction, there is a thermal interface resistance where the cooler makes

contact with substrate. The thermal interface resistance can significantly degrade the hotspot cooling and becomes increasing problematic as the contact area becomes smaller. A major advantage of the monolithic cooling configuration is that it removes the thermal resistance typically found between a thermoelectric cooler and the substrate. The Peltier cooling occurs at the interface of the semiconductor and the metal, thus there is no thermal interface resistance impeding the flow of heat out of the substrate. Additionally, the monolithic cooling configuration only requires a thin layer of metallization on the inactive side of the chip, allowing it be easily integrated into the overall thermal management system. As discussed in Section 2.1.2, due to the more complex role played by thermal conductivity, the power factor, as shown in Equation 3, is a more suitable figure of merit for the monolithic cooling configuration.

3.1.1 Experimental Demonstrations in the Literature

In 2004, Zhang *et al.* fabricated a silicon based monolithic cooler, which produced 1.2K of cooling over a 40µm x 40µm area, with an estimated cooling flux of 580W/cm^2 [61]. The cooler was fabricated on p-type, boron-doped silicon, with electrical resistivity ranging from 0.001 to 0.006 Ω-cm. Figure 32 shows a cross section of the monolithic coolers fabricated by Zhang. Current flows down the metallic layer and enters the silicon substrate at the mesa, producing localized Peltier cooling. Various cooler sizes were fabricated ranging from 40µm x 40µm to 75µm x 75µm and it was found that smaller coolers resulted in larger temperature reductions and cooling fluxes. The cooling performance of the 40µm x 40µm and 60µm x 60µm devices, as a function of applied current, is shown in Figure 33 [61].

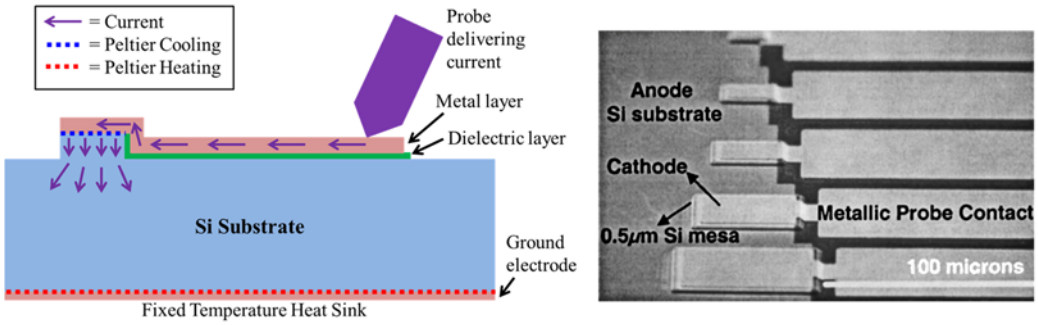


Figure 32. Section view and SEM image of the monolithic coolers fabricated by Zhang [61]

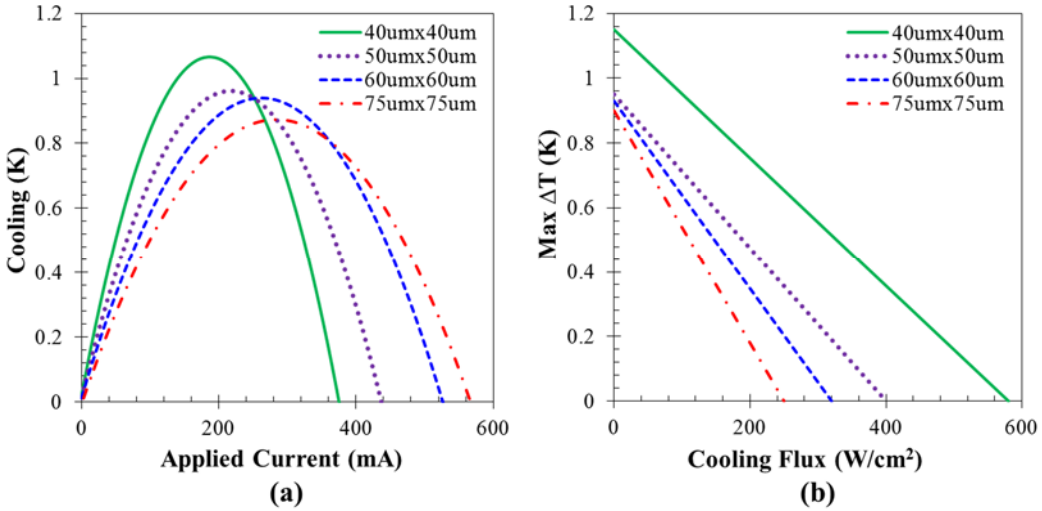


Figure 33. (a) Temperature reduction at the cooler as a function of (a) applied current and (b) cooling flux for the monolithic cooler [61].

In 2006, Zhang's work was extended and a monolithic cooler with a superlattice cap was fabricated [62]. As previously discussed, superlattice structures can enhance thermoelectric properties, resulting in improved cooling performance. Figure 34 shows a schematic of the monolithic coolers and it can be seen that the overall structure is very similar to the previous generation, except for the addition of the superlattice cap and associated layers. A variety of monolithic coolers were fabricated, all with footprints in the vicinity of 100µm x 100µm.

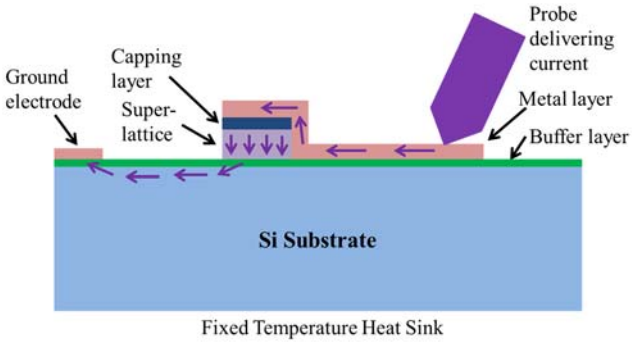


Figure 34. Schematic of the monolithic cooler with a superlattice layer [62].

The superlattice greatly improved the cooling performance of the monolithic device, resulting in temperature reduction of up to 4.5K at the cooler, as shown in Figure 35 [62]. It should be noted the optimum cooler size shifts from 40µm x 40µm in the 2004 study, to 60µm x 60µm in the 2006 work. One explanation for this shift could be the balance of spreading resistance and thermal and electrical interface resistances. Smaller coolers typically produce larger temperature reductions at the cooler because there is an increased spreading resistance. However, electrical and thermal contact resistances also have a more pronounced effect at smaller coolers sizes, thus the balance of these two effects contributes to the optimum cooler size.

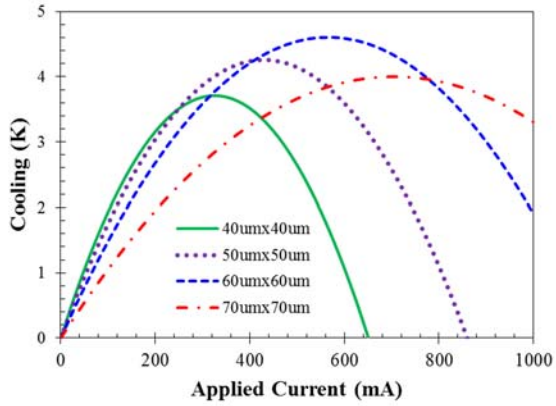


Figure 35. Temperature reduction at the cooler as a function of applied current for various cooler sizes. There is an optimum cooler size, which maximizes cooling [62].

3.1.2 Numerical Optimization in the Literature

Wang *et al.* simulated a monolithic cooler on a highly doped silicon wafer, consisting of a structure similar to that shown in Figure 31. A 3D analytical model was used to perform a parametric study and explore the ability of the monolithic cooler to reduce the temperature of a 700W/cm^2 hotspot [59], [63]. Coolers sizes ranging from 250μm x 250μm to 4000μm x 4000μm were studied along with chip thickness of 100μm to 500μm. The non-uniform Joule heating produced in the monolithic cooling configurations makes purely analytical solutions difficult, therefore numerically determined Joule heating allocation factors were used to account for the amount of Joule heating reaching the hotspot and microcooler.

In the geometric portion of the parametric study it was found that the optimum micrcooler size, which resulted in the largest hotspot temperature reduction, was typically 5 to 6 times the die thickness. Another portion of the parametric study explored the relationship between the optimum doping concentration and parasitic effects, such as electrical contact resistance. It was found that electrical contact resistances greater than $10^{-6}\Omega$-cm^2 could significantly degrade hotspot cooling and that high electrical contact resistance decreased hotspot cooling more severely in smaller coolers [59].

3.1.3 Transient Operation in the Literature

As previously discussed, transient thermoelectric cooling is an area of intensive research due to the potential to achieve hotspot reduction beyond what is achievable in steady state operation. However, there is very limited data available in the literature focusing on transient operation of a monolithic cooler, consisting mainly of a study

performed by Ezzahri *et al.* In this study, the transient performance of a silicon based monolithic cooler with a superlattice cap, similar to the configuration shown in Figure 34 [54], [64]. Figure 36 shows the temperature response of an 80µm x 80µm cooler when a 1.7 amp pulse, with a duration of 166µs, is applied. Similar to the transient behavior observed in traditional thermoelectric modules, there is an initial decrease in temperature at the cooler due to Peltier cooling, followed by an increase in temperature due to the diffusion of Joule heating generated throughout the volume. Cooler sizes ranging from 20µm x 20µm to 100µm x 100µm were fabricated and tested and it was found that larger coolers tend to result in slower but larger temperature reductions.

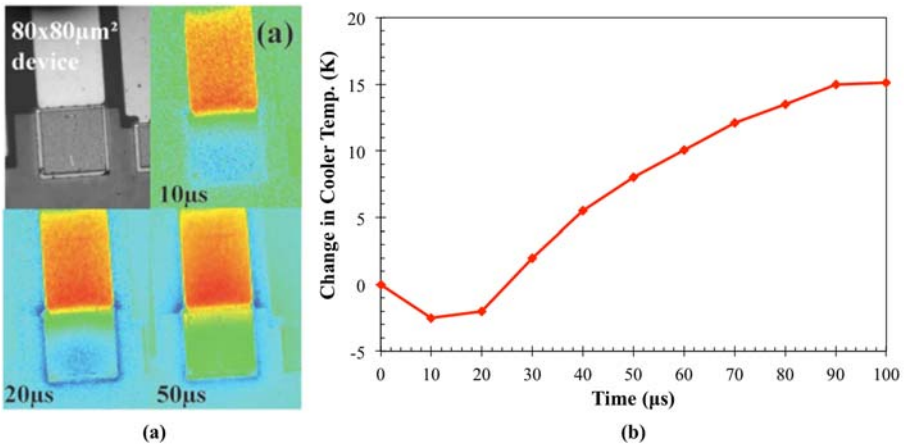


Figure 36. (a) Thermal images and (b) plot showing temperature over time for a monolithic cooler subjected to a current pulse [54].

3.2 Numerical Study of On Chip Monolithic Hotspot Cooling

Numerical modeling provides a powerful tool, as it allows for the study of thermoelectric behavior that is difficult to capture experimentally, such as transient operation and monolithic cooling on non-silicon substrates. Previously, numerical simulations had been performed at the University of Maryland on steady state monolithic cooling on silicon and germanium substrates. Therefore, the previous

studies served as a baseline for comparisons to numerical results for three new aspects of monolithic thermoelectric cooling, which consisted of transient thermoelectric "super cooling" produced by an applied current pulse, anticipatory thermoelectric cooling of dynamic hotspots, and monolithic cooling of kW/cm^2 hotspot on novel substrates, such as Si/SiC superlattices.

3.2.1 Transient Thermoelectric "super cooling" Using an Applied Current Pulse

The transient behavior of a thermoelectric cooler is inherently linked to steady state optimum conditions. Prior work, notably [63], [65], has revealed that for a given geometry there is an optimum current that provides the maximum reduction in steady-state hotspot temperature. In order to familiarize the reader with previous self-cooling results, Figure 37 shows the steady state temperature distribution along the bottom of the 100μm thick germanium die for various applied currents with a 600μm by 600μm microcooler. For this geometry, the optimal cooling current is approximately 1.25 amps and the peak hotspot temperature is reduced from 111.3°C to 106.8°C, a temperature reduction of 4.5K. It is clear that applying currents larger or smaller than the optimal current will result in less effective hotspot cooling.

As previously discussed, current that was applied using the large ring electrode flowed through the germanium die, and became concentrated at the smaller center electrode, producing localized Peltier cooling, drawing heat from the surrounding substrate and reducing the hotspot temperature. The Peltier heating and cooling were calculated based on the applied current and operating temperature and input into the model as heat flux boundary conditions while ANSYS was used to calculate the non-uniform joule heating resulting from the applied current.

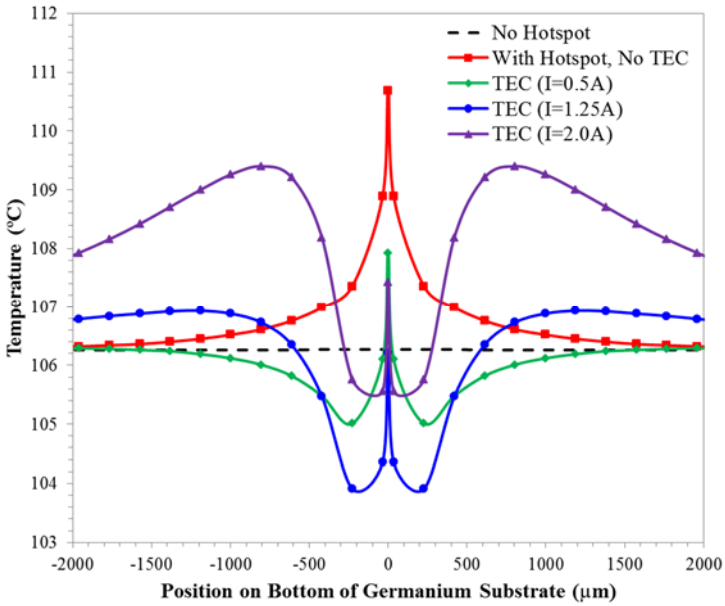


Figure 37. Steady state temperature distribution along the bottom of a self-cooled

Solid69 thermal-electric elements were used in the simulation and the full model consisted of approximately 400,000 elements. The mesh was constructed such that it is densest around the microcooler and hotspot, where the largest temperature gradients occur. Due to symmetry in the geometry, it was possible to analyze just a quarter of the structure and the number of elements was reduced to approximately 120,000 elements. A mesh refinement showed that increasing the quarter model element count from 120,000 to 440,000 elements resulted in just a 0.09K discrepancy in the calculated hotspot temperature. Thus, a quarter model of approximately 120,000 elements was utilized in the study and the results were validated qualitatively with published ANSYS Inc. results and with published experimental data [56], [57], [67].

Before studying pulsed thermoelectric cooling, the hotspot temperature was studied during the initial turn on of the monolithic cooler. In this case, the initial condition consisted of the temperature distribution resulting from the hotspot and

background heat fluxes, with no thermoelectric cooling. The current supplied to the monolithic cooler was then increased and the hotspot temperature was recorded until a steady state condition was reached, as shown in Figure 38.

An immediate steep drop in temperature is observed for all 4 currents, followed by a continued asymptotic temperature decline for the 2 lower magnitude currents and an increase in temperature for the 2 higher magnitude currents. Thus, for 0.5A and 1.25A the minimum temperature of 108.5°C and 106.4°C, representing 2.7K and 4.8K of cooling, are achieved at the new steady state conditions, while for 2A and 2.75A the initial minimum temperature of 106.4°C and 106.7°C, respectively, is rapidly exceeded as the temperature rises towards the new steady-state values of 108.1°C and 111.8°C, respectively.

As previously mentioned, the optimal steady state cooling current for this configuration is 1.25 amps. It can be seen that applying a current that is less than the steady state optimal current causes the hotspot temperature to asymptotically approach a temperature that is warmer than produced by the optimal current, while applying a current that is larger than the optimum steady state value, results in the hotspot temperature decreasing more quickly than in the steady state optimum case. However, this larger current produces additional Joule heating which, within approximately 5 milliseconds, causes the hotspot temperature to rise. Moreover, the hotspot temperature for the larger current approaches a steady state temperature that is significantly greater than the steady state optimal hotspot temperature.

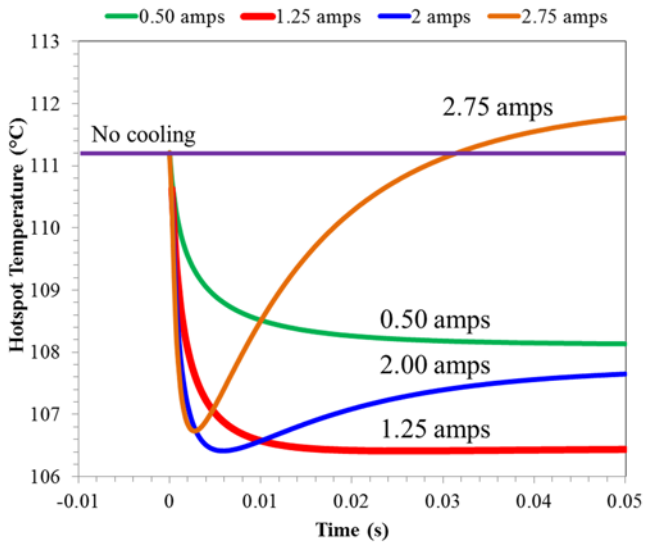


Figure 38. Hotspot temperature over time for various applied currents with no current/no cooling as initial condition.

For the pulsed thermoelectric "super cooling" study a germanium die, with a thickness of 100µm, and a 600µm by 600µm microcooler was used, with the steady-state temperature distribution created by the optimum steady state current of 1.25A serving as the initial condition for the transient analysis. A square current pulse of magnitude greater than 1.25 amps was applied to the model for a short period of time, and then the current was lowered back to the optimal steady state current of 1.25 amps.

In order to effectively capture the competing aspects of the transient response of a hotspot to a dynamically controlled germanium self-cooler, beyond limiting the maximum temperature and temporarily reducing the hotspot temperature, several novel metrics were used and are described in Table III, as well as displayed in Figure 39. The Transient Advantage (TA) metric, shown as the blue cross-hatched area in Figure 39, integrates the "super cooling" and holding time into one metric, providing the cumulative temperature reduction benefit achieved by the cooler, relative to the steady-state temperature. Similarly, the Transient Penalty (TP), shown as the red cross-hatched

area in Figure 39, incorporates "overshoot" temperature and settling time into one metric, providing the cumulative temperature increase over the steady-state value and representative of the price paid for the dynamic operation of the microcooler at larger currents.

The effect of applied current pulse magnitude, current pulse duration, die thickness, and current pulse shape were studied and the transient behavior of both the hotspot and the microcooler will be discussed. Figure 40 shows that the center temperature of the hotspot and microcooler respond similarly, though not identically, when a current pulse is applied Therefore, it is reasonable to use the metrics described in Figure 39 and Table III to characterize the behavior at both the hotspot and microcooler.

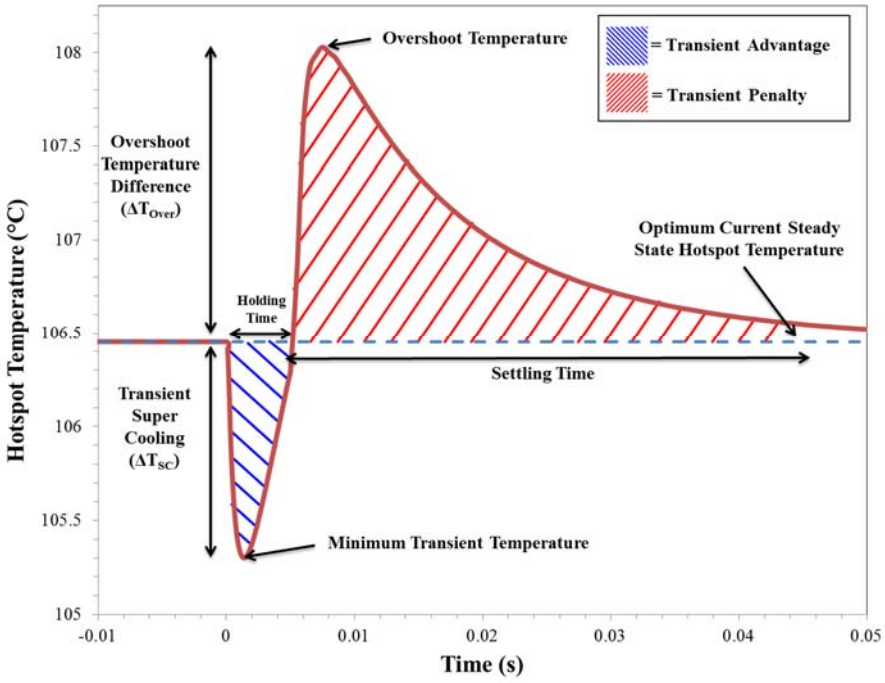


Figure 39. Key Metrics used for quantifying the transient behavior of a germanium self-cooler.

Table III. Metrics for characterizing the transient behavior of a germanium self-cooler.

Metric	Description
Optimum Steady State Current Hotspot Temperature ($T_{Hotspot,S.S.\ Optimum}$)	Steady state hotspot temperature when the optimum current is applied.
Minimum Transient Temperature ($T_{Transient\ minimum}$)	Minimum hotspot temperature after current pulse has been applied.
"Overshoot" Temperature ($T_{Overshoot}$)	Maximum hotspot temperature after current pulse has been applied.
Transient "Super Cooling" (ΔT_{SC})	Maximum temperature reduction below the steady state optimal current temperature. ($\Delta T_{SC} = T_{Hotspot,S.S.\ Optimum} - T_{Transient\ minimum}$)
Holding Time (t_H)	Duration of time the transient temperature remains below the steady state optimum temperature.
"Overshoot" Temperature Difference (ΔT_{over})	Maximum transient temperature above the steady state optimal current temperature. ($\Delta T_{Over} = T_{Overshoot} - T_{Hotspot,S.S.\ Optimum}$)
Settling Time (t_S)	The amount of time for the transient temperature to return to within 0.3% of the optimum steady state temperature.
Transient Advantage (TA)	The integrated area below the optimum steady state temperature and above the transient temperature curve (shown with blue hatching) with units of K-seconds
Transient Penalty (TP)	The integrated area above the optimum steady state temperature and below the transient temperature curve (shown with red hatching) with units of K-seconds
Pulses Cooling Enhancement (PCE)	Expresses the amount of transient cooling relative to steady state. $\left(PCE = \frac{Transient\ \ Super\ \ Cooling}{Steady\ \ State\ \ Temperatur\ e\ Reduction}\right)$

It will be shown that due to the nature of the transient thermoelectric effect as previously described, the transient thermoelectric effect is more pronounced at the microcooler than at the hotspot. When a current pulse is applied, cooling occurs instantaneously at the microcooler and the transient "super cooling" results from the time it takes for the Joule heating, produced throughout the volume, to diffuse to the microcooler. The hotspot is a small distance away from the cooler and, therefore, the cooling at the hotspot is somewhat delayed, relative to the instant cooling that occurs at the cooler, resulting in slightly less "super cooling" at the hotspot.

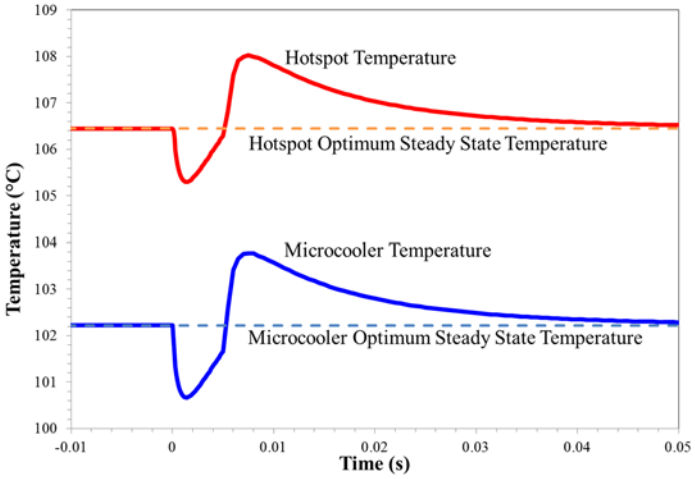


Figure 40. Transient temperature at the hotspot and the cooler as a function time during a current pulse.

Figure 41 shows the temperature distribution along the bottom of a germanium chip, with a thickness of 100μm and a cooler size of 600μm × 600μm, subjected to a temporarily elevated current. For additional clarity, Figure 42 displays contour plots of temperature for the area surrounding the hotspot at time steps of interest. A current pulse of 2.5 amps for a duration of 5 milliseconds, followed by a reduction to the optimal 1.25 amps, was applied in this part of the study.

The figures show the temperature distribution along the bottom of the chip for no thermoelectric cooling, along with the steady state profile for the optimal 1.25 amp current, and the temperature distribution associated with the minimum and maximum hotspot temperatures resulting from the 5 millisecond, 2.5 amps current pulse. It can be expected that after reaching the maximum value of 108.0°C, the hotspot temperature will decrease and approach that of the optimum steady state condition. The results indicate that the thermoelectric device can provide approximately 5ºC of cooling in steady state operation, completely removing the hotspot, though at the expense of slightly raised temperatures elsewhere. If a higher current is applied, the hotspot can be "super cooled" by up to an additional 1.5ºC, suggesting that a short duration, transient hotspot of higher heat flux or larger size could be suppressed with pulsed cooling.

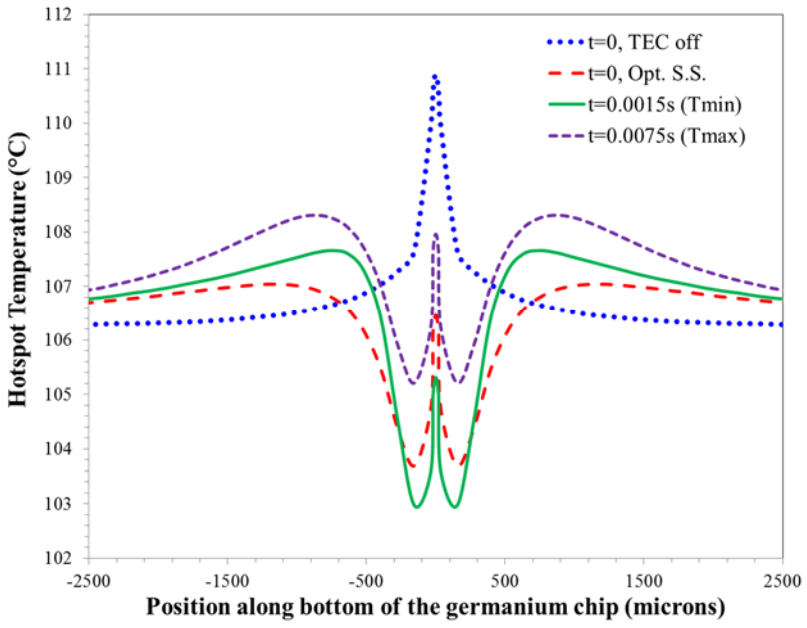


Figure 41. Temperature distribution along the bottom of the germanium chip for several time steps when a current pulse of magnitude 2.5 amps and duration of 5 milliseconds is applied.

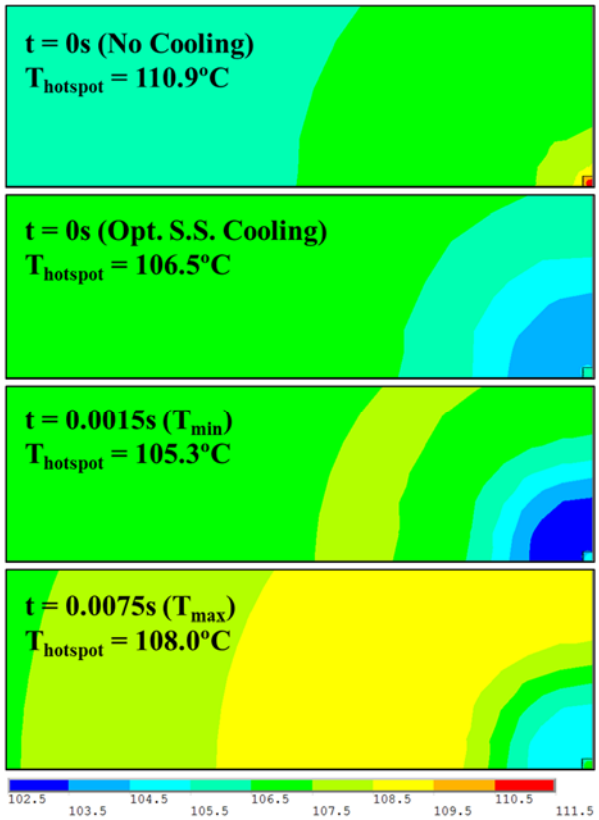


Figure 42. Contour plots of temperature along the bottom of the germanium chip. The small square in the lower right corner is the hotspot, and the plot shows the temperature distribution up to a radial distance of approximately 2500 microns.

The magnitude of the current pulse has a significant effect on transient cooling and the hotspot temperature over time for pulse magnitudes of 1.5, 2.5, and 3.5 amps is shown in Figure 43. It can be seen that increasing the current magnitude of the pulse initially produced larger and more rapid hotspot temperature reductions, but also led to hotter overshoot temperatures. For each pulse considered, once the pulse ends, and the current returns to the optimal level, there is a sudden sharp rise in temperature. This behavior is due to the diminished Peltier cooling but the continued diffusion of additional Joule heating (produced by the higher current) towards the hotspot. However, since the current has been reduced, the cooling and heating begin to re-equilibrate and after a short rise time, the hotspot temperature reaches its maximum

"overshoot" and then begins to decrease towards the original steady state temperature. A pulse duration of 5 milliseconds was used for all of the cases, unless stated otherwise.

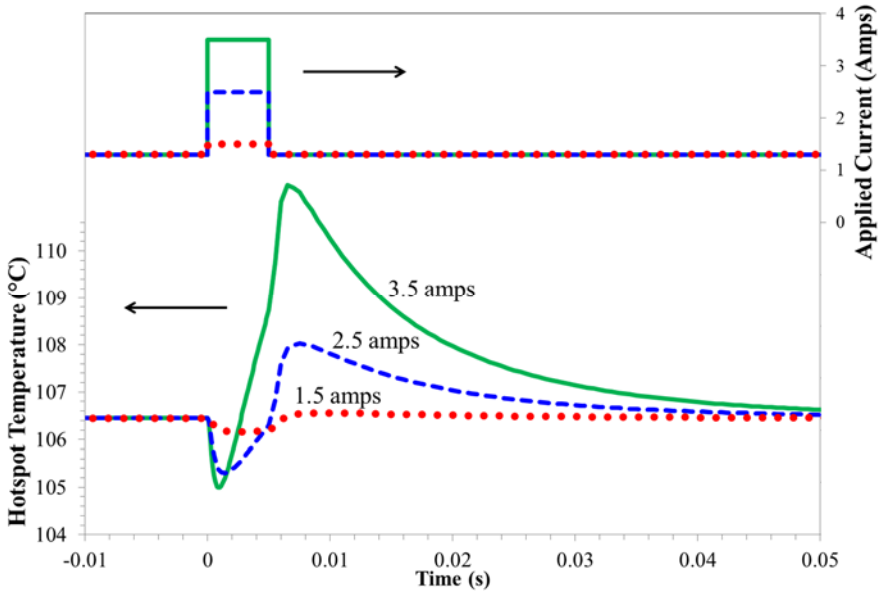


Figure 43. Transient hotspot temperature resulting from a 5 millisecond current pulse for a cooler size of 600µm x 600µm and a 100µm thick die.

Figure 44(a) shows the dependence of "super cooling" on the pulse magnitude. Increasing the pulse magnitude decreases the minimum hotspot and cooler temperature. However, for this pulse shape there are diminishing returns, especially at the hotspot. Due to the amount of volumetric Joule heating produced, using a pulse magnitude greater than 4.5 amps would result in very little additional "super cooling" and would incur a significantly higher overshoot temperature. For this geometry, i.e. a 600µm by 600µm cooler and 100µm thick die, the optimum steady state temperature reduction is 4.8K at the hotspot and 4.9K at the microcooler. Additionally, Figure 44 (b) shows the pulsed cooling enhancement, which can be seen to increase with larger pulse magnitudes.

Finally, Figure 45 shows the Transient Advantage and Transient Penalty as a

function of pulse magnitude for several different pulse durations. If a pulse duration greater than 1 millisecond is used, the optimum transient cooling advantage occurs at a pulse magnitude of 2.5 amps, while the Transient Penalty increases exponentially with pulse magnitude for all pulse durations. It can be seen that the ratio of Transient Advantage to Transient Penalty, representative of the overall transient effect, is on the order of 0.1 to 0.5 for all these cases, indicating that the Transient Penalty is typically greater than the Transient Advantage for a square current pulse.

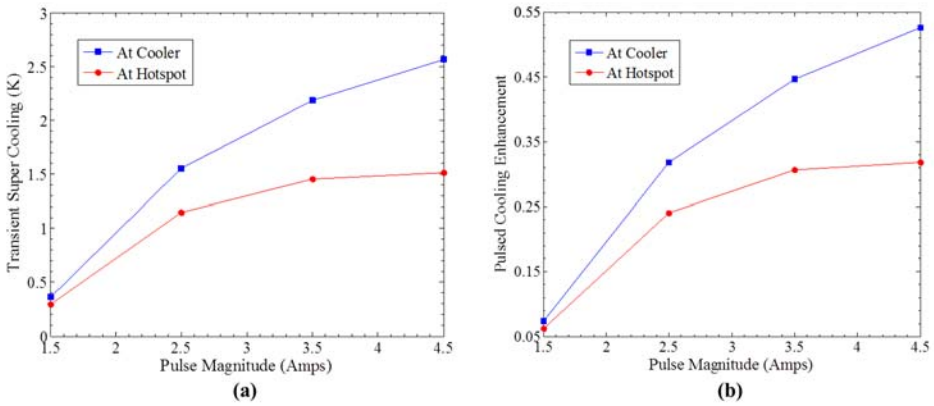


Figure 44. (a) Transient temperature reduction and (b) pulsed cooling enhancement as a function of pulse magnitude.

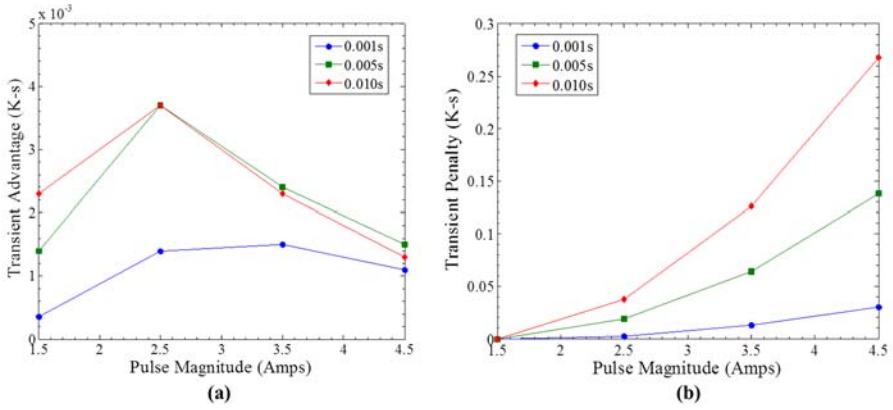


Figure 45. Dependence of (a) Transient Advantage and (b) Penalty on pulse magnitude for several different pulse durations.

The effect of current pulse duration was also explored and Figure 46 shows the temporal variation of the hotspot temperature for 1, 5, and 10 millisecond pulses of 2.5 amps, followed by a decrease to the optimal current of 1.25 amps. The hotspot temperature history for a constant current of 2.5 amps is also displayed and it can be seen that the temperature-time histories for the different pulse durations follow the same curve for the early part of the transient, decreasing for the first 2.5 milliseconds and then increasing with time past the minimum temperature. Since the different pulse durations follow the same curve, the length of the pulse does not have a significant effect on the minimum temperature achieved. However, the longer pulses produce more Joule heating, thus causing higher peak temperatures and longer settling times.

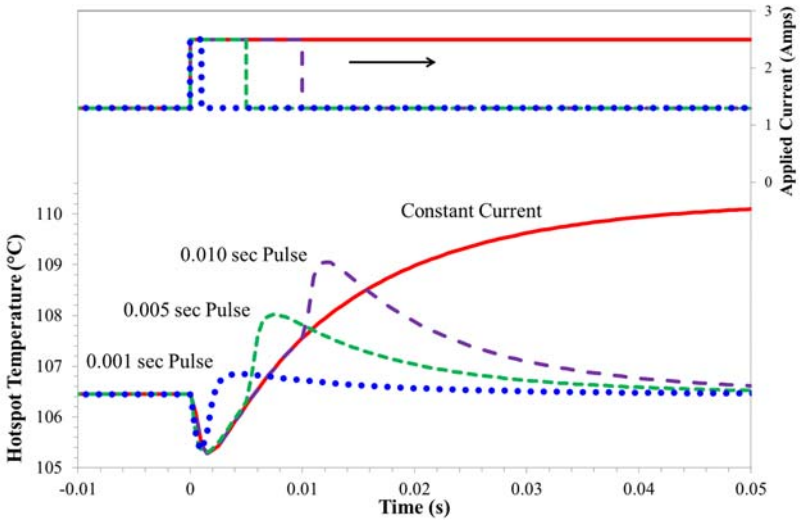


Figure 46. Hotspot temperature over time for a 2.5 amp current pulse for a cooler size of 600µm x 600µm and a 100µm thick die.

Figure 47 shows the effect of pulse duration on the Transient Advantage and Transient Penalty for 1.5, 2.5, and 3.5 amp pulses. It can be seen that for short times, increasing the pulse duration causes an increase in the Transient Advantage, due to the prolonged holding time at reduced temperature, but for longer times - when Joule

heating begins to dominate - no additional Transient Advantage is achieved with increased duration. The Transient Penalty increases nearly linearly with pulse duration due to the increased "overshoot" temperature and extended settling time. This behavior is a result of the increased Joule heating associated with longer duration current pulses. These results suggest that pulse magnitude plays a larger role in increasing Transient Advantage than pulse duration. The optimal pulse duration for this geometry and set of material properties is approximately 5 milliseconds, after which the holding time shows no additional benefit from a longer pulse. Progressing past this optimum will have no benefit, in terms of minimum transient temperature and holding time, and will have large adverse effects in terms of overshoot temperature and settling time. This can be seen in Figure 47, where there is no increase in Transient Advantage after 5 milliseconds, while the Transient Penalty increases linearly with increasing pulse duration. As mentioned in the previous section, the Transient Penalty is approximately one order of magnitude larger than the Transient Advantage, resulting in an overall transient effect (ratio of Transient Advantage to Transient Penalty) of substantially less than unity.

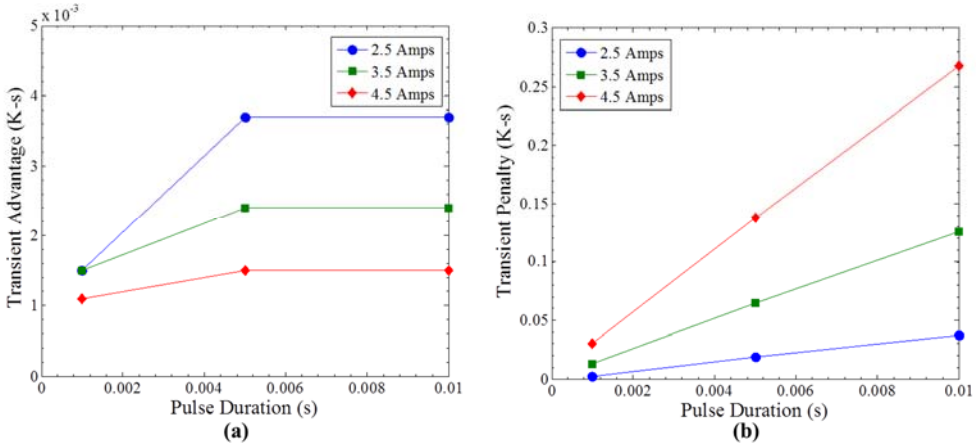


Figure 47. Transient (a) advantage and (b) penalty as a function of pulse duration.

As previously noted for the square pulse shape considered, thus far, the Transient Advantage is often substantially outweighed by the Transient Penalty resulting in a ratio of Transient Advantage to Transient Penalty of substantially less than unity. However, the time-temperature history described above implies that a square current pulse may, in fact, be the least efficient profile for transient thermoelectric remediation of on-chip hotspots. In addition to the step current profile previously discussed, a simple Ramp Up, Ramp Down, and Isosceles profile were explored, as shown in Figure 48. The Ramp Down current profile initially results in a hotspot temperature similar to that of the step profile. The current continuously decreases during the Ramp Down profile, reducing the Peltier cooling, thus the minimum hotspot temperature reached is slightly warmer than that of the step current. However, the continuous decrease in current produces less joule heating throughout the substrate, thus the Transient Penalty resulting from the Ramp Down profile is significantly lower than that of the step current. Similarly, the Isosceles profile also provides a comparable amount of Transient Advantage with less Transient Penalty, compared to the step current.

Figure 49 displays the Transient Advantage and Transient Penalty (left axis) and the overall transient effect, which is equal to the ratio of Transient Advantage to Transient Penalty (right axis). As previously discussed, the step current has the poorest overall transient effect, on the order of 0.2. However, the Ramp Down and Isosceles profiles have overall transient effects of 1.19 and 1.46, respectively, indicating that the Transient Advantage is larger than the Transient Penalty. The current profiles used were not meant to exhaust all the possible variations but rather to illustrate the ability

of pulsed thermoelectric operation to generate a net positive "super cooling" effect. It is to be expected that optimization of the pulse shape for a given hotspot dissipation profile or sensor driven-operation of the thermoelectric cooler to respond to a variable dissipation profile could result in further improvements in the net benefit of pulsed thermoelectric cooling.

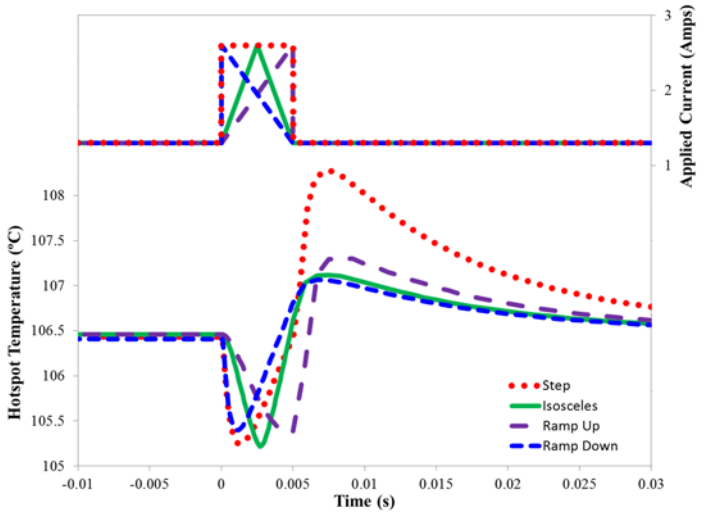


Figure 48. Alternative applied current profiles considered and the resulting hotspot temperature over time.

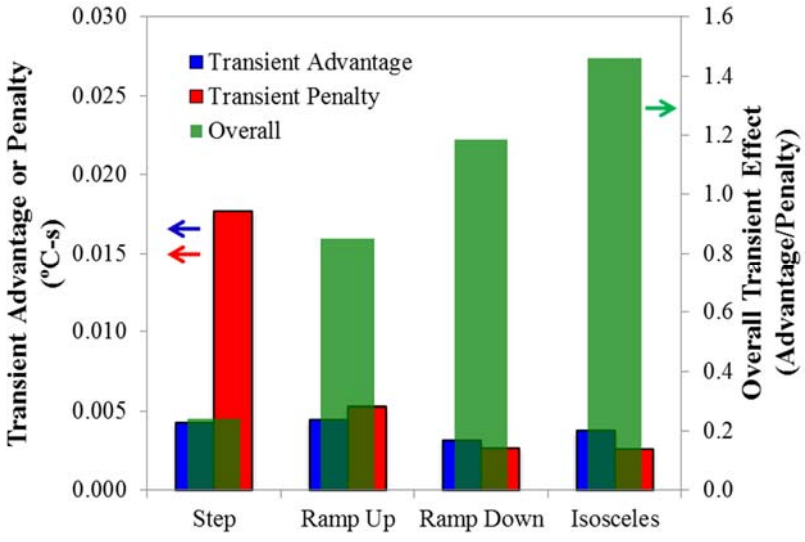


Figure 49. Transient Advantage, Transient Penalty, and overall transient effect for various current shapes.

The effect of die thickness on Transient Advantage and Transient Penalty was also investigated for a square current profile. Changing the geometry of the die alters the optimum steady state current and optimum steady state temperature reduction. It was therefore necessary to find the optimum steady state current, which minimizes the hotspot temperature for each die thickness, and the parameters associated with the optimum steady state cooling were then used as the initial condition for the transient analysis.

Figure 50 shows the steady state, transient "super cooling," and total transient temperature reduction at the hotspot and cooler as the die thickness varies from 25 to 200 microns, while the cooler size remains constant at 600µm by 600µm. At very small die thicknesses, the hotspot and cooler approach the same temperature and as the die thicknesses increases, the cooler and hotspot become physically further apart, resulting in their respective temperatures diverging from each other.

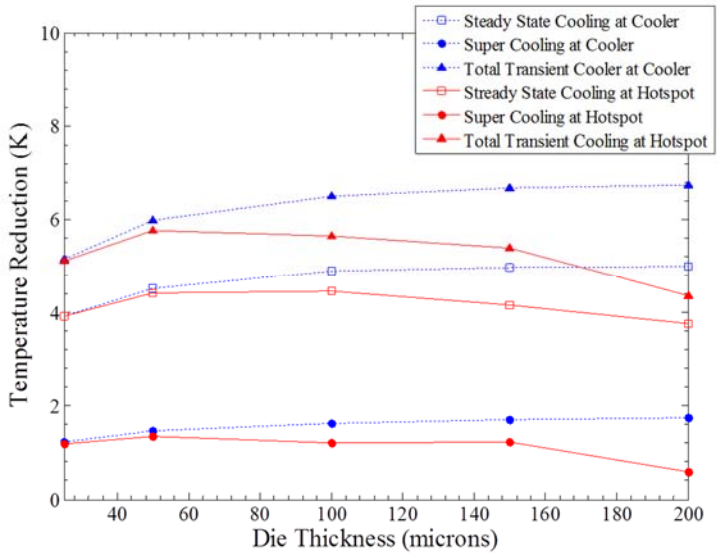


Figure 50. Optimal steady state cooling, "super cooling," and total transient temperature reduction (steady state cooling plus "super cooling") of the hotspot and microcooler as a function of die thickness.

Thicker dies result in a larger temperature reduction at the cooler because the thickness of the die insulates the cooler from the hotspot. However, the thicker die weakens the effectiveness of the cooler in reducing the hotspot temperature. Thus, as die thickness increases, both the steady state and transient temperature reduction at the hotspot decrease and for die thicknesses of 25 microns to 100 microns the pulsed cooling enhancement at the hotspot stays nearly constant, meaning that increasing the die thickness affects the steady state and transient cooling equally. However, at die thickness greater than 100 microns, the pulsed cooling enhancement begins to decrease, meaning that the increased die thickness is degrading the "super cooling" relatively more than the steady state temperature reduction.

As previously stated, "super cooling" occurs because the cooling from the cooler reaches the hotspot more quickly than the bulk joule heating. Consequently, moving the cooler further away from the hotspot, by increasing the die thickness, results in reduced "super cooling" and therefore reduced pulsed cooling enhancement. Figure 51 shows the Transient Advantage and Transient Penalty as a function of die thickness and it can be seen that he maximum Transient Advantage occurs at a die thickness of 100 microns. Unfortunately, the Transient Penalty also reaches a maximum at a die thickness close to this value.

Thus far, the effect of current magnitudes, current pulse durations, current profiles, and die thicknesses on monolithic thermoelectric "super cooling" was explored. A previously optimized germanium cooler served as the steady-state baseline design and it was determined that pulsed monolithic "super cooling" could provide a maximum of 7.5ºC in temperature reduction at the cooler and a 6.5ºC in temperature

reduction at the 70μm×70μm, 700W/cm^2 hotspot**.** The transient "super cooling" increased the cooling at the cooler and the hotspot by 50% and 30%, respectively, relative to what was achievable in steady state operation.

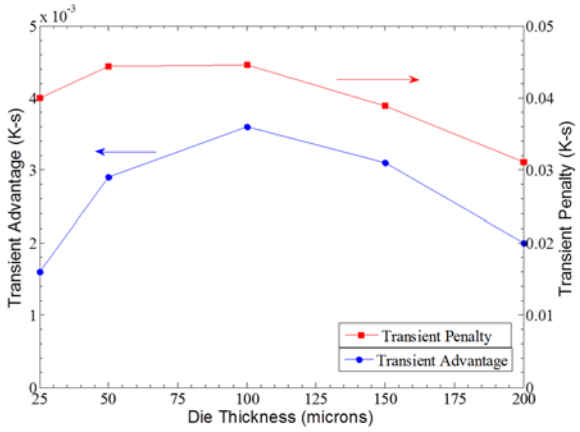


Figure 51. **Dependence of Transient Advantage and Penalty on die thickness.**

A new Transient Advantage metric was introduced in order to more clearly illustrate the transient behavior of germanium monolithic coolers and it was shown that the applied current profile is a critical factor in maximizing the overall transient benefit, where certain current profiles produced more Transient Advantage than Transient Penalty, resulting in a net positive transient effect. From all of the results presented it is clear that transient "super cooling" can be used advantageously to provide bursts of additional Peltier cooling in order to augment a monolithic cooler already operating at steady state cooling conditions.

3.2.2 Anticipatory Thermoelectric Cooling of a Dynamic Hotspot

The previous study explored transient "super cooling" using the monolithic configuration for cooling of hotspots with a constant heat flux. However, it is well established that modern electronics experience thermal transients and power

dissipation that are not constant over time [55], [68], [69]. Therefore, the ability of a germanium based monolithic thermoelectric cooler to remove a dynamic hotspot, with a heat flux that varies over time, was also studied.

A comparable geometry to that used in the "super cooling" study and shown in Figure 31, consisting of a 12x12mm germanium die with a thickness of 100μm and a 600μm x 600μm microcooler, was utilized as the starting point for the dynamic model. Similarly, a background heat flux of 100W/cm^2 was applied to the back of the die, a heat transfer coefficient representative of a finned heat sink was applied to the top, and a hotspot was created at the center of the die by applying an elevated heat flux.

In the dynamic hotspot model, two different hotspots were studied, one 70x70μm in size, with a heat flux of 700W/cm^2, and the second 100μm x100μm in size, with a heat flux of 1000W/cm^2. An initial condition of no hotspot and no thermoelectric cooling was used and a density of 5323kg/m^3 and specific heat of 320J/(kg-K) was assumed for the germanium. Additionally, the germanium was assumed to be doped with arsenic to a concentration of 2.5x10^{18}cm^{-3}, resulting in a Seebeck coefficient of 467x10^{-6}W/K, an electrical resistivity of 5x10^{-5}Ω-m, and a thermal conductivity of 60W/(m-K).

Successful thermoelectric cooling requires a favorable balance between Peltier cooling and the two parasitic effects, joule heating and thermal diffusion. It is well established that there is a steady-state optimum current which produces the most effective thermoelectric cooling and that operating at currents above or below this optimum, will not reduce hotspot temperatures as effectively. This behavior is important to recall, as it was shown that it is possible to achieve a rapid temperature

reduction by using larger currents. However, the penalty for utilizing these larger currents is extra joule heating and, eventually, increased hotspot temperature.

Due to the physical separation between the microcooler and the hotspot, activating the cooler slightly before the hotspot begins to develop and, thus, allowing the cooling to reach the hotspot before the hotspot heat flux increases, can more effectively suppress the hotspot temperature rise. The benefit of such anticipatory- or pre-cooling was studied for both the 70μm x 70μm, 700W/cm^2 hotspot and the 100μm x 100μm, 1000W/cm^2 hotspot. The optimum steady state currents for the 70μm x 70μm and 100μm x 100μm hotspots are 1.25 and 1.31 amps, respectively. Thus for simplicity, a current of 1.3 amps is used as the 'optimum' steady state current for both hotspot in the transient model.

Initially a single hotspot pulse was cooled, with the intention of then cooling multiple hotspot heat flux pulses, comparable to an electronic device operating on a duty cycle. Figure 52(a) shows the cooler current and hotspot heat flux profiles over time for the lower heat flux hotspot and, as can be seen, the hotspot heat flux starts at the background heat flux of 100W/cm^2, steps up to 700W/cm^2 for 0.01 seconds before stepping back down to 100W/cm^2. The cooler is turned on 0.0001, 0.001, 0.002, or 0.0025 seconds before the hotspot. Here, the steady state optimum current of 1.3 amps is used, so temperature overshoot due to excess joule heating is not a concern and the resulting hotspot temperatures over time are shown in Figure 52(b).

If no thermoelectric cooling is utilized, the hotspot temperature increases by 4.4K, reaching a peak temperature of 110.7°C and when the cooling pulse is initiated 0.0001 seconds before the hotspot is activated, the peak hotspot temperature is reduced

to 108.4°C. However it is clear that additional pre cooling will further reduce the peak hotspot temperature and it can be seen that using a 0.0025 second offset between cooler and hotspot activation reduces the peak hotspot temperature by 4.4K, completely suppressing the dynamic hotspot.

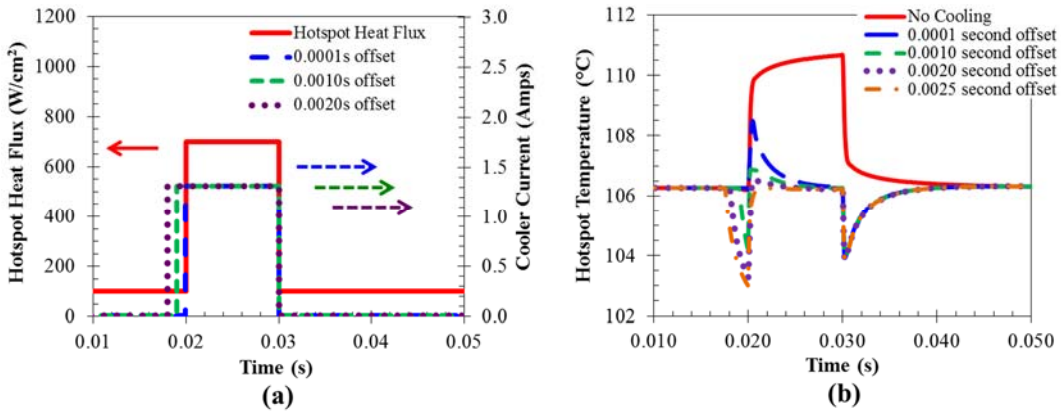


Figure 52. (a) The hotspot heat flux (left) and cooler current (right) over time for anticipatory cooling of 0.0001, 0.001, and 0.002 seconds and (b) the resulting hotspot center temperature over time with no cooling, and with cooling produced by a current magnitude of 1.3 amps and an offset of 0.0001, 0.001, 0.002, and 0.0025 seconds.

Three different current pulse magnitudes, all with 0.001 seconds of anticipatory cooling, were used to surpress the larger 1kW/cm^2 hotspot, as shown in Figure 53(a). Additionally the hotspot temperatures over time resulting from the various level of applied thermoelectric currents are shown in Figure 53(b). As can be seen, when no thermoelectric cooling is utilized, the larger and higher heat flux hotspot causes the temperature to increase by 10.6K, reaching a peak temperature of 116.9°C.

Applying the steady state optimum current of 1.3 amps reduces the peak hotspot temperature to 112.5°C, a reduction of 4.4K, and when a 2.6 amp current is used, the hotspot temperature is initially reduced to 110.0°C at 0.02 seconds, an additional cooling of 2.5K. However, due to the excess joule heating created by the larger current,

the hotspot temperature rises over time, reaching a peak temperature of 114.2°C, 1.7K above the peak hotspot temperature when the optimum steady state current was used. Additionally, the joule heating created by the 2.6 amp current causes the hotspot temperature to be elevated even after the hotspot and cooler have switched off.

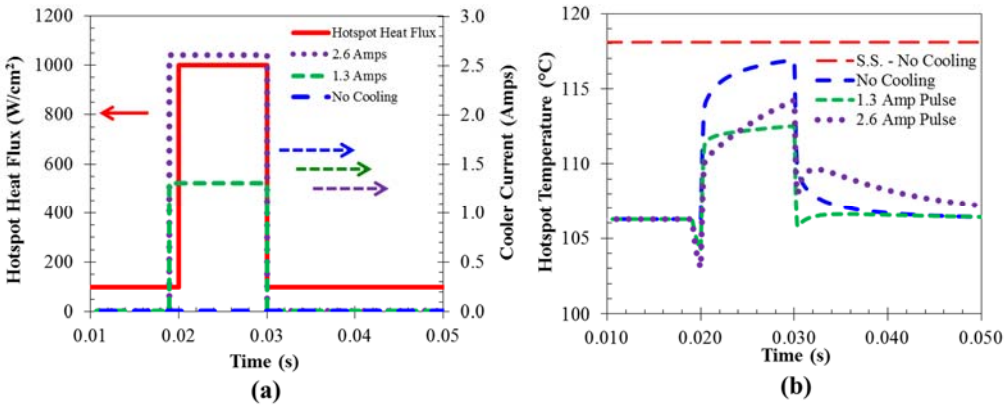


Figure 53. (a) The hotspot heat flux (left) and cooler current (right) over time when 0, 1.3, and 2.6 amps of cooler current are utilized with an offset of 0.001 seconds, and (b) the resulting hotspot temperature over time when 0, 1.3, and 2.6 amps are applied to the cooler.

The fact that the larger current provided additional hotspot temperature reduction for a short period of time suggests that using currents greater than the steady state optimum would be more effective for hotspots with a shorter duration. Therefore, a trial was performed in which the hotspot duration was reduced from 10 milliseconds to 1 millisecond. Similar to the profiles shown in Figure 52(a), an anticipatory cooling of 0.001 seconds was used; however in this case the hotspot heat flux and cooler current were stepped back down at 0.021 seconds rather than at 0.03 seconds.

The resulting hotspot temperatures from the shorter duration hotspot are shown in Figure 54, and it can be seen that if no cooling is applied the hotspot temperature increases by 8.4K, reaching a peak temperature of 114.7°C. Applying the optimum steady state current of 1.3 amps reduces the peak hotspot temperature to 111.6°C, a

cooling of 3.1K, and increasing the current to 2.6 amps further reduces the peak hotspot temperature to 110.4°C, a reduction of 4.3K. The additional joule heating from the larger current eventually diffuses to the hotspot, resulting in a slightly elevated hotspot temperature, even after the hotspot and cooler have been switched off.

The temperature distribution along the bottom of the germanium chip was recorded for the 100x100µm, 1000W/cm^2, and is presented in Figure 54(b). It can be seen that the bottom of the chip is initially isothermal at a temperature of 106.3°C. When the hotspot is activated at 0.02 seconds for 0.001 seconds and no cooling is used, it reaches a peak temperature of 114.7°C at 0.021 seconds. If a current of 1.3 amps is used, the peak hotspot temperature still occurs at 0.021 seconds, but is reduced by 3.1K to 111.6°C. Finally, if a current of 2.6 amps is used, the peak hotspot temperature can be reduced by an additional 1.2K to 110.4°C, at the expense of a slightly elevated temperature in the area surrounding the hotspot.

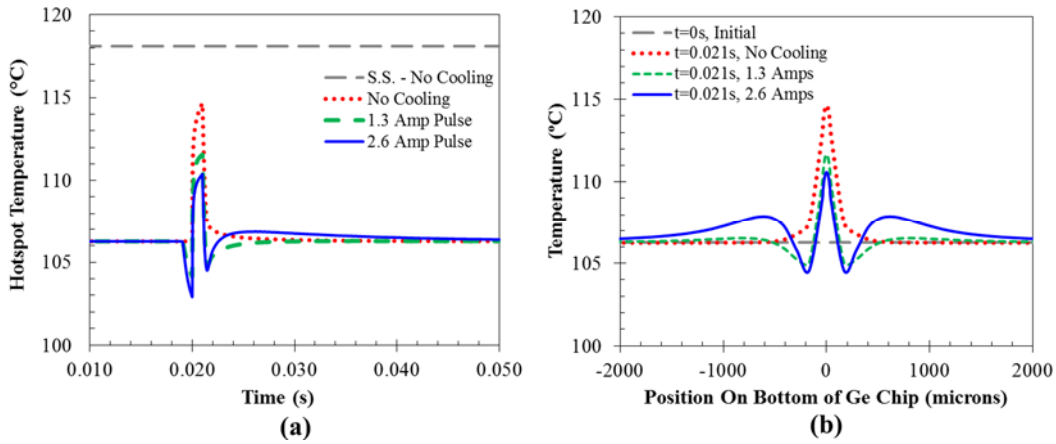


Figure 54. (a) Hotspot temperature over time when 0, 1.3, and 2.6 amps are applied to the cooler and the hotspot heat flux is 1000W/cm^2 and the hotspot duration has been reduced to 0.001 seconds, and (b) the temperature distribution along the bottom of the 12x12mm germanium chip at t = 0.021 seconds, for various applied currents.

The ability of a germanium based monolithic cooler to cool a reoccurring dynamic hotspot, which repeats over time, was also explored. Similar to the previous study, two different hotspots, a 70μm x 70μm, 700W/cm^2 and a 100μm x 100μm, 1000W/cm^2 were tested. For the sake of brevity, only the results of the 100μm x 100μm, 1000W/cm^2 paper will be presented in detail. As was previously discussed, the 70μm x 70μm, 700W/ cm^2 could be completely removed with the thermoelectric cooler using the steady state optimum current and utilizing the steady optimum current does not produce a temperature overshoot. Thus a repeating hotspot can be dealt with in a straightforward manner. As will be discussed, the more challenging situation arises when cooling the 100μm x 100μm, 1000W/cm^2 hotspot, which requires using current magnitudes greater than the optimum steady state.

The 100μm x 100μm, 1000W/cm^2 hotspot cannot be completely removed using the optimum steady state current of 1.3 amps, thus larger cooling currents were explored. In this portion of study, the hotspot has a period of 0.02 seconds and two different scenarios were examined: In the first, the hotspot was active for 0.01 seconds or a duty cycle of 50%, and in the other, the hotspot was active for 0.001 seconds or a duty cycle of 5%. Figure 55 illustrates the hotspot heat flux and cooler current over time for the case of 50% duty cycle, and as was the case previously, an offset of 0.001 seconds between cooler and hotspot activation was used. The second scenario of a 5% hotspot duty cycle utilized a similar hotspot heat flux profile, except that the heat flux was reduced after being active for 0.001 seconds rather than 0.01 seconds.

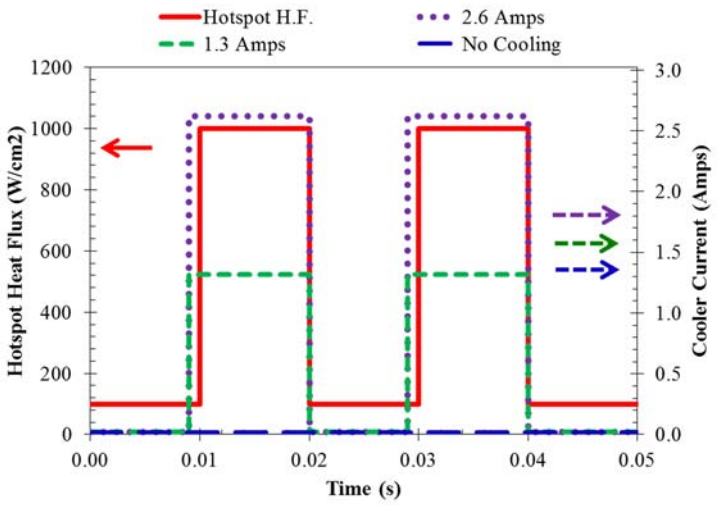


Figure 55. Hotspot heat flux (left) and cooler current (right) over time for cooling of a hotspot with a duty cycle of 50%. The hotspot is 100x100µm with a heat flux of 1000W/cm^2.

Figure 56(a) and (b) show the resulting hotspot temperatures over time for the 50% and 5% duty cycle cases, respectively. In the case of 50% duty cycle, if no thermoelectric cooling is utilized the hotspot temperature increases by 10.6K each time the hotspot is activated, reaching a peak temperature of 116.9°C. If a 1.3 amp cooler current is used, the hotspot peak temperature is reduced to 112.5°C, a cooling of 4.4K. After the hotspot heat flux and 1.3 amp current are reduced, the hotspot quickly returns to its original temperature of 106.3°C. If a 2.6 amp current is applied, the hotspot is initially cooled by an additional 2.5K at 0.01 seconds, however the excess joule heating created by the higher current causes the hotspot temperature to rise to a temperature greater than when cooled by a 1.3 amp current. Additionally, the 2.6 amp current causes an overshoot temperature after the hotspot and cooler have been switched off.

When operating at a 50% duty cycle, the hotspot does not have time to cool sufficiently after the 2.6 amp current is applied and the hotspot temperature is still elevated above the original 106.3°C when the hotspot is activated in the second cycle,

as shown at 0.03 seconds in Figure 56(a). The prolonged elevation in temperature suggests that using a current of 2.6 amps would not be sustainable for a hotspot with a period of 0.02 seconds and duty cycle of 50%, as there would not be sufficient time for cooling between hotspot heat flux pulses. As previously discussed, these results indicate that a current of 2.6 amps may be more beneficial for cooling a shorter duration hotspot, which would require the cooler to be active for a shorter amount of time resulting in less joule heating and, therefore, less temperature overshoot after the hotspot is switched off.

In the case of 5% duty cycle, it can be seen that the 0.001 second duration hotspot causes an increase in temperature of 8.4K, resulting in a peak hotspot temperature of 114.7°C, if uncooled. Applying a 1.3 amp cooler current reduced the peak hotspot temperature by 3.1K to 111.6°C. As was the case previously, the hotspot temperature quickly returns to its initial value of 106.3°C after the hotspot and current of 1.3 amps are switched off. Applying a cooler current of 2.6 amps provides an additional 1.2K of hotspot cooling, further reducing the peak hotspot temperature to 110.4°C. When the 2.6 amp current is switched off there is less temperature overshoot than in the case of the 0.01 second duration hotspot, and the hotspot temperature approaches its initial value of 106.3°C.

All of the results discussed thus far involved a hotspot heat flux and cooler current that were stepped up and down. However, many different hotspot heat flux profiles are possible. Thus, Figure 57(a) shows some alternate hotspot heat flux profiles, while Figure 57(b) shows corresponding thermoelectric current profiles. The alternate profiles consist of a ramp down profile, where the hotspot is initially stepped

up to 700W/cm^2 then ramps down to its initial value 100W/cm^2. The isosceles profile consists of the hotspot heat flux starting at 100W/cm^2 ramping up to 700W/cm^2, then immediately ramping back down to 100W/cm^2.

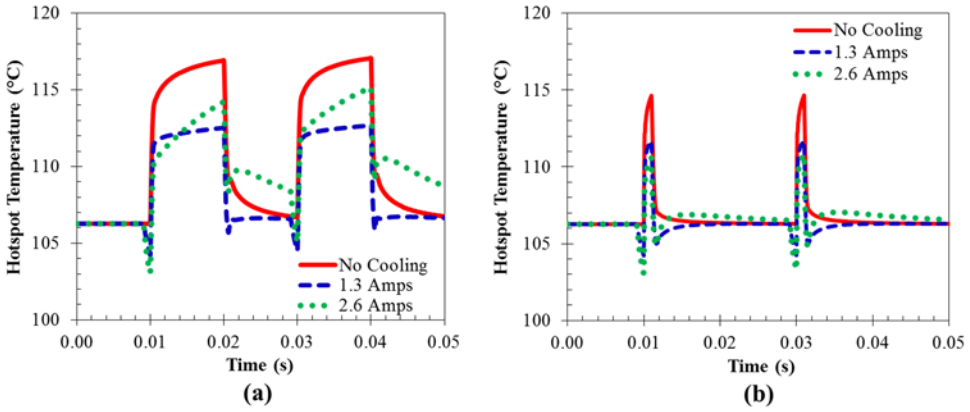


Figure 56. Hotspot temperature over time for (a) 50% duty cycle and (b) 5% duty cycle, when no thermoelectric cooling is applied and when a currents of 1.3 and 2.6 amps are used to cool the 100x100µm, 1000W/cm^2 hotspot.

Figure 58 shows the hotspot temperature over time resulting from the profiles described in Figure 57(a) and (b). Here, the effect of the hotspot with no cooling and cooling with no hotspot are shown separately for clarity. The step, ramp down, and isosceles heat flux profiles are each applied with no cooling, resulting in the upper set of curves of elevated hotspot temperatures. Conversely, the step, ramp down, and isosceles thermoelectric current profiles are applied with no hotspot, resulting in the lower set of curves showing decreased temperatures.

The step profile results in a rapid increase or decreases in hotspot temperature when the hotspot or cooler is stepped on, followed by a period of asymptotic behavior, and finally a rapid decrease or increase when the hotspot or cooler is stepped back down. The ramp down profile also has a rapid increase or decrease in temperature as the hotspot or cooler is initially stepped up, however the temperature then follows a

more gradual decrease or increase as the heat flux or current is ramped down. The results suggest that the most efficient hotspot cooling would occur when the appropriate cooler current is matched to a specific hotspot heat flux profile match.

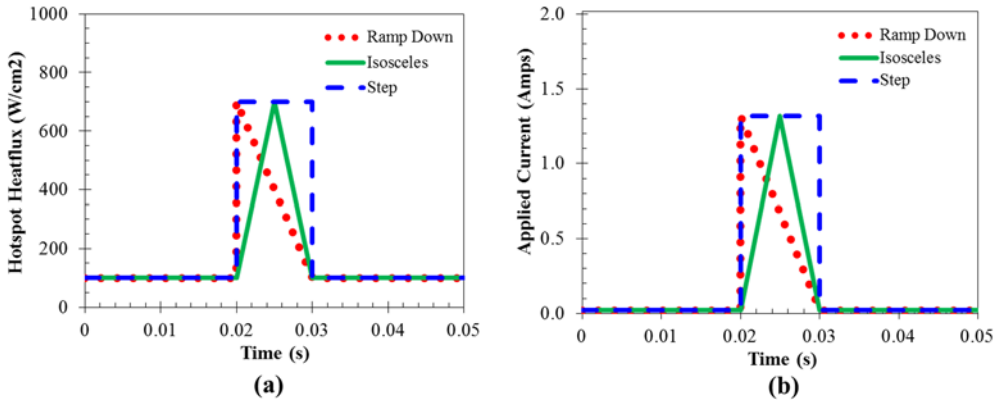


Figure 57. (a) Hotspot heat flux and (b) cooler current over time for step, ramp down, and isosceles current profiles.

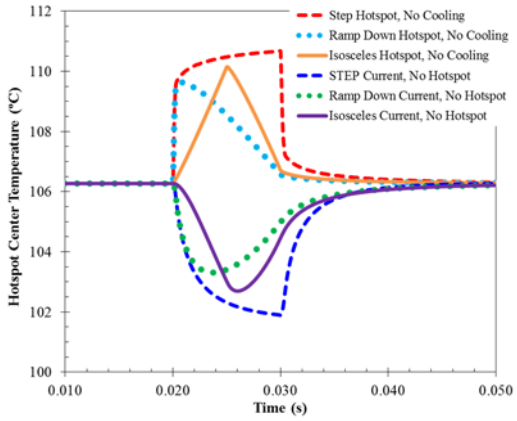


Figure 58. Hotspot temperatures resulting from step, ramp down and isosceles hotspot heat flux profiles with no thermoelectric cooling and from step, ramp down, and isosceles cooler current profiles with no hotspot heat flux.

Therefore, Figure 59 shows four different combinations of hotspot heat flux and applied current profiles. The profiles are mostly identical to those previously discussed, except that anticipatory cooling of 0.0025 seconds has been added to the cooler current in order to compensate for the spatial separation between the hotspot and the cooler. Figure 59(a) (b) consist of a step and ramp down cooler current, respectively, being

used to cool a step hotspot heat flux. Figure 59(c) and (d) consist of a step and ramp down cooler current, respectively, being used to cool a ramp down current.

The resulting hotspot temperature over time is shown in Figure 60 and as has been previously shown, a step current of 1.3 amps can completely remove the step hotspot of 700W/cm^2. If a ramp down current is used to cool the step hotspot, the Peltier cooling ramps down while the hotspot heat flux remains elevated, resulting in a rise in hotspot temperature over time. Both the ramp down and step current completely eliminated the ramp down hotspot, however, the step current significantly over cooled the ramp down hotspot, implying that matching a ramp down cooler current with the ramp down hotspot heat flux would be more energy efficient.

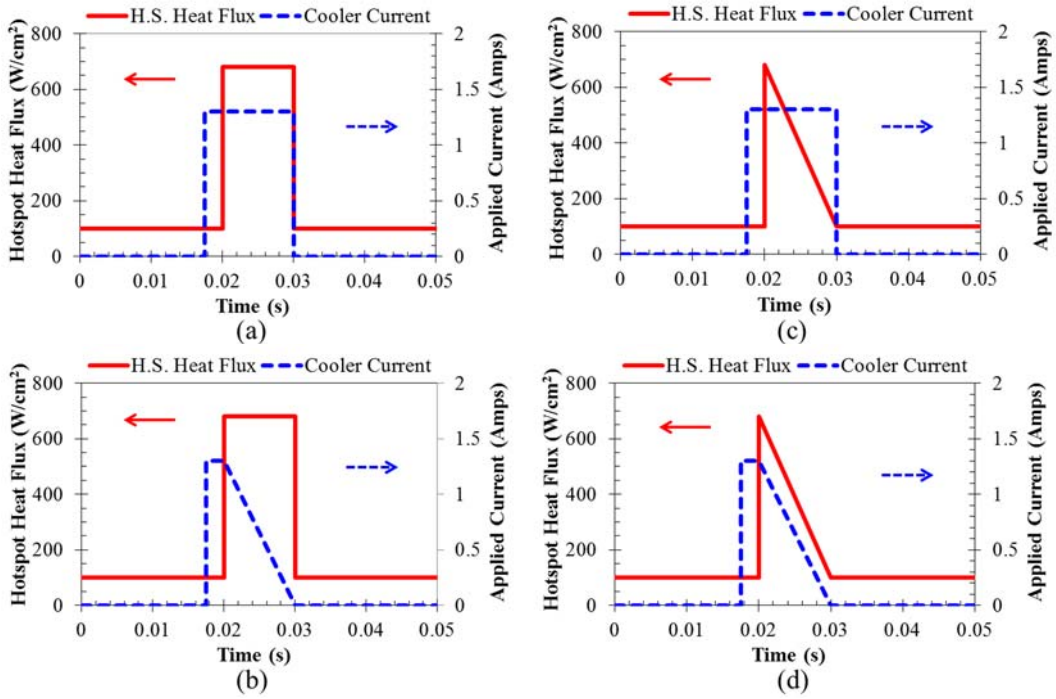


Figure 59. Four different hotspot heat flux and cooler current combinations. (a) Step hotspot, step current; (b) step hotspot, ramp down current. (c) ramp down hotspot, step current; and (d) ramp down hotspot, ramp down current.

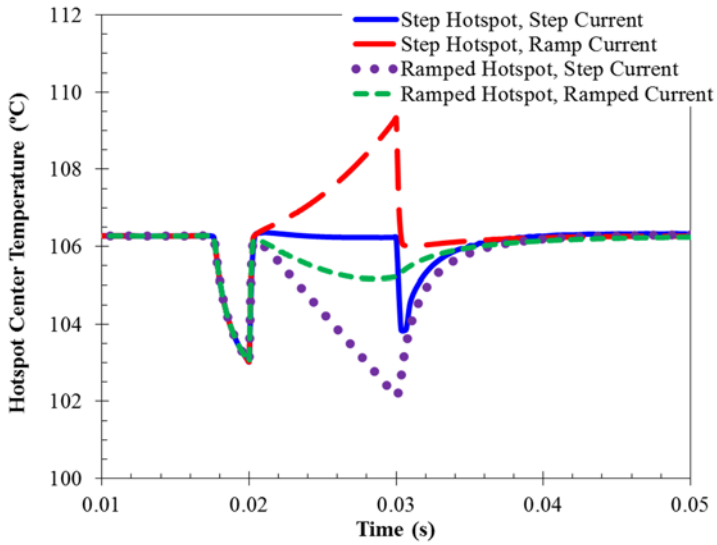


Figure 60. Hotspot temperature over time resulting from different hotspot heat flux and cooler current profiles, showing that matching cooler current to hotspot heat flux profile results in the most efficient hotspot cooling.

This study presented the results of a numerical study of on-chip monolithic thermoelectric cooling of a dynamic hotspot, with a heat flux that varies over time. The effects of anticipatory cooling, cooler current magnitude, hotspot duty cycle, hotspot heat flux profile, and cooler current profile were explored and the importance of the steady state optimum current and the dynamic hotspot duration was discussed. It was found that transient thermoelectric cooling could provide up to 4.4K reductions in the transient hotspot's peak temperature and a 700W/cm^2 hotspot could be completely removed even when continuously active or operating at a high duty cycle. Additionally, a 1000W/cm^2 hotspot could be suppressed, resulting in a greater than 50% reduction in hotspot temperature rise. Finally, it was shown that the profile over time of the current applied to the thermoelectric cooler could be engineered to match the hotspot heat flux profile in order to provide the most efficient hotspot cooling.

3.2.3 Monolithic Thermoelectric Cooling on Advanced Substrates

The previous monolithic studies focused on germanium, which is often overlooked as a thermoelectric material due to its relatively low figure of merit. However, germanium possesses a large power factor because of its high Seebeck coefficient and low electrical resistivity, making it superior to silicon in the monolithic cooling configuration [65], [66], [70], [71]. However, even germanium based monolithic coolers are unable to completely remove kW/cm^2 level hotspots. Therefore, additional work was performed to determine how far monolithic thermoelectric hotspot cooling could be advanced, if certain material property metrics could be reached.

For example, it has been reported that Seebeck coefficients of up to 1000μV/K are possible in Si/SiC superlattices and, as discussed in Section 2.3, the thermal conductivity of these materials is likely much lower than the bulk properties due to the superlattice structure [72], [73]. The large Seebeck coefficient of these materials produces intense Peltier cooling, while the low thermal conductivity has a concentrating effect, which keeps the Peltier cooling focused on the hotspot, allowing for the cooling of hotspots with heat fluxes on the order of $5kW/cm^2$.

Therefore, a parametric study of Seebeck coefficient, thermal conductivity, and electrical conductivity was performed to determine the effect of each material property on hotspot cooling performance. In addition, the effect of electrical contact resistance and the geometry of the monolithic cooling structure were also studied. The results produced by the modeling provide a roadmap of the potential ultra-high heat flux hotspots that can be cooled in the future, if specific material property targets can be reached.

In an initial study performed in collaboration with Dr. Peng Wang, the monolithic cooling configuration was applied to theoretical quantum-well Si/SiC superlattice films [73]. As discussed, superlattice materials commonly have increased Seebeck coefficient and reduced thermal conductivity resulting in larger Z and ZT values. Additionally, SiC has gained great popularity in power electronic devices due to its superior performance at high powers and high temperatures compared to silicon. The numerical model utilized a similar geometry to that used in the previous transient studies and shown in Figure 31. The substrate was assumed to include a quantum well Si/SiC superlattice and experience a uniform background heat flux of 100W/cm^2, along with a hotspot heat flux of 1500W/cm^2 at the center of the chip, intended to represent a gallium nitride (GaN) based power amplifier.

Seebeck coefficient and electrical resistivity values of -750μV/K and 22μΩ-m, respectively, were taken from published literature and applied to Si/SiC superlattice [72]. Limited data was available for the thermal conductivity of Si/SiC superlattices, thus as a conservative estimate, a thermal conductivity close to that of bulk SiC was used and a broad parametric study on the effect of thermal conductivity was performed. Figure 61 shows the temperature rise along the bottom of the SiC substrate close to the hotspot for a germanium substrate with a 700W/cm^2 hotspot and a Si/SiC substrate with a 1500W/cm^2 hotspot and it can be seen that despite the larger hotspot heat flux, the Si/SiC superlattice based monolithic cooler provides more hotspot cooling than the germanium based cooler.

It can be seen that with no thermoelectric cooling, the hotspot causes a temperature rise at the center of the Si/SiC substrate and when the optimum

thermoelectric current of 3 amps is applied, the hotspot temperature rise is reduced by 6.4K. In fact, the SiC based monolithic cooler actually reduces the hotspot below the no hotspot temperature, indicating that the device has the potential to cool a hotspot with an even larger heat flux. Additionally, due to the limited data available for Si/SiC superlattice thermal conductivity, the study assumed a conservative value near the bulk value for SiC, which reduced the amount of hotspot cooling due to thermal spreading.

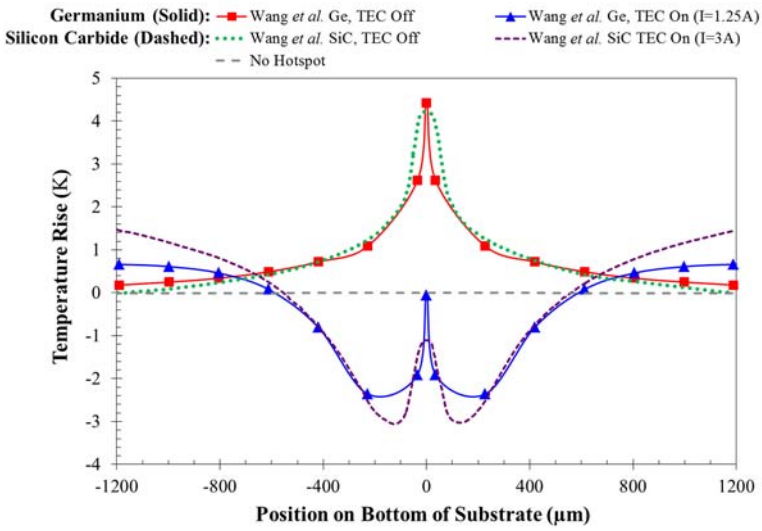


Figure 61. Temperature distribution along the bottom of the substrate for a monolithically cooled hotspot on a germanium (solid lines with markers) and a Si/SiC (dashed lines) substrate [65], [73].

The effect of thermal conductivity of the substrate on hotspot cooling was parametrically explored and it was found that although the FOM for traditional thermoelectric modules suggest that lower thermal conductivity is always better, this is not the case for monolithic hotspot cooling. In fact, there exists an optimum substrate thermal conductivity value, which maximizes the thermoelectric hotspot cooling.

In the monolithic hotspot cooling configuration, the micro cooler and hotspot are on opposite sides of the substrate. Thus, a high thermal conductivity substrate

minimizes the conduction resistance through the substrate, but also causes the thermoelectric cooling to spread and become diffuse by the time it reaches the hotspot, resulting in diminished hotspot cooling. Conversely, a lower conductivity substrate keeps the thermoelectric cooling concentrated and focuses it onto the hotspot, but also results in a large thermal resistance through the substrate, between the cooler and the hotspot. Therefore, the optimum substrate thermal conductivity occurs due to the competition between thermal spreading in the substrate and the cooler-to-hotspot conductive thermal resistance.

As shown in Figure 62, a simplified numerical model was created to explore the relationship between hotspot cooling and thermal conductivity. In a manner comparable to the transient studies, a 10mm x 10mm die, with a thickness of 100μm was used and a hotspot heat flux was applied at the center of the bottom of the chip. Unlike the previous model, it was assumed that the top of the device was attached to a heat sink fixed at 100ºC. The metal lead, which is electrically isolated from the SiC/Si substrate by a thin SiO_2 layer, delivers electrical current, which produces localized Peltier cooling at the metal to SiC/Si interface. The electrical current then flows through the substrate and continues out through the ground electrode located at the edge. Electrical current was applied in the model and ANSYS was used to calculate the non-uniform joule heating in the metallization and substrate. For simplicity, the Peltier heating and cooling was calculated based on the Seebeck coefficient of the substrate, the operating temperature, and the applied current, and applied to the model as a heat flux.

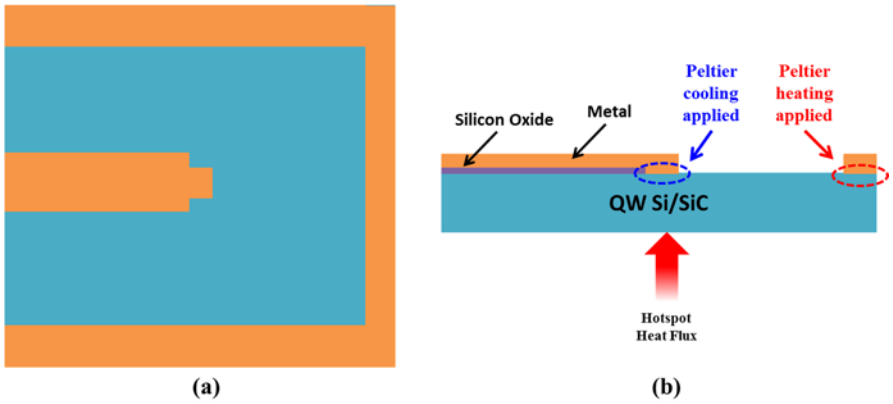


Figure 62. (a) Top view and (b) cross section of the simplified numerical model used to parametrically study the effect of substrate thermal conductivity.

Figure 63(a) and (b) show the hotspot temperature as a function of applied current for a 2kW/cm^2 and 4kW/cm^2, respectively. It can be seen that some of the low conductivity substrates produced extremely large amounts of hotspot cooling and in fact, temperatures below absolute zero could be calculated due to a simplification in the calculation of Peltier cooling**.** As previously discussed, Peltier cooling or heating at an interface is equal to the product of the difference in Seebeck coefficient, the current flow, and the absolute temperature of the interface (and therefore should go to zero at absolute zero).

In previous modeling, the monolithic configuration only produced modest temperature reductions, on the order of 10 or 20K, so an assumed operating temperature based on the boundary conditions was used when calculating the Peltier cooling. For example, if an operating temperature of 373K is assumed and the thermoelectric cooler is at a temperature of 363K, the difference in the magnitude of the Peltier cooling is less than 1.5%. However, due to the high Seebeck coefficient and low thermal conductivity of superlattice substrates, much large temperature gradients, on the order

of 100K are possible, making the previous method of calculating Peltier cooling less accurate.

Despite the simplification, it can be seen that there is an optimum substrate thermal conductivity, which maximizes hotspot cooling, and the optimum conductivity value is dependent on the hotspot heat flux. As previously discussed, the optimum substrate thermal conductivity results from the balance of the two effects; spreading of the Peltier cooling in the substrate and the thermal resistance between the hotspot and cooler. As can be seen in Figure 63(b), the thermoelectric cooling spreads laterally in the high conductivity substrates, resulting in high temperature for the 4kW/cm^2 hotspot. As thermal conductivity decreases, the thermoelectric cooling stays concentrated and the hotspot temperature can be reduced. However, continuing to lower the thermal conductivity below a value of 5W/m-K results in a high thermal resistance through the substrate, which overpowers the cooling concentration effect and causes the hotspot temperature to rise.

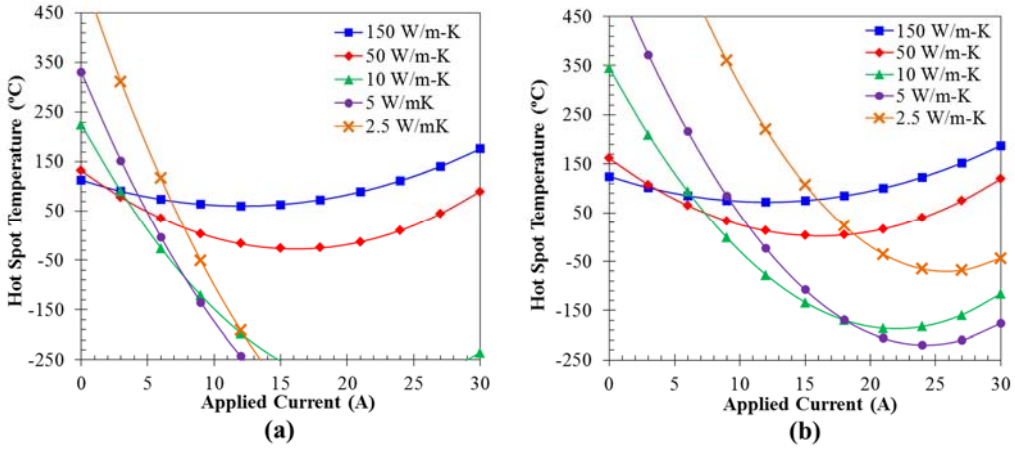


Figure 63. Hotspot temperature as a function of applied current for a variety of different substrate thicknesses and hotspot heat flux of (a) 2kW/cm^2 and (b) 4kW/cm^2.

The dashed blue line Figure 64(a) shows the active cooling, which is the change in hotspot temperature when microcooler is switched on and it can be seen that at low thermal conductivities, the Peliter cooling remains very concentrated, resulting in large values of active cooling. Figure 64(a) also shows the insulating effect, which is the hotspot temperature rise with no thermoelectric cooling, relative to a baseline case, and it can be seen that the insulating effect also increases with lower values of substrate thermal conductivity. Therefore, the optimum hotspot temperature is a balance of the active cooling and hotspot rise due to the insulating effect. Additionally, it can be seen that higher heat fluxes result in larger temperature rises. Finally, Figure 64(b) shows the hotspot temperature when the optimum thermoelectric current is applied as a function of substrate thermal conductivity for a variety of hotspot heat fluxes, and it can be seen that for each heat flux, there is an optimum thermal conductivity that minimizes the hotspot temperature and that the optimum conductivity increases with increasing hotspot heat flux.

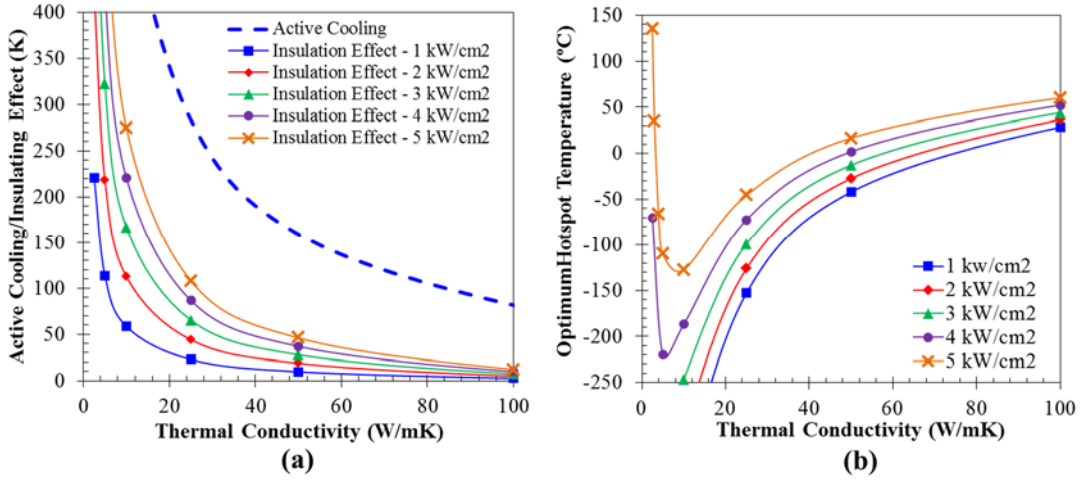


Figure 64. (a) Active thermoelectric cooling and hotspot insulation effect and (b) optimum hotspot temperature as a function of thermal conductivity for five hotspot heat fluxes.

As previously discussed, the large Seebeck coefficient and low thermal conductivity of the superlattice substrate produced large thermal gradients, making it necessary to improve the method for calculating the Peltier cooling. Therefore, a new 3D model was created in ANSYS using Solid226 thermal-electric elements, which are capable of calculating Joule heating and Peltier heating/cooling at the element level. As the Peltier heating/cooling is temperature dependent, calculating it makes the model non-linear and increases the required computational power and required solve time. However, the more advanced elements are required in order to achieve accurate predictions of hotspot cooling on advanced thermoelectric substrates. The accuracy of using ANSYS and the Solid226 element to solve thermoelectric analyses has been documented in the literature [67].

The geometry of the Solid226 model was the same as that shown in Figure 62 and Figure 65(a) shows the boundary conditions that were applied, consisting of a fixed temperature at the bottom of the substrate and electrical current supplied to the end of the metal lead. For computational efficiency, a half symmetry model was used, and Figure 65(b) shows the temperature distribution when a 300µm x 300µm monolithic cooler is supplied with 6.8 amps of electrical current. It can be seen that due to the large Seebeck coefficient and low thermal conductivity, large temperature reductions, up to 160K are possible at the surface of the cooler. Additionally, it can be seen that significant temperature rise can occur in the metal lead, due to the low thermal conductivity of the Si/SiC superlattice substrate. Finally, Figure 65(c) shows the surface temperature of the microcooler as a function of applied current.

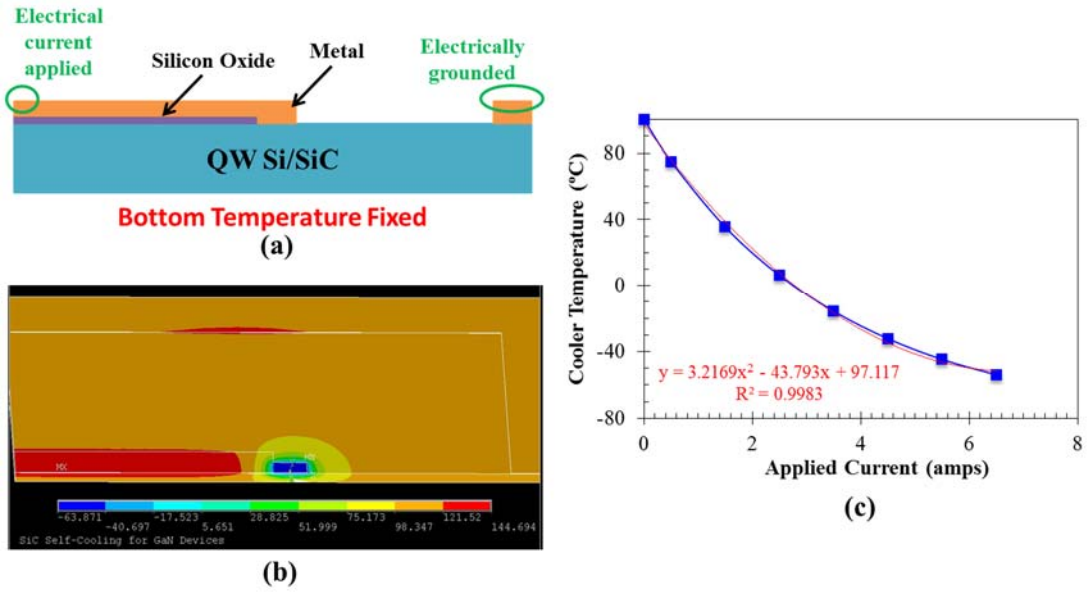


Figure 65. (a) Structure of SiC/Si thermoelectric cooler, (b) temperature distribution resulting from an applied current of 6.8 amps, and (c) change in cooler surface temperature with applied current.

In practice it is very difficult to make freestanding superlattices, and superlattice structures are typically grown on a supporting bulk substrate. Therefore, as shown in Figure 66(a), a bulk silicon substrate was incorporated into the model under the Si/SiC superlattice and unless otherwise specified, the values shown in Table IV were used in the numerical modeling of the monolithic thermoelectric cooler.

As an initial trial, Figure 66(b) shows the temperature distribution in Si/SiC based monolithic cooler when 6.5 amps of current was supplied and the microcooler size was 300μm × 300μm. It can be seen that the surface of the cooler was reduced from 100ºC to approximately 40ºC, which is equivalent to 60K of cooling. Additionally, in this case, the Si/SiC superlattice film is 10μm thick and a ring of elevated temperature can be seen immediately surrounding the cooler, resulting from the Joule heating produced as the current spreads into the Si/SiC film. While 60K of

cooling is substantial, it is significantly less than the 160K seen in the freestanding superlattice film. The reduction in cooling is due to spreading in the underlying silicon substrate and to the fact that the Si/SiC superlattice is only 10μm thick, rather than 100μm in the freestanding case. Finally, Figure 66(c) shows the cooler surface temperature as a function of applied current.

Table IV. Values used in the numerical modeling of Si/SiC monolithic cooler.

SiC/Si Electrical Resistivity (μΩ-m)	8.0
SiC/Si In-Plane Thermal Conductivity (W/m-K)	25.0
SiC/Si Cross-Plane Thermal Conductivity (W/m-K)	2.5
SiC/Si Seebeck Coefficient (μV/K)	1250
Metal Lead Electrical Resistivity (μΩ-m)	2.2
Metal Lead Thermal Conductivity (W/m-K)	250.0
Metal Lead Seebeck Coefficient (μV/K)	2.9
Contact Resistance (Ω-cm^2)	1.0×10^{-6}
Si/SiC Superlattic Film Thickness (μm)	10
Si Substrate Thickness (μm)	100
SiC/Si Cooler Size (μm^2)	300×300
Die Size (mm^2)	5.0×5.0
Oxide Thickness (μm)	0.5
Ring Electrode Width (μm)	500
Metal Lead Width (μm)	Varies with Cooler Size
Metal Lead Thickness (μm)	2.0

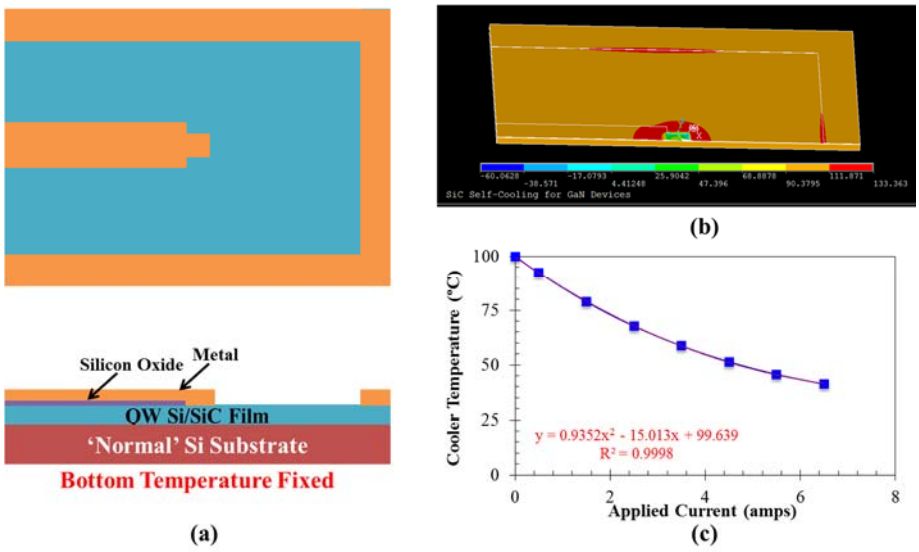


Figure 66. (a) Structure of Si/SiC thermoelectric cooler grown on a silicon substrate, (b) temperature distribution resulting from a current of 6.5 amps, and (c) change in cooler temperature with applied current.

Since the thermoelectric properties of SiC/Si superlattices are not well established, the numerical model was used to perform a parametric study on the effect of in-plane thermal conductivity, Seebeck coefficient, electrical resistivity, and electrical contact resistance on thermoelectric performance. As previously discussed, superlattice structures are made of many thin layers, and thus the through plane thermal conductivity may be much lower than the in-plane thermal conductivity. Therefore, the through-plane thermal conductivity was held constant at 2.5W/m-K while the in-plane thermal conductivity was varied from 2.5W/m-K to 200W/m-K, as shown in Figure 67.

As expected, reducing the in-plane thermal conductivity improved the cooling performance, since lower in-plane thermal conductivity prevented thermal spreading, and thus, the Peltier cooling is highly localized around the metal contact. The results show that if the in-plane thermal conductivity decreases from 200W/m-K to 2.5W/m-K, the cooling performance can be improved by at least 40°C. Additionally, reductions

in the in-plane thermal conductivity should not increase the through plane thermal resistance, thus avoiding the parasitic insulating effect previously discussed.

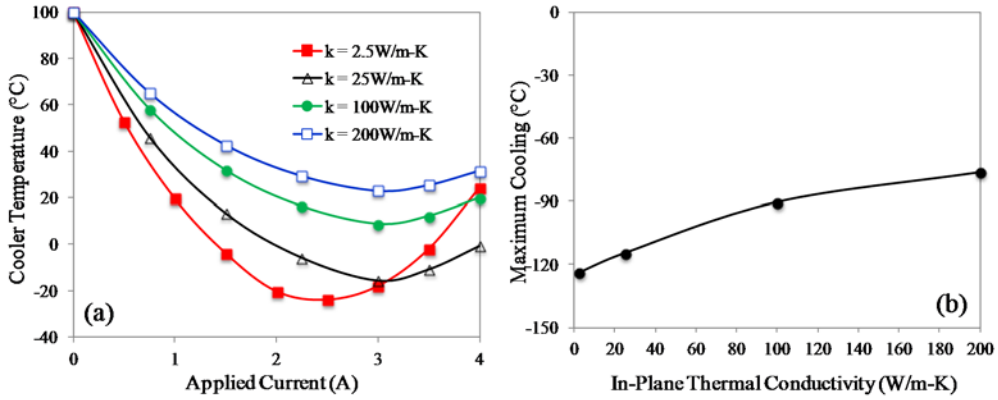


Figure 67. (a) Cooler temperature as a function of applied current and (b) maximum change in cooler temperature as a function of the Si/SiC film's in-plane thermal conductivity.

The Seebeck coefficient of the 10µm thick Si/SiC superlattice was varied from 600µV/K to 1500µV/K, as shown in Figure 68, and as it was found that Seebeck coefficient had a significant effect on the cooling performance. It can be seen that increasing the Seebeck coefficient from 600µV/K to 1200µV/K increases the cooling at the cooler by nearly three times, from 46K to 127K.

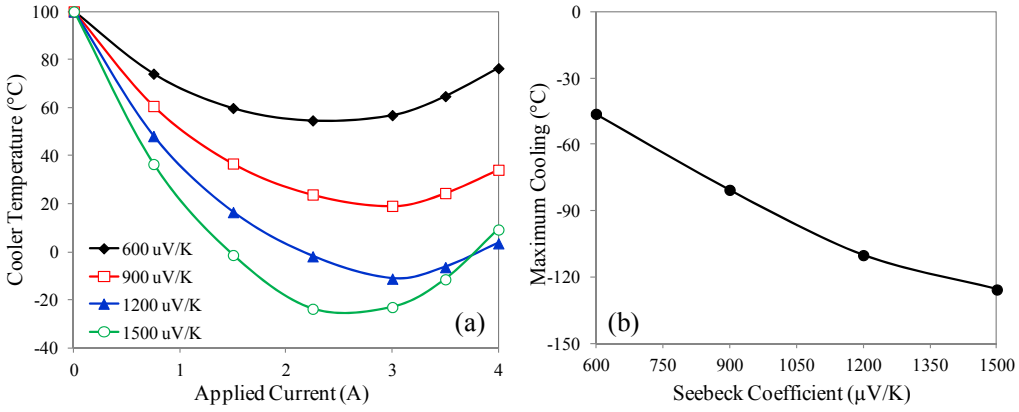


Figure 68. (a) Cooler temperature as a function of applied current and (b) maximum change in cooler temperature as a function of the Si/SiC film's Seebeck coefficient.

The effect of the electrical resistivity in the Si/SiC superlattice was also studied, as shown in Figure 69. The electrical resistivity was varied from 5Ω-μm to 35Ω-μm and it was found that decreasing the electrical resistivity increases the optimum current and improves cooling performance, due to the reduction in Joule heating. It can be seen that decreasing the electrical resistivity from 35Ω-μm to 5Ω-μm doubled the amount of cooling at the cooler, from 61K to 125K.

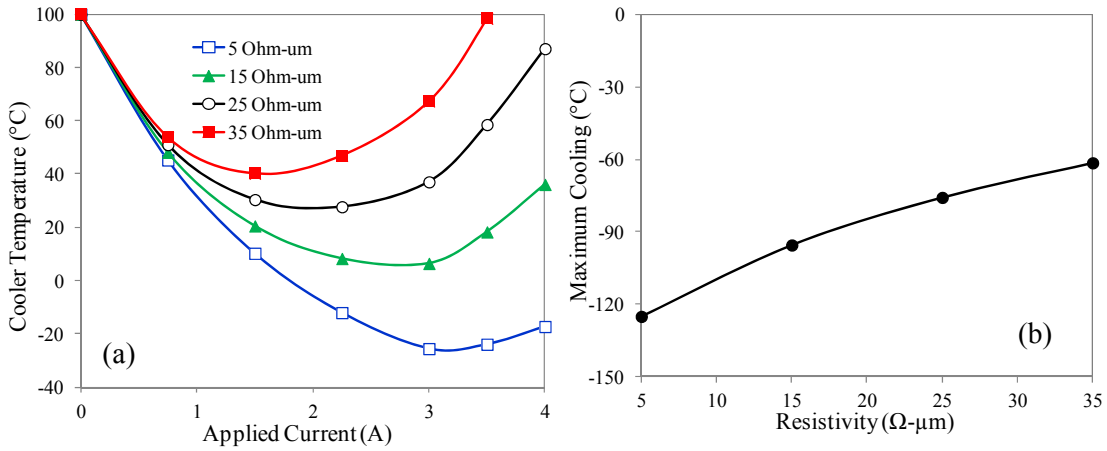


Figure 69. (a) Cooler temperature as a function of applied current and (b) maximum change in cooler temperature as a function of the Si/SiC film's electrical resistivity.

Finally, Joule heating at the metal contact to Si/SiC superlattice interface is a major parasitic effect and can become a limiting factor in monolithic thermoelectric cooling. Thus, the effect of electrical contact resistance was also parametrically studied. Since the interfacial Joule heating is located in the same location that the Peltier cooling occurs, it has the potential to be more deleterious to thermoelectric cooling than the bulk Joule heating in the substrate. Additionally, since electrical contact resistance is inversely proportional to cooler size, interfacial Joule heating increases as the cooler size decreases, which is unfavorable for device miniaturization. State-of-the-art thin

film fabrication methods typically produce electrical contact resistances in the vicinity of $1\times10^{-6}\Omega\text{-cm}^2$ [73]. Thus, as shown in Figure 70, the electrical contact resistance at the metal to Si/SiC superlattice interface was varied from $1\times10^{-7}\Omega\text{-cm}^2$ to $1\times10^{-5}\Omega\text{-cm}^2$. It was found that decreasing the electrical contact resistance to values below $1\times10^{-6}\Omega\text{-cm}^2$ only provided a small gain in cooling. However, electrical contact resistances above $1\times10^{-6}\Omega\text{-cm}^2$ significantly decreased the amount of thermoelectric cooling that could be produced.

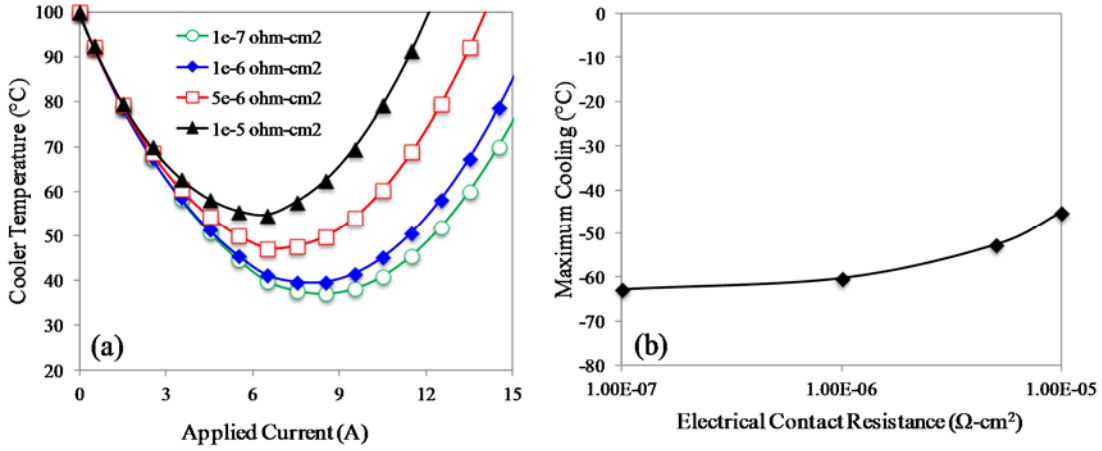


Figure 70. (a) Cooler temperature as a function of applied current and (b) maximum change in cooler temperature as a function of electrical contact resistance at the interface of the cooler and the Si/SiC film.

3.3 Experimental On Chip Monolithic Hotspot Cooling

3.3.1 Fabrication

Aside from the few studies discussed earlier in this section, there is limited experimental work on monolithic coolers available in the literature, and the monolithic cooling configuration had previously not been experimentally demonstrated at the University of Maryland. As this was the first cooler to be fabricated at UMD, silicon was used due to its well established material properties and more established

fabrication techniques. Alternate materials, such as germanium, possess a larger power factor and the ability for larger hotspot temperature reductions, however additional microfabrication expertise would have been required to move to non-silicon substrates. Therefore, a silicon based monolithic cooler was fabricated in the FabLab at the Maryland Nanocenter, as a proof of concept demonstration for this cooling technique.

Figure 71(a) shows a section view of a monolithic cooler and Figure 71(b) is a photograph of the actual coolers fabricated at UMD. For electrical connection, wires were soldered to the U-shaped ground electrode and to the solder pad for each cooler. The metal layer extends past the edge of the electrical insulation, so that when power is supplied, current flows down the metal finger and enters the substrate where the metal makes contact with the silicon, producing localized Peltier cooling. The fabrication of the coolers consisted of two deposition and patterning steps, as well as a final dicing step.

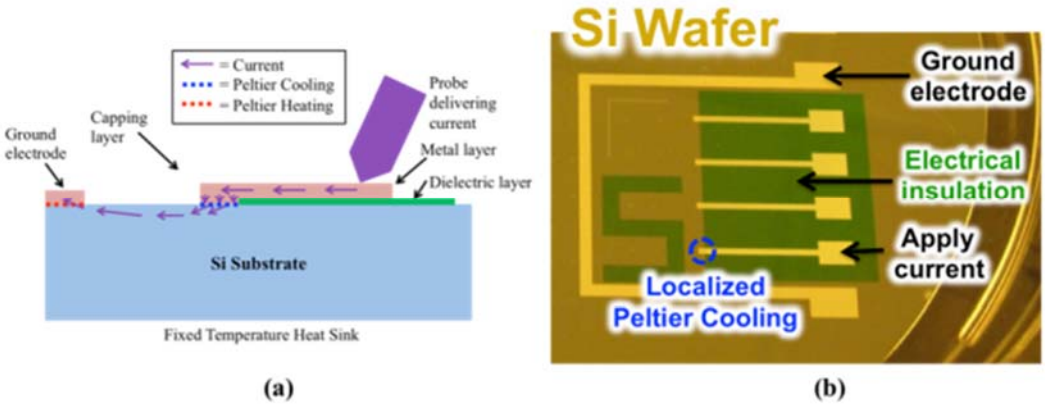
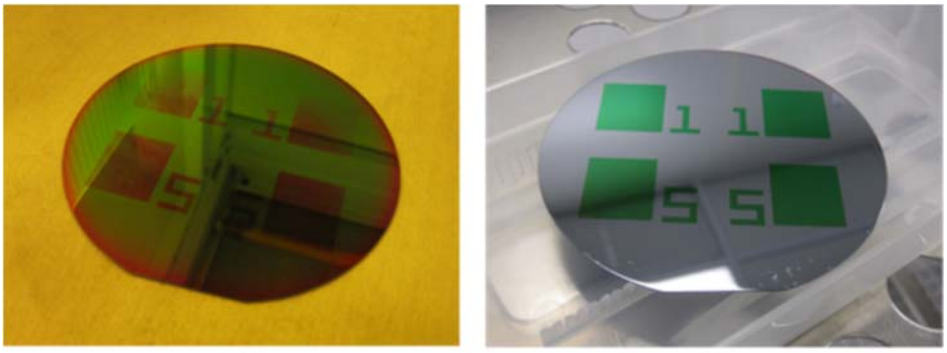


Figure 71. (a) Section view and (b) photograph of monolithic coolers fabricated on a Si wafer.

The first step in fabrication consisted of growing silicon oxide on the silicon wafer using chemical vapor deposition (CVD) to act as the dielectric layer. Patterning

of the dielectric layer was performed using a buffered oxide etch (ammonium fluoride and hydrofluoric acid) with Shipley 1813 photoresist and a positive photo-mask. After the SiO_2 was patterned and the wafer had been cleaned, approximately 1µm of gold was deposited using a Denton electron beam evaporator. The gold layer was then patterned using a similar process to the SiO_2, except that a selective etchant, specific to gold, was utilized. The wafer was then examined to ensure correct alignment of the various layers and finally, the edges of the wafer were removed using a MicroAutomation Industries dicing saw to simplify later experimentation.

Figure 72(a) shows the dielectric layer covering the wafer with the photoresist patterned and Figure 72(b) shows the dielectric layer after etching and cleaning. Similarly, Figure 73(a) shows the metal layer with the patterned photoresist and Figure 73(b) shows the wafer after the metal layer has been selectively etched. As can be seen, four sets of coolers, each set consisting of four microcoolers surrounded by a single U-electrode, were fabricated. Half of the coolers fabricated were 100µm x 100µm, while the other half were 500µm x 500µm, and this redundant approach was used to ensure some coolers would be functional, even if a few failed during fabrication or testing.



(a) (b)

Figure 72. Silicon monolithic coolers with oxide dielectric layer (a) before and (b) after photolithographic patterning.

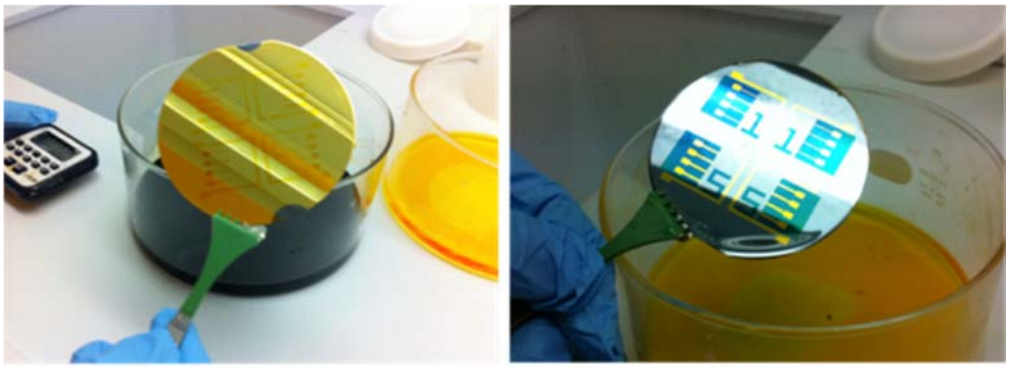


Figure 73. Silicon monolithic coolers with metaliztion layer (a) before and (b) after photolithographic patterning.

Successful fabrication of the silicon monolithic coolers required several iteration and many valuable lessons were learned through the process. One important improvement that was made in the fabrication process was switching the etching of the dielectric layer from a dry etch to a chemical etch. Dry etching produces sharp edges, which makes it difficult to deposit layers on top that conform well. Figure 74(a) shows an example where the dielectric layer was reactive ion etched (dry) and metal was deposited on top. The line across the metal layer is caused by the sharp edge of the dielectric layer and compromised the electrical continuity of the metal film. Wet etching produces a more gradual step down than dry etching and Figure 74(b) shows metal deposited on top of a wet etched dielectric layer. It can be seen that the metal forms a much more conformal layer and has improved continuity across the step.

Selection of the correct metal was also a critical consideration in the fabrication process. As previously discussed, the Peltier cooling occurs at the metal-semiconductor interface in the monolithic cooling configuration. Thus, the electrical contact resistance at this interface must be minimized for best cooling performance. For the best semiconductor-metal electrical contact, the work function of the metal must be matched

to the electron affinity, band gap, and type of doping of the semiconductor. For example, silicon has an electron affinity of 4.05eV and a bandgap of 1.1eV, and as shown in Figure 75, in order to achieve good electrical contact to p-type silicon, a metal with a work function close to silicon's electron affinity should be used. Conversely, to make contact with n-type silicon, a metal with a work function equal to sum of silicon's electron affinity and band gap should be used. Therefore, aluminum with a work function of 4.06-4.26eV is typically used to make electrical contact with p-type silicon, while gold, with a work function of 5.1-5.5eV, is often used with n-type silicon.

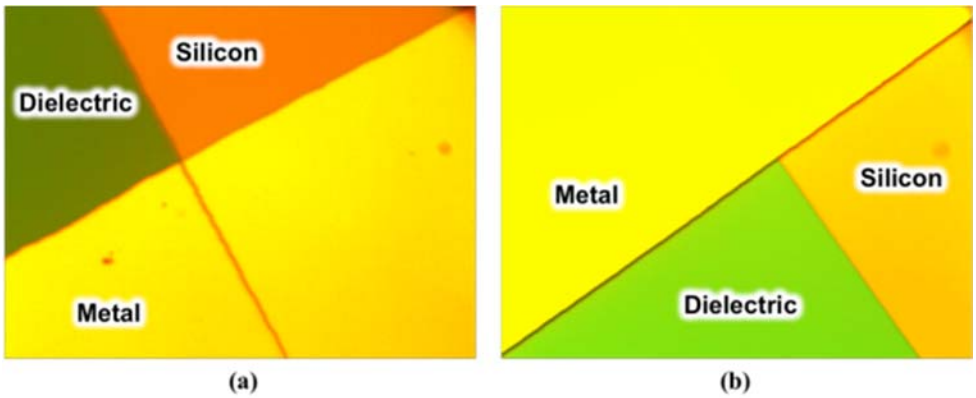


Figure 74. Close up image of the metal layer extending over the edge of the dielectric layer. (a) SiN was used as the dielectric, resulting in a sharp edge, which compromised the continuity of the metal layer, while in (b) SiO_2 was used as the dielectric, resulting in a more gradual step and improved metal conformity.

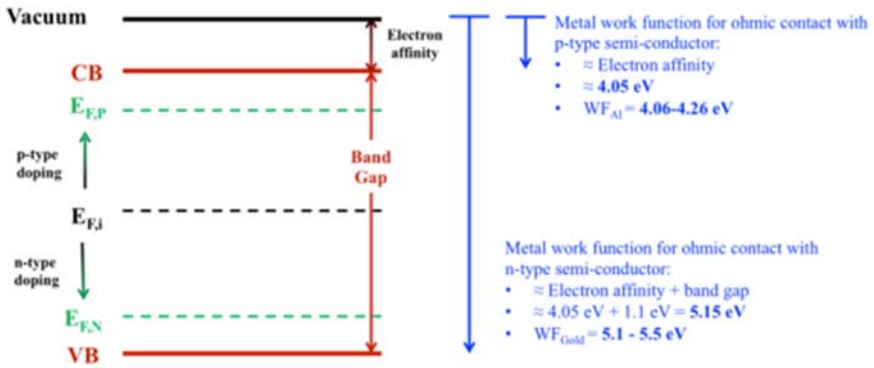


Figure 75. Example energy diagram for doped silicon, showing the importance of selecting the appropriate contact metal

3.3.2 Experimental Characterization

Testing of the silicon based monolithic coolers was performed by supplying electrical power to the coolers and measuring the temperature distribution using an infrared camera. The completed monolithic cooler consisted of several different structures with different emissivity values, making infrared imaging challenging. Uniform emissivity coatings are a common solution to the problem of multi-emissivity surfaces, however the coatings are a finite thickness and introduce additional heat spreading. The silicon monolithic coolers were only capable of producing cooling of 1-2K, thus heat spreading in the emissivity coating could degrade the cooling to a point where it could no longer be measured. Two alternative solutions are possible: silicon back-side imaging and emissivity mapping. First, the backside of the silicon, which is unpolished and uncoated and has a uniform emissivity, could be the surface imaged. While this approach would be suitable for capturing the hotspot temperature and determine hotspot cooling, it does not provide as much useful data for cooler characterization, which was the aim of the present experiment.

Alternatively, a post-processing technique, such as emissivity mapping or frame subtraction, could be used. In this method, a computer algorithm uses known temperatures to map the various emissivity values and uses this map to calculate the correct temperature field. Regrettably, this option also has limitations, mainly the strength of the signal captured by the IR detector and used to calculate temperature, is directly proportional to emissivity, and, thus, even if the computer can compensate for spatial variations in emissivity, the temperature measurement of samples with low emissivity will always have a low signal to noise ratio.

Figure 76 shows the test setup used for initial characterization of the monolithic coolers, consisting of the silicon wafer, an infrared camera, and a power supply. As discussed, emissivity mapping was used to compensate for the large disparity in emissivity between the silicon, silicon oxide, and metallization and Figure 77 shows an infrared image of the monolithic coolers with and without current applied. Due to the low emissivity of the metal, it is difficult to measure the temperature at the cooler itself, however temperature reductions of up to 0.5K can be seen in the area immediately surrounding the cooler. Additionally, the full field temperature distribution produced by infrared imaging makes it easy to see parasitic effects, such as the Joule heating generated at the solder pads.

Figure 78 shows a close-up of the temperature distribution of a 500μm x 500μm microcooler when 0.5 amps of current is supplied. The full field picture in the upper left of the figure shows an infrared image taken with no emissivity mapping and it can be seen that reflectivity of the metal causes significant fluctuations in the measured temperature. Figure 78(b) shows the temperature distribution along a line across the edge of the cooler with and without cooling. As discussed, the temperature of the cooler itself could not be measured with the infrared camera due to its high reflectivity and low emissivity and does not appear to change when the cooler is switched on. However, it can be seen that the Peltier cooling reduces the temperature in the surrounding silicon substrate by approximately 0.5K.

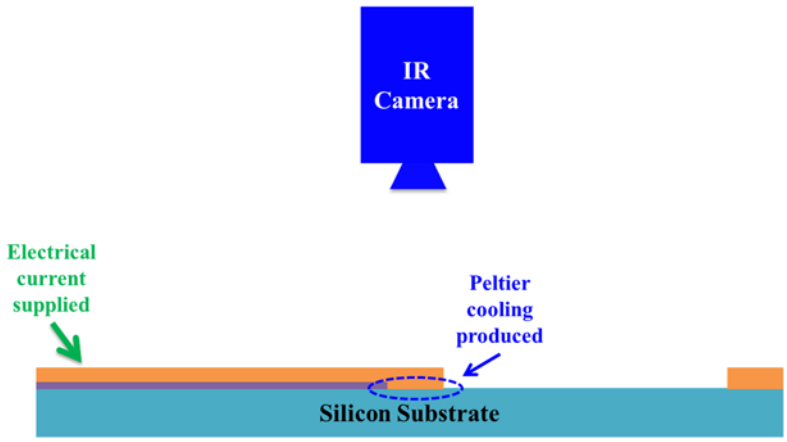


Figure 76. Schematic of the test setup used for initial characterization of the silicon monolithic coolers.

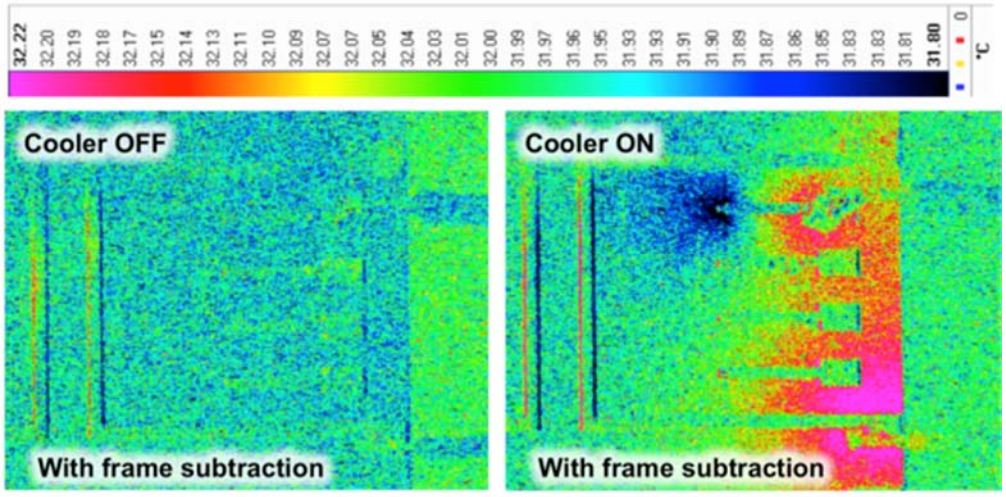


Figure 77. Infrared image showing the temperature distribution on the silicon chip when the cooler is off and on.

The ability of the silicon based monolithic cooler to cool a low power hotspot was also tested, and Figure 79 shows a schematic of the test setup, consisting of the silicon substrate, infrared camera, electrical power supply, and a laser for hotspot creation. Additional information on the laser created hotspot can be found in Chapter 5. Figure 80 shows an infrared image of a low power hotspot on the backside of the silicon wafer with and without thermoelectric cooling. In this example, the hotspot

power is approximately 0.1 watts with an average heat flux of 15W/cm^2 and the monolithic cooler is 500µm x 500µm, supplied with 0.5 amps of current. It can be seen that when the cooler is inactive a hotspot temperature rise of 0.5K occurs, and when the thermoelectric cooler is activated that temperature rise is removed.

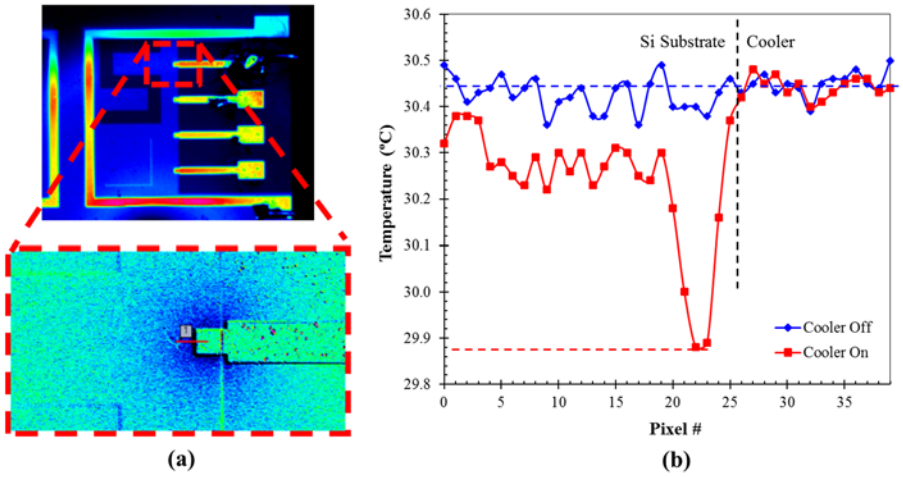


Figure 78. (a) Infrared image of a 500µm x 500µm cooler and (b) the temperature distribution along a line that runs across the cooler edge when 0.5 amps of current is supplied.

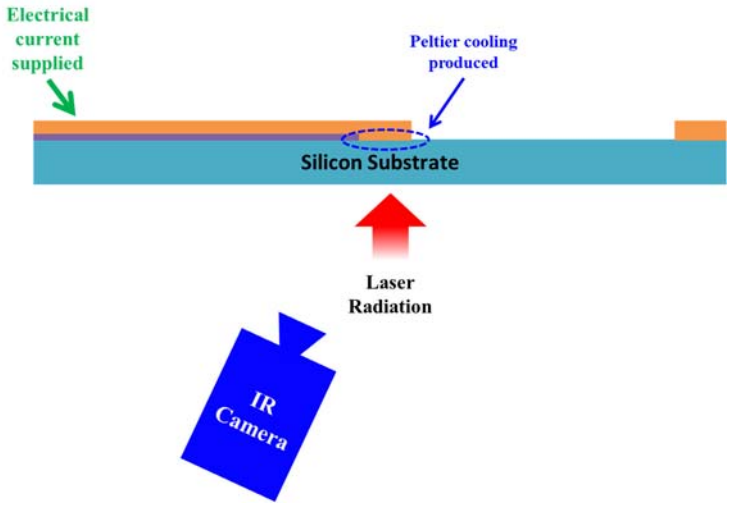


Figure 79. Schematic of the experimental setup used to test hotspot cooling ability of the silicon based monolithic coolers.

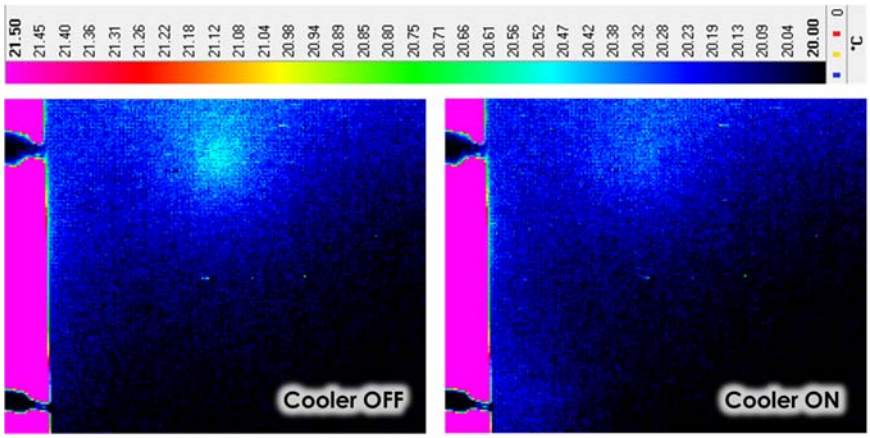


Figure 80. Infrared image of a low power hotspot on the bottom of the silicon wafer, with and without thermoelectric cooling.

In addition to steady-state testing, a preliminary study of the transient behavior of the silicon monolithic cooler was also conducted. Figure 81(a) shows the hotspot temperature as a function of time when the monolithic cooler is switched on at its optimum current of 0.5 amps. It can be seen that when the cooler is activated, the hotspot asymptotically approaches its steady state temperature. Figure 81(b) shows the hotspot temperature over time when a current pulse, with magnitude greater than the optimum steady state value, is applied to the monolithic cooler. It can be seen that when the pulse is first activated, there is initially a sharp drop in hotspot temperature due to the burst of Peltier cooling, followed by a steady rise in temperature as the volumetric Joule heating diffuses to the hotspot. Additionally, when the cooler is switched off there is a sharp increase in hotspot temperature, indicated with a red arrow in the figure, due to the removal of the Peltier cooling but continued diffusion of volumetric Joule heating.

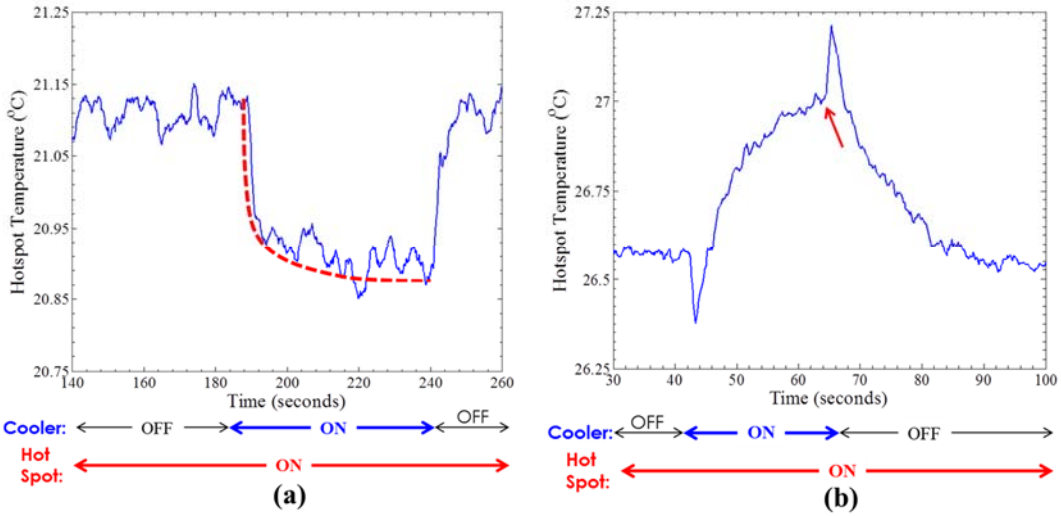


Figure 81. Hotspot temperature over time when the monolithic cooler is activated with a current pulse with a magnitude equal to the (a) optimum steady state current and (b) three times larger than optimum steady state current.

3.4 Conclusions

The monolithic cooling configuration is a planar thermoelectric cooling approach, which utilizes the underlying semiconductor substrate as a leg of the thermoelectric circuit. On-chip hotspot cooling, using the monolithic thermoelectric cooling configuration, was explored both numerically and experimentally. Numerical modeling and simulation was used to study the transient behavior of the monolithic cooling configuration and explore potential advances in performance that could be made using novel thermoelectric substrates with superior thermoelectric properties. In the transient modeling it was found that transient "super cooling" could be used to provide bursts of additional Peltier cooling which could be used to cool short duration, high heat flux hotspots. Two new metrics, Transient Advantage and Transient Penalty, were introduced to help capture the trade-offs involved. The large magnitude current pulses used in "super cooling" produce additional Joule heating, leading to an eventual rise in hotspot temperature and it was, therefore, observed that selecting the correct

current pulse profile is critical for maximizing the transient "super cooling", while minimizing the transient hotspot temperature rise that follows.

The numerical modeling also showed that the monolithic cooling configuration could be used to cool a dynamic hotspot, with a heat flux that varied over time. However, due to the spatial separation between the cooler and the hotspot, anticipatory cooling, consisting of activating the cooler slightly earlier than the hotspot, was required for the most effective hotspot suppression. Finally, thermal conductivity, Seebeck coefficient, electrical resistivity, and electrical contact resistance were parametrically studied and it was found that significant increases in hotspot cooling, on the order of a 100K, could be achieved if certain thermoelectric material property landmarks could be reached.

Finally, a silicon based monolithic cooler was successfully fabricated and tested at the University of Maryland. The cooler temperature was measured using an infrared camera and it was found that the monolithic cooler could provide 0.5K of cooling at the cooler. Additionally, the silicon based monolithic cooler was used to cool a low power laser-created hotspot in both steady state and transient operation.

4 Micro-Contact Enhanced Thermoelectric Cooling

4.1 Introduction and Motivation

State of the art thermoelectric modules are only capable of producing cooling fluxes on the order of 100s of watts per square centimeter, making them unsuitable for directly cooling kW/cm^2 level hotspots. Mini-contact enhanced thermoelectric cooling concentrates the cooling provided by a thermoelectric module, resulting in larger

cooling fluxes, which can be used to "extract" highly-concentrated heat sources from the substrate and reduce the temperature of the local hotspots. Previous work on mini-contact enhanced thermoelectric cooling was performed by Wang, Yang, and Bar-Cohen, and consisted of optimization using numerical models and experimentation for model validation [74]-[77].

Figure 82 shows a representative schematic of a mini-contact enhanced cooling system studied by Yang *et al.* [75]. As can be seen, the mini-contact concentrates the cooling produced by the thermoelectric module onto a smaller area, increasing the cooling flux removed from the hotspot. In this study, the mini-contact was fabricated by etching trenches in a silicon chip creating a pillar structure, to which the thermoelectric device was attached. The study utilized a Bi_2Te_3 based thermoelectric cooler with a footprint of 3.6mm x 3.6mm in order to cool a 400µm x 400µm hotspot with a heat flux of 1250W/cm^2 [75].

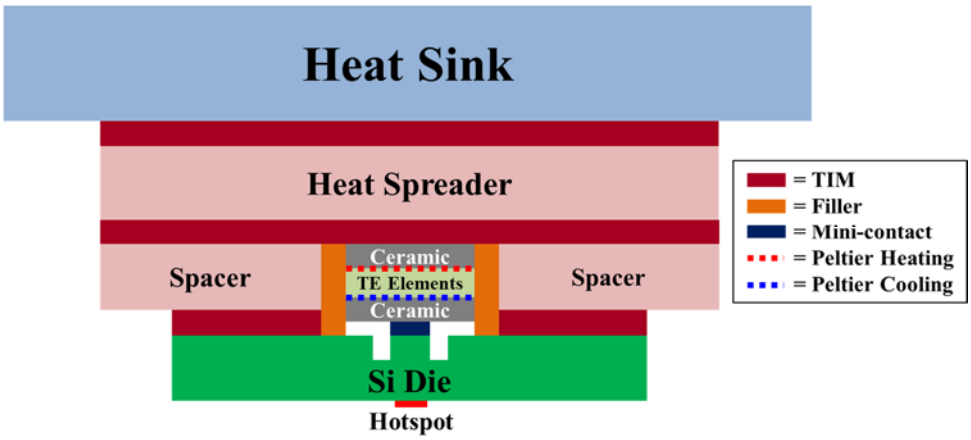


Figure 82. Schematic of the mini-contact enhanced thermoelectric cooling system tested by Yang *et al.* [75].

In order to determine the optimum mini-contact size, which would minimize the hotspot temperature rise, thermoelectric cooling was concentrated in areas ranging

from 3600μm x 3600μm (no concentration effect) to 300μm x 300μm. It was found that with no mini-contact, i.e. no concentration, thermoelectric cooling was not effectively concentrated on the hotspot, resulting in a hotspot temperature rise of over 20K. If 1mm x 1mm mini-contact was utilized, more of the thermoelectric cooling reached the hotspot, thus completely removing the hotspot temperature rise. The effect of the depth of the trench in the silicon was not studied in the original work, but there is likely an optimum depth, which balances the beneficial concentrating effect and the disadvantageous thermal conduction resistance resulting from a long pillar with a small cross sectional area. Yang *et al.* validated their numerical model with an initial experiment, in which the temperature of a 613W/cm^2 hotspot was reduced by approximately 5.5K using a 500μm x 500μm x 500μm cube of silicon as a mini contact [75].

In 2009, Wang *et al.* modified the mini-contact enhanced configuration to include a discrete copper mini-contact, rather than etching the silicon chip as previously discussed, as shown Figure 83 [74]. It should be noted that the figure is not to scale and the thickness of the lower layer of thermal interface material (TIM) is exaggerated in order to allow space to provide details on the structure of the mini-contact and TEC assembly. An extensive parametric study was performed using a numerical model and the results were validated against experimental data.

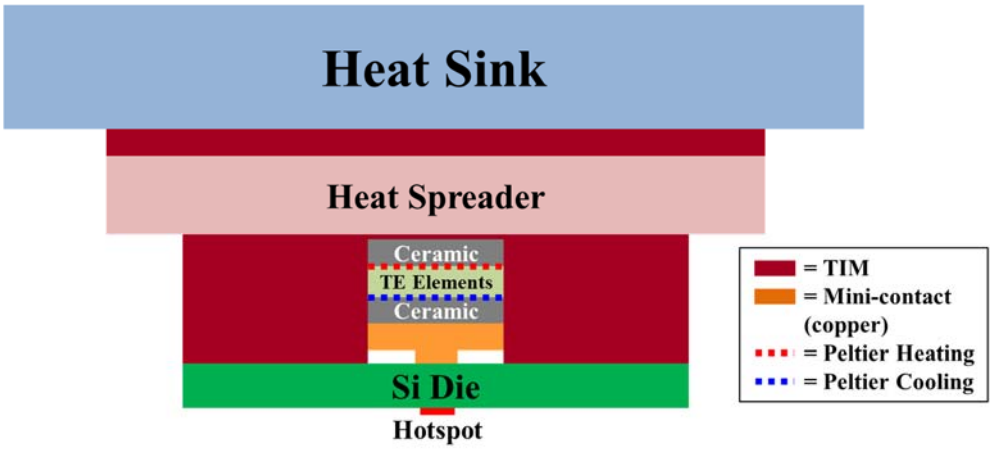


Figure 83. Schematic of improved mini-contact enhanced thermoelectric cooling system tested by Wang *et al.* [74].

Figure 84 shows the temperature distribution along the bottom the silicon chip for both the 2007 study by Yang and the 2009 study by Wang. In the 2007 study (shown with solid lines), the temperature distribution is shown with and without mini-contact enhanced cooling, and it is clear that when no mini-contact is utilized, the thermoelectric cooling is not concentrated enough to cool the hotspot and the temperature at the center of the chip rises to over 130ºC. However, when mini-contact enhanced thermoelectric cooling is utilized, the concentrated thermoelectric cooling completely removes the hotspot, reducing the center temperature of the chip to less than 115ºC.

In the 2009 study (shown with dashed lines), a cooler with 20µm thick BiTe elements and a thermal contact resistance of $1x10^{-7}m^2K/W$ at the mini-contact to silicon interface was assumed. As shown, the hotspot causes the temperature at the center of the chip to rise to approximately 137ºC when no thermoelectric cooling is used. However, when mini-contact enhanced thermoelectric cooling is utilized, the hotspot

temperature rise is almost completely removed and the temperature at the center of the chip is reduced to 120ºC.

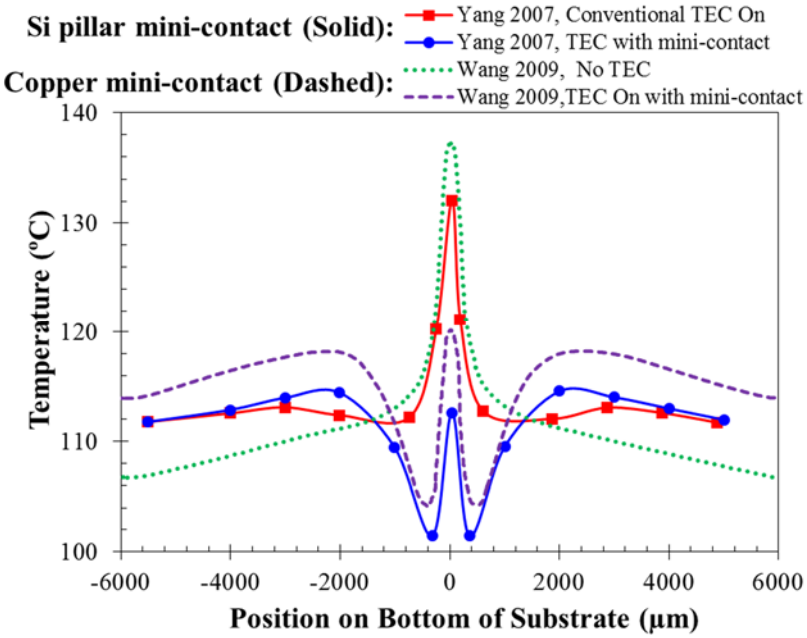


Figure 84.Temperature distribution on the bottom of the silicon substrate in the 2007 Yang and 2009 Wang mini-contact enhanced thermoelectric cooling studies [74], [75].

Figure 85 shows the maximum hotspot cooling as a function of mini-contact tip size for three different thermoelectric element thicknesses, along with previous results obtained in the 2007 Yang *et al.* study [74], [75]. It can be seen that there is an optimum mini-contact size, which minimizes the hotspot temperature, for each specific case. Additionally, the results from the study show that thinner elements produce larger reductions in hotspot temperature, in agreement with the previously observed inverse relationship between maximum heat pumping capacity and thermoelectric element thickness.

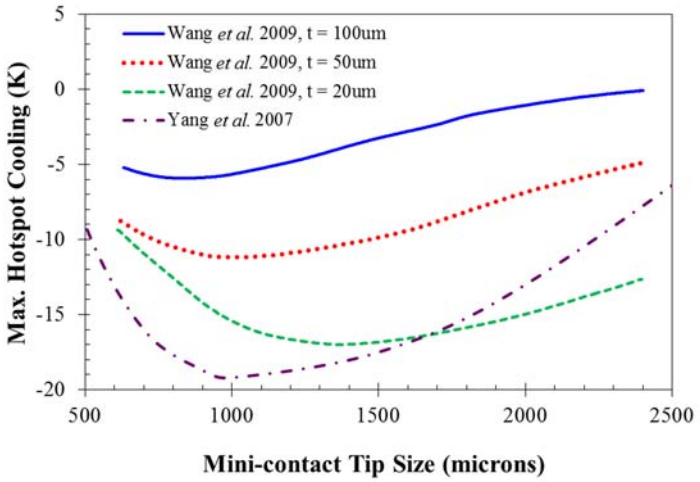


Figure 85. Dependence of hotspot cooling on mini-contact tip size, assuming a thermal contact resistance of $1x10^{-7}$ m^2K/W [74], [75].

In order to validate the numerical results, a commercially available thermoelectric device, with a footprint of 1.8mm x 1.8mm, was attached to a silicon test chip. The silicon test chip was heated uniformly with powers of 0, 30, and 67 watts and the maximum temperature reduction achieved with mini-contact enhanced cooling was measured. Figure 86 shows the maximum spot cooling as a function of mini-contact tip size for the three chip powers tested in the Wang *et al.* study. Larger chip powers resulted in elevated chip temperatures, which increased the amount of Peltier cooling, thus larger temperature reductions were achieved at higher chip powers. When the chip was dissipating a background power of 0W, a maximum spot cooling of approximately 7K was achieved. Alternatively, when the chip was dissipating a background power of 67W, approximately 9K of spot cooling was measured. The maximum spot reduction achieved experimentally was approximately 9K and there was good agreement with the numerical results. In the 2007 Yang *et al.* study, only one mini-contact tip size was tested experimentally, thus a single point is shown in Figure 86 for reference.

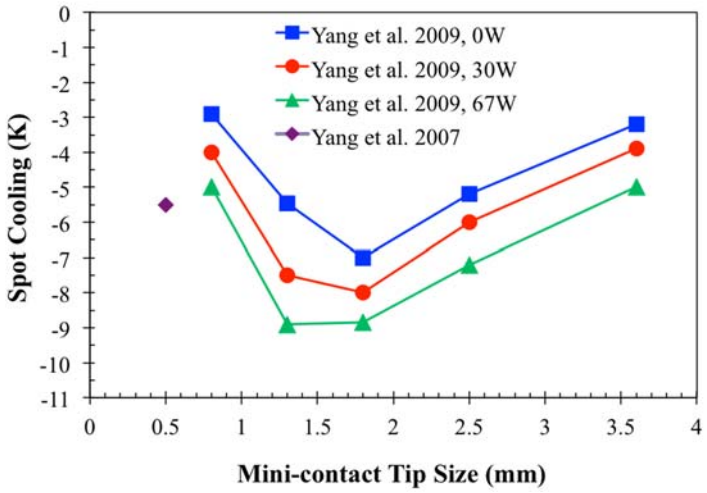


Figure 86. Experimentally determined temperature reduction on the backside of the silicon substrate as a function of mini-contact tip size [74], [75].

4.2 DARPA ICECool Fundamentals Program

Mini-contact enhanced thermoelectric cooling was a key element in UMD's efforts in DARPA's ICECool Fundamentals program, which consisted of microfluidic cooling of a 1cm x 1cm chip dissipating a background heat flux of 1kW/cm^2 combined with hotspot cooling of a 200µm x 200µm, 5kW/cm^2 hotspot [78]. The ICECool project required reducing the temperature rise resulting from the 5kW/cm^2 hotspot to less than 5K.

Prof. Michael Ohadi served as PI for the University of Maryland ICECool team and the Smart and Small Thermal Systems Laboratory, supervised by Prof. Ohadi, focused on the microfluidic cooling of the 1kW/cm^2 background heat flux. Thermoelectric cooling was used to cool the 5kW/cm^2 hotspot and consisted of two phases. First, the feasibility of using micro-contact enhanced thermoelectric cooling to remove the temperature rise of the high heat flux hotspot was demonstrated using numerical modeling and a hotspot cooling experiment. Second, in an on-going task,

the thermoelectric cooler and micro-contact are being integrated into the global manifold microchannel cooling system for an experimental demonstration of simultaneous background and hotspot cooling.

Figure 87 shows a schematic of the combined manifold microchannel and micro-contact enhanced thermoelectric cooling system. It can be seen that fluid is supplied from the edge of the chip and the microfluidic manifold delivers the fluid vertically into each microchannel. The thermoelectric cooler is attached to a micro-contact pillar, which concentrates the cooling to remove the hotspot heat flux at the center of the chip. The hot side of the thermoelectric module is cooled by fluid delivered via the manifold.

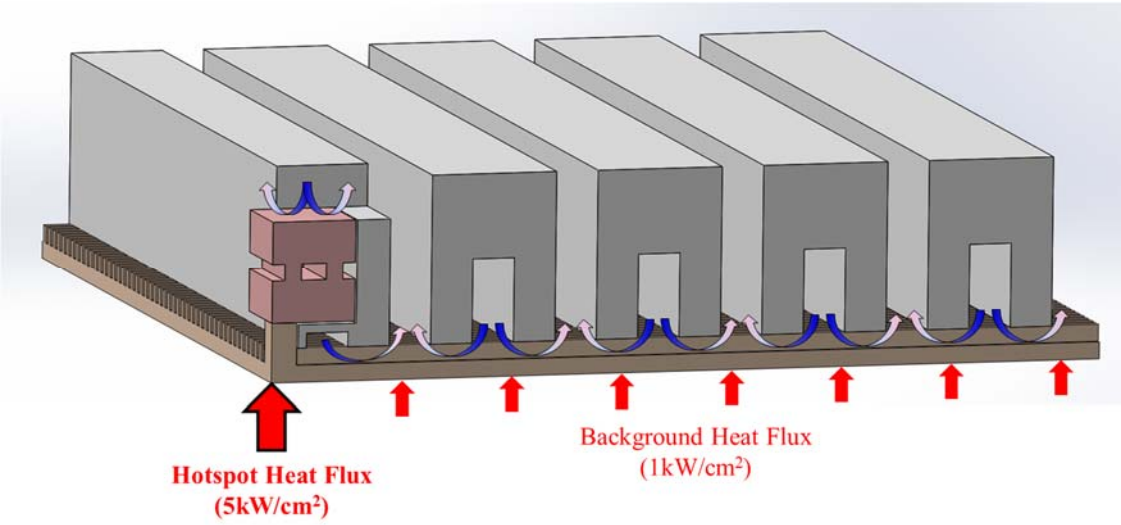


Figure 87. Manifold microchannel and micro-contact enhanced thermoelectric cooler used to cool the background and hotspot heat fluxes of 1kW/cm^2 and 5kW/cm^2, respectively.

4.3 Mini/Micro-Contact Form Factors and Materials

Before reaching the design shown in Figure 87, a variety of mini-contact form factors and materials were investigated in order to determine which were practically

feasible and most suitable for cooling of the high heat flux hotspot. Many different mini/micro-contact form factors and materials were considered in collaboration with Dr. Patrick McCluskey and the CALCE Laboratory at the University of Maryland, College Park.

Figure 88 shows four mini-contact shapes that were studied, consisting of both integrated and discrete contact designs. The integrated mini-contact shown in the upper left of the figure is T-shaped and etched directly out of the Si or SiC substrate. It was found that non-uniform cross sectional area was very difficult to fabricate, thus as previously discussed, much of the work focused on a simpler pillar shaped mini/micro-contact, in which spreading occurred in the bottom header of the thermoelectric module, rather than in the top section of the micro-contact.

Similar to the work previous performed by Wang, Yang , and Bar-Cohen, the other three mini-contact shown in Figure 88 are discrete contacts, which are attached to the underlying substrate using solder. As can be seen, a T-shaped, lofted, and tapered mini-contact were all studied and the thermal and reliability performance, as well as the manufacturability, of different discrete contact materials were considered.

The tapered mini-contact has a relatively low thermal resistance due to its larger cross sectional area for heat conduction, while the T-shaped mini-contact has a larger thermal resistance due to small cross sectional area of its lower portion. Discrete mini-contacts made of copper, silver-diamond composite, and pure diamond were considered, and details on their reliability performance can be found in the M.S. thesis by Khanna [79]

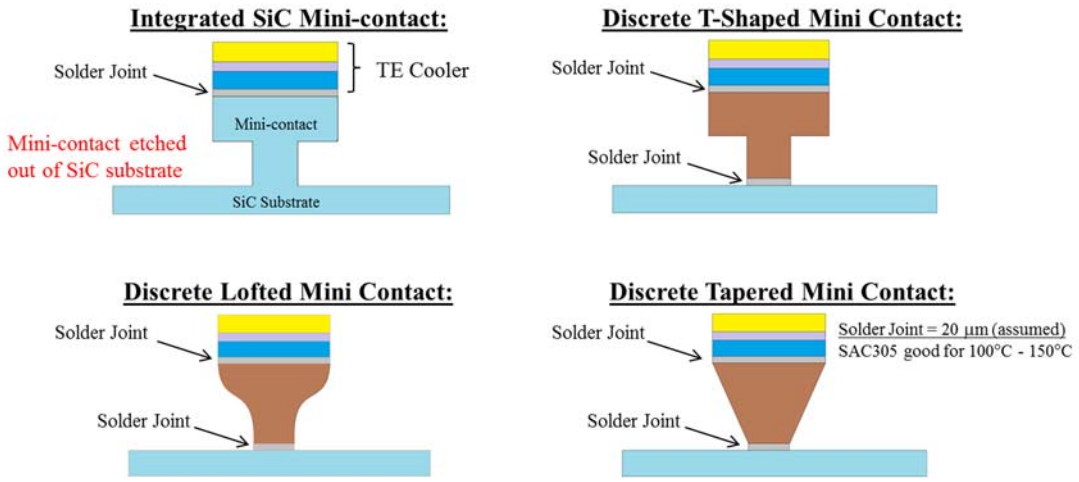


Figure 88. Integrated and discrete mini-contacts considered for high heat flux hotspot cooling.

Silver diamond composites are a relatively new composite material, with no products currently commercially available. However, their high thermal conductivity, approximately 750 W/m-K, and the fact that they can be molded into a variety of shapes, makes silver-diamond composites very good candidates for use as a discrete mini-contact structure. Figure 89 shows the thermal conductivity of silver-diamond composite shims that have been reported in the literature [80], [81]. As can be seen in Figure 89, the silver diamond composite can have a thermal conductivity of more than 800W/m-K at 22ºC, however the conductivity of the composite decreases to 650W/m-K at a temperature of 200ºC. It should also be noted that thermal cycling reduces the thermal conductivity by nearly 10% for a test temperature of 22ºC, but only has a minor impact on the conductivity at higher testing temperatures.

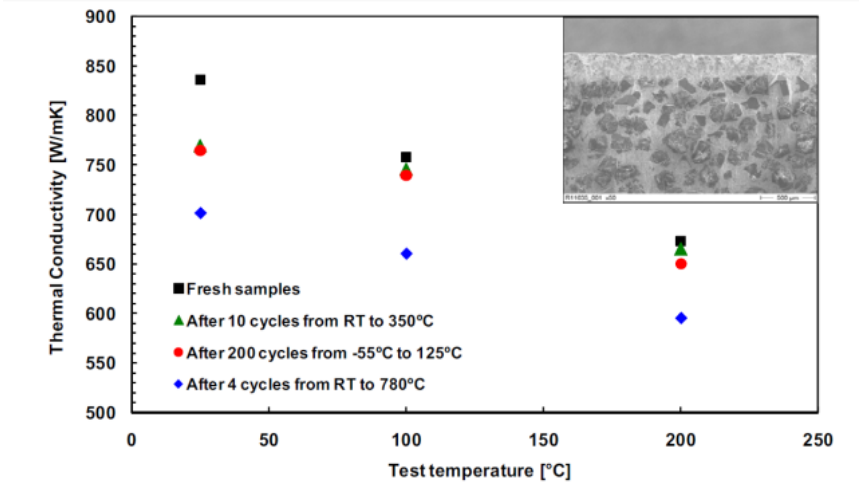


Figure 89. Thermal conductivity of a silver diamond composite after thermal cycling as a function test temperature [80].

Figure 90 shows a comparison in thermal performance between a copper and silver-diamond composite mini-contact. In both cases, a cooling flux representative of a thin-film thermoelectric cooler is applied to the top of the mini-contact to remove a hotspot on the bottom of the substrate. While both contacts are capable or reducing the hotspot temperature rise, it can be seen that there is a substantially smaller temperature gradient in the silver diamond mini-contact, relative to the copper. The thermal conductivity of the silver diamond composite is approximately twice that of copper, meaning that for a given geometry, the thermal resistance of the composite contact is half that of the copper.

Although some of the discrete mini-contact showed promise for high heat flux hotspot cooling, it was ultimately decided to focus on the integrated pillar micro-contact for thermal, reliability, and manufacturability reasons. Thermally, the integrated mini-contact had the advantage of removing the thermal interface resistance through the solder layer at the contact-to-substrate interface. Diamond and silver-

diamond mini-contacts are very difficult to manufacture, and, in the near-term, are likely to have been limited to simple geometries with constant cross sectional area. Finally, in the M.S. thesis by Khanna, it was found the mini-contact to substrate solder joint was the most likely aspect of the system to fail due to thermal cycling, and that using an integrated mini/micro-contact significantly improved the system's reliability by removing this interface [79].

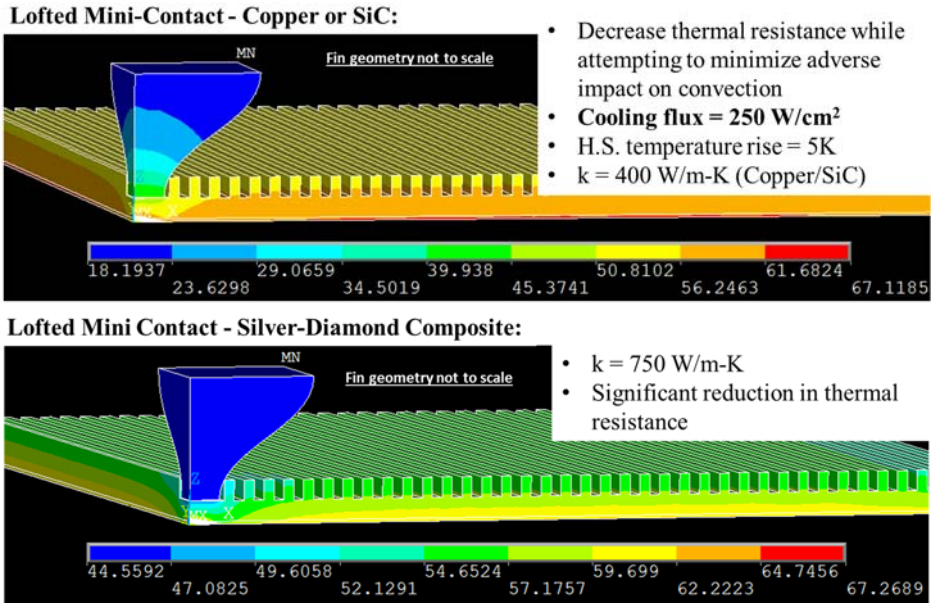


Figure 90. Numerical comparison of the thermal performance of the lofted mini-contact made of copper and a silver diamond composite.

As shown in Figure 91, the integrated micro-contact was created by etching a pillar out of the Si or SiC substrate and soldering a thermoelectric device to the top. The bottom header of the TEC, combined with the substrate pillar acts in a similar way to the T-shaped mini-contact previously discussed, however the integrated mini-contact benefits from having one less thermal interface resistance. Additionally, if advanced etching techniques are developed, it may be possible, in the future, to fabricate a tapered contact to further reduce the thermal resistance. As was the case for the monolithic

cooling configuration, both numerical and experimental research tasks were carried out for the micro-contact enhanced cooling configuration.

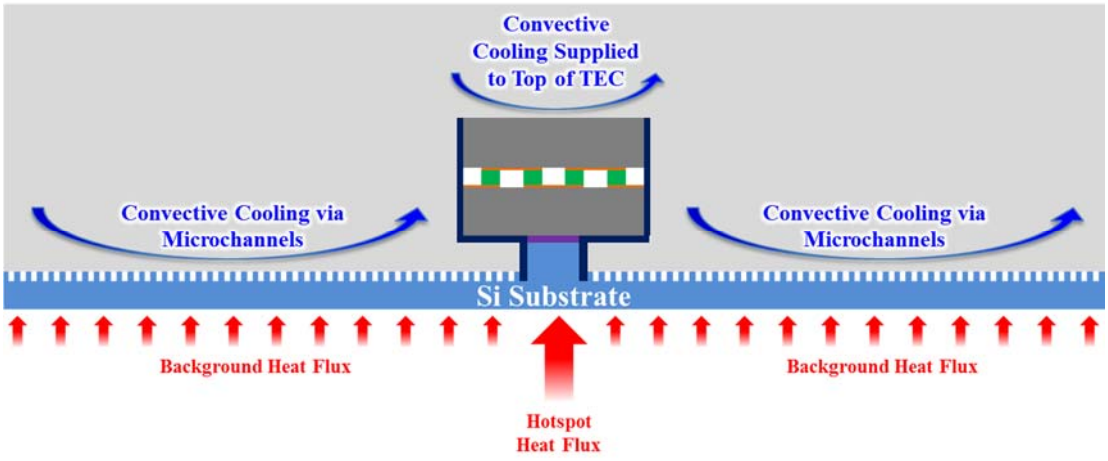


Figure 91. Schematic of an integrated SiC micro-contact etched directly out of the underlying substrate, which could be used to cool high heat flux hotspots.

4.4 Device Level Simulation of a Thermoelectric Module

Before modeling the full thermal management system, device level numerical models of commercially available thermoelectric modules were created and validated against manufacturer supplied performance curves. Figure 92 shows the boundary conditions used to model a Laird HV37 thin film thermoelectric module. As can be seen, the model consisted of ceramic headers, copper traces, thermoelectric elements, and interface volumes. The interface volumes represented the combined effect of both the solder between the copper and the thermoelectric elements and the thermal and electrical contact resistances. The electrical resistivity and thermal conductivity of the interface volumes were adjusted to tune the performance of the numerical model to match the performance curves supplied by Laird. Device performance was measured by fixing the bottom temperature of the modules and applying electrical current to the copper traces. The top surface of the thermoelectric device was left adiabatic for

determining the maximum DT and a heat flux was applied to determine the maximum device heat pumping.

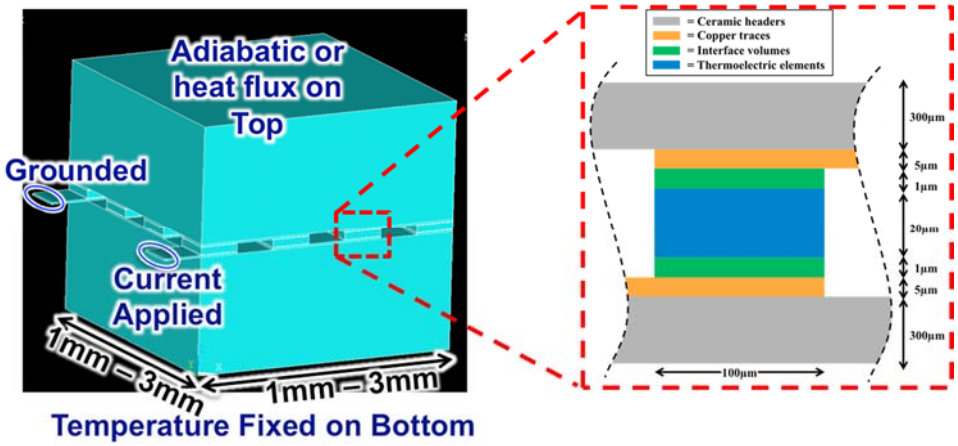


Figure 92. Geometry and boundary conditions used to model the Laird HV37 thin film thermoelectric cooler. Interface volumes were used to tune performance of the device to match manufacturer supplied values.

The N and P type bismuth telluride elements in the module were assumed to have Seebeck coefficients of -220 x 10^{-6}V/K and 220 x 10^{-6}V/K, respectively, and all other materials were assumed to have a Seebeck coefficient of 0V/K. The ceramic headers were assumed to be electrical insulators and have thermal conductivity of 250W/m-K, comparable to that of aluminum nitride. The copper, solder, and bismuth telluride thermoelectric elements were assumed to have electrical resistivity and thermal conductivity of 1.7 x 10^{-8}Ω-m, 1.3 x 10^{-7}Ω-m, and 1.0 x 10^{-5}Ω-m, and 400W/m-K, 65W/m-K, and 1W/m-K, respectively. Figure 93 shows temperature contours in the HV37 when 1 amp of electrical current is supplied while the bottom surface is fixed at 47ºC and the top surface is adiabatic.

After several iterations, it was found that thermal and electrical contact resistances of 5x10^{-6} m^2-K/W and 5x10^{-11} Ω-m^2, respectively, produced performance

that matched the manufacture supplied values well. It should be noted that the contact resistances may not be the actual real world values, since the interface volumes were used to represent both interface resistances and the solder in a single volume. The model was later refined and two dimensional contact elements were used to more accurately represent contact resistances, and will be discussed in Section 4.6. Figure 94 shows the thermal performance of the HV37 predicted by the numerical model when thermal and electrical contact resistances of $5x10^{-6}$ m^2-K/W and $5x10^{-11}$ Ω-m^2, respectively, are applied. It can be seen that the maximum ΔT of 45K is obtained at 1 amp and that the maximum cooling flux supplied by the device is 66W/cm^2, which both agree exactly with the manufacture supplied values [18].

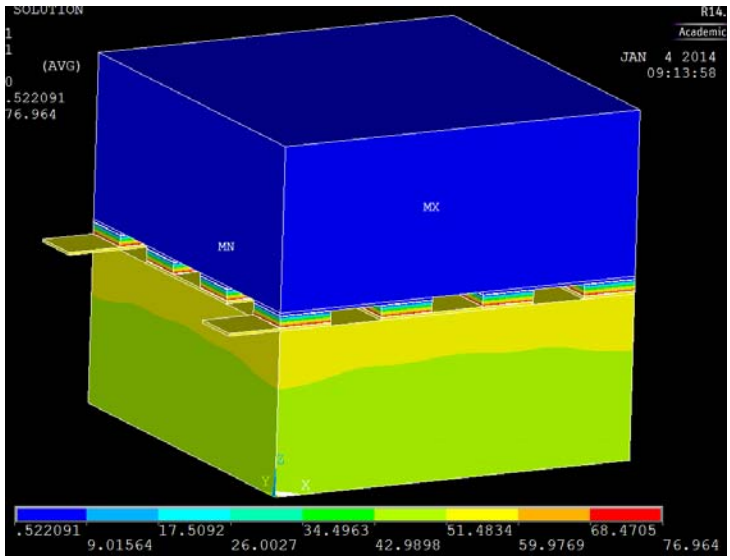


Figure 93. Temperature contours when HV37 is supplied with 1 amp of electrical current while the bottom surface is fixes at 47ºC and the top surface is adiabatic.

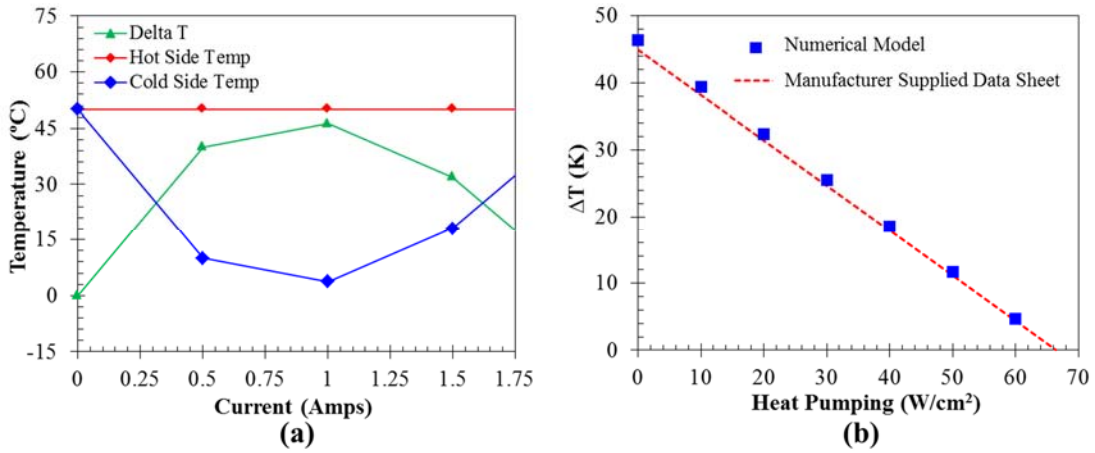


Figure 94. Numerically obtained results for (a) temperature as a function of applied current and (b) Device ΔT as a function of heat pumping for a Laird HV37 thin film thermoelectric cooler [18].

4.5 Numerical Simulations of Micro-Contact Enhanced Cooling

4.5.1 Hotspot Cooling on Si Substrates

Once the thermoelectric device level modeling had been completed, a three dimensional, system level numerical model was created in ANSYS Mechanical APDL and was validated against experimental results. The numerical model consisted of the substrate, the micro-contact pillar, and the HV37 thermoelectric module with geometry and boundary conditions that are similar to those shown in Figure 91. As a starting point, a silicon substrate with a background heat flux of 500W/cm^2 was applied to the bottom of the chip and a 200µm x 200µm hotspot with a heat flux of 3kW/cm^2 was applied at the center.

Silicon has a lower thermal conductivity than silicon carbide, resulting in larger hotspot temperature rises and greater temperature gradients from the active side to the cooled side of the substrate. Therefore, the background and hotspot heat flux of 500W/cm^2 and 3kW/cm^2, respectively, were below the ICECool metrics for the silicon

modeling. When silicon carbide was considered, as will be discussed in Section 4.5.2, the background and hotspot heat fluxes were increased back to ICECool metrics of 1kW/cm^2 and 5kW/cm^2.

An effective base heat transfer coefficient of 150kW/m^{2}K representative of single phase water cooling in high aspect ratio manifold microchannels was applied to the top of the substrate and to the hot side of the TEC [82]. Additionally, electrical current was supplied to the thermoelectric device in order to produce the thermoelectric cooling. The silicon substrate and micro-contact were assumed to have a thermal conductivity of 140W/m-K and were electrically insulated from the thermoelectric module by the ceramic header.

The die was assumed to be 10mm x 10mm, and the thickness was varied from 50µm to 400µm. Similarly, the micro-contact was assumed to be 100um tall, and its footprint was parametrically varied from 50µm x 50µm to 1500µm x 1500µm. The numerical model was created using Solid226 thermal-electrical-mechanical elements, which calculated the full 3D temperature distribution in the model by simultaneously solving for the Peltier heating and cooling, as well as the Joule heating produced in the thermoelectric module, and then solving conduction equation.

A mesh convergence study was performed in order to ensure grid independent results, and a quarter symmetry model was adopted to reduce the computational time required to solve. During the grid independence study, the number of nodes in the quarter symmetry model was varied from 15,000 to 450,000 and the hotspot temperature was monitored. It was found that when the number of nodes was increased

from 65,000 to 450,000, the hotspot temperature changed by less than 0.15K. Thus, the 65,000 node quarter model was used for the numerical simulations and the results were assumed to be grid independent. The numerical model was used to parametrically study the effect of substrate and micro-contact geometry on hotspot cooling and the numerical simulations were validated against experimental results, as will be discussed in Section 4.7.

Figure 95 shows the change in hotspot temperature as a function of micro-contact size for substrate thickness ranging from 50μm to 300μm. As can be seen in Figure 95(a) the micro-contact concentrates the convective cooling from the hot side of the thermoelectric device, producing passive cooling and reducing the hotspot temperature even when the thermoelectric cooler is off. Passive cooling is defined as the difference between the hotspot temperature when a uniform heat transfer coefficient is applied over the whole chip and the hotspot temperature when the micro-contact structure and TEC are attached to the chip, with the thermoelectric off. It can be seen that a micro-contact footprint of 300μm x 300μm produces the maximum amount of passive cooling regardless of substrate thickness. However, it is also clear that large micro-contacts trap the hotspot and surrounding background heat fluxes, resulting in significantly elevated hotspot temperatures.

Figure 95(b) shows the change in hotspot temperature when the thermoelectric cooler is activated as a function of micro-contact cross sectional area for several different substrate thicknesses. It is clear that active hotspot cooling generally increases with micro-contact footprint, due to the reduced thermal resistance from the larger cross sectional area. However, there are dimensioning returns, and after a micro-contact size

of approximately 800µm x 800µm, only small increases or decreases in active cooling occur with increasing mini-contact size. Figure 95(c) shows the total change in hotspot temperature (sum of passive and active) as a function of mini-contact size. The total hotspot cooling is also sometimes referred to as 'hotspot cooling effectiveness', as it conveys the change in hotspot temperature relative to the condition of uniform convection with no hotspot cooling. It can be seen that for the two thinner dies, a 300µm x 300µm micro-contact produces the maximum amount of hotspot cooling but for the two thicker dies, the optimum micro-contact size increases to 500µm x 500µm.

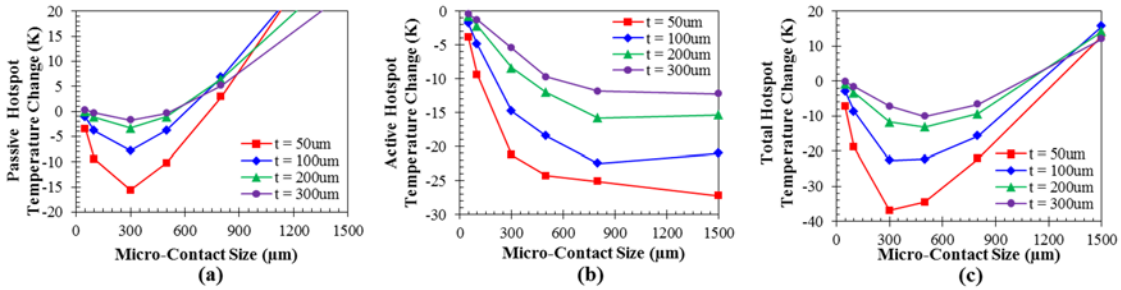


Figure 95. (a) Passive hotspot temperature change, (b) active hotspot temperature change, and (c) total hotspot temperature change produced by micro-contact enhanced thermoelectric cooling as a function of micro-contact size for a background and hotspot heat flux of 500W/cm^2 and 3kW/cm^2, respectively.

It is also important to note that there is an optimum substrate thickness, which balances the thermal spreading and through-thickness resistance in the substrate, minimizing hotspot temperature. Figure 96 shows the hotspot temperature as a function of substrate thickness when a uniform convective heat transfer coefficient is applied to the top of the substrate and it can be seen that thickness of 100µm to 200µm result in lower hotspot temperatures before any hotspot cooling techniques are even used. In addition to hotspot cooling, it is important to also consider the hotspot temperature rise, or the difference between the hotspot temperature and the temperature at the edge of

the chip, far from the hotspot, as this indicates how well the thermoelectric hotspot cooling has improved the temperature uniformity of the chip.

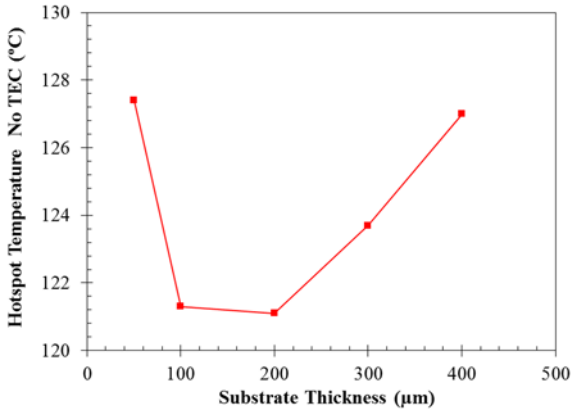


Figure 96. Dependence of hotspot temperature on substrate thickness when uniform convective cooling is applied for a background and hotspot heat flux of 500W/cm^2 and 3kW/cm^2, respectively.

Figure 97(a) shows the hotspot temperature rise as a function of micro-contact size when the TEC is off and on. It is clear that activating the thermoelectric module generally reduces the hotspot temperature rise, improving the temperature uniformity of the chip. Additionally, there is an optimum micro-contact size, which minimizes the hotspot temperature rise. Similar to the hotspot cooling case, the two thinner substrates have an optimum micro-contact size of 300µm x 300µm, while the two thicker substrates have an optimal micro-contact size of 500µm x 500µm. It is also clear that the hotspot temperature rise can be completely removed in the 50µm and 100µm thick substrates. As was previously discussed, larger micro-contacts do not sufficiently concentrate the thermoelectric cooling and trap the hotspot heat flux, resulting in larger hotspot temperature rises.

Finally, Figure 97(b) shows the hotspot temperature rise as a function of substrate thickness for the 300µm x 300µm micro-contact, with and without

thermoelectric cooling. It is clear that for substrate thicknesses of 100µm or less, the hotspot temperature rise resulting from the 3kW/cm^2 hotspot can be completely removed. As the substrate thickness increases, the micro-contact is farther from the hotspot, resulting in more thermal spreading, and reducing the ability of the system to remove the hotspot temperature rise.

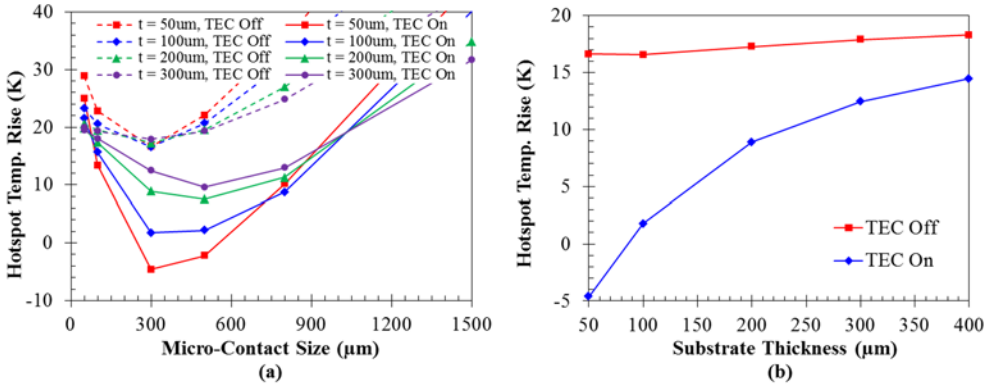


Figure 97. (a) Hotspot temperature rise as a function of micro-contact size for a variety of substrate thickness, with and without hotspot cooling, and (b) hotspot temperature rise with a 300µm x 300µm micro-contact, with and without thermoelectric cooling as a function of substrate thickness for a background and hotspot heat flux of 500W/cm^2 and 3kW/cm^2, respectively.

4.5.2 Hotspot Cooling on SiC Substrates

The numerical model was extended to predict hotspot cooling in silicon carbide substrates and in accordance with the ICECool metrics, the background and hotspot heat fluxes were increased to 1kW/cm^2 and 5kW/cm^2, respectively. Additionally, it was assumed that background cooling was provided by two phase water in manifold microchannels, so a base effective heat transfer coefficient of 364,000 W/m^2-K, with a saturation temperature of 100ºC was applied to the top of the chip and to the hot side of the thermoelectric cooler [82], [83].

In order to ensure accurate hotspot temperature predictions, a temperature dependent SiC thermal conductivity was implemented in the model, based on published values, as shown in Figure 98. Both references are for 6H single-crystal silicon carbide, however it can be seen there is variation between the two references, which produced a difference in hotspot temperature that was generally in the range of approximately 5K. In order to be conservative, the lower conductivity values, published by Burgemeister, were used for the SiC micro-contact enhanced hotspot cooling model.

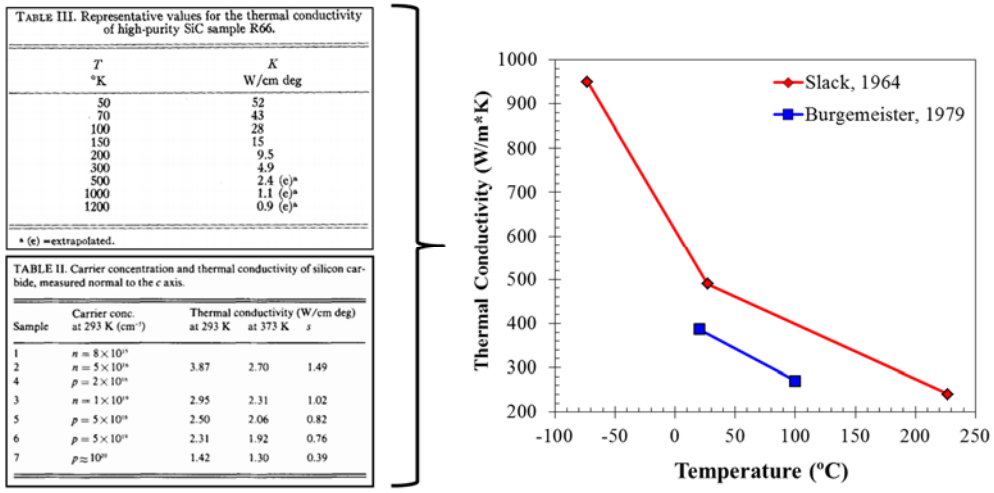


TABLE III. Representative values for the thermal conductivity of high-purity SiC sample R66.

T °K	K W/cm deg
50	52
70	43
100	28
150	15
200	9.5
300	4.9
500	2.4 (e)*
1000	1.1 (e)*
1200	0.9 (e)*

* (e) =extrapolated.

TABLE II. Carrier concentration and thermal conductivity of silicon carbide, measured normal to the *c* axis.

Sample	Carrier conc. at 293 K (cm^{-3})	Thermal conductivity (W/cm deg) at 293 K	at 373 K	s
1	$n = 8\times10^{18}$			
2	$n = 5\times10^{18}$	3.87	2.70	1.49
4	$p = 2\times10^{18}$			
3	$n = 1\times10^{18}$	2.95	2.31	1.02
5	$p = 5\times10^{18}$	2.50	2.06	0.82
6	$p = 5\times10^{19}$	2.31	1.92	0.76
7	$p \approx 10^{20}$	1.42	1.30	0.39

Figure 98. Published values for thermal conductivity of single crystal 6H silicon carbide as a function of temperature [84], [85].

The same 10mm x 10mm die and 100µm tall micro-contact, used in the silicon study, was assumed and the die thickness and mini-contact footprint were parametrically varied. Similar trends to the silicon case were observed, and it was found that the hotspot temperature rise, resulting from the much higher 5kW/cm^2 hotspot heat flux, could be reduced to less than 5K for substrate thickness below 100µm. Figure 99(a) shows the passive change in hotspot temperature, resulting from the concentration of the two-phase cooling on the hot side of the thermoelectric module

being concentrated by the micro-contact structure when the thermoelectric module is off. It can be seen that there is an optimum micro-contact size, which maximizes the passive cooling, and the effect is more pronounced on thinner substrates.

Figure 99(b) shows the change in hotspot temperature when the thermoelectric device is switched on and it can be seen that larger micro-contact sizes have smaller thermal resistances, resulting in more active cooling at larger micro-contact sizes. Finally, Figure 99(c) shows the total change in hotspot temperature, as a function of micro-contact size. As previously mentioned, the total change in hotspot temperature is commonly referred to as 'hotspot cooling effectiveness', as it conveys the change in hotspot temperature relative to the condition of uniform convection with no hotspot cooling.

Small micro-contact sizes concentrate the cooling down to a small area and only block convective heat transfer in a small area around the hotspot, but have a large conductive thermal resistance due to their small cross section. Conversely, larger micro-contacts block convection in broader area, insulting the hotspot, but also have a reduced conductive thermal resistance due to their increased cross sectional area. Thus, the optimum micro-contact size, which maximizes hotspot cooling, is determined by a balance of these two competing effects. In the parametric space studied, it can be seen that 300μm x 300μm micro-contacts can reduce the hotspot temperature by up to 25K. Additionally, it can be seen that due to silicon carbide's higher thermal conductivity the thermoelectric cooling spreads as it conducts through the die, and only minimal hotspot cooling can be achieved at die thickness over 100μm.

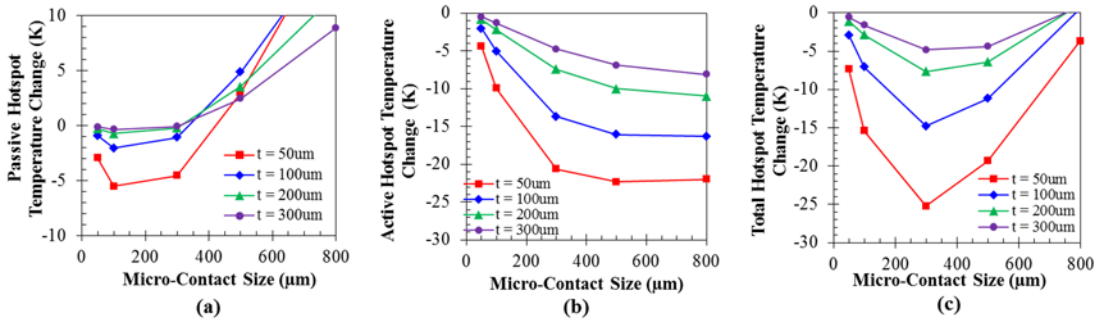


Figure 99. (a) Passive hotspot temperature change, (b) active hotspot temperature change, and (c) total hotspot temperature change produced by micro-contact enhanced thermoelectric cooling as a function of micro-contact size for a background and hotspot heat flux of 1kW/cm^2 and 5kW/cm^2, respectively.

Even when no micro-contact or thermoelectric cooler is employed for hotspot cooling, there is an optimum die thickness that balances lateral heat spreading and thermal resistance through the die. Figure 100 shows the hotspot temperature as a function of substrate thickness when the bulk evaporative heat transfer coefficient is applied uniformly across the whole top surface of the die, and it can be seen that a die thickness of 100μm minimizes the hotspot temperature. At die thickness less than 100μm, the thermal resistance for lateral spreading of the hotspot heat flux is high, driving up the hotspot temperature. Conversely, when the die is thicker than 100μm, the lateral spreading resistance is low, but the resistance through the substrate is large.

As previously discussed, while the absolute temperature of the hotspot is important to consider, the hotspot temperature rise, defined as the hotspot temperature relative to the temperature of the edge of the chip far from the hotspot, indicates how well the micro-contact enhanced cooling has improved the temperature uniformity of the chip. Figure 101(a) shows the hotspot temperature rise as a function of micro-contact size for a variety of substrate thickness, with and without thermoelectric cooling. It can be seen that thinner dies have increased lateral thermal spreading

resistance, resulting in larger hotspot temperature rises when no thermoelectric cooling is applied. However, thinner dies also result in more thermoelectric cooling being concentrated onto the hotspot, and it can be seen that for substrate thicknesses below 100µm, the temperature rise of the 5kW/cm^2 hotspot can be reduced to less than 5K.

Similarly Figure 101(b) shows the hotspot temperature rise as a function of substrate thickness with and without thermoelectric cooling, when the micro-contact size is held constant at 300µm x 300µm. It can be seen that the hotspot temperature rise can be reduced to less than 5K if the substrate is less than 100µm thick and that the effectiveness of the micro-contact enhanced cooling decreases as the substrate thickness increases.

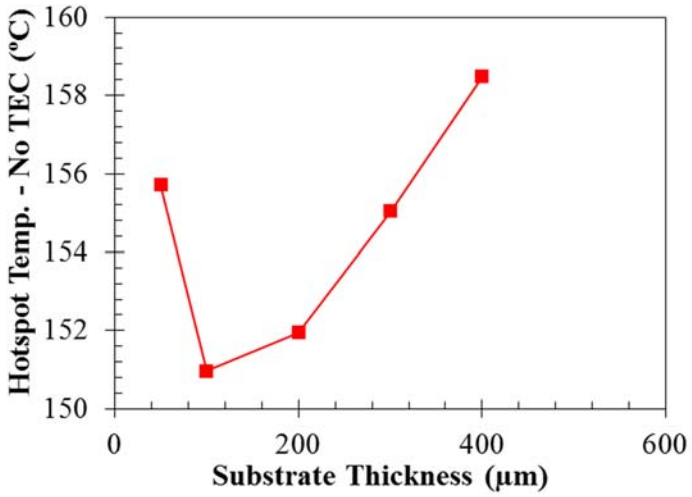


Figure 100. Dependence of hotspot temperature on SiC substrate thickness when uniform convective cooling is applied for a background and hotspot heat flux of 1kW/cm^2 and 5kW/cm^2, respectively.

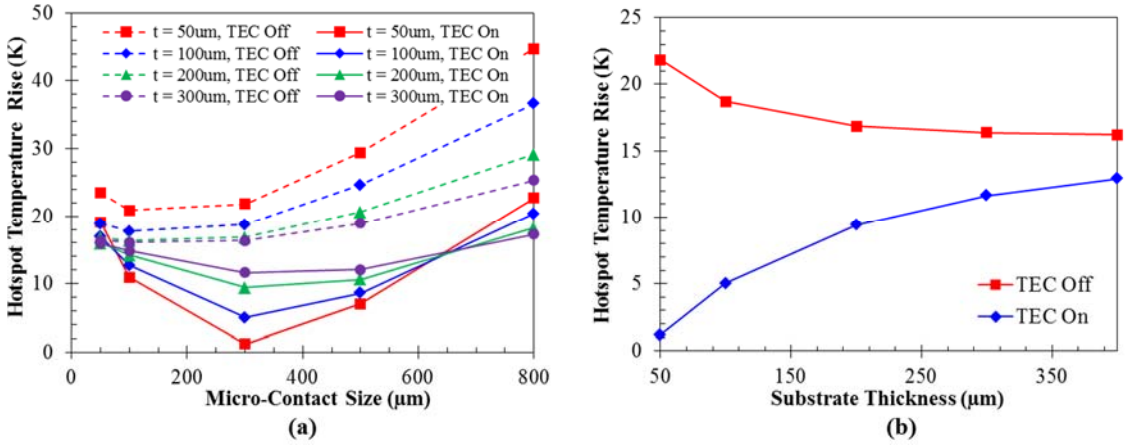


Figure 101. (a) Hotspot temperature rise as a function of micro-contact size for a variety of substrate thickness, with and without hotspot cooling, and (b) hotspot temperature rise with a 300μm x 300μm micro-contact, with an without thermoelectric cooling as a function of substrate thickness for a background and hotspot heat flux of 1kW/cm^2 and 5kW/cm^2, respectively.

4.5.3 Interaction with Convective Environment

As previously discussed and shown in Figure 87 and Figure 91, the micro-contact configuration is integrated into a bulk cooling system, such that a background and hotspot heat flux could be simultaneously removed. Figure 102 shows a more detailed schematic of how two different thermoelectric modules could be integrated into a manifold microchannel cooling system, which consists of an array of microchannels etched directly out of the die and a manifold, which delivers fluid to the microchannels vertically from above. In the figure, the die with the microchannels etched out is shown in brown, while the manifolds are shown in grey. The manifolds have alternating fluid feeds and vapor outlets. Fluid is supplied from the side of the manifold, flows through the fluid feeds, is delivered to the microchannel from above, evaporates, and exits through an adjacent vapor outlet. As can be seen, the thermoelectric device is attached to a micro-contact pillar at the center of the chip to cool a hotspot, and fluid is delivered to the microchannels in the footprint of the

thermoelectric cooler via the manifold system. An additional fluid feed can be etched into the manifold system in order to provide liquid cooling to the hot side of the thermoelectric cooler.

Figure 102(a) shows the integration of a compact, high cooling flux thermoelectric module (red blocks) into the manifold microchannel system. It can be seen that one fluid feed needs to be decreased in height in order to fit underneath the thermoelectric cooler and deliver fluid to the microchannels below. The fluid enters the microchannels beneath the thermoelectric module, evaporates, and exits through the adjacent vapor outlet. It is important to note that the hotspot generated vapor does not need to flow any farther than vapor generated by the background heat flux and flowing elsewhere in the manifold. It may, thus, be expected that the evaporative and convective cooling rates would be comparable to that on the broader, uniformly-heated areas of the chip. As the fluid is fed from the periphery of the chip, the fluid velocity is very low at the center of the chip and it is not anticipated that the reduced flow cross section will result in a large pressure drop.

Figure 102(b) shows the integration of a larger, lower cooling flux thermoelectric device (red blocks) into the manifold microchannel system. The overall integration is similar, except that due to the larger size of the thermoelectric module, the vapor needs to flow twice as far to reach an outlet after evaporation. The increased distance for vapor flow could result in higher pressure drops or reduced evaporative cooling in the area underneath the thermoelectric device. Therefore, it is clear that compact thermoelectric coolers, with large cooling fluxes, are required in order to provide sufficient cooling power to remove the hotspot temperature rise in a footprint

that is small enough to not interfere with evaporative cooling of the uniformly heated areas of the chip.

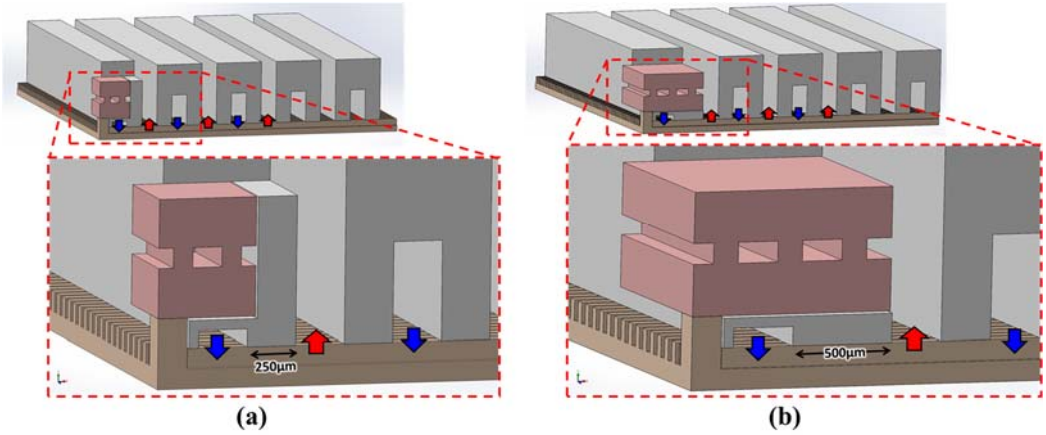


Figure 102. Integration of two different sized thermoelectric devices into a manifold microchannel cooling system. Smaller thermoelectric footprints reduce interference with the global evaporative cooling.

In order to demonstrate the importance of compact, high cooling flux thermoelectric devices for hotspot cooling, a numerical study was conducted on the effect of reduced convection in thermoelectric device's shadow. As can be seen from the schematic in Figure 103, fluid is fed to the microchannels underneath the thermeoelctric device to remove the background heat flux near the hotspot. Two different situations were studied, one in which the evaporative heat transfer was uniformly reduced in the area under the thermoelectric module and one where flow did not penetrate the full distance under the thermoelectric device, resulting in dry fins, with no evaporative or convective heat transfer, in the area immediately surrounding the micro-contact.

As indicated in the figure, a flow penetration of 0% means that no fluid is provided under the thermoelectric cooler, resulting in a heat transfer coefficient of zero

over the full thermoelectric device's shadow. Conversely, a flow penetration of 100% means that fluid reaches all of the microfins under the thermoelectric cooler, resulting in evaporative heat transfer everywhere in the thermoelectric cooler's footprint. Figure 103 shows the hotspot temperature rise, which is defined as the difference between the hotspot temperature and the temperature at the edge of the chip far from the hotspot, as a function of flow penetration or heat transfer coefficient in the thermoelectric module's shadow. The solid lines show the hotspot temperature rise when the flow penetration is varied and the dashed lines show the hotspot temperature rise when the evaporative heat transfer coefficient in the shadow is changed.

Poor flow penetration results in no evaporative or convective heat transfer in the area of the chip immediately surrounding the hotspot, and thus more severely increases the hotspot temperature rise. Similarly, larger thermoelectric devices have a larger footprint area and, therefore, cause larger hotspot temperature rises. Consequently, it is clear that compact thermoelectric modules with high cooling fluxes are required for most effective hotspot cooling, with minimal negative impact on the bulk cooling system.

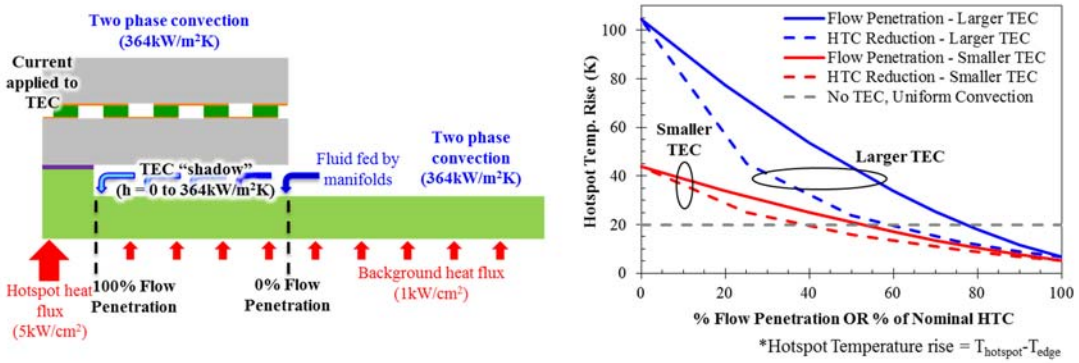


Figure 103. Effect of reduced evaporation in the thermoelectric cooler's shadow on hotspot temperature.

4.6 Optimization of TE Coolers for Maximum Cooling Flux

As previously discussed, thin film thermoelectric devices suitable for use in high heat flux cooling applications since they typically produce larger cooling fluxes than bulk devices. It was shown that successful integration of thermoelectric hotspot cooling into a bulk cooling system requires compact modules with small footprints, capable of producing large cooling fluxes. Therefore, two thermoelectric modules, a Laird HV37 and an experimental superlattice thin film thermoelectric couple produced at the Research Triangle Institute were studied to determine potential enhances in heat pumping capacity.

4.6.1 Element Packing Fraction in a Laird HV37 TEC

The effect of packing fraction on thermal performance was studied for the Laird HV37 thin film thermoelectric cooler using a numerical model similar to the one previously discussed and shown in Figure 92. The N and P type bismuth telluride elements in the module were assumed to have Seebeck coefficients of -220×10^{-6}V/K and 220×10^{-6}V/K, respectively, and all other materials were assumed to have a Seebeck coefficient of 0V/K. The ceramic headers were assumed to be electrical insulators and have thermal conductivity of 250W/m-K, comparable to that of aluminum nitride. The copper, solder, and bismuth telluride thermoelectric elements were assumed to have electrical resistivity and thermal conductivity of $1.7 \times 10^{-8}\Omega$-m, $1.3 \times 10^{-7}\Omega$-m, and $1.0 \times 10^{-5}\Omega$-m, and 400W/m-K, 65W/m-K, and 1W/m-K, respectively.

Packing fraction is the ratio of active thermoelectric area to the full footprint of the thermoelectric module. Increasing the packing fraction means that thermoelectric

elements are packed more densely into the thermoelectric device and results in larger maximum cooling fluxes. The maximum packing fraction that can be practically achieved is less generally less than 50%, and is limited by manufacturing constraints. Therefore, packing fraction was parametrically studied to determine the potential gains in thermal performance that could be achieved.

The packing fraction was incrementally increased from 40% to 60% by decreasing the spacing between individual thermoelectric elements in the module and the thermal performance of each new geometry was characterized. Figure 104(a) shows the cold side temperature as a function of as a function of applied current, and it can be seen that increasing the packing fraction has a minimal impact on the maxim achievable device ΔT. However, Figure 104(b) shows ΔT as a function of device heat pumping, and it can be seen that increasing the packing fraction from 40% to 60% double the maximum achievable cooling flux.

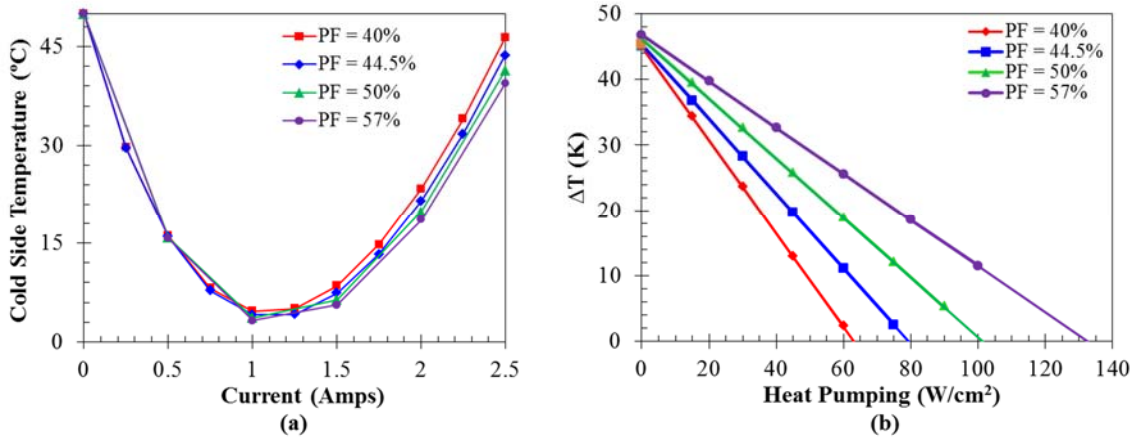


Figure 104. (a) Cold side temperature as a function of applied current and (b) device ΔT as a function of heat pumping for four different packing fractions.

4.6.2 Optimization of a Superlattice Thin Film Thermoelectric Couple

While the HV37 is considered a thin film thermoelectric cooler, experimental coolers have been produced with even thinner thermoelectric elements, resulting in greater cooling fluxes. As the thermal electric element thickness is reduced, the thermal performance becomes limited by parasitic thermal and electrical contact resistances. Therefore, in order to explore the potential improvements in thermal performance from reductions in electrical and thermal contact resistance, an experimental thin film super lattice (TFSL) thermoelectric cooler produced at the Research Triangle Institute was created in the commercial software package ANSYS.

As shown in Figure 105, the model consists of a TE couple composed of SLTF thermoelectric elements and various metallic layers and Figure 105(b) shows the 3D model and the boundary conditions used, which consisted of a fixed temperature on the hot side of the device and application of electrical current to the copper traces. The model was constructed out of Solid226, three dimensional, thermal-electric elements and consisted of approximately 20,000 nodes. Additionally, electrical and thermal interface resistance was incorporated into the model at the metal to TE element interfaces using two-dimensional contact elements, rather than the previously used three dimensional interface volumes. Additional material properties used in the model can be found in Table V. Initially, a procedure similar to that described in Section 4.4 was used to tune the numerical model to match performance curves that were obtained experimentally at RTI and University of Maryland.

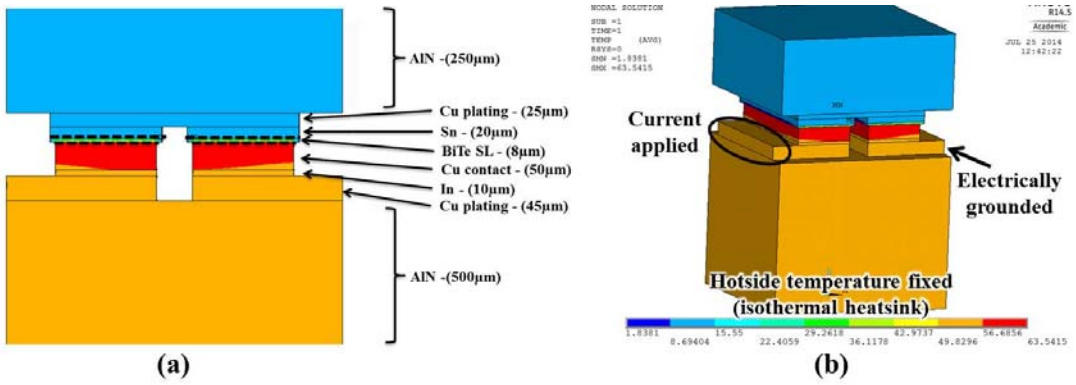


Figure 105. Three dimensional, thermal-electrical model used to study thermal and electrical contact resistances.

Table V. Thermal and electrical properties used for the various materials in the numerical model.

Material	k (W/m-K)	ρ (Ω-m)	S (µV/K)
AlN Header	250	Insulator	0
n-type SL	1.1	10×10^{-6}	-300
p-type SL	1.1	8×10^{-5}	300
Copper	400	1.7e-8	0
Tin (50% voids)	33.5 (0.5 x 67)	22×10^{-8} (2 x 11e-8)	0
Indium	82	8×10^{-8}	0

After several iterations, electrical and thermal contact resistances of 1×10^{-10} Ω-m^2 and 6.25×10^{-7} (m^2-K)/W, respectively, were found to yield excellent agreement between the modeled and reported performance characteristics of this RTI device. Figure 106 displays the modeled performance of the TFSL device, yielding a maximum ΔT of 40K at a current of 12 amps, representative of a RTI TFSL thermoelectric couple. The electrical and thermal contact resistances were then parametrically varied by two

orders of magnitude to determine their effect on the thermal performance of the TE device.

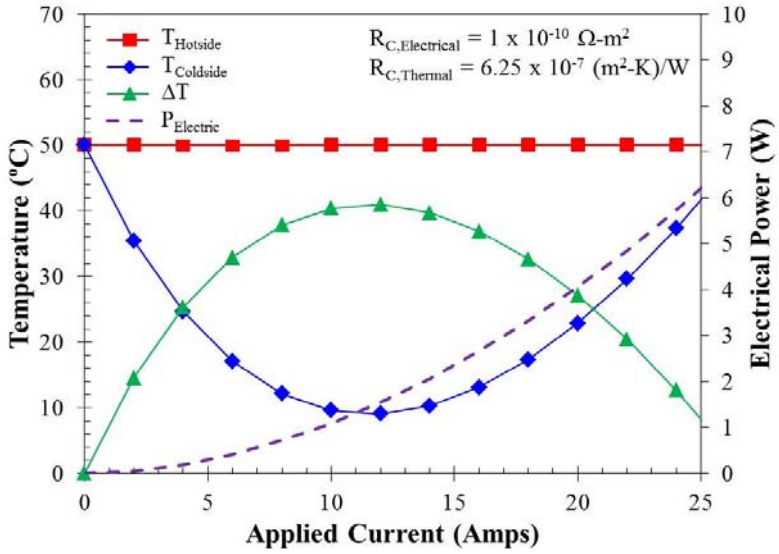


Figure 106. Device temperature difference and electrical power consumed as a function of applied current for a baseline simulation, representative of an RTI TFSL thermoelectric couple.

As shown in Figure 107, the electrical contact resistance at the thermoelectric element to metal interface was varied from 1 x 10^{-9} Ω-m^2 to 1 x 10^{-11} Ω-m^2, while the thermal contact resistance was held constant at 6.25 x 10^{-7} (m^2-K)/W. The black line with green circles Figure 107(a) shows the performance of the baseline device, representative of experimentally validated values. In can be seen that decreasing the electrical contact resistance causes an increase in optimum current, maximum device ΔT, and maximum cooling flux. Figure 107(b) shows the maximum cooling flux and ΔT, obtained at the optimum current, as a function of electrical contact resistance. From the Figure, it is clear that the thermal performance of the device can be significantly improved if lower electrical contact resistances can be obtained, and for the case of a

an electrical contact resistance of 1 x 10^{-11} Ω-m^2, a device ΔT of more than 65K and cooling fluxes greater than 500 W/cm^2 are possible.

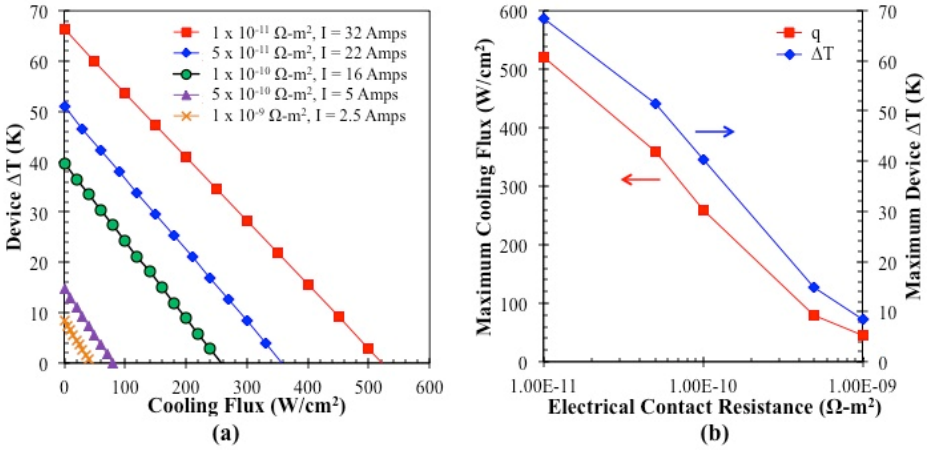


Figure 107. (a) Device ΔT as a function of cooling flux for a variety of electrical contact resistance values and (b) maximum cooling flux and maximum device ΔT as a function of electrical contact resistance.

A second study was conducted, in which the thermal contact resistance was varied from 5 x 10^{-8} (m^2-K)/W to 5 x 10^{-6} (m^2-K)/W, while the electrical contact resistance was held constant at 1 x 10^{-10} Ω-m^2. Similar to the previous case, the black line with green dots in Figure 108(a) shows the performance curve for the baseline RTI device. As can be seen in the figure, decreasing the thermal contact resistance increases the optimum current, maximum ΔT, and maximum cooling flux, however the result is less substantial than in the electrical contact resistance study. It is also clear that there are diminishing returns, and after a thermal contact resistance of 1 x 10^{-7} (m^2-K)/W is reached there is only a very small improvement in performance if the thermal contact resistance is reduced further.

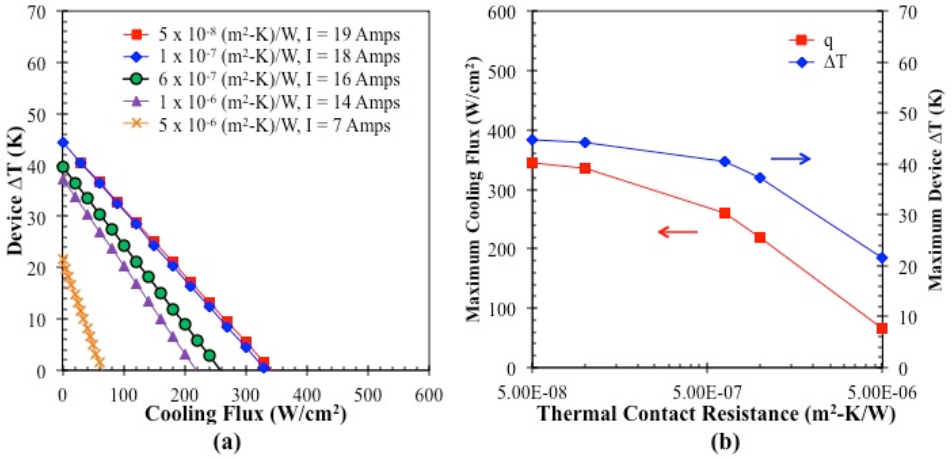


Figure 108. (a) Device ΔT as a function of cooling flux for a variety of thermal contact resistance values and (b) maximum cooling flux and maximum device ΔT as a function of thermal contact resistance.

A final study was conducted on the tin metallization, which connects the TFSL TE elements to the copper traces on the cold side of the device. Due to the manufacturing process, there was the potential for voiding in the tin and a conservative value of 50% voids was used in many previous calculations. Therefore, the effect of voiding in the tin on thermal performance was studied and Figure 109 (a) shows the device ΔT as a function of cooling flux for range of void percentages, while Figure 109(b) show the maximum ΔT and maximum cooling flux as a function of void percentage in the tin. Interestingly, the results suggest that voiding in the tin layer has only a minor impact on the performance of the device, and in fact, the tin void percentage needs to be greater than 75% to significantly degrade the maximum ΔT or maximum cooling flux.

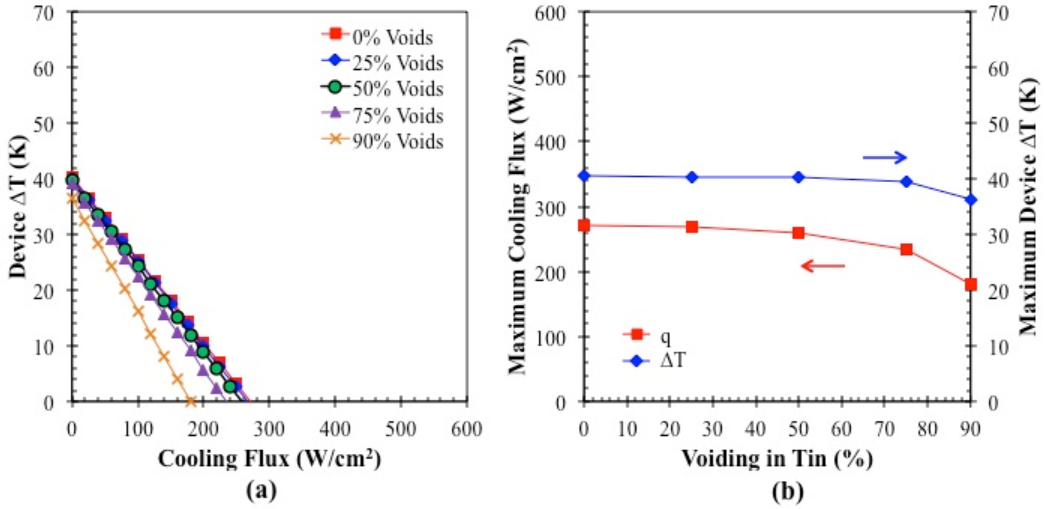


Figure 109. (a) Device ΔT as a function of cooling flux for a variety of tin void percentages and (b) maximum cooling flux and maximum device ΔT as a function of tin void percentage.

4.7 Experimental Integrated Micro-Contact Enhanced Cooling

4.7.1 Hotspot Cooling Using Integrated Si Mini-Contact

In addition to the numerical modeling, an experimental study of micro-contact enhanced thermoelectric hotspot cooling was also performed. Figure 110 shows a schematic of the test setup and boundary conditions used in the experiment, which consisted of a silicon test substrate with integrated micro-contact pillars and hotspot heaters/RTDs, a thermoelectric cooler, and a temperature controlled positioning stage.

The experimental plan focused on hotspot remediation only, so no background heat flux was applied, and the bulk of the wafer experienced natural convection. The experimental results from the study were used to validate a numerical model with comparable boundary conditions, consisting of the hotspot heat flux and thermoelectric cooling with no background heat dissipation. The validated numerical model was then extended to simulate the ICECool metrics by adding the background heat flux, global cooling, and temperature dependent silicon carbide thermal conductivity.

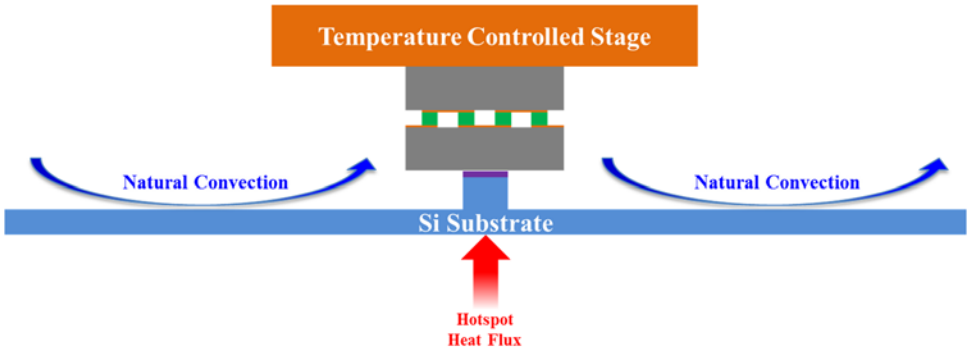
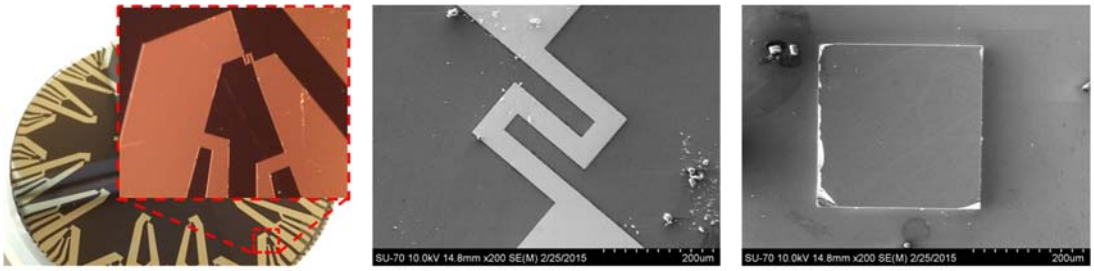


Figure 110. Schematic of the test setup used for experimental integrated micro-contact enhanced hotspot cooling.

Figure 111(a) shows an image of the silicon test wafer, taken with an optical microscope. As can be seen, the test wafer was populated with an array of platinum heaters/RTD for creation of the hotspot heat flux and measurement of the hotspot temperature. As suggested by Figure 110, a pillar was etched out of the silicon substrate on the opposite side of the wafer, centered over the heater/RTD. Figure 111(b) shows a close up of one of the heater/RTDs captured with a scanning electron microscope and Figure 111(b) shows a top-down view of a 300µm x 300µm micro-contact pillar. The silicon test wafer was 3 inches in diameter and was 350µm thick before etching of the pillars, and 40µm of the substrate was etched away to create the micro-contact pillars, resulting in a substrate thickness of 310µm and a pillar height of 40µm. The pillars all had rectangular cross sections, with footprints of 300µm x 300µm, 500µm x 500µm, and 800µm x 800µm.

As shown in Figure 112(a), the test wafer was placed in the experimental apparatus with the micro-contact pillars facing down and the platinum heaters/RTDs facing up. The hot side of the thermoelectric cooler was attached to a liquid cooled cold plate attached to a micro-position stage, such that the cold side of the TEC could be

brought into contact with a micro-contact pillar. The temperature controlled stage was capable of precise position adjustments in order to align the thermoelectric cooler and bring it into contact with the micro-contact pillar. Additionally, the stage could be leveled to ensure parallelism between the thermoelectric cooler (TEC) and test wafer.



(a) (b) (c)

Figure 111. (a) Optical microscope image of thin film heaters/RTDs, (b) SEM image close up of thin film heater/RTD, top view of a 300µm x 300µm micro-contact pillar.

A gallium-tin solder was used between the cold side of the thermoelectric module and the top of the micro-contact pillar in order to mitigate the thermal contact resistance. Figure 112(b) shows a picture of the actual experimental apparatus, and Figure 112(c) shows the Laird HV37 thin film thermoelectric module used in this experiment. The Laird HV37 is a commercially available thermoelectric module, which is capable of producing a maximum temperature reduction of 45K and a maximum cooling power of 3.7 watts [18]. In order to validate the thermal performance of the TEC before testing, a non-contact laser based characterization technique was used to confirm the maximum ΔT and heat pumping of this thermoelectric module. Additional information on the TEC characterization technique can be found in Section 5.3.

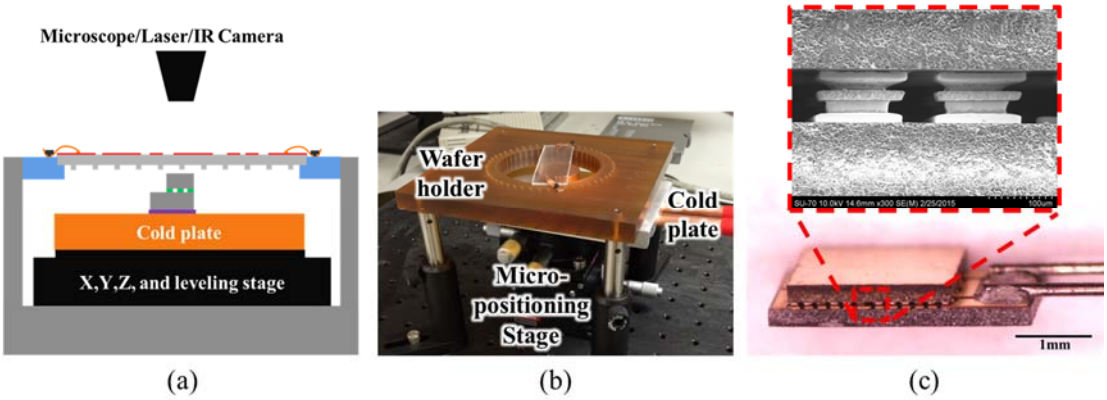


Figure 112. (a) Schematic of experimental test setup used for micro-contact enhanced thermoelectric hotspot cooling, (b) picture of actual experimental setup, and (c) optical microscope and SEM image of the Laird HV-37 TEC.

The silicon wafer was transparent in the infrared spectrum, so an infrared camera was used during the alignment process in order to ensure the thermoelectric device was centered on the micro-contact pillar. Once the thermoelectric cooler was in contact with the pillar, electrical power was supplied to the 200µm x 200µm platinum heater in order to create the hotspot heat fluxes range from 1kW/cm=to 5kW/cm^2. Electrical power was then supplied to the thermoelectric module in order to cool the hotspot, and the change in resistance of the platinum heater was monitored and used to calculate the hotspot temperature.

Additionally, the power dissipated at the hotspot, was corrected for electrical losses in the leads, and the hotspot heat flux calculated by dividing the hotspot power by the hotspot area. With the thermoelectric cooler off, the hotspot was supplied with electrical power and the hotspot power dissipation and resistance were recorded, so that the "no thermoelectric cooling" hotspot temperature could be calculated. Then, the thermoelectric cooler was supplied with electrical power, producing cooling and

lowering the resistance of the hotspot heater. The new resistance was recorded and used to calculate the hotspot "with thermoelectric cooling" temperature.

The infrared camera was used to measure the full temperature distribution in the test wafer. A graphite coating was required to make the silicon wafer visible in the infrared spectrum, which resulted in additional hotspot spreading in the area immediately surrounding the hotspot. Therefore, the infrared results were not as accurate as the RTD for measuring the hotspot temperature, but the IR did provide insight into the temperature distribution in the region of the wafer that were away from the hotspot.

The calibration of the heater/RTDs was performed in a VWR Shel Lab 1500 Incubator by measuring the resistance of the RTDs over a temperature range from 23ºC to 66ºC, in order to determine their temperature coefficient of resistance. The resistance of the RTDs was measured using a four probe method and an Agilent 34401A digital multimeter and the temperature inside the incubator was monitored using an array of five type-T thermocouples to ensure isothermal conditions. The thermocouple temperatures were measured using a National Instruments CompactDAQ system coupled with a National Instruments TB-9214 thermocouple block.

Infrared measurements were performed using a FLIR Merlin MID Infrared (IR) camera, which was connected to a computer via ThermaCAM Researcher software. The FLIR Indigo Merlin MID camera detects infrared radiation at wavelengths from 1 to 5.4μm and has a sensor resolution of 320 x 256 pixels [86]. Electrical power was

supplied to the hotspot heater and thermoelectric cooler using an Agilent 6613C DC power supply and a BK Precision XLN3640 DC power supply, respectively.

4.7.2 Silicon Experimental Results

200μm x 200μm hotspots with heat fluxes up to 3000W/cm^2 were created and cooled using the micro-contact enhanced thermoelectric configuration. Several different parameters, including the TEC input current, the pillar size, and the thermal interface between the TEC and the micro-contact were varied to determine their effect on hotspot temperature. During testing, the bulk of the test wafer was exposed to natural convection at room temperature, and the hot side of the thermoelectric device was soldered to a cold plate at 22ºC. The temperature of a 2500W/cm^2 was measured as a function of input current to the TEC, as shown in Figure 113(a). It can be seen that when no electrical power is supplied to the thermoelectric cooler, the hotspot temperature rises to 52ºC or 30K above room temperature. As current is supplied to the thermoelectric device, the hotspot temperature is reduced until the optimum thermoelectric current of 1.1 amps is reached. At the optimum current, the hotspot temperature is 32ºC, thus the net cooling of the hotspot is 20K.

In order to illustrate the importance of good thermal contact between the top of the micro-contact pillar and the cold side of the thermoelectric cooler, a round of tests were performed with no thermal interface material between the thermoelectric device and the micro-contact. In this test, a hotspot heat flux of 2850W/cm^2 was used and resulted in a hotspot temperature of 60.2ºC, with no thermoelectric cooling. When the thermoelectric cooler was activated, the hotspot temperature was reduced to 55.4ºC, a cooling of only 4.8K. Thus, it is clear that due to the small contact area at the

thermoelectric device to micro-contact interface, it is critical that good thermal contact is achieved.

Three different micro-contact pillar sizes, 500μm x 500μm, 800μm x 800μm, and 2400μm x 2400μm, were tested using the HV37 TEC with gallium-tin solder between the cold side of the thermoelectric module and the micro-contact. As can be seen in Figure 113(b), larger footprint micro-contacts result in lower hotspot temperatures when the thermoelectric cooler is off, due to passive cooling. The hot side of the thermoelectric cooler is attached to a cold plate, thus the mini-contact concentrates the cooling from the cold plate onto the hotspot, even when no electrical power is supplied to the thermoelectric device. When the thermoelectric cooler is turned on, it produces approximately 20K of hotspot cooling, with the maximum active cooling occurring at a micro-contact size of 800μm x 800μm.

The 2400μm x 2400μm micro-contact produces comparable cooling to that of the 800μm x 800μm, however as will be discussed in the next section, there was no background heating present in the experimental study, and the performance of larger micro-contacts is significantly reduced when background heating is considered. There are two main trade-offs when considering the footprint of the micro-contact pillar. A narrow micro-contact is required to concentrate the cooling down to the small hotspot area, however narrow pillars also result in a large thermal resistance, due to the small cross sectional area for conduction. Finally, if background heating is considered, narrow micro-contacts allow more space for convective bulk cooling and as will be shown in the following sections, larger micro-contacts block convective cooling, trapping the background heat flux and driving drive up the hotspot temperature.

Therefore, for a given set of boundary conditions and substrate conductivity, there exists an optimum pillar size, which maximizes hotspot cooling and results in the minimum hotspot temperature rise.

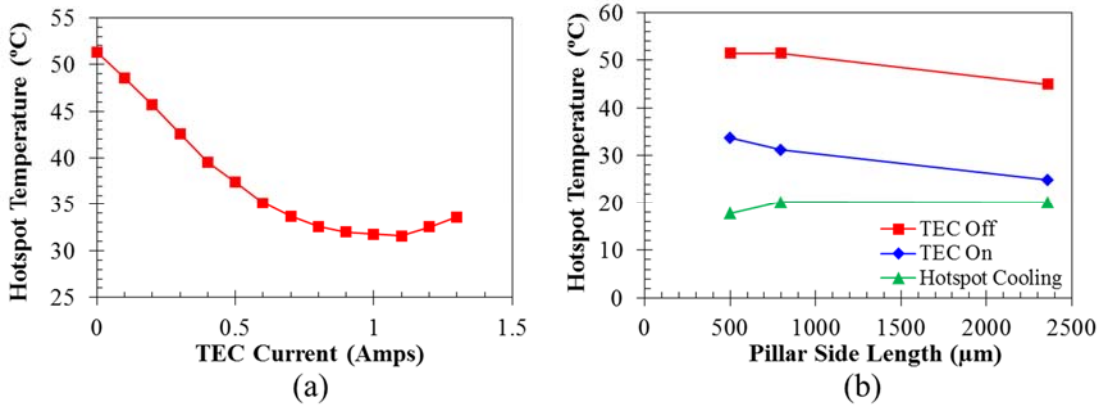


Figure 113. (a) Temperature of a 2500W/cm^2 hotspot as a function of TEC input current, (b) temperature of a 2500W/cm^2 hotspot, with and without thermoelectric cooling, for three different micro-contact footprint sizes without background heating - large micro-contacts results in elevated hotspot temperatures when background heating is considered as discussed Section 4.5.

As shown in Figure 114, an infrared camera was utilized to measure the full temperature distribution in the substrate surrounding the hotspot. Since silicon is transparent in the infrared spectrum, a graphite coating, with a thickness of ~10µm and an emissivity of 0.85, was applied to the test chip. Due to spreading in the graphite layer, the temperature distribution that the IR camera measures at the outer surface of the graphite is different than the temperature distribution on the silicon substrate around the hotspot. Therefore, in the area immediately surround the hotspot, the infrared measurements were used qualitatively, and the RTDs were relied on for the hotspot temperature measurements. Further away from the hotspot, the temperature gradients are smaller, reducing the amount of spreading in the graphite, making the infrared measurements more accurate. From the figure it is clear that the thermoelectric cooler

reduces the hotspots temperature and improves the temperature uniformity of the substrate. For the case of a heat flux of 2.5kW/cm^2 the hotspot temperature is to 52ºC, or 18K above that of the surrounding chip when no hotspot cooling is used. When the thermoelectric cooler is activated, the hotspot temperature is reduced to 31ºC, decreasing the hotspot temperature rise to less than 6K, relative to the bulk of the chip.

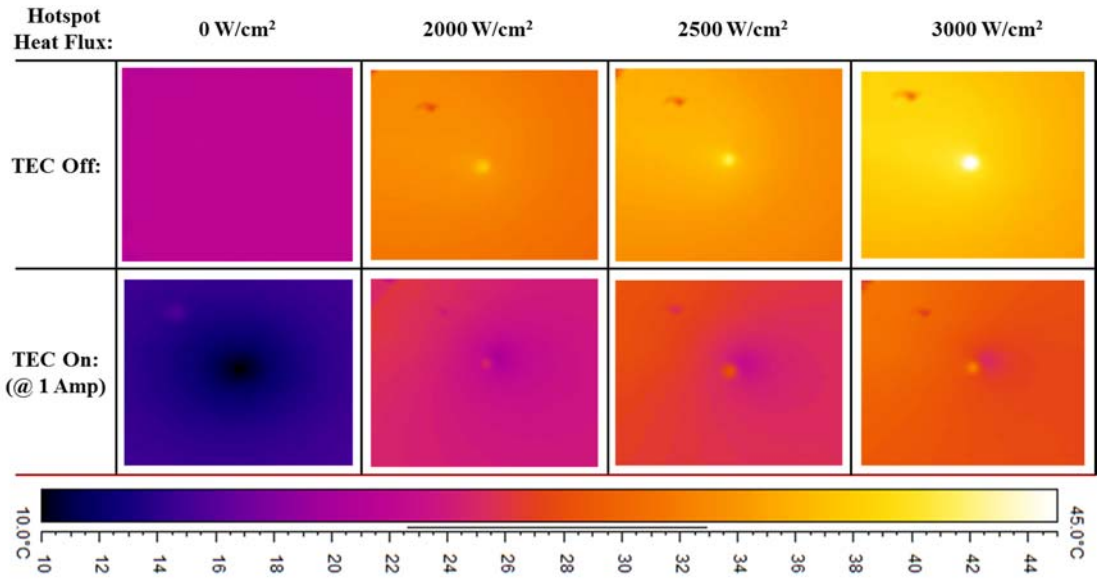


Figure 114. Temperature contours in the area around the hotspot, with and without thermoelectric cooling, for a micro-contact size of 800µm x 800µm and heat fluxes ranging from 0 to 3000W/cm^2. It can be seen that the thermoelectric cooling greatly increases temperature uniformity, reducing the hotspot temperature rise to less than 6K for the 2.5kW/cm^2 hotspot.

4.8 Comparison of Experimental and Numerical Results

The numerical predictions of thermoelectric hotspot cooling were compared against experimental results to determine the accuracy of the model. Device level thermoelectric performance was compared against manufacturer supplied data, as discussed in Section 4.4. Additionally, a numerical model consisting of the hotspot heat flux and the micro-contact enhanced thermoelectric cooling system with no background heat flux was compared with experimental results, as shown in Figure 115.

As previously indicated, The validated numerical model was then extended to simulate the ICECool metrics by adding the background heat flux, bulk cooling, and temperature dependent silicon carbide thermal conductivity.

Similar to Figure 110 and the geometries described in the experimental study, the numerical model consisted of a 200μm x 200μm hotspot at the center of a silicon substrate with a micro-contact pillar centered over the hotspot on the opposite side of the chip. A Laird HV37 thermoelectric module was attached to the top of the integrated micro-contact pillar and the hot side of the thermoelectric cooler was fixed at 22ºC, representative of the liquid cooled cold plate used in the experiment. Hotspot heat fluxes of 2kW/cm^2, 2.5kW/cm^2, and 3kW/cm^2 were applied with and without thermoelectric cooling, and the resulting temperature distributions were compared with experimental results.

Figure 115 shows the temperature distribution on the substrate for a several different hotspot heat fluxes, where the dotted and sold lines show the temperature distribution calculated in the numerical model with the thermoelectric cooler off and on, respectively. The points outlined in black indicate temperatures obtained experimentally using the hotspot RTDs and the infrared camera. There was poor thermal contact between the graphite coating required for infrared imaging and the underlying substrate, resulting in a thermal interface resistance between the substrate and the graphite. Therefore, there was a discrepancy between the temperature measured by the infrared camera on the surface of the graphite and the temperature under the coating at the surface of the test wafer, which decreased the accuracy of the infrared measurement close to the hotspot. However, far from the hotspot, where lower heat

fluxes decreased the temperature discrepancy due to the thermal interface, the accuracy of the infrared measurements was improved.

The markers outlined in black at the center of the temperature distribution in Figure 115 were measured using the hotspot RTDs, while the markers outlined in black at the periphery indicate temperature measured using the infrared camera. It can be seen that there is good agreement between the numerical and experimental results and over the range of heat fluxes tested and that the numerical predictions agree with experimental values to within +/- 1K.

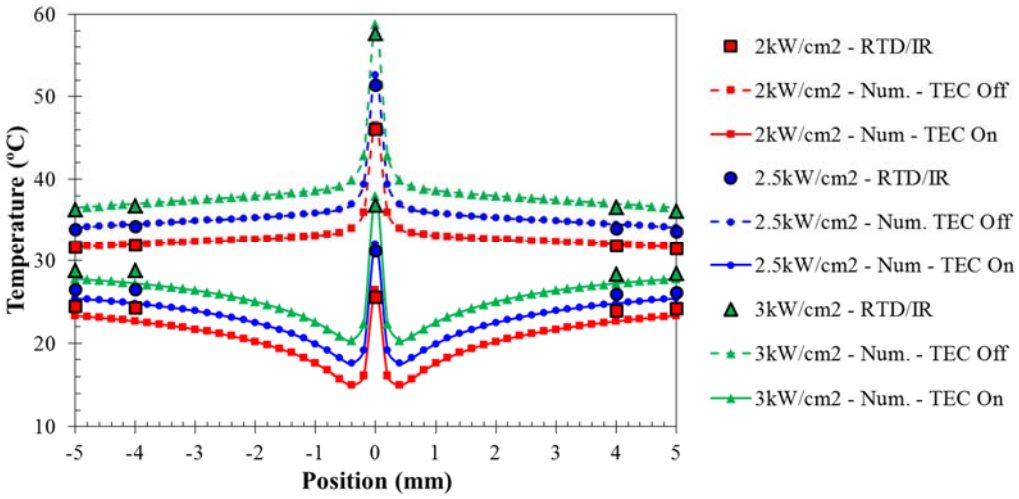


Figure 115. Numerically predicted temperature distribution compared with experimentally measured hotspot temperatures for several different hotspot heat flux levels.

4.9 Conclusions

The micro-contact enhanced thermoelectric cooling study was motivated by the DARPA ICECool Fundamentals program, which required the cooling of a GaN on SiC power chip dissipating background and hotspot heat fluxes of 1kW/cm^2 and 5kW/cm^2, respectively. A variety of discrete and integrated mini/micro-contact form factors and

materials were explored, and due to reliability, manufacturing, and thermal considerations, work was focused on the use of integrated micro-contacts for thermoelectric cooling of high heat flux hotspots.

Numerical models of commercially available thermoelectric modules were created in ANSYS and tuned to match manufacture supplied performance curves by adjusting internal thermal and electrical contact resistances. The device level numerical models were then incorporated into a system level model consisting of background and hotspot heat fluxes, bulk cooling via manifold microchannels, and an integrated micro-contact structure. The numerical results indicate that micro-contact enhanced thermoelectric cooling can significantly reduce the temperature of localized kW/cm^2 level hotspots, greatly improving the temperature uniformity and enhancing the performance and reliability of power electronic devices. However, it was also found that compact module with large cooling fluxes are required for efficient hotspot cooling with minimal impact on the bulk thermal management system.

Therefore, potential enhances to the heat pumping capacity of both a commercially available Laird HV37 and an experimental SLTF thermoelectric cooler were numerically studied. It was found that increasing the packing fraction and reducing thermal and electrical interface resistances can significantly improve the maximum achievable device level cooling flux.

Finally, micro-contact enhanced hotspot cooling of hotspot on a silicon test substrate with heat fluxes up to $5kW/cm^2$ were experimentally studied, and the results were compared with numerical predictions. The experimental study focused on hotspot

remediation, so a hotspot heat flux and thermoelectric cooling were used, but no background heat flux was applied. The experimental results showed that micro-contact enhanced thermoelectric cooling was capable of producing up to 20K of hotspot cooling and reduced the temperature rise of a 2.5kW/cm^2 hotspot to less than 6K above that of the surrounding substrate. Finally, the experimental results were compared to a numerical model with comparable boundary conditions, and good agreement was seen. Background heat flux and bulk cooling boundary conditions were added to the validated numerical model to simulate operation of a micro-contact enhanced thermoelectric cooler embedded in a comprehensive thermal management system.

5 Laser for Device Characterization and Hotspot Creation

5.1 Introduction and Motivation

A non-contact, laser based technique was developed in order to simulate high-flux hotspots on electronic chips and substrates and to facilitate the testing of novel hotspot cooling techniques, as well as to characterize miniature state of the art thermoelectric modules. Thermal test vehicles, or TTVs, are commonly used to test thermal management systems and typically have a similar geometry to an electronic chip, but contains resistive heaters and temperature measurement diodes in place of functional components. TTVs can be very useful for testing, however the initial design and fabrication of a test chip can be expensive and time consuming. Once created, it is very hard to alter the geometry of a test vehicle, restricting test parameters such as the size, location, or number of hotspots.

Therefore, the ability of a high power laser to deliver heat and produce hotspots with heat fluxes in the kW/cm^2 range was studied. While the laser and the supporting optical system did initially introduce some additional complexity, it provided a great deal of experimental flexibility, allowing for the hotspot size, location, and power dissipation to all be changed with relative ease. Additionally, it is suggested that future work will allow hotspots of different shapes and patterns to be created with the laser, to simulate operation of different power electronic devices. Additionally, the laser was used to develop a novel, non-contact method for characterizing the performance of thin film thermoelectric coolers, which is particularly well suited for testing of mini to micro sized modules. Before creating hotspots or accurately characterizing thermoelectric devices, the laser output power and spot size needed to be determined, as will be outlined.

5.2 Beam Characterization

5.2.1 Laser Power

As shown in Figure 116, the setup used to measure the laser output power consisted of a beam collimator, an adjustable pinhole aperture, a focusing lens, and a power meter. The collimator was a custom aligned Thorlabs F240SMA-780 fiber collimation package, the pinhole was a Thorlabs SM1D12SS stainless steel iris, and the focusing lens was a Thorlabs ACA254-030-B air spaced doublet, with a focal length of 30mm. The laser power was measured using a Thorlabs 322C thermal power detector, with a measurement range of 100mW to 200W, coupled with a Thorlabs PM100D digital power meter. The power detector has an absorptivity of 0.9 at a

wavelength of 810nm, which was accounted for in calculations. Additionally, the power detector has an accuracy of +/- 5% of the reading.

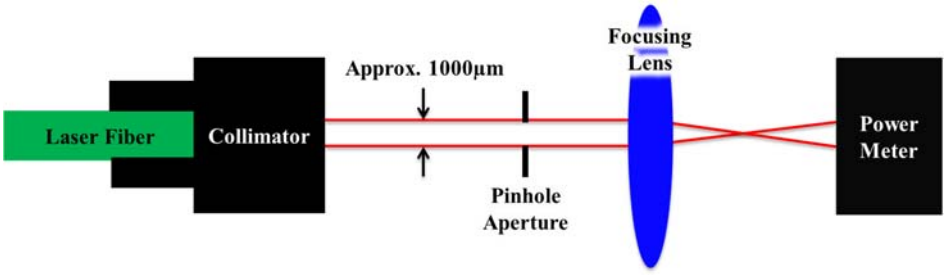


Figure 116. Schematic of the optical setup used for measuring the output power of the Coherent laser.

A power calibration curve was created for the laser by varying the input current to the laser diode and measuring the resulting laser output power incident on the power detector. A Coherent Highlight FAP 100, air cooled diode laser was used and had a central wavelength of 810nm and a maximum output power of 100 watts, which was delivered via a fiber optic cable [87]. As can be seen in Figure 117, the laser has a lasing threshold of approximately 8 amps, after which the laser output power varies linearly with diode input current. For testing of thermoelectric devices, an identical test setup is used except the power meter was replaced by the electronic substrate or cold side of the thermoelectric device. Thus, the laser power calibration setup takes into account all losses in the beam collimator, pinhole aperture, and focusing lens.

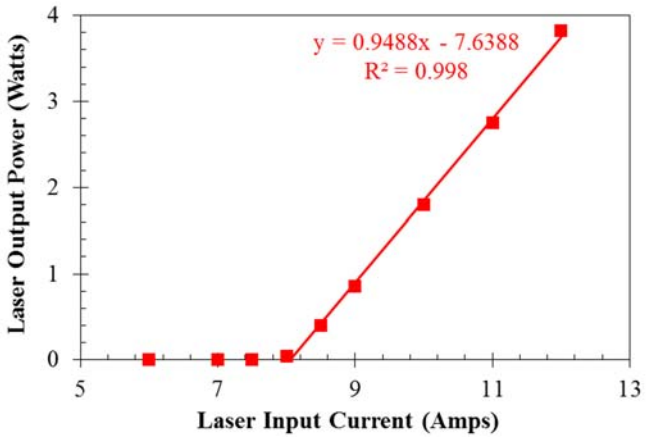


Figure 117. Calibration curve consisting of the laser output power as a function of the input diode current.

5.2.2 Laser Spot Size

In addition to the laser output power, the size of the laser spot needed to be determined in order to calculate the hotspot heat flux or to ensure that all of the laser energy was focused onto the cold side of a thermoelecric module. A razor scanning, also referred to as a knife edge, method was used to measure the laser spot size, as shown in Figure 118. It can be seen that the setup was similar to the power calibration test, except that a razor blade and micro-actuator were added between the focusing lens and the power detector. The razor blade was a standard steel utility knife blade and the micro-actuator was a Newport 462 series XYZ linear stage. The razor blade/micro-actuator system was placed the same distance from the focusing lens as the surface of the thermoelectric device, in order to ensure the laser spot size used in the device characterization was the same size as that measured using the razor scanning technique. Depending on the desired hotspot diameter or the size of the thermoelectric device to be tested, the sample could be moved closer or farther away from the laser beam's point of focus in order to achieve the desired laser spot size.

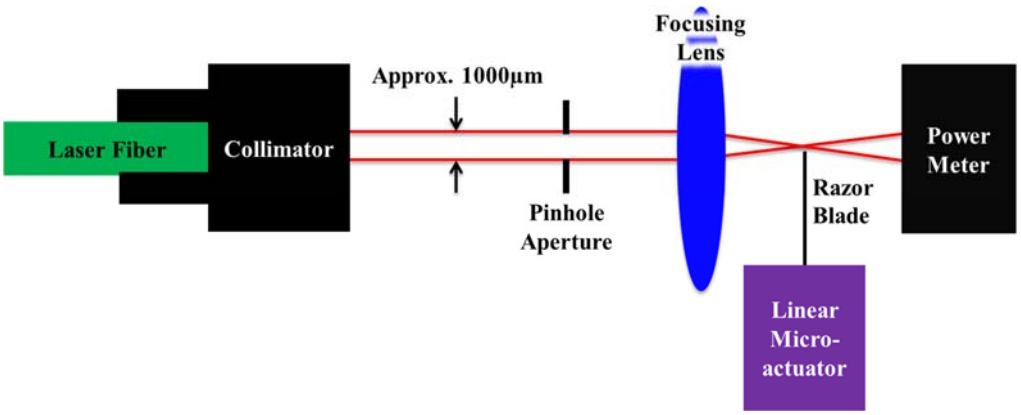


Figure 118. Schematic of the optical setup for determining the spot size of the laser near the point of focus.

With the razor blade fully out of the path of the laser beam, the laser was activated and the amount of power reaching the power meter was measured. In the example shown in Figure 119, the laser had an output power of 2.1 watts. While keeping the laser output power constant, the razor blade was stepped through the laser beam in small increments, gradually blocking an increasing portion of the laser's power from reaching the power meter. As can be seen in Figure 119(a), the razor blade was initially outside of the laser beam and the full 2.1 watts of power reached the power meter. As the razor blade was moved into the laser beam, the amount of laser power reaching the power meter decreased, and when the razor blade had moved approximately 1mm, the laser beam had been completely blocked.

The slope of the curve from Figure 119(a) can be calculated, giving the curve shown in Figure 119(b). Points where the slope are zero indicate that moving the razor blade had no change in the amount of power reaching the power meter, which means the razor blade was at the edge of the laser beam. Therefore, from Figure 119(b) it is clear that the laser spot was approximately 1mm in diameter, and had an average

intensity of 267W/cm^2. It should be noted that the vertical axis of Figure 119(b) is the change in laser power per length, not intensity of laser, which has units of power per area. The spatial intensity distribution within the laser beam, with units of W/m^2, can be calculated from the razor scanning results, and is discussed in Section 5.4.

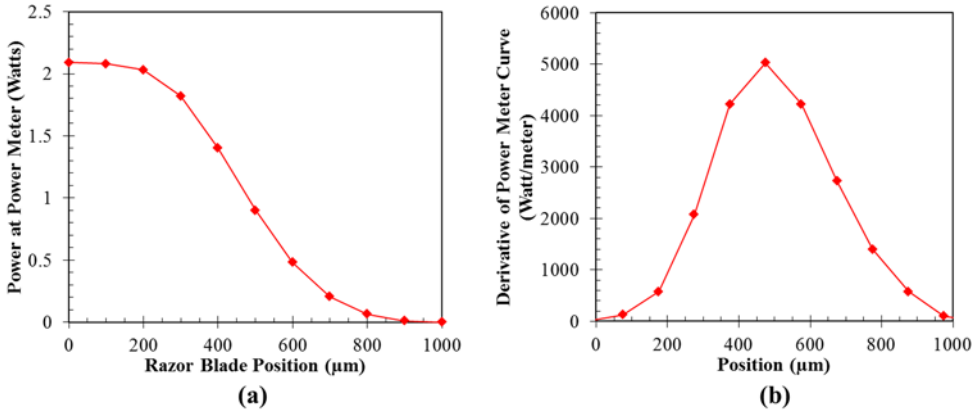


Figure 119. (a) Laser power reaching the power detector as a function of razor edge position and (b) change in power divided by change in position as a function of razor edge position.

5.3 Thermoelectric Device Characterization

As previously discussed, thermoelectric coolers have become an area of intense research for cooling of electronic packages, particularly for the removal of high heat flux hotspots, and in order to integrate TECs into electronic packages, new mini-to-micro sized devices are required [1], [2], [35], [37], [40], [45], [48], [49].

The performance of thermoelectric modules is typically characterized using two metrics: 1) The maximum temperature difference (ΔT_{max}) that the device can produce, and 2) the maximum amount of heat (Q_{max}) that the device can pump, and manufactures of thermoelectric devices must measure these performance metrics to characterize their thermoelectric devices. Conventional characterization techniques typically use

thermocouples, q-meters, and/or heat flux sensors, which all need to be brought into physical contact with the thermoelectric device, and introduce losses and measurement error into the measurement process, particularly as the device size decreases. The present effort introduces a novel, non-contact technique that is well suited for the characterization of new mini–to-micro sized thermoelectric modules.

Figure 4 and Figure 120 show representative performance curves for a thermoelectric device, which reveals that for a given current, there is a maximum temperature difference (ΔT_{max}) that can be produced, between the hot and cold side of the thermoelectric device, and a maximum cooling flux that can be pumped through the device (Q_{max}). It should be noted that for a given current, the maximum ΔT occurs at a cooling rate of zero, and, conversely, the maximum cooling rate occurs when the temperature difference is zero. Therefore, thermoelectric module manufactures must be able to measure the maximum temperature difference and the maximum cooling flux in order to characterize the performance of their modules.

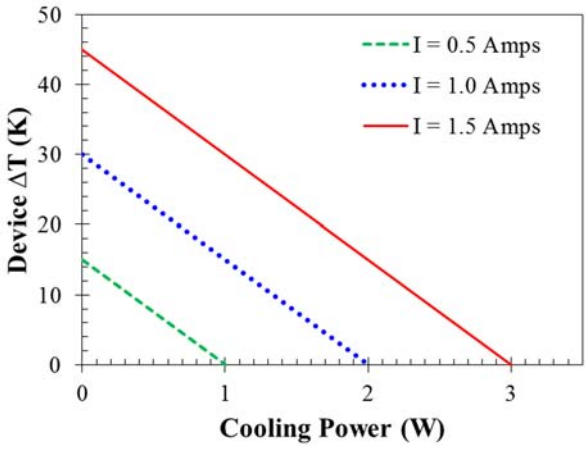


Figure 120. Typical performance curve for a thermoelectric device. For a given a given current, the maximum ΔT occurs at cooling flux of zero, while the maximum cooling flux is reached when the ΔT is zero.

5.3.1 Traditional Characterization of Thermoelectric Performance

Figure 121 shows conventional testing methodologies used for characterization of thermoelectric devices, which as previously mentioned, requires bringing thermocouples and/or q-meters into contact with the module being tested. As shown in Figure 121(a), the maximum temperature difference is typically measured by attaching thermocouples to the hot and cold side of the device and supplying electrical power to the cooler to produce a temperature difference (ΔT). For large scale devices, testing is often performed in a vacuum to minimize convection at the cold side of the device and ensure that the cooling flux is as close to zero as possible. To test the sample, the amount of electric power supplied is gradually increased until the maximum temperature difference, as measured by the thermocouples, is reached.

As shown in Figure 121(b), the heat pumping capacity of the thermoelectric device is measured using a q-meter, which is a block of material with known thermal properties and geometry. By assuming one dimensional conduction and measuring the temperature gradient in the block, heat flow can be calculated using Fourier's law. Similarly to ΔT testing, the amount of electrical power supplied to the thermoelectric device is gradually increased until the maximum heat pumping value is reached. There are a few commercially available q-meters and heat flux sensors, but since these sensors must come into contact with the sample that is being characterized, they introduce loses and error into the measurement, which must be accounted for.

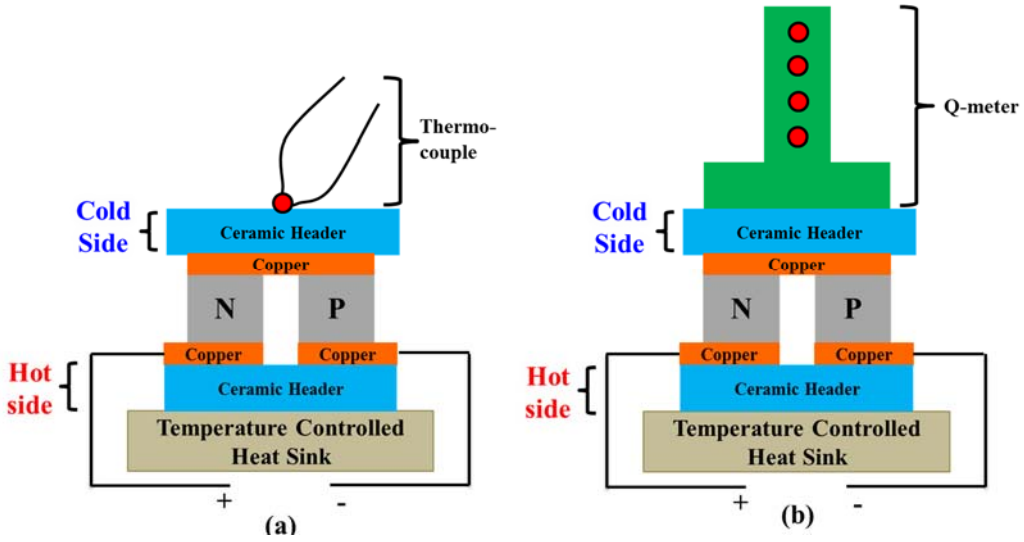


Figure 121. Conventional methods for measuring (a) maximum ΔT and (b) maximum heat pumping of thermoelectric modules.

5.3.2 Non-Contact Technique for Device Characterization

Many of the losses that degrade traditional, contact-based measurement techniques become more pronounced at small scales, thus the novel non-contact measurement technique that was developed, as part of this PhD Dissertation, is particularly well suited for mini and micro sized thermoelectric device characterization [88]. Additionally, since the sample does not need to be attached to a bulky q-meter, the non-contact approach could be automated to rapidly characterize multiple samples, greatly reducing the amount of time required for testing.

As will be described, the experimental methodology consists of techniques for measuring both the device maximum temperature difference (ΔT_{max}) and maximum heat pumping (Q_{max}). For measurement of maximum device ΔT, an infrared camera is used to measure the hot and cold side temperature of the thermoelectric device, while electrical current is supplied. For heat pumping characterization, an infrared camera is again used to measure the hot and cold side temperature of a device; however a laser is

also utilized to heat the cold side of the TEC. The thermoelectric device must pump the heat produced by the laser beam from the cold side of the module to the hot side, thus the maximum heat pumping capability of the thermoelectric device can be determined by finding the laser power that results in the cold and hot side of the module being at the same temperature ($\Delta T = 0$).

For the maximum temperature difference measurement, current is supplied to the device while an infrared camera is used to measure the temperature of the hot and cold sides of the thermoelectric device, as shown in Figure 122. As previously mentioned, thermoelectric module ΔT measurements have traditionally been performed using thermocouples. However, much like other electronic device, thermoelectric devices have become smaller and smaller over recent years. Thus, if the cold side of the thermoelectric device becomes very small, the thermal mass of the thermocouple being used for the measurement may be comparable to that of the cold side of the thermoelectric device, thus altering the measured values. Additionally, heat conduction down the thermocouple wires can change the measured temperature, giving inaccurate results. Thus, using a non-contact measurement technique is advantageous for mini to micro sized devices. In order to accurately to measure the temperature of the thermoelectric cooler, the emissivity of the surface must be considered, which is discussed in greater detail in the following section.

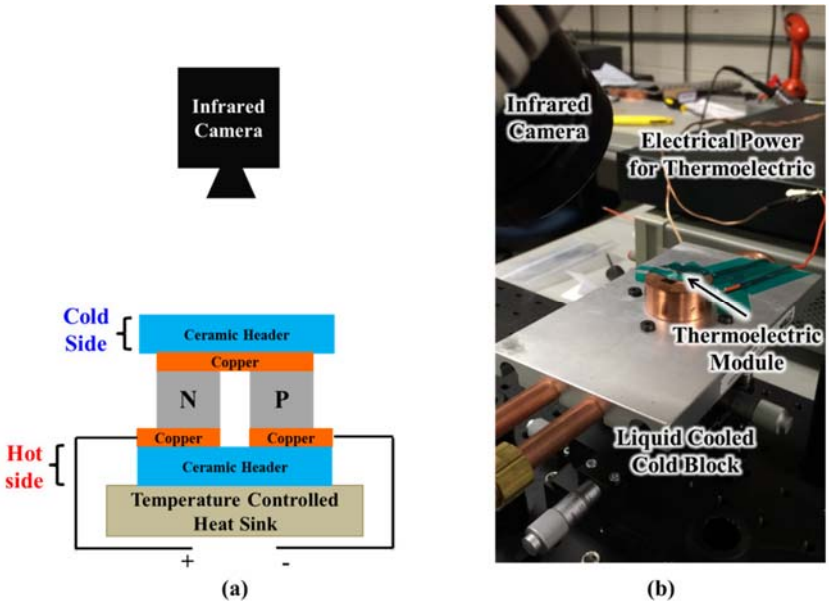


Figure 122. (a) Schematic and (b) picture of test setup used to measure maximum device ΔT, consisting of a liquid cooled heat sink, the thermoelectric module, and an infrared camera.

As shown in Figure 123, the cooling flux of the thermoelectric device is again measured using a non-contact technique, consisting of a water cooled heat sink, infrared camera, laser, and the thermoelectric module. Similar to the ΔT_{max} testing, the thermoelectric device is supplied with electrical power and an infrared camera is used to measure the temperature of hot and cold side of the device. A laser is used to heat the cold side of the TEC and the amount of laser radiation incident on the cold side of the sample is gradually increased, decreasing in the device ΔT.

Since the thermoelectric module must pump the laser heating on the cold side to the heat sink on the hot side, the amount of laser heating is equivalent to the heat pumping of the module. Eventually, the laser power is large enough that it heats the cold side to the point where the cold side and hot sides are at the same temperature. At

this point, the ΔT across the module is zero and the maximum cooling flux has been reached for that current.

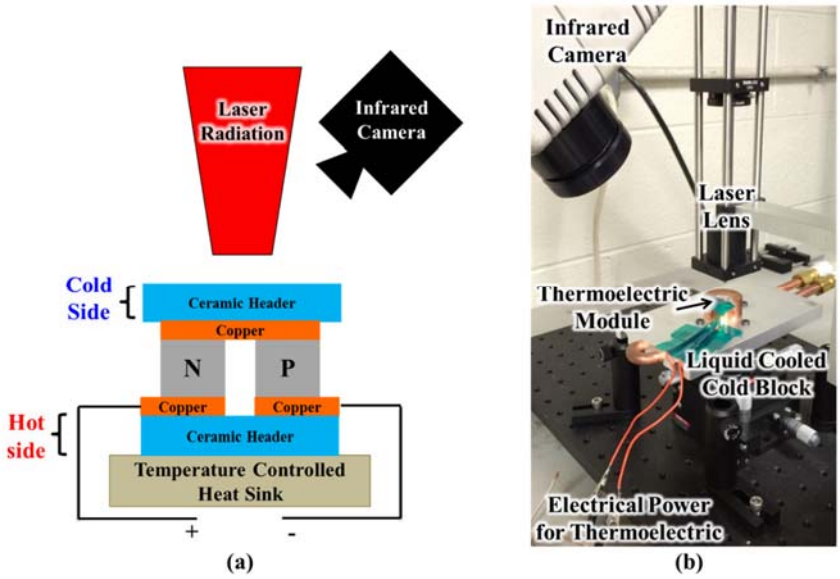


Figure 123. (a) Schematic and (b) picture of the heat pumping experimental apparatus, consisting of a liquid cooled heat sink, infrared camera, laser, and thermoelectric device.

5.3.3 Laird HV37 Thin Film Thermoelectric Cooler

The performance of a commercially available Laird HV37 thermoelectric module was characterized and the results agreed well with the manufacturer supplied data sheet [18]. The HV37, which is shown in Figure 124, is an eTEC series thin film thermoelectric module with a maximum device ΔT of 45K, at a current of 1.1 amps, and a maximum cooling power of 3.7 watts. The cold side of the thermoelectric module is metalized in order to make it easy to solder to an electronic device when integrating the cooler into a system. Metals typically have high reflectivity and low emissivity, increasing the error when taking infrared temperature measurements. Therefore, the cold side of the HV37 was coated with graphite, which provided a uniform emissivity of 0.85. Additionally, it was assumed that the absorptivity of the graphite was equal to

its emissivity, thus an absorptivity of 0.85 was assumed during the laser heat pumping characterization.

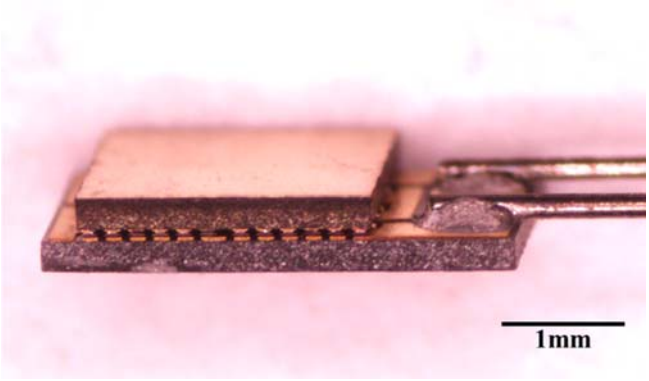


Figure 124. **Optical microscope image of a Laird HV37 thin film thermoelectric module.**

Similarly to what is shown in Figure 122 and Figure 123, the hot side of the thermoelectric cooler was attached to a temperature controlled cold plate, using a GaSn based solder, and electrical power was supplied to the thermoelectric module using a BK Precision XLN3640 DC power supply. The hot and cold side temperatures were measured using a FLIR Merlin MID Infrared (IR) camera, which was connected to a computer via ThermaCAM Researcher software. The FLIR Merlin MID camera detects infrared radiation at wavelengths from 1 to 5.4μm and has a sensor resolution of 320 x 256 pixels [86].

As shown in Figure 122, the thermoelectric module was soldered to a liquid cooled cold plate and the temperature of the hot and cold side of the device was measured using an infrared camera. As can be seen in Figure 125, the thermoelectric module was gradually supplied with current, causing the temperature of the cold side of the device to decrease and the hot side temperature to increase slightly. Due to the small size of the device, it was assumed that natural convection off of the cold side of

the TEC would be minimal and could be neglected. A maximum device level temperature difference (ΔT_{max}) of 42.3ºC was measured at a TEC current of 1.1 amps. This result agrees well with the manufacturer supplied value of ΔT_{max} of 45ºC at 1.1 amps, which was measured under vacuum, and thus it is suspected the small discrepancy is due to the small amount of heat absorbed at the cold side of the device via natural convection [18].

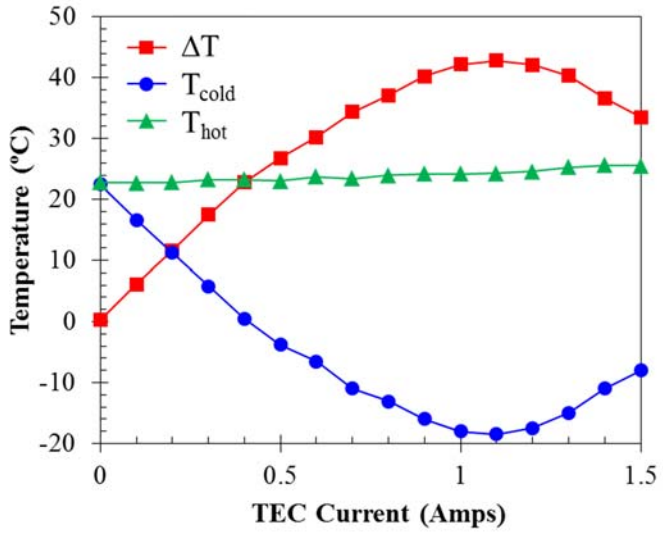


Figure 125. Cold and hot side temperature and device level temperature difference as a function of applied current for a Laird HV37 TEC.

The heat pumping capacity of the HV37 thermoelectric module was also measured and compared with manufacturer supplied values. The test setup was similar to that used in the device ΔT characterization, consisting of a liquid cooled cold plate, the HV37 module with a graphite coating on its cold side, and a DC power supply providing the TEC with electrical current. The laser system was integrated into the testing apparatus using an adjustable XYZ stage, allowing the laser spot to be precisely aligned with the cold side of the thermoelectric device. Although the wavelength of the laser was slightly different from the wavelengths detected by the infrared camera

(810nm vs 1 to 5.4μm), based on Kirchhoff's law, it was assumed that the absorptivity of the graphite at the wavelength of the laser was equal to the emissivity of the graphite measured using the infrared camera. Thus, an absorptivity of 0.85 was used when calculating the amount of laser heating being pumped through the thermoelectric module.

Characterization of the module was performed by initially supplying the thermoelectric module with electrical current, with no laser radiation, producing the maximum device level ΔT for that current. The laser radiation was then gradually supplied to the cold side of the thermoelectric cooler, producing heating and reducing the device level ΔT. Assuming minimal natural convection at the cold side of the thermoelectric device, all of the laser heating needed to pumped through the device and into the heat sink attached to the hot side of the module. Thus, the amount of laser heating is synonymous with the thermoelectric device heat pumping. Using the infrared camera, the device level ΔT was measured as a function of device heat pumping and recorded, as can be seen in Figure 126.

Two different TEC currents were tested, 0.39 amps and 1.1 amps, and the results were compared to those from the manufacturer's data sheet. As can be seen from the markers in the figure, 0.39 amps and 1.1 amps of electrical current produced maximum device ΔTs of 24K and 42K, respectively, which agrees well with the maximum ΔT characterization in the previous section. As laser heating was supplied to the cold side of the TEC, the device ΔT decreased linearly, until the maximum heat pumping value was reached at a ΔT of 0K. It can be seen that a thermoelectric current of 0.39 amps and 1.1 amps produced a maximum heat pumping of 2.0W and 3.4W,

respectively, which agree with the manufacture reported values to within 10%. The manufacture supplied performance curves are shown by dotted and dashed lines, and it can be seen that the experimental values are slightly below those from the manufacturer. It is suspected that one source of this discrepancy was that testing was done in ambient air, while the manufacture characterized their devices in a vacuum.

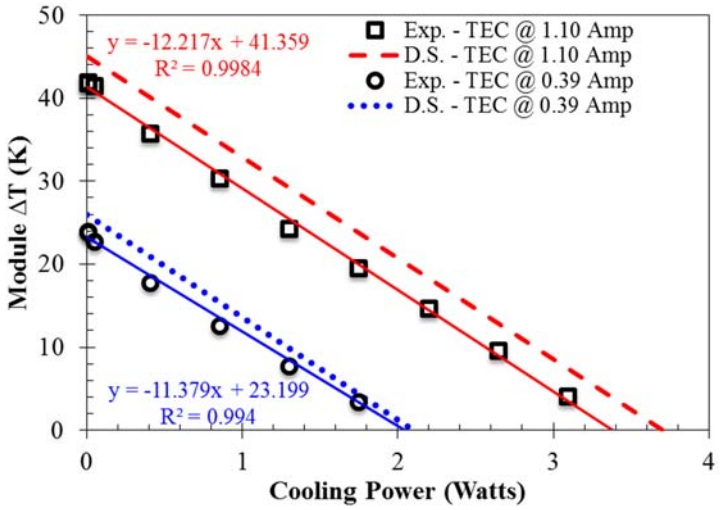


Figure 126. Module ΔT as a function of heat pumping for the Laird HV37 thermoelectric cooler at currents of 0.39 and 1.1 amps [18].

5.3.4 RTI Thin Film Superlattice Cooler

Using a similar non-contact technique, an experimental super lattice thin film thermoelectric cooler (SLTF) produced at the Research Triangle Institute was also tested. The cooler consisted of a single thermoelectric couple, with a geometry similar to that shown in Figure 105. As was the case previously, both the maximum ΔT and maximum heat pumping of device were measured. Again, due to the small size of the cold side of the module, heat transfer due to natural convection was minimal and was therefore neglected in the calculations.

To characterize the maximum ΔT of the device, current was gradually supplied to the TE couple and the temperature difference was recorded, using the infrared camera, as shown in Figure 127. It can be seen that a maximum temperature difference of 37K was reached at a current of 14 amps, which agrees well with the results obtained at RTI of a maximum ΔT of 36K at 14.3 amps.

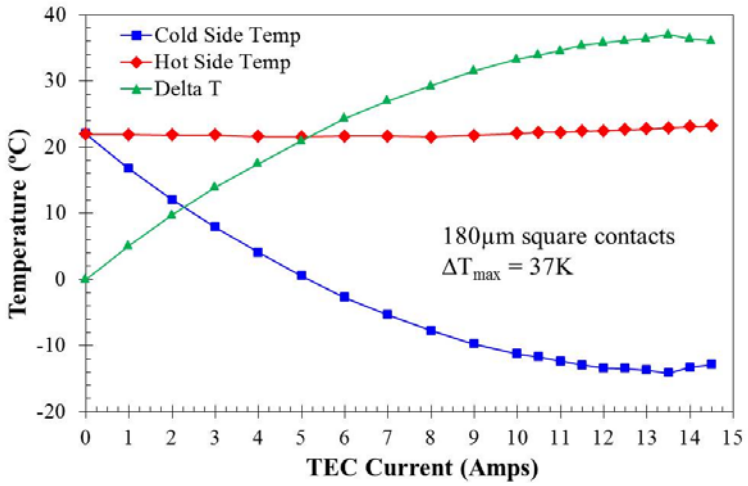


Figure 127. Hot side and cold side temperature, and device temperature difference as a function of applied current for RTI SLTF thermoelectric couple.

The non-contact, laser based method was also used to characterize the heat pumping of the TE couple by of first providing the TE couple with electrical power, thus creating a temperature difference across the device. The laser was then used to heat the cold side of the TE couple, decreasing the device level ΔT. The laser power was gradually increased until the ΔT across the device was 0K, indicating that the maximum heat pumping for that current had been reached. The process was repeated several electrical powers to determine the electrical current that produced the maximum device heat pumping.

The emissivity of the cold side of the thermoelectric device was determined using the infrared camera, and from Kirchhoff's law, the absorptivity of the cold side was assumed to be equal to the emissivity. Thus, the total amount of power being pumped through the device could be readily calculated. Figure 128 shows the heat pumping performance of a thermoelectric device, and it can be seen that a maximum heat pumping of approximately 235 W/cm^2 was reached at an electrical current of 11 amps. These results also agree well with the maximum cooling flux value of 213.7W/cm^2 at a current of 11.5 amps, obtained at RTI.

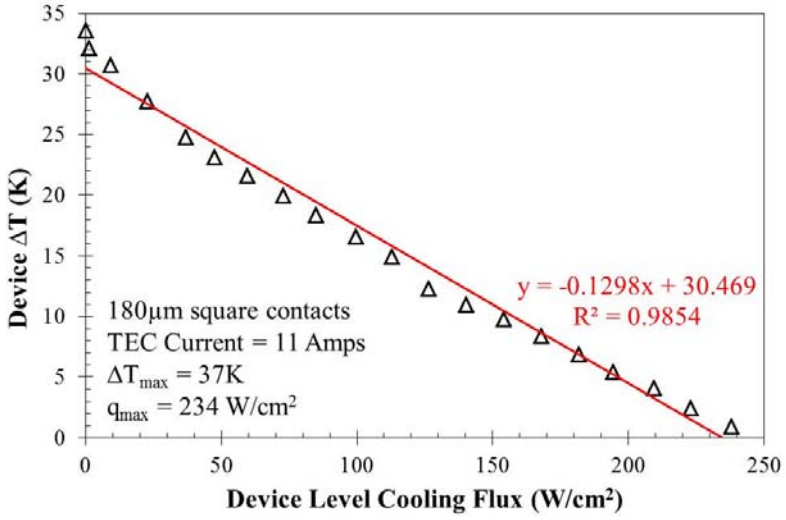


Figure 128. Device level ΔT as a function of cooling flux for the RTI SLTF cooler at a current of 11 amps.

5.4 Hotspot Creation

As previously mentioned, laser generated hotspots allow for more experimental flexibility, compared to photolithographic resistive heaters. The laser allows for the location, size, and number of hotspot to be readily changed, and methods for determining the laser power and spot size were discussed in Section 5.2. However, in order to accurately characterize laser created hotspots, the spatial intensity of the laser

spot must also be known and can be calculated using the data collected during the razor scanning technique previously mentioned.

5.4.1 Laser Beam Spatial Intensity Distribution

As indicated in Figure 129, it can be assumed that the laser beam is radially symmetric and made up of a series of rings, each with an intensity, I_j (shown in red). For the sake of computational simplicity, only a quarter of the laser beam was analyzed, but due to the radial symmetry, the results can be extrapolated to the full beam profile. In the razor scanning experiment, the amount of power in different slices of the laser beam, DP_i, was determined (shown in blue). The laser beam can be further broken down into smaller areas, $A_{i,j}$, as shown in the figure, which can be calculated using geometric identities. Recalling that power is equal to the produce of intensity and area, a system of linear equations can be constructed relating the geometrically calculated areas, the intensity of each ring, and the experimentally determined power in each slice of the beam.

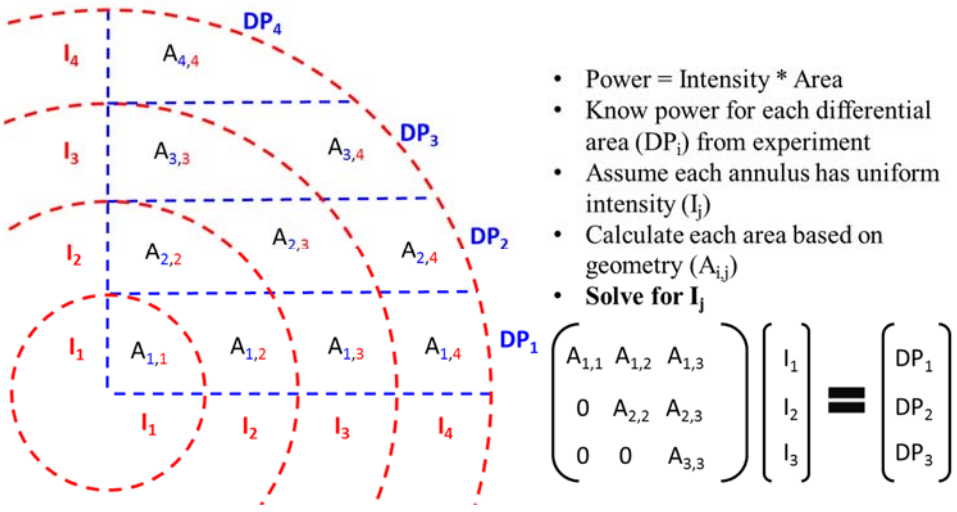


Figure 129. Mathematical approach for calculating radial intensity distribution of the laser beam using experimental data obtained from razor scanning experiment.

The system of equation can then be solved to find the intensity of each ring, giving the radial intensity distribution of the laser beam. Figure 130 shows an example of such an intensity distribution for laser powers of 2, 5, and 10 watts. Additional testing was performed at higher powers and smaller spot sizes, however as heat fluxes began to exceed 5-10kW/cm^2 the steel razor blade used for beam scanning would begin to melt, as shown in Figure 131.

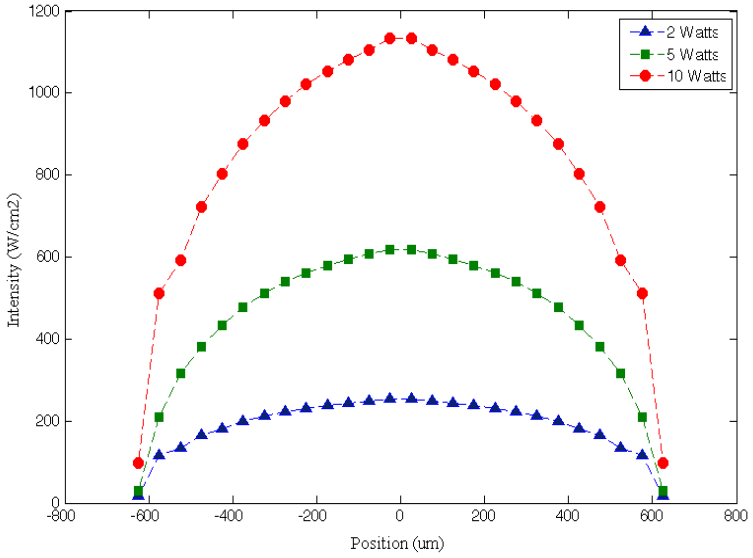


Figure 130. Radial intensity distribution of a focused laser beam with total power of 2, 5, and 10 watts.

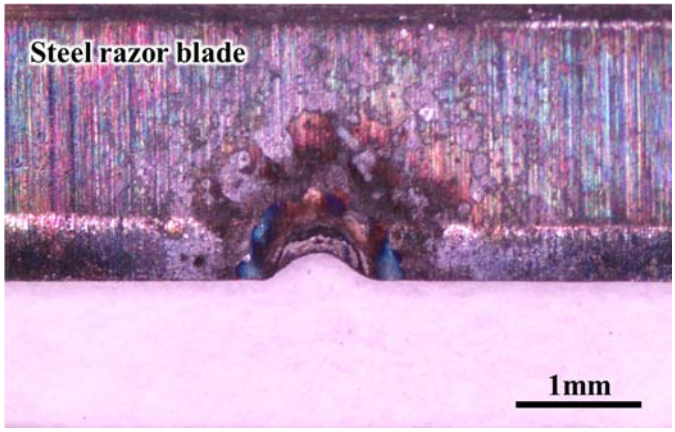


Figure 131. High power beam characterization resulted in melting of the steel razor blade used for scanning.

In order to check the accuracy of the intensity distribution calculation, the calculated distribution was integrated over the area of the beam, giving the total power, and the value was compared with the total power initially measured during experimentation. As can be seen in Table VI, the percent error in the calculated intensity distribution was calculated for three different laser powers, and it was found that the error decreased with increasing laser power.

Table VI. Experimentally determined power and power integrated from the calculated laser beam intensity distribution.

Power	Measured Power (W)	Integrated Power (W)	% Error
Low	2.02	2.33	15.6
Medium	5.00	5.54	10.7
High	9.85	10.29	4.5

5.4.2 Experimental Demonstration of Laser Created Hotspot

Laser created hotspots were experimentally demonstrated on Si and SiC substrates. In Section 3.3, a low power hotspot was created on a silicon substrate and cooled using a monolithic thermoelectric cooler. Additional testing was performed on blank silicon and silicon carbide substrates, using the test setup shown in Figure 132. These experiments were not exhaustive, as their purpose was not to prove the hotspot cooling merits of thermoelectric modules. Rather, the results are meant to show that a laser can be used to create areas of elevated temperature on electronic substrates.

As shown in the Figure, the cold side of the thermoelectric device was attached to the silicon or silicon carbide substrate using GaSn solder and the hot side of the thermoelectric cooler was attached to a liquid cooled cold plate. The laser was then

used to create a hotspot on the opposite side of the wafer, centered under the thermoelectric cooler. The laser system was connected to an XYZ positioning stage, so the laser created hotspot could be precisely aligned with the thermoelectric cooler.

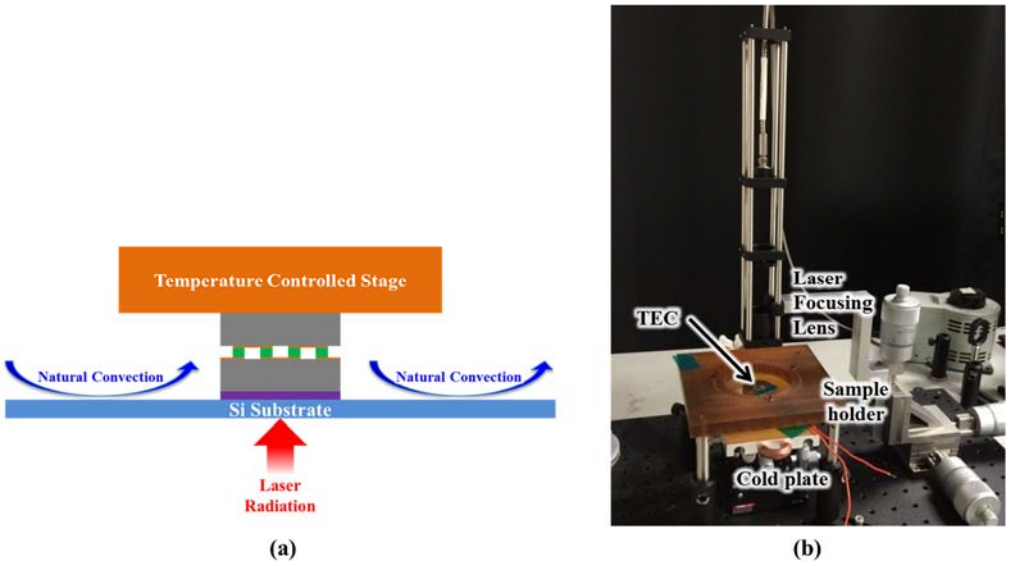


Figure 132. Hotspot creation using a laser and thermoelectric cooling on a blank silicon or silicon carbide wafer.

Since there is no mini/micro-contact structure to concentrate the thermoelectric cooling, the hotspot heat flux was limited to 100 to 200W/cm^2. However, the hotspots that were generated were fairly large, with a diameter of 1300µm, thus the total powers of the hotspots were up 2.5 watts which is greater than the power of the 200µm x 200µm, 5kW/cm^2 hotspot considered in the ICECoool project. Higher power and heat flux hotspot could have been created by increasing the laser power, however the higher power would have exceeded the cooling capacity of the thermoelectric device. Figure 133 shows the temperature distribution in the silicon and silicon carbide substrate resulting from the laser created hotspot. Both hotspots have a diameter of 1300µm and

the silicon hotspot has a power of 2.5W (150W/cm^2 heat flux) and the silicon carbide hotspot has a power of 1.1W (85W/cm^2 heat flux).

Figure 133(b) shows the temperature distribution along the bottom of the substrate, and as can be seen in red, the laser heating increases the temperature of the silicon hotspot by 20K to a temperature of approximately 40ºC. When the thermoelectric cooler is activated, the hotspot is completely removed, and temperature distribution in the silicon substrate is flattened. The SiC was transparent to the laser radiation and infrared camera, so the bottom of the SiC substrate was coated with graphite.

As can be seen from the blue lines in Figure 133, the laser radiation creates a hotspot with a peak temperature of 32ºC on the silicon carbide substrate. It is suspected that the thermal resistance between the SiC substrate and the graphite coating impeded spreading of the laser created hotspot into the underlying substrate and trapped the heat in the graphite layer, which limited the laser heat flux that could be applied. Therefore, if a coating with better thermal contact was used, more of the laser heating would conduct into the silicon carbide substrate, and larger laser powers could be applied. As can be seen, when the thermoelectric cooler is activated, it reduces the temperature of the chip uniformly, thus proving 10K of hotspot cooling, but only marginally improving the temperature uniformity in the chip.

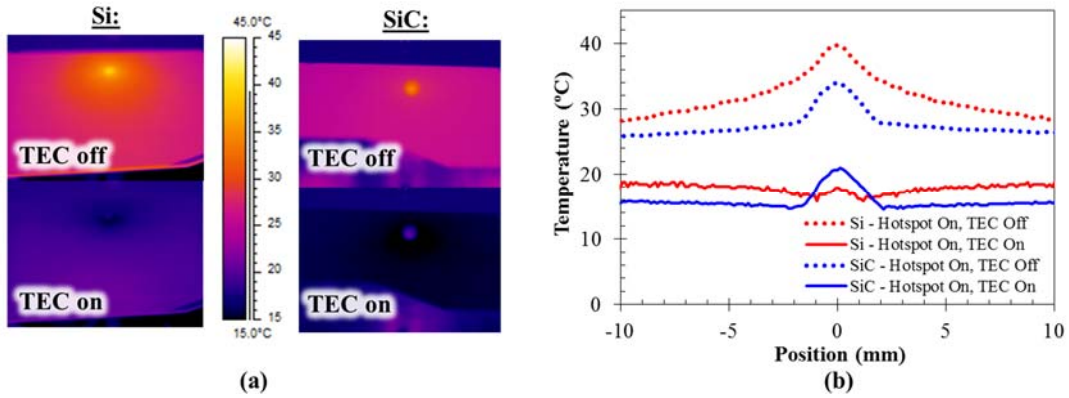


Figure 133. Temperature distribution around the laser created hotspots on silicon and silicon carbide substrates, with and without thermoelectric cooling.

5.5 Conclusions

The feasibility of using a laser to create hotspots for testing of novel thermoelectric configurations and to characterize thin film thermoelectric devices was studied and experimental demonstrations of both applications were presented. Two different thermoelectric modules were characterized using laser heating and localized hotspots were created on both silicon and silicon carbide substrates.

The non-contact thermoelectric device characterization method used an infrared camera to measure the hot and cold side temperature of a thermoelectric module to calculate the device temperature difference (ΔT), and used a laser to provide heating for measuring the device heat pumping (Q). Corrections for the emissivity of sample's surface and calibration of the laser power and spot size were performed to ensure accurate results. A commercially available Laird HV37 thermoelectric device was tested and is was found that the device produced a maximum ΔT of 42.3K at a current of 1.1 amps, which agreed well with manufactures supplied values. Additionally, it was found that currents of 0.39 and 1.1 amps could produce maximum heat pumping of 2.0W and 3.4W, which also was comparable to manufacture specified

values. An experimental superlattice thin film device was also characterized, and it was found to have a maximum ΔT or 37K and maximum cooling flux of 235W/cm^2, which agreed well with previously determined values of a 36K maximum ΔT and 213W/cm^2 maximum cooling flux.

The laser was also used to create hotspots on silicon and silicon carbide substrates for testing of novel hotspot cooling systems. In order to quantify the spatial distribution of heat flux in the laser created hotspot, a method for calculating the radial intensity distribution of the laser beam from the razor scanning results was developed. As was presented in Section 3.3, the laser was used to create hotspot for the testing of the silicon based monolithic cooler fabricated at UMD. Additionally, hotspots were created on blank Si and SiC wafers and cooled using thin film thermoelectric modules.

6 Conclusions and Future Work

6.1 Conclusions

Hotspots on electronic substrates often limit device performance and compromise device reliability. While hotspots can have heat fluxes in the kW/cm^2 range and temperature rises in excess of 100K, they are typically small and have modest total power dissipation. Therefore, a hotspot cooling system only needs to be capable of removing a few watts of heat in order to have a profound impact on a device's thermal performance. Two different thermoelectric cooling configurations were considered, and their ability to provide localized cooling of kW/cm^2 hotspots was numerically and experimentally studied.

The monolithic cooling configuration is a planer thermoelectric cooling approach, which utilizes the underlying semiconductor substrate as a leg of the thermoelectric circuit. It was found that transient "super cooling" could be used to provide bursts of additional Peltier cooling in order to cool short duration, high heat flux hotspots, and two new metrics, transient advantage and transient penalty, were introduced to help capture the trade-offs involved. Additionally, the large magnitude current pulses used in "super cooling" produce additional Joule heating, leading to an eventual rise in hotspot temperature, and it was therefore shown that selecting the correct current pulse profile is critical for maximizing the transient "super cooling," while minimizing the transient hotspot temperature rise.

The thermal conductivity, Seebeck coefficient, electrical resistivity, and electrical contact resistance of a monolithic cooler were parametrically studied and it was found that significant enhancement in hotspot cooling, on the order of a 100K, could be achieved if certain thermoelectric material property milestones could be reached. Finally, a silicon based monolithic cooler was successfully fabricated and tested at the University of Maryland, and it was found that the silicon monolithic cooler could provide 0.5K of localized cooling at the cooler. Additionally, monolithic cooler was used to cool a low power laser created hotspot in both steady state and transient operation.

Micro-contact enhanced thermoelectric cooling was numerically and experimentally shown to be capable of significantly reducing the temperature of localized kW/cm^2 level hotspots, greatly improving the chip temperature uniformity and enhancing performance and reliability of power electronic devices. A variety of

mini/micro-contact materials and form factors were studied and integrated micro-contacts were found to be thermally superior and more reliable than discrete contacts. Numerical models of thermoelectric coolers were created in ANSYS and tuned to match manufacturer supplied performance curves. The device level models were then added to a system level model with an integrated micro-contact and hotspot cooling was parametrically studied.

Hotspot temperature reductions of up to 40K were demonstrated using a commercially available thermoelectric module, and the hotspot temperature rise resulting from a 3000W/cm^2 hotspot in silicon was completely removed. Finally, micro-contact enhanced thermoelectric hotspot cooling was numerically extended to silicon carbide substrates, and due to silicon carbide's relatively higher thermal conductivity, it was predicted that the hotspot temperature rise resulting from heat fluxes up to 5000W/cm^2 could be reduced to less than 5K.

It was shown that the micro-contact enhanced thermoelectric cooling system must be optimized and negative impacts on the global convective or evaporative cooling system must be minimized. Therefore, potential enhancements to the heat pumping capacity of compact thin film thermoelectric coolers were also studied. It was found that the maximum cooling flux of the thermoelectric device increased linearly with element packing fraction and that reductions in electric contact resistance could produce device level cooling fluxes in excess of 500W/cm^2.

Finally, the feasibility of using a laser to create hotspots for testing of novel thermoelectric configurations and to characterize thin film thermoelectric device

performance was studied, and experimental demonstrations of both applications were presented. The non-contact thermoelectric device characterization method used an infrared camera to measure the hot and cold side temperature of a thermoelectric module in order to calculate the device temperature difference (ΔT), and used a laser to provide heating for measuring the device heat pumping (Q). A commercially available Laird HV37 thermoelectric device and an experimental superlattice thin film thermoelectric cooler produced at the Research Triangle Institute were both tested and the results agreed well with previously measured values. The laser was also used to create hotspots on silicon and silicon carbide substrates for testing of novel hotspot cooling systems and an algorithm was developed for calculating the radial intensity distribution of the laser beam in order to quantify the spatial heat flux distribution in the laser created hotspots.

6.2 Future Work

6.2.1 Monolithic Cooling Configuration

Extensive numerical modeling of the monolithic cooling configuration has been performed at the University of Maryland, but there are limited experimental demonstrations of monolithic cooling in the literature. In particular, fabrication of monolithic coolers on advanced substrates could produce significantly enhanced cooling performance, such as hotspot temperature reductions in excess of 50K, but require additional expertise in microfabrication and material science.

Advanced superlattice substrates with high Seebeck coefficient and low thermal conductivity, such as Si/SiC, Si/SiGe and BiTe based alloys have been reported in the

literature, so these materials could be integrated into thermoelectric modules and planer thermoelectric cooling configurations.

6.2.2 Micro-Contact Enhanced Cooling

Numerical modeling predicts that due to silicon carbide's relatively higher thermal conductivity, the hotspot temperature rise resulting from heat fluxes of $5kW/cm^2$ could be completely removed using an integrated micro-contact. Thus, thermal performance on silicon carbide substrates should be experimentally demonstrated and a more comprehensive experimental demonstration, with a thermoelectric cooler embedded in a global cooling system, could be created to cool a chip with hotspot and background heating.

As a part of this effort, compact thermoelectric modules with high cooling flux and small footprint should be developed for integration into the background cooling system. Improvements in manufacturing could be studied to increase the maximum thermoelectric packing fraction and reduce electrical contact resistances inside thermoelectric modules. Additionally, if evaporative cooling is used to remove the background heat flux, the flow behavior and heat transfer characteristics in the thermoelectric shadow should be studied using CFD and experimental studies.

High conductivity discrete micro-contacts make of diamond or silver-diamond composites concentrate hotspot cooling very efficiently, but are currently restricted to basic geometries due to manufacturing limitations. Advanced techniques to make diamond contacts with varying cross sectional area or silver diamond composites that

are reliable and can be molded into complex shapes could be beneficial in many heat spreading applications.

6.2.3 Laser Created Hotspots and Device Characterization

The optical system used for creating hotspots could be refined in order to create smaller hotspots and to create patterns and hotspot of various shapes. The focusing lens for the laser must be far enough from the substrate that the infrared camera has space to measure the hotspot temperature, preventing the use of shorter focal length lens for smaller hotspot sizes. Higher quality lenses or better alignment techniques could potentially be utilized to reach hotspot diameters below 500μm and a more advanced optical setup could be created that uses a single objective lens for both viewing the temperature with the infrared camera and focusing the laser beam.

Additionally, many different optical techniques for creating multiple hotspot or different hotspot shapes could be explored. There is interest in creating rectangular hotspots representative of the transistor 'fingers' on power amplifiers. The 'fingers' are typically 1μm x 100μm, making it unlikely that they could be created using a mask. Thus, one potential approach could be using alternating fringes of constructive and destructive interference, similar to Young's double slit experiment.

6.3 Major Contributions

6.3.1 Monolithic Cooling Configuration

Numerical:

- Created multiple transient monolithic cooling models in ANSYS and parametrically studied "super cooling" and transient cooling of a dynamic hotspot

- Introduced Transient Advantage and Transient Penalty metrics to better capture trade off involved in transient thermoelectric cooling
- Simulated different current and heat flux profiles, highlighting that step changes in current are actually the least efficient profile for transient "super cooling"
- Incorporated ANSYS' Solid226 element into models, which improved predictive accuracy by calculating Peltier heating/cooling at the element level
- Parametrically studied advanced thermoelectric substrates for the monolithic cooling configuration and showed potential for temperature reductions up to 100K.

Experimental:

- Successfully fabricated silicon based monolithic thermoelectric cooler in the UMD Nanocenter
- Developed an experimental method for testing the monolithic cooler, including compensation techniques to allow for infrared imaging of the multi-emissivity sample
- Measured localized cooling at the cooler level and cooled a laser created hotspot

6.3.2 Mini-Contact Enhanced Cooling

Numerical:

- Created a variety of device level thermoelectric models and matched performance to experimentally determined values

- Created a variety of system level models for simulation of integrated and discrete mini/micro-contacts of different materials
- Implemented temperature dependent SiC thermal conductivity for more accurate hotspot temperature predictions
- Used modeling and collaboration with reliability group to select a micro-contact configuration with acceptable thermal and reliability performance
- Parametrically studied interaction of thermoelectric cooler with global cooling system
- Demonstrated 40K of hotspot cooling and complete removal of hotspot temperature rise for heat flux of 3kW/cm^2 in silicon
- Demonstrated hotspot temperature rise of less than 5K for a 5kW/cm^2 hotspot in silicon carbide
- Demonstrated the potential for significant improvement in the heat pumping capacity of thin film thermoelectric modules

Experimental:

- Designed and constructed experimental apparatus for integrated micro-contact enhanced cooling of hotspots
- Designed a test wafer consisting of heater/RTDs and micro-contact pillars
- Experimentally demonstrated 20K of cooling and a temperature rise of less than 6K for a 3kW/cm^2 hotspots

6.3.3 Laser Created Hotspots and Device Characterization

- Designed and implemented optical setup for laser hotspot creation and device characterization
- Created calibration curve for laser output power
- Used razor scanning technique to measure laser beam diameter
- Developed algorithm for calculating spatial intensity distribution of the laser beam, based on a razor scanning data
- Developed a novel non-contact technique for characterizing mini to micro sized thermoelectric devices and tested commercially available and experimental modules
- Filed an invention disclosure and provisional patent for TEC characterization technique
- Created hotspot to test silicon monolithic cooler and created hotspots on blank silicon and silicon carbide substrates

6.3.4 Miscellaneous

- First author on thermoelectric cooling review article for the Annual Review of Heat Transfer
- Mentored undergraduate RevCon team and made it to the final round of the DARPA RevCon Competition
- Filed an invention disclosure and provisional patent for the RevCon team's design

6.4 Publications

6.4.1 Journal Papers

1. **M. Manno**, P. Wang, and A. Bar-Cohen, "Pulsed Thermoelectric Cooling for Improved Suppression of a Germanium Hot Spot," *IEEE Transactions On Components Packaging and Manufacturing Technologies*, Vol. 4, No. 4, pp. 602-11, April 2014.

2. **M. Manno**, B. Yang, and A. Bar-Cohen, "Thermoelectric Coolers – Active Thermal Vias," *Thermal Management volume (V. 18) for the Annual Review of Heat Transfer*, Awaiting publication, January 2015.

3. **M. Manno**, B. Yang, S. Khanna, P. McCluskey, and A. Bar-Cohen , "Micro-Contact Enhanced Thermoelectric Cooling of Ultra High Heat Flux Hotspots," *IEEE Transactions on Components, Packaging, and Manufacturing Technology,* Submitted March 2015

4. **M. Manno**, B. Yang, A. Bar-Cohen, "Non-Contact Characterization Method for State of the Art Thermoelectric Modules" *Review of Scientific Instruments,* Submitted April 2015

5. Z. Liu, K. Fu, Z. Yang, Y. Yao, **M. Manno**, Z. Wang, J. Dai, B. Yang, L. Hu, "Cooling Textile Through Integrated Controlled Hot Spots Water Evaporation and Effective Infrared Transmission," *Energy and Environmental Science*, Submitted March 2015

6. G. Bulman, P. Barletta, J. Lewis, **M. Manno**, B. Yang, A. Bar-Cohen "Thin-Film Bi^2Te^3 Superlattice Thermoelectric Devices for Cooling Ultrahigh Heat Fluxes," *Nature Nanotechnology*, In preparation

7. W. Luo, L. Zhou, K. Fu, Z. Yang, J. Wan, **M. Manno**, Y. Yao, H. Zhu, B. Yang, L. Hu, "A Thermal Conductive Separator for Stable Li Metal Anodes," Nano Letters, In preparation

6.4.2 Conference Proceedings

1. **M. Manno**, P. Wang, and A. Bar-Cohen, "Transient Thermoelectric Self-Cooling of a Germanium Hotspot," *Proceedings of the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM 2012)*, May 2012, Paper No.: ITHERM2012-6231460.

2. **M. Manno**, P. Wang, and A. Bar-Cohen, "Anticipatory Thermoelectric Cooling of a Transient Germanium Hotspot," *Proceedings of the International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems (*InterPACK2013), July 2013, Paper No.: IPACK2013-73186.

3. P. Wang, **M. Manno**, and A. Bar-Cohen, "Quantum-Well Si/SiC Self-Cooling for Thermal Management of High Heat Flux GaN HEMT Semiconductor Devices," *Proceedings of the ASME* Third International Conference on Micro/Nanoscale Heat and Mass Transfer (*MNHMT2012)*, Sep.2012, Paper No.: MNHMT2012-75290.

4. G. Bulman, P. Barletta, J. Lewis, **M. Manno**, A. Bar-Cohen, and B. Yang, "High Heat Flux Measurement of Thin-Film Thermoelectric Devices," *Proceedings of the International Conference on Thermoelectrics (ICT2014)*, July 2014.

5. R. Mandel, **M. Manno**, D. Squiller, P. McCluskey, B. Yang, M. Ohadi, "Embedded FEEDS Micro Channel Cooling with Thermoelectric Hotspot Removal – An Intrachip Approach," Poster presented at *DARPA/MTO ICECool Modeling Workshop*, January 2015

6. **M. Manno**, B. Yang, P. McCluskey, M. Ohadi, "Micro-Contact Enhanced Thermoelectric Cooling for Removal of High Heat Flux Hotspots," Poster presented *GOMACTech Conference*, March 2015.

7. S. Khanna, P. McCluskey, **M. Manno**, B. Yang, M. Ohadi, A. Bar-Cohen, "Micro-Contact Enhanced Thermoelectric Cooling for Removal of High Heat Flux Hotspots," *IMECE2015*, In preparation.

6.4.3 Patents Activity

1. **M. Manno**, B. Yang, H. Liu, J. Fustero, "Low-Resistance Seamless Wedge Thermal Connectors," Invention Disclosure Filed February 2014.

2. **M. Manno**, B. Yang, and A. Bar-Cohen, "Non-Contact Laser Method for Characterization of Thermoelectric Modules," Invention Disclosure Filed June 2014.

Appendices

Appendix A. Silicon Monolithic Cooler Microfabrication Process

Fabrication Process Flow:

1. High temperature growth of SiO_2 dielectric layer
    - Tystar CVD; 200nm
2. Photolithography of $Si0_2$
    - Dehydration bake 5-minutes @ 110-120°C
    - Apply HMDS for adhesion (spin for 40 seconds @ 4000 RPM)
    - Apply 1.3µm Shipley 1813 photoresist (spin for 40 seconds @ 4000 RPM), soft bake (90-100°C for 1min)
    - Align and expose using MJB-3 Mask Aligner (365nm, 12-16 seconds)
    - Develop using Shipley 352 developer (40- seconds with slight agitation)
    - Rinse with DI water for 30-60 seconds followed by nitrogen blow dry and hard bake
    - Buffered Oxide Etch SiO_2 (ammonium fluoride and hydrofluoric acid)
    - Strip photoresist using Photoresist Remover
3. Deposition of metallization layer
    - Denton Evaporator (EBPVD), ~1µm of gold (to match n-type Si)
4. Photolithography of metallization
    - Dehydration bake 5-minutes @ 110-120°C
    - Apply 1.3µm Shipley 1813 photoresist (spin for 40 seconds @ 4000 RPM), soft bake (90-100°C for 1min)
    - Align and expose using MJB-3 Mask Aligner (365nm, 12-16 seconds)
    - Develop using Shipley 352 developer (40- seconds with slight agitation)

- Rinse with DI water for 30-60 seconds followed by nitrogen blow dry and hard bake
- Selective wet etch of gold
- Strip photoresist using Photoresist Remover

Appendix B. Effective Base HTC Used in Micro-Contact Modeling

SiC		
Two Phase Water (h = 80,000 W/m-K)		
50 x 400µm channels, 100 x 400µm fins		
Die x:	1.00E-02	m
Die y:	1.00E-02	m
Fin w:	1.00E-02	m
Fin h:	4.00E-04	m
Fin t:	1.00E-04	
MC w:	5.00E-05	m
Fin k	300	W/(m-K)
h avg:	8.00E+04	W/(m^2-K)
# of Fins:	67	
P	2.02E-02	
Ac	1.00E-06	
m2:	5.39E+06	
m:	2.32E+03	
Fin Eff:	**0.786**	
Fin area	5.33E-04	
Base area	3.33E-05	
Fin HT	3.35E+01	
Base HT	2.67E+00	
Eff. HTC:	**3.62E+05**	W/(m^2-K)
	3.64E+05	

Si		
Single Phase Water (h = 20,000 W/m-K)		
50 x 700µm channels, 100 x 700µm fins		
Die x:	1.00E-02	m
Die y:	1.00E-02	m
Fin w:	1.00E-02	m
Fin h:	7.00E-04	m
Fin t:	1.00E-04	
MC w:	5.00E-05	m
Fin k	160	W/(m-K)
h avg:	2.00E+04	W/(m^2-K)
# of Fins:	67	
P	2.02E-02	
Ac	1.00E-06	
m2:	2.53E+06	
m:	1.59E+03	
Fin Eff:	**0.724**	
Fin area	9.33E-04	
Base area	3.33E-05	
Fin HT	1.35E+01	
Base HT	6.67E-01	
Eff. HTC:	**1.42E+05**	W/(m^2-K)
	1.50E+05	

Appendix C. Micro-Contact Test Wafer Microfabrication Process

Oxide and Heater Side of Wafer:

1. Wafer Cleaning and Prep
    - RCA clean (Organic and particle, Oxide strip, Ionic clean, Rinse and dry)
    - Si wet oxide with Hydrochloric Acid (HCl) (~200nm on Si a little less on SiC)
2. Deposition of dielectric
    - Low Pressure Chemical Vapor Depostion (LPCVD) of silicon nitride (45 min, 120 nm)
    - High temperature oxide growth (HTO) of silicon oxide (250 nm)
    - Apply FCS to one side, hard bake
    - Strip oxide:10 min 6:1 BOE (wet)
    - Strip nitride: 4 min in CHF_3/O_2 at 150 Watts (dry)
    - Finish with 10 min in 6:1 BOE (wet)
    - Strip FSC using O_2 asher (15 min, 900W)
3. Piranha clean wafer (removes organics)
    - Sulfuric Acid (H_2SO_4) + Hydrogen Perodixde (H_2O_2)
4. Deposition of Heater Metal
    - Sputter 10.5nm titanium (adhesion layer) and 400nm platinum
5. Lithography of Heaters
    - Apply AZ nLOF negative photoresist, bake 60 sec, 115°C
    - Expose on MA6B (7 sec)
    - Post exposure bake (60 sec, 115°C)
    - Develop using AZMIF 726 developer (90 sec)

- Pattern metal layer using ion mill (3X3 min millings @ 600V 70DGS)

6. Strip Photoresist using O_2 plasma in Barrel resist stripper

Etching of Micro-Contact Pillars:

1. Apply AZ nLOF negative photoresist, bake 60 sec, 115°C
    - Expose on MA6B (7 sec)
    - Post exposure bake (60 sec, 115°C)
2. Develop using AZ MIF 726 developer (90 sec)
3. Etch pillars reactive ion etching
4. Strip Photoresist using O_2 plasma in Barrel resist stripper

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