ABSTRACT

Title of Document: READ-OUT CIRCUITS FOR INTEGRATED SURFACE ACOUSTIC WAVE SENSORS.

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Readout modules for vapor and liquid phase SAW sensors fabricated on piezoelectric films are typically configured as single or dual delay line oscillator loops. Mass loading of the sorbent film realized on the SAW device is detected as a frequency shift which is read externally via a frequency counter. However, this approach is not directly applicable in the development of a monolithically integrated autonomous sensor system suitable for wearable sensor tags and other field applications. In this work we have developed a data measurement topology suitable for monolithically integrated SAW sensors on CMOS chips, a technology that is not fully developed and will significantly increase Si-CMOS functionality. This readout technology achieves closed loop conversion of the SAW frequency response to a well-defined output voltage accurately tracking sensor behavior in real time. The topology is appropriate for thin film, low loss interdigitated (IDT) SAW devices used as mass loading sensors, such as those reported in [1] and [2].

The proposed closed loop system is controlled by a finite state machine (FSM) which forces the system output to oscillate within a narrow voltage range that correlates with the SAW pass-band response. The period of oscillation is of the order of the SAW phase delay. We also use timing information from the FSM to convert SAW phase delay to an on-chip 10 bit digital output operating on the principle of time to digital conversion (TDC). The output voltage range varies with changes in SAW center frequency, thus tracking mass sensing events in real time. This architecture precludes mode jumping issues found in designs incorporating the SAW delay line or the resonator in the feedback loop of an amplifier. It was demonstrated that the system can be adapted to alternate SAW center frequencies and group delays by adjusting the VCO control and TDC delay control inputs. Because of frequency to voltage and phase to digital conversion, this topology does not require external frequency counter setups and is uniquely suitable for full monolithic integration of autonomous sensor systems and tags.

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READ-OUT CIRCUITS FOR INTEGRATED SURFACE ACOUSTIC WAVE SENSORS

By

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Dedication

To Mayurika

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Chapter 1: Introduction

Surface acoustic wave (SAW) devices have been used as filters, sensors, oscillators, signal convolvers. Application as filters in telecommunication systems has been particularly widespread because SAW filters have roughly linear phase delay characteristics resulting in relatively low distortion. Bandpass and linear phase characteristics are achieved at lower design areas compared to LC filters. SAW devices have been tested in extreme temperature ranges. SAW technology is also less susceptible to process and power supply variations that affect semiconductor devices.

In addition to these features, another property of SAW devices makes them ideal for sensor applications. The confinement of surface acoustic waves to the piezoelectric surface results in high sensitivity to mass loading of the film. Mass loading lowers the phase velocity of the sound wave which causes a shift in the center frequency of the SAW device. The significance of this property is that if a sorbent film is realized on the piezoelectric surface and the film is subsequently exposed to vapor or liquid phase media, then resulting absorption will lead to a measurable change in electrical characteristics of the entire device. SAW sensors, therefore, operate on the principle of measuring frequency, phase shift or return loss as a result of mass loading.

Diverse approaches have been targeted in measuring such shifts and identifying the presence and weight of specific gaseous or liquid substances using SAW sensors in critical or harsh environments. A readout module in the case of a

SAW sensor may be thought of as a unit that measures and reports the changes in SAW parameters. In the most straightforward case, a readout module might be external instrumentation that measures the change in frequency response. However, if the sensor is to be used in a real time application or a tag, a readout circuit that both controls the SAW device and measures output changes is necessary.

Most research in the case of SAW sensors remains focused on expanding the pool of adsorbates, ranging from toxic gases to biomarkers including proteins. In addition, increasing mass sensitivity by optimizing piezoelectric film thickness and selecting polymer sorbent films have also received attention [9], [17], [20]. Targeting these new substances and films inevitably leads to a need for integrated readout circuits that are able to report measurements in a variety of environments.

Reported readout circuits have configured the SAW device in topologies that have targeted band-center frequency or phase as measured parameters. Nevertheless, research in this area remains rewarding since it is possible to uncover novel methods to integrate the SAW device in a CMOS based readout. A challenge in designing readouts is the loss of resolution resulting from an on chip conversion of the SAW output frequency. Another challenge is to adequately analyze the composite circuit using models of both the piezoelectric and the analog sections of the readout.

1.1 Motivation

Typically, readout modules for vapor and liquid phase SAW sensors fabricated on piezoelectric films are configured as single or dual delay line oscillator loops. Remote readout mechanisms using wireless interrogation have also been proposed. In the case of oscillator topologies mass loading of the sorbent film realized

on the SAW device is detected as a frequency shift which is read externally via a frequency counter. Both in the case of direct frequency response measurements with network analyzers and in the case of frequency counter based measurements, high resolution can be achieved. However, these approaches are not directly applicable in the development of a monolithically integrated autonomous sensor system suitable for wearable sensor tags and other field applications.

The motivation of this work is to develop a data measurement topology suitable for monolithically integrated SAW sensors on CMOS chips, a technology that is not fully developed and will significantly increase Si-CMOS functionality. This readout technology achieves closed loop conversion of the SAW frequency response to a well-defined output voltage accurately tracking sensor behavior in real time. Using a finite state machine (FSM) to control the VCO, the goal is to design a robust and stable loop which will be able to start up from any state and reach steady outputs. The use of such a finite state machine leads to an added benefit. The design is expanded to efficiently convert the sensor output to a digital readout. This is accomplished by using the timing information embedded in the existing FSM outputs and adding a second FSM in the conversion circuit. This topology avoids loss of resolution resulting from buffering of the analog signal for use in switched capacitor based conversions. Our readout topology is appropriate for high quality, thin film, low loss interdigitated (IDT) SAW devices used as ultra-sensitive mass loading sensors, such as those reported in [1] and [2]. Additionally, this low frequency loop architecture would preclude mode jumping issues found in designs incorporating the SAW delay line or the resonator in the feedback loop of an amplifier.

1.2 Overview of Dissertation

The dissertation is organized in the following manner. In Chapter 2 we present a background on surface acoustic devices. The structure of a non-apodized inter-digitated transducer (IDT) and the frequency and phase response of such a device are discussed. Electrical modeling techniques of IDT devices are also presented along with simulation results using equivalent circuit models.

In Chapter 3 we present a background on interaction of vapor mode analytes with mass-sensitive films which are coated on the IDT structure. This chapter is essentially a review on sorption mechanisms and time varying SAW device response under the impact of mass loading.

Chapter 4 presents a review of prior work in the area readout circuits for SAW sensors. Various topologies including open loop direct frequency measurement, single and dual oscillator based designs, PLL based topology and transponder based measurements are discussed, with examples from recent work. Review of these techniques is meant to introduce and present a contrast to the work done during this dissertation research.

In Chapter 5 we present the top level architecture of our design, discussing the primary and secondary conversion loops and the communication between these two sections.

In Chapter 6 we delve into block level design and analysis of the primary sensor loop. Circuit operation, functionality in various modes and physical design are discussed for the VCO, the peak detecting comparator and the finite state machine. We next analyze the loop operation presenting equations governing steady behavior.

Discrete time analysis along with behavior modeling are also presented in this chapter.

In Chapter 7 we present simulation and experimental results of the primary sensor loop. The readout is simulated with SAW devices operating at 374MHZ, 140MHZ and 70MHZ. Experimental results are presented for the 140MHZ and 70MHZ devices. The main observation nodes are the sensor output ramp and the finite state machine outputs. The envelope of the SAW output voltage and the time varying VCO and SAW outputs are also observed under various control voltages.

In Chapter 8 we analyze the block level design of the secondary conversion circuit including the second finite state machine that is embedded in this module, the modified up/down counter and the time to digital converter.

In Chapter 9 we present test results of the secondary conversion loop. We start with system simulation results showing the steady state behavior of the digital output bus with the corresponding signals from the primary sensor loop. The core level digital signals behavior is also observed. This chapter also presents a summary of results from previous published work and results from our work.

In Chapter 10 we summarize the study with a discussion of potential for future work and expansion of the readout.

Chapter 2: Surface Acoustic Wave Device Modeling

2.1 IDT Structure

Before discussing the existing sensor approaches using SAW devices, we present some theoretical background of interdigitated transducers. We consider the basic two transducer SAW device as shown in Fig.2.1. When a voltage is applied to the input transducer, a periodic electric field is generated and a corresponding elastic stress is caused due to the piezoelectric effect. Surface waves are generated for frequencies at which the wavelength matches the transducer pitch. The output transducer receives the incident wave and converts it to an output voltage. Thus, in effect this is a two port device, often characterized as a delay line, the frequency response of which depends on various factors including number of electrodes, pitch, separation, apodization overlap and substrate characteristics. The center frequency is set by choosing the IDT pitch as the SAW wavelength.

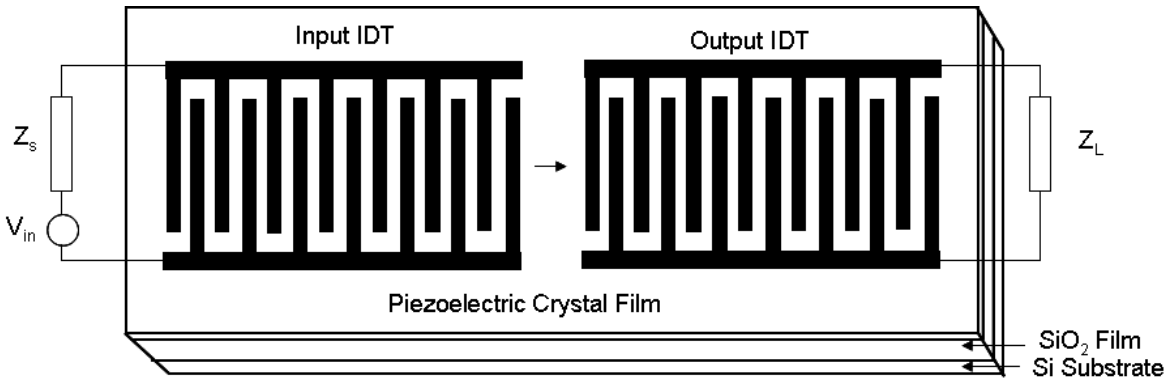

Figure 2.1: Basic IDT Comb Structure

2.2 Circuit Models

Various circuit models exist for the analysis of SAW IDT device modeling. The delta function model which models the charge distribution as delta function sources situated on the electrodes will not be used for this analysis as it cannot be used to determine absolute values of input and output impedances and hence cannot be used to design appropriate matching circuitry. Only relative insertion loss levels can be estimated [19].

In our work we have used the crossed field model for generating admittance and scattering matrix parameters of SAW devices. We have used these models for selected circuit simulations to plot typical frequency responses in loaded and unloaded cases. Magnitude of passband ripple and input and output impedances were also estimated. In the crossed field model the field lines are assumed to be normal to the piezoelectric substrate. The actual electric field and the cross-field approximation are shown in Figure 2.2.

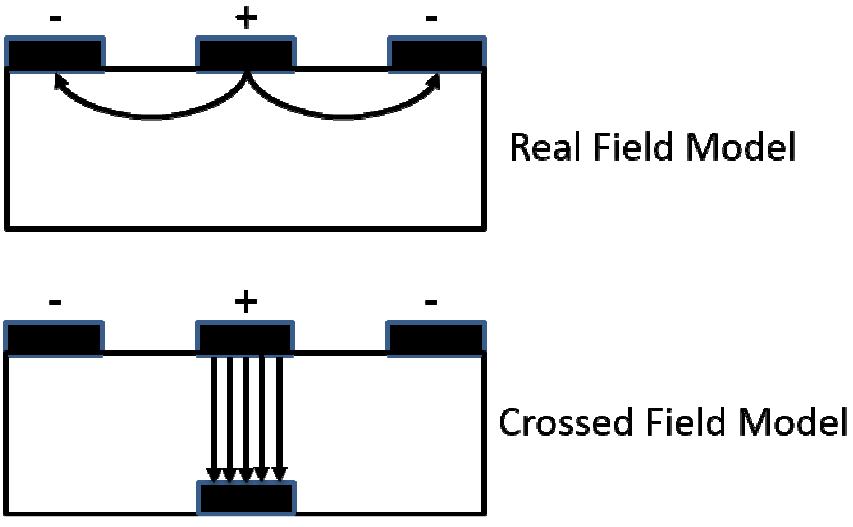

Figure 2.2: Electric field - Real and approximate

As outlined in [19], each IDT can be separately modeled as a three port with two acoustic ports and one electric port. The electrical equivalent of the two acoustic ports is represented as a SAW transmission line while the third is a true electrical port at which the input voltage is applied. Fig. 3 shows this representation.

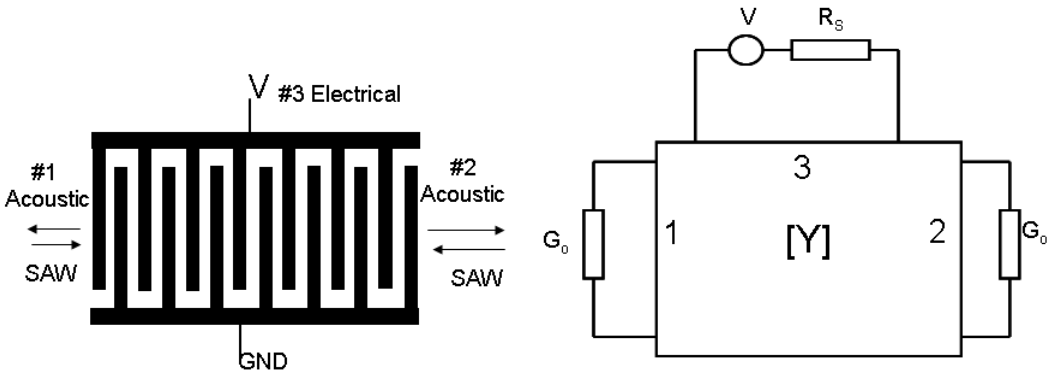

Fig. 2.3: Equivalent three port representation of a single IDT

In this model, the acoustic forces are converted into electrical voltages and SAW velocities are converted into equivalent currents. These transformations allow the mechanical characteristic admittance to be expressed as an equivalent transmission line characteristic admittance which is

$$G_o = K^2 C_s f_o \tag{2.1}$$

Here f_o is the center frequency, K is the electro-mechanical coupling coefficient and C_s is the static electrode capacitance of one periodic section. The electro-mechanical coupling coefficient can be defined in terms of the change in phase velocity as a result of surface metallization.

$$K^2 = 2\Delta v / v = 2(v_f - v_m) / v_f \tag{2.2}$$

Here v_f and v_m are the velocities on a free surface and a metallized surface respectively.

The center frequency can be determined from the known surface wave velocity (v) and period of the IDT; the capacitance can be experimentally or theoretically determined. Tabulated K values are available for various substrates. If the IDT is a generator, the emergent acoustic waves are assumed to be absorbed completely (without reflections) by the receiver and has a matched termination at its acoustic ports and vice versa. The 3-port matrix equation is given by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -jG_0\cot N\theta & jG_0\csc N\theta & -jG_0\tan(\theta/4) \\ jG_0\csc N\theta & -jG_0\cot N\theta & jG_0\tan(\theta/4) \\ -jG_0\tan(\theta/4) & jG_0\tan(\theta/4) & j\omega C_T + 4jNG_0\tan(\theta/4) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \quad (2.3)$$

Where $C_T = NC_s$ (total IDT capacitance of finger sections), N being the number of electrode pairs and $\theta = 2\pi f/f_0$ the electrical transit angle through one period (center to center distance between successive electrodes) [19].

In one possible approach we can model each IDT as an equivalent 3-port and cascade them to form the two port device of interest as shown in Fig. 2.4.

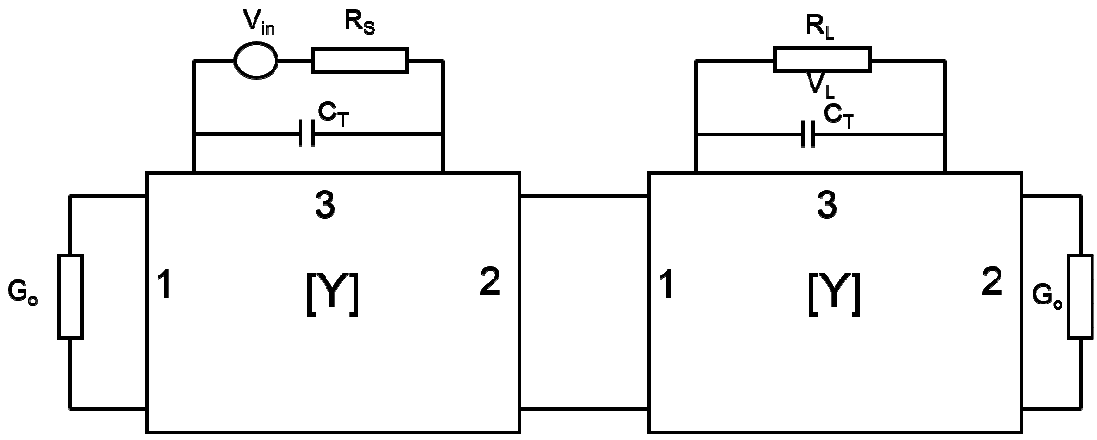

Figure 2.4: Two-IDT representation using cascaded three port model

Note that in the above diagram the effective capacitance C_T has been shown to be outside the 3 port model which is also a valid representation based on the admittance matrix.

The second approach is to directly derive the two port admittance parameters of the circuit in Figure 2.4. This is the method we have used. These parameters have been derived in [14] and are as follows:

$$y_{11} = G_{aa}(f) + j2\pi f C_{Ta} \quad \text{(input)} \tag{2.4}$$

$$y_{22} = G_{ab}(f) + j2\pi f C_{Tb} \quad \text{(output)} \tag{2.5}$$

$$y_{12} = 8NMG_o \frac{\sin(N\pi\Delta f / f_o)}{N\pi\Delta f / f_o} \cdot \frac{\sin(M\pi\Delta f / f_o)}{M\pi\Delta f / f_o} e^{j[\pi(1-(N+M)\Delta f / f_o)-\phi]} \tag{2.6}$$

N: Number of input IDT finger pairs *M*: Number of output IDT finger pairs

Δf=f-fo

ϕ: Phase shift between IDT centers

For the input IDT, the radiation conductance is given by

$$G_{aa}(f) \approx 8N^2 G_o \left| \frac{\sin(x)}{x} \right|^2$$
$$x = N\pi(f - f_o)/f_o \tag{2.7}$$

The radiation conductance of the output is obtained by substituting M for N above.

From standard network analysis the transfer function is obtained in terms of the admittance parameter and the source and the load impedances as follows:

$$H(f) = \frac{V_L}{V_{in}} = \frac{y_{12} R_L}{(1 + y_{11} R_s)(1 + y_{22} R_L) - y_{12}^2 R_s R_L} \tag{2.8}$$

The above analysis applies to a SAW delay line. Another configuration that is widely used is the resonator which has reflection gratings in either side of the IDT structures as shown in Figure 2.5.

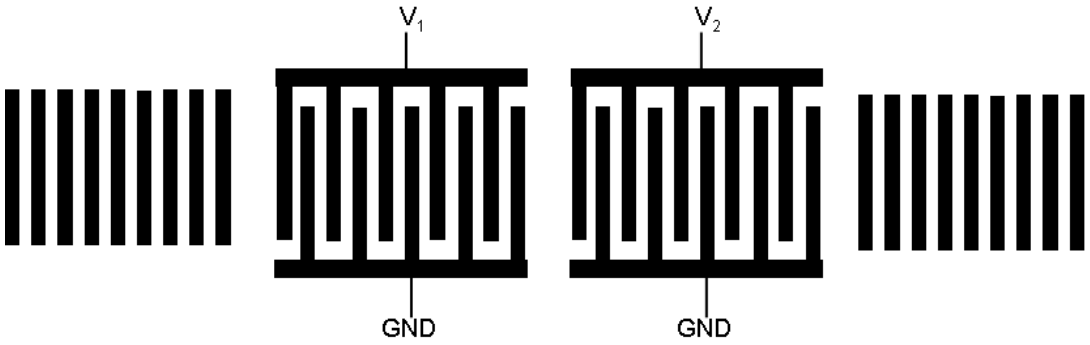

Figure 2.5: Two Port SAW Resonator

The presence of the gratings causes a sharp peak at the resonant frequency to be superimposed on top of the background delay line amplitude distribution. Equivalent circuits of resonators are given in [19]. The resonator design is more complicated as input and output radiation conductances have to be mismatched to

ensure minimum insertion loss levels of the delay line structure. It is also difficult to characterize and model parameters such as grating reflectivity and loss.

2.3 Coding and Simulation

We have implemented the crossed field model and obtained the admittance matrix for a two port delay line circuit incorporating an input and an output IDT. This matrix was generated over a range of frequencies using MATLAB and the results were then written to a data file in Spectre format and used in simulations to obtain the circuit frequency response.

To prepare such a model which can be incorporated into a large integrated circuit either in open loop or in closed configuration such as in the implementation of a delay line oscillator, we have written a MATLAB program where we have supplied available values of K and C_o for a ZnO substrate [18]. The value of the coupling coefficient is dependent on the normalized thickness of the piezoelectric substrate.

The program computes S parameters and Y parameters in a range of frequencies and writes these to a file. This file can be used to create the "nport" model available in the Spectre simulation tool. This two port model can either be simulated individually with appropriate source and load impedances or instantiated in a larger sensor design. Example transfer function simulation results have been shown.

Input and output matching networks can be designed from the calculated admittance parameters. The equivalent input and output admittances can be further refined by adding a susceptance term.

$$Y_{in} = G_a(f) + jB_a(f) + j2\pi fC_T \tag{2.9}$$

$$B_a(f) = 8N^2 G_o(\sin(2x) - x)/2x^2 \tag{2.10}$$

However, since this susceptance goes to zero at center frequency, it does not play a role in matching circuit design if match is desired only at this frequency.

Additional refinements can be made to the equivalent circuit model to incorporate various second order effects including reflection from electrodes.

The insertion loss, transfer function and equivalent normalized input admittance are plotted below based on MATLAB and Spectre simulation results. The MATLAB code is given in the appendix. Figure 2.6 shows the insertion loss of a SAW device centered at 300MHz. Here we note some passband ripple caused by triple transit interference. Passband ripple can be controlled by mismatching the output load at the cost of increasing the insertion loss [19]. In Figure 2.7 we observe the voltage transfer function measured at the load with respect to a 1V input. Figure 2.8 shows the frequency normalized input admittance with the expected band pass characteristics.

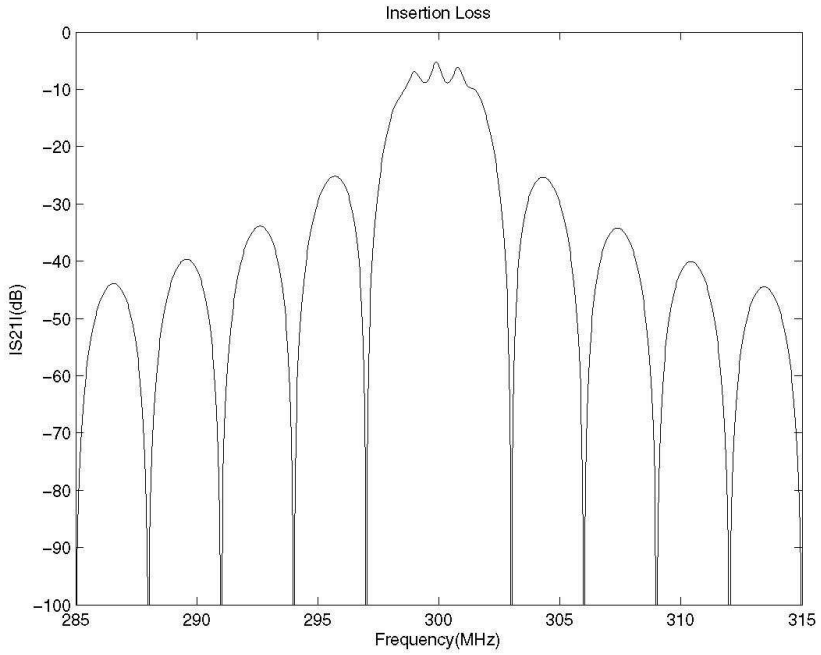

Fig. 2.6: SAW Delay Line Simulated Response at 300MHz

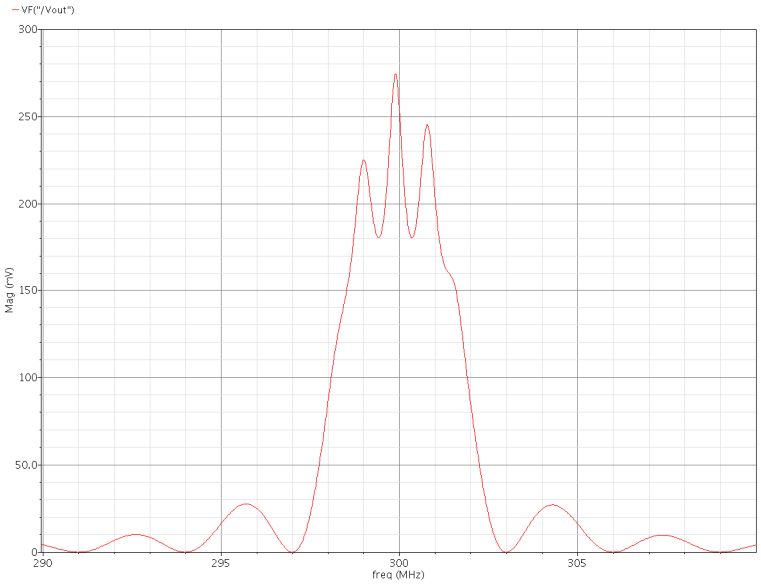

Figure 2.7: SAW Output Frequency Response of Transfer Function

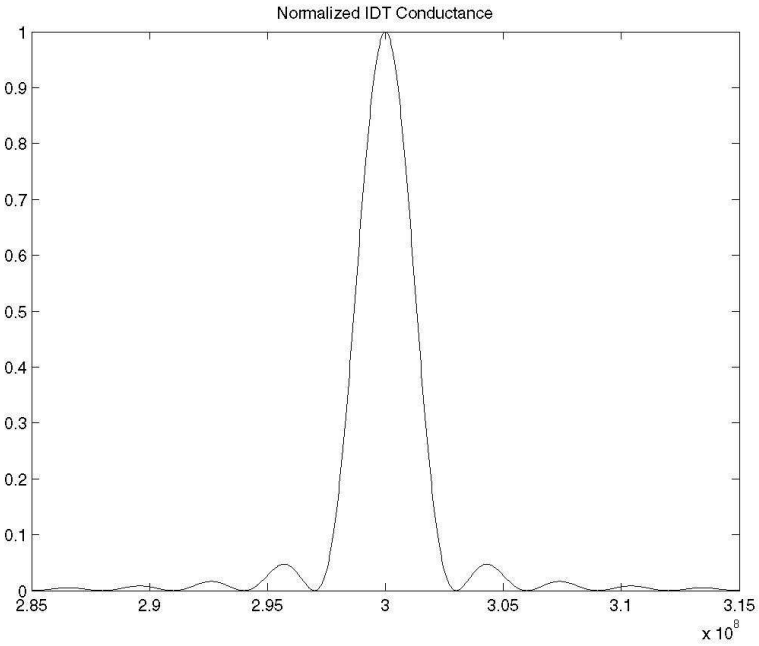

Fig. 2.8: Frequency Response of Normalized Input Admittance

Section 2.4 Summary

We have presented a theoretical background of interdigitated transducers and the transduction mechanism. A voltage excitation of the input transducer results in generation of surface acoustic waves with a bandpass response. The center frequency is specified by the transducer pitch while the bandwidth and ripple characteristics are governed by the apodization geometry.

To incorporate SAW devices in simulations, circuit models must be used. The delta function model and crossed field models are some such available models [19]. Starting with the crossed field model, a two IDT delay line structure can be represented as an equivalent two port. The admittance parameters of this two port are given by the conductance and effective capacitance of each IDT. The conductance itself is a bandpass function obtained by summing the excitation at each finger. The capacitance is a function of the number of electrodes as well as the capacitance per

finger pair. The transfer function and characteristic impedance of the delay line are determined by the parameters of the equivalent two port.

A MATLAB program was used to generate equivalent models of typical SAW delay lines with low insertion loss and characteristic impedance close to 50 Ω. The results show both passband and stopband ripples. The passband ripples are caused by triple transit interference. Such ripples can be reduced by deliberately mismatching the input and output terminations to absorb reflections at the cost of increasing insertion loss.

Chapter 3: Analyte Interaction with Sensitive Film

Section 3.1 Introduction

Layered SAW devices with shear horizontal polarization can be used for detection of gaseous or liquid analytes. A sensitive film coating the SAW devices absorbs the analyte and the resultant change in acoustic wave velocity causes a change in the center frequency of the device. In resonator or oscillator based approaches, the shift in frequency is measured and gives an estimate of the quantity of the absorbed analyte.

The frequency change due to mass loading can be expressed as

$$\Delta f / f_0 = \Delta v / v = (k_1 + k_2) f_0 \Delta m / A \qquad (3.1)$$

Here k_1 and k_2 are material constants related to the substrate, f_0 the operating frequency, A the area of the sensitive film, and Δm the mass of the absorbed gas. The sensitivity can be increased by increasing the operating frequency at the cost of increased attenuation.

Various sensitive films have been reported in literature. These can be broadly categorized into

i) Metal Pthalocyanines e.g. CuPc and PbPc on LiBNO3 for NO_2 and C_2H_4

ii) Nanostructured films such as MoOx on LiTaO3 for NO, NO, CO, H_2 and NH_3, SnO_2 nanobelts for CO and NO_2, ZnO nanobelts for H_2 and NO_2

iii) Polymer films

Existing literature shows that polymer films offer the benefit of being able to detect a broad spectrum of gases. Hence, an array of sensors coated with different polymers offers the best hope of detecting unknown vapors. However, response time is slow. Here we present an outline of various interaction mechanisms of gases with polymer coatings.

Section 3.2 Diffusion

A change in equilibrium pressure of a gas in contact with a thin polymer film can result in diffusion into the film and a resultant increase in acoustic wave frequency. Although most diffusion mechanisms are non-Fickian, in the case of some interactions such as Polyimide with Methanol, a Fickian model is sufficient [20]. For a diffusion coefficient D, the concentration variation is be given by the partial differential equation [20]

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}$$
$$\frac{\partial C}{\partial x} = 0 \text{ at } x = 0, C(h,t) = C_o(P_2) \text{ for } t \geq 0 \text{ and } C(x,t) = C_o(P_1) \text{ for } t \leq 0 \quad (3.2)$$

where C(x,t) is the gas concentration at a distance x from the interface, t the time after the change in partial pressure, h the film thickness, P_1 the equilibrium gas partial pressure and P_2 the partial pressure due to mass loading . The above can be solved to obtain

$$C(x,t) = C_o(P_2) - 2(C_o(P_2) - C_o(P_2))\sum_{n=1}^{\infty}\frac{\sin(ax/h)e^{-a^2Dt/h^2}}{a}$$
$$a = \pi(n - 1/2) \quad (3.3)$$

Integrating this over x, an expression can be obtained for the total moles diffused as a function of time.

$$M(t) = M_{\max}(1 - 2\sum_{n=1}^{\infty} \frac{e^{-a^2 Dt/h^2}}{a^2}) \tag{3.4}$$

This predicts that accumulation into the film will saturate after some time.

In the case of Non-Fickian diffusion, relaxation equations are needed for analysis [20].

Section 3.3 Adsorption

In this process the gas adheres to the polymer film surface due to molecular interactions. In the case of weak interaction such as Van der Waals forces this process is termed physisorption. Physisorption reaches an endpoint when the gas concentration in the polymer reaches a saturation value. Physisorption is typically reversible. Also it is relatively non-specific. Certain porous polymers such as tenax, XAD and Chromosorb can be used as adsorbents for analytes such as polynuclear aromatic hydrocarbons. Selectivity can be potentially improved by controlling the pore size. Various adsorption models such as the Langmuir model, the Freundlich model and the BET model can be used to predict adsorption into monolayers or multi-layers. For example the BET isotherm model gives

$$\frac{n}{n_m} = \frac{c(p/p_o)}{(1 - p/p_o)[1 + (c-1)(p/p_o)}$$

where n = number of adsorbed molecules,
n_m = number of molecules adsorbed molecules at a surface monoloayer, (3.5)
c is a constant dependent on binding energies,
p is the partial pressure in the gas phase and p_o is the saturation vapor pressure.

This model can be used for gases such as Argon or Nitrogen i.e. for gases which do not interact with one another on a surface in a manner dependent on concentration.

Models are also available for evaluation of adsorption rates in terms of the "sticking coefficient" (which is a measure of collision probability with an empty site), molar mass and activation energy. The system reaches equilibrium when adsorption and desorption rates balance each other.

Chemisorption is caused by strong interactions including hydrogen bonding or covalent bonding between the adsorbate and the polymer. This process can occur at relatively low gas concentrations and can be irreversible. A finite energy barrier must be overcome for adsorption. This process can be highly specific. For example a PEM (Poly Ethylene Maleate) coated SAW device can be used to detect Cyclopentadiene. An illustrative response of this film to multiple vapors is shown in Fig. 3.1 [20].

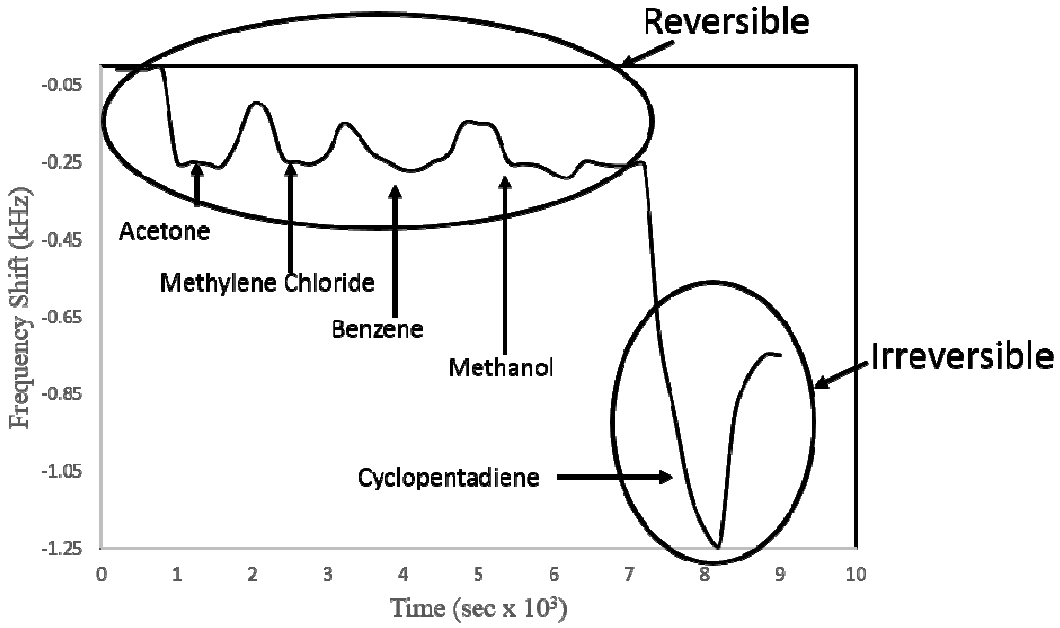

Figure 3.1: Physisorption and Chemisorption Mechanisms

Section 3.4 Sorption/Absorption Mechanisms

Linear solvation energy relationship (LSER) theory explains this mechanism. Vapor solubility properties are characterized and quantified by solvation parameters related to polarizability, dipolarity, hydrogen bond acidity, hydrogen bond basicity, and dispersion interactions. In terms of partition coefficients $K=C_s/C_v$ (ratio of gas concentrations in sorbent polymer phase and vapor phase repsectively), the frequency shift of a SAW device is given by

$$\Delta f_v = n\Delta f_s C_v K/\rho \tag{3.6}$$

Parameter n depends upon mass loading and polymer modulus change effects.

Partition coefficient K can be broken up based on various interaction mechanisms as follows:

$$\log K = c + rR_2 + s\pi_2^H + a\sum\alpha_2^H + b\sum\beta_2^H + l\log L^{16} \tag{3.7}$$

R_2, π_2^H, α_2^H, β_2^H and $\log L^{16}$ are solvation parameters characterizing the solubility of the vapor. A regression method obtained from measurements yields the partition coefficients (*s*, *r*, *a*, *b*, c and *l*).

LSER coefficients have already been tabulated for many compounds, and LSER equations derived from chromatographic measurements at 298 K have been reported for polymers which can be used on acoustic wave devices. A matrix of calculated log *K* values can be used to estimate sensor responses. Grate et al. [18] have outlined how classical least squares and inverse least squares approaches can be used to convert a matrix of log K values to a matrix of estimated sensor responses

assuming mass-loading responses Such estimates can be used to select polymers offering sensitivity to particular vapors and to estimate limits of detection.

Section 3.5 Summary

We have presented a brief overview of reaction mechanisms of analytes with sensitive coatings realized on SAW devices for sensor applications. In the case of polymer films the reaction mechanism could be diffusion, adsorption and absorption. Diffusion could be the result of a change in gaseous pressure when in contact with the film. Adsorption is the mechanism of surface adhesion of molecules to the film. In the case of chemisorption, such as when cyclopentadine is adsorbed by Poly-ethylene Maleate, the process is irreversible. Absorption mechanisms are broadly governed by vapor solubility properties which depend on polarizability, dipolarity, hydrogen bond acidity, hydrogen bond basicity, and dispersion properties.

The purpose of this overview is to get an understanding of the real time shifts in response of the SAW device when exposed to a broad range of analytes so that our design can serve this range.

Chapter 4: Sensor Readout Circuit Design

4.1 Introduction

The purpose of readout circuits incorporating SAW sensors is to measure the change in the SAW center frequency arising from a change in the acoustic wave velocity as a result of gaseous or liquid phase absorption.

The most accurate methodology is to use a single delay line and an external network analyzer to characterize the insertion loss and ascertain the passband peak response in loaded and unloaded states. This method has been used in laboratory settings with the goal of measuring the effectiveness of different piezoelectric and sensitive film thicknesses.

Among circuit based approaches dual delay line and single delay line based oscillator configurations have been reported. In these topologies the oscillator outputs are measured with external frequency counters.

A third approach uses a PLL in conjunction with the SAW device. The PLL configuration is reported to have more stability at the cost of a more limited frequency range and lower resolution.

In the following sections we discuss these topologies with case studies highlighting the function and typical performance of the component blocks.

4.2: Network analyzer based readout

External network analyzer based readout configurations are ideal for measuring resonant frequencies of SAW delay line or SAW resonator topologies. Such methods have been employed in [1] and [2] for example.

Krishnamoorthy et al. [1] reported two sets of devices designed for low insertion loss. One was designed for operation in the sub-GHz range (λ = 6.8 μm). The second was designed to achieve a fundamental frequency of operation in the GHz range (λ = 3.2 μm). The insertion losses of these devices were 3.4dB and 7.2dB respectively. Both were designed in Love mode configuration with $ZnO/SiO_2/Si$ layers. The high frequency *s*-parameters of the devices were evaluated using a HP8510C parametric network analyzer in the frequency range of 300 kHz and 3 GHz. Impedance matching to the load line of 50 Ω was achieved by optimizing the length of the transmission lines leading to the measuring pads and the thickness of the deposited Al. Linearity of frequency shift with respect to applied mass was reported in [1] for a Love mode IDT SAW sensor. Copolymer masses in the range of femto-grams were detectable by these sensors. Frequency shifts of 0.1MHz-4MHz were measured with the network analyzer for applied mass of 13fg-140fg.

Another example of a SAW sensor with a network analyzer readout topology is given in Kim et al. [5] who reported a Love mode $ZnO/SiO_2/Si$ SAW sensor passivated with Al_2O_3 for biofilm detection. Mass loading due to biofilm growth resulted in a frequency shift in the range of 300 kHz to 1MHz at a center operational frequency of 401-406 MHz. Real time resonant frequency monitoring was accomplished to measure bacterial biofilm formation using a custom package with the

capability of connecting the core sensor to the network analyzer with low impedance BNC cable connections. The device package was composed of a bacterial growth well, and a chip package connecting the sensor and BNC cables. The network analyzer was used to sweep a wide range of RF frequencies into the sensor and the device resonant frequency was analyzed. In this case the resonant frequency of the sensor was detected by measuring a low peak of the return loss. The data was read using a computer which communicated with the network analyzer via a GPIB bus.

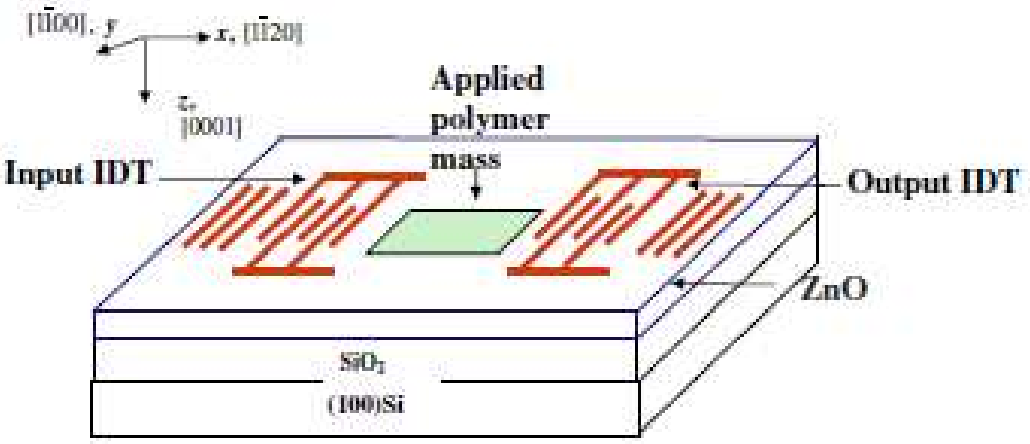

Fig. 4.1: Polymer mass measurement with Love mode sensor

Tigli et al. [8] have presented a CMOS-SAW biosensor for the detection of mammoglobin (hMAM). Post-processing steps were applied to the standard CMOS process to functionalize a Love mode ZnO/SiO2/Si SAW sensor on the wafer. An additional Au layer was patterned on the sensor. The insertion loss, center frequency, and phase responses of the sensor were measured with a wide spectrum, high-accuracy radio-frequency (RF) network analyzer operating in the range of 300 kHz-1300MHz. A micron-level RF electrical probing was used to access and characterize the CMOS-SAW devices. The measurement system included an RF synthesized source, transmission/reflection testset, multimode receivers, and display. The source

featured 1-Hz resolution, 40-ms sweep time, and up to 16-dBm output power. A ground-signal-ground (GSG) probe configuration was used. In the case of CMOS-SAW devices, the ground contact pads were shorted with on-chip metal routing. This pad provided a substrate contact for electromagnetic (EM) feedthrough suppression by grounding the substrate.

The mass sensitivities were analyzed by measuring center frequency shifts using the set up described. For a center frequency of 322MHz, the frequency change varied from the sub-kHz range to the MHz range depending on the type of applied mass. Reported mass sensitivities were 8.704 pg/Hz and 12.495 pg/Hz for the circular and rectangular devices, respectively.

Network analyzer based measurements represent the most accurate available methods of obtaining frequency shift, the limitation only being the resolution of the instrument. Taking advantage of this capability, reported sensors can operate in open loop mode. The drawback of such a readout is clearly the lack of portability and integration. In general, direct RF frequency measurements in open loop mode cannot be conveniently converted to a digital capable readout.

4.3: Oscillator based readout

As mentioned earlier, the main approaches in sensor design surveyed have been single and dual delay line oscillator systems. A block diagram of a single oscillator system in Fig. 4.2. A typical block diagram of a dual delay line oscillator sensor which combine two single oscillators is shown in Fig. 4.3.

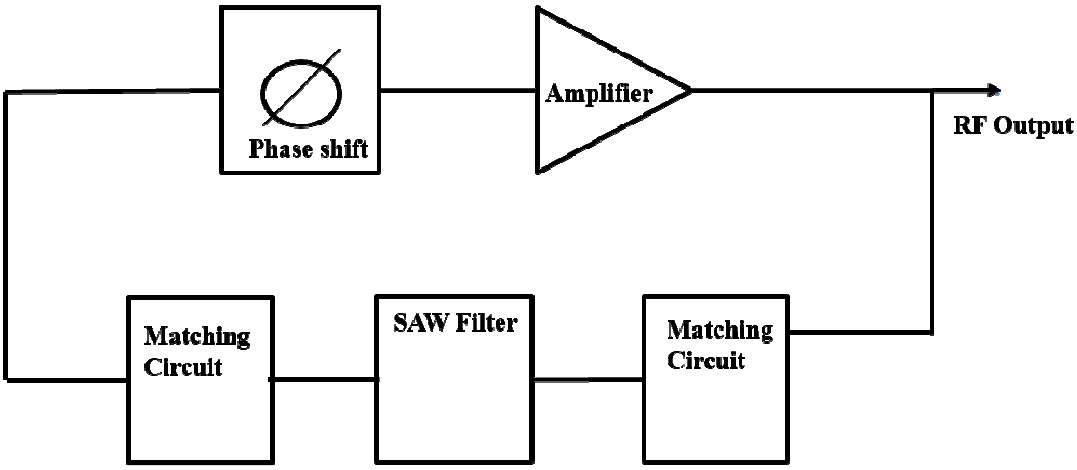

Figure 4.2: General SAW oscillator block diagram

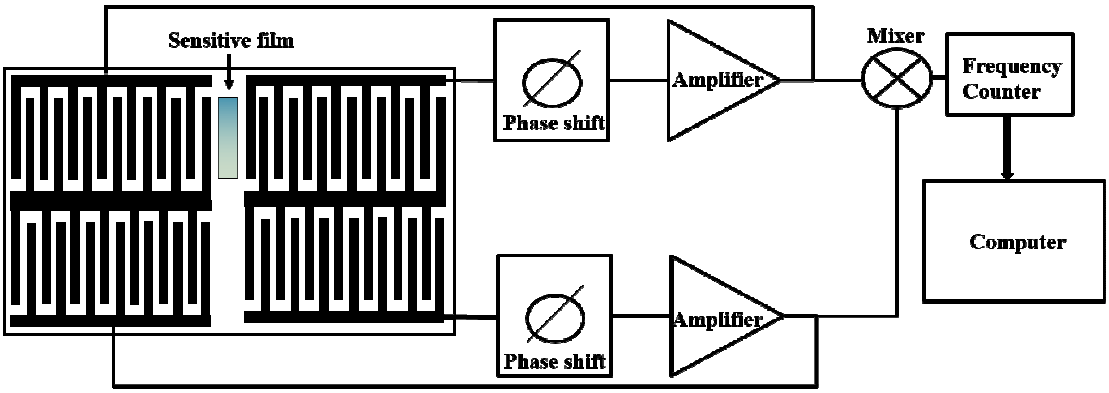

Figure 4.3: Oscillator Based Sensor Example

Oscillation will occur in the system shown in Fig. 4.2 if the loop gain exceeds unity and the phase shift is multiple of 360 degrees.

$$\phi_{SAW} + \phi_E = -2n\pi \qquad (4.1)$$

Here Φ_{SAW} and Φ_E represent the phase delays of the SAW device and the electrical circuit respectively. The integer n represents a given mode of oscillation.

In terms of the phase velocity v_p, the effective acoustic waveguide length, L, and the angular frequency, ω, we can express the SAW phase delay as

$$\phi_{SAW} = -\omega L / v_p \qquad (4.2)$$

Combining (4.1) and (4.2), the oscillation frequency is obtained as

$$\omega = (v_p / L)(2n\pi - \phi_E) \tag{4.3}$$

For a resonator configuration, because of the narrow response and rapid phase variation, (4.3) is satisfied at only one frequency. For a delay line, the bandwidth needs to be narrow enough for these two conditions to be satisfied at a given frequency.

Thus the oscillation frequency and also the stability of the frequency with respect to ambient parameters are critically dependent on the phase shifter in the loop [13], [14], [15]. There is thus inherent sensitivity to interconnect parasitic effects. Mode jumping issues may also be present (4.2) can be satisfied at multiple modes.

In the dual delay line scheme shown in Fig. 4.3 the mixer produces an output that is the difference of the two frequencies from the coated and the reference oscillator. The oscillator output is connected to a programmable frequency counter. The digital output can then be recorded and analyzed using a computer.

The drawbacks of the above configuration are that it requires an external measurement setup and also that the design of the phase shifter is extremely critical for proper functioning of the oscillator.

Wang et al. [24] have reported a dual delay line oscillator readout which operates on this principle. The SAW oscillation frequency was targeted to be 158MHz surface acoustic. Low insertion loss was implemented by Electrode Width Control Single Phase Unidirectional Transducer (EWC/SPUDT) configuration. Single mode selection was accomplished by a comb transducer [10].

The oscillator circuit incorporated a low gain amplifier, a phase shifter, a mixer and an LPF. The difference frequency was in the MHz range. This was measured using a programmable low frequency counter whose output was analyzed on a computer with a design specific software package. In addition, the insertion loss and phase response were measured using the UP 8753D network under matched conditions.

A calibration curve for DMMP gas established linearity of frequency response with respect to gas concentration at low concentrations. The measured frequency shifts ranged from 900 Hz to 2.6 kHz with a calculated sensitivity of 25 Hz/ mg/ m^3.

Fernandez et al [9] have reported an array of SAW sensors using ZnO over silicon substrates to detect low concentrations of different volatile compounds. The SAW gas sensors are equipped with different sensitive layers and preferential selectivities to various gases. A pattern recognition method is employed for selective chemical analysis.

Each individual sensor has its own delay line SAW oscillator operating on the principle outlined earlier. The central frequency of the delay lines was 210MHz and the propagation velocity of the SAW was 4200 m/s. The mass change caused by film deposition was detected by a shift of the oscillation frequency. This frequency was monitored with HP 8510B vector network analyzer during deposition, to monitor film thickness.

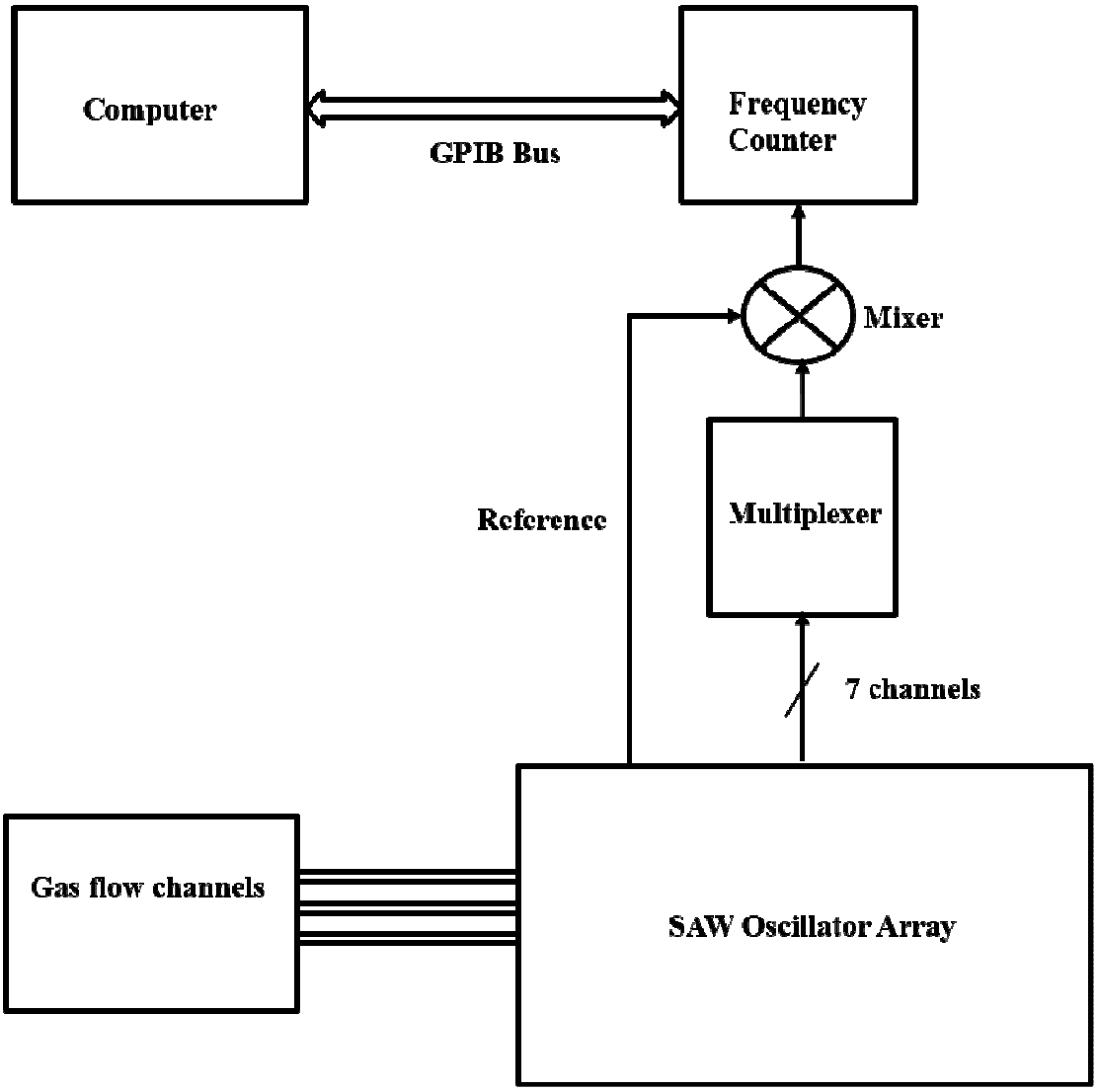

Fig. 4.4: Readout and measurement setup (Fernandez et al)

A schematic of the readout including the measurement system is shown in Fig. 4.4. The sensor array was formed by eight SAW devices, one of which was used as a reference. The frequency measured for each of the seven sensors is the difference between the frequency of the sensor and that of the reference device.

The devices were introduced into a test chamber in two rows on a printed circuit board. Different concentrations of volatile gases were introduced with concentrations between 20-500ppm. The sensor responses, in term of frequency

shifts, were measured with a frequency counter HP 53131A equipped with a high stability time-base. The counter received its input from a 7:1 microwave multiplexer switch connected to the sensor outputs. A computer system was connected via GPIB interface board to the frequency counter. This was used for the frequency display of the seven sensors and the reference. Data acquisition and processing gave the frequency of each device and the frequency shift with respect to the reference.

The measured frequency shifts produced by the different polymers deposited on sensors were in the range between 200 kHz and 500 kHz. Different concentrations of octane, toluene, and methylethylketon were detected at room temperature. Discrimination among these gases was then identified based on the distinct time signature of these gases. The separation among the gases was extracted from principal component analysis plots. In addition, a neural network was trained and validated to classify the gases.

Chiang et al. [10] have also reported a gas sensor array based on SAW oscillator devices with polymer coatings. The IDT substrate was $LiNbO_3$ (YX). The operating center frequency of SAW was 117.4 MHZ and the reported frequency shift was 800Hz for ammonia gas concentration of 150ppm. The complete gas sensing consisted of a sensing chamber which incorporated the gas steel cylinder, a mass flow controller, mixer, SAW oscillator array, power supply, function generator, frequency counter and monitor. Real time readings from the frequency counter were used to record the frequency shifts for alternate cycles of gas flow and air injection.

Pasternak [11] has reported a variation of the SAW oscillator which operates at a harmonic of the resonant frequency. This presents the possibility of higher mass

sensitivity based on proportionality of such sensitivity to the square of the operating frequency. In this case the oscillator circuit was reported to operate at the 29th harmonic of the loaded resonator resulting in a frequency of 4.71GHz. Another advantage of operation at this frequency is the possibility of using distributed microstrip based matching circuits and phase shifters.

The dual oscillator system is structured as a λ-length asymmetric microstrip ring with λ/4 short-circuited stubs halfway to the amplifier input of the amplifier. The purpose of the stub is to introduce a low impedance into the ring for undesired harmonics, thus preventing oscillation. The input and output resistance of both amplifier and resonator are equal to 50 Ω which matches the microstrip line characteristic impedance. In addition, the amplifier is selected to have a sharp roll off in order to permit operation at one harmonic. The amplifier also needs to provide a sufficient signal level to the mixer. The topology of each oscillator system with distributed components is shown in Fig. 4.5.

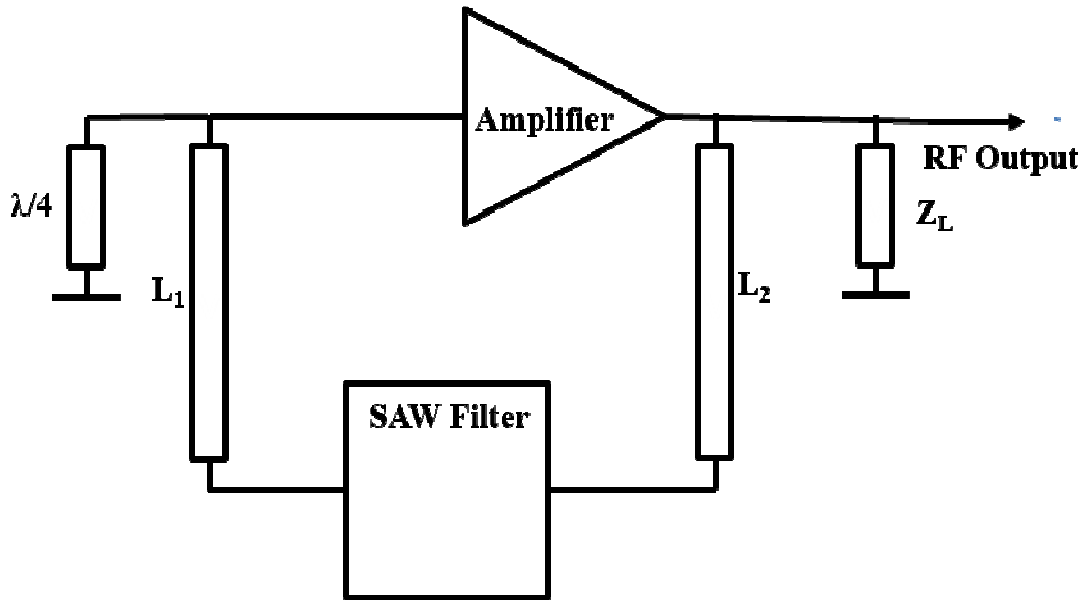

Fig. 4.5: Oscillator topology with distributed microstrip components.

The oscillator output was monitored with an HP-8593E spectrum analyzer and a TED-10-CM digital-frequency meter. The undesired harmonics were suppressed below −30 dBm. For Dimethylmethyl-phosphonate (DMMP) gas flow, a frequency shift of 2 kHz was measured for a concentration of 25ppm.

4.4: Transponder based measurements

Luo et al. [7] have reported an integrated passive impedance-loaded SAW H_2S sensor. The sensor comprised a SAW transponder based on a delay line structure and a resistive H_2S impedance-loaded component. The SAW delay line was fabricated on a 128° LiNbO3 substrate with a center frequency of 233 MHz. The principle is that resistivity of the film changes several orders of magnitude after the film is exposed to the gas. As a result the measured return loss will vary, with the magnitude increasing with decreasing load resistance.

The readout unit consists of a network analyzer and a 233 MHz dipole antenna. A pulse transmitted from the readout is received by the spiral antenna and sent to the transmitting/receiving IDT. The signal is then propagated to the SAW and partially reflected by the reflecting IDT. The reflection coefficient varies with the resistance variation of the external gas sensor. The network analyzer with a Visual Basic interface processes the reflected signal and records return loss of the signal every two seconds thus providing real time monitoring.

The sensor was exposed to gas and air alternately. The average change of the relative return loss was 2.51 dB in response to 50ppm gas flow. The calculated range of the loaded resistance was in the range of 100Ω to 10,000Ω. Wireless measurement demonstrated linearity of the return loss with respect to the gas concentration.

4.5: Digital Readout

The development of digital readout electronics for SAW sensors has been rare. Hao et al. [6] have presented one such readout which can be considered a benchmark in this technology.

The topology incorporates multiplexed oscillators and readout electronics. The SAW sensor array was fabricated on YX-LiNbO3 substrate. The center frequency of the SAW devices was 99.8 MHz. Seven polymers were coated on the sensing areas. The SAW array was controlled by a multiplexing technique. Sensor signals were obtained by readout electronics and further analyzed with an 89C51 microprocessor.

The readout module incorporates a 24 bit counter at the output of the SAW device. This is the main converter in the module. The total sampling time of the counter is set to 0.12 s. A second counter is used to control the D flip–flop which stores the data from Counter 1 until ready for collection by the 89C51 microprocessor. A system clock is used to enable the counters and reset the previous data. A second clock (CLK2) triggers Counter 2 which, in turn, clocks the D flip-flop after activation of Counter 1. The microprocessor processes the data from the D flip-flop and stores real time SAW sensor frequency in memory. The comparison of the measured frequency with a reference frequency gives the frequency shift which is displayed in a LCD display module. A block diagram of the topology is shown in Fig. 4.6.

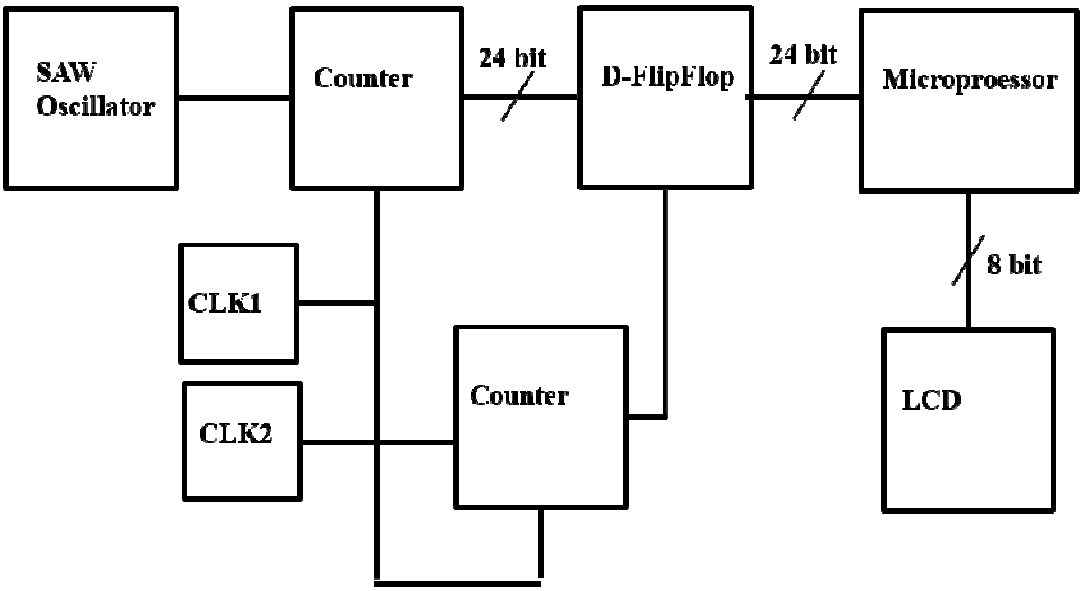

Figure 4.6: Oscillator topology with digital readout (Hao et al.)

Though using a readout module with relatively high resolution, the system still used external feedback amplifiers in the oscillator circuits. Integration of the readout onto a single chip was not reported.

The average frequency shift depended on the polymer coating as well as the gas injected. This shift was in the order of 10 kHz. A two-way hierarchical clustering was used to extract and analyze data from the SAW oscillator array. The goal was to recognize the signatures of different families of gases.

4.6: PLL based SAW sensor

Phase detector and PLL based SAW sensors both rely on a comparison of the SAW device output to a reference phase. The block diagrams of these topologies are presented in Fig. 4.7 and Fig. 4.8. Both of these provide better stability compared to the oscillator based topology since they avoid mode hopping possibilities [14].

The phase detector based sensor operates essentially in open loop mode. Hence it requires a signal generator or oscillator operating in a fixed frequency range to provide a reference phase. The oscillator output is also processed by the SAW sensor device which is typically configured as a delay line. The phases of these signals are compared using a phase detector which might use a mixer topology, for instance. This output is passed through a low pass filter which converts the phase difference to a voltage output. A change in phase delay as result of mass loading will be reflected in the low pass filter output.

The PLL based topology operates in closed loop and incorporates a VCO which is tuned by the low pass filter output. The function of the phase detector is, again, to convert a phase difference between the VCO output and the SAW delay line output. Because of closed loop operation, a constant phase difference is maintained. This difference changes in the event of mass loading. The loop filter controls the stability and response time of the loop. In addition to a voltage output, this architecture also provides a frequency counter output which provides better resolution than the open loop phase detector sensor..

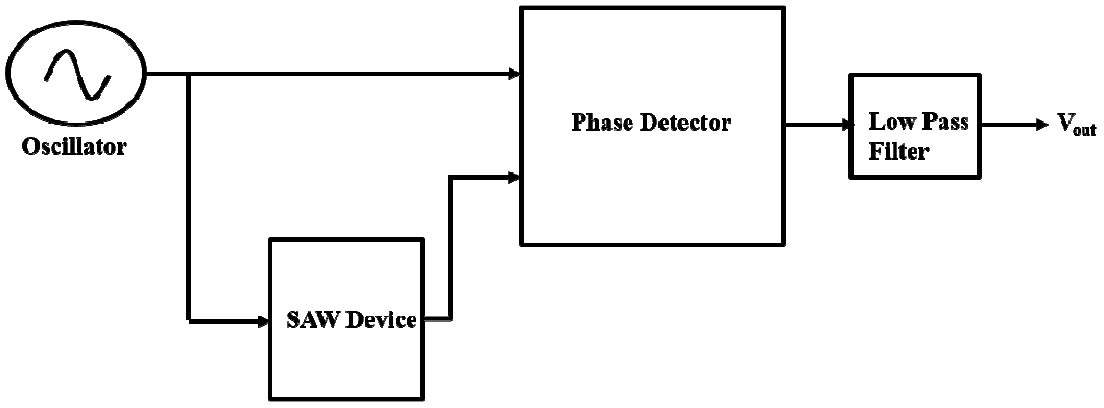

Figure 4.7: Phase detector based SAW sensor

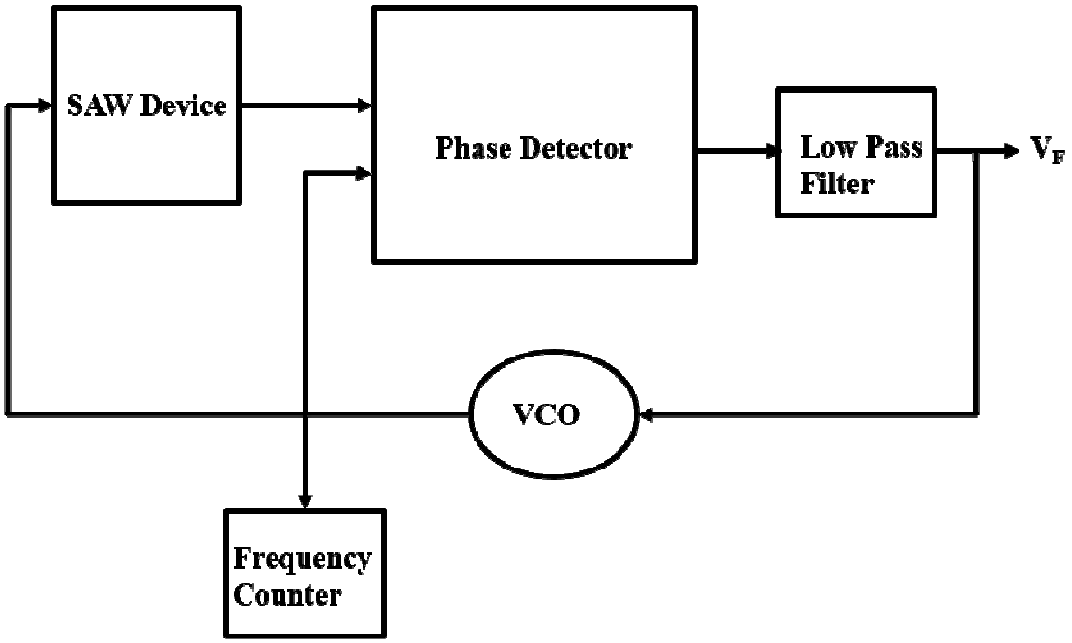

Figure 4.8: PLL based SAW sensor

A particular variation of the PLL based sensor has been reported by Sternhagen et al. [12]. This variation uses a direct digital synthesis (DDS) based system which provides a digitally controlled VCO output. The digital VCO incorporates an analog-to-digital converter (ADC), a microcontroller, a DDS integrated circuit, and a loop filter. Such control is reported to have the advantages of a programmable frequency range. It also allows for large SAW sensor insertion losses.

In this implementation the SAW frequency range was 80 MHz to 125 MHz. The output of a phase frequency detector (PFD) was sent to a loop filter and signal conditioning circuit whose output was digitized by a 12 bit ADC. The system output was measured by a HP model 53131A frequency counter connected to a PC via a GPIB.

The sensor was tested for temperature and relative humidity variations. Relative humidity was varied from 0 to 100%. The digital VCO had a center frequency of 99.93 MHz and a dynamic range of 60 kHz. The observed frequency shift in response to relative humidity variation ranged from 200 Hz to 1.25 kHz. The response to temperature variation was more significant with a 155 kHz shift observed for a 30C temperature change. The frequency shift was observed to be linear with respect to temperature shift.

4.7: Summary

We have presented an overview of available readout topologies that have been used for sensors based on SAW devices. The most accurate method is to use an external network analyzer in open loop configuration. In such cases the resolution is determined by the specification of the calibrated instrument and is of the order of 10Hz. Several articles have demonstrated this technique for sorption of liquid based and gaseous media. By its very nature, this method is not suitable for integration or portability.

Single and dual oscillator topologies represent the most extensively reported configurations for SAW sensors. The advantages are relative simplicity of the design and the elimination of an RF source for excitation. In addition, a mixer can be used to downscale the frequency, measuring only the shifts in the presence of an analyte. This configuration has the disadvantages of requiring an external frequency counter and susceptibility to mode hopping.

Another class of readouts use wireless measurement using a SAW device configured as a transponder. The return loss variation in the presence of resistance

changes can be measured to estimate the amount of gas absorbed. The advantage of remote sensing has made this topology popular. Such a wireless system requires the SAW resonator or delay line to be at a distance from the interrogating readout, thus precluding compactness in the setup.

A digital readout topology using a counter at the output if the SAW oscillator has been reported. While presenting a high resolution digital output this topology relies on both an oscillator and a microprocessor which would complicate monolithic integration.

The last topology discussed is phased detector and PLL based readouts. These are architecturally closest to the readout that has been presented in this thesis, though with significant differences. In the topology we propose, the loop is controlled by a finite state machine. In addition, the reported PLL based architecture, differs from a stable PLL design in that there is no reference clock. Both phase and amplitude of the SAW oscillator could be in unknown states during startup leading to problems with lock acquisition. These complications have not been addressed in the reported designs.

Chapter 5: Readout Architecture

5.1 Introduction

In this work we report a novel read-out circuit for an integrated CMOS SAW sensor which produces a voltage output the average DC value of which responds to changes in SAW velocity due to analyte-sensor interaction. The primary novelty of the design lies in a loop architecture incorporating a dual control VCO, a SAW sensor and a finite state machine. The fine control of the VCO depends on the instantaneous response of the SAW device through a feedback path resulting in a well defined output voltage accurately tracking sensor behavior in real time. In a second layer of conversion the design the loop sensor output is converted to a digital readout. This is accomplished by using the timing information embedded in the existing FSM outputs and adding a second FSM in the conversion circuit. This topology avoids loss of resolution resulting from buffering of the analog signal for use in switched capacitor based conversions.

In previously reported oscillator based designs, the oscillation frequency and also the stability of the frequency with respect to ambient parameters are critically dependent on the phase shifter in the loop [13], [14], [15]. Since, in our design the SAW device with matching networks is not part of the high frequency loop, there is little sensitivity to interconnect parasitics. We can rely on the accuracy of on-chip parasitic extraction for a given fabrication process allowing more robust modeling and simulation capabilities. Additionally, this low frequency loop architecture

precludes mode jumping issues found in designs incorporating the SAW delay line or the resonator in the feedback loop of an amplifier.

In the following sections the design, simulation and experimental verification of the novel frequency-to-voltage conversion read-out IC circuit will be presented and discussed.

5. 2 Top Level Architecture of Primary Sensor Loop

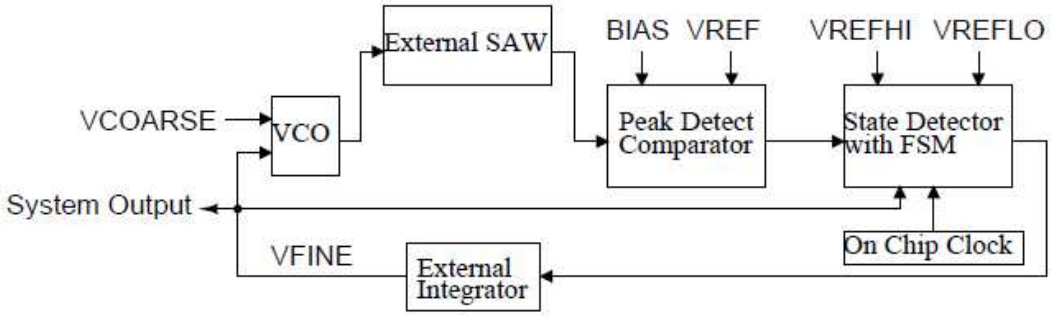

Figure 5.1: Primary Sensor Loop Block Diagram

The FSM based read-out is implemented in two layers. The communication between the two layers occurs via the FSM and the comparator outputs. The primary loop sensor loop block diagram is shown in Fig. 5.1. Considering this block diagram, the VCO has two control inputs. The coarse control is set so that the open loop frequency falls within the SAW bandwidth when the fine control is in the middle of its range. An on-chip buffer delivers the VCO output to the matched input of an external SAW delay line filter which can be wire-bonded to the chip. When the loop is closed as shown, the VCO output frequency varies between limits dependent on the device passband, the SAW phase delay, the RC filter time constant and the VCO gain. The SAW output frequency is centered at the upper edge of the passband. This output is fed to a peak detecting comparator with hysteresis whose output is high if

the frequency is in the passband. The comparator output serves as input to a finite state machine which also receives the VCO fine input. Each toggle of the comparator output causes a state transition in the FSM. These transitions cause the VCO ramp input to reverse slope and this, in turn causes the VCO output frequency to enter and exit the passband. The average value of the VCO fine ramp thus serves as the system output. Two additional comparators provide reset and clear functionality to bring the ramp to the working band from its initial high or low state. A finite state machine ensures correct transitions between states.

5. 3 Top Level Architecture of Secondary Sensor Loop

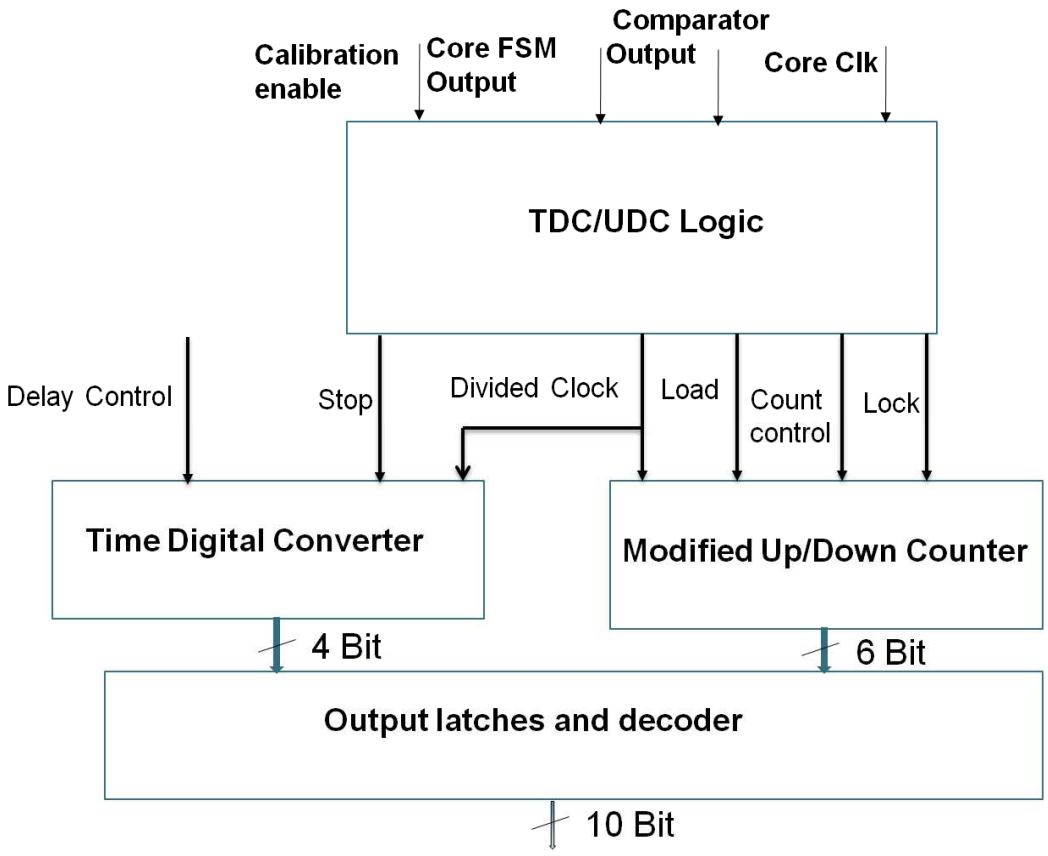

Figure 5.2: Digital Conversion of Sensor Output

In the second layer of conversion, the analog sensor output is converted to an equivalent 10 bit digital output. The block diagram of this read-out phase is shown in Fig. 5.2. The FSM and comparator outputs from the primary sensor loop are fed into a digital control logic block which generates control inputs for a 4 bit time to digital converter (TDC) and a 6 bit modified up/down counter (UDC). The UDC counts up or down when the comparator output is high while remaining locked at other times. The TDC provides a finer resolution of the delay from the count clock to the comparator output. Combining these two digital buses, we obtain a digital representation of the total charge up time of the external filter. As will be derived subsequently, the average sensor output is a function of this charge up time.

Section 5.4 Summary

In this chapter we have presented a high level view of the proposed sensor readout architecture. We have divided the architecture into primary and secondary loops. The primary loop contains the core of the design, incorporating a VCO, a peak detecting comparator, a finite machine, an external RC filter and the SAW device. In steady state the loop ensures that the VCO frequency is centered at the upper edge of the passband. The average valued of the VCO fine voltage input serves as the system output.

The secondary readout takes advantage of the FSM and comparator outputs of the primary loop to convert the SAW phase delay to an equivalent digital bus. The bus consists of a modified counter output and a time to digital converter output. A logic and FSM block handles the interface between the two architectural sections.

Chapter 6: Design and Analysis of Primary Sensor Loop

Section 6.1 Voltage Controlled Oscillator (VCO)

The VCO has a cross coupled current controlled ring topology whose coarse input (V_C) directly controls the stage pull-up current. A decrease of the coarse control voltage results in increased stage current and, therefore, faster slew rate. The fine input (V_F) controls the stage delay through voltage dependent NMOS capacitors, MC1 and MC2. An increase in the fine control voltage will result in higher load capacitance. Thus both V_C and V_F have an inverse relationship with the ring oscillation frequency. The cross coupling leads to a pseudo-differential output structure. This topology leads to better duty cycle control compared to a non-coupled current starved inverter stage. The VCO frequency variation with respect to the fine input is shown in Fig. 6.1. The sensitivity from simulations is 52MHz/V for TSMC 0.35µm models (Figure 6.2). For AMI 0.5µm models, the typical sensitivity is 16MHz/V.

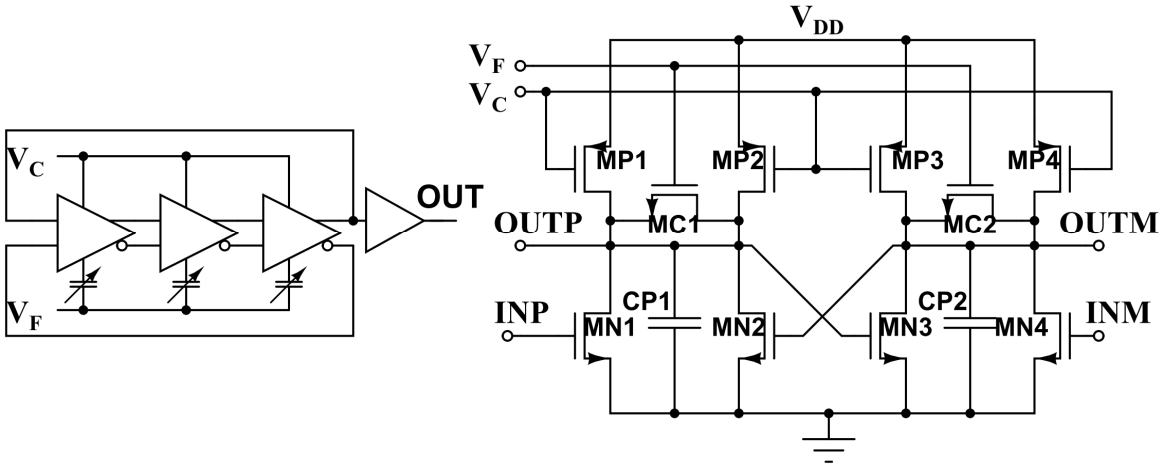

Figure 6.1: VCO with Coarse and Fine Controls

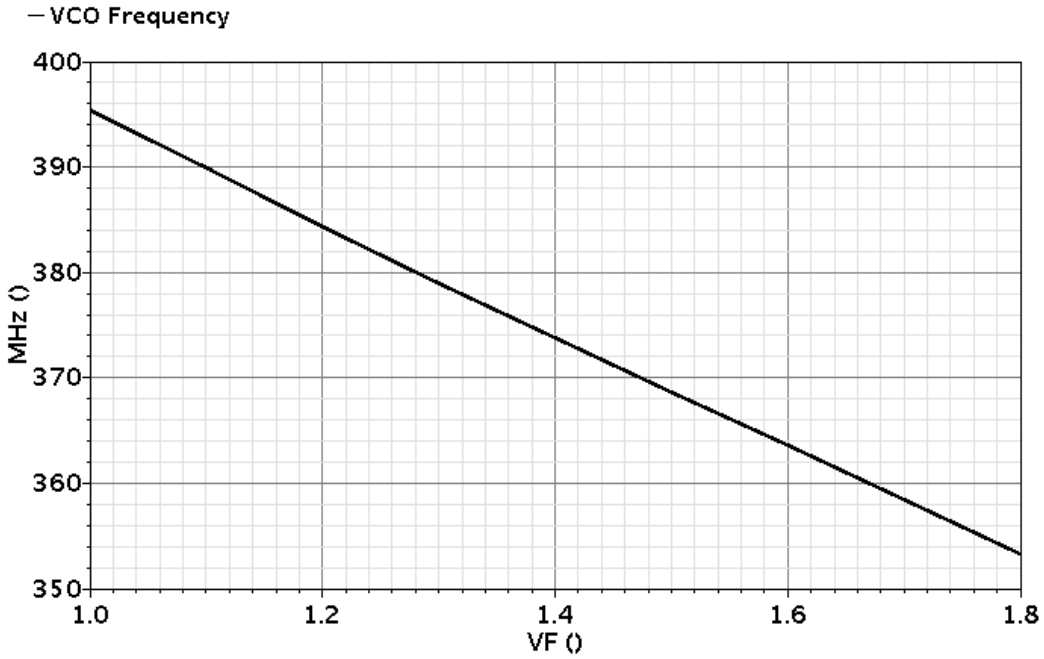

Figure 6.2: VCO Frequency versus Fine Input Voltage

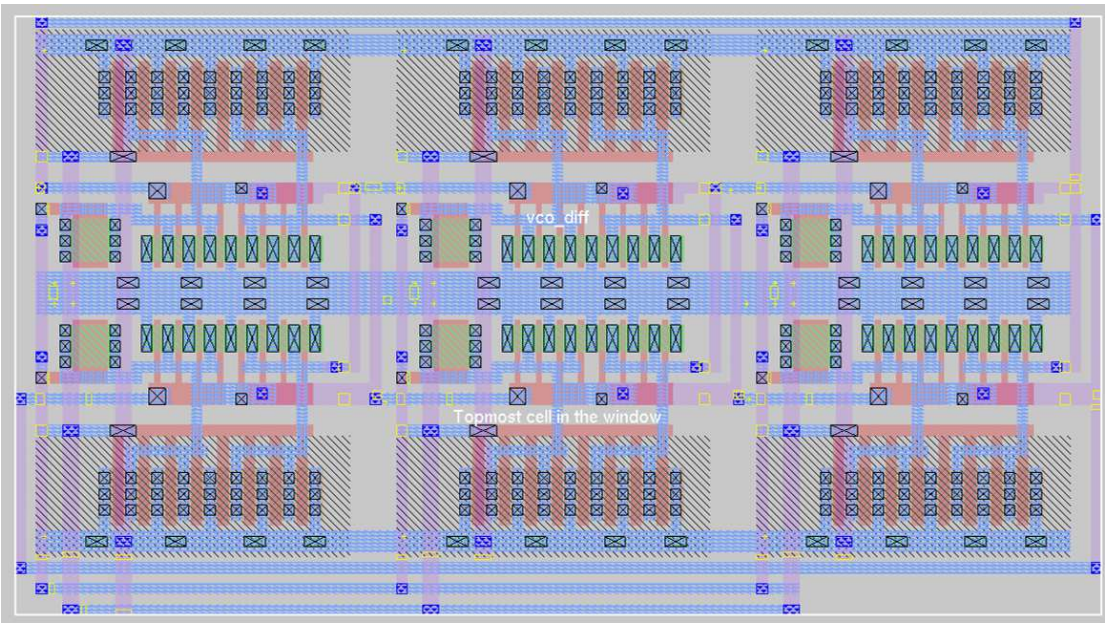

Figure 6.3: VCO Layout

The layout of the VCO is shown in Fig. 6.3. The routing uses two metal layers. The cross coupled cells are physically inverted to minimize layout area.

6.2 Surface Acoustic Wave Device Model and Properties

Our readout topology is best targeted for low loss interdigitated (IDT) SAW sensors, such those reported in [1] and [2], that have high electromechanical coupling coefficient (K^2). A band-width capability of a few MHz is considered here, as shown for example in Fig. 6.4, although higher band-widths are easily adaptable. Other examples of suitable SAW sensors are given in Kim et al. [5] who reported a Love mode $ZnO/SiO_2/Si$ SAW sensor passivated with Al_2O_3 for biofilm detection. Mass loading due to biofilm growth resulted in a frequency shift in the range of 300 kHz to 1MHz at a center operational frequency of 401-406 MHz. Linearity of frequency shift with respect to applied mass was reported in [1] for a Love mode IDT SAW sensor. It will be shown from simulation and experimental results that the proposed circuit can easily track frequency shifts of this order.

To illustrate typical responses of low loss unloaded and loaded IDT SAW devices, the crossed field model [3] of a SAW filter was developed using MATLAB and the resultant s-parameter model was used in the circuit simulator. The reference and loaded transfer function of the modeled device on a $ZnO/SiO_2/Si$ structure with an aperture of 50λ, separation of 100λ and a 70 finger pair IDT is shown in Fig. 6.4. The electromechanical coupling coefficient and velocity were obtained from [18] and [1] for modeling purposes assuming normalized guiding layer thickness $h/\lambda<0.02$.

For entire system simulation we have used the s-parameter models of commercially available SAW devices from Triquint [21], [22], [23]. These devices are centered at 374 MHz, 140MHz and 70MHz with corresponding insertion losses of

5dB 7.5dB, and 7.5dB respectively. The last two devices were also used for experimental verification and comparison with our simulation results.

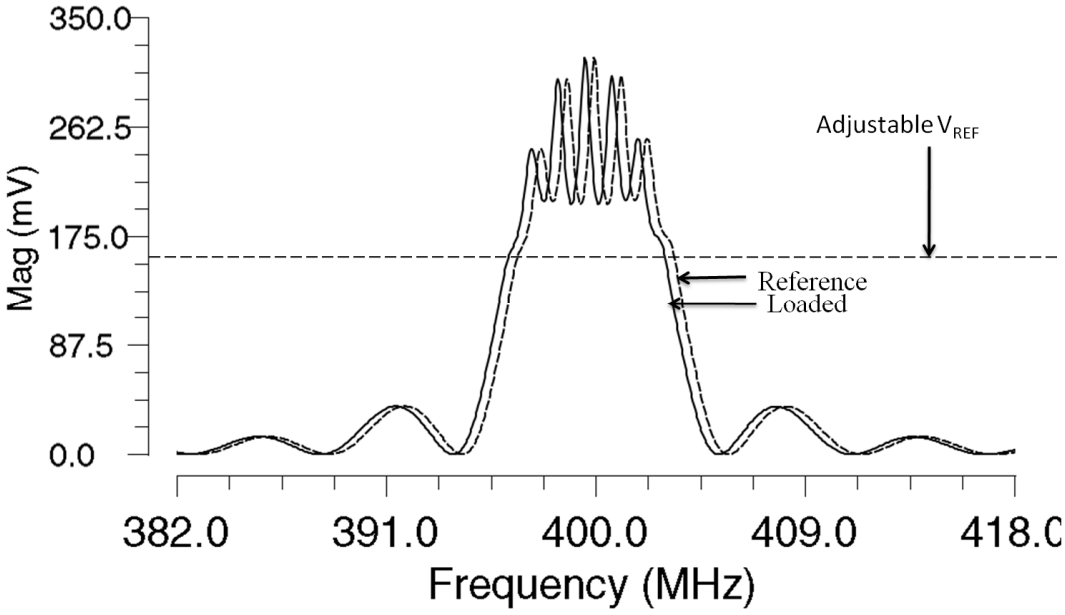

Figure 6.4: Illustrative response of loaded and unloaded data lines.

6.3: Open Loop Response of SAW-VCO

To understand the primary loop behavior as depicted in the block diagram in Fig. 5.1, we first consider only the VCO and SAW devices and sever the loop at the output of the SAW. We now consider a ramp input at the fine input of the VCO such that ramp is centered at a voltage that corresponds to the SAW center frequency. In addition, let the ramp endpoints be voltages for which the corresponding frequencies lie outside the SAW passband. For this test case we use an idealized model of the VCO with the following function.

$$V_{out}(t) = V_o \sin(2\pi \int_o^t (f_c + a(V_{in}(\tau) - V_{ref})d\tau) \qquad (6.1)$$

where a is the gain of the VCO.

If the VCO input is a ramp, VCO output will be a frequency modulated waveform. Under this stimulus, the simulated SAW response is obtained as follows:

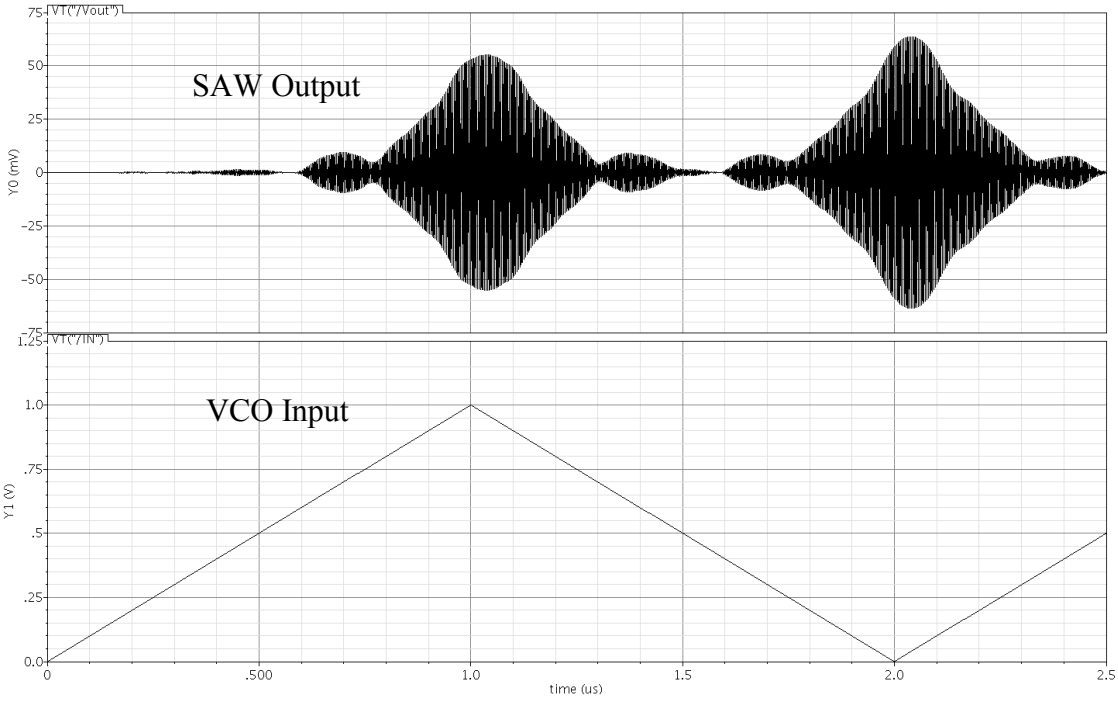

Figure 6.5: SAW Response to VCO

Clearly, since the frequency at the SAW input is a varying transient, the SAW output peak voltage will also vary and will attain a maximum when the input frequency is at the band center. Additionally, because of the phase delay due to the separation of the IDT devices, the peak of the output occurs after the time needed by the surface acoustic wave to traverse this distance.

If now the SAW velocity decreases due to mass loading, the center frequency of the delay line will also shift in the same direction. Hence, for the same ramp input, the peak will be attained at an earlier point of time. At the same time, the phase delay between the IDT centers will shift in the opposite direction. However, the latter effect

will be minimal if the input ramp is sufficiently slow i.e. by lowering the VCO gain. This will also increase the sensitivity of the system to small changes in frequency.

To simulate the effect of mass loading we first build a model of the shifted frequency response (caused by a shift in velocity) using MATLAB. The responses of the reference and the mass loaded IDT devices are plotted in Figure 6.4. This model has a more exaggerated shift than might be observed in real time sensor applications and is used only to illustrate the concept.

Next we use the two port models of these two devices and simulate the transient response to a VCO input. The response is shown in Figure 6.7. We note that the peak of the loaded device is attained about 31ns earlier for the loaded device compared to the unloaded one. This delay and hence the resolution can be improved by slowing the slew rate of the VCO input.

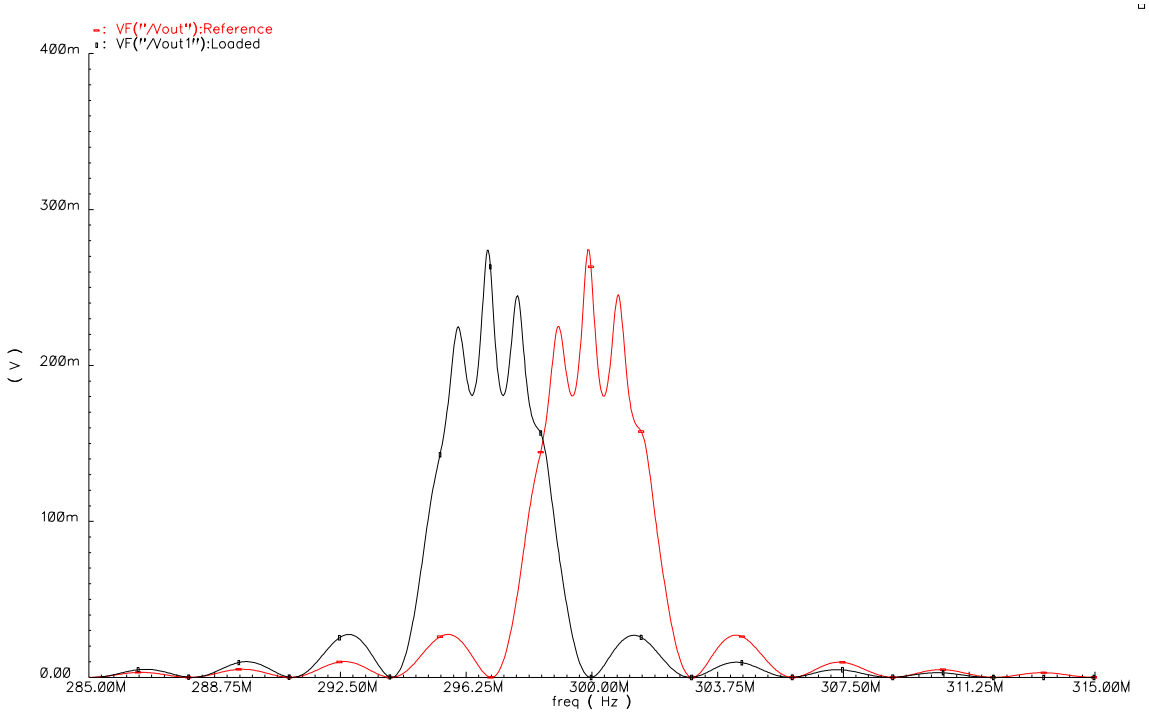

Figure 6.6: Response of loaded and unloaded IDTs

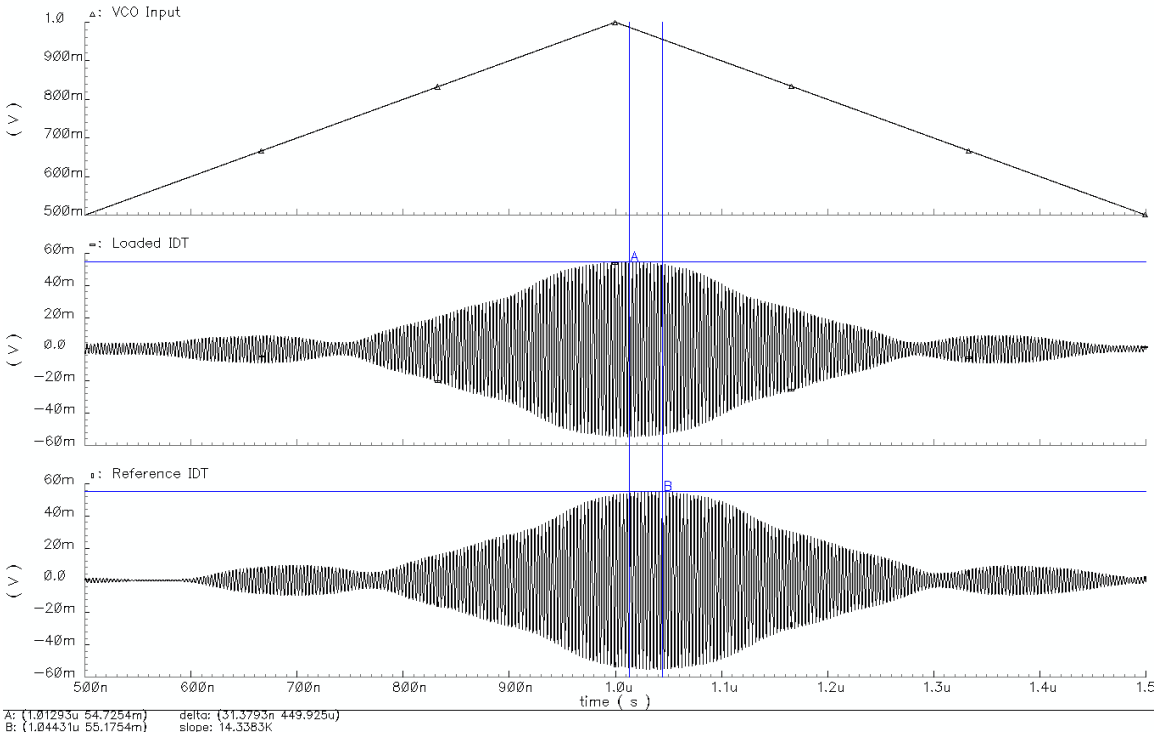

Figure 6.7: Transient responses of loaded and unloaded IDT

6.4; Peak Detecting Comparator

In a conventional comparator we expect the output response to be high when the positive input is greater than a given threshold within a certain offset. In this case we are, however, interested in an output which would only trigger high if the peak amplitude of the input is above a certain user programmed threshold. Considering the SAW frequency response as shown in Fig. 6.4, this implies that the comparator output would be high if the peak is above $V_{REF.}$ This further implies that if the SAW device and the comparator blocks are considered together as one system, then the system output would be high only if the time varying SAW output frequency is within the frequency band defined by the intersection of the V_{REF} line with the SAW frequency

response. An increase in V_{REF} would increase the sensitivity of the system. However, this would raise the requirements on comparator speed restricting operation at lower process nodes. In addition, the system would also risk approaching the pass-band ripple low voltage. In this design the threshold has been left adjustable or trimmable by the user for finer optimization.

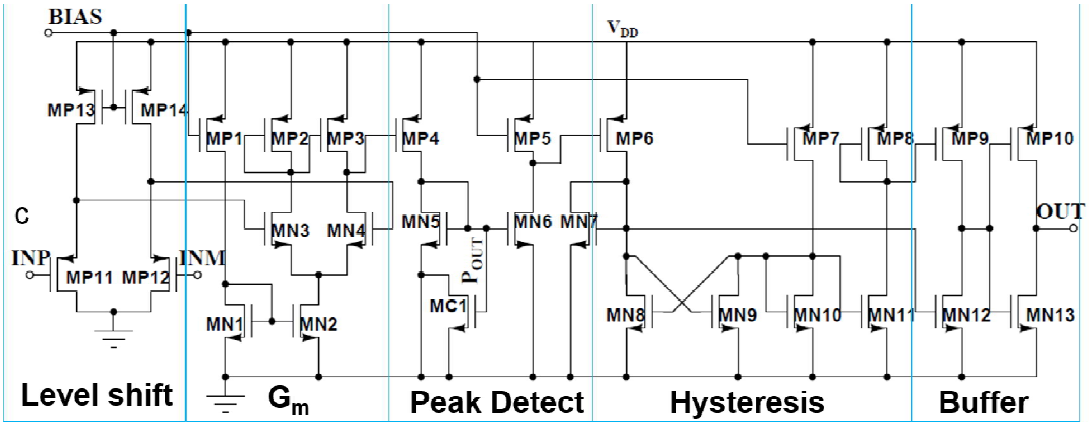

Fig. 6.8: Peak detecting comparator

Shown in Figure 6.8 is the circuit schematic of the entire peak detecting comparator. The W/L ratios of the individual devices can be found in Table 6.1. The circuit can be roughly compartmentalized into five stages. In the first stage, a DC level shift is added to the input. The second stage is a differential transconductance stage. In the third stage, the core peak detection occurs through an NMOS varactor. The fourth stage is a hysteresis stage where residual high frequency ripple is removed. In the fifth stage there is a buffer which provides full swing for use in the finite state machines. The operation of these stages is now described in detail.

Table 6.1: Transistor W/L ratios in Peak Detecting Comparator for AMI 0.5µm process.

Device	W/L (µm/µm)	Type
MP1	12/0.6	PMOS
MP2	12/0.6	PMOS
MP3	12/0.6	PMOS
MP4	12/0.6	PMOS

MP5	12/0.6	PMOS
MP6	12/0.6	PMOS
MP7	12/0.6	PMOS
MP8	12/0.6	PMOS
MP9	12/0.6	PMOS
MP10	36/0.6	PMOS
MP11	12/0.6	PMOS
MP12	12/0.6	PMOS
MP13	12/0.6	PMOS
MP14	12/0.6	PMOS
MN1	9/0.6	NMOS
MN2	36/0.6	NMOS
MN3	12/0.6	NMOS
MN4	12/0.6	NMOS
MN5	1.2/6	NMOS
MN6	36/0.6	NMOS
MN7	6/0.6	NMOS
MN8	12/0.6	NMOS
MN9	12/0.6	NMOS
MN10	6/0.6	NMOS
MN11	6/0.6	NMOS
MN12	6/0.6	NMOS
MN13	12/0.6	NMOS
MC1	72/3	NMOS

6.4.1 Input Level Shift:

This stage is comprised of the PMOS devices MP11, MP12, MP13, and MP14. The SAW output which serves as the input to the comparator stage has no DC component because of its band pass response. To shift the common mode for use in the subsequent NMOS differential pair stage, a level shifter in the configuration of a PMOS divider is employed. After level shifting the common mode, by inspection is obtained as

$$V_{CM} = V_{DD} - V_{BIAS} \qquad (6.2)$$

6.4.2 Transconductance Stage

This stage consists of the differential pair, MN3/MN4, the tail current mirror, MN1/MN2 and the PMOS active load pair MP2/MP3. Since this is a high speed stage, the devices have been chosen as minimum length. The stage transconductance is a function of the width of the differential pair devices and the tail current which, in turn, is controlled by the bias voltage V_{BIAS}.

6.4.3 Peak Detection Stage

This stage consists of the branch MP4/MN5 and the NMOS capacitor MC1. Current pulses are injected into MC1 for every fractional positive cycle during which $V_{INP}>V_{INM}$. Hence, if the instantaneous input frequency is in the SAW passband, node P_{OUT} will be charged in successive cycles till the drain output of the strong N, weak P pair (MN6/MP5) is pulled low. On the other hand, in the stopband region there will be no current injection into node P_{OUT} which will discharge via MN5 pushing it to subthreshold. We now analyze the peak detect stage in a state where high speed comparator input has sufficient amplitude to toggle the output of the transconductance stage and, therefore, the current through MP4. In this state the NMOS capacitor will charge and discharge in alternate cycles. In the charge cycle the current through MP4 will inject charge into MC1. Let this current be denoted by a step approximation, I_P. This will be valid if the g_m of the differential pair and the injection device MP4 are high. Further, let the peak voltage at the end of the charge cycle be denoted by V_1 and the minimum voltage at the end of the discharge cycle be denoted by V_2. In addition, let the corresponding overdrive voltages of MN5 be denoted by V_{ov1} and V_{ov2}. Then, during the discharge cycle, we have

$$C\frac{dV_{ov}}{dt}+\frac{\beta V_{ov}^2}{2}=0 \qquad (6.3)$$

Solving this differential equation for the time varying overdrive voltage,

$$V_{ov1}-V_{ov2}=V_{ov1}V_{ov2}\beta T_2/C \qquad (6.4)$$

Here T_2 is the discharge period. On the other hand, during the charge cycle,

$$C\frac{dV_{ov}}{dt}+\frac{\beta V_{ov}^2}{2}=\mathrm{I_p} \qquad (6.5)$$

Linearizing this equation in the neighborhood of the mean, we get

$$I_p=C(V_{ov1}-V_{ov2})/T_1+V_{ov1}V_{ov2} \qquad (6.6)$$

where we have used the geometric mean of V_{ov1} and V_{ov2}

$$V_{ovm}^2=(V_{ov1}V_{ov2})^{1/2} \qquad (6.7)$$

Combining these equations we obtain,

$$V_{ovm}=(2\eta I_p/\beta)^{1/2} \qquad (6.8)$$

where $\eta = T_1/(T_1+T_2)$ is the duty cycle of the switching waveform.

$$V_{ov1}-V_{ov2}=\beta V_m^2 T_2/(2C) \qquad (6.9)$$

Further simplification leads to an expression of the voltage variation in terms of the peak current and the switching frequency, f.

$$V_{ov1}-V_{ov2}=\eta(1-\eta)I_p/(fC) \qquad (6.10)$$

It is clear from this above equation that the mean voltage increases with the duty cycle of the current switching waveform which, in turn, depends on the positioning of the comparator threshold with respect to the common mode voltage of the high frequency input in the transconductance stage.

Fig. 6.9 illustrates a charge sequence during which the amplitude of the input (node INP) is gradually increased. Since, in this example, the threshold voltage (node INM) remains fixed, the duty cycle decreases as the duration of excursions below this threshold increases. The mean voltage at node P_{out} also decreases which is in accordance with equation (6.8). In addition, the peak to peak swing increases as the duty cycle approaches 0.5 and the charge current also increases. These behaviors are also consistent with equation (6.10).

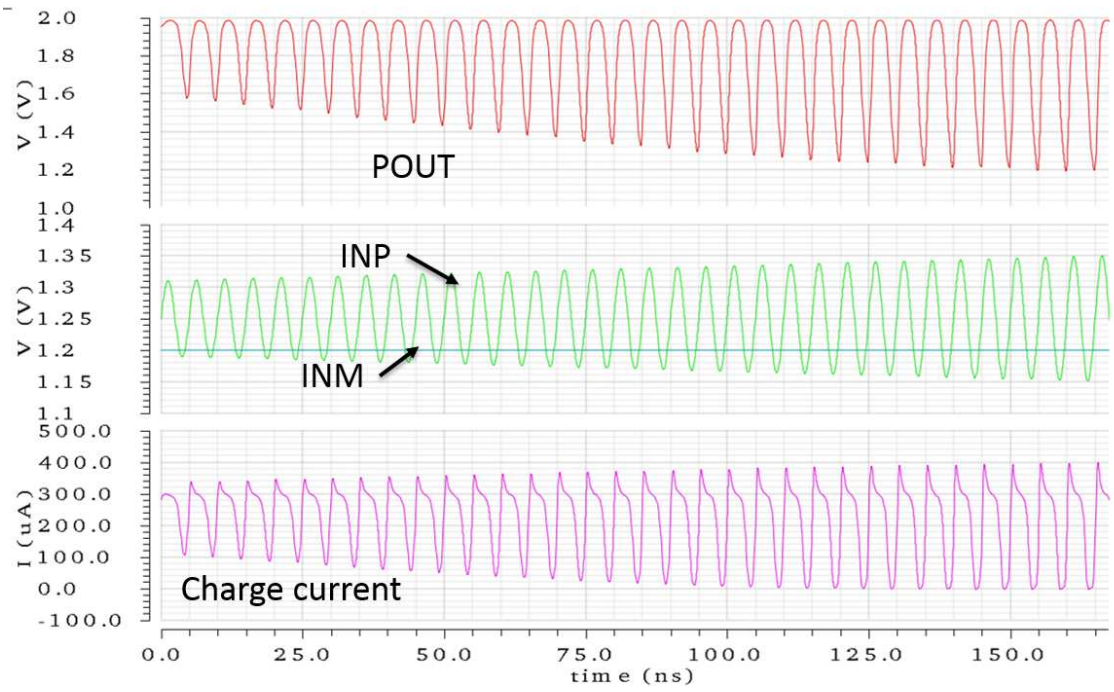

Fig. 6.9: Peak detect stage waveforms

6.4.4 Hysteresis Stage

This stage consists of the PMOS comparator pair MP6/MP7 and the cross coupled NMOS sinks MN7/MN8/MN9/MN10. The level of hysteresis is determined by the ratio of the widths of MN7/MN8. This stage removes high frequency ripple present on the drain of MP5.

6.4.5 Buffer

The output of the hysteresis stage is fed to a gain stage comprising PMOS pair MP8/MP9 and NMOS pairs MN11/MN12. The output of this gain stage is treated to a final inverter stage MP10/MN13 which produces the final comparator output.

6.4.6 Node transitions

The comparator node transition diagram is shown in Fig. 6.10. The comparator threshold V_{REF} is the adjustable level which determines the passband of the SAW device. If the peak of the level shifted SAW output exceeds the threshold for a given time window, as seen, the comparator peak detect node will be charged. The drain of MP5 which serves as the hysteresis stage input will be pulled low. The subsequent hysteresis, gain and buffer stages will produce a ripple free final output. We note that the hysteresis and buffer stages do not need to handle a high speed input, since the peak detect output stage is high for the entire window during which the passband condition is satisfied. However, the differential stage needs to handle the full speed input corresponding to the SAW frequency range.

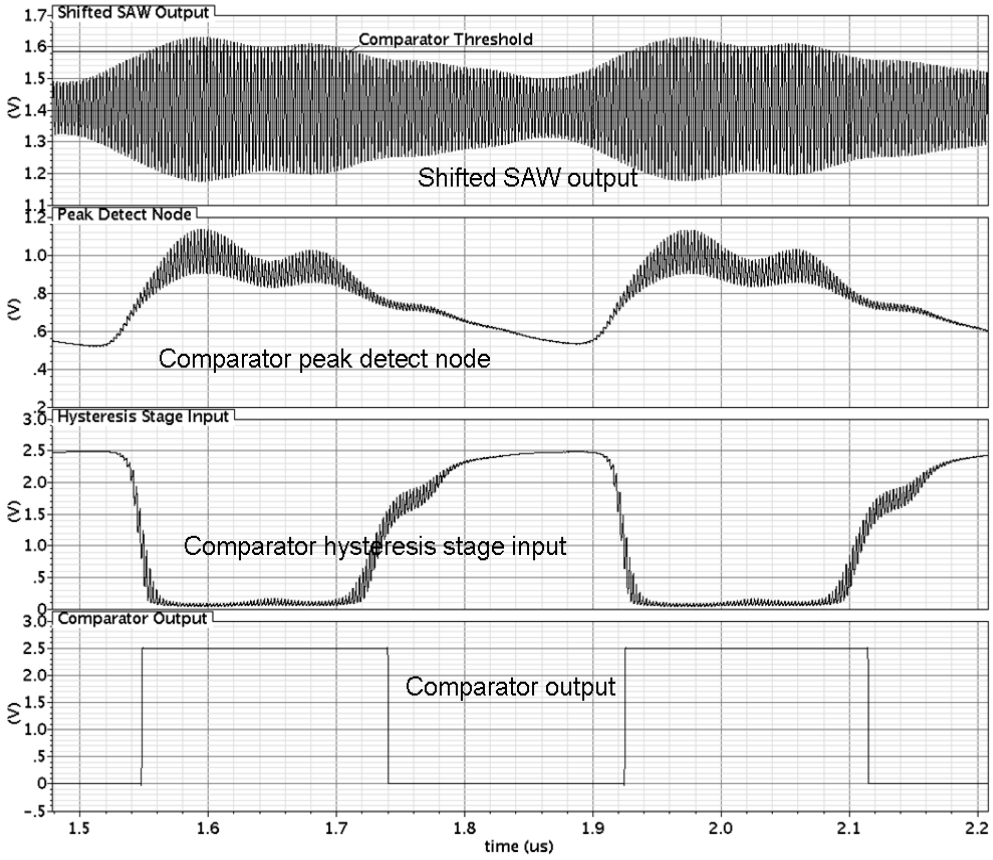

Figure 6.10: Peak detecting comparator node transitions

6.4.7 Layout

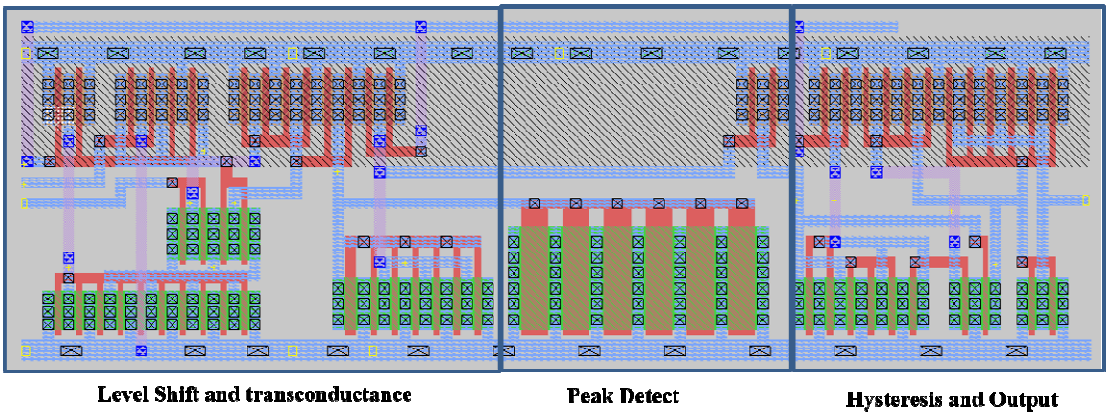

Fig. 6.11: Layout of peak detecting comparator

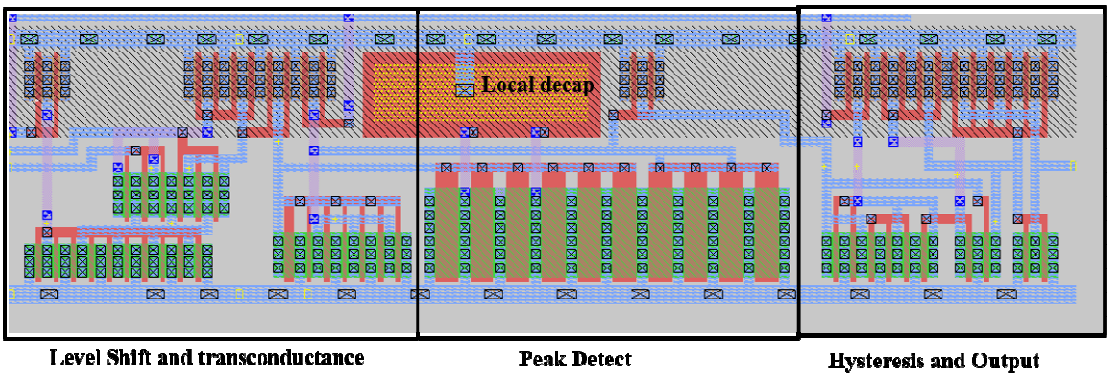

Figure 6.12: Layout of comparator with external common mode

Shown in Fig. 6.11 is the layout of the peak detecting comparator. The layout is horizontally compartmentalized into three stages. The first stage contains the input level shifter, the mirror bias, the differential stage and the charge current injector. The peak detection stage has the NMOS capacitor and the PMOS pull up. The final stage consists of the cross coupled hysteresis NMOS pairs and the output buffer stage.

A second version of the comparator which was used in a revision of the chip uses an external common mode, thus removing the need for a level shifter. This reduces noise interference from the supply. Noise immunity is also enhanced in this version by adding NMOS cap on the drain of MN6 and by adding local supply decoupling capacitance using poly layers. The layout of this version is shown Figure 6.12.

6.5: Finite State Machine Implementation

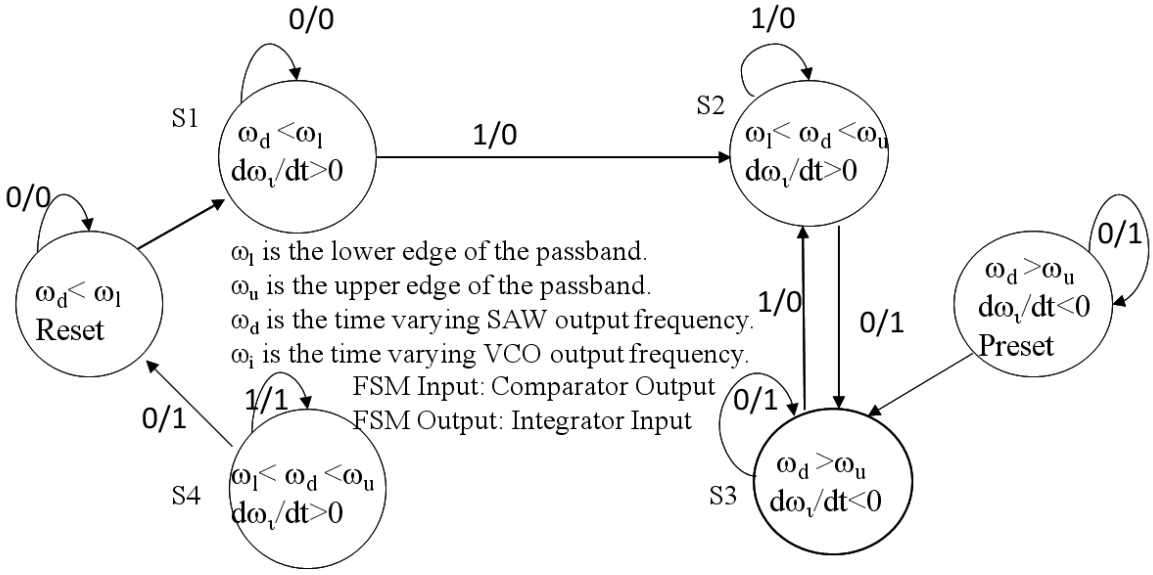

Figure 6.13: Finite State Machine Diagram

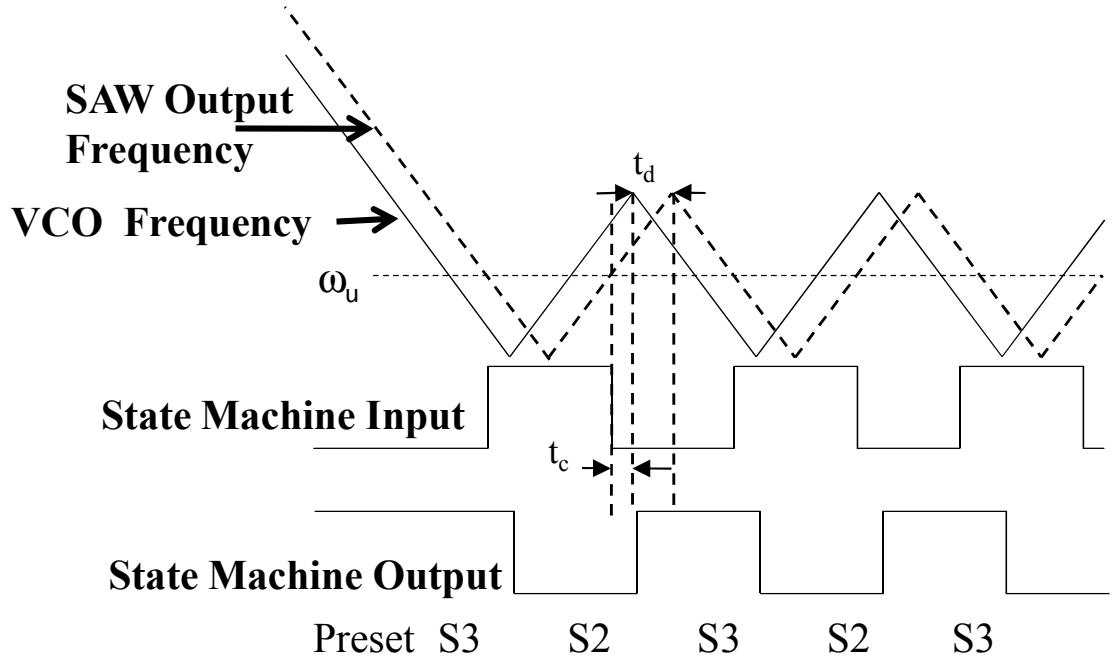

Figure 6.14: Conceptual Timing Diagram

Shown in Fig. 6.13 is the state transition diagram for the detector. Six states are observable here. In all cases a transition is contingent on a change in the comparator output which serves as the FSM input and the current state of the FSM. In

state S1, the instantaneous SAW output frequency is below the passband and the instantaneous VCO output frequency is increasing. Note that the SAW delay line imposes a delay between the time varying frequencies at the SAW output and the VCO output. In S2 the SAW output frequency is within the passband and the VCO output frequency is increasing. A transition from this state is induced when the SAW output frequency exits the passband causing the comparator output to go low. In S3 the SAW output frequency is above the passband and the VCO output frequency is decreasing. In state S4 the SAW output frequency is within the passband and increasing while the VCO output frequency is decreasing. In stable operating mode the FSM toggles between states 2 and 3. Therefore the SAW output frequency is centered at the upper edge of the passband, i.e. at ω_u.

To ensure that these stable states are reached, two comparators provide reset and preset functionality to account for random initial latch outputs. These startup states where the VCO instantaneous frequency is outside the linear range of operation are marked as Reset and Preset. In these cases the slope of the fine input is accordingly set so that the frequency is brought back to the band of interest. The FSM is not a standalone system but rather operates within the entire system loop. Thus, we note that S1 and S4 cannot be permanent stable states as the input is forced by the loop to toggle.

The complete circuit schematic of the FSM including the comparators is shown in Fig. 6.15. The FSM output is the buffered flip flop output Q1. This output acts as the input to the RC filter. The filter output ramp VCO_IN is the fine input to the VCO and also the primary loop sensor analog output.

A typical sequence is demonstrated in Fig. 6.14. The initial VCO output frequency F_{VCO} and SAW output frequency F_{SAW} are both out of band on the high side. This corresponds to the Preset state. In this state the FSM output is set high causing VCO_IN to ramp high, thus decreasing the VCO output frequency F_{VCO} till it enters the passband. This entry point marks entry into state S3 where the FSM output remains high since the SAW output frequency F_{SAW} which is delayed from F_{VCO} by the SAW groups delay t_d is still out of band. When the SAW output frequency enters the passband the FSM output goes low and the FSM enters state S2. At this point the VCO input VCO_IN slope reverses causing the VCO output frequency to also reverse slope. After a time delay of t_d F_{SAW} also reverses slope but the state S2 is maintained since F_{SAW} is still in the passband. When the SAW output frequency exceeds the upper edge of the passband, the FSM input goes low and after a circuit delay t_c the state machine output goes high. At this point the FSM is in state S3. This also marks the point where VCO_IN reverses slope, also causing a slope reversal in $F_{VCO.}$ After another t_d F_{SAW} reverses slope and decreases till it reenters the passband. At this point the FSM input toggles high and after another t_c the FSM output goes high marking entry point into state S2. The cycle repeats, stabilizing the FSM to alternate between states S2 and S3.

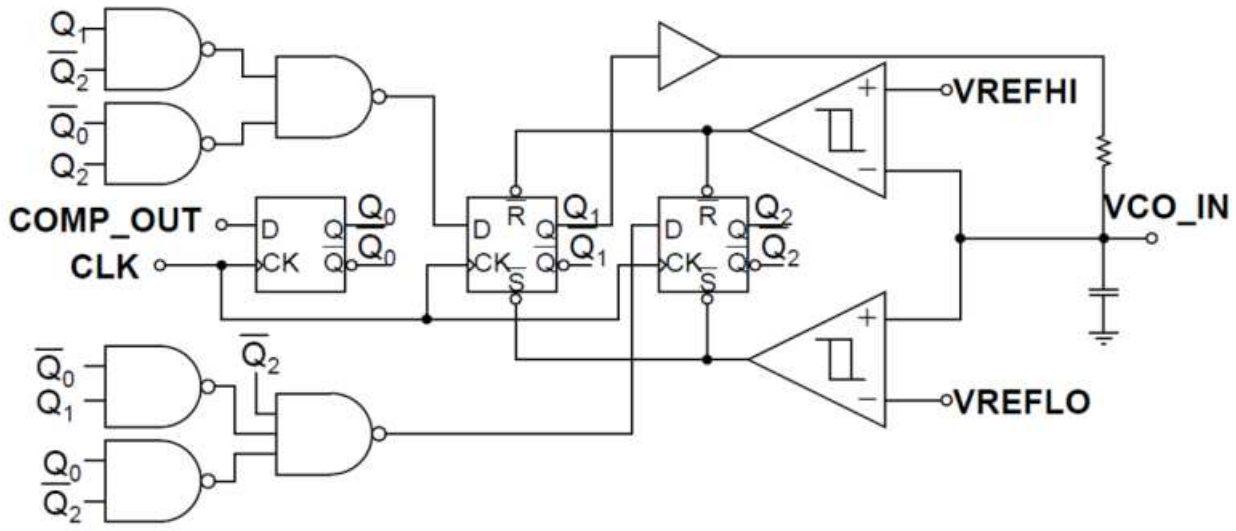

Fig. 6.15: Finite State Machine Circuit

6.6: External Integrator

This is a basic RC filter whose time constant determines the slope and range of the VCO fine input and hence the output frequency variation of the VCO. Typical values of R and C are 100K and 200pF respectively. The time constant needs to be large compared to t_d such that the time varying frequency does not exit the lower edge of the passband on the down-slope. This filter can be incorporated into the chip as well at the cost of design area.

6.7: Circuit Analysis

We assume a linear variation of the VCO frequency with the fine input. This can be ensured by adjusting the coarse input. Further, we assume that the RC integrator slope is linear in the stable operating range.

From the operation of the FSM we note that the state machine input toggles high when the SAW output frequency f_d crosses the upper edge of the passband f_u with positive slope. At this point the VCO output frequency reverses slope and hence corresponds to the local maximum in steady state. Consequently, after a delay of t_d,

the SAW output frequency will reverse slope where $t_d = x/v$, x being the separation between the IDT midpoints and v is the acoustic wave velocity. After another t_d the SAW output frequency will reenter the passband, this time with negative slope. This corresponds to a state transition to state 2 at which point the VCO output reverses slope corresponding to a local minimum. Thus the local maximum and minimum of the VCO fine input are given by

$$V_{\max} = V_u + \frac{V_{dd}}{\tau}(t_d + t_c) \qquad (6.11)$$

$$V_{\min} = V_u - \frac{V_{dd}}{\tau}(t_d + t_c) \qquad (6.12)$$

where V_u is the VCO fine voltage corresponding to the upper edge of the passband, τ is the RC time constant, t_d is the SAW delay and t_c the circuit delay between the comparator output going high and the FSM output going high.

The range of the ramp is given by:

$$V_{band} = \frac{2V_{dd}}{\tau}(t_d + t_c) \qquad (6.13)$$

The change in the maximum input ramp voltage due to a change in the IDT mid-band frequency is

$$\Delta V_{\max} = \frac{\Delta f_u}{K} + \frac{V_{dd}\Delta t_d}{\tau} \qquad (6.14)$$

where K is the gain of the fine VCO input.

We note that the VCO sensitivity can be increased by reducing the fine gain.

In the case of narrowband or resonator devices, a constraint is necessary to ensure loop operation.

$$B > \frac{V_{dd} K (t_d + t_c)}{\tau} \qquad (6.15)$$

where B is the resonator bandwidth.

More exact expressions can be derived for the maximum and minimum voltages of the VCO fine input without the need for linearization. Let us denote the net delay comprising both SAW and circuit delays as T_0 i.e.

$$T_0 = t_d + t_c \qquad (6.16)$$

Then, the charge time from V_0 to V_{max} is T_0. In addition, the discharge time from V_0 to V_{min} is also T_0. Here V_0 is the equivalent VCO input voltage corresponding to the edge of the passband. Further, let the discharge and charge times be T_1 and T_2 respectively. Then, from RC analysis, we have

$$V_{\max} = V_{dd}(1 - e^{-T_0/\tau}) + V_0 e^{-T_0/\tau} \qquad (6.17)$$

$$V_{\min} = V_0 e^{-T_0/\tau} \qquad (6.18)$$

$$V_{\min} = V_{\max} e^{-T_1/\tau} \qquad (6.19)$$

$$V_{\max} = V_{dd}(1 - e^{-T_0/\tau}) + V_{\min} e^{-T_2/\tau} \qquad (6.20)$$

From these equations the differential changes in the minimum and maximum voltages in terms of differential changes in the equivalent reference voltage and SAW phase delay can be expressed as

$$\Delta V_{\min} = (\Delta V_0 - V_0 \Delta T_0/\tau) e^{-T_0/\tau} \qquad (6.21)$$

$$\Delta V_{\max} = [\Delta V_0 + (V_{dd} - V_0)\Delta T_0/\tau] e^{-T_0/\tau} \qquad (6.22)$$

The differential change in mean voltage V_m is now computed as

$$\Delta V_m = [\Delta V_0 + (V_{dd}/2 - V_0)\Delta T_0/\tau] e^{-T_0/\tau} \qquad (6.23)$$

while the differential change in the peak to peak voltage is given by

$$\Delta V_{\max} - \Delta V_{\min} = (V_{dd} \Delta T_0 / \tau) e^{-T_0/\tau} \qquad (6.24)$$

We note that the linear approximations derived earlier are valid if $T_0/\tau << 1$.

We now derive expressions for the charge and discharge times in terms of the reference voltage and the composite delay. From equation (6.18) the discharge time is given by

$$T_1 = T_0 + \tau \ln(V_{\max} / V_0) \qquad (6.25)$$

$$T_2 = T_0 + \tau \ln[(V_{dd} - V_1) / (V_{dd} - V_0)] \qquad (6.26)$$

Denoting $p = e^{-T_0/\tau}$ and $r = V_0 / V_{dd}$ we obtain expressions for the charge and discharge times in terms of earlier derived expressions for V_1 and V_2.

$$T_1 = T_0 + \tau \ln[(1 - p) / r + p] \qquad (6.27)$$

$$T_2 = T_0 + \tau \ln[(1 - pr) / (1 - r)] \qquad (6.28)$$

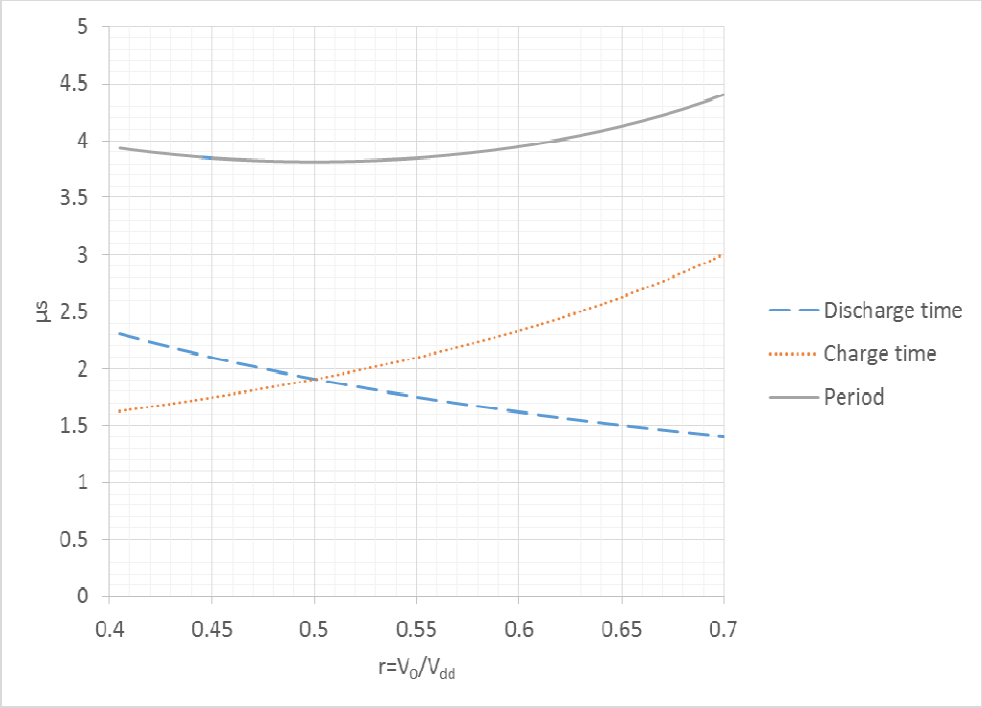

Figure 6.16 Variation of charge time, discharge time and period with equivalent passband threshold

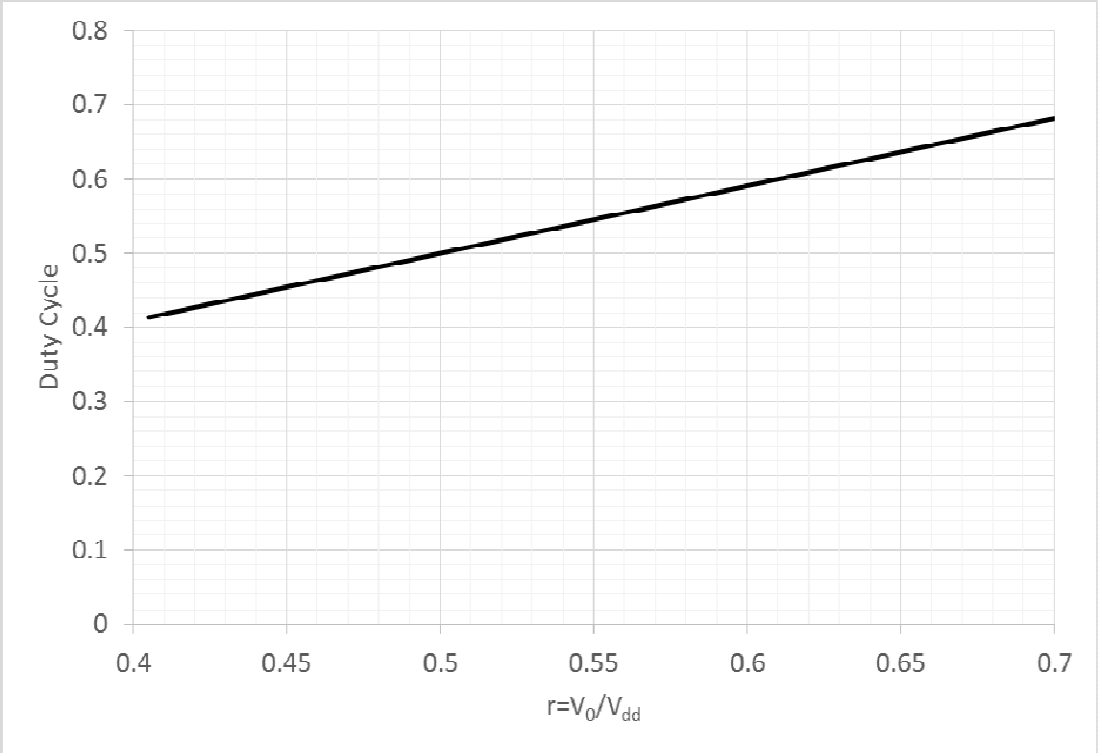

Figure 6.17: Variation of duty cycle with equivalent passband threshold

The equations have been graphically represented in Figures 6.16 and 6.17. For this example the ratio, p, has been taken to be 0.1 with T_0=1μs. Shown in Figure 6.16 are effects of increasing the ratio V_0/V_{dd} on the charge and discharge times and the time period of the sensor output. In Figure 6.17 this variation is observed as the duty cycle dependence on V_0/V_{dd}. Curiously, this duty cycle tracks r in the range of 0.4 to 0.7. The total time period is in the vicinity of $4T_0$ for 0.4<r<0.6.

6.8: Primary Loop Readout Sensitivity

The sensitivity of the proposed circuit can be defined as the ratio of the output voltage shift to the frequency shift of the SAW device caused by mass loading. From equation (6.14), the differential voltage shift increases with decreased VCO fine gain, but a lower bound is given by equation (6.15). The deterministic component of the circuit delay t_c has no effect on the voltage shift. The random component arising from the discretization of the interval between the comparator edge and the system clock edge can be minimized by increasing the clock frequency and the filter time constant. Supply noise interference causing frequency and phase jitter is also considered. However, statistically, this will not cause a shift in the mean output voltage. Simulations with superimposed supply noise are considered in Chapter 7.

6.9: Discrete Time Analysis

We construct a discrete time model of the closed loop as shown in Fig. 6.18.

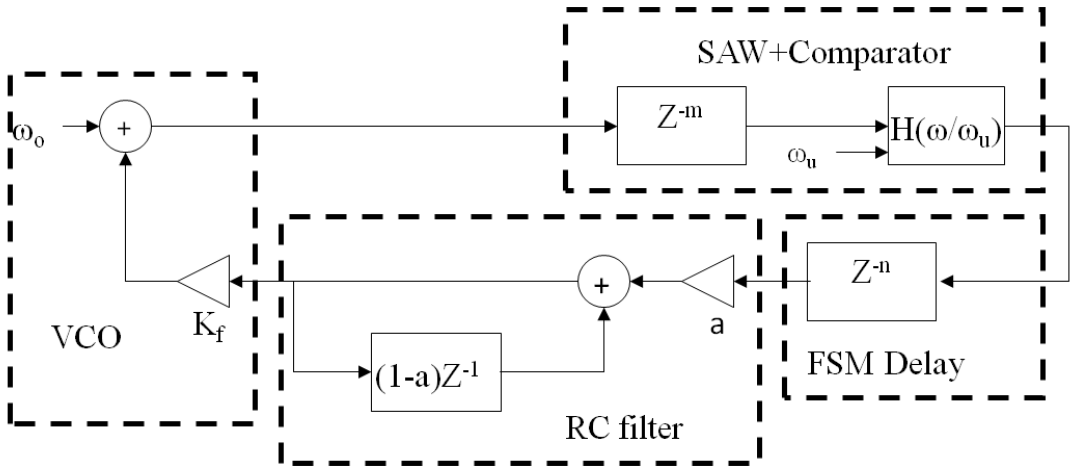

Fig. 6.18: Discrete Time Model

In this model we take the system to be operating in steady state mode i.e. toggling between states 2 and 3. In this mode the FSM can be approximated by a lumped clock and circuit delay. This delay is represented by Z^{-n}. The combination of the SAW and the peak detecting comparator is represented by a delay element and a discrete comparator transfer function. This transfer function can be represented as $H(\omega_k/\omega_u)=1$ for $\omega_k < \omega_u$, where the upper limit of passband (ω_u) is set by the corresponding voltage threshold. The SAW delay is represented by the element Z^{-m}.

The VCO is represented by a linearized model with a gain of K_f and an offset of ω_o. The input of the VCO stage comes from the RC filter output. Consistent with the block diagram of Fig. 5.2, the VCO output serves as input to the SAW device.

In this discrete time model a stage of inversion has been removed and to account for this the slope of the VCO output frequency with respect to the fine input has been reversed.

Using this model, we formulate the following difference equation at node ω.

$$\omega_k - (1-a)\omega_{k-1} = a\omega_o + K_f aH(\omega_{k-m-n}/\omega_u) \qquad (6.29)$$

Let k-m-n be the time step at which the comparator output switches high. Then at time step k we have

$$\omega_k - \omega_{k-1} = a(\omega_o - \omega_{k-1}) \tag{6.30}$$

$$\omega_{k+1} - \omega_k = a(\omega_o - \omega_{k-1} + K_f) \tag{6.31}$$

Since $\omega_k > \omega_o$ for all k we have

$$\omega_{\mathrm{k}} < \omega_{k-1} \tag{6.32}$$

$$\omega_{k+1} > \omega_{\mathrm{k}} \tag{6.33}$$

indicating a local minimum at k.

Denoting this minimum by ω_{min}, the time step interval between $\omega=\omega_u$ and ω_{min} is thus m+n.

Solving for ω_k in a piecewise manner, we get the following expressions for the maximum and minimum frequencies, ω_{min} and ω_{max}:

$$\omega_{\min} = (\omega_u - \omega_o)(1-a)^{m+n} + \omega_o \tag{6.34}$$

$$\omega_{\max} = (\omega_u - \omega_o - K_f V_{dd})(1-a)^{m+n} + \omega_o + K_f V_{dd} \tag{6.35}$$

Equations 6.34 and 6.35 give expressions for the minimum and maximum bounds of the time varying SAW output frequency in terms of the VCO center frequency, the SAW passband edge, the SAW delay, RC time constant and the SAW and circuit delay elements.

If, due to mass absorption, the SAW velocity changes, causing a change in ω_u, the corresponding maximum of the observed filter output will also change.

A behavioral event driven simulation was carried out using a Verilog model. Here the sensor event was simulated in the form of a step change in ω_u. The resulting

signals are plotted in Fig. 6.18. It is noted that at the sensor event the average of the analog output voltage also changes. Further, as expected from the circuit analysis, the comparator output is high when the time varying SAW frequency is below the passband upper limit.

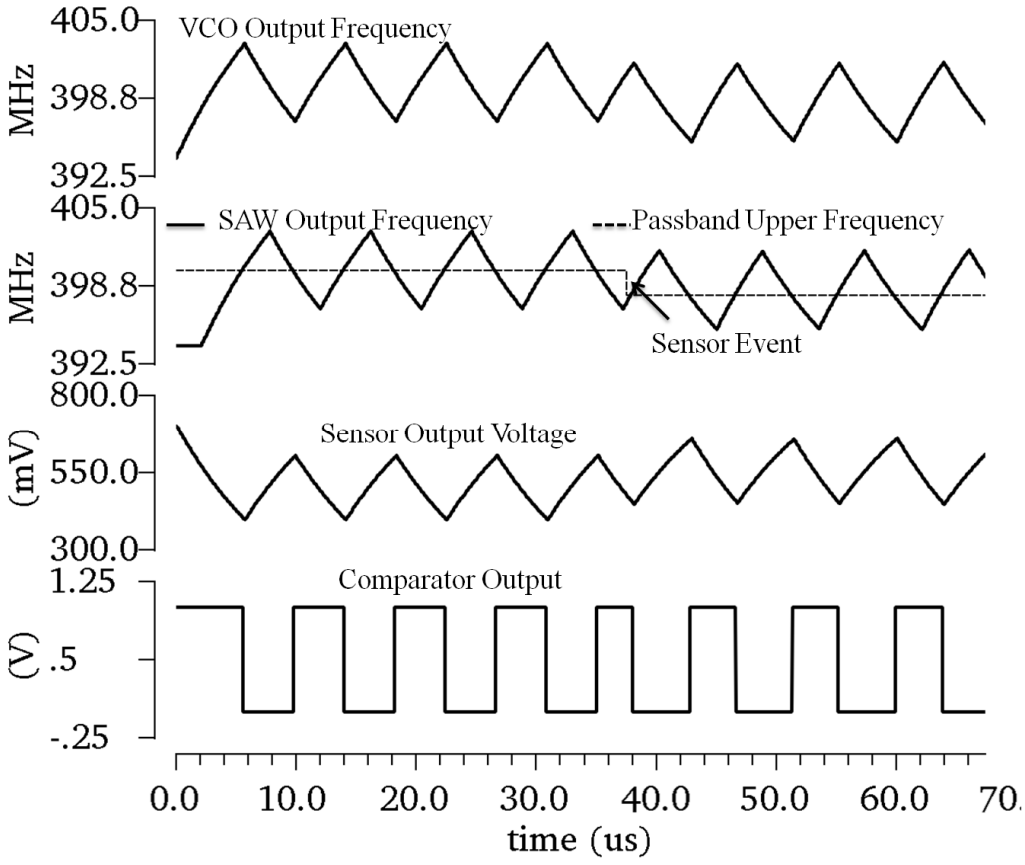

Fig. 6.18: Behavioral Model Simulation Results.

Section 6.10: Summary

In this chapter we have presented the readout architecture and discussed the top level operation of the primary sensor loop. We have also discussed and analyzed the individual blocks of the primary sensor loop. The primary loop consists of the VCO, the SAW device, the peak detecting comparator, the finite state machine and the RC filter. The VCO is configured as a pseudo-differential ring with coarse and fine

inputs. Several models of the SAW device are considered and the open loop response of the VCO-SAW pair is analyzed for a ramp input at the VCO fine input. We have then analyzed the operation of the peak detecting comparator, discussing the functionality of each stage separately. The five stages of this comparator are input level shift, transconductance, peak detection, hysteresis and output. Next, the operation of the loop core constituted by the FSM has been discussed with a description of the individual states and the transition diagram. The states of the FSM depend on the time varying frequency relationship between the SAW output frequency and the VCO output frequency. The slope of the instantaneous frequency are also given by the FSM outputs. A typical sequence from startup to steady state has been used to illustrate the transition map. The requirements of the RC filter have been presented. We have next analyzed the loop with a linearized model of the filter and derived design equations of the analog readout sensitivity in terms of the VCO gain, the RC filter time constant and SAW characteristics. Finally, we have applied discrete time modeling techniques to the loop and derived the maximum and minimum bounds of the SAW and VCO frequency variation. The discrete time model has been implemented using a Verilog behavioral model and the behavioral simulation results demonstrated for a step change in the SAW passband frequencies.

Chapter 7: Simulation and Experimental Results of Primary Sensor Loop

Section 7.1: Introduction

Top level simulations of the primary sensor loop requires models for a given process node and an S parameter or equivalent model of the SAW device. The primary loop readout operation is tested with S-parameter models of commercially available SAW devices from Triquint [21], [22], [23], one centered at 374 MHz with an insertion loss of 5dB and another centered at 140 MHz with an insertion loss of 7.5dB [14]. For the 374MHz operating frequency the circuit design uses TSMC 0.35µm process models. For the 140MHz and 70MHz devices we have used AMI 0.5 µm process models. The designs incorporating the 140MHz SAW filter and the 70MHz IF SAW filter were also used for experimental verification.

Section 7.2: Simulations for 374MHz Device

7.2.1 Transient Simulations

The entire closed loop sensor was simulated with TSMC 0.35µm device models and a SAW device model centered at 374MHz [21]. The usable passband of this filter is 17MHz with an insertion loss of 5 dB. The transient signals are plotted in Figs. 7.1 and 7.2. As can be seen, regardless of the initial state of the FSM output, in steady state the system output ramps between limits depending on the RC time constant and the average value corresponds to a VCO output of ω_u. If the time constant is

increased, the component of variation due to modulation of SAW delay is reduced. The SAW output frequency variation in steady state was between 376.2 MHz and 388.9 MHz while the corresponding output voltage ranged from 1.244V to 1.327V. For a frequency shift of 10 kHz due to mass loading [1], the mean voltage shift is calculated from to be 0.2mV which would correspond to a detected mass in the fg range for a SAW device similar to that reported in [1].

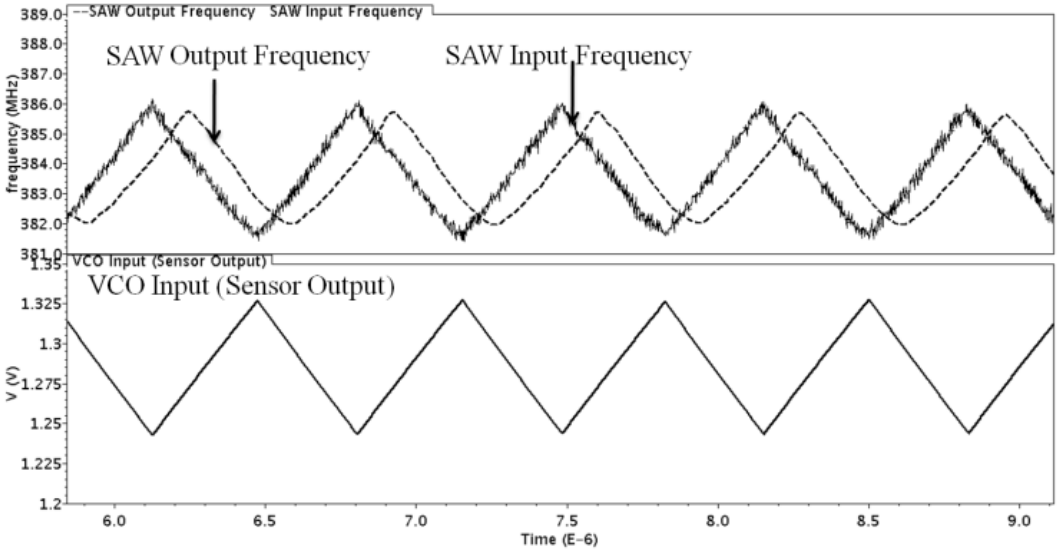

Figure 7.1: Steady State Transient Simulation

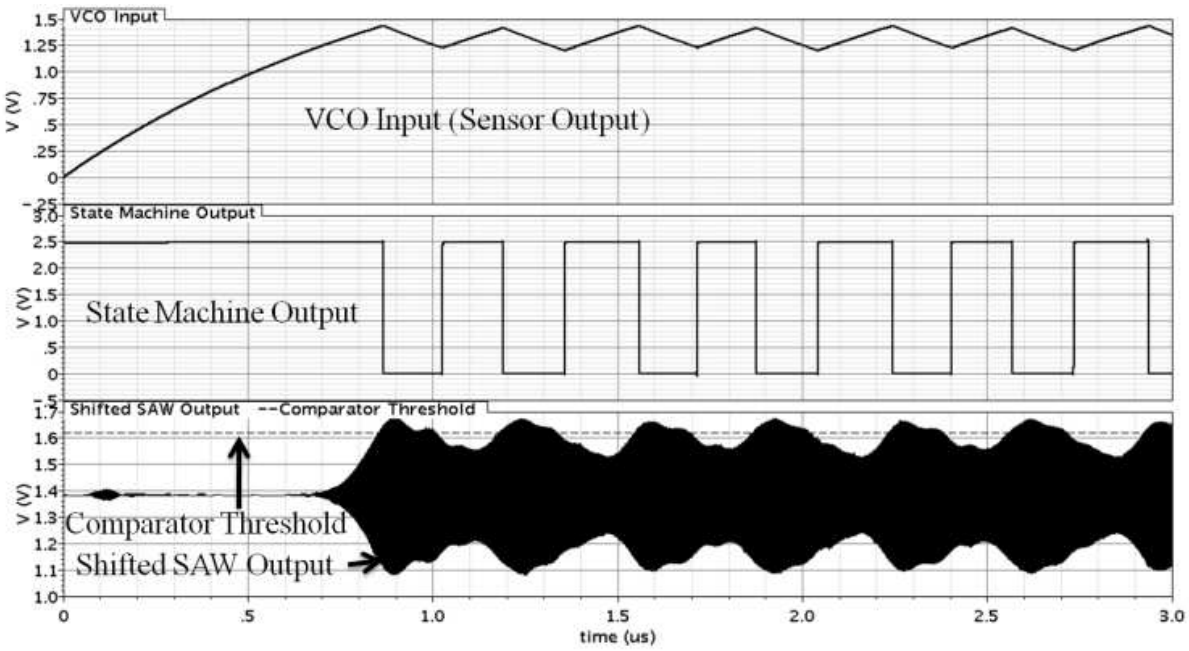

Fig. 7.2: Startup transient simulation

7.2.2 Transient Simulations with Noise

Noise was injected at the VCO input by superimposing a white noise source with peak to peak variation of 25mV at the coarse control input. Figure 7.4 shows a superimposed plot of output transitions within a time period of the sensor output. We observe that although there is an increase in jitter at the sensor output, the average and peak voltage values of the sensor output are not significantly affected due to the filtering by both the SAW filter and the RC filter. The deviation in peak voltage as a result of the noise injection is about 0.1%.

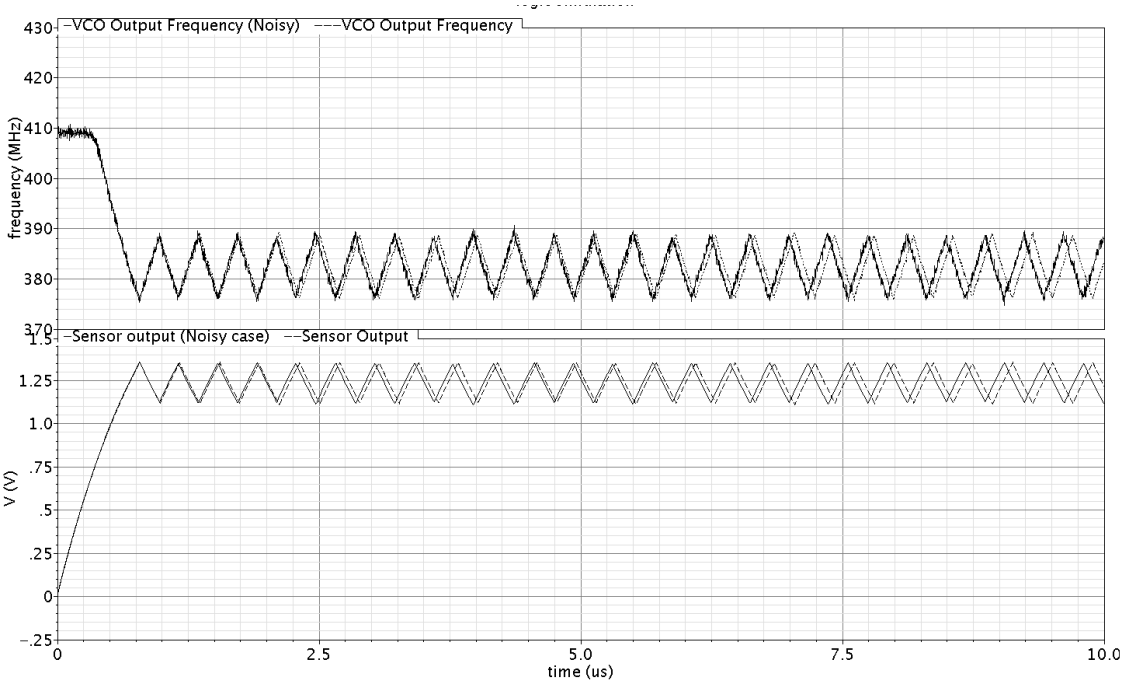

Figure 7.3: Transient simulation with VCO noise

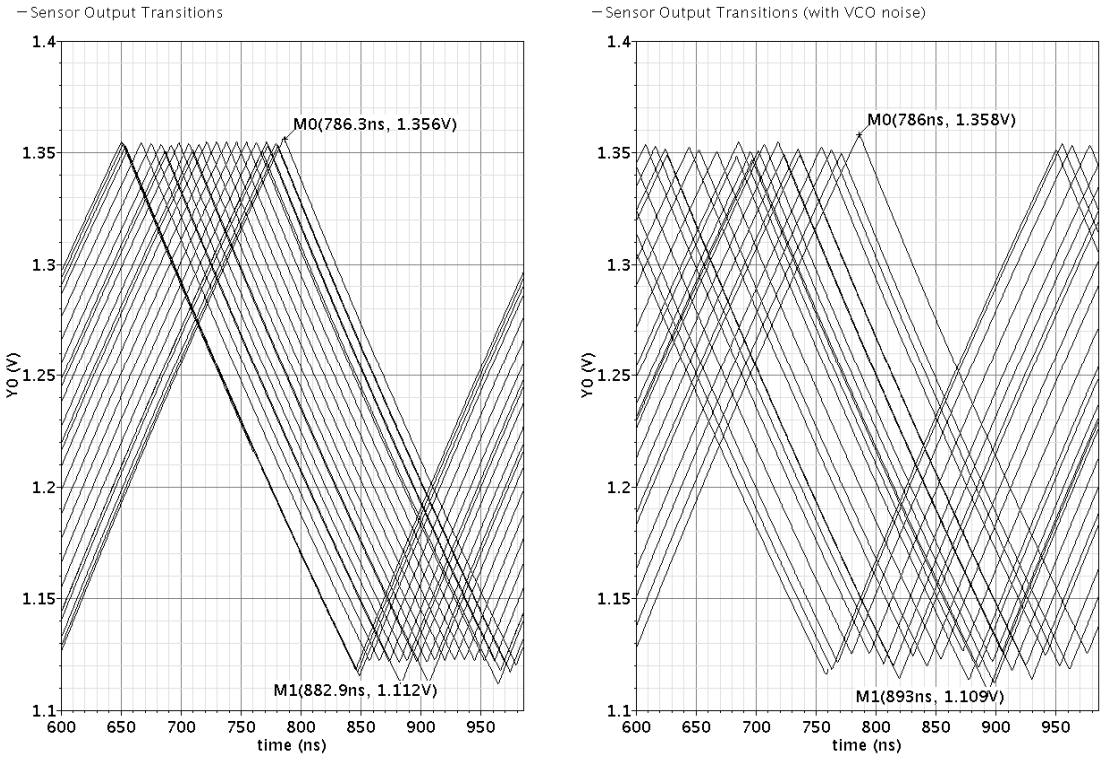

Figure 7.4: Superimposed Output Transitions within Time Period

Section 7.3: Simulations for 140MHz Device

Subsection 7.3.1: Transient Simulations

The entire closed loop sensor was simulated with 0.5μm AMI_C5N device models and a SAW device operating at 140MHz with insertion loss of 7.5dB [14]. The transient signals are plotted in Figs. 7.5 and 7.6. Regardless of the initial state of the FSM output, in steady state the system output ramps between limits depending on the RC time constant and the average value corresponds to a VCO output of ω_u For a coarse voltage (V_c) setting of 1.32V the SAW output frequency variation in steady state was between 143.4 MHz and 146.4 MHz while the corresponding output ranged from 1.9664V to 2.1476V. More critical is the shift of the output voltage mean in case of SAW sensor mass loading. For a frequency shift of 20 kHz due to mass loading [1], [5], [6], the output voltage mean shift is calculated to be 1.25mV which is easily measured with an analog to digital converter (ADC).

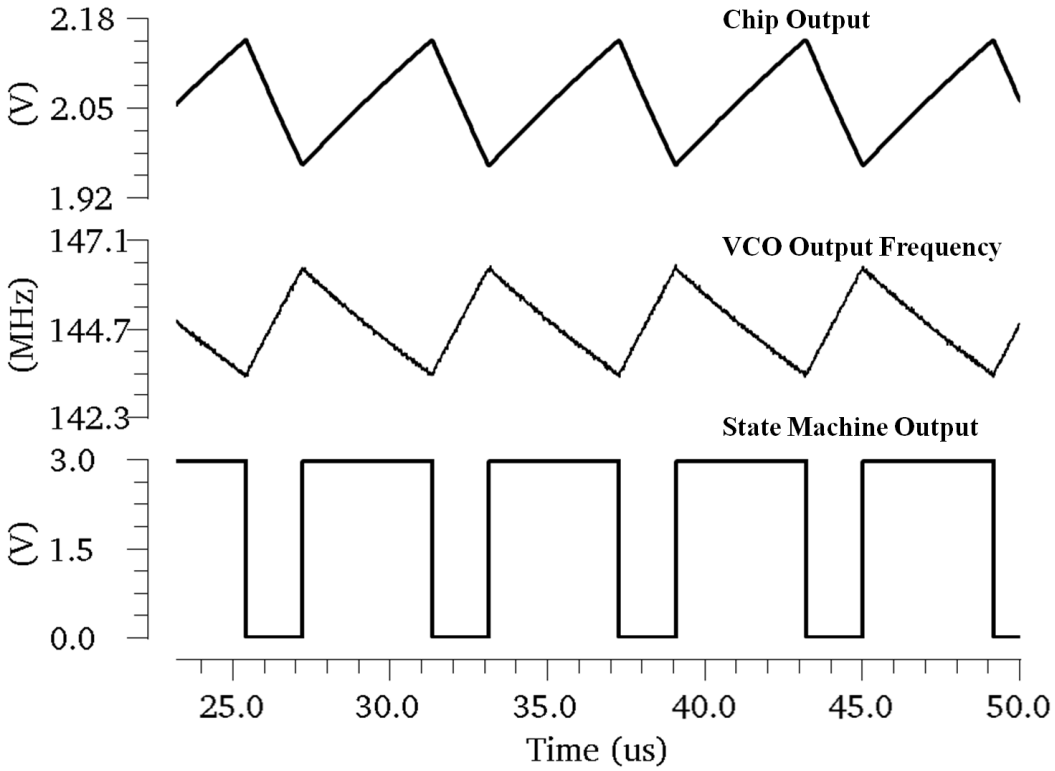

Figure 7.5: Steady State Transient Simulation Outputs

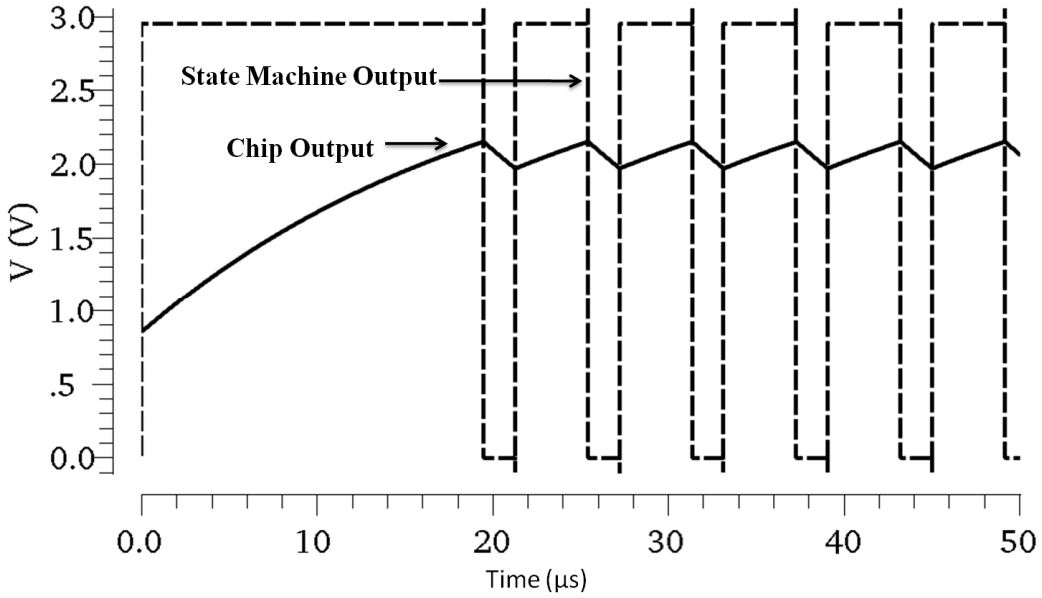

Fig. 7.6: Output Transition from Initial to Steady State

Subsection 7.3.2 Transient Simulations with Noise

Noise was injected at the VCO input by superimposing a white noise source with peak to peak variation of 30mV at the coarse control input. Figure 7.7 shows a

superimposed plot of output transitions within a time period of the sensor output. The result shown is for the 140MHz device. We observe that although there is an increase in jitter at the output, the statistical mean of the output is unchanged. Thus noise induced variation can be distinguished from mass sensing since in this case the output mean will have a detectable shift.

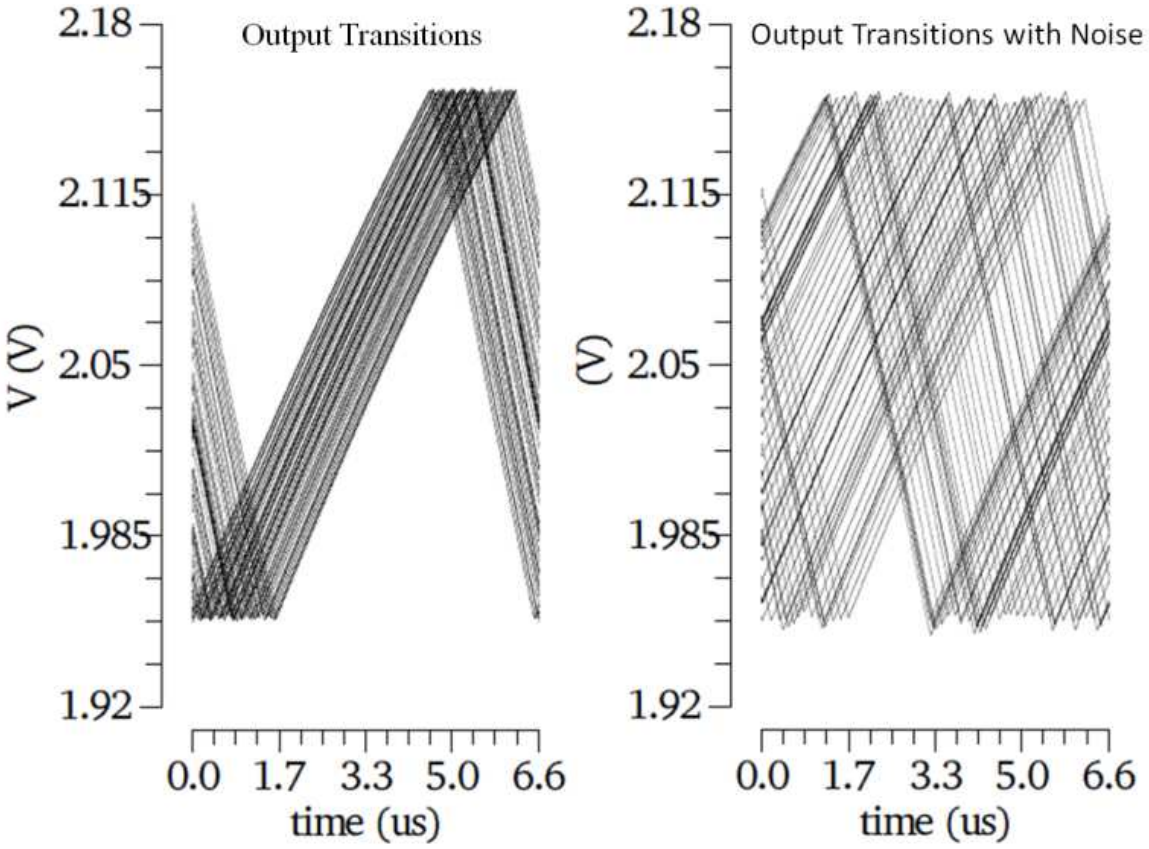

Figure 7.7: Superimposed Output Transitions within Time Period, 140MHz SAW Device

7.4: Simulations for 70MHz Device

7.4.1 Transient Simulations

The closed loop sensor system was also simulated with 0.5µm AMI_C5N device models and a SAW device operating at 70MHz with insertion loss of 7.5dB and a 3 dB bandwidth of 6.35 dB [15]. The phase delay was reported to be 1µs. To obtain

a usable fine tuning range, the coarse voltage setting was obtained from simulations to be in the range of 1.83V to 1.87V. A set of simulations was carried out with different values of V_c. The goal was to observe the variation of the mean and range of sensor output variation and time varying SAW frequency variation for these different settings of V_c. In addition, the variation of duty cycle of the finite state machine output with increasing mean chip output was also observed.

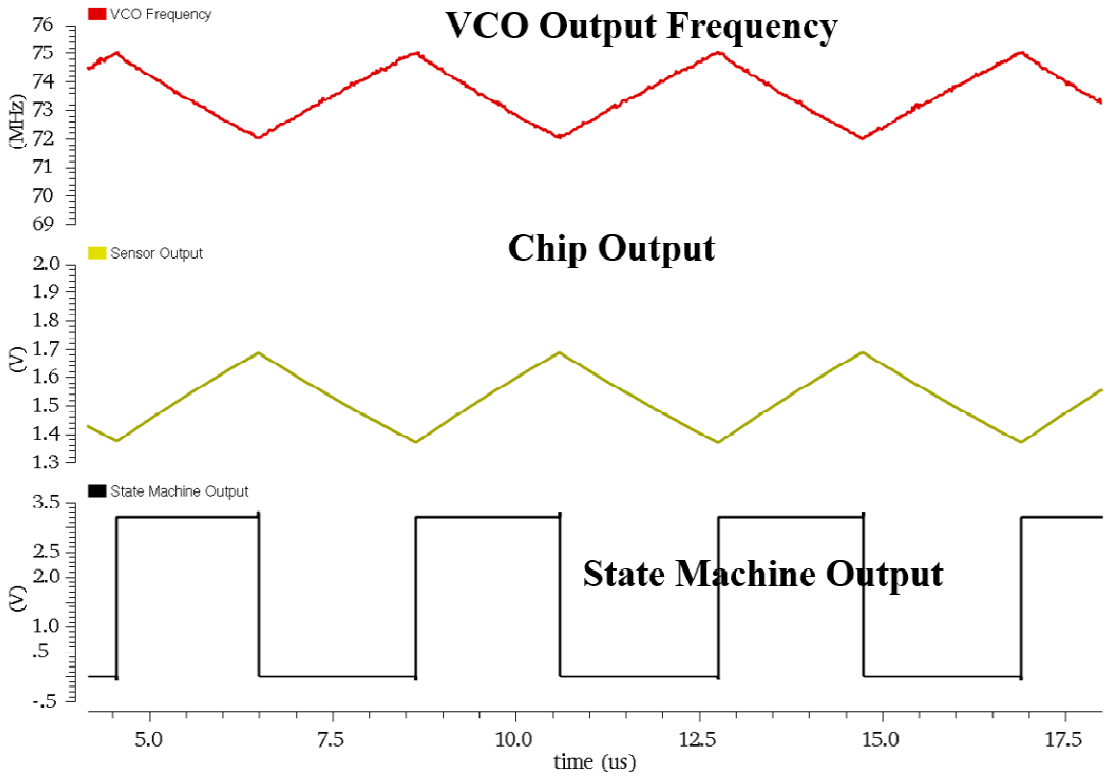

Figure 7.8: Steady State Transient Simulation Outputs for V_c= 1.86V

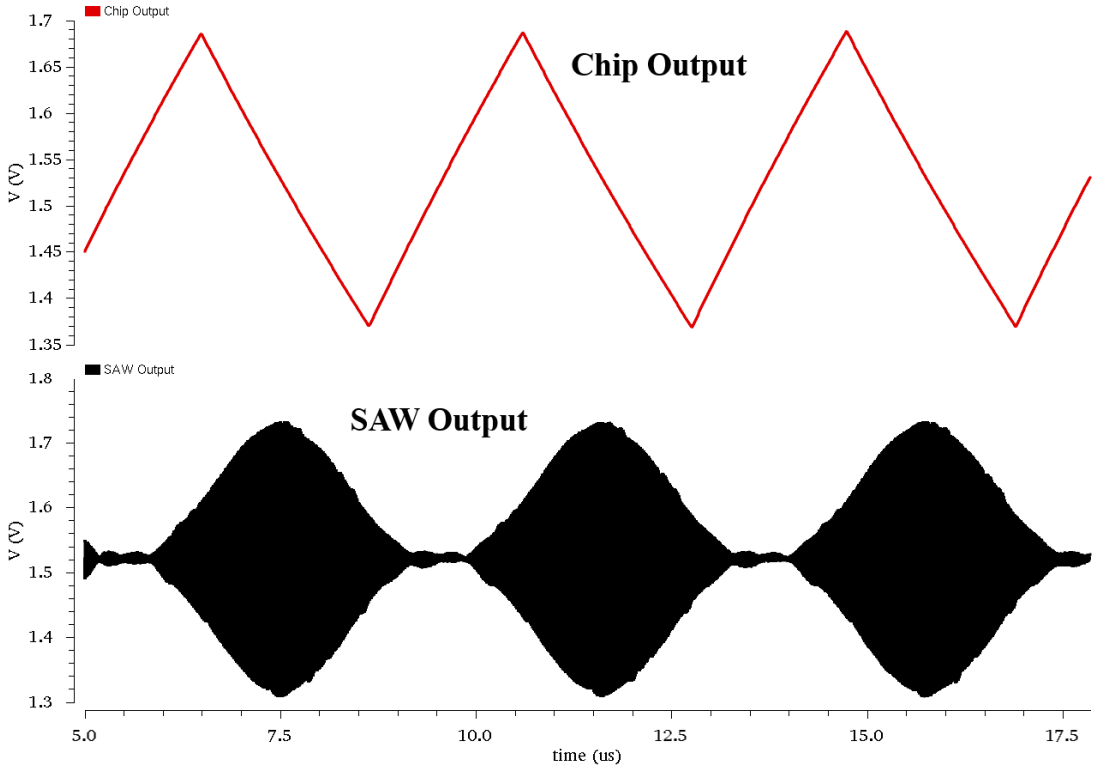

Figure 7.9: Steady State Transient SAW Output and Sensor Output for V_c= 1.86V

Shown in Figure 7.8 are the steady state VCO output frequency, the VCO input and the state machine output for a V_c setting of 1.86V which produces a mean chip output roughly in the center of the tuning range. The VCO output frequency ranges from 72.61MHz to 75.44MHz. The maximum and minimum values of the sensor output are 1.6835V and 1.3926V respectively.

In Figure 7.9 we observe the envelope of the SAW output waveform in steady state transient simulation. Consistent with theoretical derivations, the SAW output amplitude varies with varying VCO frequency which exits and reenters the passband. The entry point, as observed from Figure 7.7 is approximately 74.1MHz.

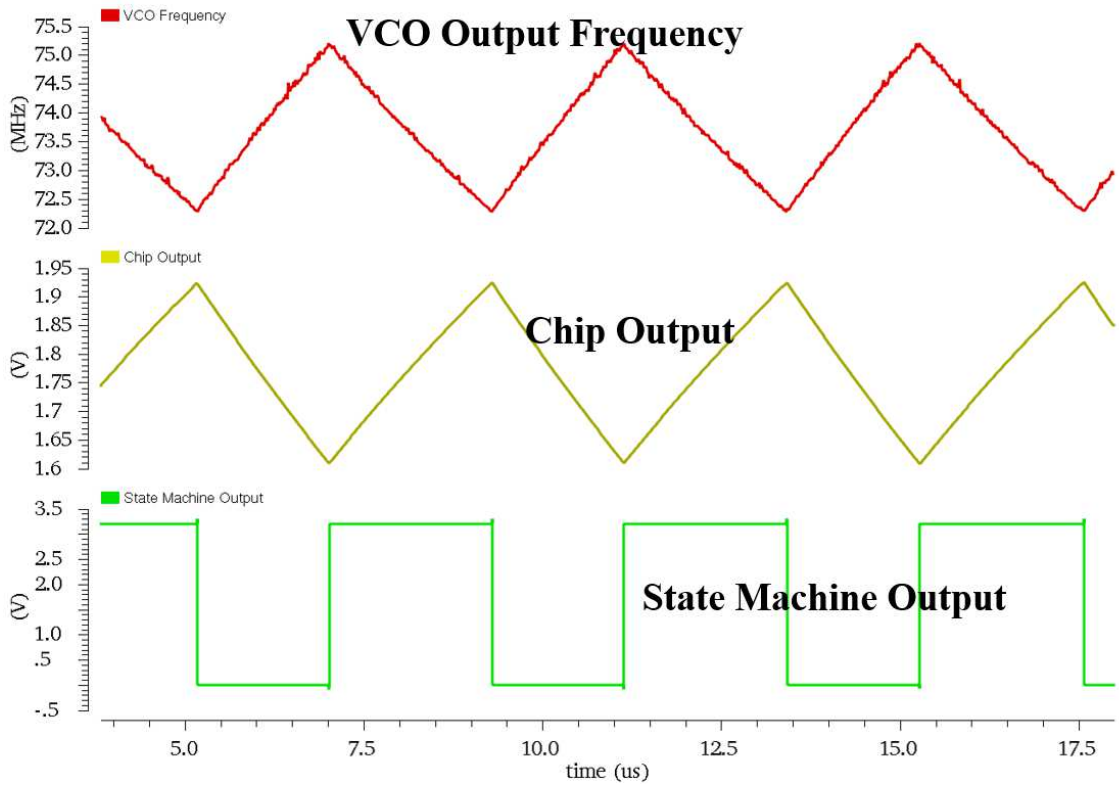

Figure 7.10: Steady State Transient Simulation Outputs for V_c= 1.85V

In Figure 7.10 the steady state VCO output frequency, the VCO input and the state machine output are observed for a V_c setting of 1.85V The maximum and minimum values of the sensor output are 1.9239V and 1.6101V respectively. The VCO output frequency range, as expected, remains unchanged from the previous case. We also note an increase in duty cycle consistent with theoretical results derived in Chapter 6. Figure 7.11 shows the corresponding envelope variation of the SAW output voltage in relation to the chip output ramp.

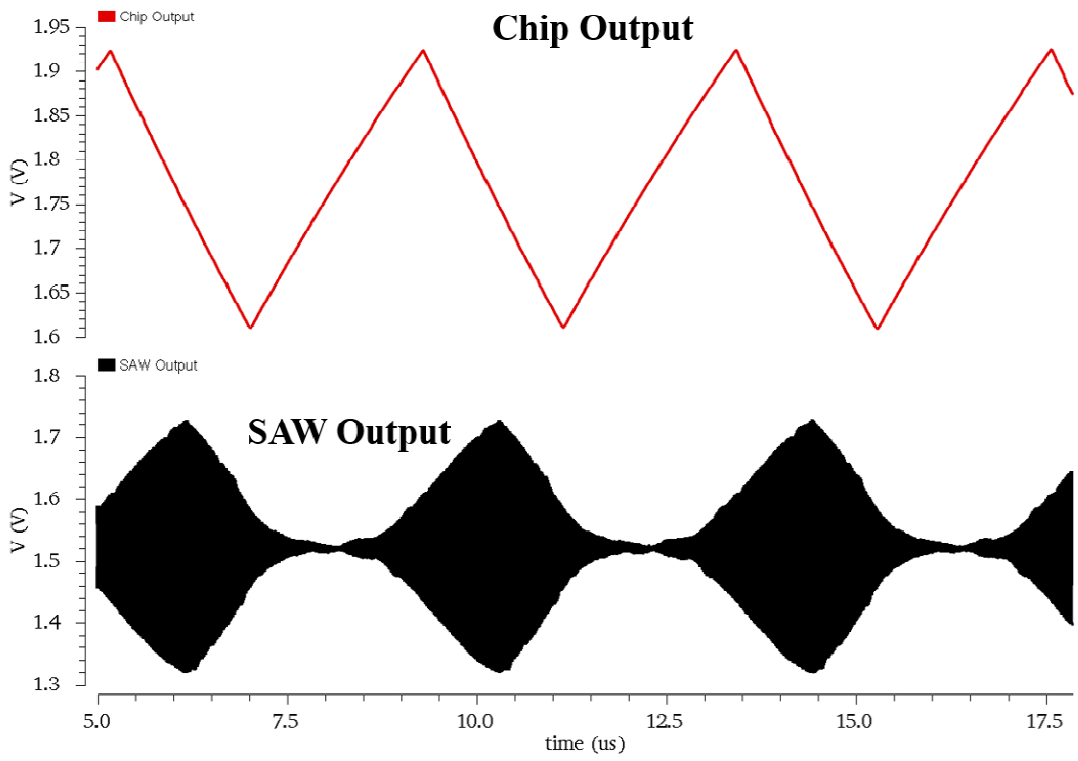

Figure 7.11: Steady State Transient SAW Output and Sensor Output for V_c= 1.85V

Similar plots are shown in Figure 7.12 and Figure 7.13 for a V_c setting of 1.84V. The maximum and minimum values of the sensor output are 2.1679V and 1.8493V respectively. Further increase in duty cycle of the FSM output is also noted.

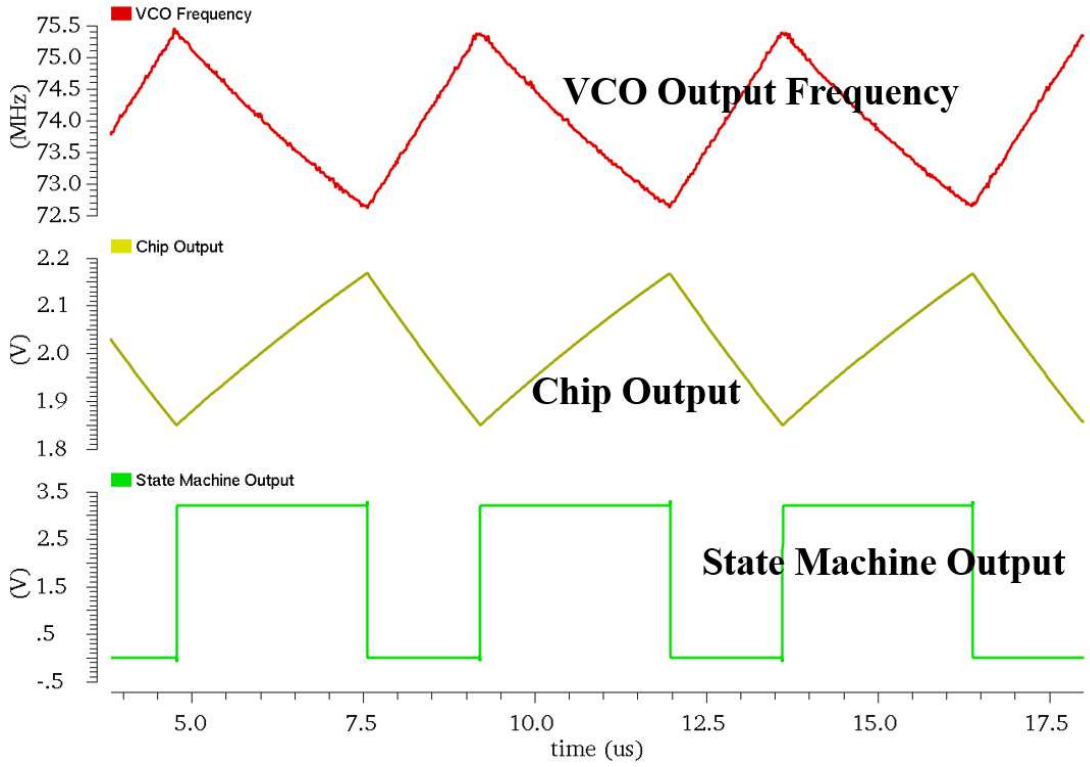

Figure 7.12: Steady State Transient Simulation Outputs for V_c= 1.84V

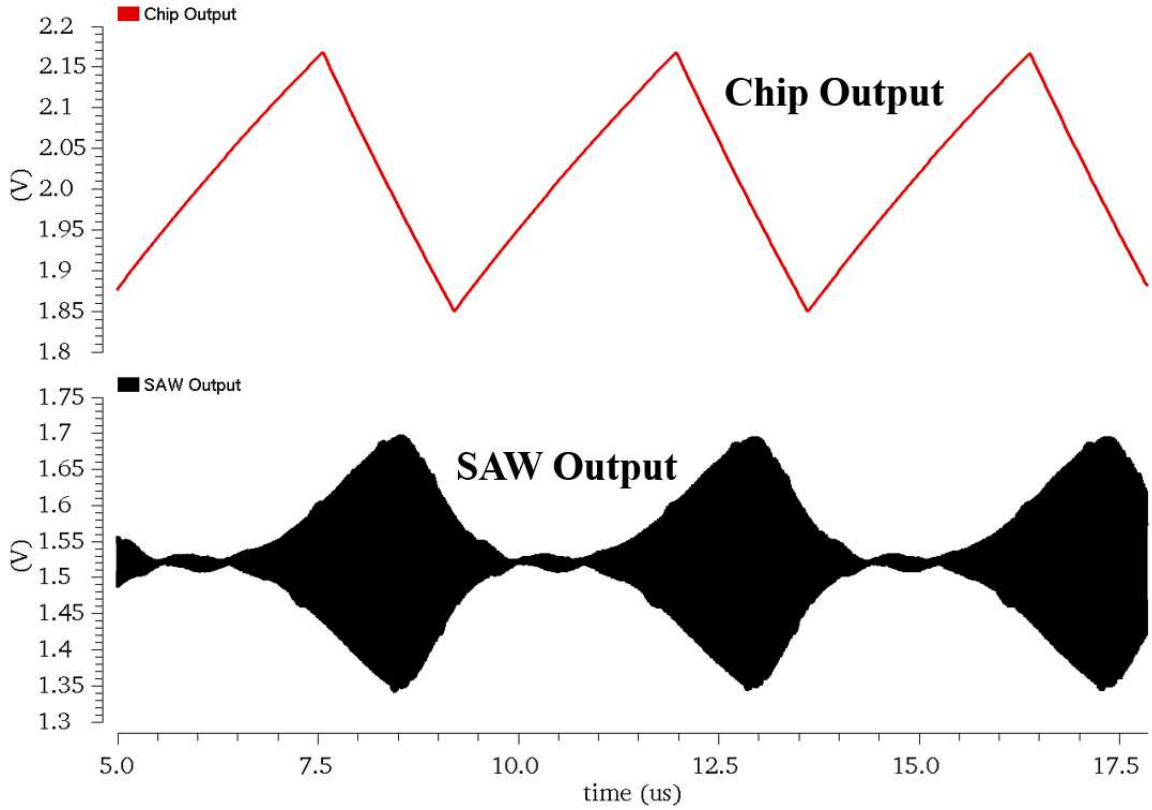

Figure 7.13: Steady State Transient SAW Output and Sensor Output for V_c= 1.84V

Table 7.1: Summary of Simulation Results for 70MHZ SAW device. Ton and Toff represent the high and low durations respectively of the FSM output.

V_c	Output mean	Output maximum	Output minimum	T_{on}	T_{off}
1.86	1.5391V	1.6855V	1.3926V	1.964µs	2.16µs
1.85	1.767V	1.9239V	1.6101V	2.279µs	1.8445µs
1.84	2.0086V	2.1679V	1.8493V	2.77µs	1.6409µs

In Table 7.1 we have summarized some findings from simulated measurements conducted on the readout incorporating the 70MHz IF SAW device.

7.5: Experimental Results

A test chip fabricated using MOSIS 0.5µm AMI_C5N process. The core circuit area layout was 306µm by 216µm. A micrograph of the core area is shown in Fig. 7.14. The micrograph of the entire chip using the standard miniframe is shown in Fig. 7.15. This includes the power grid and internal decoupling capacitors. Primary ESD structures are located on the bond pads. The pads are wire bonded to a DIP package which was used for test purposes. The parasitic capacitance on the high frequency signals which, in this case are the VCO output and the SAW device output are dependent not only the wirebond capacitance but also the routing to the package leads. Therefore, for these signals, the pads with minimum capacitance are chosen although, even the minimum lead capacitance remains in the vicinity of 2pF. Trace capacitance on the printed circuit board would, of course, significantly add to the capacitive load.

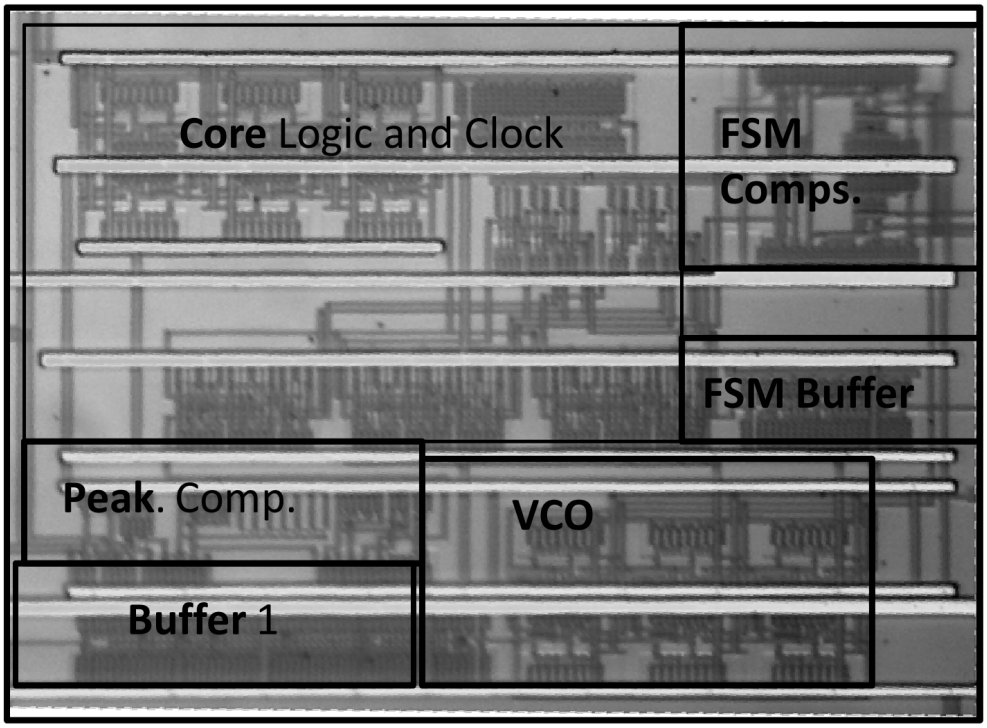

Figure 7.14: Micrograph of Die Active Area

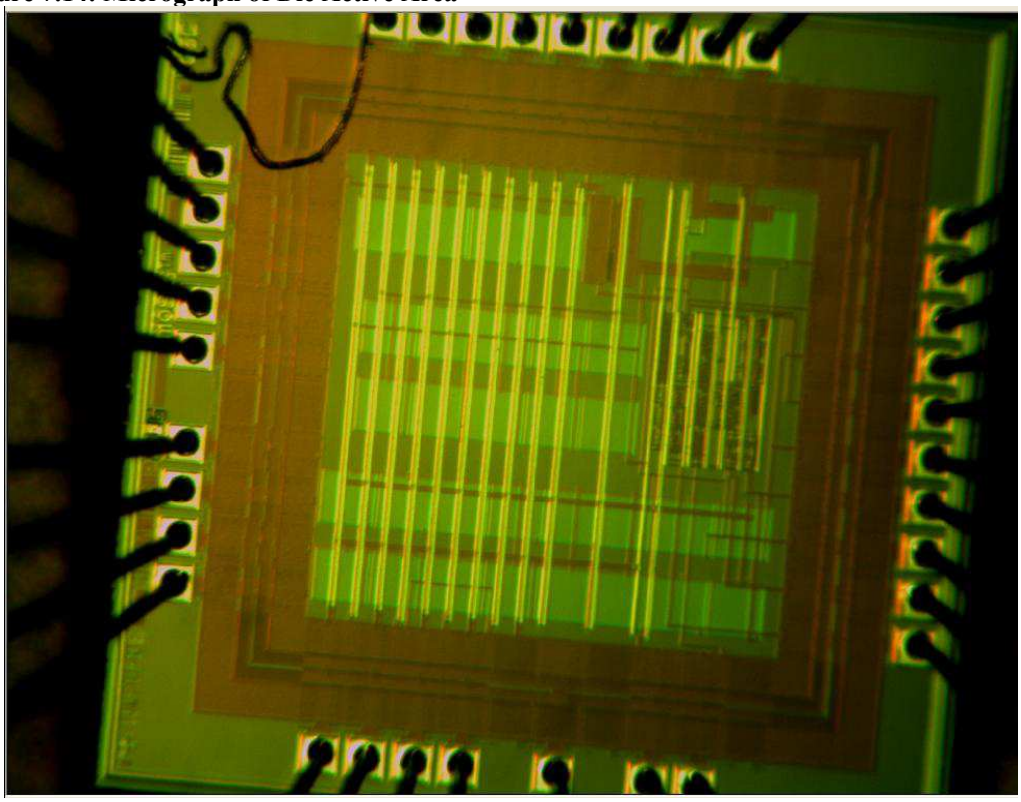

Figure 7.15: Micrograph of Die with Pad Frame

7.5.1: Test results with 140MHz IF SAW device

The chip was tested using a PC board incorporating the 140MHz IF SAW filter in the loop and the test results were compared to our simulation results using the s-parameter model of the filter. For test we set V_{dd}= 3V, V_c=1.2V, V_{bias}=V_{dd}/2, V_{refhi}=0.8V_{dd} and V_{reflo}=0.3V_{dd}. Simulation setting of V_c was 1.32V so as to obtain the same V_f tuning range as in the experiment.

With these settings we first measure the VCO fine gain in open loop mode by varying the fine input voltage and measuring the output frequency. In the range of 0.8V to 2.8V an inverse linear relationship is observed between the fine input voltage and the frequency since the effective NMOS capacitance increases with gate voltage. Below the device threshold the curve flattens out as the VCO NMOS varactors lose voltage dependency. Experimental and simulation results are compared in Fig. 7.16. Experimental results show good agreement with the simulation results with respect to the VCO fine input sensitivity which is determined to be 16.8MHz/V for experiment and 15.8MHz/V for simulated at the typical process corner.

Next the loop is closed and finite state machine output, the analog sensor output node and the regulated SAW frequency are measured. Shown in Fig. 7.17 are transient oscilloscope plots of the low frequency sensor output and the finite state machine output. We confirm from Figs. 7.16 and 7.17 that when the loop is in regulation for a given setting of the coarse control voltage (V_c), the average value of the chip output will correspond to the upper edge of the SAW passband as detectable by the comparator. We further confirm that in steady state the FSM output will toggle for each transition to and from the passband.

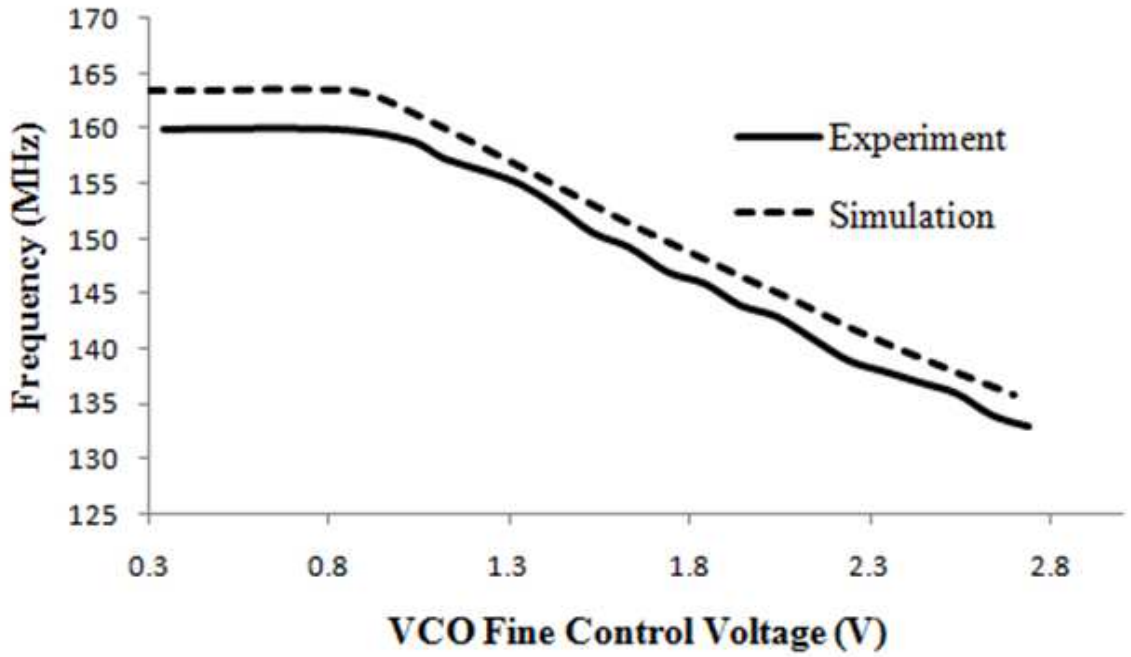

Figure 7.16: VCO fine input gain: Simulated vs. Experimental Results

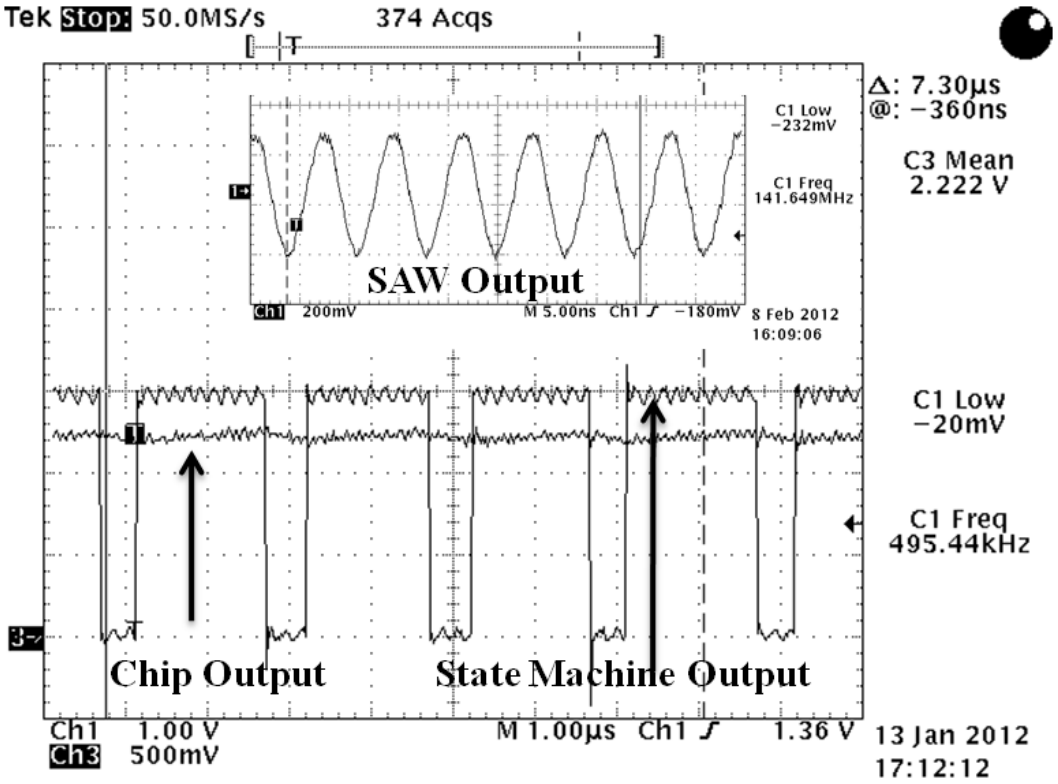

Figure 7.17: Experimental waveforms of sensor and state machine outputs.

In addition to the normal operating mode where the VCO fine input toggles in mid-range, there are additional modes of operation.

The first mode arises when the adjustable threshold of the comparator is set below the optimal range. In this case the comparator output will be continuously high. The state machine will start from Preset mode. However, since the FSM input is already high, the FSM output will toggle, causing the RC output to reverse slope and trip the preset comparator. This will cause another reversal of slope of the output voltage and the cycle will repeat. The oscillation period will be determined by the hysteresis limits of the comparator and the RC filter time constant. This mode of operation is illustrated in Fig. 7.18.

In the second alternate mode the adjustable threshold of the comparator is above the optimal range or the SAW center frequency has shifted to a point where the peak level shifted SAW output is below the comparator threshold for the entire range of the VCO fine input. In this case the comparator output will be always low. In this case the RC output will ramp up, thus sweeping the SAW input frequency. However, since the comparator output will remain low for the swept range, the slope will not reverse and the ramp will reach the reset threshold. At this point the reset comparator will trip causing the ramp slope to reverse and trace back to the preset threshold. An oscillatory mode will thus be set up with the period being determined by the RC time constant and the reset and preset thresholds. This mode is illustrated in Fig. 7.19.

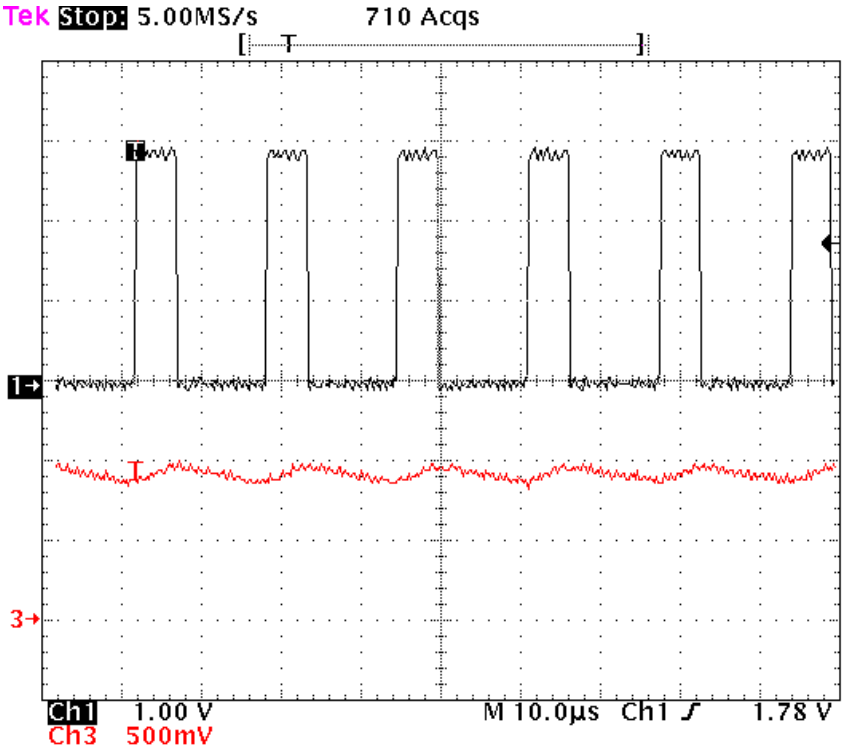

Figure 7.18: Experimental waveforms of alternate mode where comparator threshold is below range.

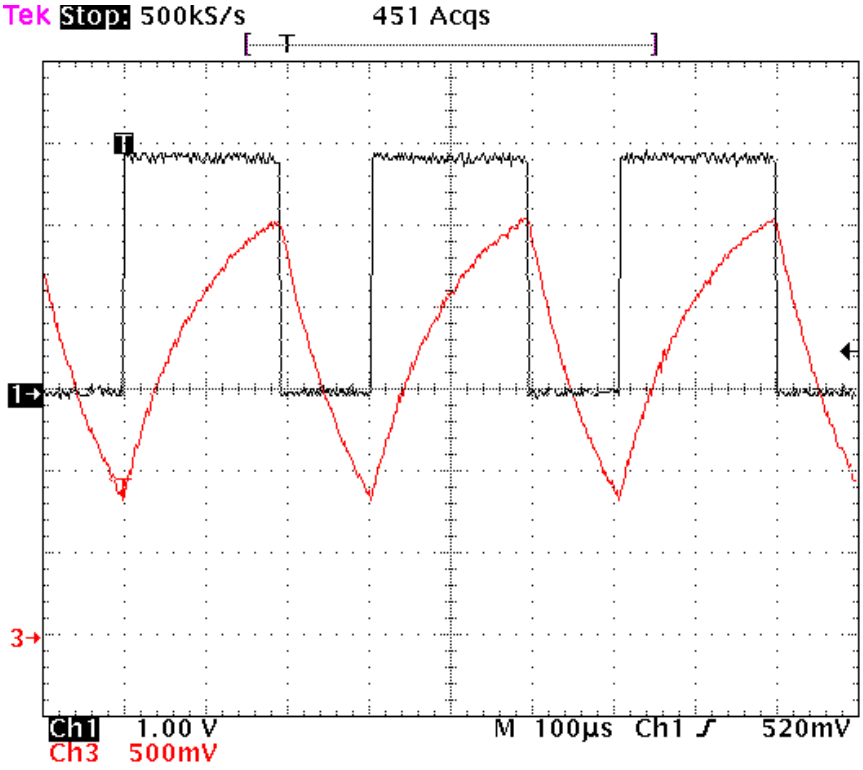

Figure 7.19: Experimental waveforms of alternate mode where SAW frequency is out if range.

7.5.2: Test results with 70MHz IF SAW device

To prove experimentally the concept of using the readout for SAW devices operating at multiple frequencies, we also tested the chip with a 70MHz IF SAW filter manufactured by Triquint. This is the same device for which we have shown simulation results. The bench testing was done with roughly the same settings as the simulation. We measured the mean, minimum and maximum values of the sensor output for three different settings of the coarse control. We also observed the change in duty cycle of the state machine output under these conditions.

In Figure 7.20 we have captured an oscilloscope plot of the chip output and the state machine output for a V_c setting of 1.8V. The settings of V_{bias} and V_{refmid} are 1.52V and 1.66V respectively. Under these conditions, consistent with simulation results, the output is observed to ramp between limits which, in this case are measured to be 1.435V and 1.707V. In Figure 7.21, the same capture is done in average sampling mode which enables us to extract mean and ramp minimum and maximum measurements without noise interference.

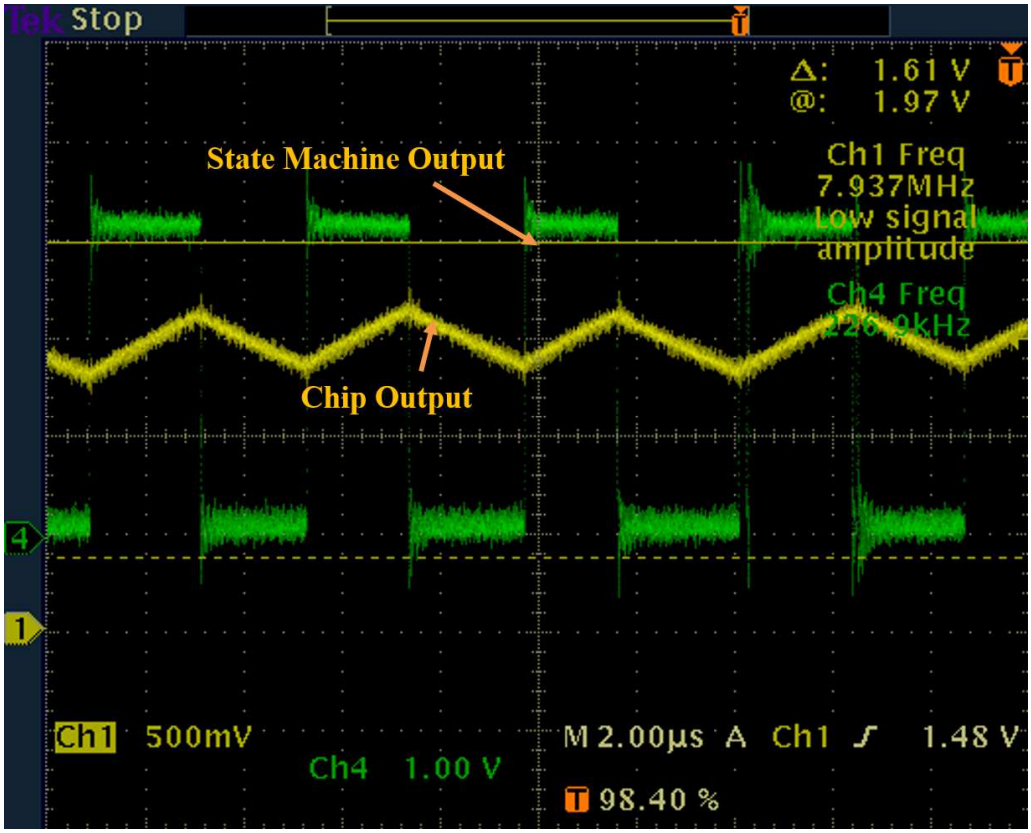

Figure 7.20: Capture of Chip Output and State Machine Output for V_c= 1.8V

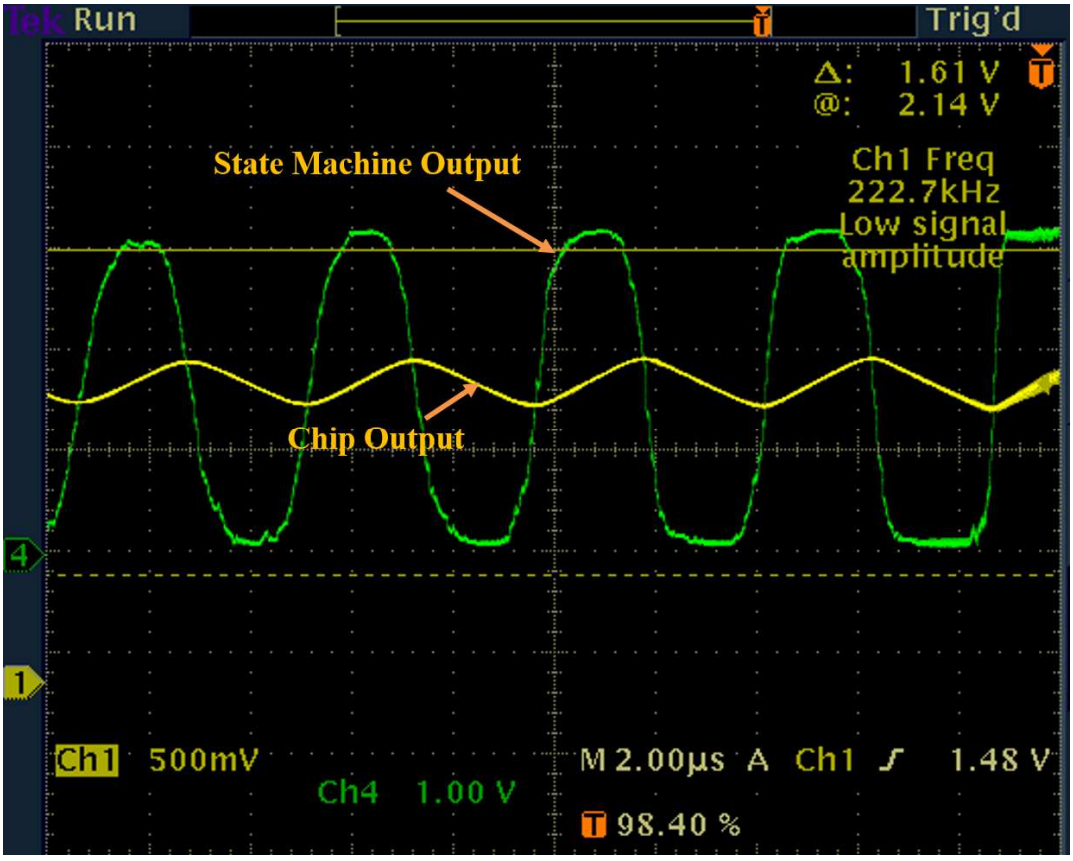

Figure 7.21: Capture of Chip Output and State Machine Output for V_c= 1.8V: Averaging Mode

Shown in Figure 7.22 is a capture of the envelope of the SAW output triggered from the chip output. The amplitude is observed to decay sharply as the time varying frequency exits the passband. This behavior is consistent with simulation results (Figure 7.8).

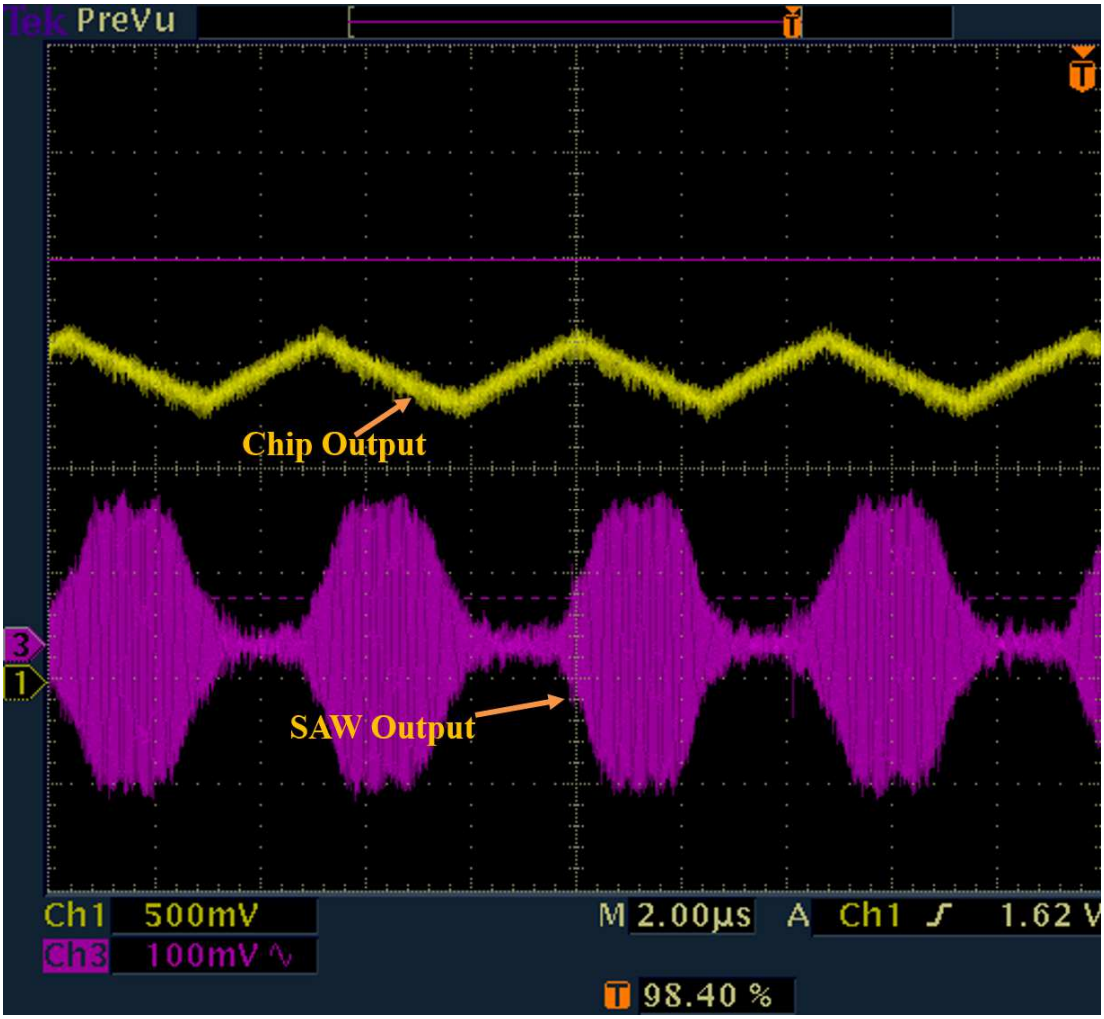

Figure 7.22: Capture of SAW Output and Chip Output for V_c= 1.8V

In Figure 7.23 we observe an oscilloscope plot of the chip output and the state machine output for a V_c setting of 1.79V. The plot is in averaging mode. For this setting the ramp minimum and maximum limits are 1.5712V and 1.904V.

Figure 7.24 shows a similar plot for a V_c setting of 1.78V. The ramp limits in this case are 1.66V and 2.2V with noise interference. In averaging mode, the limits are measured to be 1.75V and 2.004V respectively.

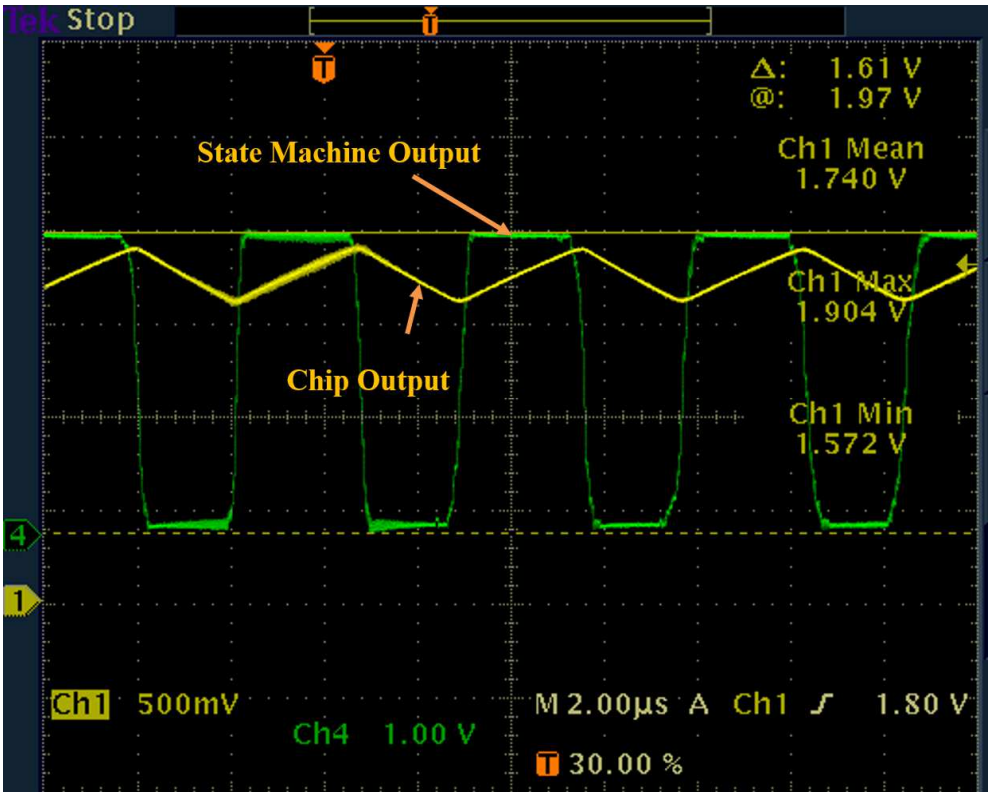

Figure 7.23: Capture of Chip Output and State Machine Output for V_c= 1.79V

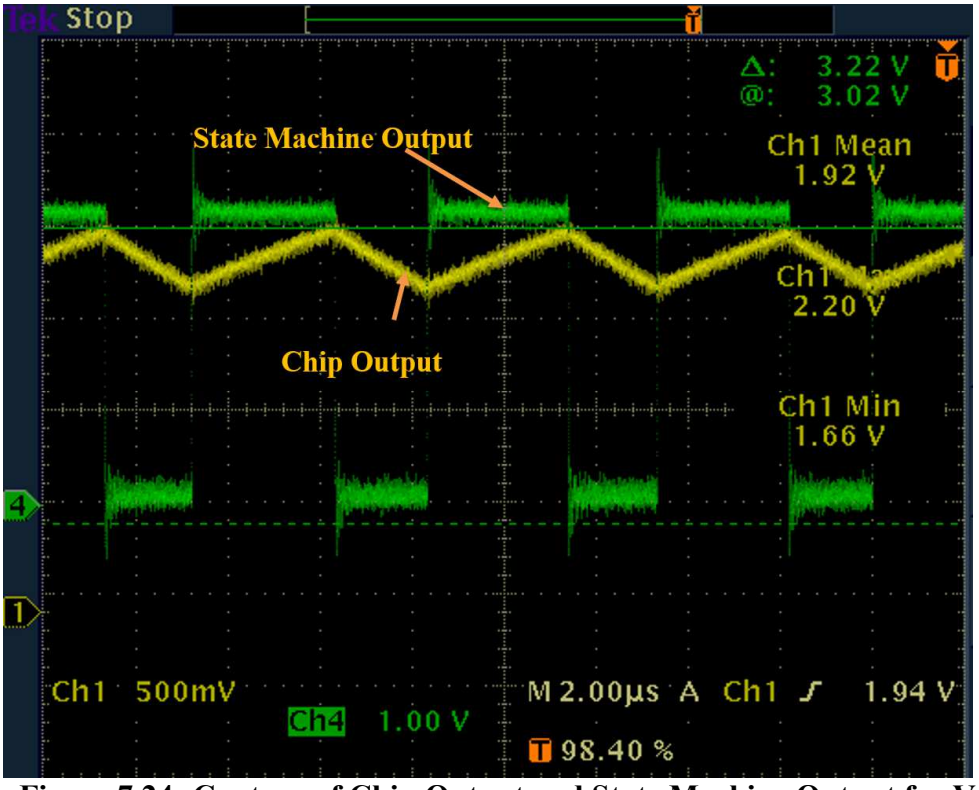

Figure 7.24: Capture of Chip Output and State Machine Output for V_c= 1.78V

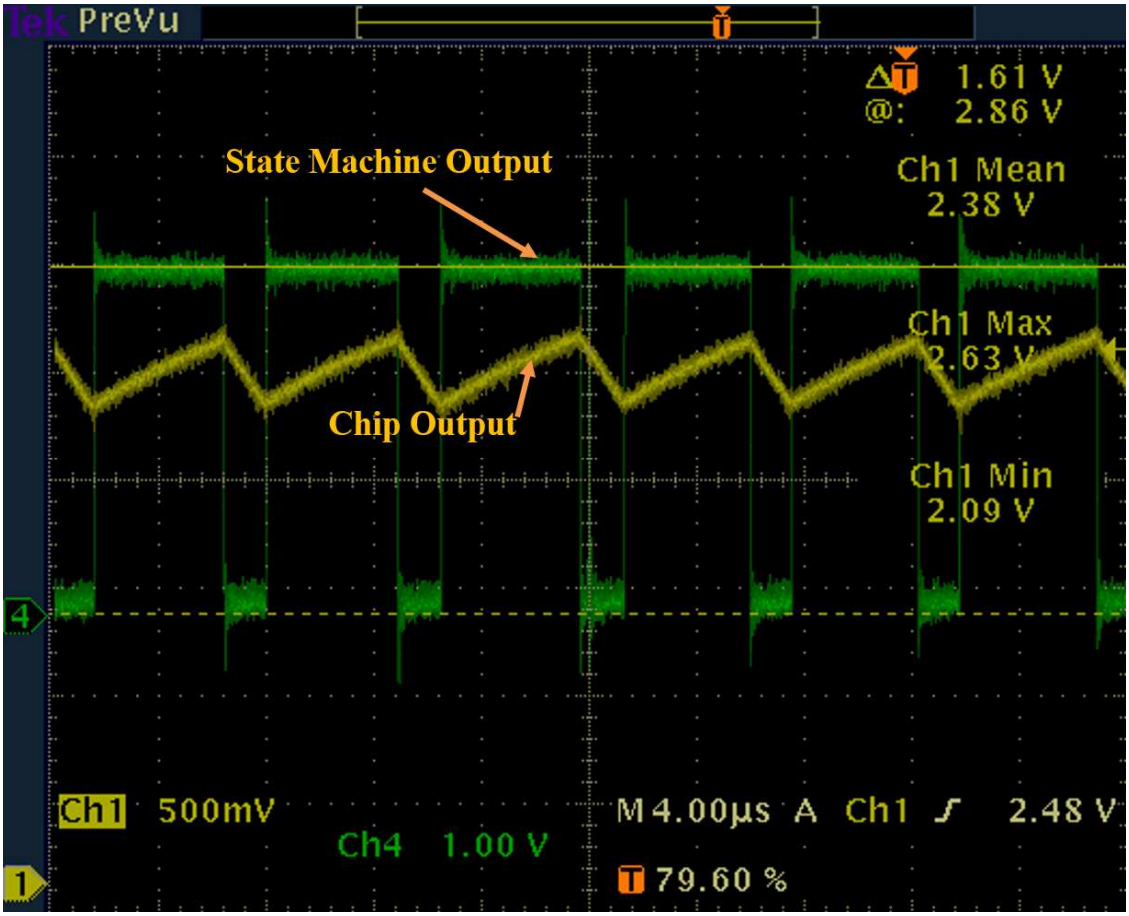

Figure 7.25: Capture of Chip Output and State Machine Output for V_c= 1.765V

In Figure 7.25 we have a plot of the chip output and state machine outputs for a V_c setting of 1.765V. In averaging mode the ramp limits are 2.169V and 2.511V. Consistent with derived results the higher setting of the ramp average results in a higher duty cycle.

The FFT of the waveforms at the SAW output and the VCO output are shown in Figure 7.26 and Figure 7.27 respectively. In both cases the peak occurs at 72.5MHz which is consistent with the upper edge of the passband as determined by the comparator threshold.

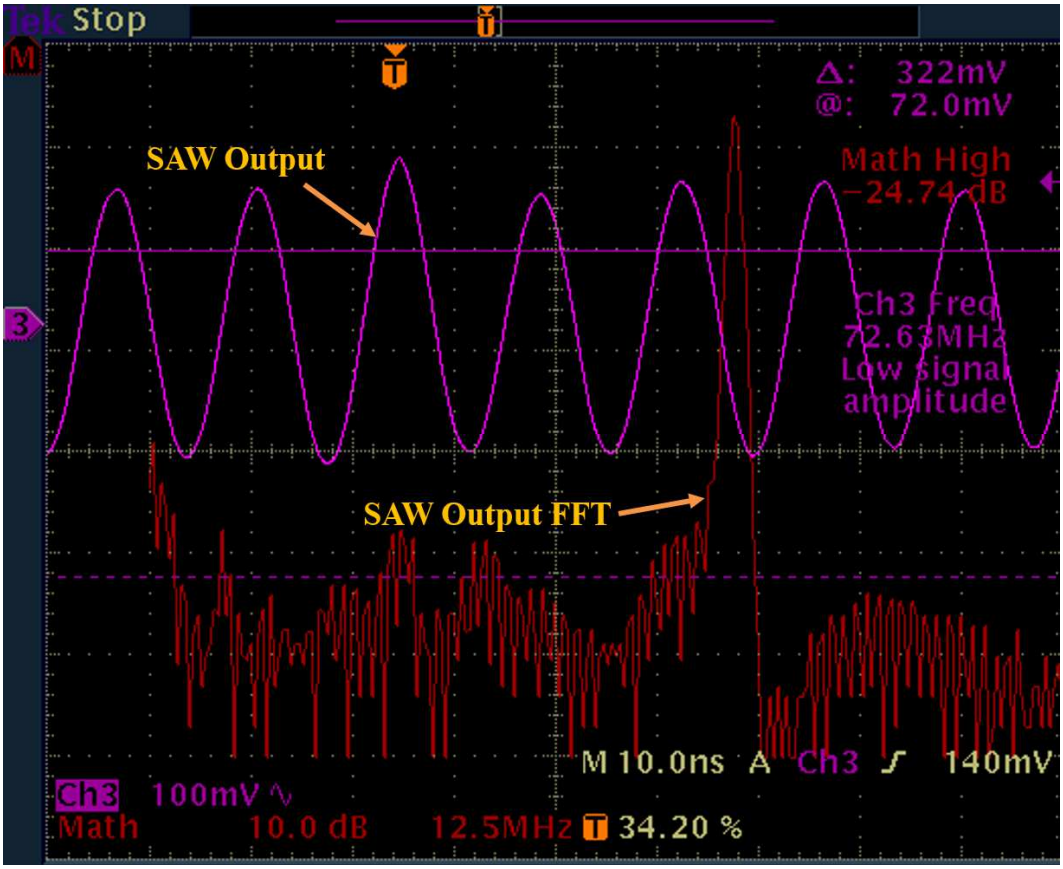

Figure 7.26: Capture of SAW Output and its FFT

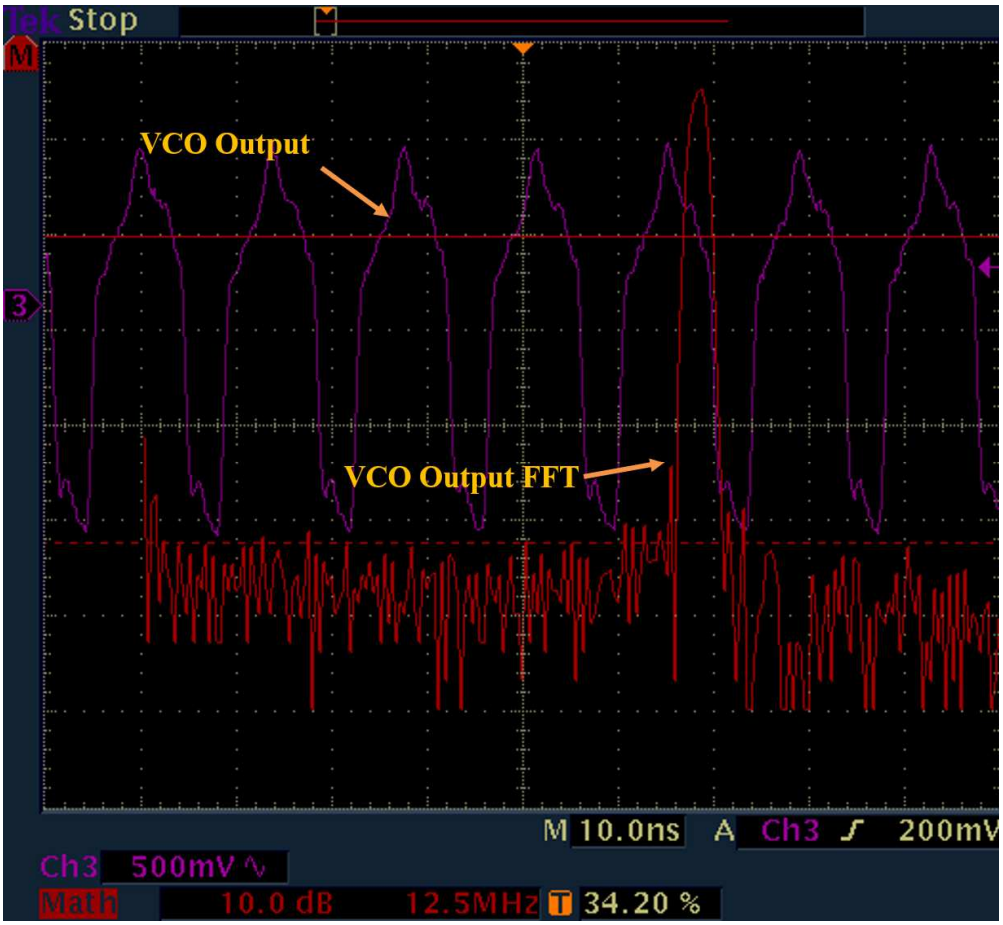

Figure 7.27: Capture of VCO Output and its FFT

Table 7.2: Summary of Experimental Results for 70MHZ SAW device. T_{on} and T_{off} represent the high and low durations respectively of the FSM output

	Output mean	Output maximum	Output minimum	T_{on}	T_{off}
1.8	1.577V	1.707V	1.435V	2.2µs	2.4µs
1.79	1.858V	2.031V	1.704V	2.8µs	2.05µs
1.78	1.91V	2.004V	1.75V	2.9µs	1.8µs
1.77	2.2282V	2.411V	2.113V	3.8µs	1.8µs

In Table 7.2 we have summarized some findings from experimental measurements conducted on the readout incorporating the 70MHz IF SAW device. Increasing V_c results in increasing output mean. With increasing output mean the output duty cycle also increases. The total time period remains of the order of four times the SAW phase delay, though increasing gradually with higher output.

Section 7.6: Summary

Here we have presented simulation and experimental results of the primary sensor loop. The loop was evaluated with a SAW device operating at 374MHz and TSMC 0.35μm process models. In steady state operation the device frequency variation limits were confirmed to be centered at the upper edge of the passband as determined by an adjustable threshold. The upper frequency limit was obtained to be 388.9 MHz. The variation limits are also dependent on the RC time constant. We also simulated the loop with a 140MHz SAW device and AMI 0.5μm process models. In both cases noise was injected through the supply and the jitter and statistical variation of the output was determined. Using the same process models we simulated the readout with a 70MHZ IF SAW filter in the loop. For this case simulations were run at multiple settings of the coarse voltage, each of which yielded a different mean chip output. The mean, minimum and maximum of the ramp were measured under these conditions. The duty cycle was also measured and sound to have the predicted relationship with the equivalent threshold corresponding to the passband edge.

Experimental results were measured using a chip fabricated in the AMI 0.5μm process. This chip was incorporated in two printed circuit boards, one for operation with a 140MHZ SAW device and the other with a 70MHZ device. Experimental results were then obtained by testing these two configuration. The results show close agreement with simulation results with respect to measured VCO fine gain for comparable coarse setting. Transient oscilloscope plots showing functionality under various modes of operation also validate simulation results under similar settings.

Chapter 8: Design and Analysis of Secondary Sensor Loop

8.1 Introduction

The delay to digital converter converts the sensor output voltage to an equivalent digital output by quantizing the delay between successive changes in the slope of the instantaneous VCO frequency. It can be seen from Fig. 6.14 that this delay is of the order of twice the sum of the SAW phase delay and the circuit response delay of which the SAW phase delay is by far the dominant term. Further, from Figure 6.14, a change of slope of the sensor voltage output corresponds to a transition of the SAW through the upper edge of the passband and is indicated by a toggle of the comparator output.

From Fig. 7.2, the delay to digital converter consists of three major blocks. These are a control logic block, a modified up/down counter block and a time to digital converter.

8.2: Control Logic Block

The control logic block encapsulates a second finite state machine which creates inputs to the UDC and TDC for conversion. Table 8.1 lists the transitions of this FSM. The states as enumerated here are “Load”, “Count up”, “Lock: TDC”, “Count Down” and “Lock: No TDC”. The state transitions are controlled by two inputs which are the calibration enable and the comparator output. The latter signal is generated by the primary sensor loop.

Table 8.1: State transition table of conversion control block

State	Load	Count Up	Lock:TDC	Count Down	Lock: No TDC
Load	Calibration =1	Calibration =0, Comparator o/p=1			
Count Up	Calibration =1	Calibration =0, Comparator o/p=1	Calibration =0, Comparator o/p=0		
Lock: TDC	Calibration =1		Calibration =0, Comparator o/p=0	Calibration =0, Comparator o/p=1	
Count Down	Calibration =1		Calibration =0, Comparator o/p=1		Calibration =0, Comparator o/p=0
Lock: No TDC	Calibration =1	Calibration =0, Comparator o/p=1		Calibration =0, Comparator o/p=0	

Based on this table we note that the FSM starts from an initial load condition enabled by the calibration input. From this state it transitions to the up counter mode when the calibration enable goes low. On transition out of the passband indicated by the comparator output going low, the counter locks in the count value and simultaneously registers the time to digital conversion output. On the next comparator toggle the counter counts down from the previous locked value. The down counter stops when the comparator output returns to low and locks in the count. In this state the TDC outputs are not registered. We return to the up count mode on the next toggle of the comparator and the cycle repeats. The circuit schematic of the entire FSM block including the primary loop FSM is shown in Fig. 8.1. The up/down mode

control is represented by CSEL while the TDCSTOP signal indicates the stop trigger to the TDC.

It is seen that the control outputs CSEL and UDCLOADN are synchronized to the rising edge of the FSM input COMP_OUT. This implies the count direction will alternate only on these rising edges. On the other hand the falling edge will asynchronously turn the TDCSTOP signal on for immediate time to digital conversion. This falling edge will also signal the end of the current count cycle.

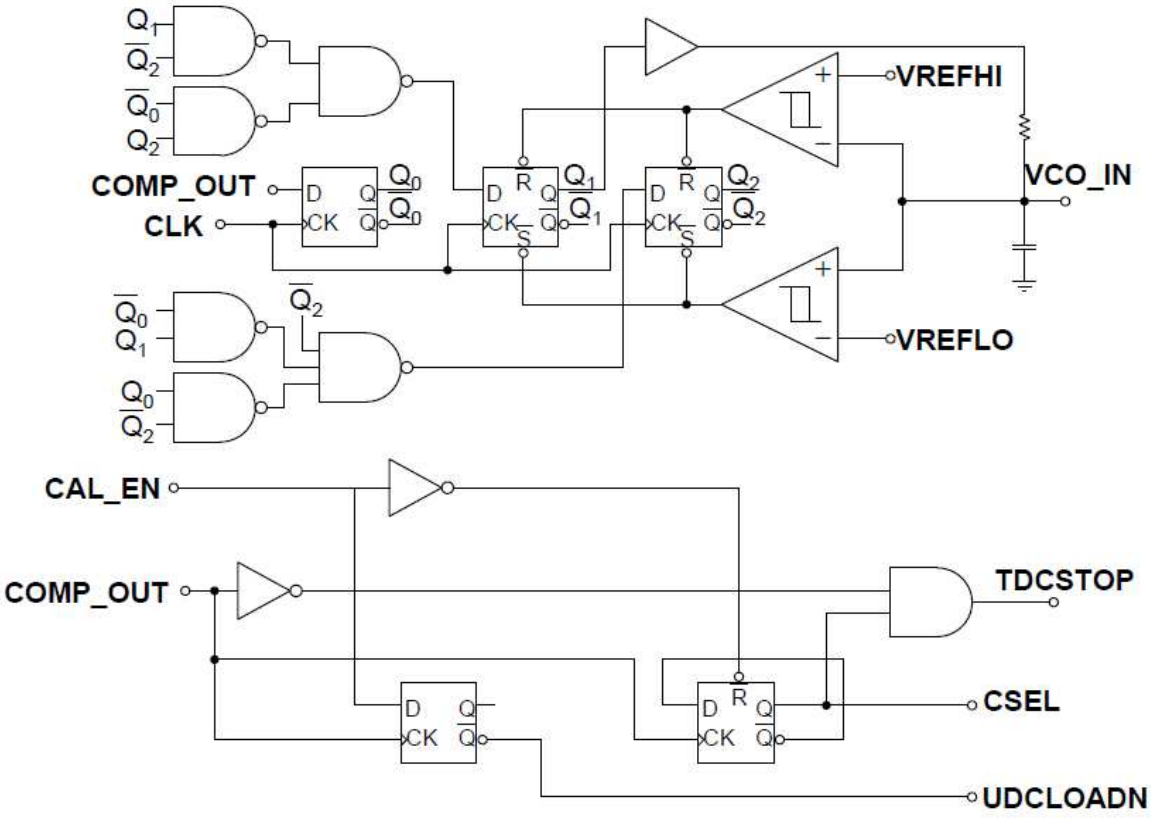

Figure 8.1: Complete Finite State Machine Implementation

Section 8.3: Modified Up/Down Counter

The counter is equipped with load, count up, count down and lock/hold modes. The load mode is enabled when the LOADN control signal is low. In this mode a fixed value is loaded into the counter flip flops. This ensures that the start

count is a known value. The count mode is controlled by the CSEL and LOCK control inputs. The LOCK input needs to be low for either count up or down. In the up count mode the CSEL input is high. The counter counts up till the count stop signal CSTOPC is asserted and the LOCK input remains low. On the other hand in the down count mode the counter decrements from the current value till CSTOPC signal is asserted. In case the maximum or minimum count value is reached, the counter does not count cyclically but retains the extreme value till the count direction is reversed. In the lock mode the existing counter value is retained until either count mode is enabled.

In normal operating mode the counter will go through an initial load followed by alternate count up and down cycles. In the absence of noise or a sensor event causing a shift, the count up and count down intervals will be identical. This will result in the counter returning to the initial load value after a period dictated by the SAW phase delay.

The schematic of the UDC is shown in Fig. 8.2. This schematic uses arrayed instances and signals. The main counter D flip flops are denoted by UD<0:5> which are synchronously clocked. The D inputs to these flops are denoted by D<0:5> and the corresponding outputs and complementary outputs are denoted by Q<0:5> and QC<0:5> respectively. The finite state machine logic internal to this counter are implemented with an array of custom AND and NAND gates which receive the flop outputs as inputs. Separate FSM logic arrays are implemented for the up count and the down count branch. Each of these arrays generate a set of intermediate signals denoted by UT, UCMUXN and DT, DTMUXN which are routed to a multiplexer

array. The multiplexer output select is the CSEL input. An XOR array followed by a final gating stage controlled by the LOCK input generates the D input array to the flip flops.

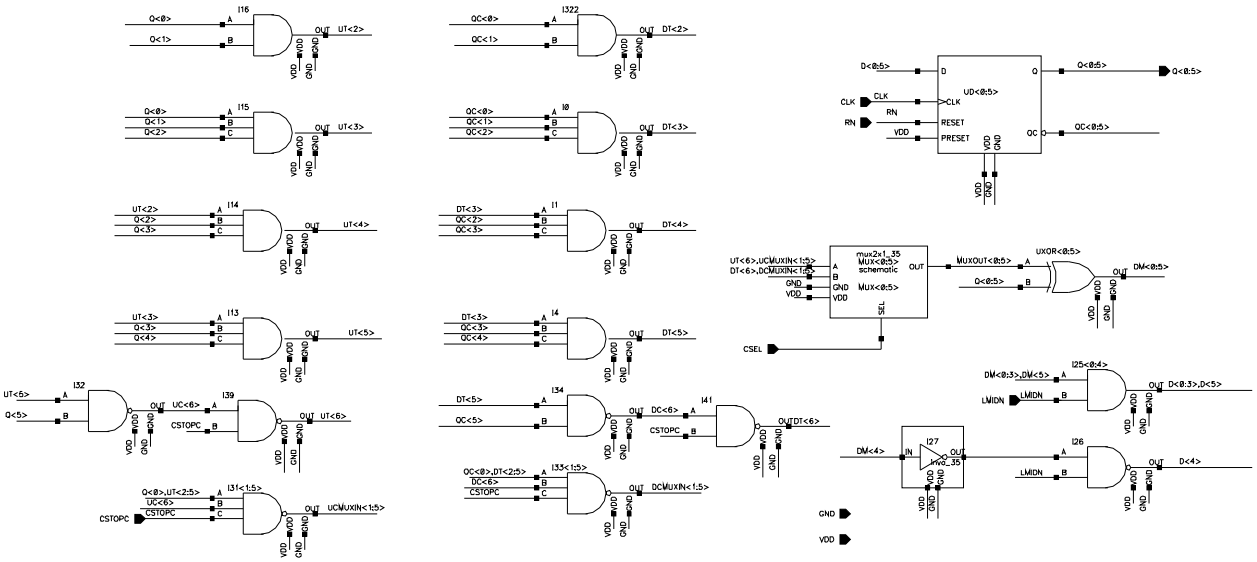

Fig 8.2: Modified Up/Down Counter Schematic

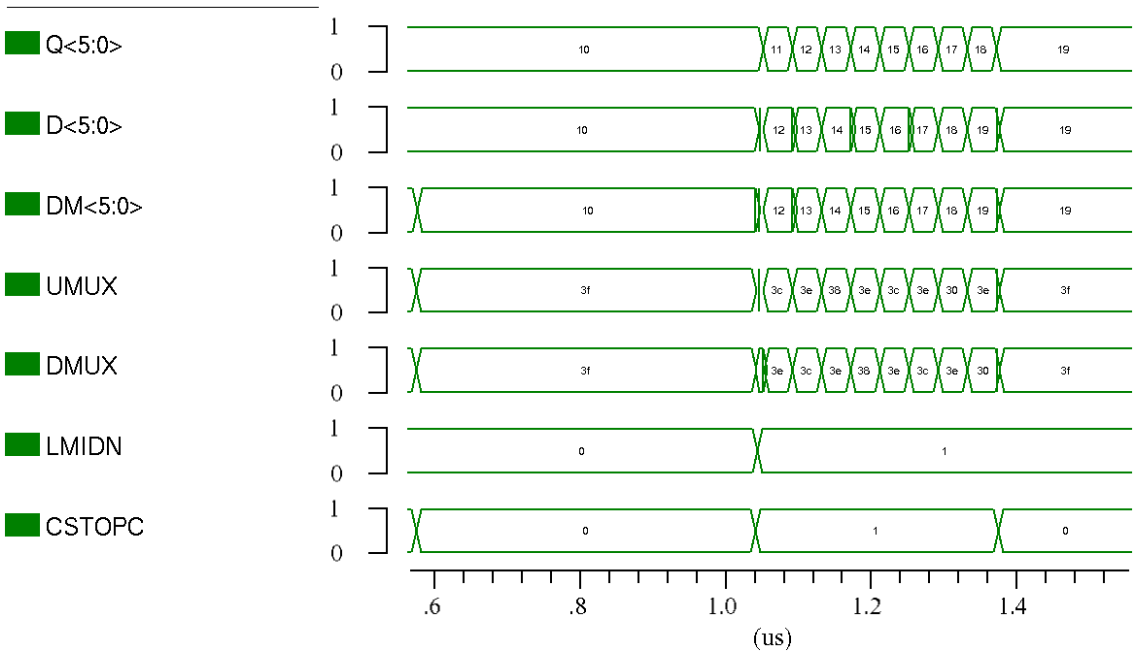

Fig 8.3: Node transitions during up count and load

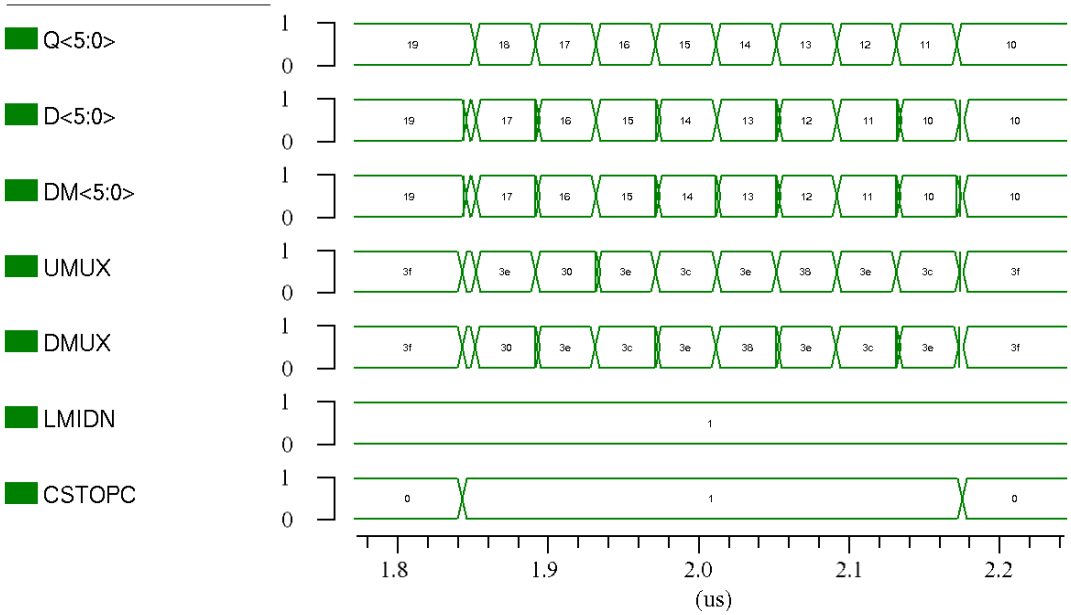

Fig 8.4: Node transitions during down count mode

The internal node transitions during up count and down count modes are shown in Figures 8.3 and 8.4 respectively. The XOR output bus is denoted by DM. The DMUX and UMUX buses are the input buses to the multiplexer array. The count starts when CSTOPC toggles high and stops when the same control signals returns to low. The two modes are distinguished by the multiplexer selection.

Section 8.4: Time to Digital Converter

The time to digital converter provides a fine resolution to conversion by quantizing the delay between the last synchronous count and the asynchronous comparator output going low. The positive edge of the counter clock serves as the start signal of the TDC while the comparator output in up count mode is the stop signal that latches the TDC outputs. A typical delay to digital conversion is shown in Fig. 8.5.

In this standard topology of time to digital conversion, the start signal is propagated through a chain of TDC cells or buffers where the stage delay is

controlled by a varactor voltage. This voltage input is represented by V_F. A higher varactor voltage increases the stage delay by increasing the capacitive delay at the output. The stage outputs are represented by DP<15:0>. These pre-latch outputs are triggered successively after the start signal rising edge and serve as the data inputs to the array of D flip flops. The latching occurs at the TDCSTOP signal which is buffered to act as the clock input to the flip flop array. All data rising edges which arrive after the clock edge will thus fail to trigger the corresponding flip flop. A thermometer code will thus be generated with all flip flop outputs for which the data edge precedes the clock edge going high. On the other hand, outputs will be held low in the case of those flip flops in the array for which the data edge trails the clock edge.

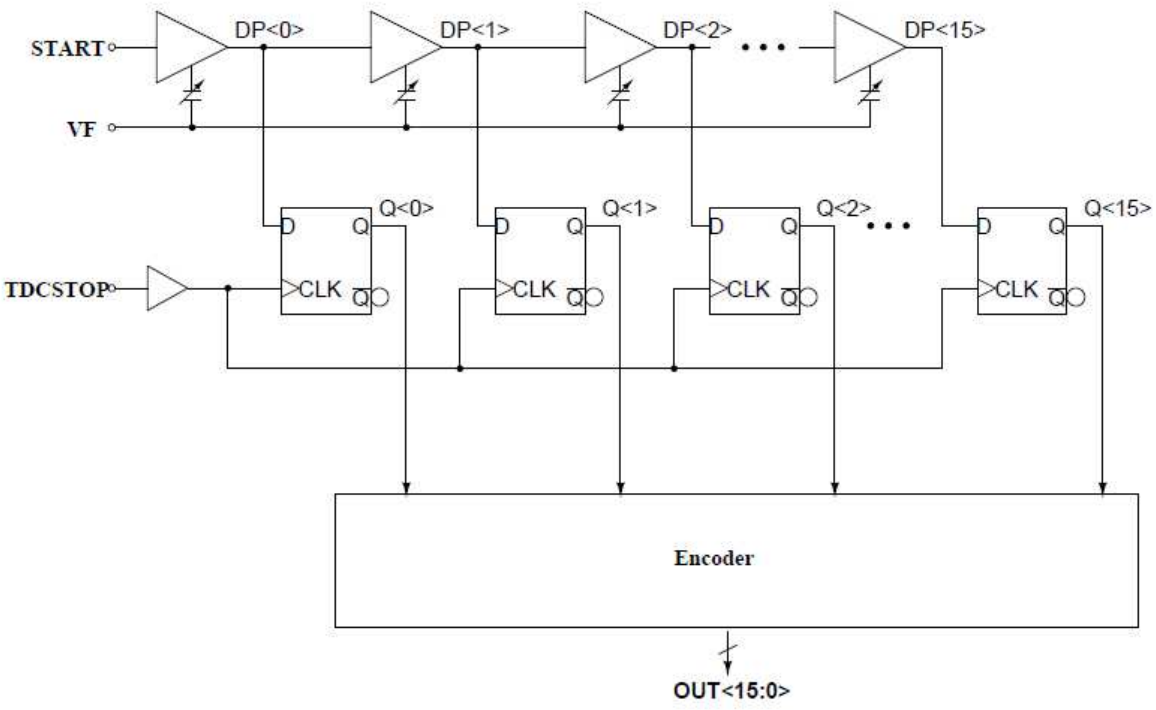

Figure 8.5: TDC Top level diagram

A multiplexer based thermometer to binary converter delivers the TDC output bus. The same TDC stop signal is also used to latch the counter outputs to create a composite bus comprising both UDC and TDC outputs.

The digital transient waveforms are shown in Fig. 8.6. The conversion is launched at the rising edge of the divided clock signal and is complete at the rising edge of the TDCSTOP signal. Note that the latched outputs are not reset at the start of the next conversion cycle. On the contrary, they will only change if the ensuing conversion provides a result different from the conversion result. The pre-latch internal nodes DP<15:0> will, however, launch on every cycle.

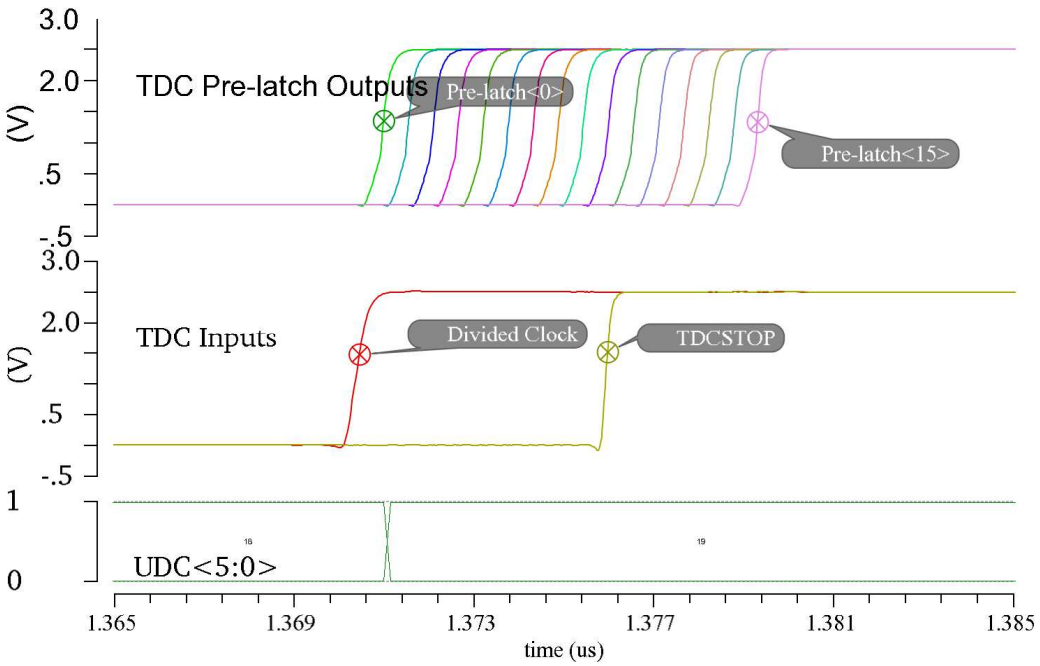

Figure 8.6: TDC internal pre-latch outputs

The layout floor plan of the TDC is shown in Fig. 8.7. The layout is vertically compartmentalized into the TDC core and the encoder. The TDC core contains a chain of delay cells and D Flip-flops. The varactor voltage is routed to all delay cells while the buffered TDCSTOP signal is routed to the clock input of all flip-flops. In

the encoder section the multiplexers are arranged in a pyramidal scheme, mirroring the circuit schematic. The actual physical layout is shown in Fig. 8.8.

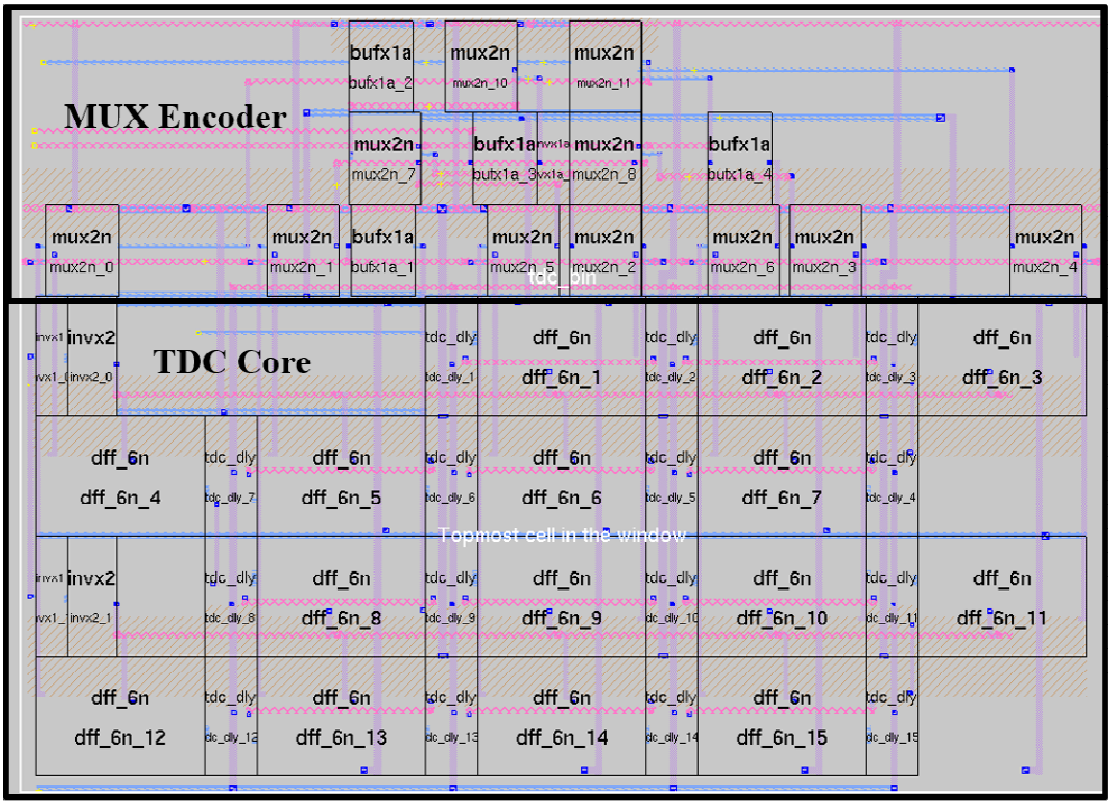

Fig. 8.7: Layout floor plan of time to digital converter

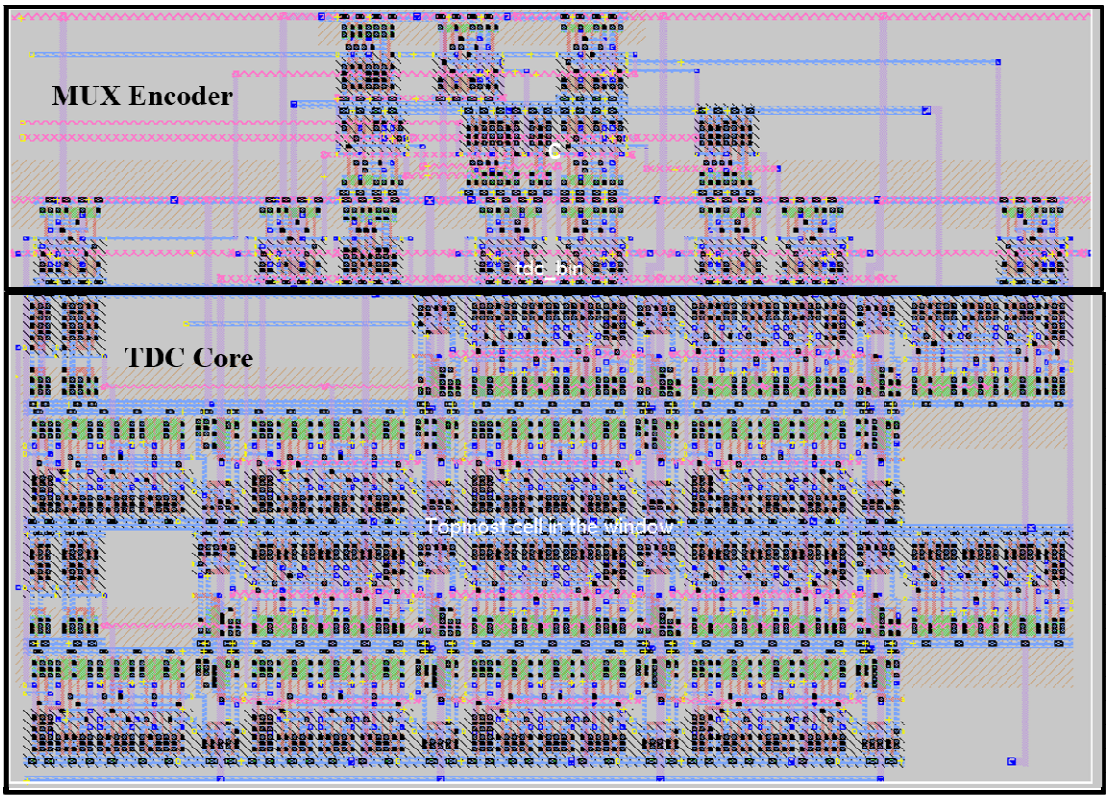

Fig. 8.8: Physical layout of time to digital converter

Section 8.5: Summary

Here we have presented the topology and architecture of the secondary sensor loop which converts the RC filter time delay between SAW band reversal events into a 10 bit digital output. A direct conversion of the sensor output voltage was also possible using a high resolution ADC converter, using, for example, a successive approximation topology. However, this would not have been the most optimal solution since it would have loaded the sensor output. In addition, there would be significant circuit and area overhead. In this implementation the conversion uses the time delay properties inherent in the architecture and relies on time to digital conversion.

The delay to digital converter consists of three major blocks. These are a control logic block, a modified up/down counter block and a time to digital converter. The control logic block produces the necessary control signals for the operation of the counter and the time to digital converter. As inputs it receives the comparator output, the FSM output and the core FSM clock from the primary conversion loop. The modified up/down counter counts up or down depending on the count select signal. In addition, there are lock and hold modes during which count is stopped and the current counter value is retained till the next count cycle. A load signals enables initial loading of the counter during the calibration sequence. The time to digital converter which is the essential fine conversion block consists of a traditional delay chain topology with a varactor voltage for tuning of the stage delay and expanding or compressing the range of conversion. The positive edge of the counter clock serves as the start signal of the TDC while the comparator output in up count mode is the stop signal that latches the TDC outputs. A multiplexer based thermometer to binary converter delivers the final TDC output to the fine conversion bus.

Chapter 9: Experimental and Circuit Simulation Results of Secondary Sensor Loop

9.1 Introduction

Simulations of the primary sensor loop and the secondary loop were carried out using TSMC process models and S parameter models of the SAW device. The system level testing was carried out with the S-parameter model of a commercially available SAW device centered at 140 MHz with an insertion loss of 7.5dB [20]. Testing is intended to prove the concept of using the finite state machine to trigger the secondary readout circuit while the primary loop is running. As in the case of primary loop simulations, the open loop frequency should be measured first by disconnecting the connection between sensor output and the RC filter and directly forcing the sensor output pin to an approximate mid-rail voltage. This will establish the fine input voltage of the VCO. Then the coarse VCO voltage should be swept till the VCO output frequency matches the SAW band center. Now the loop can be connected and closed loop observations can be made. Functionality was first established by measuring the closed loop SAW output frequency and the analog output voltage. Then the digital outputs are measured to verify delay to digital conversion.

Further simulations and measurements were carried out at the block level to verify transitions between states and performances of individual blocks. Such simulations can give access to internal nodes and will establish functionality and

performance of the up/down counter, the time to digital converter and the secondary finite state machine.

9.2 Test Chip Fabrication

A test chip was fabricated using MOSIS 0.5µm AMI_C5N process. The core circuit area layout of the primary loop was 306µm by 216µm while the entire readout including the decoupling capacitance and buffers was contained in a standard 1.5mm^2 die frame. The micrograph of the fabricated chip is shown Figure 9.1. The secondary conversion section of the chip is shown in Figure 9.2.

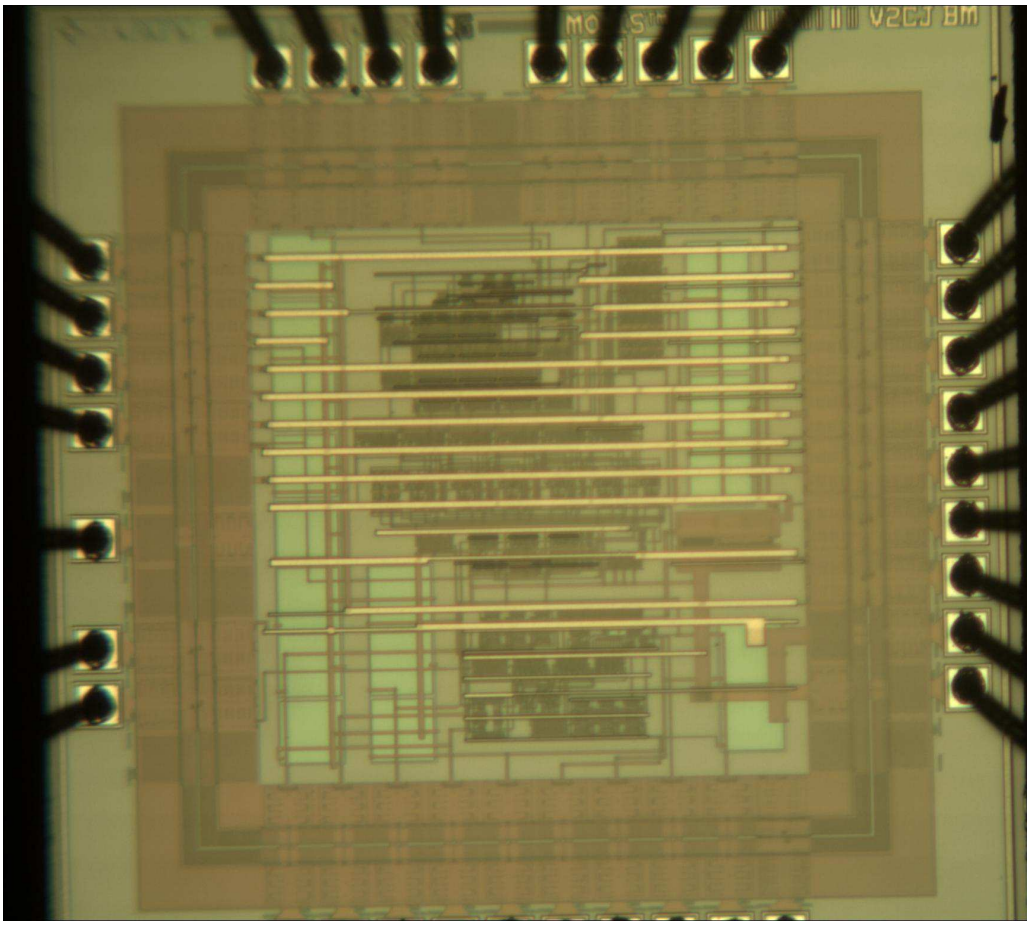

Figure 9.1: Die Micrograph

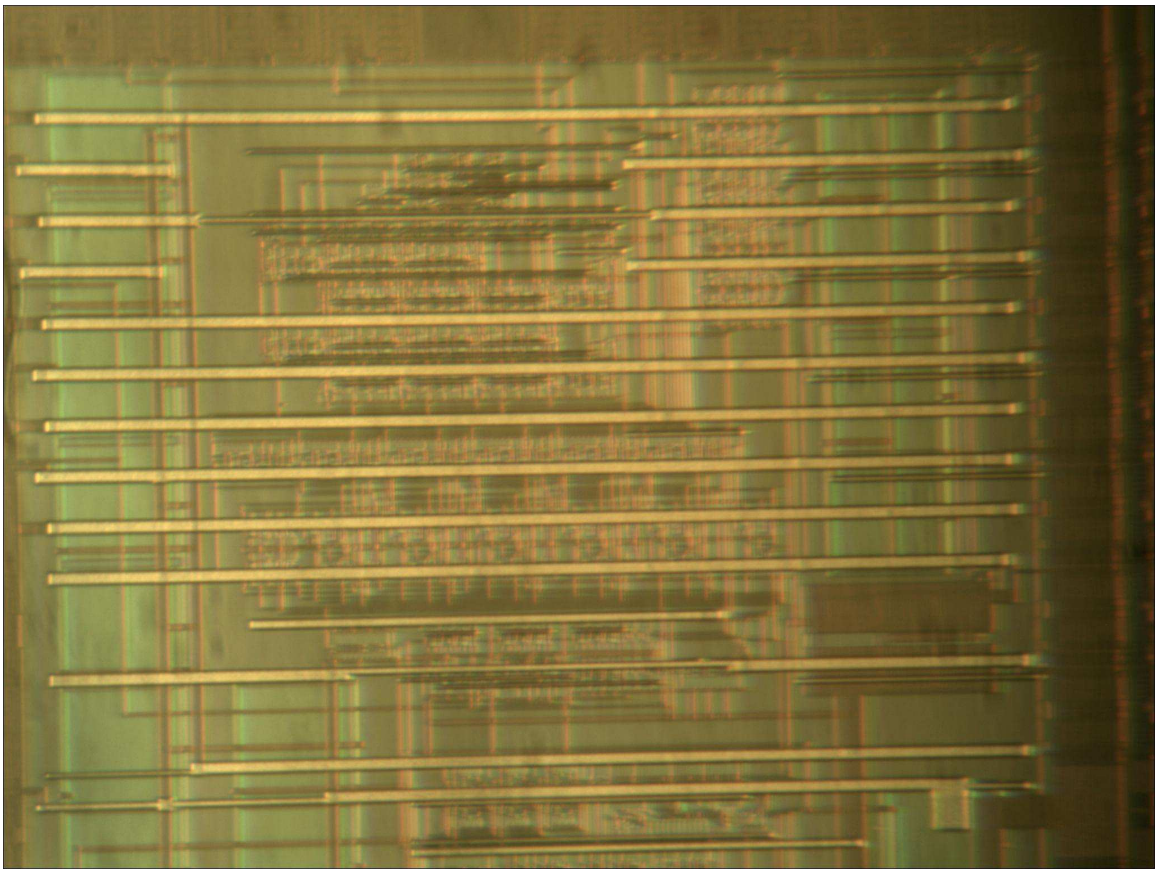

Figure 9.2: Micrograph of Secondary Conversion Circuit

The chip was tested using a PCB incorporating a 140MHz IF SAW filter in the loop. The PCB layout showing the surface mount IF SAW device with input and output matching components and the test chip fabricated in a DIP package is shown in Fig. 9.3. Test results were compared to simulation results using the S parameter model of the filter [19], [20].

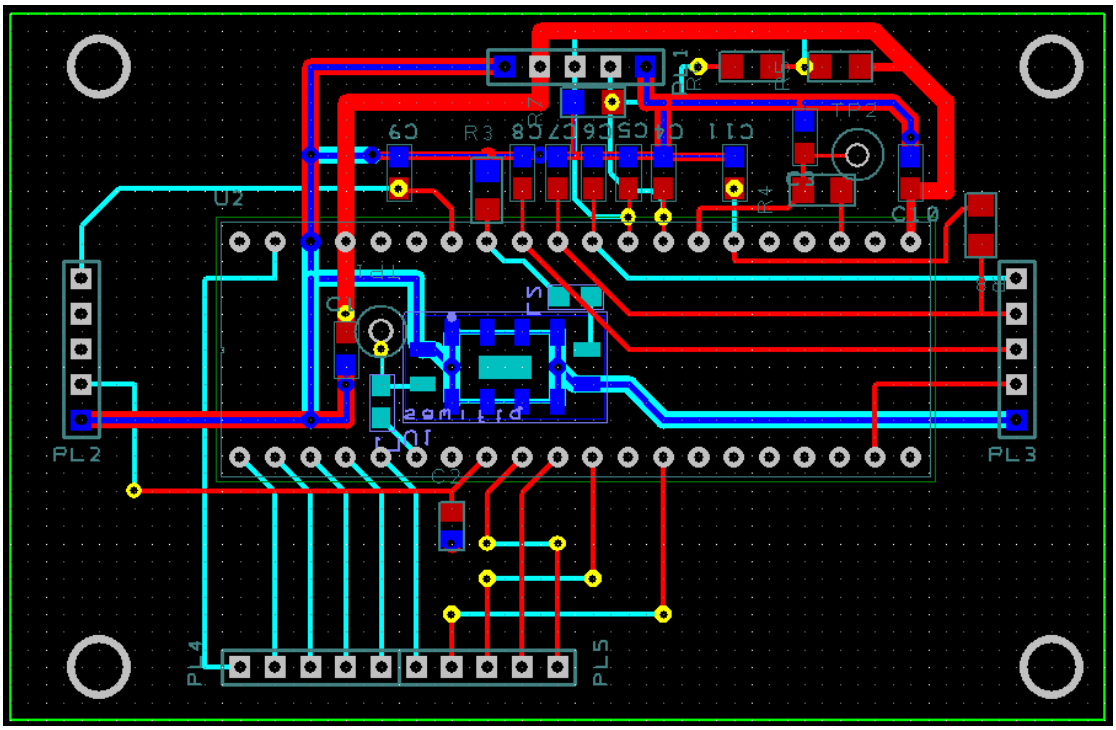

Figure 9.3: PCB layout of test chip

9.3 System Test Results

System simulation was carried out with 0.5µm AMI_C5N device models and an IF filter operating at 140MHz with insertion loss of 7.5dB [20]. The steady state transient signals are plotted in Fig. 9.4. For this example, a coarse voltage (V_c) setting of 1.32V was selected. The SAW output frequency variation in steady state was observed to be between 143.4 MHz and 146.4 MHz while the corresponding analog output ranged from 1.9664V to 2.1476V.

The pre-latch counter output labeled UDC alternately increments and decrements when the SAW frequency is in the passband as indicated by the SAW output envelope. The presence in the passband is detected by the peak detecting comparator and finite state machine in the primary sensor loop. The TDC fine conversion occurs at the end of the counter conversion. The converted TDC value and

the counter value are read from a bank of buffers located on the pads. These buffers are driven by a bank of registers which latch the TDC outputs.

In the case illustrated in Fig. 9.4, the UDC increments to a count of 33 during the passband cycle. At this point the UDC outputs are latched and read out. The latched TDC outputs vary between a code of 10 and 15, showing cycle to cycle variation arising from supply switching and uncertainty between the clock edge and the comparator output.

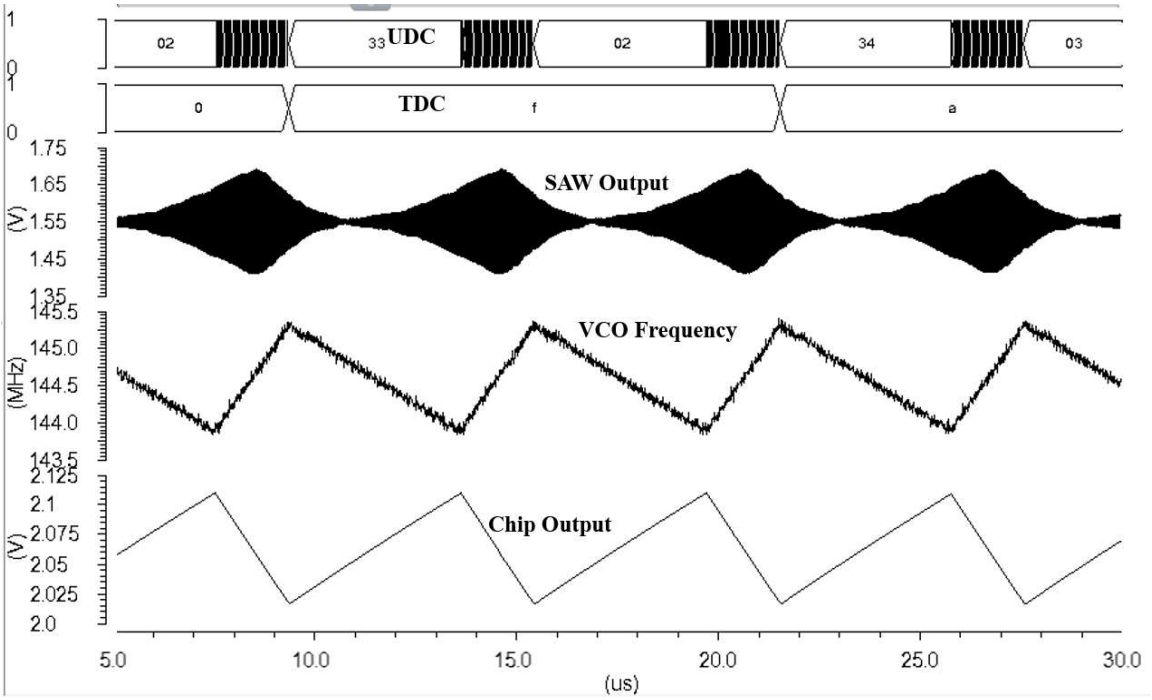

Figure 9.4: Steady State Transient Simulation

9.4 Delay to Digital Conversion test Results

The functionality of the delay to digital conversion is verified by plotting the timing signals and the digital outputs as shown in Fig. 9.5. An initial calibration pulse produces a synchronized load signal (UDCLOADN) which loads a known state into the counter. The converter is now ready. On the other hand the primary sensor loop is

operating in steady state as indicated by comparator output. During conversion the counter counts up or down depending on the state of the UDCMODE signal. The TDC converts the delay between the system clock and the TDCSTOP signal to a 4 bit digital bus. In steady state the latched UDC and TDC buses will provide a constant output in the absence of a sensor event. A mass loading event will cause a change in the steady state sensor analog output voltage and a corresponding change in the 10 bit steady state output.

The performance of the converter under supply noise injection is considered in Fig. 9.6. In this case, noise induced random variation of the comparator edge is converted to variation of the latched TDC outputs. In the case shown the TDC bus output varies by as many as 3 codes from cycle to cycle. The latched six bit counter outputs still retain the same value cycle to cycle.

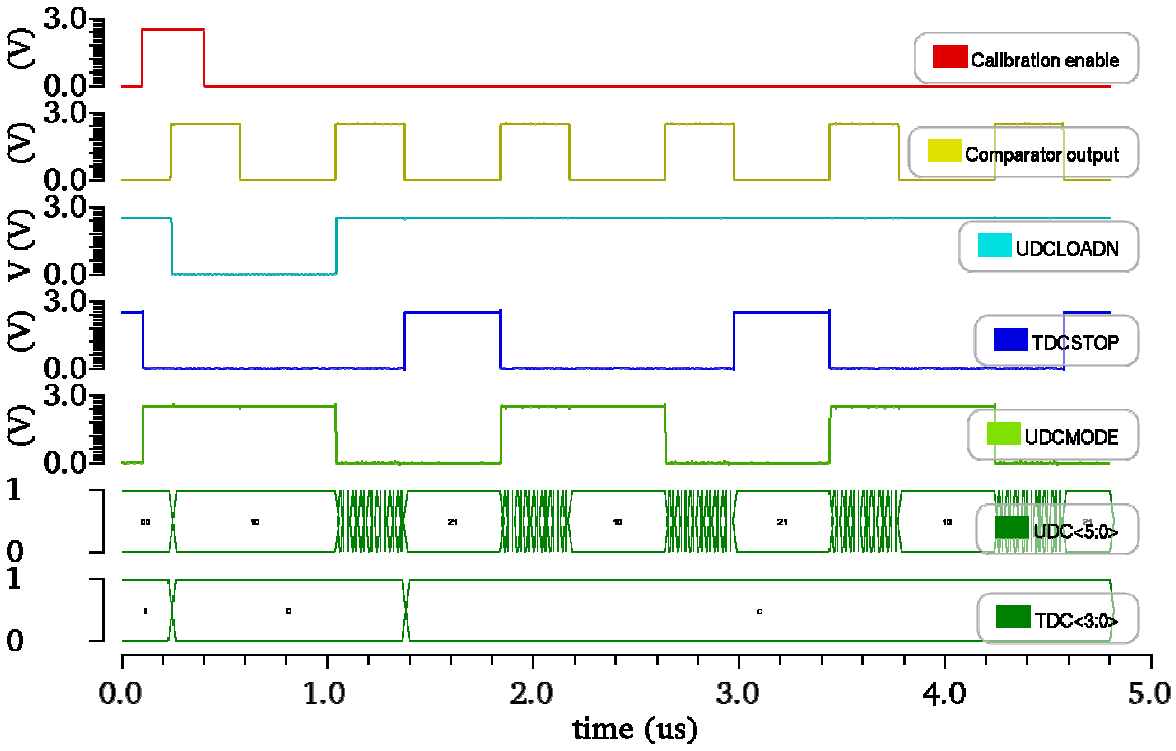

Figure 9.5: Waveforms of FSM based digital readout and control signals.

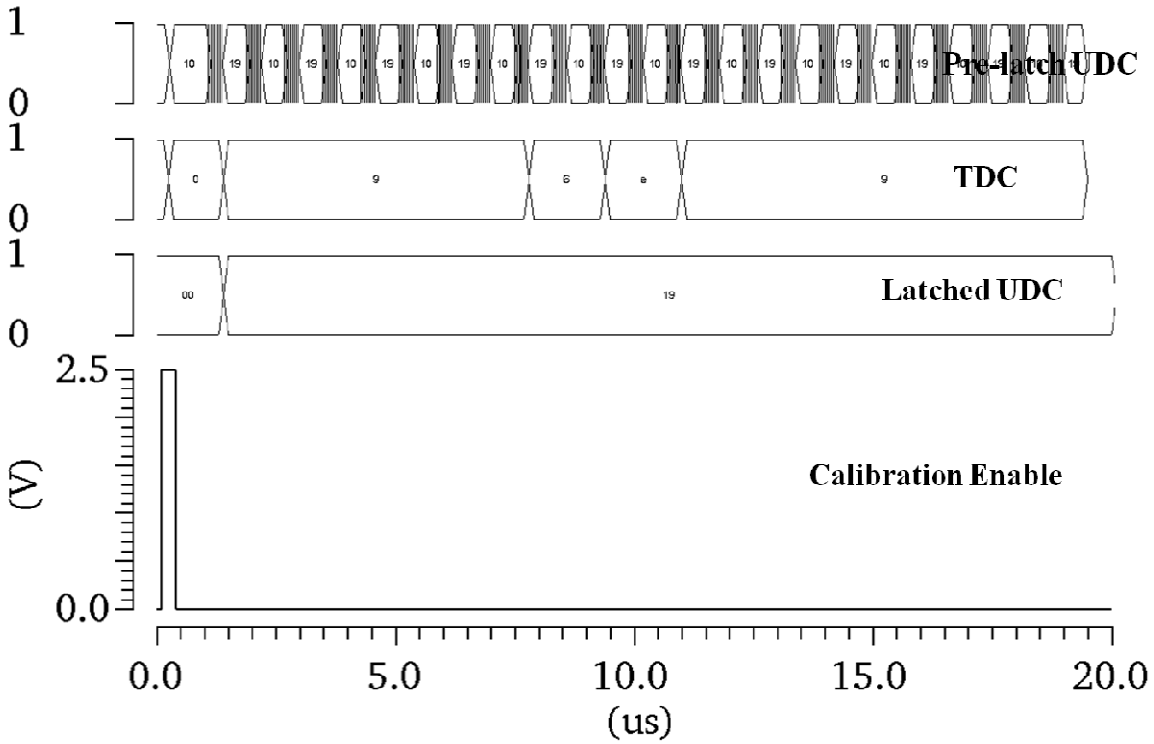

Figure 9.6: Waveforms of FSM based digital readout with supply noise injection

The TDC resolution can be adjusted using the varactor voltage $V_{F.}$ This control along with the coarse control of the primary loop VCO allow adaptation to SAW devices with different center frequencies and groups delays. Plotted in Fig. 9.7 is the least significant bit of the delay to digital conversion in delay units vs. the varactor voltage which is varied up to 2.5V. The maximum to minimum tuning range obtained is 2.8:1.

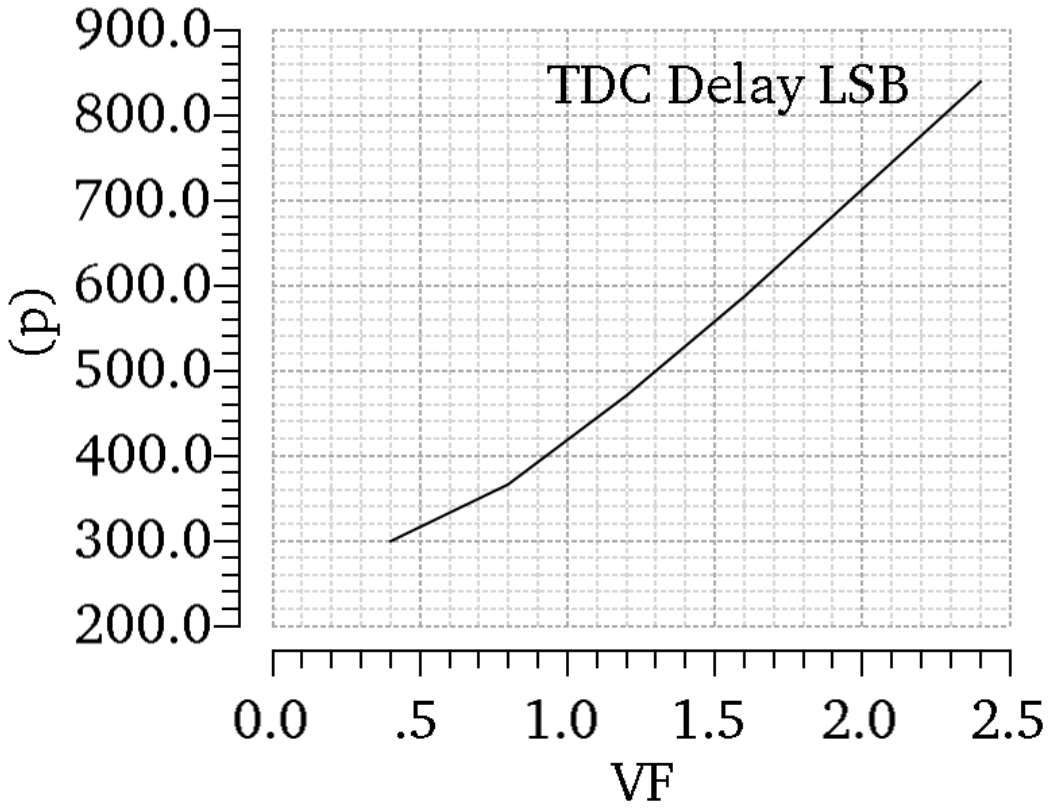

Fig. 9.7: TDC resolution (ps) vs. varactor voltage: 4 bit TDC

The phase resolution achieved can be improved by increasing the TDC bus width and moving to a faster process node. Potentially, the TDC resolution could be of the order of gate delays. However, the bus width would also need to increase to retain the same conversion range. A simulation with 8 bit TDC and TSMC 18nm process models shows increase of LSB resolution of 85ps as seen in Fig. 9.8. The tuning range obtained is 2.6:1 for the same supply range.

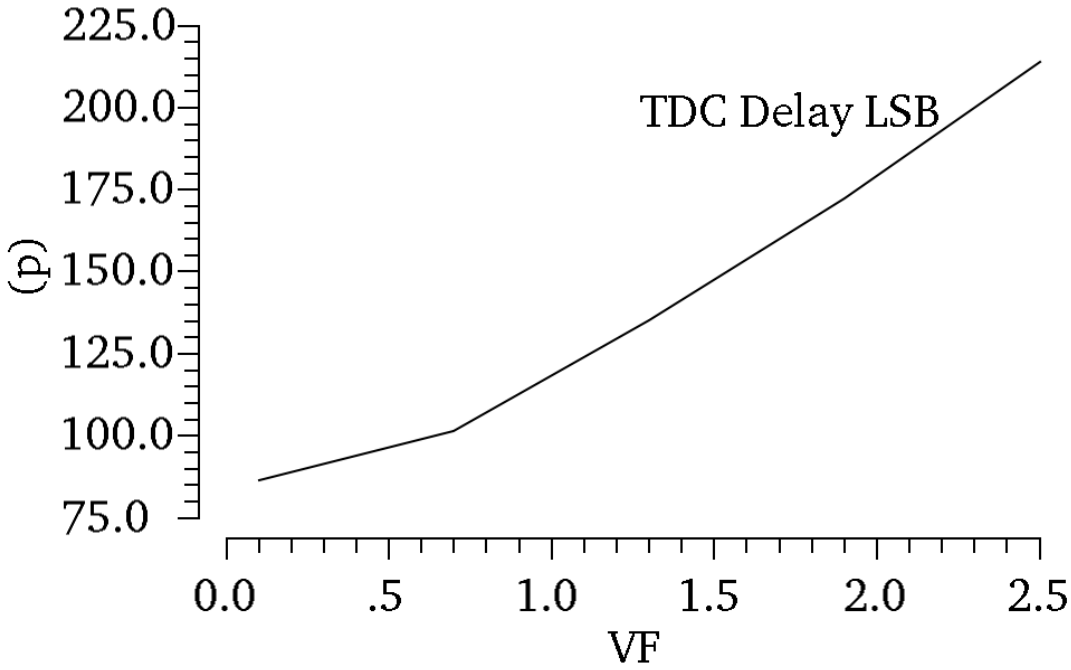

Figure 9.8: TDC resolution (ps) vs. varactor voltage: 8 bit TDC

9.5 Performance Summary

The performance of the proposed readout along with selected reported sensors has been tabulated in Table 2. These sensor topologies were discussed in Chapter 4. The comparison points have been selected based on comparable frequency operation in the range of 100MHz to 400MHz. While fine frequency shift detection of the order of 100Hz is possible using external measurement equipment as employed in [7],[8], integration into a CMOS compatible readout is not feasible with such set ups. The digital readout proposed in [4] can be considered as a benchmark. However, the proposed design employs a different topology with an FSM control inside the SAW loop.

Table 9.1: Performance Summary

	Topology	Readout Method	Integration Feasibility	Measured parameter	Typical shift
This work	FSM controlled loop	10 bit digital	Y	Phase delay	250ps
[6]	Oscillator	24 bit digital	Y	Frequency	10kHz
[8]	Open loop	Network analyzer	N	Frequency	300kHz
[9]	Dual delay line	Frequency counter	N	Frequency	200Hz
[10]	Dual delay line	Frequency counter	N	Frequency	800Hz
[7]	Transponder	Network analyzer	N	Return loss	1dB

9.5 Summary

System test results were carried out at the top level with instantiation of the SAW device. The steady state showed the counter incrementing and decrementing alternately for periods when the comparator output is high. The latched TDC outputs provide a finer resolution of the delay from the system clock edge to the comparator transition. Simultaneously, observation of the time varying SAW output frequency, the sensor output voltage and the envelope of the SAW output voltage confirm functionality according to the designed finite state machine implementation.

Sub-system simulations show the functionality of FSM waveforms. Noise injection into circuit leads to variation of the TDC output bus by up to 3 codes from cycle to cycle. Analysis of the TDC itself shows a resolution of 300ps which can be improved to 85ps using a different process node and increasing the bus width to 8 bits.

Chapter 10: Conclusions and Future Work

10.1 Design Features

We have presented the design and analysis of a novel frequency to voltage readout circuit for integrated SAW sensors. The system operates in closed loop and outputs a low frequency voltage ramp the mean value of which tracks the state of the sensor whether loaded or unloaded. The sensitivity of the voltage output to frequency shifts can be increased by decreasing the VCO fine control gain. The demonstrated sensitivity is sufficient for most physico-chemical applications with the advantage of small footprint and portability which are not present in high resolution single or dual oscillator systems with external frequency counter setups. We further show that the mean output voltage shift is immune to supply noise. As demonstrated by testing with SAW devices with center frequencies at 70MHz, 140MHz and 374MHz and different phase delay times, we only need to adjust the coarse VCO input and the closed loop behavior will ensure a different steady state range of the fine input. This flexibility gives us an option to expand the design to an array of filters with different passband characteristics or mass sensitive coatings for discrimination among multiple analytes.

Expanding the core loop, we have further implemented a dual FSM based readout circuit for integrated SAW sensors. A direct A/D conversion would load the sensor output and affect loop performance. Instead, a novel delay to digital conversion scheme was employed to convert filter charge time to an equivalent digital output. The resolution of the voltage output to frequency shifts can be increased by decreasing the VCO fine control gain as well as the TDC varactor voltage. For

increased digital conversion sensitivity the number of conversion bits which in this prototype has been selected as 10 can be increased. The design demonstrates full digital readout capability for SAW sensor applications under mass loading resulting in frequency shifts in the order of 10 kHz or phase shifts in the order of 100ps.

10.2 Modeling and Analysis

In addition to the implementation of the new readout topology, the dissertation research also yielded interesting methods to theoretically analyze SAW based designs. Analysis carried out both at the block level and the system level yielded representations of node behavior both in steady state and startup modes. On the one hand we used traditional analog models to analyze transients. On the other hand for a system level representation, we adapted discrete time analysis to obtain and solve difference equations representing the nodes in the loop. Such analysis has been used for digital phase locked loops (DPLL) or delay locked loops (DLL). Our adaption of this representation to the SAW sensor loop is not only theoretically interesting but might lead to new modeling capabilities. Behavioral modeling is particularly useful in Verilog or System Verilog based simulations which would be several orders faster than SPICE based analog simulations. These would be applicable not only to sensor design but also to communication systems which use SAW filters.

Also used to facilitate and optimize design was extensive use of simulation of the readout with incorporated SAW models. For such simulation, device and interconnect parasitics were obtained from extractions of the chip layout. In mature process nodes, these parasitics are usually accurate and are able to predict bench test results.

Indeed, bench measurements were found to functionally and parametrically confirm simulation results. Effects of noise interference, were, of course, found to be reduced at lower operating frequency due to a reduction of switching noise on the supply.

10.3 Future Work

The main area of future work would be realization of the SAW device and the readout on the same CMOS chip. Fabrication of SAW devices in CMOS technology has been reported by Tigli et al [6] in AMI 0.5μm technology. Using a three step post processing sequence, the IDT mask was imprinted using reactive ion etch (RIE), ZNO was deposited through magnetron sputtering and the pad frame was defined through shadow mask photolithography. These steps could be applied to wafers with the fabricated readout to generate an integrated sensor. Similar post-processing steps could be applied to faster process nodes to target RF operation frequencies. Operation at these frequencies would lead to increased mass sensitivities. The IDT dimensions and chip areas would also decrease. Monolithic integration remains a very feasible target for this readout topology.

An improvement in noise performance would come from use of fully differential current mode logic (CML) outputs from the VCO. The SAW matching circuits, inputs and inputs could then be configured for differential input and output ports. CML signals will provide increased noise immunity both in the readout and in the SAW response. The stage delay will still be controlled by a voltage dependent capacitor with the control voltage being the fine input to the VCO.

The design of an array of SAW filters for multiple analyte discrimination is a more involved challenge in monolithic integration. The primary difficulty is the realization of these IDTs on the same die because of area constraints. The real time signatures of the readout output buses would then be used to identify the specific gas.

The need for future implementation and data collection remains in the area of obtaining the time varying sensor outputs with ZnO based Love mode SAW devices coated with polymer sensor film.

Appendix

A.1 Alternate readout topology

An alternate topology of the readout design was also designed. In that variation the SAW output frequency is centered in the middle of the passband. The integrator input toggles on the falling edge of the latched comparator output. This causes the integrator output (which is also the fine input to the VCO) to reverse slope and hence push the VCO frequency back into the passband.

The upper limit of the VCO input ramp is given by

$$V_{\max} = V_{mid} + \frac{1}{K}(f_{mid} + \frac{B}{2}) + \frac{V_{dd}}{\tau}(t_d + t_c)$$

where V_{mid} = VCO fine voltage corresponding to midband, B = bandwidth, f_{mid} = midband frequency, K is the VCO sensitivity, τ is the integrator time constant, t_d is the IDT delay and t_c the circuit delay. (A.1)

The range of the ramp is given by

$$V_{band} = \frac{B}{K} + \frac{2V_{dd}}{\tau}(t_d + t_c) \quad \text{(A.2)}$$

The change in the maximum input ramp voltage due to a change in the IDT mid-band frequency is given by

$$\Delta V_{\max} = \frac{\Delta f_{mid}}{K} + \frac{V_{dd}\Delta t_d}{\tau} \quad \text{(A.3)}$$

Simulation results of this topology with TSMC 0.35μm process parameters and a low loss SAW filter operating at 374MHz are shown Figure A.1 The VCO frequency is centered at the mid-band frequency with the limits roughly corresponding to the passband. In this variation the range of the ramp will be higher

than in the main design since the VCO frequency will need to traverse the entire passband before reversing.

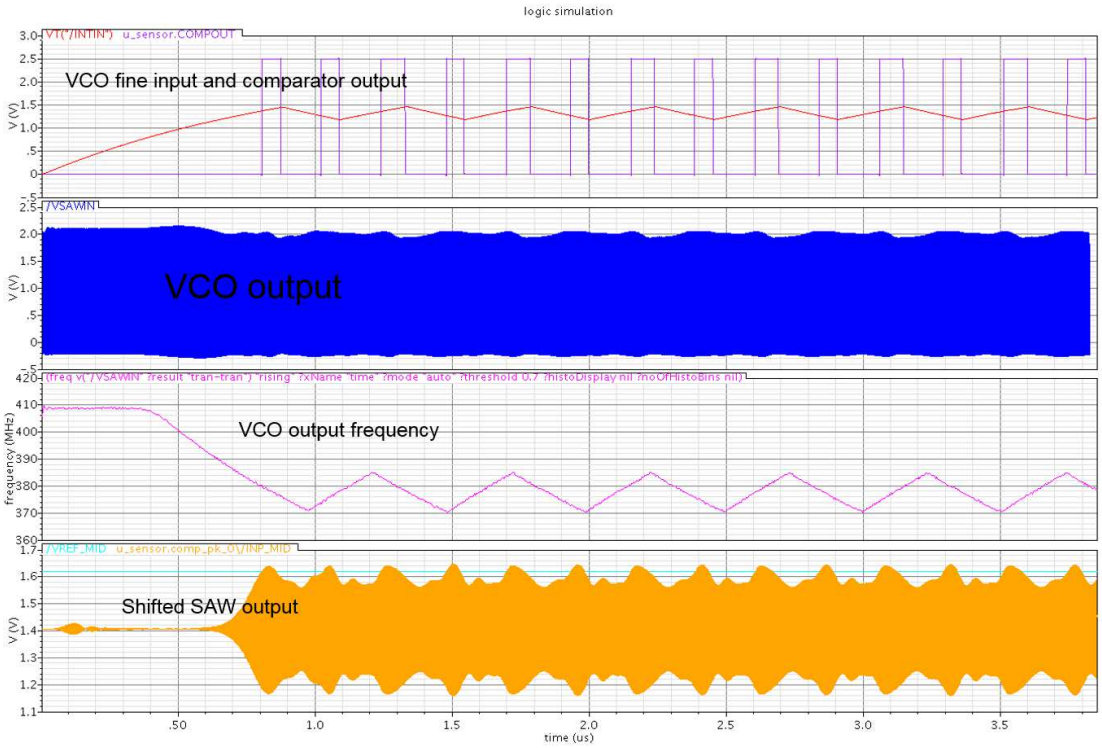

Figure A.1: Simulation results for alternate SAW design

A.2 MATLAB Code

MATLAB Code for SAW model generation:

```
%Program for generating Yport and Sport parameters for a two
transducer
%device. Also calculates and plots transfer function.
clear;

Zref=50;
Zo=50;
%Set IDT parameters
Rs=1.8E03;
Rl=4.5E04;
Rs=50;
Rl=50;
delta=0.05;
N=100;  %100 fingers on input
M=100;  %100 fingers on output
%fo=300*1E06;  %Center frequency
fo=300*1E06;  %Center frequency
%v=3488;       %SAW velocity
v=4800;       %SAW velocity
```

```
%K=0.04;       %Coupling coefficient
K=0.1;       %Coupling coefficient
lammda=v/fo;
lammdao=v/fo;
W=100*lammdao;  %Apodization overlap/aperture
d=60*lammdao;
Co=0.5*1E-10;  %Capacitance per unit length/finger pair
Cs=Co*W;
Go=K*K*fo*Cs;  %Equivalent characteristic admittance
Gao=8*N*N*Go;  %Radiation conductance of input IDT at center
frequency
Gbo=8*M*M*Go;  %Radiation conductance of output IDT at center
frequency


Ct1=N*Cs;       %Total capacitance of 1 section
Ct2=M*Cs;

%f1=250*1E6;
%f2=350*1E6;
f1=0.95*fo;
f2=1.05*fo;
numpoints=1000;

file_1 = fopen('ypara.txt','w');

for n=1:numpoints+1
    f=f1+(n-1)*(f2-f1)/numpoints;
    frequency(n)=f;
    k(n)=2*pi*f/v;
    if (f==fo)
        theta=2*pi*(f+delta);
        X1=1E-14;
        X2=1E-14;
    else
        theta=2*pi*f/fo;
        X1=pi*N*(f-fo)/fo;
        X2=pi*M*(f-fo)/fo;
    end
    array_factor_input=0;
    for m=1:N
        array_factor_input=array_factor_input+exp(-
m*k(n)*lammdao*1i);
    end
    array_factor_output=0;
    for m=1:M
        array_factor_output=array_factor_output+exp(-
m*k(n)*lammdao*1i);
    end
    %Calculate three admittance matrix for input section
    Y(1,1)=-Go*cot(N*theta)*1i;
    Y(1,2)= Go*csc(N*theta)*1i;
    Y(1,3)=-Go*tan(theta/4)*1i;
    Y(3,3)=2*pi*f*Ct1*1i+4*N*Go*tan(theta/4)*1i;
    Y(2,2)=Y(1,1);
    Y(2,1)=Y(1,2);
    Y(3,2)=-Y(1,3);
```

```
    Y(2,3)=-Y(1,3);
    Y(3,1)=Y(1,3);
    Ga(n)=Gao*(abs(sin(X1)/X1)^2);
    Gb(n)=Gbo*(abs(sin(X2)/X2)^2);

    %Calculate two port matrices for entire device
    Y2port(1,1)=Ga(n)+2*pi*f*Ct1*1i;
    Y2port(2,2)=Gb(n)+2*pi*f*Ct2*1i;
    Y2port(1,2)=sqrt(Ga(n)*Gb(n))*exp((pi-X1-X2)*1i)*exp(-
k(n)*d*1i);
    Y12approx(n)=Y2port(1,2);
    %Y2port(1,2)=sqrt(Ga(n)*Gb(n))*exp(1i*(pi*(1-(N+M)*(f-
fo)/fo)))*exp(-k(n)*d*1i);
    Y2port(1,2)=8*Go*array_factor_input*array_factor_output*exp(-
k(n)*d*1i);
    Y2port(2,1)=Y2port(1,2);
    Y2p11(n)=Y2port(1,1);
    Y2p22(n)=Y2port(2,2);
    Y2p12(n)=Y2port(1,2);
    H(n)=Y2port(1,2)*Rl/((1+Y2port(1,1)*Rs)*(1+Y2port(2,2)*Rl)-
Rs*Rl*(Y2port(1,2)^2));
    Z2port=inv(Y2port);
    S2port=(eye(2)-Zref*Y2port)*inv(eye(2)+Zref*Y2port);
    S2p=(inv(Z2port+Zref*eye(2)))*(Z2port-Zref*eye(2));
    S21(n)=S2port(2,1);
    S21_x(n)=S2p(2,1);
    S11(n)=S2port(1,1);
    fprintf(file_1,' %8.6E:  %8.6E, %8.6E %8.6E, %8.6E
\n',frequency(n),real(Y2port(1,1)),imag(Y2port(1,1)),real(Y2port(1,2
)),imag(Y2port(1,2)));
    fprintf(file_1,' %8.6E, %8.6E %8.6E, %8.6E
\n',real(Y2port(2,1)),imag(Y2port(2,1)),real(Y2port(2,2)),imag(Y2por
t(2,2)));
end
fclose(file_1);
figure(1);
plot(frequency, Ga/Gao, 'k-');
figure(2);
plot(frequency, abs(H), 'k-');
figure(3);
plot(frequency, abs(S21), 'k-');
figure(4);
plot(frequency, abs(S11), 'k-');
figure(5);
plot(frequency*1E-6, 20*log10(abs(S21)), 'k-');
xlabel('Frequency(MHz)');
ylabel('|S21|(dB)');
```

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