ABSTRACT

Title of dissertation: LOW FREQUENCY NOISE IN CMOS TRANSISTORS

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The minimum measurable signal strength of an electronic system is limited by noise. With the advent of very large scale integrated (VLSI) systems, low power designs are achieved by reducing the supply voltage and the drive current. This reduces the dynamic range of the system. As the signal in an amplifier system is usually set to be a significant fraction of the dynamic range, all other factors being equal, reduction in dynamic range leads to a degradation of the signal to noise ratio (SNR). This thesis addresses this issue in low power design.

Focus is given to low frequency ($\leq$ 1 kHz) noise. This frequency range is dominated by flicker noise, also referred to as pink or $\frac{1}{f}$ noise. Most biomedical and audio signals lie in this low frequency domain. For example, electrocardiograms (ECGs) record signals which are $<$ 50 Hz. Audio signals have a large portion of signals that lie in the low frequency bandwidth <100 Hz. The focus here is on low-frequency performance of CMOS transistors. This represents a significant challenge in detection as noise in solid state devices tends to increase with decreases in frequency. That is, it becomes "pink," weighted to the low frequency spectral

range. Usually, we find that noise power changes reciprocally with frequency as we reach the kilohertz frequency range.

While there has been no single, definitive theory of of pink noise, system design principles can be formulated to minimize the impact of this noise. There are two factors to consider here. First, the pink noise process appears to be related to interaction with the defect structure of the solid through which charge is transported. As the number of defects is finite, there is a limit to the number of charges that can interact with this defect population. Thus, there is a limit on the amount of fluctuation in this interaction "current." This limit depends on the number of defects present in the solid through which transport occurs. It also depends on the number of charges transported. Thus, the trivial and often cited optimization principle demanding a reduced solid defect density presents itself.

This leads to a second, less obvious principle of optimization. If the number of transported charges is large, and the trap defect parameters (number density, cross-section, trap lifetime, etc.) does not depend on total current passed, it is possible to "overcome" the defect-related noise. This is done by increasing the bias current. For fixed defect density, increased bias current will "saturate" the 1/f-noise fluctuation at some level resulting in an increase in SNR. Large current leads to large power dissipation, an undesirable side-effect of saturating the 1/f-noise current. This problem of SNR and power optimization has been addressed in this work.

The main contribution of the work is development of an analog design methodology utilizing saturation effect to improve system SNR through bias optimization. Flicker noise measurement was carried out for the low frequency region in 0.5μ and

130 nm CMOS process and SNR studied under different gate bias voltages. We further investigated the impact of size variation, radiation stress and low temperature on the optimal bias point of the device. In addition, low temperature noise spectroscopy was conducted to study the noise behavior. Double channel method was used which enabled measurement of pink noise at very low gate biases for 130 nm process. The work investigates signal, noise and power in deep subthreshold region for the first time.

Low Frequency Noise in CMOS transistors

by

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Dissertation submitted to the Faculty of the Graduate School of the
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To my family

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Chapter 1

Introduction to Noise Processes in Semiconductor Device and their Measurement

1.1 An Overview of the Problem

This thesis presents an overview of noise minimization techniques for analog systems. Focus is on minimizing the impact of low frequency noise (referred to as "pink," or 1/f noise) in the kilohertz region of the signal spectrum. While considerable literature exists on modeling component performance in the presence of this noise, the literature on system level design is contradictory or incomplete. This thesis seeks to provide simple design rules based on current biasing to achieve optimum signal to noise (SNR) ratio in an analog signal path.

Random variations imposed on signal power from extraneous physical processes limit our ability to sense physically significant changes in the state of an observed system. The state here referred to may be the frequency-dependent audio power content of a musical recording or the neural firing pattern of a segment of brain tissue. These examples were selected as they represent target systems for the work presented in this thesis. The focus here is on low-frequency performance. This represents a significant challenge in detection as noise in solid state devices tends to increase as frequency decreases. That is, it becomes "pink," weighted to the low

frequency spectral range. Usually, we find that noise power changes reciprocally with frequency as we reach the kilohertz range of frequencies. Neural firing patterns and audio data tend to be in the kilohertz frequency range.

While there has been no single, definitive theory of of pink noise, system design principles can be formulated to minimize the impact of this noise. There are two factors to consider here. First, the pink noise processes appears to be related to interaction with the defect structure of the solid through which charge is transported. As the number of defects is finite, there is a limit to the number of charges that can interact with this defect population. Thus, there is a limit on the amount of fluctuation in this interaction "current." This limit depends on the number of defects present in the solid through which transport occurs. It also depends on the number of charges transported. If a small number of charges are transported, a relatively small number of defects can make a large percentage difference in the number of charges measured as output in some integration period. Thus, the trivial and often cited optimization principle demanding a reduced solid defect density presents itself.

This observation leads to a second, less obvious principle of optimization. If the number of transported charges is large, and the trap defect parameters (number density, cross-section, trap lifetime, etc.) does not depend on total current passed, it is possible to "overcome" the defect-related noise. This is done by increasing the bias current. The output signal is usually set to be some significant fraction of the bias current, increased bias current usually translates to higher signal currents. For a moment, let us just consider the noise due to the interaction of the total current stream with the defect population. As, shown below, for fixed defect density,

increased bias current will "saturate" the 1/f-noise fluctuation at some level. *The overall result is an increase in SNR.*

Of course, large current leads to large power dissipation, an undesirable side-effect of saturating the 1/f-noise current. So our design goal must be to increase the bias current in such a way as to improve SNR without exceeding critical limits in power dissipation. If our only concerns were with trap interaction and power dissipation, one could raise the background current (and thus the signal) until some critical dissipation limit is reached. This would be a rather simple optimization problem.

Unfortunately, other noise-generating mechanisms may appear as the bias current is increased. For example, to increase channel current in a metal-oxide-semicounductor field effect transistor (MOSFET), we increase the gate bias voltage. This draws channel charge closer to the interface in which most of the channel scattering centers reside. Scattering becomes stronger, mobility declines and it is possible that mobility fluctuations may add further noise to the current stream. Also, The position of the semiconductor Fermi level at the semiconductor-oxide interface determines the density of traps with which the mobile channel charge can interact. The Fermi level moves toward the band edge as the bias increases. The region near the band edge is rich in interface charge, effectively increasing the trap density as we move the transistor into saturation. Furthermore, local channel heating due to increased channel current may increase other familiar noise processes, like Johnson noise.

These factors must all be accounted for in order to achieve a true optimization

of system SNR.The question remains, is it possible to move into a region of operation in which the noise current is saturated well below the signal current, taking into account all these noise generation mechanisms and satisfying the pre-determined limits in power dissipation? This is the question to be answered by this thesis.

In addition, one persistent problem inhibiting our ability to understand the physics of low frequency noise processes is the noise floor of the measurement tool. This thesis describes a new two-channel noise measurement process that reduces noise floor by autocorrelation techniques exercised between the two channels.

1.2 Statement of the Thesis Problem and Summary of the Thesis Contributions

From the discussion given above, we see that flicker noise is highly problematic for many important classes of analog systems. The fact that the physical process or processes giving rise to this noise result from a finite number of solid defects leads to a potential mitigation of this problem through system level design. In particular, adjusting the "background current" (e.g., the system bias current) apparently serves as a convenient way to minimize the 1/f-noise impact. The work presented in this thesis will address this issue by answering the following questions:

1. Is it possible to create a meaningful improvement in SNR through optimum bias?

2. Is it possible to affect this improvement while staying within pre-determined system power bounds?

3. Will the increase in bias current necessary to "overcome" the 1/f-noise component create additional noise processes that invalidate the proposed design technique?

The thesis problem is to provide answers to these questions. In addition, during the course of this thesis work, it became obvious that more sensitive noise detection techniques would be required to experimentally determine the bias optimum points. A subsidiary problem addressed in this thesis is the application of a sensitive "two channel" noise detection technique making use of autocorrelation of current in two channel branches. This technique, its application, and the degree to which it reduces the measurement noise floor are presented here.

The main contributions of this work are:

1. Development of a "Trap occupancy saturation model"' explaining the observed behavior of 1/f noise CMOS channel as a function of channel current. We study the change in noise behavior for CMOS transistor operating in conditions leading to device degradation and explain it using the trap occupancy model.

2. Development of an analog design methodology utilizing this saturation effect to improve system SNR through bias optimization. The optimization described traces noise behavior in the MOS channel from deep sub-threshold to strong saturation in a 0.5 μ CMOS process and a 130 nm CMOS process.

3. Low temperature noise spectroscopy is carried out to comprehensively study the noise behavior at low temperatures in a 0.5 μ CMOS process and a 130 nm CMOS process.

1.3 Overview of the Thesis to Follow

In the next chapter, we provide a background on low-frequency noise modeling, citing all major theories of noise generation and describing how these theories translate into noise models for computer aided design (CAD.) This includes fluctuation phenomena specific to low frequency transport (1/f-noise models) as well as the "white noise" effects associated with thermal (Johnson) noise and shot noise. We further summarize the impact of bias dependent mobility on transport and on transport fluctuations.

The basic theory and methods are described in chapter three. We provide detailed theory of the trap saturation model for flicker noise and background of measurement methods. This chapter also contains a full description of the two channel autocorrelation method of reducing noise floor in low frequency noise measurements. This is followed in chapter four by background of the experiments, test devices and test setup. Chapter five gives the results from the experiments. Chapter six shows how these optimization techniques are useful in improving system-level performance. In chapter seven we extend the discussion and analysis of optimal biasing to an integrated amplifier. Finally, we conclude our work by summarizing the main contributions and describing future applications and improvements on the work described in chapter seven.

Chapter 2

Noise in Electronic Systems: Some Background Material

Noise sources can be classified in a number of different ways. White noise processes have constant spectral power content over the band of frequencies operated on by an analog system. Stationary processes have spectral power constant over time. In this thesis, the focus is on stationary processes exhibiting enhanced low-frequency noise content. In particular, we are concerned with noise processes giving spectral power density varying inversely with frequency - the so-called "1/f noise" signature. As described in the introduction, there is no generally accepted "unified" theory of 1/f noise. In this section, the major approaches to modeling this type of noise are summarized.

In order to fully characterize the noise content of a system, though, we must first consider the "white noise" processes. We do this in order to place the 1/f-noise components in perspective and to understand their relative impact on overall performance. We also describe the formalism currently in use to perform both "back-of-the-envelope" and more sophisticated CAD calculations of noise power in MOSFETs.

This is followed by a summary of the three major approaches to 1/f modeling generally referred to as the McWhorter, Hooge and Claeys models. We describe how these models are implemented in standard CAD system approaches such as

the Berkeley BSIM model. There has been a considerable amount of study on how 'scaling" (dimension reduction) impacts 1/f processes and these effects are summarized below. In the following chapter, we enter into a discussion of how trap density, trap occupation levels affect 1/f noise power densities with respect to the "white noise" processes.

2.1 White Noise in MOSFETs: Origins and Impact

There are two dominant white noise processes in semiconductor devices. These are thermal noise (frequently referred to as Johnson or resistive noise) and shot noise. Other "telegraph" or "pop-corn" noise is also mentioned in the literature, although it's impact is limited. Each of these processes has a different physical origin. We discuss these processes, in turn, below.

2.1.1 Thermal Noise

Energy is stored in a number of different forms in a solid. Kinetic energy in the form of mobile carrier motion and vibrational energy in the atomic lattice (quantized as phonons) are the dominant stores of energy. As these are related to the temperature of the lattice, these are known as the thermal energy stores. Thermal noise is due to random thermal motion of charge carriers and phonons. Local pocket of energy form, dissipate and become deficits (with energy below the mean) as a result of this random motion. These energy fluctuations exist even when there is no current flow and it does not depend on the magnitude of the current (as

long as the current does not add significant energy to the transport medium.)

Consider the local energy density fluctuation resulting from random associations of mobile charge carriers. This manifests itself as charge density fluctuation, variation in electrostatic potential and fluctuation in the number of carriers transported in a unit time. Voltage fluctuation in voltage-induced bulk transport is expressed in the well known Johnson-Nyquist formula (equation 2.1) in a simple resistor. If we consider the channel transconductance of a device as, G_0, this formula becomes equation 2.2. Thermal noise is the dominant noise at frequencies much higher than 1kHz [26].

$$v_{th}^2 = 4\kappa T R \Delta f \tag{2.1}$$

where, κ is the Boltzmann constant (units are V^2/Hz) and Δf is the bandwidth of the measurement. The "electrical engineering" format in which fluctuation is symbolized with a lowercase variable is employed here.

$$v_{th}^2 = 4\kappa T \frac{1}{G_0} \Delta f \tag{2.2}$$

where, G_0 is the channel conductance of the device.

In the next section, a heuristic derivation of this formula is provided. It is by no means a rigorous proof of the Johnson-Nyquist result. But it does neatly demonstrate the relative roles of thermal fluctuation and bandwidth on noise generation. In addition, it highlights the effect of source resistance and negative frequency (phase) components in the overall noise generation process.

2.1.1.1 A Heuristic Derivation of the Johnson-Nyquist Relationship

Consider a conducting bar and unidirectional mobile carrier transport in this bar. From the equipartition of energy theorem, the thermal voltage fluctuation at a temperature T is given by [72]:

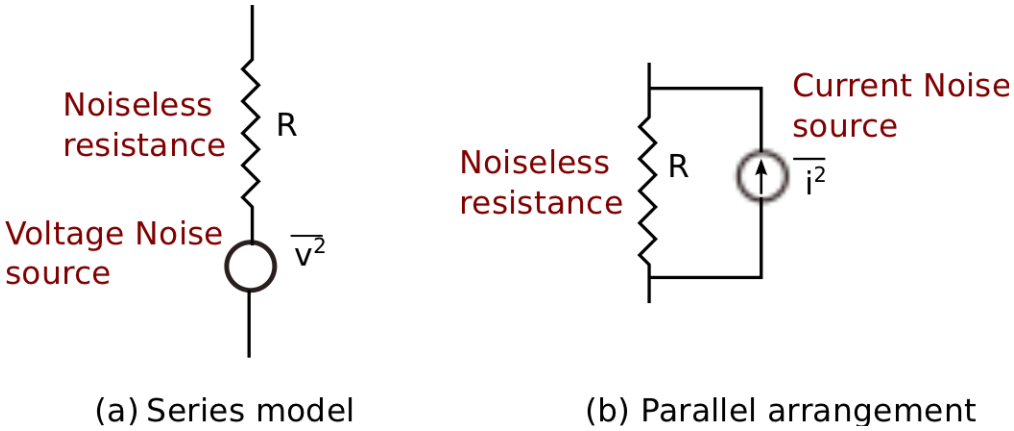
$$\Delta V = \frac{\kappa T}{q} \tag{2.3}$$

On first pass, it appears that the current fluctuation can be obtained from this expression by dividing by the resistance, R. However, as Nahin discusses, to get the worst-case noise power transform, estimate, we must account for the source resistance [57]. The source resistance should equal the load resistance in order to achieve maximum noise power transfer. This source resistance appears in series with the load. Thus, the current fluctuation associated with thermal voltage of the resistance of the bar is 2R, rather than R alone. This yields:

$$\Delta I = \frac{\kappa T}{2qR} \tag{2.4}$$

As the band of admissible frequencies broadens, more noise is admitted to the system. Certainly, the admitted noise must increase with bandwidth. We can use a dimensionally consistent argument to estimate this fractional increase in the noise current accompanying a broadening of the admission band. We simply multiply the result in equation 2.4 by 2qΔf. This yields [1]:

[1]Symbol <> denotes average



(a) Series model (b) Parallel arrangement

Figure 2.1: Series (a) and parallel (b) model of for Thermal Noise. Noise source is represented by voltage or current sources or 'generator'. Resistance 'R' is noiseless.

$$< \Delta I >^2 = q\frac{\kappa T}{2qR}2\Delta f = \frac{\kappa T}{R}\Delta f \tag{2.5}$$

or:

$$< \Delta I >= \sqrt{\frac{\kappa T}{R}\Delta f} \tag{2.6}$$

$< \Delta I >^2$ is the variation in noise current. [2]

We can get the voltage fluctuation by multiplying both sides by 2R:

$$< \Delta V >= 2R < \Delta I > = 2R * \sqrt{\frac{kT}{R}\Delta f} = \sqrt{4kTR\Delta f} \tag{2.7}$$

The "physics format" in which mean fluctuation is expressed as a "delta value" enclosed in wedge brackets, <>, is used here. This is equivalent thus to the expression shown in equation 2.7, with a shift in formats.

It should also be noted (and will be important for a later discussion) that the Johnson noise formula can be re-written for a system containing capacitive

[2]This can be obtained by assuming a Poisson's distribution.

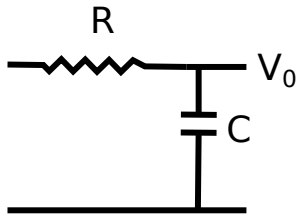


Figure 2.2: Schematic of RC filter for shaping thermal noise.

reactances. The capacitances do not, by themselves, "generate" noise. But they do limit the noise bandwidth and, thus, affect the final form of equation 2.7. First, we find the "effective" noise bandwidth by integrating over all frequencies, as weighted by the RC low-pass filter (figure 2.2) transfer function set up by the combination of the network resistance and capacitance [65, 4]:

$$\Delta f = \frac{1}{2\pi}\int_0^\infty \frac{d\omega}{1+(\omega RC)^2} = \frac{1}{2\pi}\frac{\pi}{2RC} = \frac{1}{4RC} \tag{2.8}$$

Substituting this result into 2.7 Yields:

$$< \Delta V >= \sqrt{\frac{kT}{C}} \tag{2.9}$$

an expression that has no dependence on the resistance [65]!

2.1.2 Shot Noise

Shot noise is a second stationary white-noise process observed in a variety of transport processes. Its origin is quite distinct from thermal noise. The lack of temperature dependence is an obvious reason for this assertion! Shot noise is independent of both temperature and frequency.The spectral density of shot noise

is given by equation 2.10 in units A^2/Hz [4].

$$i_d^2 = 2qI_d\Delta f \tag{2.10}$$

where, I_d is the direct current.

2.1.2.1 Shot Noise Derivation

Let us consider an average value of current I_m flowing through a conductor. The number of charges passed in some unit time interval is $I_m \times 1$ [74]. This number fluctuates as a result of the fact that particles entering some transport volume exhibit an ensemble (a distribution) of path lengths from their point of admission to their point of exit from the volume. Assuming a Poisson process, the variance in the number transported is proportional to the square root of the mean number. But, once again, the bandwidth plays a role in defining the noise admitted to the system. Using the same heuristic principle described above for thermal noise, we can multiply the Poisson variance by the bandwidth noise to give:

$$< \Delta I_d >^2 = 2qI_m\Delta f \tag{2.11}$$

This is the expression shown in equation 2.10. Again, both the physics and engineering formats are used interchangeably. A complete and more rigorous method of derivation is by taking a Fourier transform of electron current pulse [78].

It is interesting to compare thermal and shot noise processes. Thermal noise is the result of "clumping together" of energetic (or less energetic) particles in space

as a result of the random thermal motion of mobile carriers. This results in local thermal potential differences and these, in turn create current fluctuations. The shot noise component of the total noise results from the fact that the path length through a given section of wire varies from particle to particle. This is because the point of entry and angle of entry of each particle moving through the solid may be different. Also, if there are scattering centers in the solid, these will also cause an ensemble of path lengths. More will be said on this later when we discuss "pink" noise.

2.2 Pink Noise Processes

Noise processes exhibiting spectral power densities weighted to low frequencies are ubiquitous in nature. They are seen in tidal patterns off the shores of Bermuda to light emission fluctuations emanating from quasars. Our concern here is with fluctuations in current flow occurring in solid state charge. Here we find that there are two basic models for generating a "pile-up" of low frequency noise in solid state current flow.

The first is the "number density" class of fluctuation models initiated by McWhorter in his Ph.D. thesis of 1955 [50]. Here, the process is assumed to be driven by surface trapping and subsequent carrier release [41, 52, 14]. Subsequent studies by Hooge attempted to refute the number density model and replace it with an empirical mobility fluctuation model [32, 31, 33, 34]. Hooge's work attempted to show that the 1/f noise power was proportional to the bulk mobile carrier density

and thus was not tied to the surface. He further proposed a number of mechanisms that related noise spectra to Brownian motion in three dimensions. More recently, 1/f noise models were developed by Claeys and his group to cope with scaling in semiconductor MOSFETs [71, 17]. These Models are discussed in the next three sections below. The chapter ends with a discussion of the relative importance of the various noise processes on MOSFET transport.

2.2.1 The McWhorter Model

In this section, the McWhorter model is presented using the approach closely following the presentation given by Milotti, available on ArchiX [54]. The basic approach dates back to early papers by Johnson and by Schottky [39, 68]. First, a time dependent relaxation relationship is postulated based on single-particle interaction with a trapping center. This leads to an exponential relaxation relationship given as:

$$N(t) = N_0 \exp(-\lambda t) \tag{2.12}$$

N(t) is the number of particles in trapping center, λ is time constant. The frequency content of this relaxation is obtained by taking the Fourier transform of this expression:

$$F(\omega) = \int_{-\infty}^{\infty} N(t) \exp(-i\omega t) dt = N_0 \int_0^{\infty} \exp(-(\lambda + i\omega)t) dt = \frac{N_0}{(\lambda + i\omega)} \tag{2.13}$$

Next we assume that there is a train of such trapping/de-trapping pulses at

random times t_k. The frequency content of such a train is given by:

$$F(\omega) = \int_{-\infty}^{\infty} \sum_k N(t, t_k) \exp(-i\omega t) dt = N_0 \sum_k \exp(i\omega t_k) \int_{-\infty}^{\infty} \exp((\lambda + i\omega)t) dt$$
$$= \frac{N_0}{(\lambda + i\omega)} \sum_k \exp(i\omega) \tag{2.14}$$

The power spectrum of this pulse train is:

$$S(\omega) = \lim_{T\to\infty} (\frac{1}{T}) < |F(\omega)|^2 >= \frac{N_0^2}{\lambda^2 + \omega^2} \lim_{T\to\infty} (\frac{1}{T}) < |\sum_k \exp(i\omega t_k)|^2 > \tag{2.15}$$

The last term in this expression (the magnitude of a sum over exponentials squared) only takes on value when t_k is zero, as the random dispositions of the other pulse times sums to zero. Thus, the sum becomes a repeated sum of unity totaling n, the number of pulses per unit time interval. The expression finally becomes:

$$S(\omega) = \frac{nN_0^2}{\lambda^2 + \omega^2} \tag{2.16}$$

McWhorter noted the similarity between this expression and the distribution of particle velocities in a random walk model. Milotti developed these ideas further, deriving power spectrum relationships for Brownian motion and concluded that there were significant differences between McWhorter's model and Brownian behavior [54]. Other workers in the field further noted that equation 2.16 does not quite model the experimentally observed 1/f spectrum. It is relatively flat at very low frequencies and declines as the reciprocal of the frequency squared at higher

frequencies. To fully achieve the goal of modeling experimental behavior, we must assume a *distribution* of relaxation times, λ. The simplest approach is to take a uniform distribution between λ_1 and λ_2 and sum over the contributions from each time constant. In that case, we have:

$$S(\omega) = \frac{1}{\lambda_2 - \lambda_1} \int_{\lambda_1}^{\lambda_2} \frac{nN_0^2}{\lambda^2 + \omega^2} d\lambda \tag{2.17}$$

or:

$$S(\omega) = \frac{nN_0^2}{\omega(\lambda_2 - \lambda_1)} \left[\arctan\left(\frac{\lambda_2}{\omega}\right) - \arctan\left(\frac{\lambda_1}{\omega}\right) \right] \tag{2.18}$$

This power spectrum formula achieves three limiting cases:

$$N_0^2 n \qquad 0 < \omega << \lambda_1 << \lambda_2 \tag{2.19}$$

$$\frac{N_0^2 n \pi}{2\omega(\lambda_2 - \lambda_1)} \qquad \lambda_1 << \omega << \lambda_2 \tag{2.20}$$

$$\frac{N_0^2 n}{\omega^2} \qquad \lambda_1 << \lambda_2 << \omega \tag{2.21}$$

And so, at low frequency the spectral density is rather flat, converting to a true 1/f variation between $\lambda 1$ and $\lambda 2$ and dropping as the square of frequency at higher frequencies.

Both in his thesis and in other published work, McWhorter addressed the issue of non-linearities in the surface trap occupancy process. He felt that an occupied trapping site would repel charge from adjacent sites, leading to a net reduction in the effective trap density. Berz and Rimbaud have analyzed the model taking Debye

shielding of trapped charge into account and conclude that the these non-linearities are not significant in surface trapping [7, 6].

2.2.2 The Hooge Model

Hooge proposed that flicker noise is a bulk phenomenon and not a surface phenomenon. His model theoretically and experimentally supports the idea that the fluctuation in conductivity is due to the fluctuations in mobility and not due to the occupancy of surface traps. He postulated that bulk phonon scattering is the dominant source of 1/f noise. He also cited the possible roles for bulk Coulombic trap scattering and for surface roughness scattering [32, 31].

Hooge proposed his initial model for resistors. His work is not theoretical. But rather, it is based on empirical observations. His noise density formula:

$$\frac{S_R(\omega)}{R^2} = -\frac{2\pi\alpha}{N\omega}\Delta f \tag{2.22}$$

was similarly empirically derived. Here, R is the resistance through which the transport occurs, and N is the total number density of mobile carriers present in the resistor and α is a constant (the Hooge constant.) As justification for this model, Hooge cites the fact that the 1/f noise density correlates (inversely) with bulk density and noise goes up with damage introduced by bulk implantation.

2.2.3 The Impact of Scaling on the 1/f-Noise Power in a MOSFET: Claeys Approach

As technology advances, computing becomes faster, microprocessors shrink and chips become denser. Power dissipation becomes a critical factor and supply rail voltages must be reduced to prevent thermal failure. The impact of scaling on noise has been studied extensively. The relevant work in this area is summarized here.

As geometries are scaled to smaller dimensions, the gate oxide thickness reduces as well. This has a positive effect on noise in that it becomes more difficult for the bulk oxide to retain charge without tunneling out. However, direct leakage through the transistor gate oxide may be an added source of noise. In order to improve yield and reliability, composite gate insulators (such as oxide/nitride) or high-k dielectrics are used. These tend to exhibit large densities of interface states and an increase in the slow state density as well. This increases noise and 1/f noise in particular. Another problem with device scaling is an increase in current density. Decreasing the area of transistors causes an increase in current density in the device channel. This leads to higher power dissipation, higher temperature and more thermal noise.

Finally, the basic models (McWhorter and Hooge) presented thus far don't account for capacitive terms such as oxide capacitance, depletion layer capacitance, interface state capacitance and inversion layer capacitance (C_{ox}, C_{dl}, C_{it} and C_{n}.) This might be thought of as a simple addition of the kTC noise terms (devices above)

to the channel transport model. This is not the case, as kTC noise is just a another way of expressing thermal noise in an RC-network. Simply adding capacitive noise term would "double count" the noise.

The "physics" behind the presence of the capacitance terms in the noise expression (to appear shortly) derives from the paper by Yau and Sah. They explored the way in which a fluctuation in trap charge (δq_t) affects the mobile channel charge. They cited to reasons why δq_t wouldn't simply equal δQ_n, the change in mobile channel charge. First, they point out that the change in trap occupancy may occur through the whole of the depletion volume and some weighting factor accounting for position would have to be included. As it turns out, the bulk of the trapping is weighted to a position quite close to the oxide/semiconductor interface, and the weighting factor tends to be close to unity. However, there is a charge division among the various capacitances cited above. This leads to a capacitor divider ratio pre-multiplier relating δq_t to δQ_n:

$$\delta Q_n = \frac{C_n}{C_n + C_{ox} + C_{dl}} \delta q_t \tag{2.23}$$

The net impact on 1/f power spectrum is expressed (according to Reimbold) as:

$$\Delta S_{I_d} = \frac{q^4 \lambda}{LWkT} I_d^2 \frac{N_t}{(C_{ox} + C_d + C_{it} - \beta Q_n)^2} \frac{1}{f} \tag{2.24}$$

Here, W is the channel width, L is the channel length an λ is given by the expression:

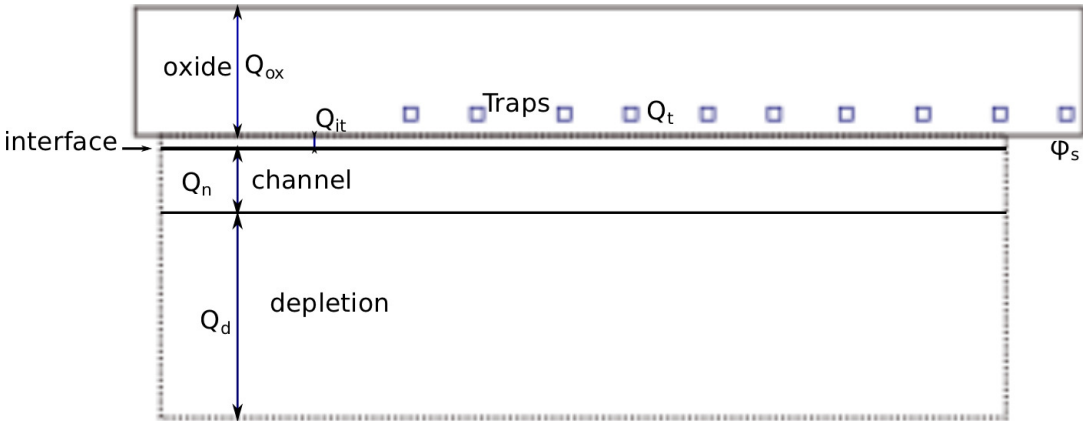


Figure 2.3: This figure explain Reimbold's explanation. Voltage fluctuations in trapped charges are balanced out by the surface voltage fluctuations. $C_{ox}\phi_s$+Q_{it}+Q_n+Q_D+Q_t=0. (Ref: equations 2.23 and 2.24)

$$\lambda = \frac{\hbar}{\sqrt{8m^*\phi}} \tag{2.25}$$

where $\hbar$ is the reduced Planck constant, m^* is the effective carrier mass and ϕ is the tunnel barrier. This term acknowledges the quantum mechanical nature of the tunneling from the inversion channel into the fast or slow interface trap.

2.3 Comparison of the Relative Importance of the Various Noise Process in Semiconductor Design

The paragraphs below, concluding this chapter, are aimed at describing how we may take specific transistor design parameters into account in defining noise performance. These paragraphs also elucidate how geometric effects (such as scaling length and width and oxide thickness, affect noise. Thermal noise in a MOS tran-

sistor depends on the conductance $1/g_m$ of the channel and a factor represented by γ. γ is equal to $\frac{2}{3}$ [26]. This noise is represented by a noise current generator, $\overline{i_d^2}$.The transconductance g_m is constant throughout the complete frequency spectrum giving a uniform distribution for the thermal noise.

$$\overline{i^2} = 4kT(\frac{2}{3}\gamma)\Delta f \overline{i^2} = 4kT(\frac{2}{3}g_m)\Delta f \tag{2.26}$$

$$\tag{2.27}$$

Flicker noise in the MOS transistor is represented by a drain-source current generator. The flicker noise is given by:

$$\overline{i^2} = k_1 \frac{I^a}{f^b}\Delta f \tag{2.28}$$

At low frequencies the relative magnitude of the flicker noise is much higher than at increased frequencies. Experiments show that flicker noise is the dominant noise process at low frequencies and thermal noise is dominant at higher frequencies. Shot noise has a magnitude much lower than the flicker noise at low frequencies but a comparable magnitude at higher frequencies.

2.4 Modeling Approaches

Flicker noise in circuits and devices have been modeled using present accepted understanding of 1/f phenomenon. It is important to model flicker noise as it is a ubiquitous phenomenon and affects the circuits and devices. Below two main

models: (1) the small signal model, used in circuit analysis and (2) BSIM model, widely used in simulators, are discussed.

2.4.1 Small Signal Models

Intrinsic noise due to semiconductor processes, as described above, are important parameters of a solid state device and need to be completely represented in a model for accurate device simulation and analysis. All these intrinsic low frequency noise sources dominant in MOSFET transistor are modeled in the transistor small signal model. Equation 2.29 shows the small signal noise for flicker and thermal noise in a CMOS transistor with transconductance g_m. I_D is the drain current and K is a constant for the device and is a function of fabrication process. 'a' determine the slope of the curve and usually lies between 0.5 and 2. This is also dependent on the fabrication process [26]. The first term denotes the thermal noise (as in equation 2.26) and the second term, the flicker noise. For large frequencies, the second term would diminish and thermal noise will dominate.

$$\overline{i_d^2} = 4kT(\frac{2}{3}g_m)\Delta f + K\frac{I_D^a}{f}\Delta f \tag{2.29}$$

The small signal equivalent circuit with all the intrinsic noise sources is shown in figure 2.4. Thermal noise appears due to resistive nature of the channel. It is shown as a component of current noise source $\overline{i_d^2}$ (equation 2.29). Flicker noise component is also represented by drain-source current noise $\overline{i_d^2}$ (equation 2.29). Another noise source is the shot noise due to gate leakage. It is represented by $\overline{i_g^2}$. This

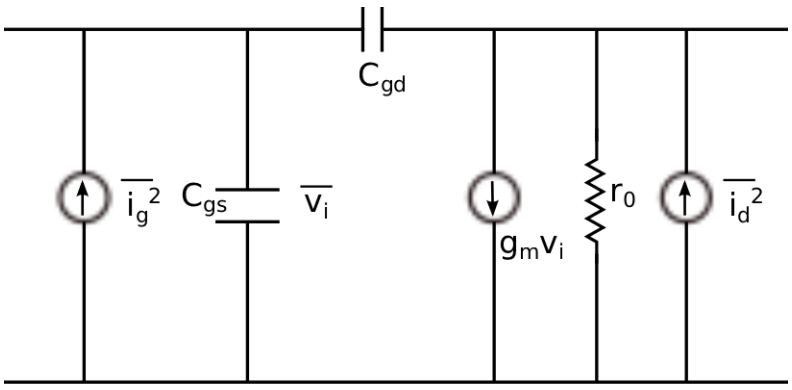


Figure 2.4: Schematic representation of various noise sources in a MOSFET. $\bar{i}_d^2$ denotes flicker and thermal noise (equation 2.29). $\bar{i}_g^2$ represents shot noise.

component of shot noise is very small and is independent of $\overline{i_d^2}$.

2.4.2 The BSIM Model

BSIM (Berkeley Short-channel IGFET Model) model developed for integrated circuit design are widely used by circuit simulators in industry [36, 45]. The complete model reflects various secondary and third order effects along with the primary model. The simplified model is given in the equation 2.30 for saturation region and in equation 2.31 for subthreshold region. Equation 2.31 takes into effect the second order parameters as well. The total flicker noise in the model is given by the inverse of the sums of reciprocals of subthreshold and saturation flicker noise [36].

$$S_{id_{sat}}(f) = \frac{K_{sat} F I_{ds}^{AF}}{C_{oxe} L_{eff}^2 f^{EF}} \tag{2.30}$$

$$S_{id_{sub}}(f) = \frac{K_{sub} k_B T I_{ds}^2}{W_{eff} L_{eff} f^{EF} N^{*2}.10^{10}} \tag{2.31}$$

K is noise parameter, AF flicker noise exponent, EF is the flicker noise frequency exponent (equivalent to a in general model) in the equation.

Chapter 3

Theory and Experiment: Saturation Models and Precision 1/f-Noise Measurement

This chapter presents the motivation behind this work. We first discuss 'First Order Saturation Model' to develop the theory behind study of finding an optimal bias point. In second part we present the measurement system using which very low current noise can be measured for investigating the noise phenomenon in very weak inversion region.

3.1 A First Order Saturation Model

As detailed earlier, this thesis concentrates on two issues in the study of low frequency noise in semiconductors. These are the impact of trap "saturation" (leading to a plateauing of low frequency noise as a function of mobile charge concentration) and the noise floor of the measurement equipment used to characterize noise. In this chapter, the basis of the saturation model is set forth. In addition, we provide a framework for precision noise measurements using the two-channel measurement too.

No matter which model of 1/f noise we choose (McWhorter or Hooge's) the density of scatterers and the density of mobile carriers determine noise generation at low frequencies. In the McWhorter model, the scattering is an interface

phenomenon. The scatterers are either the "fast" interface states located at the oxide-semiconductor interface; or, they are the "slow" states some distance into the oxide (within some "tunneling" distance of the interface.) In the Hooge model, the scatterers are either bulk traps or phonons and the mobile density is the total bulk density of mobile charge. In any event, we can derive a "first order kinetic model" of the scattering process. This is done below.

Our discussion by working with noise in the McWhorter context. As shown, Hooge's model is incorporated as a minor extension of this discussion. Consider a channel with n_{inv} carriers per cm^{-2} in a MOSFET with a surface trap density of N_t defects per cm^2 [62]. Let the rate of trapping be r_1 and rate of de-trapping be r_2 and the probability that a trap is occupied at a given time be P_{occ}. In that case, we can write:

$$r_1 = c_1 n_{inv} N_t (1 - P_{oc}) \tag{3.1}$$

$$r_2 = c_2 N_t P_{oc} \tag{3.2}$$

where, c_1 and c_2 are constants. These are first order rate equations stating that trapping is linearly proportional to the density of unoccupied traps and the density of "trappable" charge; de-trapping is linearly proportional to the number of occupied traps.

Under steady state conditions, the rate of capture will balance with the rate of emission ($r_1 = r_2$.) Thus:

$$c_1 n_{inv} N_t (1 - P_{oc}) = c_2 N_t P_{oc} \tag{3.3}$$

$$P_{oc} = \frac{c_1 n_{inv}}{c_1 n_{inv} + c_2} \tag{3.4}$$

$$r = r_1 = r_2 = \frac{c_1 c_2 N_t n_{inv}}{c_1 n_{inv} + c_2} \tag{3.5}$$

Let us explore the case in which the mobile density gets large. As $n_{inv} \to \infty$,

$$r = c_2 N_t$$

This indicates that the noise is only a function of trap density when the transistor is in strong inversion (n_{inv} is large.) The rate of capture, r, is equal to i_n. This is the total noise current. Assuming trapping and de-trapping to be a Poisson's process, the fluctuation in the trapping noise current $< \Delta i >$ can be written (recalling equation 2.9) as:

$$< (\Delta i_n) >^2 = 2 c_2 N_t \Delta f \tag{3.6}$$

or:

$$< \Delta i_n > = \sqrt{2 c_2 N_t \Delta f} \tag{3.7}$$

If the channel current is i_{ch}, total current is given by:

$$i_t = i_{ch} + i_n \tag{3.8}$$

It appears that by increasing the channel current, we can make the trapping noise current an insignificant part of the total current. Thus, the traps appear "saturated," the trapping/de-trapping current saturates, as does the trapping/de-trapping noise.

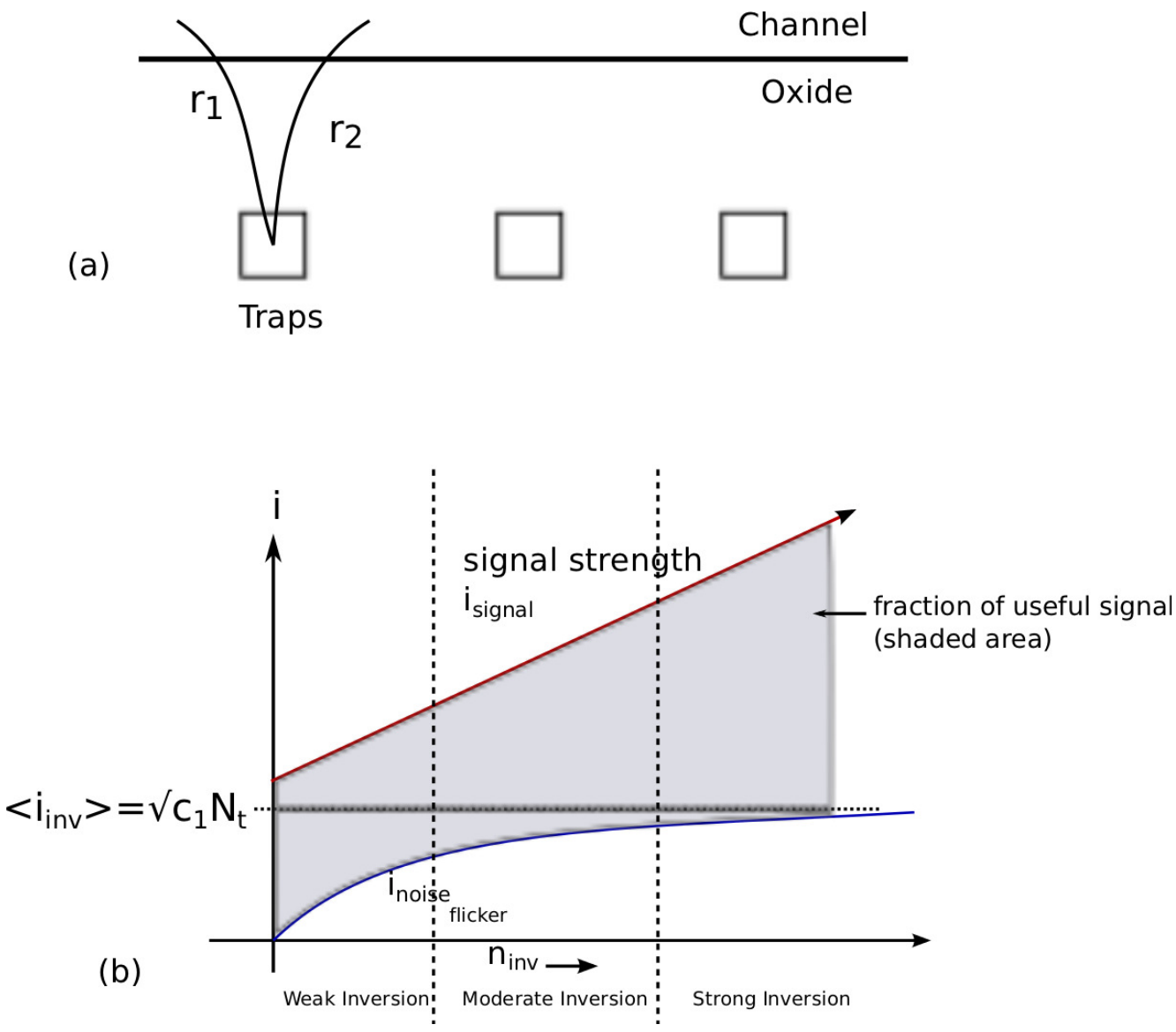


Figure 3.1: (a) Process showing trapping and de-trapping: Charge carrier capture rate r_1 and release rate r_2 from oxide trap. (b) Noise current i_n increases with inversion charge (McWhorter) but converges to $\sqrt{c_1 N_t}$ as inversion charge density increases. Noise becomes a small fraction of the total signal in the channel.

We can increase the channel current by increasing the gate bias. This, of course, increases power dissipation. From a design perspective our goal must be to "overwhelm" the trapping current with channel current without exceeding the power dissipation design goals for the system. This is the basis for the noise-optimized design methodology described in greater detail below. We must set the transistor gate bias points at the onset of the noise plateau. This will minimize noise without overdriving the system into excess power dissipation.

A few things should be noted. First, these results do not indicate that we can drive the signal-to-noise-ratio (SNR) to infinity! The saturation calculation only refers to the scattering-center induced noise which exhibits a bias dependence. This noise will reach a minimum as shown in equations 3.6 or 3.7. This noise will add to the bias independent thermal noise to achieve a noise floor and to the current dependent shot noise. And, as previously remarked, high channel current leads to more thermal noise through channel heating.

The treatment described here does not lead to a 1/f process per se. That is because it does not include the distribution in relaxation lifetimes required to achieve the pink noise spectrum. That, though, does not invalidate the saturation model. We may view the relaxation lifetime distribution resulting purely from the depth distribution of traps moving into the oxide from the oxide semiconductor interface. We can look at the noise spectrum as the result of contributions from planar sheets of oxide charge separated from the interface by some incremental distance. The total noise will be the sum of individual contributions from each sheet. Each sheet will exhibit saturation and the whole process will saturate at some critical voltage

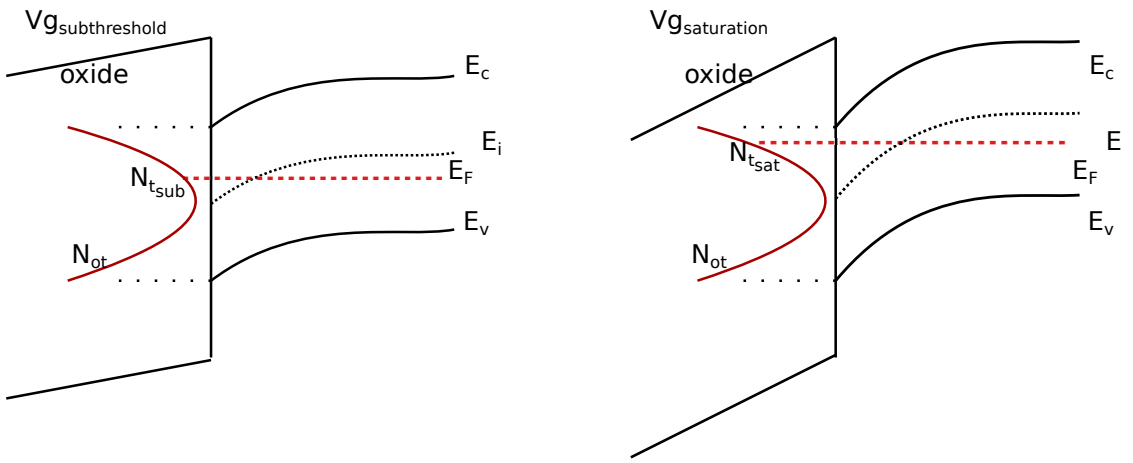


Figure 3.2: Change in trap density with increase in gate voltage. In weak inversion, oxide trap density is equal to $N_{t_{sub}}$ and in strong inversion, it is equal to $N_{t_{sat}}$. $N_{t_{sub}} < N_{t_{sat}}$.

bias level.

In addition, there are processes that lead to higher noise as the gate bias increases. The dependence of mobility on gate bias has been known for some time. Higher interface electric fields force mobile charges closer to scattering centers, leading to stronger scattering. The net effect is as though we had increased the number density of interface scatterers, N_t. In addition, as the band bending in the semiconductor increases, the Fermi level at the surface intercepts higher densities of interface states present in the band gap (figure 3.2). This, too, leads to an apparent increase in the number of surface scatterers. Thus, the plateau region in the SNR vs gate bias might actually turn around at high gate bias, leading to a mathematical optimum point for gate bias. As these effects are all process dependent, it is impossible to derive a first principles optimization for gate bias. All of these bias issues raised

here must be explored experimentally. An attempt to do this is provided in chapter 4.

Before moving on, let us summarize by describing the bias-dependent noise levels predicted by the discussion so far. At very low bias the low density of channel charge leads to small output signals from amplifying devices. Also, a significant fraction of the charge present in the channel interacts with the surface defect population, leading to larger fluctuation in channel current (higher noise.) Thus, as the bias increases from the onset of sub-threshold on to strong inversion, the signal to noise ratio should increase monotonically. This is experimentally observed, as shown in the next chapter.

But the increase in SNR cannot continue indefinitely. The maximum driving point current of the device is set by the safe operating range of the transistor. Also, power dissipation increases as the driving point current increases. These considerations set hard limits on the maximum signal to noise ratio. Moreover, even before these hard limits are reached, other factors potentiate the trap scattering effect. Increasing the surface field of the active channel forces channel charge closer to the oxide-semiconductor interface, increasing scattering, reducing mobility. In addition, as the gate is biased toward inversion, the Fermi level at the interface moves toward the band edge. It is well known the density of interface traps pile up near the band edges [27]. Thus, the mobile channel charge has a larger effective trap density to scatter off of. This further degrades SNR as bias increases. Also, channel heating may increase phonon scattering at the interface, further degrading SNR.

Thus, we might even anticipate a "roll-over" in the monotonic SNR vs gate

bias curve, leading to some maximum in the SNR followed by a decline. While no such maximum has been observed, the SNR vs gate bias curve tends to flatten out as we move past the strong inversion bias point, consistent with the arguments given above. This behavior is shown in the next chapter.

The remaining question centers on the relation of the number density (McWhorter) model to the bulk mobility fluctuation (Hooge) model. Both models hinge on the interaction of mobile channel charge with a finite density of scattering centers. Thus, the saturation model described here should be operant in Hooge's model as well. Hooge's model includes phonon scattering explicitly, while McWhorter's model emphasizes the impact of defect trapping and de-trapping. As such, there would be a stronger temperature dependence on SNR as predicted by Hooge. In this case, there should be a strong improvement in SNR as the phonons are "frozen out" at low temperatures. This is normally dealt with as a temperature dependent α parameter in Hooge noise term. This could be handled by a temperature dependent N_t in the saturation model.

The observed dependence of noise on temperature is quite complicated. This is most likely because some aspects of each model are active over a broad range in temperatures. And each of these models has temperature dependence built in. The McWhorter trap lifetimes and cross sections are temperature dependent. For example, the impact ionization parameters ([1]) tend to increase at lower temperatures. This would lead to stronger coupling between the traps and the mobile carriers in the active channel. This in turn, leads to larger SNR at low temperatures. More discussion of this effect is presented in chapter 6.

3.2 Low temperature operation of MOSFET

Operation of the MOSFET and the associated flicker noise phenomenon is affected by operating temperature. In this section we discuss low temperature operation of device and its effect on flicker noise. We are particularly concerned with channel current in the main operating bias regions as well as with cooling or transient behavior. Key points are summarized below.

Current

Strong inversion region:

With fall in temperature ($50K < T <$300 K), lattice vibration decrease and scattering of mobile carriers reduces. This results in increase of electron mobility. Temperature reduction also increases the depletion region and space charge length. t also results in rise of threshold voltage as fermi level moves to the band edge ($\frac{dV_t}{dT} \approx -1mV/K$, as shown in equation 3.9) but the increase in mobility dominates all other effects. This results in higher current value in saturation region.

$$\frac{dV_t}{dT} = -(2m-1)\frac{k}{q}(ln(\frac{\sqrt{N_c N_v}}{N_a}) + \frac{3}{2}) + \frac{m-1}{q}\frac{dE_g}{dT} \tag{3.9}$$

Weak inversion region:

Conduction in weak inversion is dominated by diffusion and increase in net mobility has no effect at these temperatures, instead decrease in thermal voltage dominates and causes a net decrease in channel current (equation 3.10).

$$I_{wkinv} = I_0 e^{(}\frac{\kappa V_{GS}}{U_T})e^{(} - \frac{V_{DS}}{U_T}) \tag{3.10}$$

where, I_0 is the leakage current.

Transient:

Due to carrier freeze out, drain current rises slowly to its steady state value. Inversion layer and depletion region are formed after impact ionization by drain substrate current. After inversion charge is formed (impact ionization), there is a significant drain-substrate current and source-substrate current, and drain current is much less than the current at room temperature [5].

Steady State:

At time of depletion region formation, the substrate due to freeze-out is not grounded and is floating. On increasing the drain voltage, drain-substrate current increases and causes a potential drop across the substrate forward biasing the channel-substrate and hence, decreasing the threshold voltage of the NMOS. This leads to a rise in drain current seen as a kink in drain voltage vs drain current. In weak inversion, drain current is much less (cut off for the On Semi process) compared to the leakage current.

3.2.1 Flicker Noise at Low temperatures

The decrease in temperature has both positive and negative effects on SNR. As temperature goes down, phonon scattering must clearly go down, reducing fluctuations of the type envisioned by Hooge. But trap scattering cross sections go up (as predicted by the Chynoweth model [16, 15].) This is further substantiated by

the increase in impact ionization observed at cryogenic temperatures [1]. The traps seem to "get stickier" at low temperatures indicating a stronger coupling between these traps and the mobile charge population. Also, at low temperatures, the Fermi level moves to the band edge, increasing threshold. Thus, at a given gate bias, the mobile channel density will decrease as temperature reduces due to a reduction in channel mobile charge. Increasing the gate bias would offset this effect. But the overall effect of these contributions is quite complex and explains the widely varying reports of the results of cooling on noise in the literature.

3.3 Noise Measurement Technique

Measuring the noise floor of a device is a challenging problem. Most of the techniques available use low noise amplifiers and signal analyzers but measurement accuracy and precision is limited by the instrument noise floor [38, 9]. This has restricted the ability to probe device operation in deep subthreshold region where channel current is extremely low (<100 nA). Device current is much lower than the instrument 1/f noise. Noise spectroscopy also plays a very important role in defect analysis as it can capture G-R response. Hence, it is very important to find a more accurate and sensitive method of noise measurement. It has been shown that cross-correlation can be used to eliminate the measurement noise [67, 70]. Another major contribution of this thesis noise characterization of devices (130 nm IBM and 0.5μ On-Semi) biased in deep-subthreshold region using two-channel noise measurements. Double channel technique made it possible to characterize noise behavior under

very low channel currents. This method and its impact on 1/f characterization is described in some detail here.

Here, we analyze and compare the two measurement techniques: single channel and double channel measurement of methods. Double channel technique eliminates the instrumentation noise allowing accurate and 'fast' measurement of noise under very low drain currents. We use cross-correlation method to probe deeper into subthreshold region of noise.

3.3.1 Single Channel Method of Noise Measurement

Noise measurement using a single channel method provides a record of the transistor channel noise as well as the noise of the measuring device superimposed on it. Measured noise of the device is thus limited by the noise floor of the measuring equipment [38, 56, 14]. A large number of averages improves the measured noise to some extent as it gets rid of Gaussian noise process (thermal and shot) but can be time consuming [67]. It is important to get rid of the noise of the measuring equipment in order to accurately get the noise of the device using fewer averages. This would provide the ability to measure noise of very low currents in the device under test (DUT) which would not be feasible using the conventional methods. It reduces the impact of thermal noise on data interpretation.

3.3.2 Double Channel Method of Noise Measurement

It has been shown that by taking the correlation between measurements from two separate amplifiers (shown in figure 3.4) measuring same DUT removes the amplifier noise, improving the accuracy of the results [70, 67]. This is similar to differential input signal sampling in a standard operational amplifier. In that case, though, signal processing is done at a single point in the time domain. The essence of the multi-channel approach is to have one channel probe a node on which the desired signal is present along with noise. A second amplifier channel is placed on the same node (figure 3.4). The instrument noise in the first amplifier is uncorrelated with instrument noise on the second. Identical copies of the signal are also placed on the inputs of each amplifier. Taking the cross correlation of the output stream from both amplifiers followed by Fourier transform of the cross-correlated data yields a power spectrum with the noise cancelled.

The computational basis is obtained by writing the total signal at each node as a sum of signal plus noise:

$$v_1(total) = v_1(t) + e_1(t) \tag{3.11}$$

$$v_2(total) = v_2(t) + e_2(t) \tag{3.12}$$

where the v's are the signal components and the e's are the noise components on each channel. The v(total)'s refer to the total excitation present on each channel (signal plus noise.) We can cross-correlate the total signals as follows:

$$R_{1,2} = \int (v_1(t) + e_1(t))(v_2(t+\tau) + e_2(t+\tau))dt \tag{3.13}$$

or:

$$\begin{aligned} R_{1,2} = \int v_1(t)v_2(t+\tau)dt + \int e_1(t)e_2(t+\tau)dt + \\ \int e_1(t)e_2(t+\tau)dt + \int e_1(t)v_2(t+\tau)dt + \int v_1(t)e_2(t+\tau)dt \end{aligned} \tag{3.14}$$

The first integral in this equation 3.14, is the autocorrelation of the signal with itself. The second integral is the autocorrelation of the noise, identically zero. The last two expressions are also zero, as the noise takes on random values (positive and negative) above and below the signal mean line. By the Wiener-Khinchen theorem, the Fourier transform of this gives the power spectrum [43]:

$$S(\omega) = \mathcal{F}\{R_{1,2}\} \tag{3.15}$$

where $\mathcal{F}$ indicates Fourier transformation. Note that the noise terms are missing.

Double channel method increases the sensitivity of the measurement, making it possible to extract noise of deep-subthreshold current. Double channel method is capable of measuring signal power one order of magnitude below the single channel method [70]. Added advantage of the method is that it allows the measurement of noise in fewer averages [67]. Thus, double channel method can extract low current noise in a smaller amount of time. In other words, the noise floor of the instrument can be reduced substantially by use of double channel method. It has been been shown that PSD of as low as 1 fA/$\sqrt{Hz}$ can be measured using this method along

with averaging [70]. Its been shown that for a 100 Gohm resistor, the theoretical PSD given by $\sqrt{\frac{4\kappa T}{R}}$ is 4x10^{-16} A/$\sqrt{Hz}$. Single channel method give a value of 4x10^{-14} and double channel method gives a reading of 0.1x10^{-14} These measurements were taken at room temperature (290 K) [70].

Table 3.1: Comparison of Single Channel and Double Channel Noise measurement: Single channel method which uses one amplifier with double channel method which uses cross-correlation of data between two amplifiers (double channel) to eliminate uncorrelated noise from amplifiers. Double channel method shows more an improvement by a factor >10.

S.No.	Parameter	Single Channel	Double Channel
1	Low Noise Amplifier	1	2
2	Method	Autocorrelation	Cross-correlation
3	Noise Floor (100GOhm)	$4e^{-14}$A/$\sqrt{Hz}$	0.1 e^{-14} A/$\sqrt{Hz}$

The figure 3.3, shows the noise measurement setup. Details for single channel measurement were provided in Chapter 3. And figure 3.4 shows the double channel method. The amplifier 1 is connected to the drain of the transistor (DUT), drain voltage is set to fixed value. The source current of the transistor is read by the amplifier 2 and such voltage to set to zero. Signal analyzer was operated in double channel mode and correlation function used between the channel 1 and channel 2. The DUT gate was biased using battery. DUT was placed in an enclosed chamber.

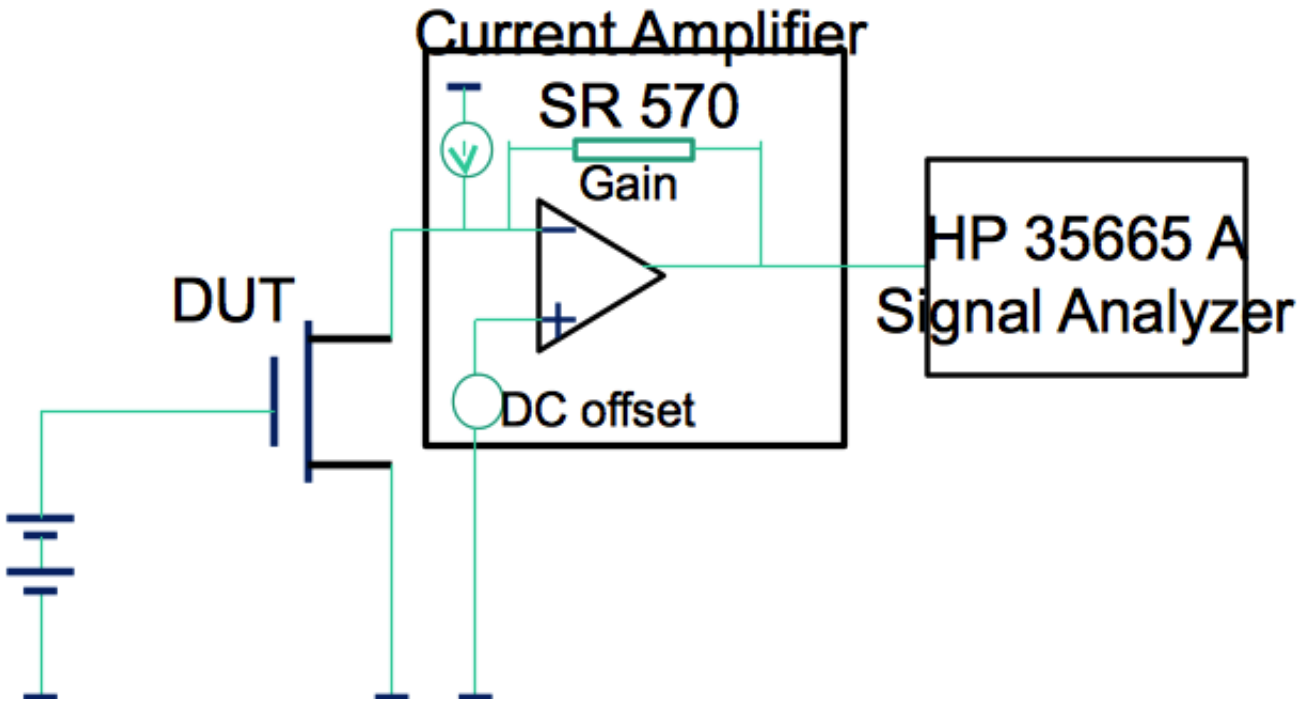


Figure 3.3: Experimental setup for single channel measurement. Drain current is amplified using Low Noise Current Amplifier (SR 570). FFT is obtained using Signal Analyzer.

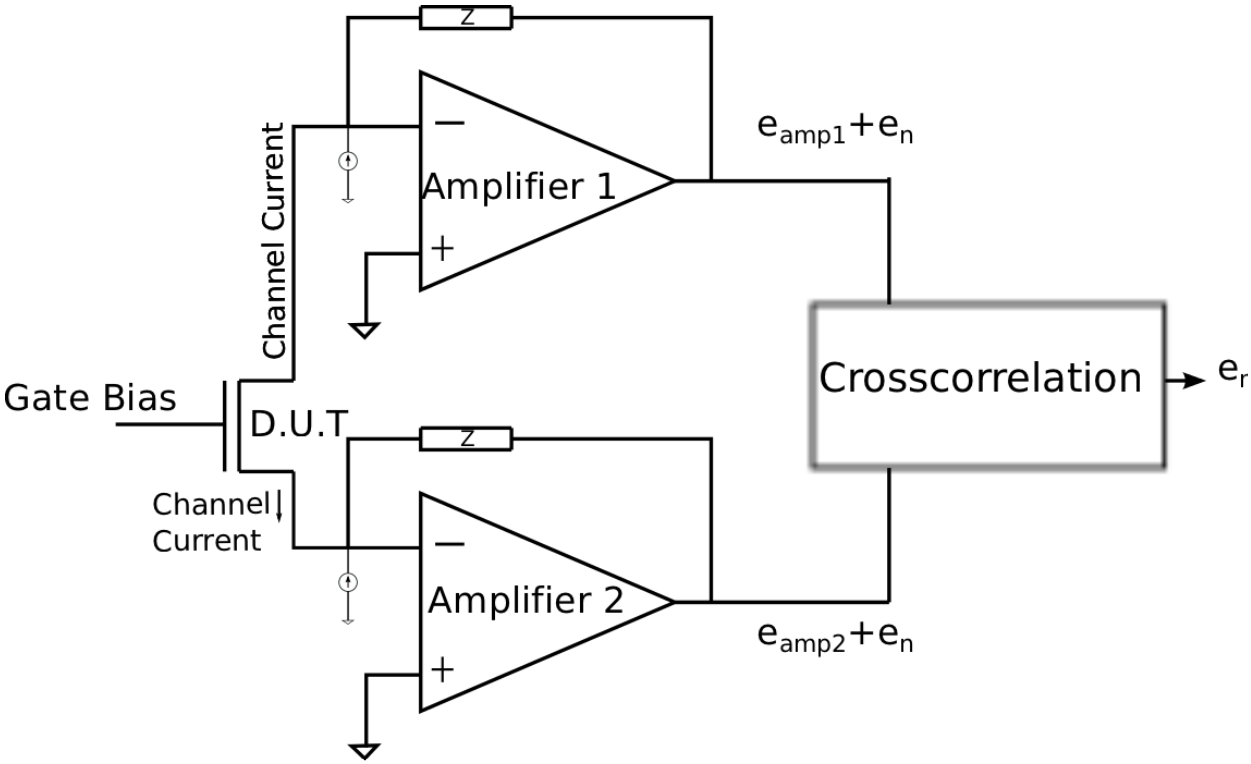


Figure 3.4: Schematic for Double channel measurement. DUT current is measured using two different amplifiers and then cross correlation is taken between the two signals to eliminate the amplifier noise.

3.4 Figure of Merit for Flicker Noise

As mentioned in the previous chapters, flicker noise in CMOS transistors has been under investigation since past few decades. One of the reason for discrepancy on flicker noise literature is due to differences in evaluation methods. Flicker noise is measured either as noise in drain current or at the gate of the MOSFET transistors. In 1994, researchers at UCLA measured noise in number of MOS transistors from various foundries [14]. In first part of their study, they compared input referred flicker noise behavior with change in gate bias voltage in their devices and in the second part of their study, they studied the noise at different temperatures. They did not observe any variation of input referred flicker noise with change in gate bias and change in noise with variation of flicker noise with change in temperature was not conclusive either. Noise did not follow any particular trend with change in temperature.

In another study done in 1998, authors compared normalized flicker noise in CMOS devices [10, 23]. Normalized noise was defined as the noise divided by the signal strength (drain current). This comparison gave a better understanding of noise per unit signal strength. Their observation led them to conclude that normalized noise decreases with increase in drain current.

In 2001, another research group compared the absolute flicker noise (S_{I_D}) in CMOS transistors [58]. They observed an increase in flicker noise with increase in drain current and concluded that operating circuits at very low drain currents reduces the effect of flicker noise. This has been a recent trend among analog circuit

designers- to bias the circuits in subthreshold region to reduce effect of both noise and power [21, 11, 28, 44].

3.4.1 Signal to Noise Ratio for Low Frequency Design

From the perspective of a circuit designer, it is important to consider both the bias strength (I_D) and noise (S_{I_d}). The bias strength, is the biasing current in the transistor. It is the D.C. current which determines the inversion charge density in the channel on which small signal A.C. current is superimposed. For any distribution (e.g. Gaussian, Stochastic) of signal super-imposed on the DC bias, the signal power being carried on DC current I_d, can be defined as HI_d^2. We define, SNR as:

$$SNR_{signal} = \frac{HI_d^2}{S_{I_d}} \tag{3.16}$$

where, H is constant and depends on the property of the signal. Let us focus on $\frac{I_d^2}{S_{I_d}}$ and define:

$$\frac{I_d^2}{S_{I_d}} = SNR_{DC_{flicker}} \tag{3.17}$$

Units for I_d^2 is A^2 and for S_{I_d} is A^2/Hz. Hence, we define SNR for a bandwidth Δf Hz or at a single frequency f Hz . A ratio of $current^2$ to noise power for a given frequency is also dimensionally consistent. For a circuit designer dealing with low frequency signals, a good assessment of inversion charge to fluctuating current/charge can be made by the ratio of D.C. signal to flicker noise into consideration. As S_{I_d} depends on channel inversion current, $SNR_{DC_{flicker}}$ gives a fair

comparison of useful inversion charge density to noise due to fluctuation in conductivity. From this point onwards, $SNR_{DC_{flicker}}$ will be written as 'SNR' only in this dissertation but it will imply the DC SNR for low frequencies.

SNR gives a relative measure of signal and noise unlike other figure of merits: input referred noise or the absolute noise which cannot be directly used for comparison purposes by circuit designers. Normalized noise as discussed above ([23]) forms a preface for our choice of using SNR as a figure of merit (for low frequency region).

In subthreshold region, the DC signal strength I_d^2 is weak and flicker noise S_{I_d} is also low. Whereas under high gate bias voltages, the inversion charge density (signal strength), I_d^2, is high and noise S_{I_d} is also high. Investigation into the how ratio I_d^2/S_{I_d} behaves with gate bias addressed through experimental work.

Chapter 4

Chapter 4: Test Devices, Environmental Stress Experiment and Measurement Techniques

During the course of this work, noise generation in MOSFET transistors was studied under a variety of environmental conditions. The transistors were obtained as test structures from two foundries: the MOSIS 0.5 micron line operated by ON semiconductor and the IBM foundry (through its 8RF process line). This chapter contains information on device processing and the selection of test vehicles for inclusion in this thesis. In addition, the types of environmental stress applied are described. Test and evaluation methodology is fully outlined. This includes a description of the one and two channel noise measurements techniques.

4.1 Transistor Fabrication

Both of the selected foundries are bulk CMOS process lines. Information on the ON SEMI process can be gotten from the website:

http://www.onsemi.com/PowerSolutions/content.do?id=16693.

Information on the 8RF line is found on-line at

http://public.dhe.ibm.com/common/ssi/ecm/en/tgl03002usen/TGL03002USEN.PDF.

The on-foundry is a standard bulk CMOS line, while the IBM process contains a

SiGe biCMOS option as well. This is described in [19, 37]. The 130 nm IBM process is a 5-8 metal layer twin well (n-well and p-well), low noise technology for RF analog design. It is extensively used in industry for low-cost high-speed analog radio frequency designs like bluetooth and global positioning systems. Low impedance interconnects made of Cu are used in lower layer and Aluminum is used only in the top layers. The substrate is a non epitaxial doped p-type Silicon. Another feature is the use of low resistance cobalt silicide poly-silicon and diffusion regions. Recommended operating voltages are 1.2 V and oxide thickness is 2.2 nm. The process provides shallow trench isolation. The measured threshold voltage is approximately 0.45 V.

The ON 0.5μ CMOS process is 3 metal - 2 poly process in a p-type substrate. The process provides a medium density process for mixed signal analog design [60]. Aluminum metal is used for interconnects. Gate oxide thickness is 13.5 nm. Estimated threshold voltage is 0.9 V

4.1.1 Test structures

On Semi: Transistor and op-amp circuits were designed, simulated and fabricated using the 0.5 micron On Semi product design kit (PDK.) The n-MOS and p-MOS transistors were W=L=3.5 μm, as laid out. The details of the amplifier will be discussed in chapter 7. Noise measurements were taken on five different chips all from the same process batch. A magnified picture of the chip area is shown in figure 4.1.

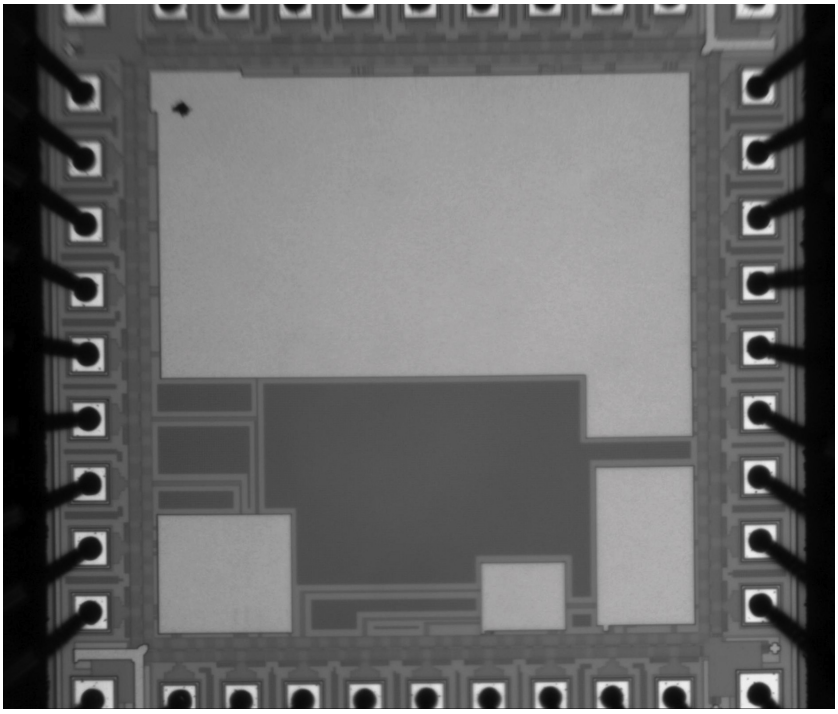


Figure 4.1: Picture of chip with test structures for noise. Process: On Semi 0.5 μ. Part of the chip is covered with ground plane to minimize noise and interference.

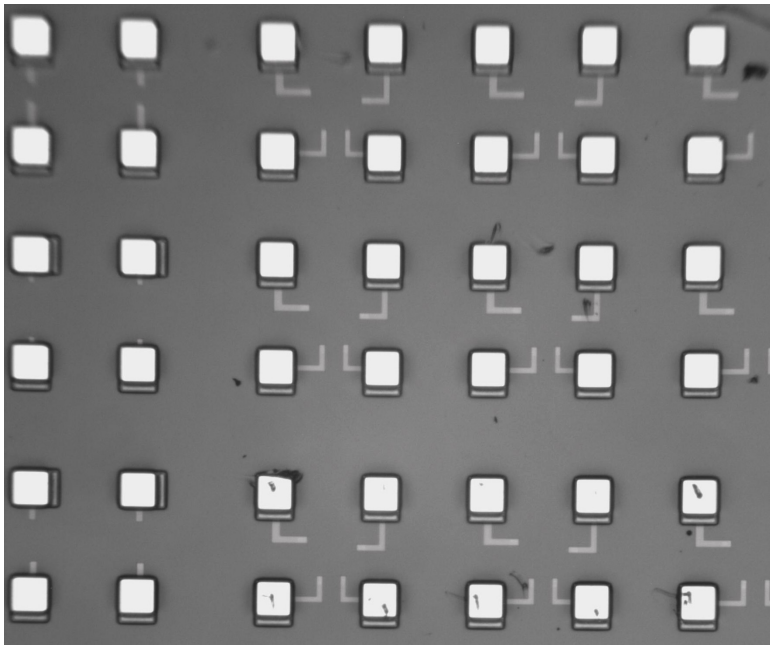


Figure 4.2: Picture of chip with array of transistors. Process: IBM 130nm. (Courtsey: CoolCAD)

IBM: An array of n-MOS and p-MOS transistors with varying sizes was laid out (courtesy: CoolCAD). The W and L values selected for the tests were W=960 nm and L=960nm and 480 nm; and W=480 nm and L=120 nm. Picture of test array structures is shown in figure 4.2.

4.1.2 CMOS Process Flow

The CMOS process flow provides, in detail, the sequence of oxidation, etching and patterning steps involved in the fabrication of a transistor on a silicon substrate. Present day CMOS technology uses poly-silicon as a gate material [1] and uses a self-alignment process registering the transistor gate to the source and drain. In a n-well

[1] deeply scaled CMOS structures may include refractory metal gates.

process, like the one discussed here, NMOS transistors are fabricated directly in the p-type substrate where as PMOS transistors have to be fabricated in an n-well.

The basic steps involved in the fabrication of a n-type transistor are outlined here (figure 4.3). Starting with a p-type wafer, the field oxide is grown first on the wafer (Step A). A window, for fabricating the transistor is opened in the field oxide and gate oxide (thermal oxidation) is grown. The complete window is covered with covered with poly (doped amorphous silicon) (Step B). Then, gate is patterned on the poly and gate oxide and two windows for source and drain opened (Step C). The gate poly and oxide act as a mask for next stage which is ion implantation in the drain and source by n-type dopant (phosphorous) (Step D). The implanted ion pockets are formed which are annealed by heating the wafer. Annealing diffuses the dopant ions which extend under the gate oxide forming the channel overlap region (L_{ov}). After formation of drain and source, field oxide is deposited. Connection the drain and source are made by opening a contact window in the drain and source (Step E). The contact window is filled with metal. This metal (aluminum or copper depending on the process) connects to other layers via connections called 'via'.

Twin well processes, like IBM process described here, first form a large p-well in the substrate by ion implantation. The gate oxide is grown over gate oxide installed in the cut in the field oxide. Post fabrication trenches are fabricated in IBM RF process to minimize cross talk.

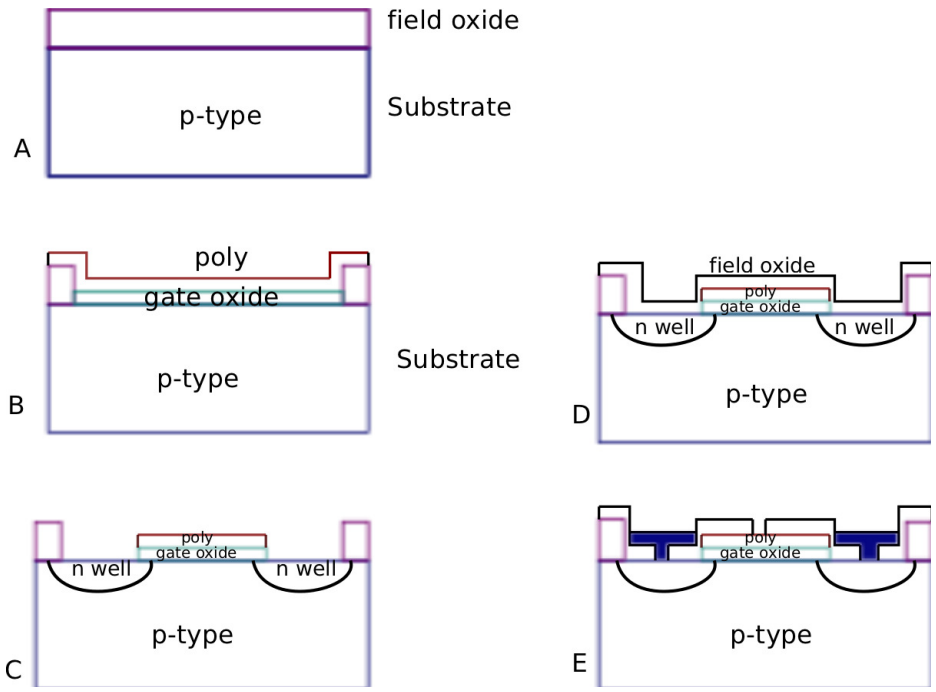


Figure 4.3: Fabrication of N-MOS transistor: Process Flow.

4.2 Transistors Stress

Transistors operating under environmental extremes (like radiation and high drain currents,) become damaged and there is an attendant increase in channel noise due to the reasons outlined in chapters 2 and 3. The two main stresses studied are (a) γ-radiation and (b) hot electron injection. Irradiation degrades the material by creating traps in the oxide; high drain current degrades the oxide by hot electron injection. Introduction of extra traps by the process of irradiation and hot electron injection affect the low frequency noise differently in different biasing regions of operation. This chapter is limited to a description of the stresses employed and the pre- and post stress measurements made on these structures.

4.2.1 γ-ray Radiation Exposure

γ-rays are high energy electromagnetic (EM) waves which tear/rip electrons away from atoms creating ionizing effect and damaging the material they interact with. Exposure of CMOS device to γ-radiation (gamma radiation), degrades the device material including the gate oxide. Damage increases with increase in duration and intensity of exposure. Ionizing effect creates defects in the oxide generating more traps (both, oxide and interface traps) [61]. An increase in flicker noise magnitude is expected.

The effect of radiation exposure on nMOS transistor is shown in the figure. 4.4. Mobile electrons created by radiation exposure move out of the oxide easily whereas the positive ions due to lower mobility (due to its higher mass), stay in oxide and silicon interface. The positive ions trapped in the gate cause a change in the threshold voltage of the NMOS device and increase the device g_m. Over time, the traps get self annealed [22].

Irradiation of the device results in an increase in oxide trap density as well as an increase in interface traps. Using I-V curve and subthreshold slope, for the irradiated transistor, the trap density for interface trap and oxide trap is calculated using a standard method of trap density extraction [51] (details in following section). Research into investigation of the nature of traps generated by irradiation has shown that the traps generated are mostly close to the boundary of the silicon and silicon oxide and are different from interface traps which have shorter time constant [69]. These traps have been called **boundary traps**. Interface traps lie at the interface

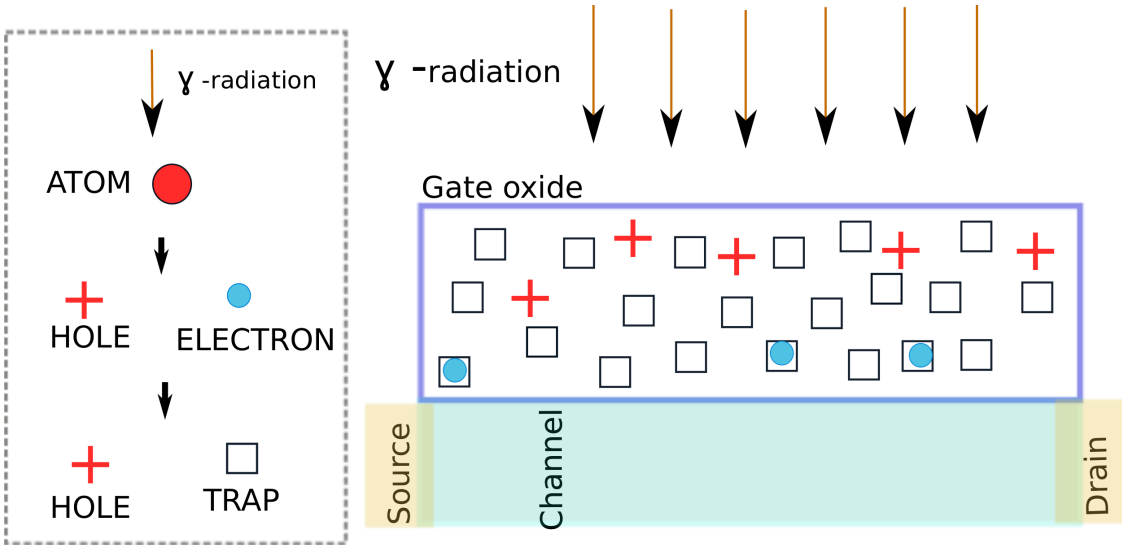


Figure 4.4: Effect of γ-radiation on NMOS transistor. Positive ions due to low mobility stay in oxide and decrease the threshold voltage. There is a net increase of trap density per unit inversion charge after exposure to γ-radiation. Thus, $\frac{S_{I_d}}{I_d^2}$ is higher after irradiation.

and are due to free dangling bonds at the interface. Interface traps give rise to a stretched-out appearance to the capacitance-voltage plot. Oxide boundary traps are responsible for threshold voltage change. By measuring the change in stretch-out voltage change in interface density can be determined similarly measurement of change in mid-gap voltage gives the change in boundary oxide traps.

Experimental results disclosed in this thesis were the result of γ-rays generated by Co-60 gamma-ray beams. The irradiations described here were performed in the University of Maryland Radiation facility. Beam sources contain energy of 1.17 and 1.33 MeV.

4.2.2 Hot electron injection (HEI)

HEI is the transfer of high energy electrons from transistor channel to its gate node across the MOSFET (here, nMOS) gate oxide. High energy electrons are created by the impact ionization of atoms by carriers (electrons) moving under the influence of high electric field near the drain. Higher the drain voltage, larger is the depletion electric field at drain and higher is the kinetic energy an electron gains in the electric field. High kinetic energy increases the chances of impact ionization which results in formation of a hot (high energy) electron and an ion. A positive gate voltage (nMOS) draws the hot-electron across the gate oxide and in this process of hot electron injection oxide defects are created. HEI is unavoidable in transistors operating in deep saturation. Such applications are common in circuits using trimming programmable floating gates [76, 73]. Increase in number of oxide traps, increases the trapping and de-trapping of electrons in the traps and hence, there is an increase in the total flicker noise. Figure 4.5 shows the process of HEI and trap creation. HEI in thin oxide transistor results in significant gate leakage noise.

g_m **degradation** For thick gate oxides, the electrons get trapped in the gate oxide which increases the subthreshold voltage near the drain and changes the g_m of the device channel. Trap creation needs at least 2 eV. Its been shown that thick oxides ($> 100\mathring{A}$) show fewer trap generation [18]. 0.5 μCMOS has a thin oxide approx. 1.3 μm which implies that fewer traps are generated.

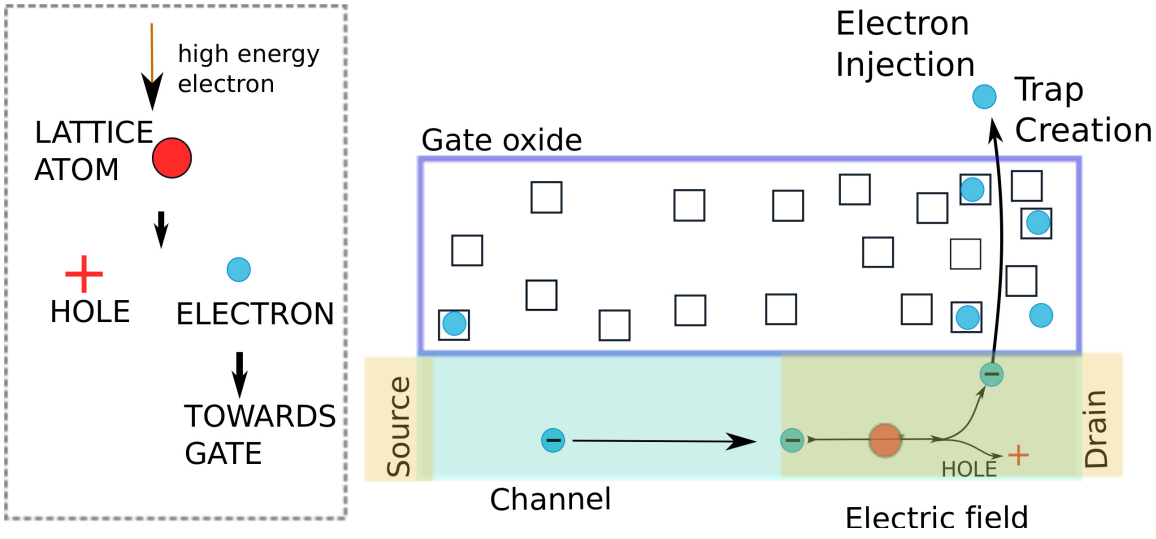


Figure 4.5: Effect of HEI on NMOS transistor. Some electrons get deposited in the oxide and some are injected to the gate after trap creation.

4.2.3 Environmental Stress Experiments

Devices are regularly operated in hazardous conditions like high energy physics laboratory synchrotron (e.g. LHC), hospital radiation lab, outer space etc. It is necessary to study the affect of radiation on devices and see how the SNR is affected. This section gives the experiment details for this study.

4.2.3.1 Radiation

Initial noise (pre-radiation) measurements were obtained and then the chip was treated with 0.5 Mrad dose of γ radiation (courtesy: Department of Materials Science, University of Maryland, College Park, Maryland). Low frequency noise and current-voltage characteristics were measured 2 hours after the treatment as described.

4.2.3.2 HEI

After measuring the initial noise in the MOSFET, the MOSFET was biased at Vds=7 V and Vgs=2 V for 15 minutes for hot electron injection. Relaxation time of two hours was given and the low frequency noise measurements taken as described in Chapter 2 (section 2).

4.2.3.3 Single Channel Data Collection

The noise measurement set-up used for the experimental work is shown in the figure 4.6. The drain current is amplified using trans-impedance amplifier. SR570 is a low noise amplifier commonly used. Signal analyzer (HP 35665A) is used to obtain the FFT of the output signal. All equipments were grounded and tri-ax cables, BNC connections used. The test device was shielded using a metal box. Batteries were used to bias the transistors.

Chapter 5 gives the detailed results derived from these experiments.

4.3 Double Channel noise measurement

The single channel techniques employed use a low noise amplifier and signal analyzer. This measurement system is explained above and we find that measurements are limited to the instrument noise. This has restricted the ability to probe the device operation in deep subthreshold region which is limited by current. In this chapter, we analyze and compare the two measurement techniques: single channel and double channel measurement of device noise. Double channel technique elim-

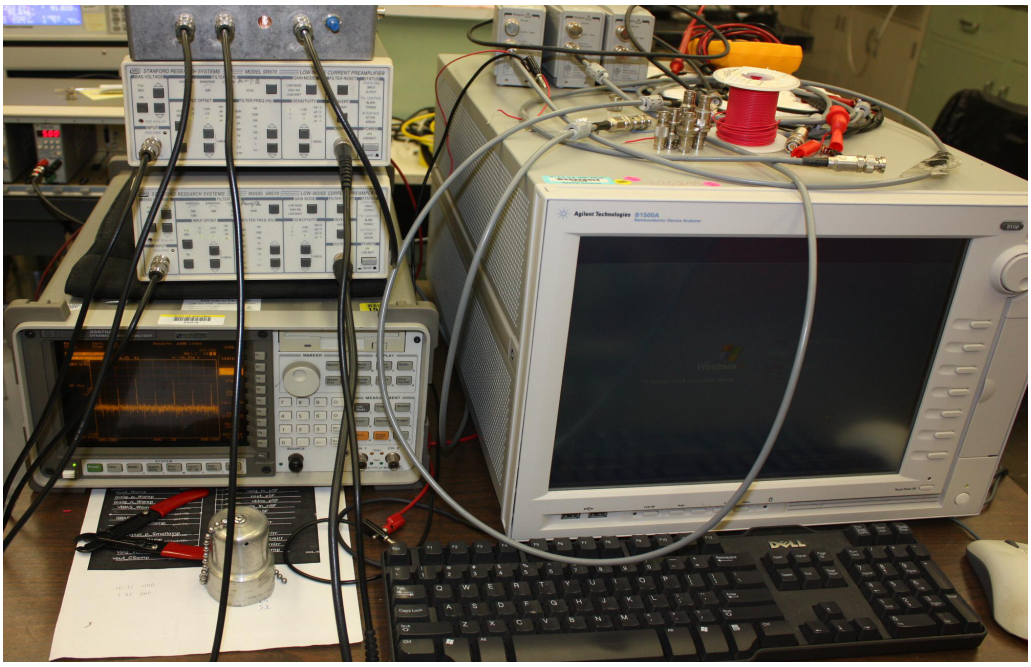


Figure 4.6: Picture showing the two channel experimental setup (Material Measurement laboratory, NIST, Gaithersburg. PI: Dr. Motayed and Dr. Davydov).

inates the instrumentation noise allowing accurate and fast measurement of noise under very low drain currents. Details have been presented previously in chapter 3.

4.3.1 Double Channel Experiments

The figure 3.4, shows the noise measurement setup. The amplifier 1 is connected to the drain of the transistor (DUT), drain voltage is set to fixed value. The source current of the transistor is read by the amplifier 2 and such voltage to set to zero. Signal analyzer was operated in double channel mode and correlation function used between the channel 1 and channel 2. The DUT gate was biased using battery. DUT was placed in an enclosed chamber. Reading were taken at a frequency resolution of 0.25 Hz. A high frequency resolution enables to see the noise processes

like G-R noise as well. In second part of the experiment, liquid nitrogen was used to cool the chamber and low temperature noise spectroscopy carried out.

Results from various experiments are given in the next chapter.

Chapter 5

Results

In chapter 4, we described the experiments where we measured flicker noise variation in transistors under different conditions and with different gate bias. The objective of the work was to determine biasing to obtain highest SNR. In this chapter, results from experiments are given. The first section gives the noise variation in NMOS transistors with gate voltage using single channel as well as double channel methods. We then investigate SNR variation with gate bias in different transistors with varying temperature and dimensions. Finally we present the results of SNR after the devices were exposed to various forms of stress.

5.1 Noise measurements methodology

Noise was measured using two different techniques: single and two-channel techniques. This was done to demonstrate the efficacy of the two-channel method.

Single Channel Noise measurement

The single channel method as explained earlier is strongly affected by addition of noise from the low noise amplifier. Normalized noise in 0.5 μm CMOS device increases with increase in gate voltage as shown in figure 5.1. The subthreshold measurements are limited by amplifier 1/f noise and the strong inversion region is dominated by thermal noise.

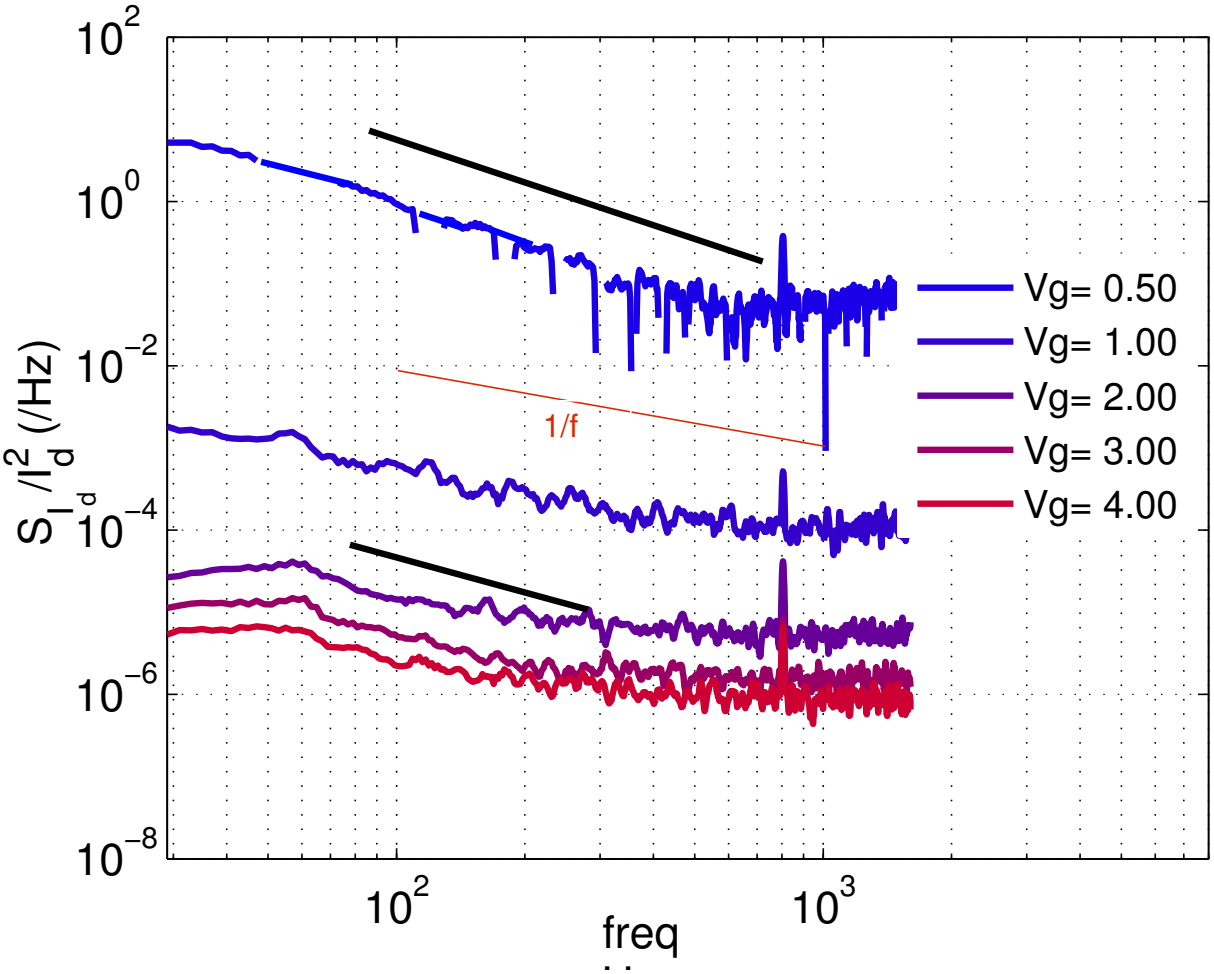


Figure 5.1: Low frequency noise (normalized) measured using single channel method. Normalized noise decreases with decrease in gate noise. As current increases thermal noise increases. Lower limit of measurable flicker noise is defined by instrument noise. Each reading was averaged 80 times approx.

Double Channel Noise measurement

The double channel method is used for noise measurement (figure 5.2) of the same device as shown in figure 5.1. We see that the noise is not corrupted by thermal noise as was the case shown in figure5.1. We were able to measure noise for very low currents in subthreshold region corresponding to gate bias as low as 0.2 V in 0.5 μm CMOS process.

Double channel measurements show uniform slopes for 1/f measurements. The measurements are not affected by thermal noise and 1/f instrument noise.

5.2 SNR

Signal to noise ratio and normalized noise variation are studied as the gate bias voltage is increased. Results are plotted for different devices under different conditions of variable length (L), temperature (T) and effect of radiation. SNR is defined as the signal strength $I_d^2\ A^2$ to the noise $S_{I_d}\ A^2/Hz$ value for chosen bandwidth or frequency. We choose Δf=1 at f=100 Hz [20].

5.2.1 Device size

Low frequency noise is a function of device size [47, 53]. Effect of device size on SNR will provide a better understanding of signal and variation in required biasing for different devices. We measured noise for different devices of sizes $\frac{960nm}{960nm}$, $\frac{960nm}{480nm}$ and $\frac{480nm}{120nm}$ in 130 nm process. The results are shown in the figure 5.5. The temperature was 230 K.

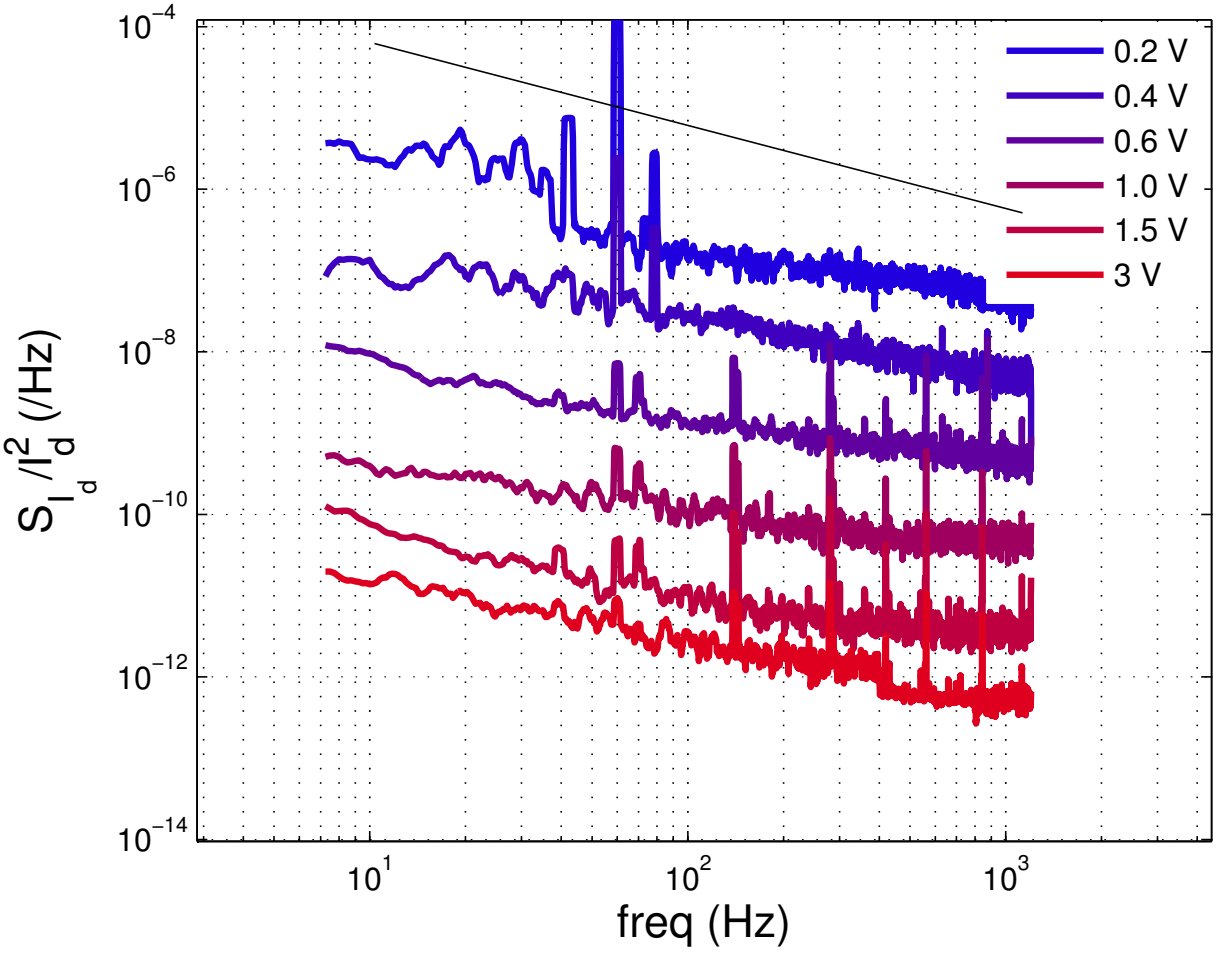


Figure 5.2: Low frequency noise (normalized) measured using double channel method. Normalized noise decreases with decrease in gate noise. 0.5 μm CMOS process. W=L=3.5 μm. 20 averages taken. Low currents value

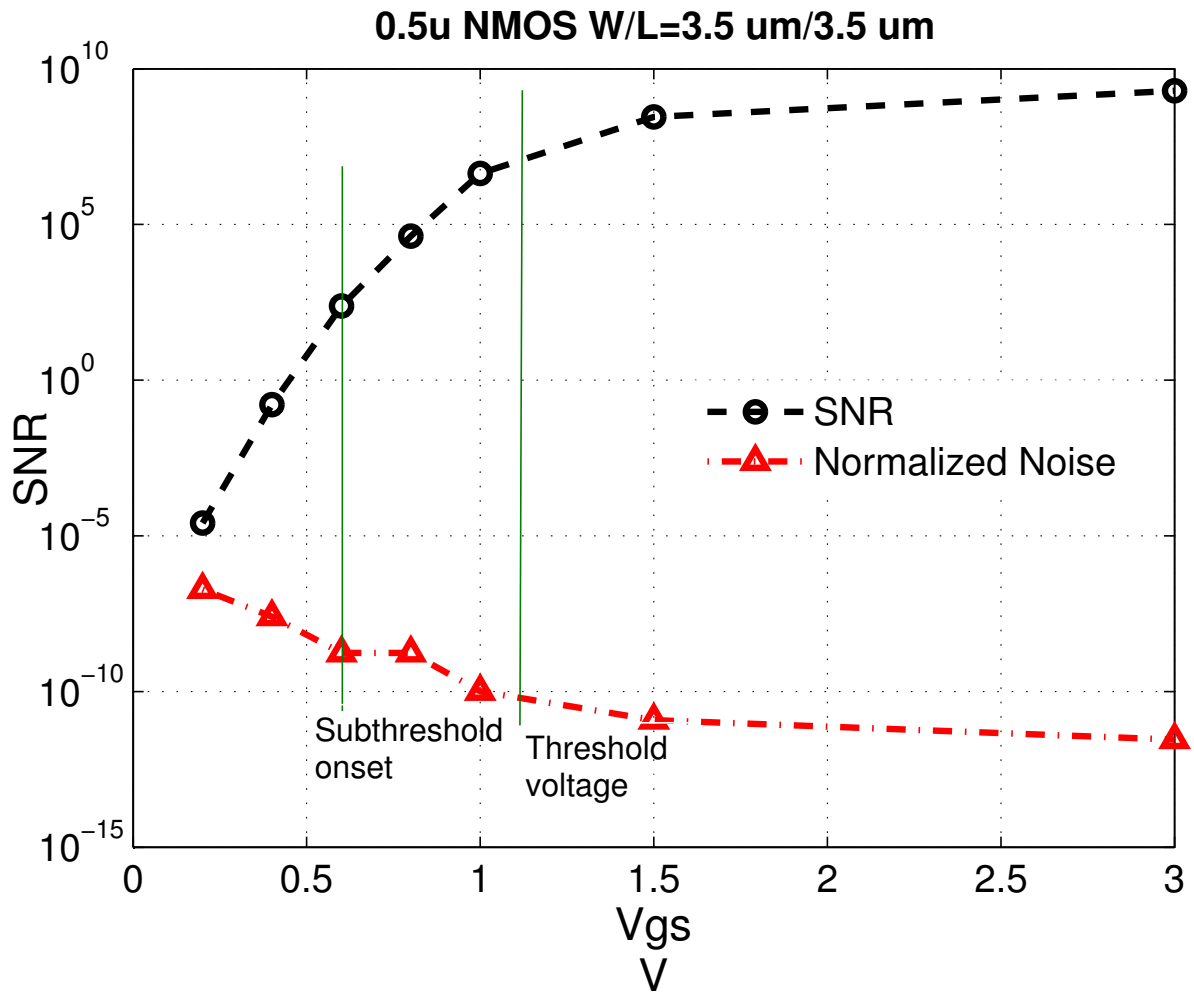


Figure 5.3: Variation of SNR at room temperature with gate voltage for 0.5 μm OnSemi process at room temperature at 100 Hz. Normalized noise is also shown in the same graph (20 sample averages taken.)

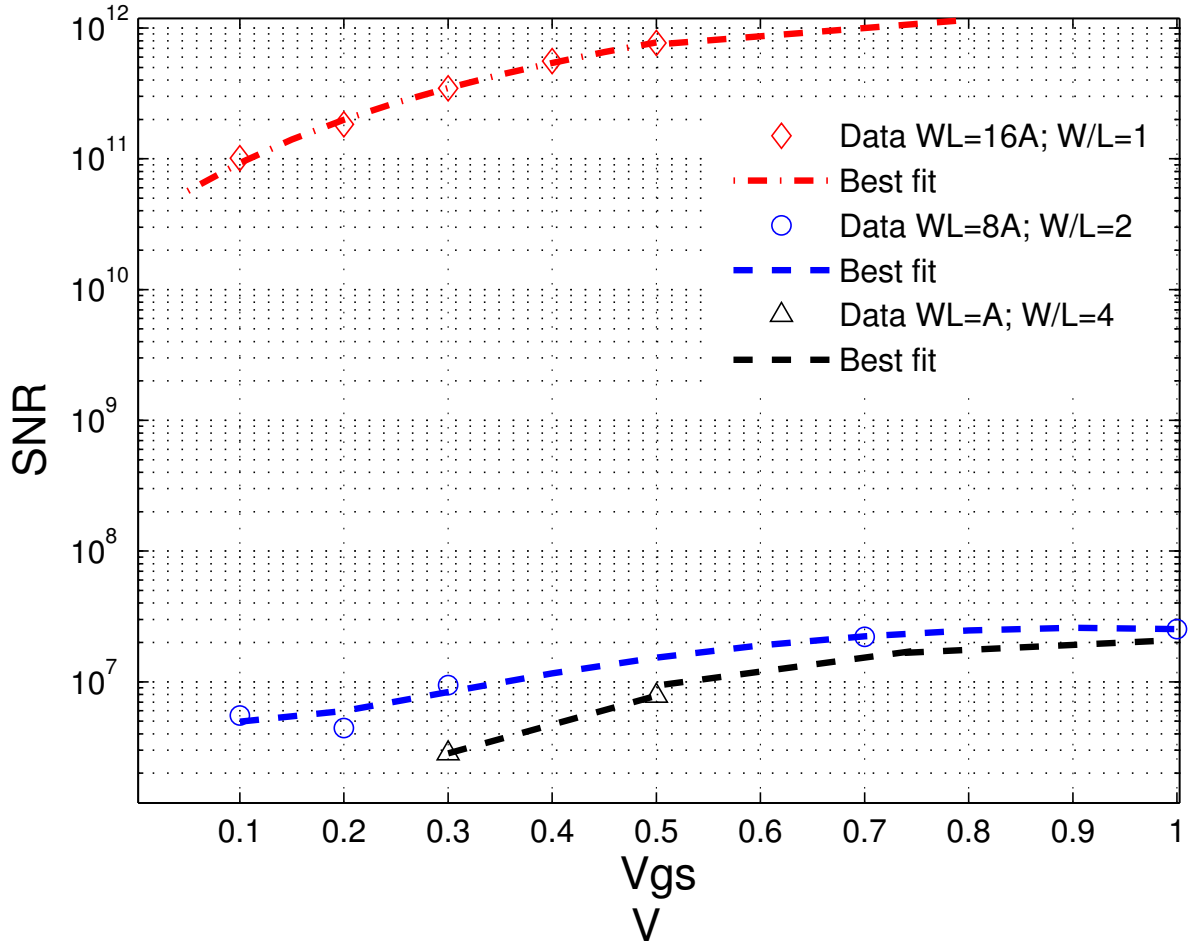


Figure 5.4: Variation of SNR at 230K with gate voltage for 130 nm IBM process. W/L sizes vary.

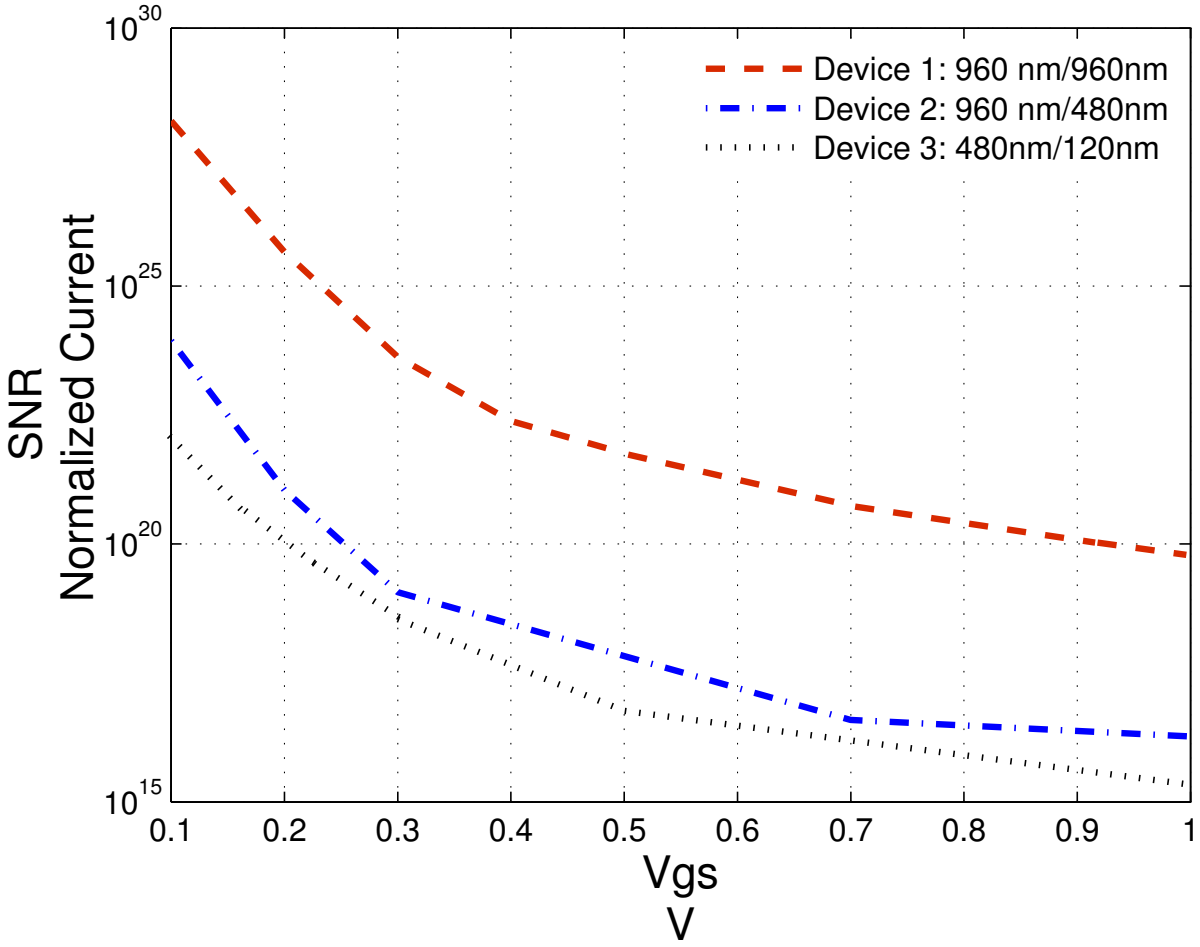


Figure 5.5: SNR for various devices was normalized with current I_d^2 for square device W=L=960 nm from figure 5.5 and plotted against gate voltage.

5.2.2 Temperature

The effect of variation in temperature was outlined in previous chapters. We know that in a MOSFET, the subthreshold current falls and current above threshold increases with fall in temperature. Study of variation of flicker noise with temperature is much disputed with no definite noise trend [46, 75]. Study of SNR with decrease in temperature can be applied to devices operating under very low temperatures like space applications.

The variation of SNR with temperature for various devices: On Semi (figure 5.6), IBM ($\frac{960nm}{960nm}$ (figure 5.7), $\frac{960nm}{480nm}$ (figure 5.8) is shown below.

5.2.3 Device degradation

Noise measured from a CMOS device before and after degradation due to radiation and hot electron injection has been summarized in table 6.2. The change in SNR observed was insignificant both for the radiation and hot electron injection (figure 5.9).

5.3 Noise Simulations

We used IBM 130 nm PDK to simulate the noise in transistors in Cadence. The simulation results are shown in the figure 5.10. The SNR trend is as expected. The simulation results for very low gate voltages showed a zero noise. This was not in conformation with our experimental results. The reported gain in simulation are higher then we measured experimentally. The reason is models are approximations

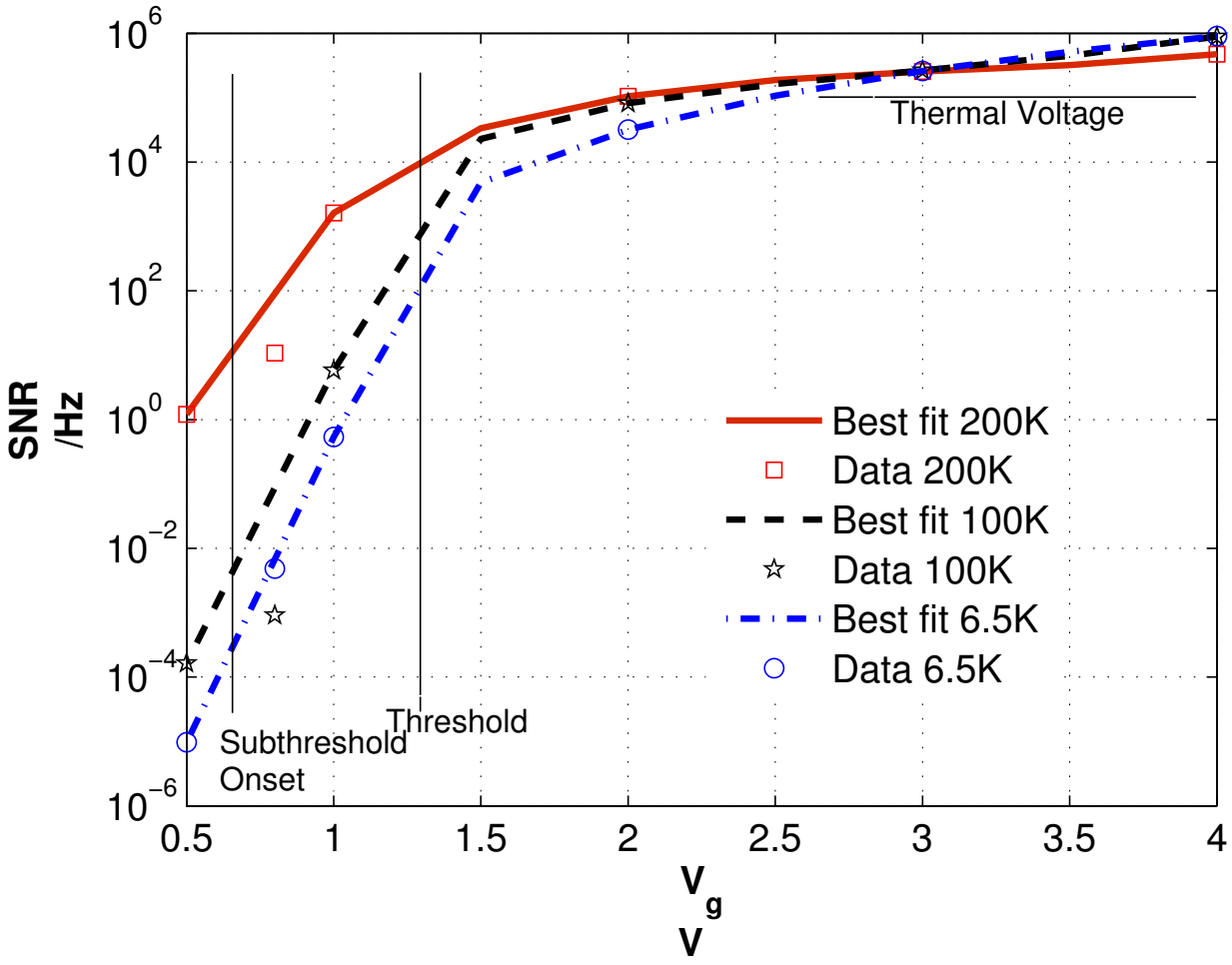


Figure 5.6: Variation of SNR with gate voltage at various temperatures for 0.5uC-MOS OnSemi. Device W/L=1. (Single Channel Measurements. 80 averages)

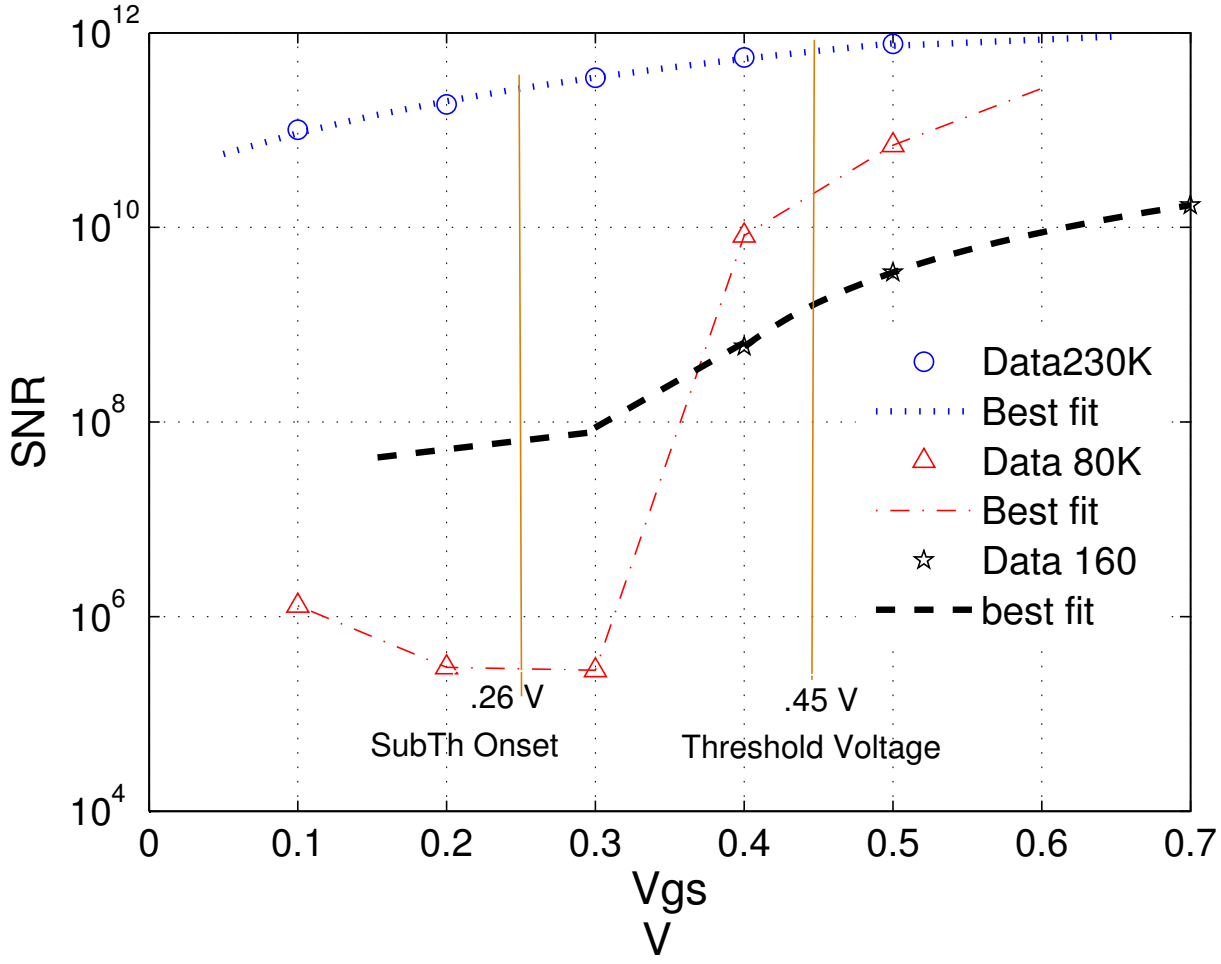


Figure 5.7: Variation of SNR with gate voltage at various temperatures (230K, 160K and 80K) for 130 nm IBM process. Device W/L=.96μm/.96μm. (Double Channel measurements. 10 averages.)

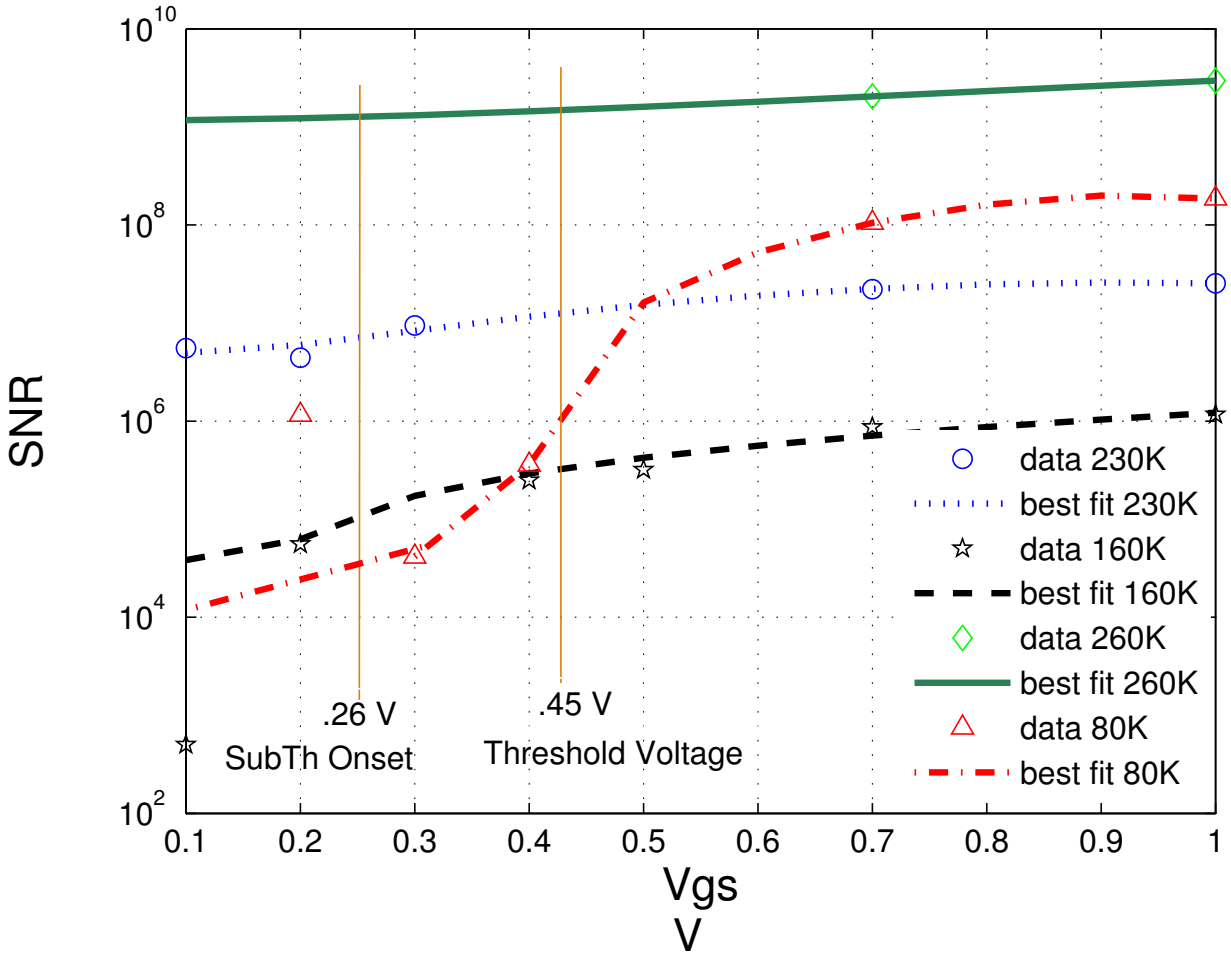


Figure 5.8: Variation of SNR with gate voltage at various temperatures (230K, 160K and 80K) for 130 nm IBM process. Device W/L=.96μm/.48μm. (Double Channel measurements. 10 averages.)

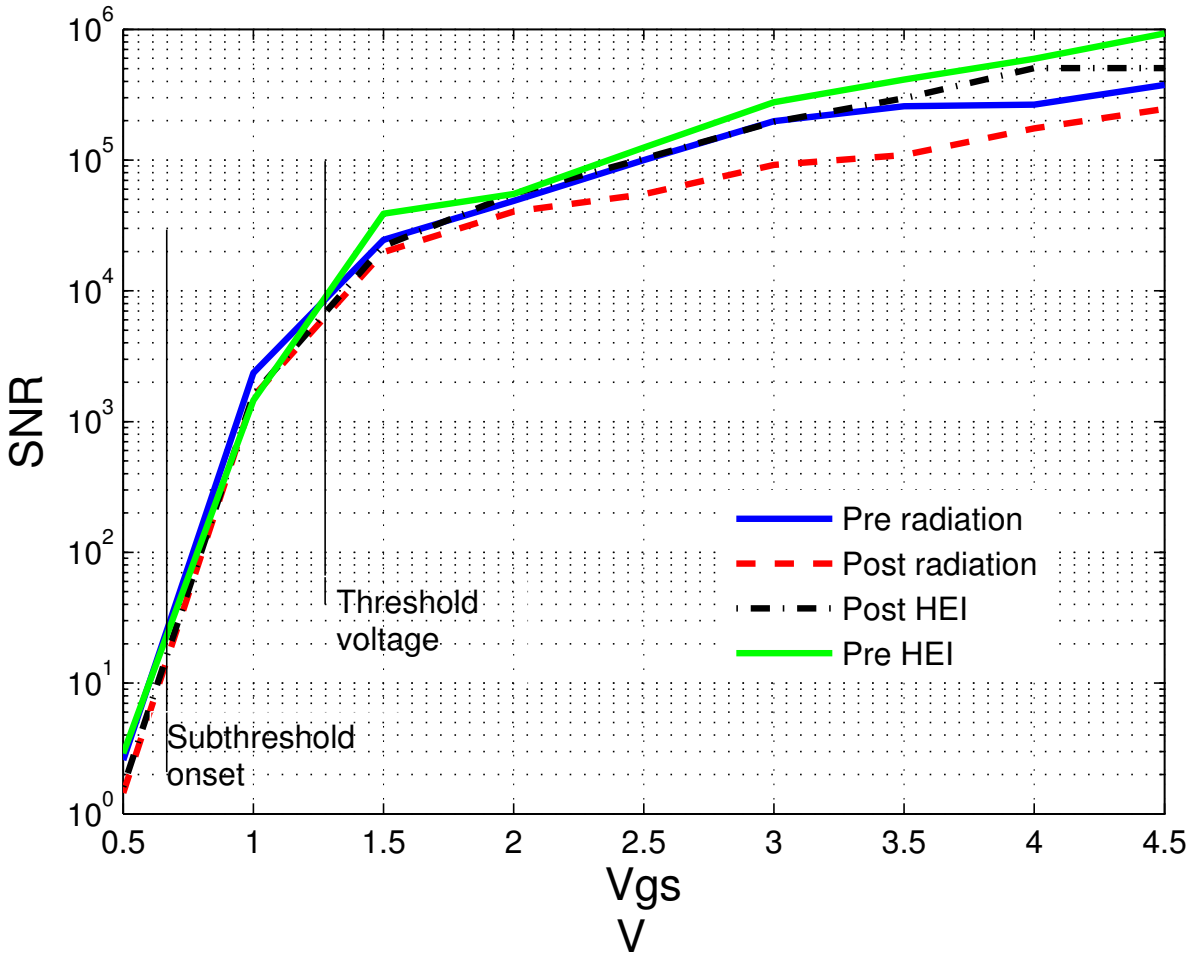


Figure 5.9: Variation of SNR with gate voltage before and after being treated with radiation and HEI. 0.5 μmCMOS process. Device W/L=1.

and measurement technique still has limitations in terms of noise.

With this we complete description of our results. In the next chapter, we present discussion and interpretation of the results.

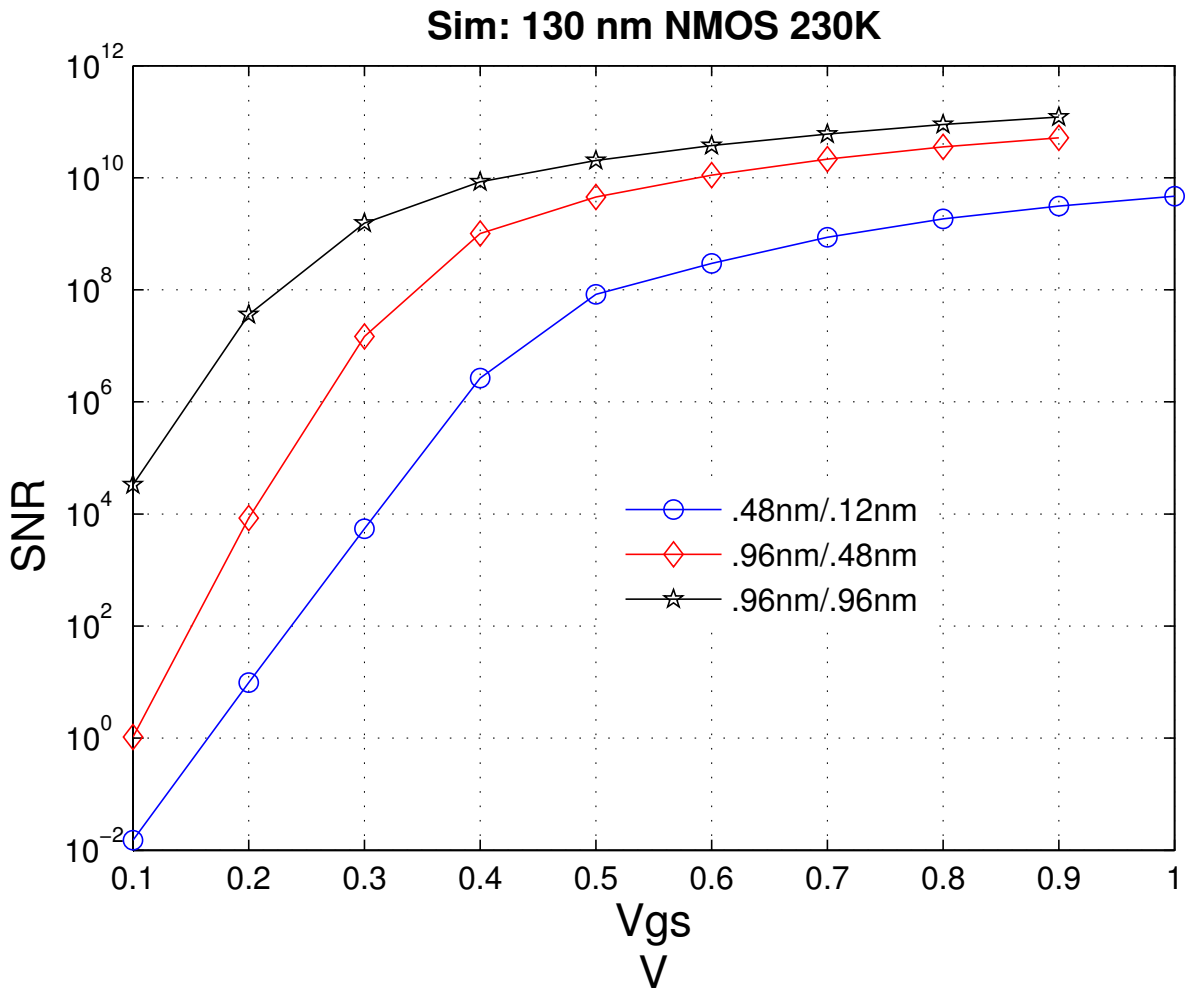


Figure 5.10: Simulation results showing SNR in IBM 130 nm process at T=230K for different W/L ratios. SNR increases with increase in device area. SNR increases with increase in gate biases.

Chapter 6

General Discussion of Transistor-Level Measurement Techniques and Results

In chapter 4 and 5, experimental methods and results for transistor-level noise measurements were presented. As stated earlier, the noise and signal relationship at low frequencies is analyzed with the objective of determining an optimal bias point with highest SNR and lowest possible power dissipation. The results from chapter 5 are compared for different gate biases and for different operating conditions Specifically the impact of various types of stress, (electrical and temperature stresses are presented. In addition,the impact of gate size variation is presented here. The prime goal is to seek a formal methodology for determination of an optimal bias point. Data generated in this thesis is compared to previously published work on flicker noise in subthreshold to saturation region and under different conditions of stress and temperature by various authors.

6.1 Measurement technology

On comparing the two measurement techniques: Double Channel and single channel, we find that the double channel method figure 5.2 provides lower measuring-instrument related gate bias base-line variation as compared to the single channel measurement technique figure 5.1. In low current regions (weak inversion), the

measurement is no longer limited by the 1/f noise floor of the instrument. For higher currents, the instrument thermal noise is cancelled out without the need for taking long-time sample averages.

Earlier work by other authors who investigated the subthreshold region did not measure deep subthreshod region of transistor [14, 38]. Their gate voltage was close to the edge of subthreshold region. Using the double channel measurement technique enabled us to measure the noise in very weak inversion region (figure 5.2) and study the SNR in that region (figure 5.3).

6.2 Experiment vs Simulation

Simulated results from SNR in 130 nm were presented in the first part of chapter 5, the trends followed between the simulated and the measured values of SNR are similar but the measured values of flicker noise is higher than the simulation values. Another discrepancy is that the simulation shows a zero flicker noise at very low gate voltages.

6.3 Optimal Bias

The objective of this dissertation is to thoroughly investigate the behavior of noise under all regions of gate bias and find a bias point for transistor operation such that the signal to noise ratio is the lowest with lowest power consumption. Prior research and literature does not provide a comprehensive way to bias the transistors processing low frequency noise. Though some literature suggests biasing

in subthreshold regime, there is no study of signal, noise and power variation with gate bias to suggest a best operating regime. There has been a trend towards reduction of power by biasing the circuits in region of very low currents [20, 44]. Researchers investigating low frequency domain also suggest subthreshold region.

Based on data supplied by Enz and Nemirovsky, it would appear that operating the circuits in subthreshold regime is optimal, as the input referred flicker noise is the lowest [20, 44], [38, 59]. We agree that the flicker noise, S_{I_d}, is lowest in subthreshold region and decreases as the gate bias is reduced and currents reduce. It should also concern a circuit designer that in-spite of lucrative advantages of subthreshold namely low power and low noise, the signal strength also reduces. Hence, we have plotted SNR of the transistor under various gate bias and studied the noise trend. Below we discuss the SNR results under various conditions of stress (radiation and hot electron), dimensions and temperature variation.

6.3.1 SNR

SNR vs gate voltage for 0.5 μ On Semi (figure 5.3) shows an increase in SNR with gate voltage. The increase is steeper in subthreshold region and flattens out at higher gate voltages. The curve attains a maximum as the device moves out of weak inversion region to moderate inversion region and remains more or less constant in the strong inversion region. In other words, the maximum increase in SNR with increase in gate voltage is obtained in the subthreshold region. Further increase in gate voltage results in a small gain of SNR. Similar trends are observed for 130 nm

process as discussed below.

6.3.1.1 SNR variation with device size

SNR for devices $\frac{960nm}{960nm}$, $\frac{960nm}{480nm}$, $\frac{480nm}{120nm}$ are plotted. The trend indicates an increase in SNR with device area. This is in conformation with literature which indicates a decrease in flicker noise with increase in gate area. Table 6.1 shows the current density for all the devices [12, 47, 53].

Table 6.1: Device Noise dependence on current density. A=$960nm^2$

Parameter & Devices	480nm/120nm	960nm/960nm	960nm/960nm
Gate Area	A/16	A/2	A
W/L	4	2	1
Current density	64/A	4/A	1/A

The SNR trend followed is similar in spite of the change in device dimensions.

6.3.1.2 Temperature

Study of the variation of SNR (and optimal bias point) with temperature variation is required for determining the reliability of a circuit when operated under conditions of low temperature (sub zero environment) or very low temperatures like space applications [5, 40, 75]. It is understood that making such measurements is a challenge. Work reporting flicker noise at very low temperature have not reported

any conclusive trend of noise variation. A group at UCLA studied noise at different temperatures for voltages ranging from subthreshold to saturation region [14]. Their results did not show any consistent trend in the variation of input referred noise. Another major pitfall of their assessment of flicker noise is that is has not been normalized. A study of noise at room temperature and liquid He temperature was done [24]. Another work in which noise in n-silicon MOSFET was studied reported a complex temperature dependent trend in flicker noise measurement [46]. In another study of silicon-nanowires, low temperature (100K) flicker noise has been attributed to number fluctuation whereas the a combination of number fluctuation and mobility fluctuation is believed to be responsible for noise at higher temperatures [63]. Our experimental results for both 0.5μ On Semi and 130 nm IBM process are discussed below.

On Semi: On semi 0.5μm NMOS transistor was operated at room temperature, 200K, 100K, and 6.5K. Variation of SNR in On Semi process is shown in (figure. 5.6). SNR deteriorates in weak and moderate inversion as the temperature of the chip is reduced. This reduction can be attributed to decrease in subthreshold current with fall in temperature. Hence SNR (200K) > SNR(100K) > SNR (6.5K).

IBM: Figure 5.7 and figure 5.8 show the SNR variation in 130 nm NMOS transistors with $\frac{W}{L} = \frac{960nm}{960nm} and \frac{960nm}{480nm}$ respectively. Data at 230 K and 160 K show expected trend (SNR (230K) > SNR(160K)). At 80K the transistor remains in its off state throughout the subthreshold region. The strong temperature dependence of the diffusion dominated subthreshold transport is far from sufficient to saturate traps, coupling to the traps is strong and we see (essentially) no signal. But SNR

increases after gate voltage crosses gate bias voltage necessary for turn-on. This explains the strange behavior of the 80K curves. When the device is not conducting, little current flows and fluctuations are strong.

From the above plots it would be correct to generalize that the SNR increases with increase in temperature of the device. The SNR increases with increase in gate bias voltage as indicated in the simulations. The above trends from experimental data agrees with the trend observed in silicon nanowire as well [63]. Besides, two different system for the two different CMOS processes were studied. Results of both the studies point toward a similar trend.

6.3.1.3 Stress

Prior studies of the magnitude of radiation induced flicker noise have appeared in the literature [2, 35, 22]. The mechanism of transistor damage is well understood and characterized [77, 52, 64]. A decrease in subthreshold voltage and increase in current is observed. There is also an increase in the slope of the noise vs gate bias curve. Data for SNR change when the 0.5μ On Semi process devices are exposed to γ-radiation and hot electron injection is show in the figure 5.9 below. There is only a slight decrease in the SNR in the saturation region of operation. Table 6.2 summarizes the effect of stress on device trap levels. An increase in slope of flicker noise due to radiation indicates introduction of traps with higher time constant. A detailed analysis of trap density using indicates an increase in oxide traps and negligible increase in interface traps [51].

Table 6.2: Effect of radiation and hot electron injection

Parameter	Radiation	Hot Electron Injection
Threshold voltage shift	0.06 V	None
SNR	No significant change	No significant change
Noise slope	Increases	No change
Trap Density	ΔN_{ot}=$11x10^{10}$ $/cm^2$; ΔN_{it}=negligible	None

According to Reimbold equation 2.24, the value if I_D^2/S_{I_d} is given by [66]:

$$\frac{I_D^2}{S_{I_d}} = \frac{f^\beta}{K}\frac{\beta^2 Q_n}{N_t} \tag{6.1}$$

Radiation data shown in figure 5.9 conforms with the result. SNR, $\frac{I_D^2}{S_{I_d}}$, shows a slight dip for the radiation data indicating an increase in trap density N_t after radiation.

6.4 Result Summary

In this chapter, we studied the variation of SNR for different transistors with change in gate voltage bias. The table 6.3 summarizes the experiment and conclusion drawn from them. All transistors are NMOS. Operating the transistor under various operating conditions supports our conclusion about selection of a stable bias point.

6.4.1 Bias Methodology

From the graphs, it is clear to us that at very low gate voltages, the signal to noise ratio is very small. As the gate voltage is increased, the ratio increases rapidly till the device moves into moderate inversion region. From moderate inversion to strong inversion, the signal to noise ratio increases by a small amount. Power consumption will increase linearly with gate voltage. Another parameter that a circuit designer is interested in maximizing is dynamic range. Dynamic range increases with drain current. We define an **optimal biasing point** as a point where the minimal power and maximum SNR and dynamic range is achieved. This point is defined as weighted function of 'SNR', 'Power' and 'Dynamic Range'. This optimization function is defined below. The weighting is chosen by the designer based on power constraints.

$$OPT = a * SNR + b * Power + c * DynamicRange \tag{6.2}$$

where, 'a', 'b' and 'c' are the weights. 'a' and 'c' are unit-less positive constant and 'b' is a negative constant with units'1/W'.

For the transistor example (ref. figure 5.2), power and SNR are plotted in figure 6.1. Here we want to select an optimal bias point to maximize SNR and minimize power consumption. Dynamic range is weighted low and for this example it is considered as not a critical parameter. We selected 'a' as 1 and 'b' as -10^{15} based on range of SNR and power values. The optimization function is plotted in figure 6.2. Maximum point in the weighted function is obtained for $V_g = 1.4$ V.

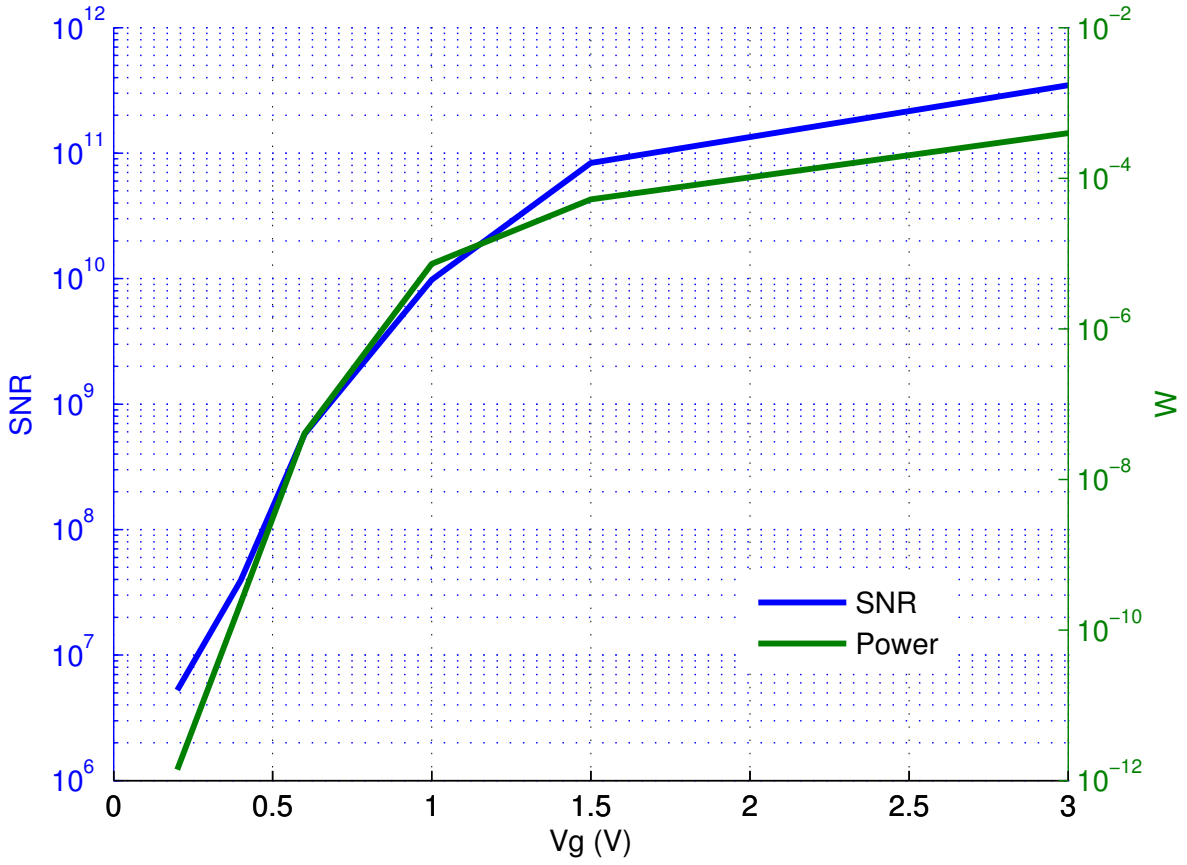


Figure 6.1: Power and SNR for On Semi 0.5 μ NMOS transistor. SNR and power both being a function of I_d, increase with increase in gate bias voltage. Interest in selecting a bias point that maximizes SNR and minimizes power.

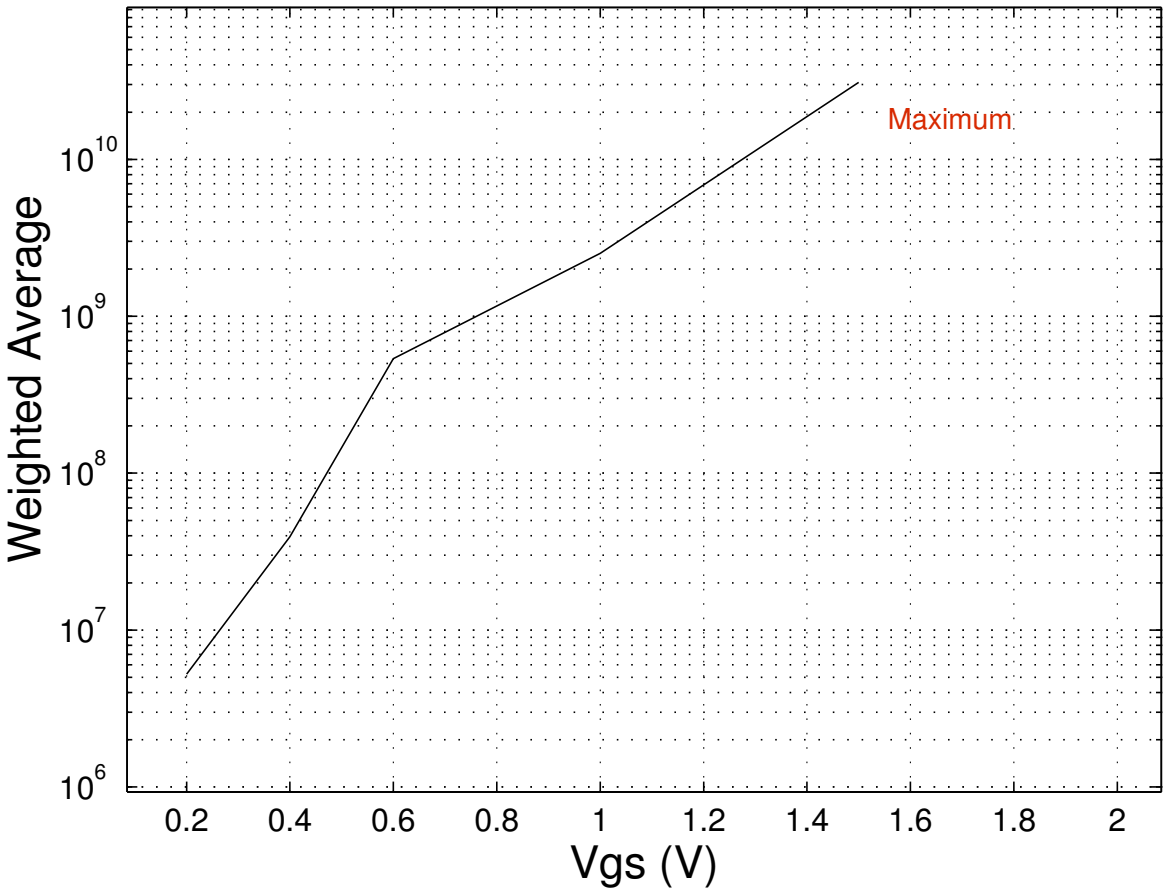


Figure 6.2: Optimizing Power and SNR. Optimal function plotted for On Semi 0.5 μ NMOS transistor. W=L=3.5 μ. The function increases, reaches a maximum at V_g=1.4 V and then drops to very low values for $V_g > 1.4$ V.

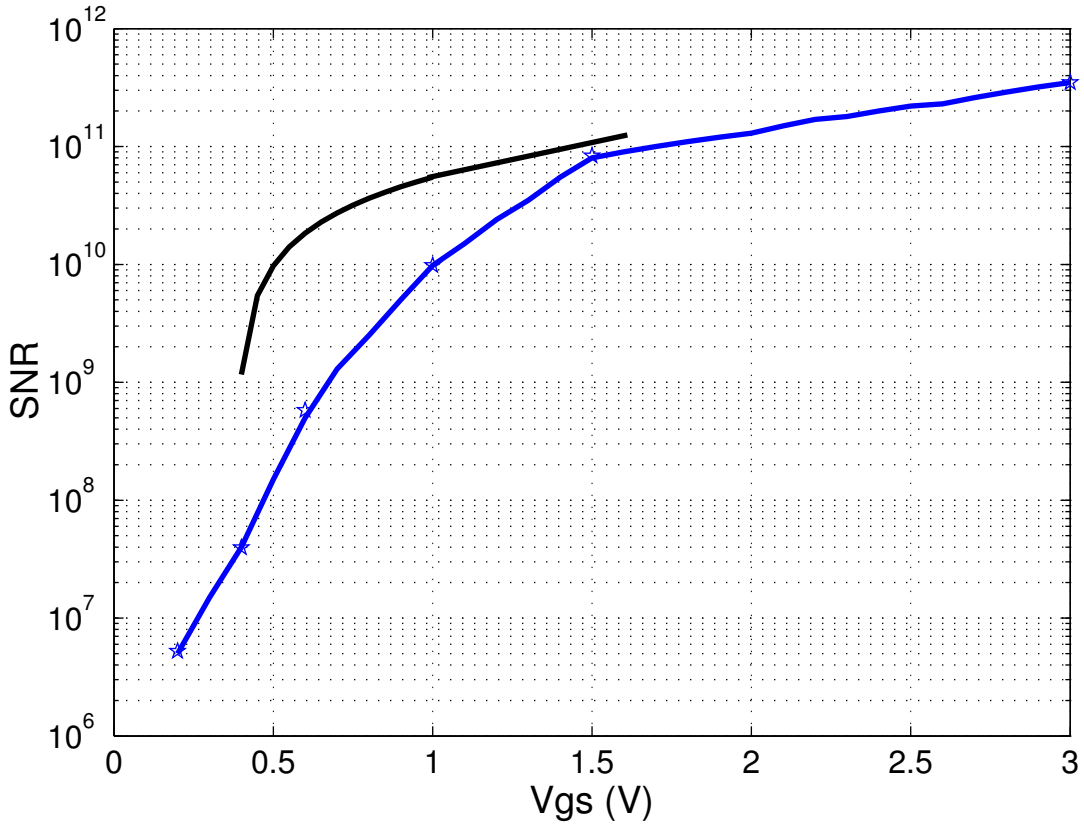


Figure 6.3: Blue curve shows the SNR and black curve shows the slope (0.5 uCMOS OnSemi). Slope increases and then starts to decrease. The point where slope change decreases and becomes gradual is point of maximum inflection. After this point the change in SNR is smaller. Recommended biasing region lies around the region of maximum change .i.e is in subthreshold region.

Another biasing strategy based on only SNR is shown in figure 6.3.

We can explain above two optimization functions as follows: *above threshold region, the increase in SNR is not significant in comparison to increase in power; we trade off small increase in SNR for minimizing power consumption. Therefore, edge of threshold region before the onset of moderate inversion is the most optimal bias point.*

6.4.2 First Order Saturation model

Revisiting the first order saturation model explained in chapter 3, we see that the initial SNR is low but it increases steadily after inversion layer saturates the trap density (figure 3.1). Increase in SNR after moderate inversion, depends only on the increase of current. For low power design, region just before onset of threshold voltage is most appropriate: noise is not minimal but signal to noise ratio is significantly improved.

6.4.3 A note about trap distribution

The slope of the flicker noise ($1/f^{\beta}$) curves has been used to estimate the trap distribution in the oxide in a device. This model depends on dependence of time constant τ on the trap's distance from the channel oxide interface. Based on McWhorter theory, a perfect 1/f slope is achieved for uniform distribution of traps N_{ot} [74]. As explained by Van derZeil in the classical derivation, when noise density is integrated over bandwidth f_1 to f_2, any change in trap distribution,N_{ot},

will change the slope of the 1/f noise. Slope (β) greater (or less) than 1 points out towards higher number of slow traps (or fast traps). This has been used to extract information about trap distribution in different processes [29]. From the flicker noise slope $\beta > 1$ we can conclude that 0.5μ CMOS process (figure 5.2) has a higher number of slow traps than fast traps. This suggests presence of higher number of oxide traps than boundary traps. For 130 nm IBM process the $1/f^{\beta}$ slope ($\beta = 1$) indicates a uniform distribution of traps in the gate oxide.

6.5 Significance of this Study

Though optimizing SNR and minimizing power is not a new problem. This problem has been addressed by researchers earlier [20]. In our study we have focused on low frequency noise as behavior of low frequency noise is different from thermal noise and prior published studies do-not emphasize on this aspect for low frequency domain. From this study we want to stress on the fact that 'low noise' does not always imply best region of operation. Though recent circuit design trends focus on low power design, they are more prone to noise especially for audio processing and bio-medical signal processing applications.

This study on transistors also shows that temperature drop, radiation stress and gate size reduction causes a drop in over all SNR. But, the overall behavior is SNR and point of inflection of curve does not change. SNR curve flattens for regions above threshold voltage.

Table 6.3: Summary of Experiment and Results

Process	W/L	Study	SNR
0.5μ OnSemi	3.5μ/3.5μ	Gate bias variation	SNR increases and saturates
0.5μ OnSemi	3.5μ/3.5μ	Effect of γ-radiation	Small change in SNR
0.5μ OnSemi	3.5μ/3.5μ	Effect of HEI	Insignificant change in SNR
0.5μ OnSemi	3.5μ/3.5μ	Decrease of temperature	SNR decreases
0.5μ OnSemi	3.5μ/3.5μ	Effect of HEI	Insignificant change in SNR
130nm IBM	Various	Variation of gate bias	Increases
130nm IBM	$\frac{.96}{.96}$, $\frac{.96}{.48}$, $\frac{.48}{.12}$	Increase of gate area	Decreases
130nm IBM	Various	Decrease of temperature	Decreases

Table 6.4: Summary of Flicker Noise Dependence

Study	Literature	Our study vs Lit.	Conclusion:SNR
Device area (A)	$S_{I_d} \downarrow$ as Area↑ [3, 47, 53]	Agreement	SNR↑ as Area↑
Temperature (T)	No trend (MOSFET) [63, 14, 46]	SNR ↑ T(>80K)↑	more complex
Radiation	S_{I_d} increases	In agreement	SNR decreases

Chapter 7

A Circuit Example

In previous chapters we addressed the issue of noise and optimal biasing for individual transistors in two different processes and under various conditions of operation. Our objective is to improve performance of circuits operating in low frequency regime by finding range of optimal biasing point. This chapter provides a discussion of the impact of flicker noise on actual circuit performance at different current biasing levels in a differential amplifier. We find three things:

- SNR generally increases as driving point current increases.
- There is no "maximum" SNR, but rather, the slope of the SNR vs bias current curve decreases with increasing current
- The "upper limit" creating the optimum bias current is set by the safe-operating-bias levels of the transistor, requirements for dynamic range and maximum allowed power

7.1 Noise in Differential Amplifier Front end

As stated above, there has been a trend towards low-power design to satisfy the growing demands of portable devices like PDA, medical sensors, cell phones. Low power design compromise creates a trade-off between speed and dynamic range of

circuits. Reducing supply rail voltage for low power reduces the signal strength and results in performance degradation. In lower power design, output signal strength needs to be considered before considering the biasing currents. Power consumption in analog circuits is therefore dictated by the required SNR [20]. A detailed study of SNR and dynamic range is required to obtain satisfactory performance. The output signal is kept large enough in order to maintain the required SNR, but this sets a limit to circuit power dissipation.

For typical differential amplifier shown in (figure 7.1), main noise contributions come from the MOSFET. Just like single transistors, at low frequencies, flicker noise dominates in amplifiers [30, 26]. For the amplifier (figure 7.1), noise referred to the output is given by the equation 7.2. Once again, we take the flicker noise component of a single transistor as:

$$\frac{K}{C_{ox}WLf} \tag{7.1}$$

In that case, we can write an overall expression for the total amplifier noise:

$$\begin{aligned}\overline{S}_V = (\frac{k_3}{C_{ox}W_3L_3f}g_{m3}^2 + \frac{k_5}{C_{ox}W_5L_5f}g_{m5}^2)(r_{o3}||r_{o5})^2 + \\ \frac{2k_1}{C_{ox}W_1L_1f}g_{m1}^2(r_{o1}||r_{o3})^2(g_{m3}+g_{mb3}+\frac{1}{r_{o3}})^2r_{03}^2\end{aligned} \tag{7.2}$$

7.1.1 SNR

Amplifier SNR can be broadly defined as the output signal over the noise of the amplifier. Output signal of the amplifier depends on the gain of the amplifier. Intrinsic noise of various components determines the total amplifier noise.

For voltage gain 'A' V/V, and input signal v_{in}, the output power is given by

${Av_{in}}^2$. At a low frequency, dominant noise is the flicker noise $S_{v_{1/f}}$. The SNR is given by equation 7.3.

$$SNR = \frac{{Av_{in}}^2}{S_{v_{1/f}}} \tag{7.3}$$

For high frequency region, $S_{v_{1/f}}$ will be the thermal noise. It is apparent that reduction in flicker results in a better gain. Equation 7.2 can be approximated to equation 7.4 as area of tail transistor (M1) is much larger. Gain $A = g_{m3}(r_{o3}||r_{o5})$.

$$\overline{S}_V = (\frac{k_3}{C_{ox}W_3L_3f}g_{m3}^2 + \frac{k_5}{C_{ox}W_5L_5f}g_{m5}^2)(r_{o3}||r_{o5})^2 \tag{7.4}$$

7.1.2 Dynamic Range of an amplifier

Another important circuit parameter that is affected by the noise is the dynamic range. Dynamic range for an amplifier can be defined as the ratio of maximum output voltage to the minimum output voltage [49]. It might seem that the minimum output voltage can be zero and dynamic range will be infinity. But this is not true as the minimum output voltage is determined by the system parameters of the circuit. The dynamic range for an amplifier is given by equation 7.5.

$$DR = 20log_{10}\frac{V_{out}(max)}{V_{out}(min)} \tag{7.5}$$

$V_{out}(max)$ is the maximum output voltage before the one of the transistors moves out of saturation region and $V_{out}(min)$ is the minimum output voltage given by the error and noise at the output when input signal is set to zero. $V_{out}(min)$ consists of

internal and external noise and amplifier offsets. Dynamic range can be improved by reducing the intrinsic noise and errors of the amplifier. Another point to be noted is that at higher bias currents dynamic range of the amplifier decreases due to higher voltage drop at the load.

7.2 Simulations

A differential amplifier was simulated using Cadence and IBM 130 nm BSIM models. The schematic is shown in the figure 7.1. Current biasing was provided to the circuit using a 1:1 current mirror. The single ended output voltage at the drain of the input transistors was studied. As described in work done on single transistors, the biasing of the transistor would affect the low frequency noise at the output. The circuit was operated at a supply of 1.2 V and bias current varied. A zero differential input voltage was provided. The output noise is given in the figure 7.2 and 7.3.

7.3 Amplifier Test Data

Diff-amp fabricated in 0.5 μmCMOS On Semi process was biased at different currents by changing the bias voltage of the tail amplifier (Vdd= 5 V). Noise was measured directly using signal analyzer (SR 770 FFT analyzer, courtesy: Dept. of Physics) at node 'vout'. SNR was computed from the flicker noise at the output node for different bias voltages of the bias amplifier (figure 7.6). The plot of SNR vs gate voltage shows that the SNR increases with bias current.

The optimal point of operation To determine the optimal bias point, we

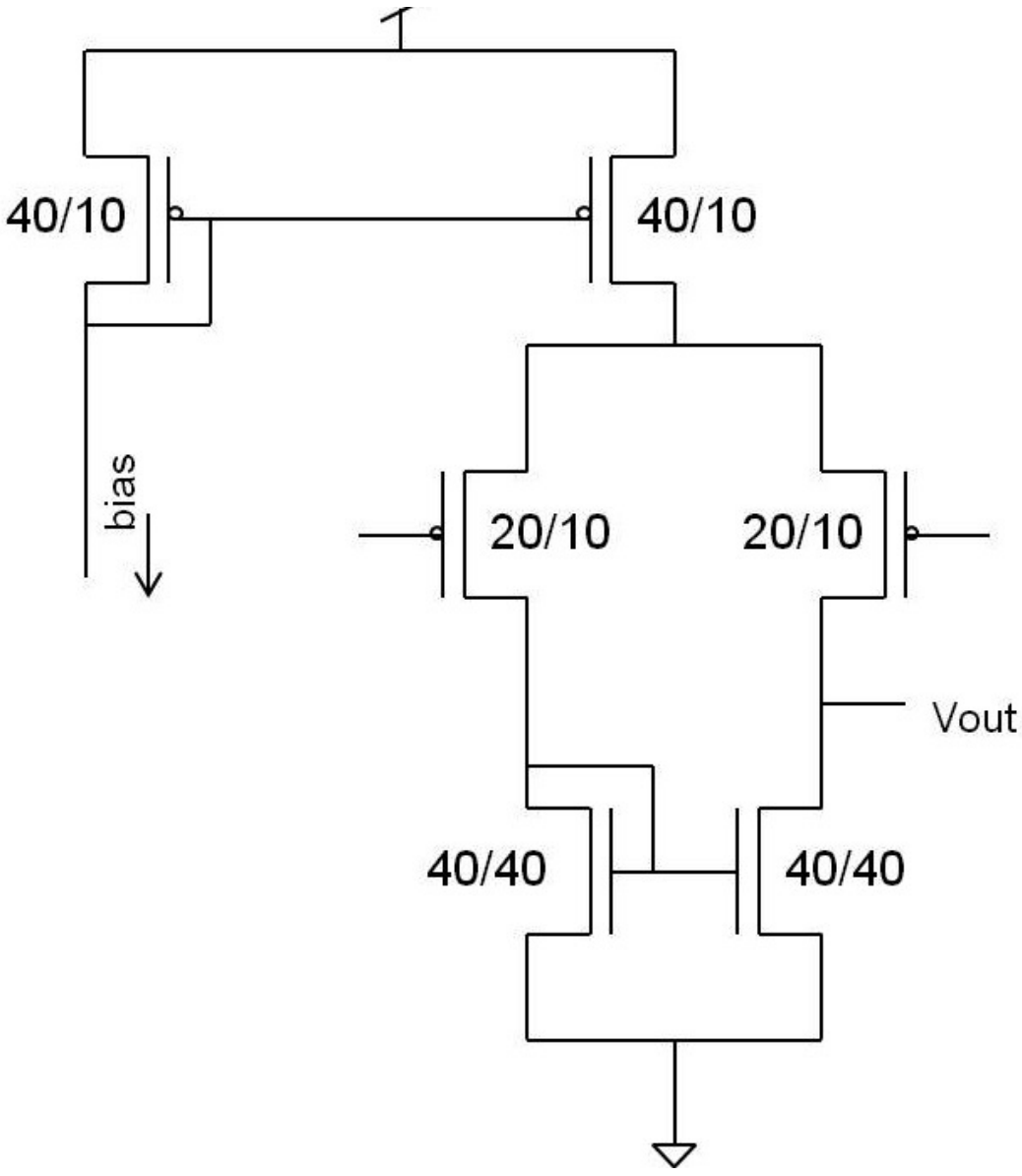


Figure 7.1: Schematic of differential amplifier used for experiments in 0.5 uCMOS.

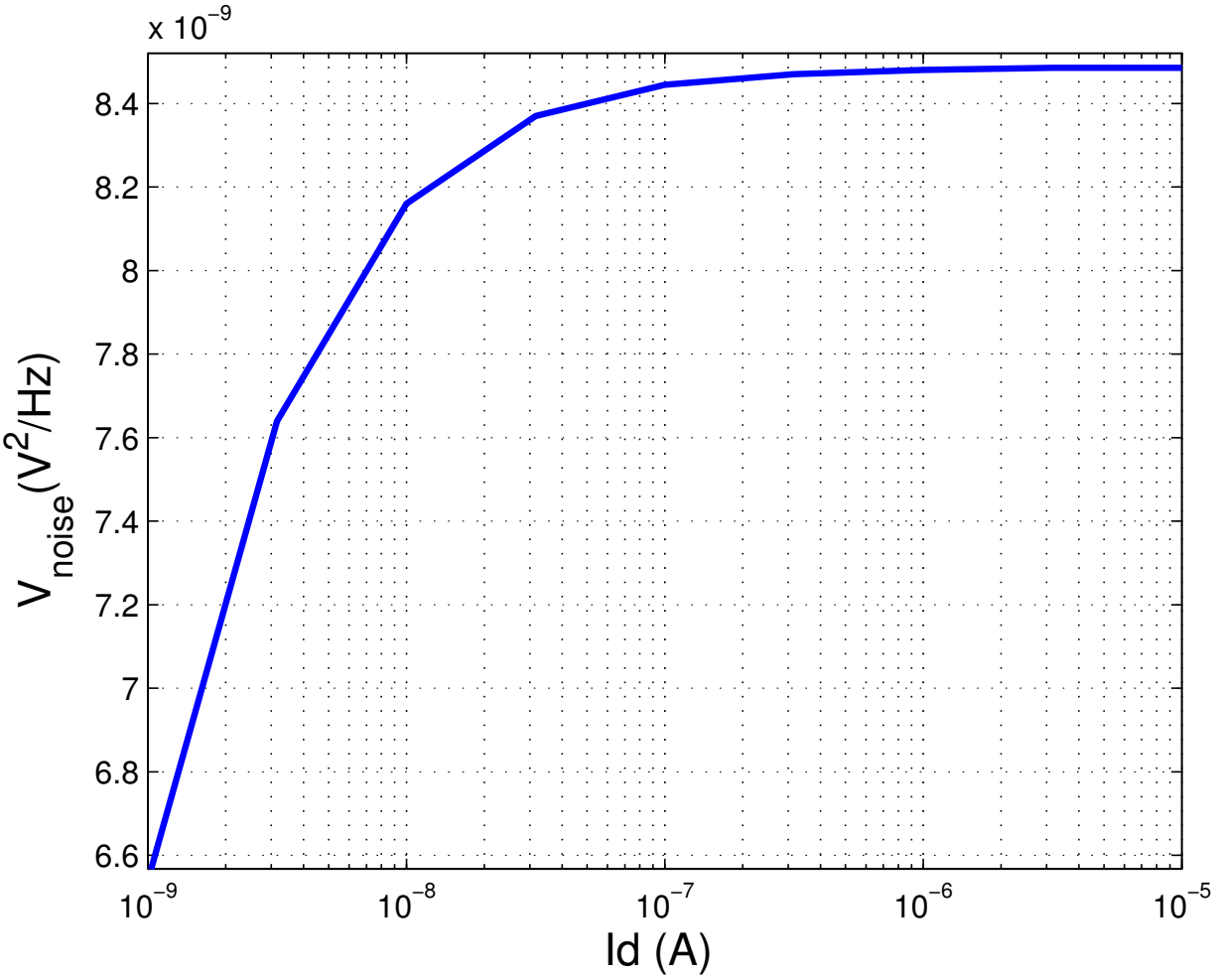


Figure 7.2: Simulation (130 nm IBM) results showing variation of voltage noise at output node with change in bias current. The results are plotted for f=100 Hz. 1/f noise increases as the drain current increases.

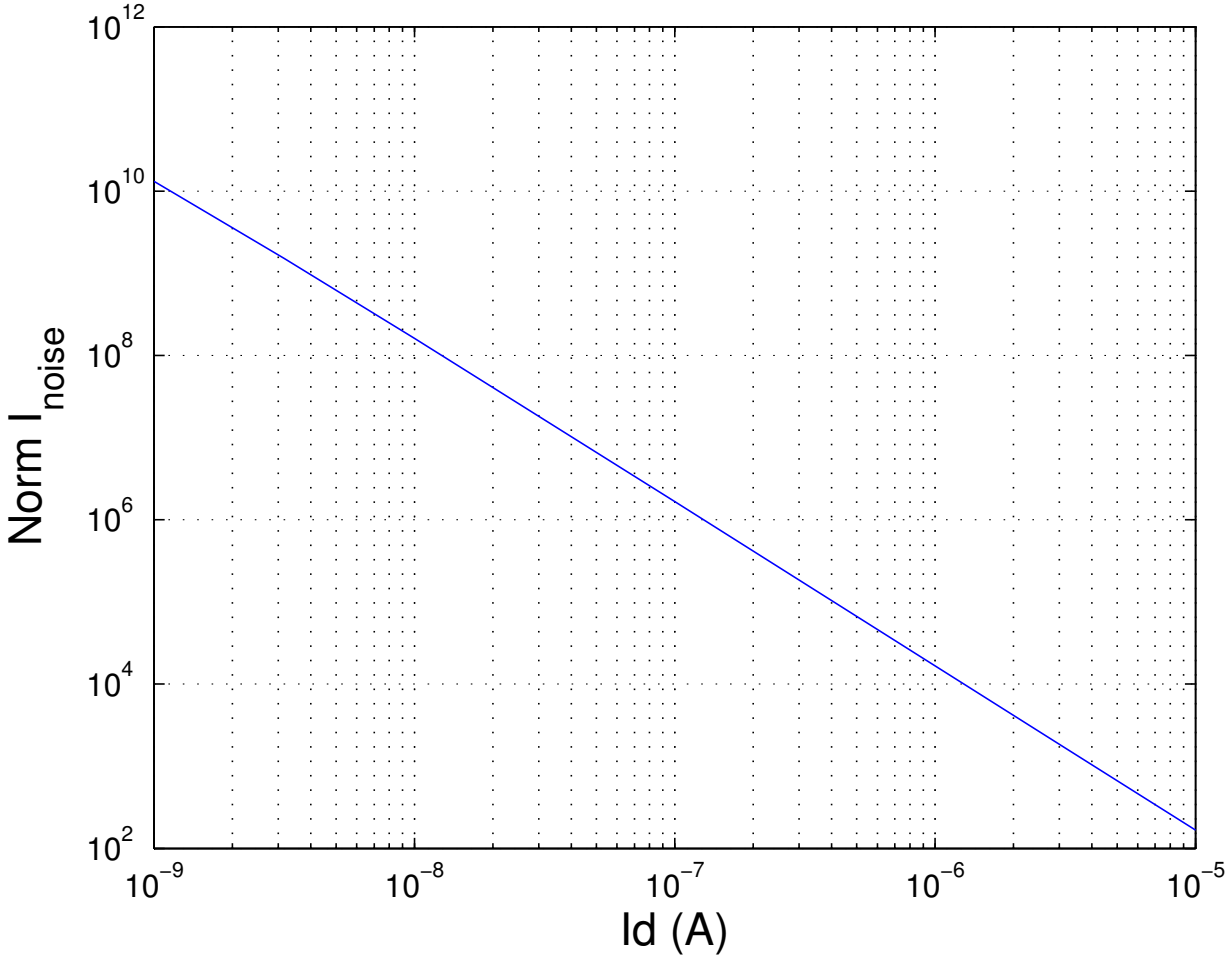


Figure 7.3: Normalized current noise decreases with bias current. Noise directly depends on the bias current. Normalized noise (S_v/I_{bias}^2) decreases with increase in bias current. (130 nm IBM)

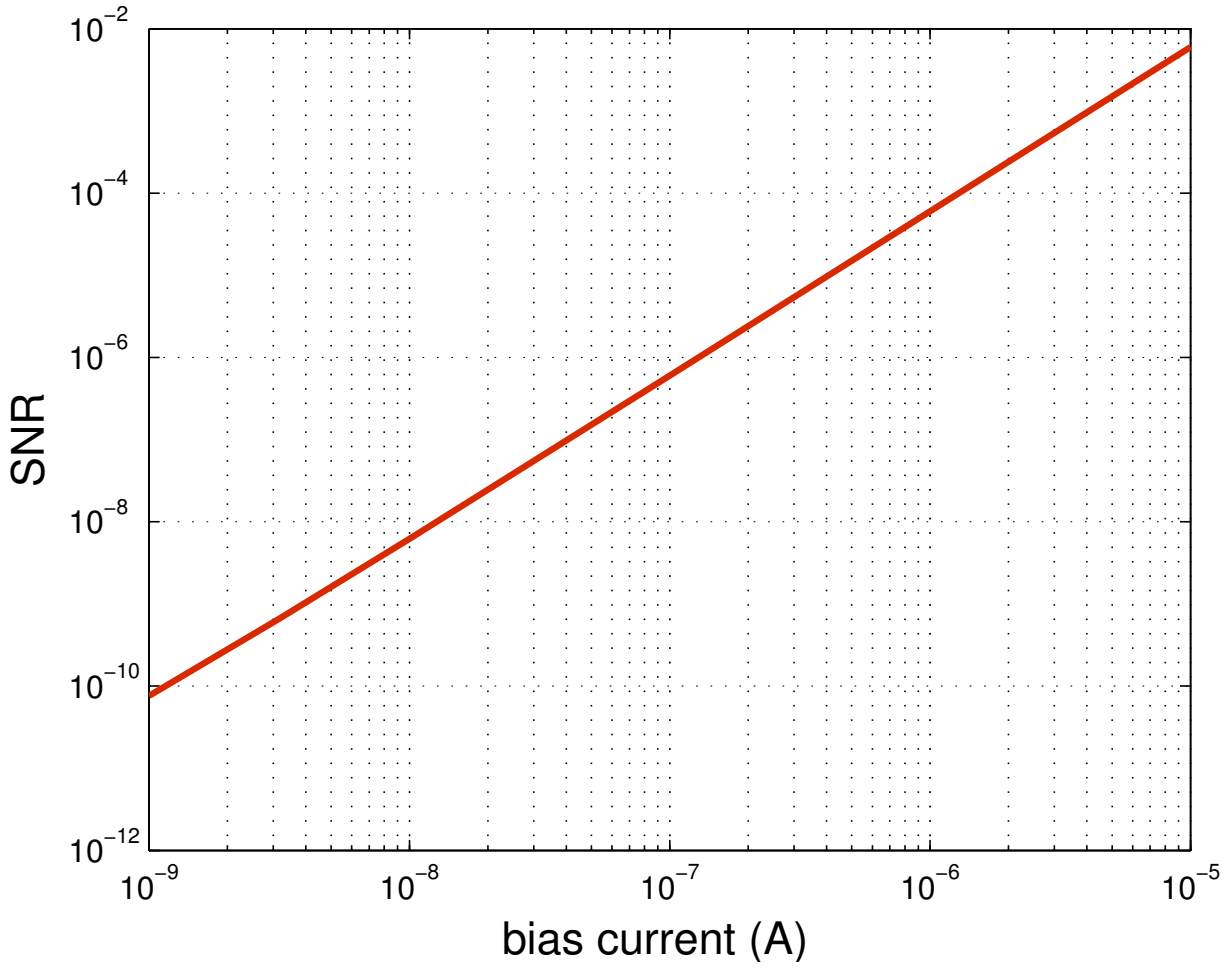


Figure 7.4: SNR (bias current/current flicker noise) variation with bias current. Signal is a function of bias voltage and flicker noise at 100 Hz is the noise. (130 nm IBM)

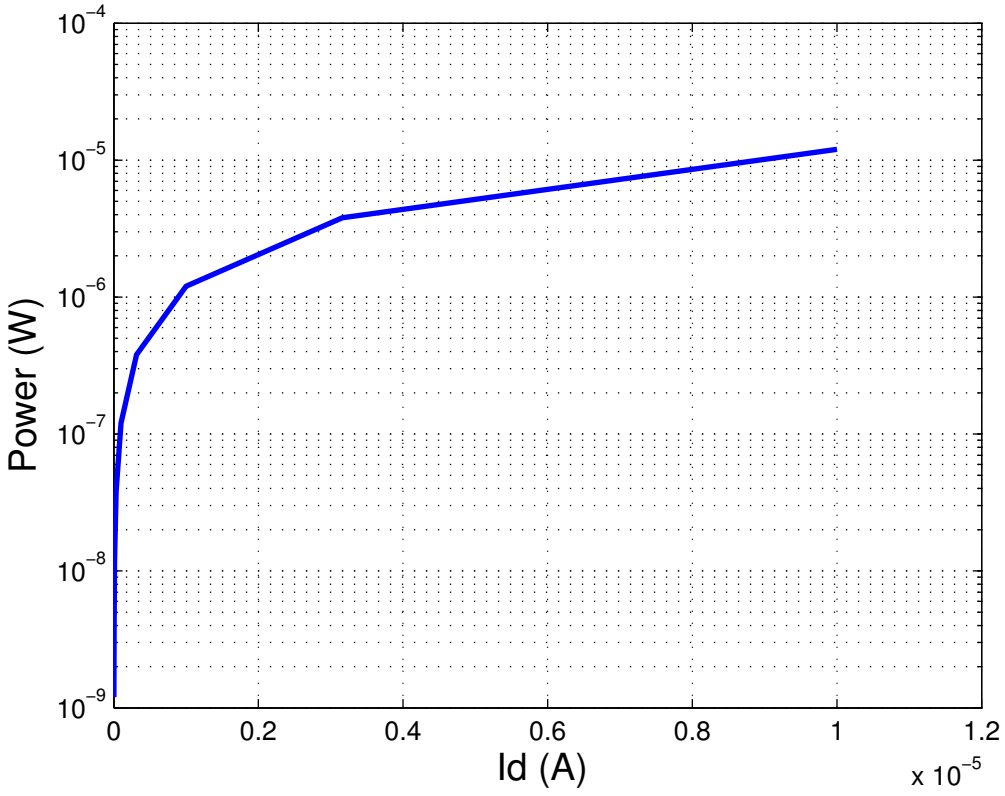


Figure 7.5: Power of the diff-amplifier as a function of bias current. Power increases with increase in bias current. Low power operation is achieved at the expense of SNR.

need to maximize SNR and at the same time, power needs to be minimized or in other words $Power^{-1}$ should be maximized. It is clear from the plot that optimal point of operation is close to the threshold voltage where SNR is high enough and power is low. SNR can be improved at the expense of higher power consumption.

7.4 Discussion

The result shows an increase in SNR with increase in bias current. This an important conclusion. Subthreshold operation of the amplifier degrades the signal even though the noise is low. It is recommended to operate the amplifier at higher currents that bias the transistor in the saturation region. However, at such currents the power consumption is high. The plot figure 7.5 shows the increase in power of the amplifier. The optimal bias point of the transistor can be selected according to the SNR and power requirements of the application. This also indicates that operating the amplifier in saturation will decrease the noise of the transistor.

An optimization routine for this differential amplifier circuit is given by selecting b = $-4 * 10^9$ in the equation 6.2. 'a'=1 and 'c'=0. Plot for this function is shown in figure 7.7. The function decreases as the bias current is increased. The maximum point is obtained for gate bias of 1.1 V and biasing current $0.7 * 10^{-10}$.

7.4.1 Trade offs

To select an optimal bias point one has to trade off between bias current or SNR and power in the low frequency domain. Though the flicker noise $S_v V^2/Hz$

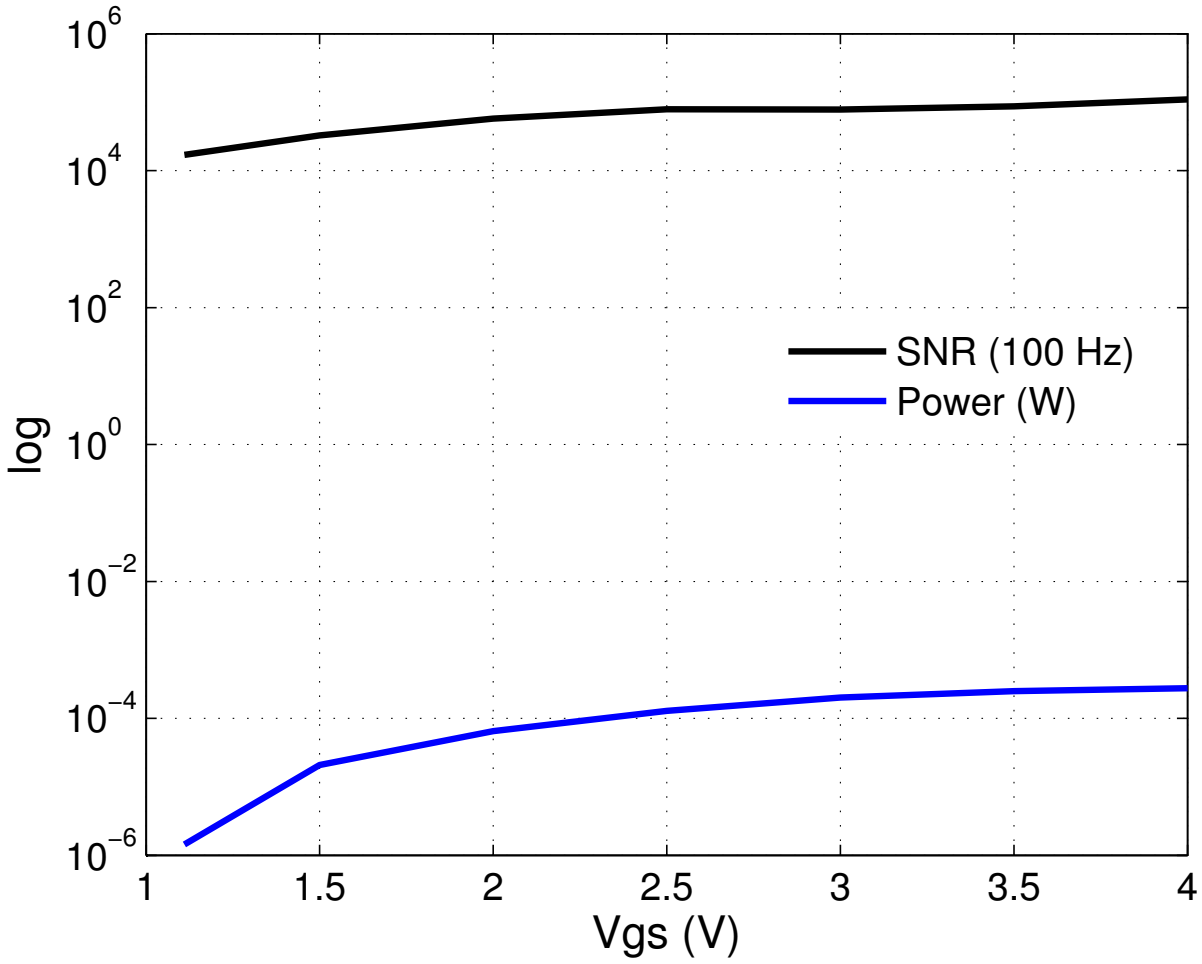


Figure 7.6: Experimental results: SNR and Power for a differential amp as the bias voltage of biasing amplifier is varied. Calculation are made for f=100 Hz. Our objective is to maximize both SNR and minimize Power.

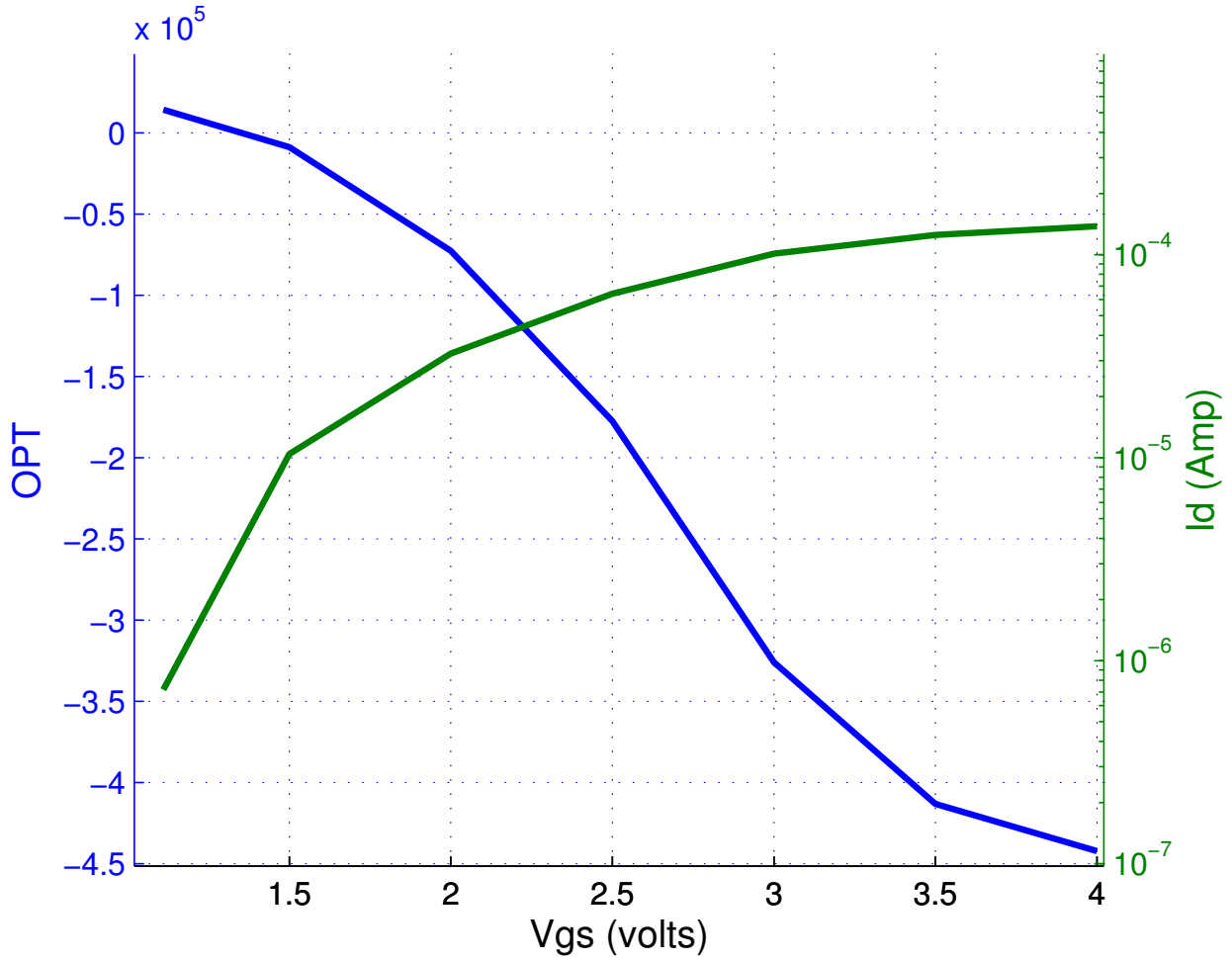


Figure 7.7: Optimal function and bias current for amplifier. Optimization function decreases as bias current increases.

is a function of bias current and its value increases with increase in bias current (assuming the node impedance remains constant), the signal to noise ratio also increases with bias voltage. For low power designs, hence, it is important to select the maximum required SNR as stated earlier by other authors [20].

7.4.2 Subthreshod region

Another important work by Nemirovsky's group analyzes the flicker noise without its relation to the signal [58, 59]. They correctly say that reducing the bias reduces the noise; but, their statement that biasing circuits in subthreshold is best region due to (1) low noise (2) low power is not completely true. Our investigation of behavior of noise and SNR in deep subthreshold region indicates that the SNR decreases in the deep-subthreshold region. We suggest a biasing point depending on noise and power trade-off for circuits.

7.4.3 A low noise mixer

Our results as shown in the figure 7.4 are in agreement with other reported techniques. One of the applications increasing the bias current to reduce the flicker noise has been discussed in the patent [13]. In this mixer circuit, a DC current is introduced in the RF transistors to reduce the flicker noise caused by the RF transistors without overloading the local oscillator drive requirements.

We can conclude that for low power low frequency circuits like amplifier, an optimal bias point can be selected which operates the circuit at the edge of sub-

threshold region without compromising the performance (i.e. SNR) and without consuming too much power. Higher SNR can be achieved to some degree at the expense of power consumption.

Chapter 8

Conclusion and Contributions

This work presented theory and data for finding an optimal bias point with substantial signal to noise ratio and low power consumption for the CMOS design in general. In course of the study we also completed an extensive study of flicker noise from deep subthreshold to strong inversion in On Semi 0.5μ CMOS and 130 nm IBM process. We probed into deep subthreshold region to find answer to our question, such extensive study has not been done before. Further, effect of temperature and stress was evaluated on flicker noise and selection made for optimal bias point.

8.1 Optimal Bias: Study Summary

The motivation behind the work is to address the circuit design problem of finding an optimal biasing for circuits operating in low frequencies (LF) ($<$ few kHz). Biasing strategy for such circuits has not been addressed and circuit designers usually bias the circuits where the low frequency flicker noise is minimum [58]. One of the short comings of this approach is that it focuses only on minimizing noise and does not take signal strength into consideration. In this work, we have focused on studying the variation of LF noise and LF SNR for transistors for different regions of transistor operation; and extended it to circuit level design. Our biasing strategy focuses on measuring flicker noise under different gate bias voltages, calculating SNR

and comparing the power dissipation for different bias voltages. SNR and power consumption are the two most important design criterion [20]. We know that at low gate biases, flicker noise is small, but we are also aware that the signal strength at low gate bias is also very weak. Finding optimal bias point would maximize SNR and minimize power dissipation.

The motivation behind finding the optimal biasing strategy is based on the fact that as inversion charge increases, the signal to noise ratio in the channel increases (for low frequency domain). The flicker noise is the dominant noise in low frequency region. This noise also increases in magnitude with increase in inversion charge density. It is depends on the trapping and de-trapping rate and the trap density. Flicker noise increases with increase in inversion charge [50] but it eventually converges to a constant value given by $\sqrt{c_1 N_t}$ at very high inversion charges (figure 3.1(b)). This is the result of the saturation effect described above. Signal strength is dependent on inversion charge and it can be concluded that at very high inversion charge (if no other noise dominates), the SNR increases with signal. This model gives us a good understanding that at higher inversion charge in the channel, SNR improves.

The experiment and results support the above theory and show that the SNR, signal (Id^2) to noise ratio S_{I_d} ratio increase as the gate bias is increased (or inversion charge increased). The SNR increase in weak inversion region is larger and at higher gate biases is much gradual. We use weighted equation for SNR, power and dynamic range to determine a maximum biasing point (equation **??**). Maximum gain in SNR is seen before moderate inversion is reached. For maximizing SNR and minimizing

power dissipation, we conclude that biasing the transistor in subthreshold region close to threshold voltage is optimum. Biasing transistors in strong inversion region would give slightly higher SNR but at the expense of higher power consumption.

In order to generalize our biasing strategy, we studied the flicker noise behavior and SNR in different processes: On Semi and IBM. We further extended the study to different device dimensions. The study conformed with earlier published works on flicker noise and sowed that SNR variation follows similar behavior with change in gate bias voltage. Reliability of circuit design is another concern for a circuit designer. Circuits are regularly operated under varying temperatures for space application etc. and under effects of stress for various nuclear laboratories and hospitals. We studied the reliability of approach under the above conditions. It was found that SNR follows similar trend under conditions of low environmental temperature and stress. Hence, our biasing strategy is not affected by adverse environmental conditions.

We showed that our biasing strategy can be applied to circuits as well. Same trends were shown using simulations for integrated circuits which gives us a analog design methodology for circuits processing signals in the range of <1 kHz. Another example of a circuit was presented where flicker noise was reduced by increasing the signal strength.

In summary, this work analyzed and presented a detailed and complete analysis of noise behavior in low frequency domain. As mentioned in previous chapters, authors who have tried to address this topic of flicker noise and subthreshold regime of circuit operation have only looked at the noise behavior. Whereas we, analyzed

the problem in totality and can confidently say that our results indicate that subthreshold regime does not necessarily mean best region of operation. Keeping in mind both noise and power, regions close to threshold voltage provide optimal gate biasing.

8.2 Frequency characterization in Deep-subhreshold region

Characterization in deep subthreshold region was limited due to instrumentation noise. But this challenge has been overcome as discussed earlier. Using this break through in measurement technology, we could analyze the behavior of noise under very weak inversion regions. This region is also being explored by circuit designer who are operating circuits with currents below nano-ampere range. Hence, this region of very weak inversion is of interest to many. Our analysis of SNR in this region can help circuit designer to improve circuit technology.

Further, to have a better understanding of noise phenomenon, we have completed low temperature noise spectroscopy. This sheds some light on low temperature behavior of flicker noise.

8.3 Summary: Contributions

We summarize the main contribution of this work below:

1. Development of a "Trap occupancy saturation model"' explaining the observed behavior of 1/f noise CMOS channel as a function of channel current. We study the change in noise behavior for CMOS transistor operating in condi-

tions conducive to device degradation and explain it using the trap occupancy model.

2. Development of an analog design methodology utilizing this saturation effect to improve system SNR through bias optimization. The optimization described traces noise behavior in the MOS channel from deep sub-threshold to strong saturation in a 0.5 μ CMOS process.

3. Low temperature noise spectroscopy is carried out to comprehensively study the noise behavior at low temperatures in a 0.5 μ CMOS process and a 130 nm CMOS process. Double channel method enabled us to probe deep into subthreshold region where noise behavior was not studied before.

We summarize the most important conclusions of the work is we can device an optimal circuit biasing strategy based on our observation that very low signal current does not necessarily improve the SNR though it may decrease the flicker noise.

8.4 Future Work

Study of impact of noise on circuit design methodology can be extended to other processes as well. Study can be extended to find optimal bias point for drain voltage as well.

Tuning circuits for low frequency signal processing to maximize SNR, extending the study to larger integrated circuits will be more time consuming and simulators need to be written to achieve this optimal point. The main advantage in

using this strategy, we can avoid modulating low frequency signal to high frequencies before carrying out any computations.

8.4.1 pMOS transistors

We did not include a study of PMOS devices in this work. It is claimed that PMOS devices have lower noise compared to NMOS devices [29]. This is maybe due to their larger area (hence, lower charge density), low mobility of holes (and larger effective masses) and lower trapping and de-trapping time constants for holes. The reasons are seem to be same as for unpopularity hole tunneling.

This work can be extended to PMOS devices and we expect to see similar trends in LF noise behavior with variation in biasing strategy. Double channel noise measurement will enable noise measurement in deep-subthreshold region of pMOS devices.

8.4.2 Temperature variation

Mobility is one of the parameters that changes with temperatures. Behavior of low frequency noise at low temperatures provides invaluable information about fraction of flicker noise dominated by mobility fluctuation and another fraction coming from number density fluctuation. Flicker noise can be a useful tool for study of effect of mobility fluctuation with temperature. This would require deeper investigation of various factors affected by low temperatures.

8.4.3 Defect characterization

Low temperature noise spectroscopy provides useful information about time constant of impurities and their time constants [48, 42]. It has been used in semiconductor industry for defect characterization. We characterized our devices at a resolution of 0.25 Hz and did not find any defect except for one case where Lorentzian spectra was seen.

8.4.4 Optimization Problem

Study in this dissertation answered the optimization problem in circuits dealing with low frequency signals experimentally. We found the optimization problem by biasing and measuring noise for certain devices and a circuit. The problem of maximizing signal to noise ratio, dynamic range and minimizing power and signal distortion is critical for circuit designers especially for those working under more constrained environments like sensors and mobile applications [**?**, 8, 55, 20]. Our experimental approach gives us a good understanding of the behavior of the noise, signal strength and power and the critical need of selecting an optimal point to enhance the performance of a circuits. It is not feasible for circuit designers and analysts to spend time and effort measuring noise and SNR for each biasing condition and come up with a best biasing strategy. This optimization problem can be framed as a mathematical optimization problem and solved using circuit simulators (CAD, neural networks) for more complicated circuits and appropriate biasing scheme utilized [25]. Computers provide a faster and an efficient solution to such problems

without having to fabricate, test and characterize the circuits. It also provides the flexibility of changing configuration, size and circuit parameter at a very low cost and within fraction of time needed for experiments. One of the main challenges that will be encountered is having accurate flicker noise model. As the dominant flicker noise phenomenon depends on the device and fabrication process, small signal model needs to obtained first. Having the accurate models, optimal point for high SNR and low power can be easily estimated.

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