ABSTRACT

Title of dissertation: CHAOTIC OSCILLATIONS
IN CMOS INTEGRATED CIRCUITS

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Chaos is a purely mathematical term, describing a signal that is aperiodic and sensitive to initial conditions, but deterministic. Yet, engineers usually see it as an undesirable effect to be avoided in electronics. The first part of the dissertation deals with chaotic oscillation in complementary metal-oxide-semiconductor integrated circuits (CMOS ICs) as an effect behavior due to high power microwave or directed electromagnetic energy source. When the circuit is exposed to external electromagnetic sources, it has long been conjectured that spurious oscillation is generated in the circuits. In the first part of this work, we experimentally and numerically demonstrate that these spurious oscillations, or out-of-band oscillations are in fact chaotic oscillations. In the second part of the thesis, we exploit a CMOS chaotic oscillator in building a cryptographic source, a random number generator.

We first demonstrate the presence of chaotic oscillation in standard CMOS circuits. At radio frequencies, ordinary digital circuits can show unexpected nonlinear responses. We evaluate a CMOS inverter coupled with electrostatic discharging (ESD) protection circuits, designed with 0.5μm CMOS technology, for their chaotic oscillations. As the circuit is driven by a direct radio frequency injection, it exhibits a chaotic dynamics, when the input frequency is higher than the typical maximum operating frequency of the CMOS inverter. We observe an aperiodic signal, a broadband spectrum, and various bifurcations in the experimental results. We analytically discuss the nonlinear physical effects in the given circuit : ESD diode rectification, DC bias shift due to a non-quasi static regime operation of the ESD PN-junction diode, and a nonlinear resonant feedback current path. In order to predict these chaotic dynamics, we use a transistor-based model, and compare the model's performance with the experimental results. In order to verify the presence of chaotic oscillations mathematically, we build on an ordinary differential equation model with the circuit-related nonlinearities. We then calculate the largest Lyapunov exponents to verify the chaotic dynamics. The importance of this work lies in investigating chaotic dynamics of standard CMOS ICs that has long been conjectured. In doing so, we experimentally and numerically give evidences for the presence of chaotic oscillations.

We then report on a random number generator design, in which randomness derives from a Boolean chaotic oscillator, designed and fabricated as an integrated circuit. The underlying physics of the chaotic dynamics in the Boolean chaotic oscillator is given by the Boolean delay equation. According to numerical analysis of the

Boolean delay equation, a single node network generates chaotic oscillations when two delay inputs are incommensurate numbers and the transition time is fast. To test this hypothesis physically, a discrete Boolean chaotic oscillator is implemented. Using a CMOS 0.5 μm process, we design and fabricate a CMOS Boolean chaotic oscillator which consists of a core chaotic oscillator and a source follower buffer. Chaotic dynamics are verified using time and frequency domain analysis, and the largest Lyapunov exponents are calculated. The measured bit sequences do make a suitable randomness source, as determined via National Institute of Standards and Technology (NIST) standard statistical tests version 2.1.

CHAOTIC OSCILLATIONS IN CMOS INTEGRATED CIRCUITS

by

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To my parents Jonghwa Park and Sookwon Kim

for all their support, love, sacrifices, and prayers.

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I would like to give special thanks to my two greatest advisors, Professor Daniel Lathrop and Doctor John Rodgers. My long journey has started from Summer of 2009, when I was introduced to unknown fields of chaos. I would like to express my gratefulness to Professor Daniel Lathrop for giving me an invaluable opportunity to work this challenging and interesting projects. He has always encouraged me in every positive ways and showed boundless enthusiasm. I also give my special appreciations to Doctor John Rodgers who is a great engineer and scientist. I am forever grateful to his dedications to the projects. I will cherish the opportunity I had to work with him and always remember his valuable discussions, lessons, and times.

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This graduate school life would have not been made this far without my wife, Ena Kim. I would never forget her love, support, prayers, and endurance and I

promise to return all for the rest of our lives. Last, but not the least, I would not be where I am now, without the supports, prayers, and sacrifices from my parents. I truly appreciate for everything that my parents have done for me.

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Chapter 1

Introduction

1.1 Motivation

Chaotic dynamics describe a signal that is aperiodic, and sensitive to initial conditions, yet deterministic. Chaotic oscillations have long been studied as an intriguing mathematical phenomenon, yet engineers usually see it as an undesirable effect to be avoided in designed systems. However, a new view has recently emerged, and researchers now recognize that chaos may offer substantial benefits to a number of engineering applications, including communications, remote sensing, and cryptography. This change in perspective was prompted by two important discoveries: (1) chaotic systems are easily controlled [2] and (2) multiple chaotic systems can synchronize [3]. These discoveries have shown that the unpredictable instability of chaos may be transformed into natural versatility and flexibility. Consequently, much theoretical and experimental research has advanced this new area of chaos engineering.

Many chaotic systems require chaotic circuits or chaotic oscillators as core parts. The design of chaotic oscillators has been a field of increasing interest during the past few decades. After the first thrust of chaotic circuits in the early 1980s, the development of chaotic circuits has taken interesting paths in unique directions [1]. The main design goal in chaotic circuits has been to develop new chaotic circuits,

and to study the nonlinear dynamics responsible for chaos generation. The study of chaotic circuit design has been more popular ever since scientists and engineers began to find applications of these chaotic circuits in fields such as communication and cryptography [4, 5].

Most of the present chaotic circuits are developed through careful modeling of nonlinear dynamics and are purposely designed to operate in the chaotic regions. We would like to introduce a new *paradigm* of generating chaotic oscillations that utilize the chaotic oscillations present in standard CMOS circuit design. In this thesis, we study the chaotic dynamics observed in a practical integrated circuit (IC). This is, to the author's knowledge, the first work demonstrating chaotic oscillations in a generic CMOS integrated circuit.

Not only does chaotic oscillation in standard CMOS circuits provide an opportunity to develop chaotic circuits in the simplest structures, it can also motivate a better understanding of the stability of electronics when are exposed to high power microwave sources. Especially in the operation of radio frequency CMOS integrated circuits, we observe various forms of instability and other effects. As a consequence of such high power microwave signals coupling to the circuits, many forms of destructive and non-destructive effects occur and are reported [6]. Examples of destructive effects include junction and dielectric breakdown, which are merely physical damages of systems. As examples of non-destructive effects, researchers have identified some low-order nonlinear effects, usually categorized as a single bit error [7], a latch-up [8], or even a relaxation oscillation [9]. Yet, there have been no reported observations of higher-order effects like chaotic oscillation in generic CMOS circuits when a

given circuit is excited by electromagnetic interference. In many different contexts, as ways to characterize nonlinear behaviors of radio frequency power amplifier design, many studies suggest high-order instability [10], or spurious oscillation [11], or parametric subharmonic oscillation [12], but none have analyzed this effect further in the context of nonlinear dynamics. The importance of understanding chaotic oscillation lies in the fact that, unlike a low-order instability, this chaotic oscillation can actually drive the system into a temporary reset or failure. This is of interest to people studying high power microwave (HPM) effects. The effect under exposure to HPM sources is the concern, and if a large RF signal can drive the system into a chaotic state, then this could bring new ways to destroy or upset the system without physically damaging the system.

Another topic in this thesis is the use of CMOS chaotic circuits in the design of random number generators, which is key in the fields of hardware cryptography. A random number generator in hardware cryptography is used mainly for the security and privacy of users. Building a successful cryptographic solution relies heavily on the outcomes of randomness in the system. Among many candidates for random sources, the chaotic oscillator has gained popularity over many non-deterministic sources like thermal noise and stray radio frequency waves. In building a random number generator to be more compatible with CMOS technology, we examine an important class of generating chaotic oscillations, that is, *Boolean Chaos*. In this way, we have successfully built a CMOS Boolean chaotic oscillator which is feasible for generating random numbers. The NIST statistical test version 2.1 is perform to check its feasibility [13].

1.2 Theoretical Background

To demonstrate the presence of chaotic dynamics in electronics, at the fundamental stages, we need to study circuits in the nonlinear dynamics context. In this sense, it is important to look at previous studies regarding chaotic circuit development. For background, many terms, characterizations, and the structure of generic chaotic circuits are reviewed.

Many HPM effects and directed electromagnetic source effects have been reported. We review several examples of these effects, and categorize them as either non-destructive and destructive effects.

1.2.1 Chaotic Circuits in Nonlinear Dynamics

Chaos theory describes the behavior of a dynamical system that is aperiodic, and sensitive to initial conditions, yet deterministic. Chaotic systems are encountered in a wide variety of fields including chemistry [14], biology [15], optics [16], and electronics [17]. This definition of chaos is generally an accepted one throughout a broad community, including mathematics, pure and applied physics, and engineering.

At first, study of chaotic circuits has generally been purely for academic and theoretical reasons. Chaotic circuits were built as physical tools to study the nonlinear dynamics described by a set of governing equations. Mathematicians and theoretical physicists built chaotic circuits to explain the dynamics of complex systems. Lately, research in chaotic circuits has been extended to actual applications

in communication and cryptography. New types of chaotic oscillators are increasingly being introduced to meet the needs in such fields. Here, we would like to summarize the work and research trends in chaotic circuits, along with introducing the important works.

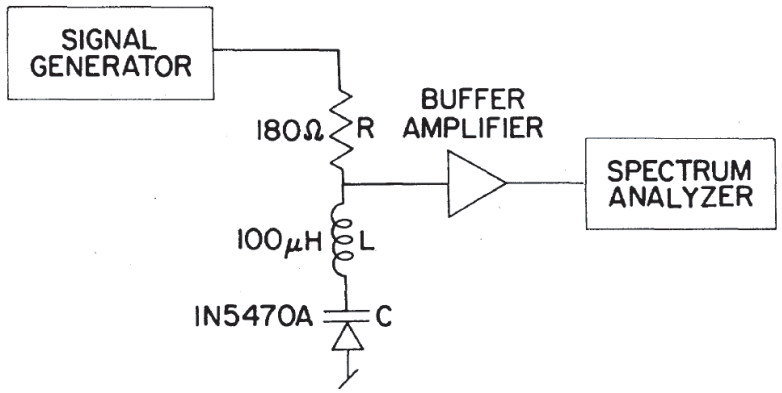
At this point, it is interesting to note an important finding in developments of chaotic circuits: chaos synchronization. Since chaotic signals are hard to control and predict, many engineers have neglected or underestimated their use in engineering systems [3]. Due to the discovery of the interesting phenomenon that chaotic signals can synchronize, chaos research has expanded to the engineering fields as well. Likewise, chaotic circuits play central roles in the physical implementation of chaotic systems. As an active research topic, new types of chaotic circuits are introduced to meet the needs of system. We will introduce a few important chaotic circuits, and will categorize numerous chaotic circuits by the method of chaotic oscillation generation.

- Chaotic circuits, from nonlinear nature of semiconductor device parameters [1] and [18].
- Chaotic circuits, from piecewise-linear negative resistance [19] and [20]
- Chaotic circuits, from hysteresis [21] and [22].
- Chaotic circuits, for high speed operation [23], [24], and [25].

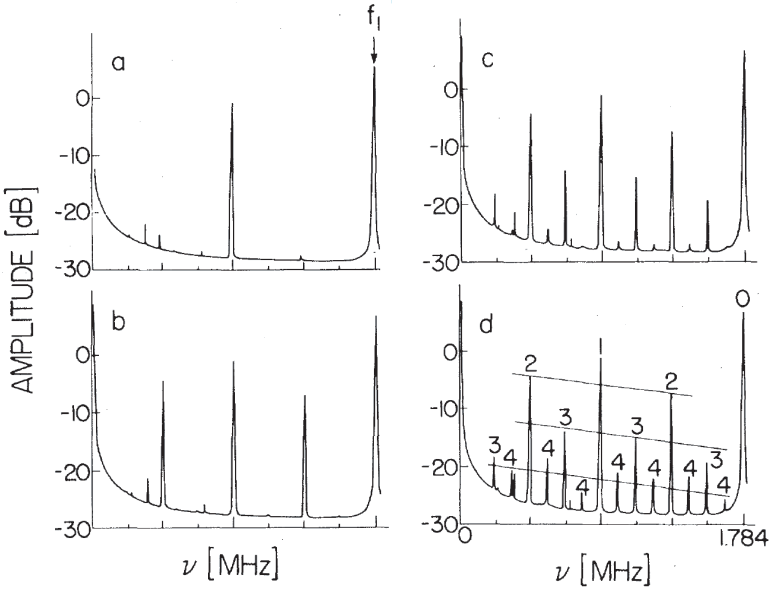
At first, chaotic circuits were developed as a tool to validate nonlinear dynamics theory. Famous attractors named after Poincare, Lorenz, and Rossler have all

been subjects of study in mathematical modeling of complex nature. An attractor is a set of points that is used to describe a system towards which the system evolves. Scientists have built chaotic circuits to validate their models. One of the early examples of chaotic circuits is the "Linsay circuit," or RLD circuit, made of a nonlinear diode, a resistor, and an inductor with a non-autonomous signal excitation. The first electronic circuit implementations appeared in the mid-1980s with the driven anharmonic oscillator [1]. Fig. 1.1(a) shows the diagram of this chaotic circuit. Its nonlinear element in this chaotic circuit is a nonlinear p-n junction diode whose capacitance varies as the voltage across the junction changes. As the circuit is driven by a signal generator and its magnitude changes, period doubling as well as period tripling and quintupling, and other subharmonic generations are observed, as shown in Fig. 1.1(b). Further study on these driven RLD chaotic circuits revealed important nonlinear dynamics. Ref.[26] explains the universal behavior of chaotic oscillation seen in this type of circuit including important features of chaotic dynamics such as intermittency, crises, period doubling, and coupled oscillator behavior. The junction capacitance was identified as the source of chaotic oscillation. The capacitance varies with applied voltage as well as applied signal frequency. Another interesting work relies on the chaos found in a driven diode-terminated transmission line, with the transmission line impedance mismatched with that of the source [18]. Ref.[18] discusses the relationship of reverse recovery time of the junction diode with the generated chaos.

Another class of chaotic circuits is based on a piecewise-linear resistance, usually implemented with operational transconductance amplifiers. One of the most



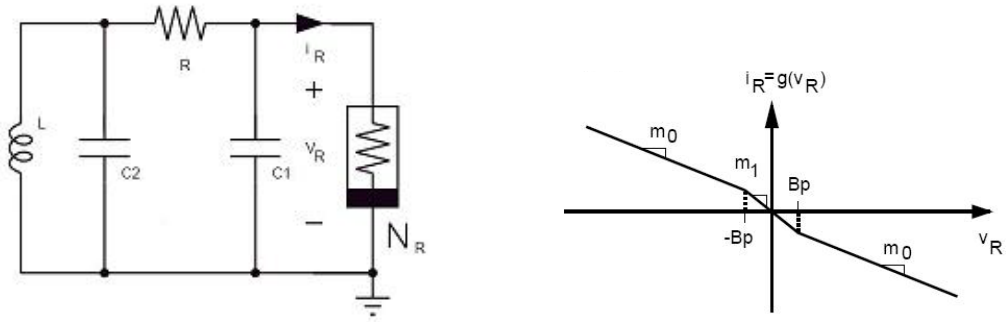
(a)



(b)

Figure 1.1: (a) Circuit diagram of driven anharmonic oscillator. This circuit consists of a nonlinear capacitor, a resistor, and an inductor [1]. (b) Voltage spectrums as RF amplitudes change, driving circuits from periodic oscillation to chaotic oscillation.

famous chaotic circuits is probably Chua's circuit, shown in Fig. 1.2(a) [19]. This circuit consists of linear capacitors, inductors, and a diode with negative resistance whose current and voltage relation is shown in Fig. 1.2(b). For chaotic oscillation, the DC load line has to generate two unstable equilibrium points in the transfer curve of the Chua diode. In other words, we need at least two unstable equilibrium points, one to provide stretching dynamics and the other to provide folding dynamics. Nearby trajectories of a dynamical system are repeatedly diverged exponentially and converged back together in phase space. The operating principle of



(a) (b)

Figure 1.2: (a) Circuit diagram of Chua chaotic circuit. (b) Current-voltage transfer characteristics of Chua diode [19].

this circuit is that the DC equilibrium points are given by the intersection between v_R-i_R characteristics of the nonlinear element and the load line $1/R$. For the general double scroll strange attractor, the circuit has three DC equilibrium points or three intersections. One of them is at the origin and the other two are usually located at

the second and fourth quadrants. These two latter points act as the fixed points in the attractor. There are many different versions of Chua's circuit as the Chua diode, or the negative resistance function can be implemented with various kinds of forms. This work [27] is the first monolithic realization of the nonlinear element in Chua's circuit.

While Chua's circuit relies on the nonlinearity of Chua's diode, the circuit first introduced in [21] generates chaotic oscillation via hysteresis. This circuit, shown in Fig.1.3, consists of op-amps which produce a type of hysteresis. The basic idea

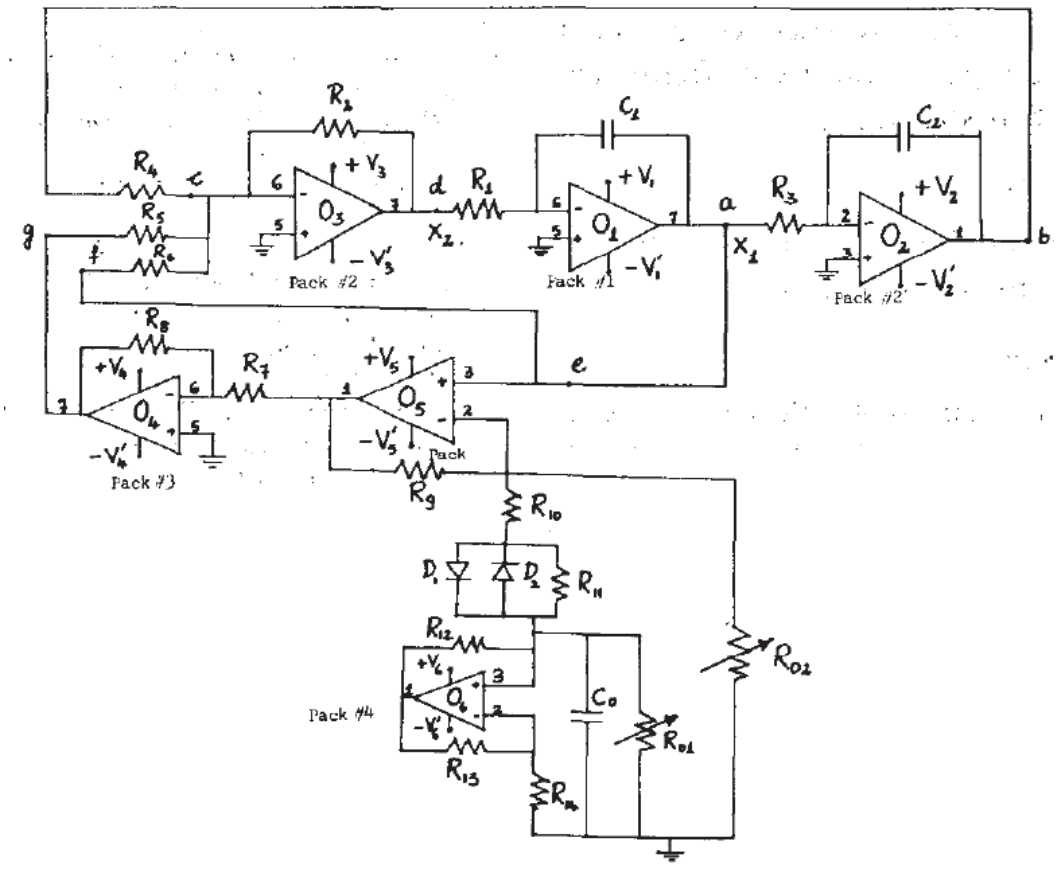


Figure 1.3: Circuit diagram of an RC Op-Amp chaos generator using a hysteresis [21].

is to begin with second-order ordinary differential equations whose nonlinearity is mainly from a type of bent hysteresis. The modification is made so that each cycle of the dynamical system produces the hysteresis to a different point of its loop which eventually causes chaotic oscillation [28]. In Fig. 1.3, the circuits with O_1, O_2, and O_3 form a dynamical system and O_3, O_4, O_5, and O_6 form a bent hysteresis nonlinearity.

Another important class of chaotic oscillators aims at the generation of a high frequency chaotic signal. Due to an increasing need for high frequency chaotic oscillators, various types of chaotic oscillators have been developed. However, most of the important attempts in designing high frequency chaotic oscillators involve the adaptation of nonlinear radio frequency components, such as the phase-locked loop, the oscillator, and the power amplifier. A phase-locked loop (PLL) is a functional device, widely used to synthesize and convert the frequency, and is used as a frequency-modulated demodulator. The basic configuration of a PLL consists of a phase detector, a low-pass filter, and a voltage controlled oscillator, as shown in Fig. 1.4 [23]. Chaotic oscillation is observed when the maximum angular frequency deviation exceeds some critical value. This critical value is chosen so that the frequency difference between the free-running frequency and the input carrier frequency is slightly greater than the pull-in frequency in order to realize the out-of-lock condition.

The Colpitts oscillator [24] which is shown in Fig. 1.5, consists of a single bipolar junction transistor with the feedback network from an inductor L with a series resistance R_L, and a capacitive divider from C_1 and C_2. The complex dynamics

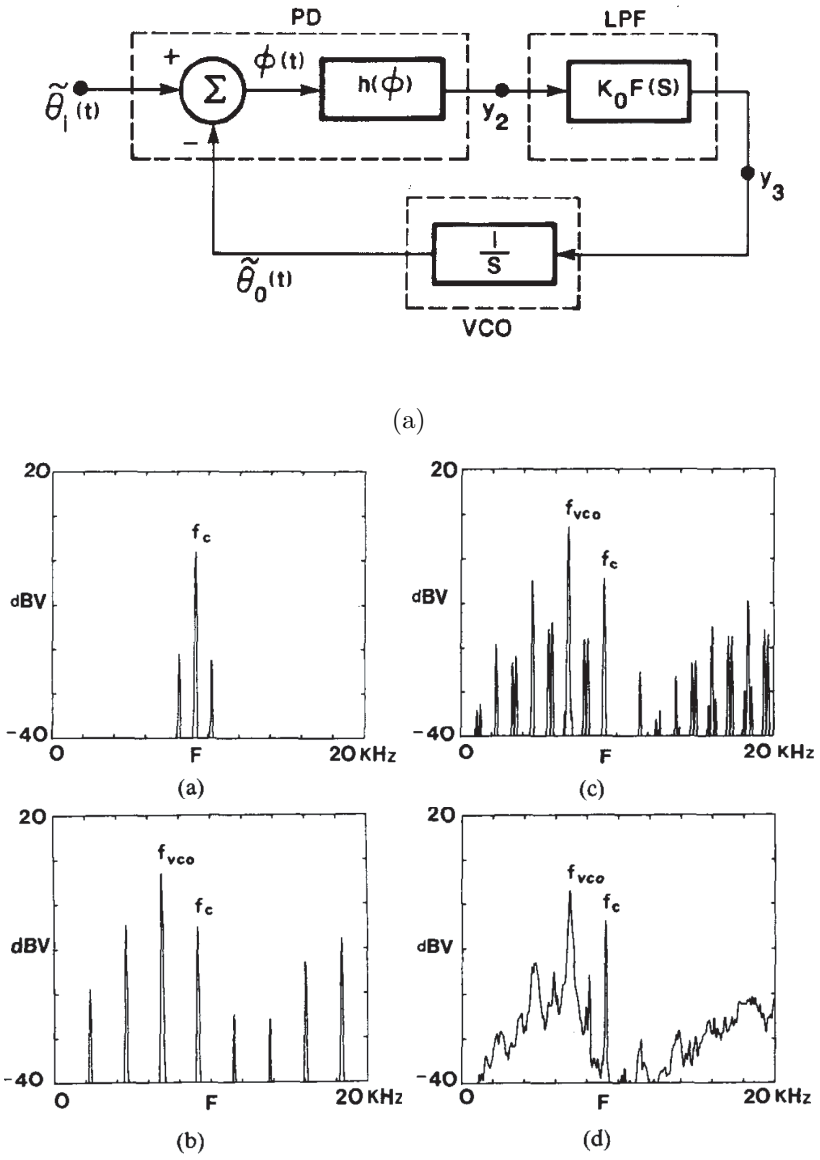


Figure 1.4: (a) Block digram of a phase-lock loop (PLL). (b) The bottom right figure shows a broad chaotic spectrum [23].

of the oscillator may be understood by having two equilibrium points, one in the forward active region and one in the cutoff region, resulting in asymmetric driving point characteristics [29].

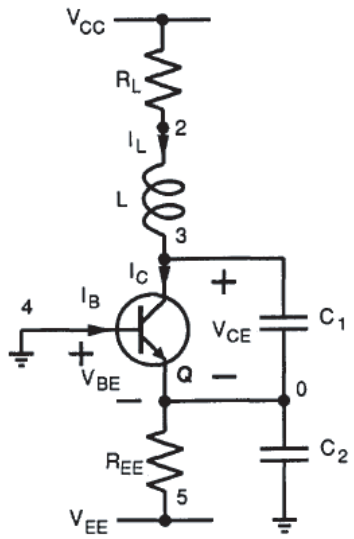


Figure 1.5: Circuit diagram of a bipolar junction transistor Colpitts oscillator [24].

Another important class of chaotic circuits make use of so-called "Boolean chaos". Boolean chaos [25] is a phenomenon in an autonomous network which shows high dimensional chaotic oscillation, exponential sensitivity to initial conditions, and has a broad power spectrum. This unique behavior was first described by a group of mathematicians, using a Boolean delay equation [30]. The circuit node includes Boolean-like state transitions with a fast transition time, and a feedback loop with incommensurate delay inputs that lead to Boolean chaotic oscillation. Fig. 1.6 depicts an example of a Boolean chaotic circuit, which consists of digital circuit elements. The bandwidth of the chaotic oscillation depends on the propagation delay time as well as the power supply of the system.

Another research approach to chaotic circuits would be to study the necessary and sufficient mathematical conditions for chaos generation. While there is an ever-

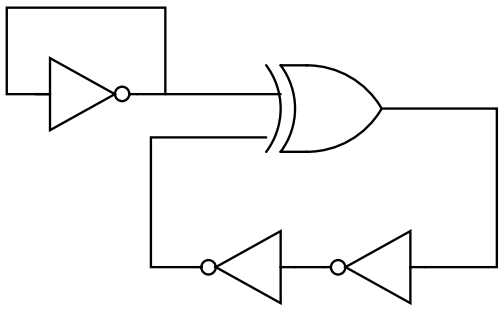


Figure 1.6: Example of Boolean chaos circuit, which consists of one NAND gate with three NOT gates.

increasing number of chaotic circuits, the necessary and sufficient mathematical conditions for chaos generation are unknown. The purpose of this kind of work is to find the simplest mathematical function that gives rise to chaos and to find general classes of oscillators that exhibit chaos. Researchers looked for the simplest "jerk" functions which result in positive Lyapunov exponents [31][32]. A system that has received considerable attention is

$$\dddot{x} = J(\dddot{x}, \dot{x}, x) \tag{1.1}$$

"jerk function"means a function J such that the third-order ODE can be written in the form of (1.1). The computational model considers systems of the form

$$\dddot{x} = a_1\ddot{x} + a_2\varphi(\ddot{x}) + a_3\dot{x} + a_4\varphi(\dot{x}) + a_5x + a_6\varphi(x) + a_7 \tag{1.2}$$

where $\varphi(x)$ is a simple nonlinear function chosen to permit electronic implementation with diodes and operational amplifiers. The procedure for finding the jerk function is to run a 4th-order Runge-Kutta algorithm to solve the equations with randomly chosen coefficients a_1-a_7, and a selected nonlinear function $\varphi(x)$.

Next, there was an attempt to find a design methodology for building chaotic oscillators [33].This paper explains the three important classes of core oscillators that are necessary to generate chaotic oscillation. The active networks in Fig. 1.7 are usually voltage controlled current sources.

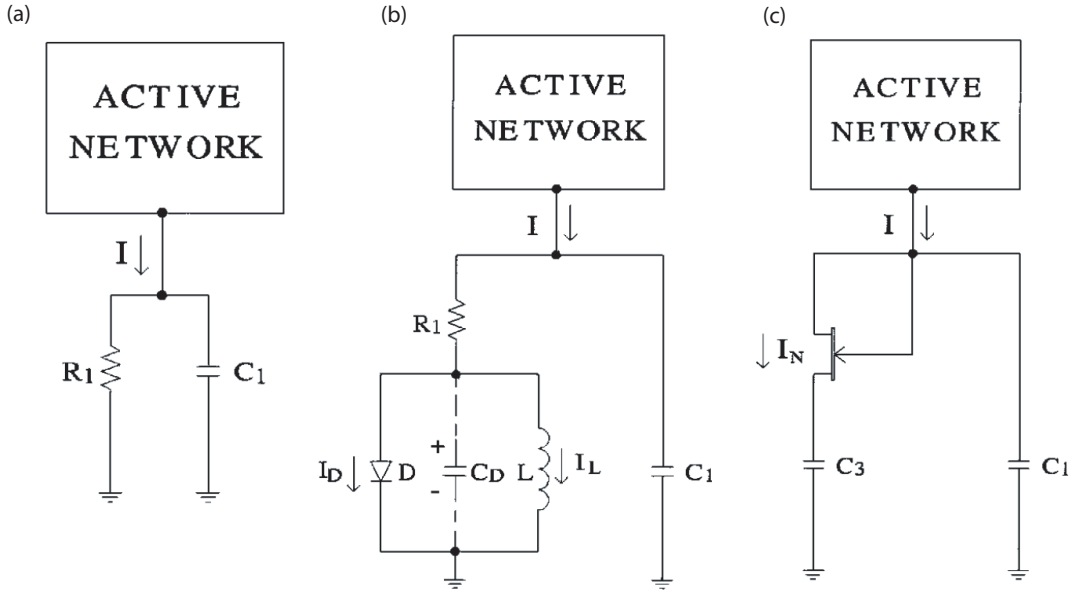


Figure 1.7: Classes of core chaotic oscillators. (a) sinusoidal oscillator with a parallel RC, (b) using diode inductor composite, and (c) with FET and capacitor composite [33].

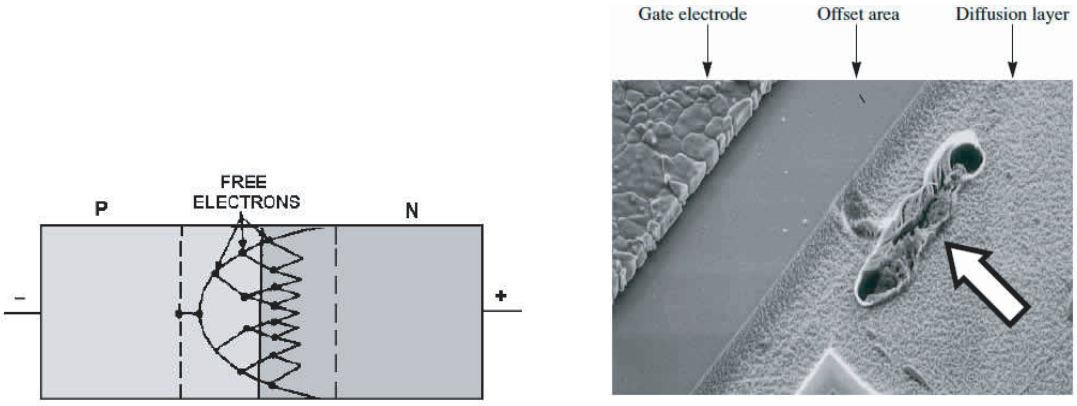
1.2.2 Examples of Electromagnetic Interference Effects

Electromagnetic emission is of concern to many circuit designers. This concern has become more important as improvement in chip technology has led to a higher density of circuits inside a single chip, and a decrease in the operation wavelength of the circuit. When high power microwave sources are coupled to a circuit, various kinds of effects can occur. Examples of external electromagnetic sources are the

signals from radars and high power microwave weapons that are usually intentionally designed to bring high power RF outputs.

Microwave signals interference with electronic systems is not an entirely new concern. Although this may not be exactly fit into the scenario of HPM effects in the CMOS ICs, the following story is a good example of electromagnetic interference in our daily lives. We are reminded of the importance of EMI compliance whenever we take off or land in an airplane, and are requested to refrain from using all electronic devices. This request suggests that electromagnetic energy emitted from our laptops and personal devices might induce noise in the communication between airplanes and control towers. In any case, the importance of keeping electronic systems from interfering with others is recognized by all designers.

Previous studies have shown that various physical mechanisms result in instabilities when a circuit is excited by microwave signals. The first observation is the rectification of radio frequency (RF) signals in bipolar junction transistors and field-effect transistors. When a microwave signal is injected into the base of the BJT, qualitatively speaking, the AC signal is rectified to a DC value by the nonlinearity of the emitter-base junction characteristics, and may shift the quiescent point of operation. Many studies [34, 35] have reported the experimental observation as well as the mathematical proof of this effect. Low frequency rectification is often within the operating passband of the circuit, and may have unintended effects on the entire circuit. Similar behaviors are also observed in junction field-effect transistors [36]. The model in this literature, from a small signal viewpoint, demonstrates that the effect is caused by device nonlinearity, especially the nonlinear transconductance of



(a) (b)

Figure 1.8: (a) Diagram of PN-junction in the Avalanche breakdown. High reverse field creates the multiplications of free electrons by impact ionizations. (b) Scanning electron microscopy image of a junction breakdown. The arrow region shows a physical PN-junction damage.

the field-effect transistors.

Effects can be grouped into two non-destructive and destructive effect, depending on the degree of damage. First, many PN-junction exist inside the CMOS structure, and due to high reverse biasing of these PN-junctions, these junctions can experience breakdowns, as shown in Fig. 1.8. In a high reverse bias state, the electrons cause impact ionization, resulting in the freeing multiple electrons. This is called the avalanche breakdown. Eventually, the high reverse fields even break the bondings of the donors or acceptors, resulting in a sudden current spike. This is called the Zener breakdown [37]. Another destructive effect is a dielectric breakdown. Most CMOS ICs have dielectrics as insulating layers, and when they are shorted due to high RF signal coupling, the circuit no longer functions. Gate oxide

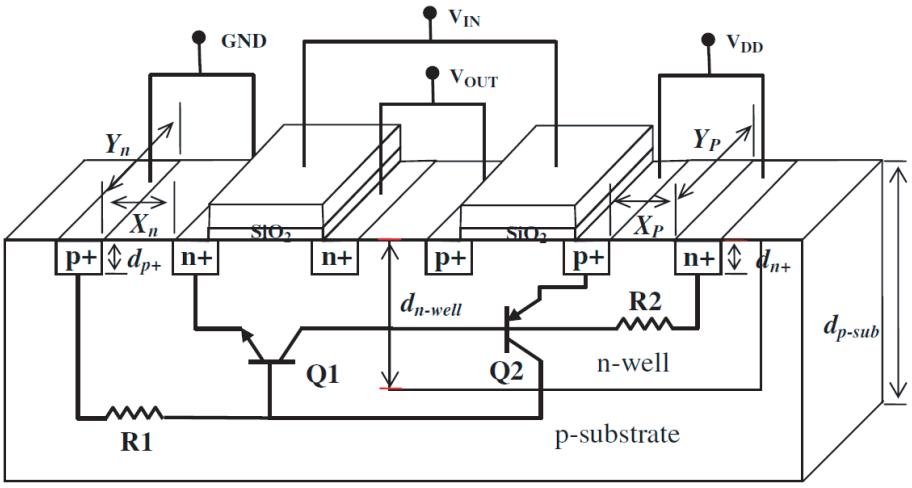


Figure 1.9: Schematic diagram of CMOS inverter showing two parasitic bipolar junction transistors Q_1 and Q_2. Latch-up effects are due to the BJT action.

breakdown can cause a conduction path between the metal gate and the channel. These two destructive effects are well known in the start-of-art CMOS technology, and this damage requires replacement of the parts.

Next, we give a reported example of non-destructive effects. This is a transient-induced latch-up. Latch-up can occur when the parasitic bipolar transistor action in the body is turned on, resulting in conduction through the body, rather than through the channel of the MOSFET device. Fig. 1.9 shows that parasitic BJTs are present inside a CMOS inverter. This nonlinear mechanism results in overshoot and undershoot voltage spikes at the outputs and inputs, and most latch-ups occur as a result of high power pulse electromagnetic interference and electrostatic discharging [8, 38].

There is no doubt that these examples are harmful in building reliable CMOS

electronics. However, on the other hand, these effects in standard CMOS circuits could be targets for researchers developing electromagnetic weapons (EMP) [39].

1.3 Organization of the Thesis

The material presented in this thesis is organized into four chapters. The first half of the work focuses on the chaotic oscillation found in generic CMOS circuits, and the second half talks about the specific design of the CMOS Boolean chaotic oscillator.

Chapter 2 is devoted to an experimental demonstration of chaotic oscillation in a CMOS inverter design under microwave signal excitation. We present the design details of the CMOS inverter coupled with electrostatic discharging (ESD) circuits using On-Semiconductor 0.5 μm technology. We also describe how the experiment is performed. We give some experimental observations which suggests ch aotic dynamics. We also give a qualitative analysis of the nonlinear sources.

In Chapter 3, we focus on modeling the chaotic oscillation events demonstrated in Chapter 2. We present a transistor-based simulation, using BSIM 4 SPICE parameters and a lumped-element model, and also numerical modeling, built with sets of ordinary differential equations. We also compute the largest Lyapunov exponents for the outputs generated from the numerical models to verify the existence of chaotic oscillation.

In Chapter 4, we present a new class of chaotic oscillator, the Boolean chaotic oscillator. Based on the Boolean delay equation, we verify the presence of chaos in

such networks. We then test our hypothesis generated with the numerical models by building a Boolean chaotic oscillator with discrete commercial parts. Using CMOS 0.5 μm technology, we build an on-chip CMOS Boolean chaotic oscillator.

Chapter 5 is devoted to a test of the applicability of the designed Boolean chaotic oscillator in cryptographic random number generation. With proper post-processing of the analog signal, we design a random number generator using our integrated circuit. Moreover, a statistical analysis of the random number generation, the NIST test suite, is performed to test the feasibility of our circuit as a random number generation source.

Chapter 6 provides a summary to the thesis and discusses future work.

1.4 List of Contributions

Chaotic oscillation has long been conjectured or observed as an effect of high power microwave signals or directed electromagnetic signals; however, there has been no study or thorough proof of the phenomenon. This becomes more problematic when chaotic oscillation is found in our state-art-technology like CMOS.

One of main reasons that this issue has been overlooked is the divergent research fields involved. As stated, chaotic dynamics in circuits should be studied in the context of nonlinear dynamics; nonlinear dynamics researchers traditionally characterize chaotic oscillation or circuits via a set of governing mathematical equations. Period doubling, intermittency, and positive Lyapunov exponents are important tools in nonlinear dynamics theory for investigating the chaotic nature of

the various systems. However, chaotic oscillation is not a primary concern for RF circuit designers, as long as the circuit is classified as unstable.

In this thesis, we investigate the chaotic dynamics in the CMOS integrated circuits, and validate the presence of chaotic oscillation, when the circuit is under a direct microwave injection.

In second part of the thesis, we exploit chaotic oscillation in building a random number generator. Here, we use a new paradigm of chaos generation: Boolean chaos. We are able to build CMOS on-chip Boolean chaotic oscillators. This type of chaotic oscillator is well-suited to building a cryptographic random number generator.

The contributions of this thesis can be listed in the following points:

Investigation of chaotic oscillation in standard CMOS digital ICs as new class of high power microwave effects. (Chapter 2 and chapter 3)

1. Design of Test CMOS ICs: CMOS Inverter coupling with ESD protection circuits using On-Semiconductor 0.35 μm technology.

2. Direct RF injection experiment on the CMOS IC. Experimental results that shows evidences of chaotic oscillation.

3. Characterization and analytical discussion of the nonlinearity.

4. Transistor-based circuit modeling based on BSIM4 and numerical modeling to verify the presence of chaotic oscillation by computing positive largest Lyapunov exponents.

Design of Random Number Generator using CMOS Boolean Chaotic Oscillator (Chapter 4 and Chapter 5)

1. Numerical analysis of a new chaos generation called Boolean chaos.

2. Design of CMOS Boolean chaotic oscillator using On-Semiconductor 0.35 μm technology, whose bandwidth reaches from DC to 300 MHz.

3. NIST statistical tests about the random number generation using our CMOS Boolean chaotic oscillator.

Chapter 2

Experimental Chaotic Oscillation in CMOS Digital Circuits

2.1 Overview

Here, we study the effect of electromagnetic sources, especially high power microwave (HPM) signals, such as those from radars and directed microwave sources, on the operation of CMOS integrated circuits. The term "effect" is used to study the behavior of the circuit, when high power electromagnetic sources are coupled into the circuit.

Previous study on the "effect" has focused on the behavior of commercial components. While CMOS has been a start-of-art technology over the last several decades, little research was done on electromagnetic source effects in CMOS ICs. As the technology has developed, the device switching rate has gotten higher and scaling of the devices becomes smaller, making the dielectric of CMOS even thinner. These devices, in turn, become highly vulnerable to HPM signals, thus causing some disruptions to the entire system.

In addition, when the circuit is operating in radio frequency range, signal wavelength is comparable to the dimension of passive components. In this regime, printed circuit board traces, packaging, bond-wire, and other passive parasitics all become important to consider. Also, due to high frequency HPM signals, the operating speed of CMOS IC nearly reaches the maximum operating speed of the design

circuit, which brings more nonlinear effects to the dynamics of the circuit.

Some reported circuit effects of HPM signals can be categorized as non-destructive or destructive effects. Destructive effects are caused by large electromagnetic sources which can permanently damage a system. The damaged components have to be replaced for the system to function. Some examples of these permanent damages are junction breakdown and dielectric breakdown. Non-destructive effects generate undesirable results, causing disruption to normal behavior. This requires less electromagnetic energy and effects are temporary. For a system to function again, the system only requires reset. One example is latch-up, which is caused by turning on parasitic bipolar junction transistors inside CMOS structure. The details are explained in Chapter 1.

Another kind of effect is chaotic oscillation. As mentioned, chaos is defined by aperiodicity and sensitiveness to initial conditions, but is deterministic. Researchers have long conjectured and observed a high dimensional instability, referring to it as spurious oscillations, or unstable oscillations [11][12]. This instability is also encountered in high power amplifier stability study. Highly nonlinear power amplifiers are often exposed to these phenomenon, when they are driven under large RF signal [10]. Confirming the existence of chaotic dynamics in the circuit requires some nonlinear dynamics background.

Our approach in solving this problem is purely based on investigating the nonlinear dynamic nature of the designed circuit, because the presence of chaos can only be proven by in context of nonlinear dynamics. Therefore, the work focuses on investigating and observing evidences in experiment and numerical analysis.

In Section 2.2, we give a brief overview of the test circuit and a motivation of the work with the CMOS technology.

In Section 2.3, we show the design details of CMOS digital ICs, which consist of a CMOS inverter, a cascade output buffer, and electrostatic discharging (ESD) protection circuits. The test circuit was designed using Cadence Virtuoso layout tools and was fabricated using the On-Semiconductor 0.5 um process. Basic DC and transient test results are given.

In Section 2.4, we present experimental results of the designed circuit under a direct microwave excitation. We introduce a general experimental procedure and a test-board design. We suggest some evidences of chaotic oscillation through experimental observations.

In Section 2.5, we include the device physics characterization of nonlinear sources present in the circuit. We give qualitative and quantitative analysis of these nonlinear behaviors. Using Lyapunov exponents, we quantify chaotic oscillation in the experimental results.

2.2 Test Circuit Overview

As stated, previous study has involved mainly commercial devices, and has used basic models to describe very simple behaviors. On top of this, it is hard to look inside the physical layouts of circuits due to proprietary restrictions. For these reasons, we design our circuit in house, starting from layouts to PCB soldering. In this manner, all of our circuit parameters are known. In addition, all the SPICE

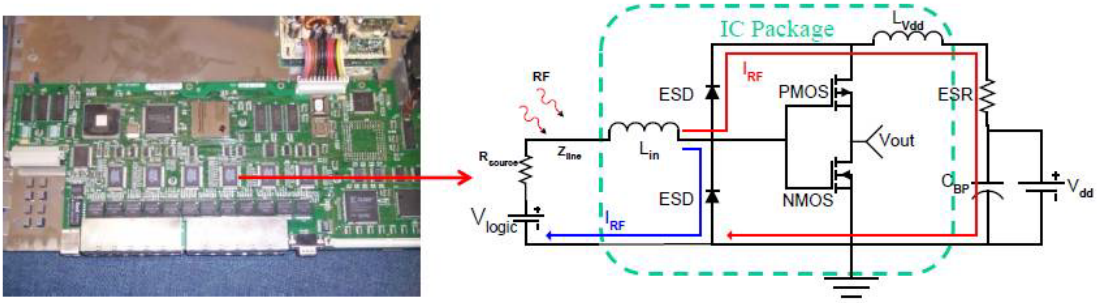


Figure 2.1: Schematic diagram and basic elements in modern CMOS digital ICs.

parameters of the circuit are provided from the foundary service after the company measure and extract from their process test wafers.

As shown in Fig. 2.1, many current electronic systems consist of CMOS ICs. Because the CMOS is the state-art-technology, the study of HPM effects should also be carried out for CMOS ICs. A CMOS digital logic IC is an important and standard functional block in many electronic systems. It generally consists of three main components; electrostatic discharging protection circuits, core logic circuits, and output buffer. All these are essential parts in the CMOS digital IC. Here, we design CMOS inverter which has all three components. The test circuit design is to create basic CMOS ICs, using already established design principles, which is not much different from the commercial CMOS inverters. By keeping the test circuit design as generic as possible, we are able to translate our study into general effects and behaviors.

The following sections cover the design details of three important blocks, as well as basic tests to confirm their functionality.

2.3 Design of CMOS Inverter Chain and Electrostatic Discharging Circuits

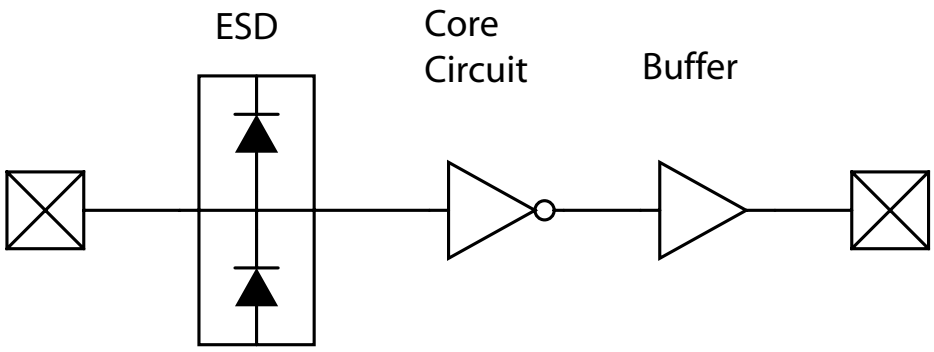


Figure 2.2: Basic components of CMOS digital circuit, consisting of electrostatic discharging (ESD) protection circuit, core circuit, and output buffer.

To demonstrate that chaotic oscillation can occur in the simplest CMOS digital circuits, a CMOS inverter is designed with an electrostatic discharging (ESD) protection circuit and an output buffer. The circuit was designed using On-Semiconductor (formerly AMI) 0.5μm technology from the MOSIS consortium. MOSIS provides access to a wide variety of semiconductor processes offered by many different foundries [40].

A conceptual circuit diagram is shown in Fig. 2.2. The circuit's input is protected by a gate-grounded NMOS (ggNMOS) and gate-coupled PMOS (gcPMOS) ESD structure, and its output is buffered using the cascaded output buffer design. Table 2.1 summarizes the physical dimensions of the designed circuit. The test cir-

cuit is packaged with a surface mount type carrier and is soldered onto a printed circuit board (PCB). An external bypass capacitor of 0.1μF is connected between the DC power trace and the ground plane on the PCB.

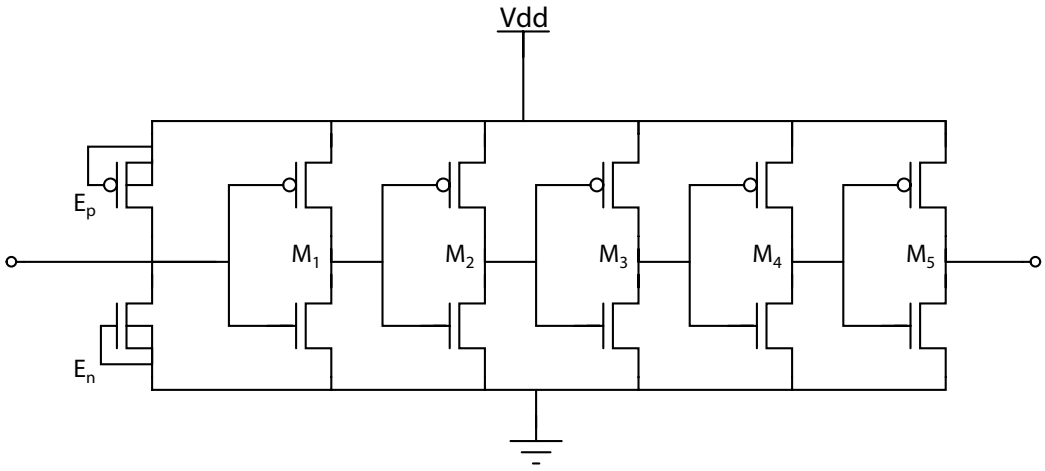
Table 2.1: Physical dimensions of the designed circuit.

		ESD	M1	M2	M3	M4	M5
Length [μm]	pMOS	0.9	0.6	0.6	0.6	0.6	0.6
	nMOS	0.9	0.6	0.6	0.6	0.6	0.6
Width [μm]	pMOS	30	3	10.2	6.9	11.7	25.5
	nMOS	30	1.5	5.1	8.7	11.8	20.3
Number of Fingers	pMOS	12	1	1	5	10	16
	nMOS	12	1	1	2	5	10

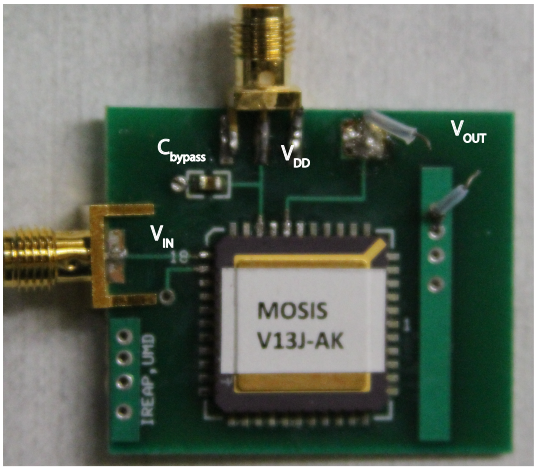
2.3.1 CMOS Inverter

We perform some basic DC tests in both simulation and experiments before injecting an microwave signal. First, we design an inverter using a complimentary MOSFET structure. The nMOSFET and pMOSFET are connected in series, either pulling currents from Vdd or from Gnd.

The switching current of the CMOS inverter is a current flowing at the nFET and the pFET as shown in Fig. 2.4, which is



(a)



(b)

Figure 2.3: (a) Circuit diagram of a CMOS inverter designed using On-Semiconductor 0.5μm process technology. This circuit resembles the simplest digital circuit. The circuit consists of ggNMOS and gcPMOS ESD protection circuits at the input (E_p and E_n). The inverter functions at M1 and output buffers M2, M3, M4, and M5 are designed to drive enough current at the capacitive load. (b) Picture of device-under-test (DUT) on the printed circuit board.

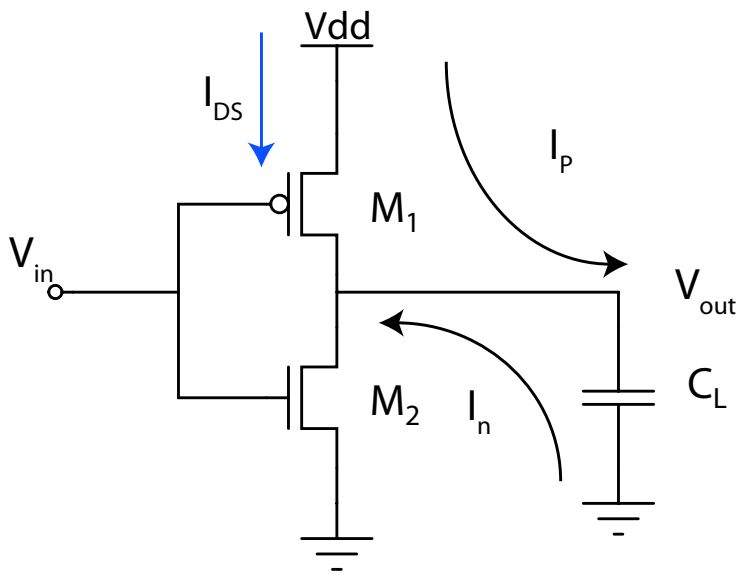


Figure 2.4: Circuit diagram of a CMOS inverter. The switching current is the sum of currents flowing in both the nFET and the pFET.

$$I_{DS.MAX} = I_{n,SAT} = I_{p,SAT} \tag{2.1}$$

with

$$I_{DS.MAX} = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}(V_G - 0 - V_{th,n})^2 = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}(V_{DD} - V_G - |V_{th,p}|)^2. \tag{2.2}$$

Test results of the DC transfer characteristics are shown in Fig. 2.5. The DC current is at a maximum when the saturation currents flow in the nFET and pFET during transition from high to low, as seen in (2.2).

Next, we evaluate the transient behavior of the CMOS inverter. A low-frequency pulse is injected at the input, and the output voltage is measured in real time. Table 2.2 summarizes the switching behavior of this circuit. t_{PHL} is defined as the switching time from a high state to a low state (fall time), and t_{PLH} is

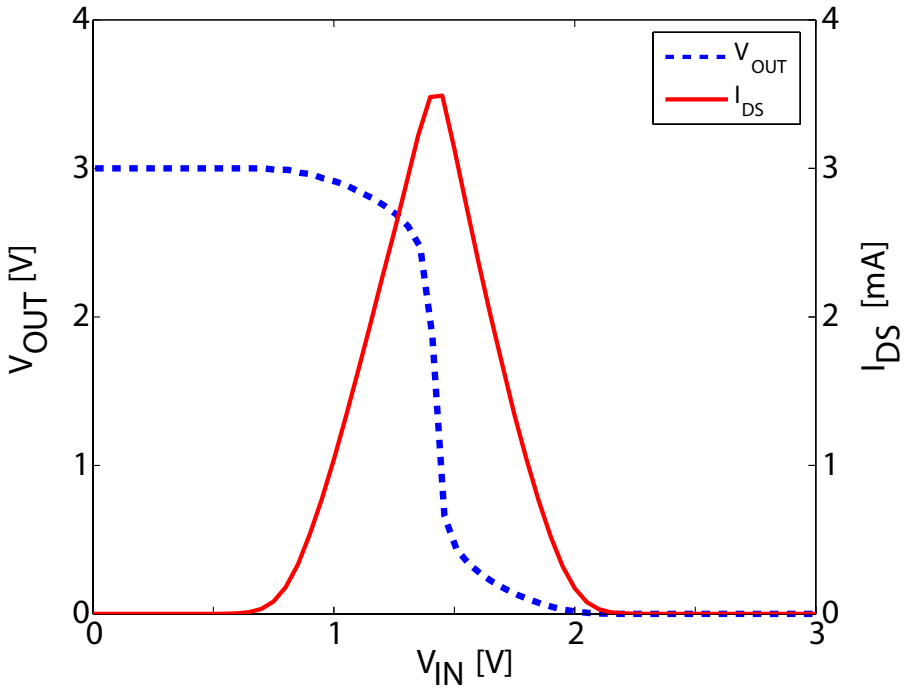


Figure 2.5: Experimental results of DC transfer characteristics and short current of CMOS inverter in DC condition. Peak current of 3.5 mA is measured when DC input voltage is at 1.5 V.

Table 2.2: Switching Characteristics of CMOS inverter.

t_{PHL} [nsec]	t_{PLH} [nsec]	t_{PD} [nsec]	f_{max} [MHz]
2.5	3.2	2.85	350

the switching time from a low state to a high state (rise time). t_{PD} is an average of the two, and f_{max} is an inverse of t_{PD}. Note that there is an increase in the propagation time because of the cascaded output buffer design, which will be explained shortly.

The maximum operating frequency is determined by the inverse of the sum of high-to-low and low-to-high propagation delay times. The time delay constant associated with the discharging of a load capacitor (NMOS switch) is approximately,

$$t_{PHL} = 0.7 \cdot R_n \cdot (C_{ox} + C_L) \tag{2.3}$$

The time constant associated with the charging of a load capacitance (PMOS switch) is,

$$t_{PLH} = 0.7 \cdot R_p \cdot (C_{ox} + C_L) \tag{2.4}$$

where R_n and R_p correspond to the channel resistances of the NMOS and the PMOS, respectively. They differ because of the low mobility associated with holes in the p-channel MOSFET [41].

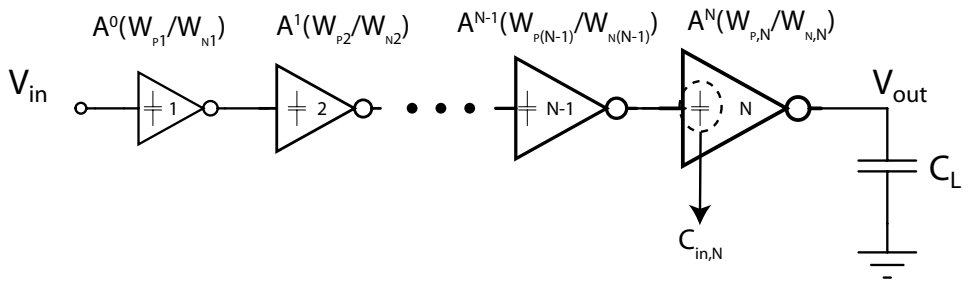


Figure 2.6: Schematic diagram of a cascaded scale-up buffer. The number of stages N should be an even number, and A is a scale ratio for the widths of transistors

2.3.2 Cascaded Output Buffer

To drive a capacitive load, introduced by the parasitic capacitance of a scope probe, we need to design an output buffer. A poorly designed buffer can distort the original signal as well as introduce an extra delay time. Here, we designed a cascaded scale-up CMOS buffer, as shown in Fig. 2.6. The number of stages of the output buffer was carefully adjusted so that there is no degradation in time delay and performance [41]. We add a string of inverters between the on-chip logic and the bonding pads. The number of stages N and the scale ratio A are carefully chosen to minimize the delay of the series of inverters as well as to scale up the input capacitance of the inverters to match the parasitic load capacitance.

$$C_{IN,N} = C_{in1} \cdot A^N = C_{Load} \tag{2.5}$$

or

$$A = \left[\frac{C_{Load}}{C_{in1}}\right]^{\frac{1}{N}} \tag{2.6}$$

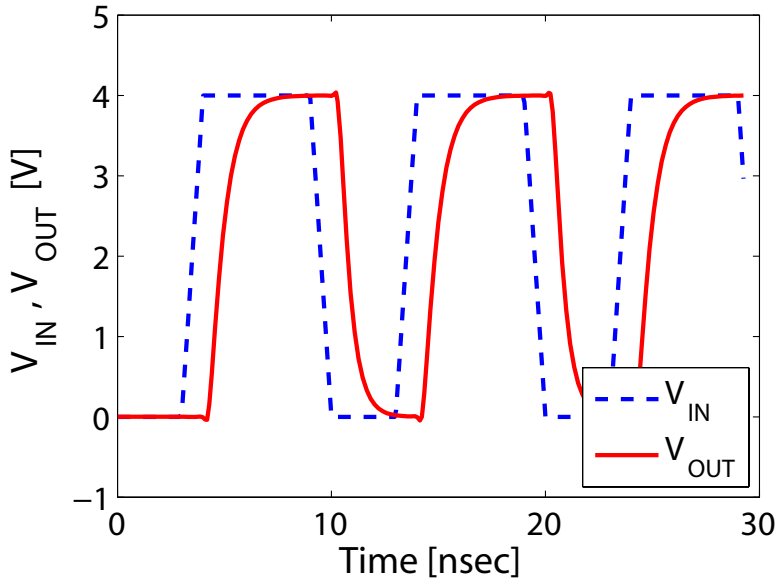


Figure 2.7: Time evolution of input and output voltage of the designed buffer. The simulated results show that the output of buffer has only a small time delay.

To minimize the delay,

$$(t_{PHL} + t_{PLH})_{total} = 0.7 \cdot \sum_{k=1}^{N} (R_{n1} + R_{p1})(C_{out1} + AC_{in1}), \tag{2.7}$$

We take the derivative with respect to N, set the results equal to zero, and solve for N.

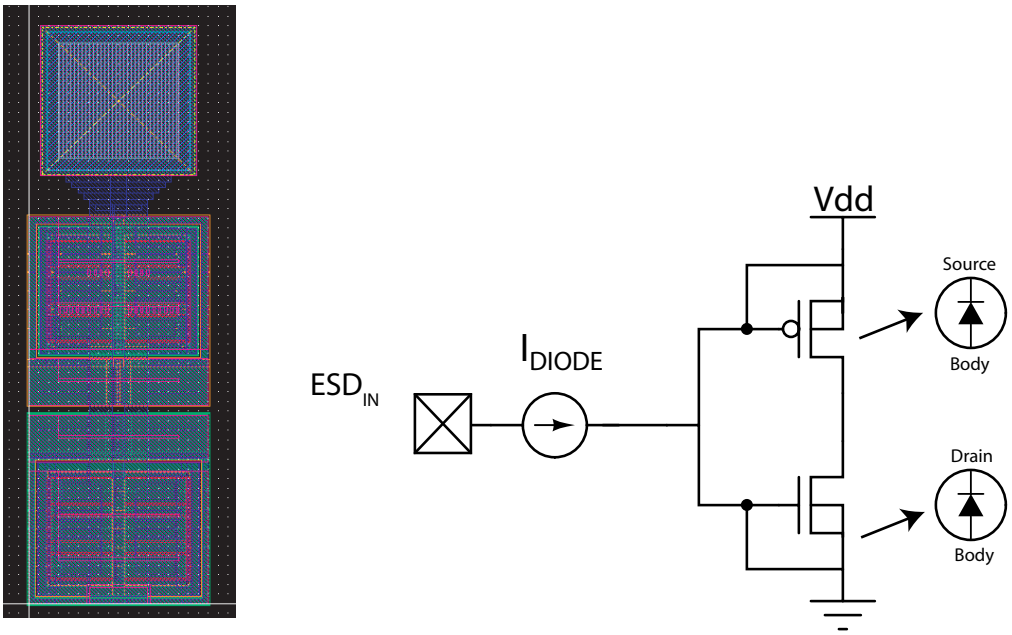
$$N = \ln \frac{C_{Load}}{C_{in1}} \tag{2.8}$$

As a result of the calculation above, assuming a 10 pF of loading capacitance, we design a four stage cascaded output buffer. Fig. 2.7 shows the simulated time trace of input and output voltage signal of the designed buffer. The simulated output signal shows a small finite time delay.

2.3.3 Electrostatic Discharging Protection Circuit

The gate oxide of the MOSFET is the most susceptible to damage from an electrostatic discharge (ESD). For protection from such an ESD event, it is common practice to build an extra circuit to protect the core circuit. Here, we build two junction diodes to prevent the ESD static currents from flowing into the core circuit. As shown in Fig. 2.2, a gate-grounded NMOS (ggNMOS) in a series with a gate-coupled PMOS (gcPMOS) is located at the input of the logic circuit. The drain-body junctions of the NMOS and the PMOS operate as PN-junction diodes, which are the main junction areas implemented for ESD protection. In the absence of an ESD event, the two diodes remain reverse-biased, but when a strong positive ESD event occurs, the gcPMOS turns on, preventing ESD current from flowing into the metal-oxide of the circuit. When a strong negative ESD event takes place, the ggNMOS turns on resulting in the ESD current flowing towards the ground.

Fig. 2.8(a) shows the layout of an ESD protection circuit, consisting of a multi-finger design of ggNMOS and gcPMOS, and a circuit schematic of such a configuration. The current voltage characteristics of ESD switching are shown in Fig. 2.9. Since the circuit is held at the DC supply voltage of 4V, gcPMOS turns on when the ESD voltage exceeds 4V (Region III), and ggNMOS turns on when the ESD voltage falls below 0V (Region I). During the Region 2, both gcPMOS and ggNMOS devices are turned off.



(a) (b)

Figure 2.8: (a) Layout of ESD protection circuits. The topmost square represents a pad design, and the two bottom squares represent several ESD MOSFETs, connected as back-to-back diode. (b) ESD event occurring at the input of CMOS digital circuits. V_{DD} is biased at 4V, and I_{DIODE} is measured at the input.

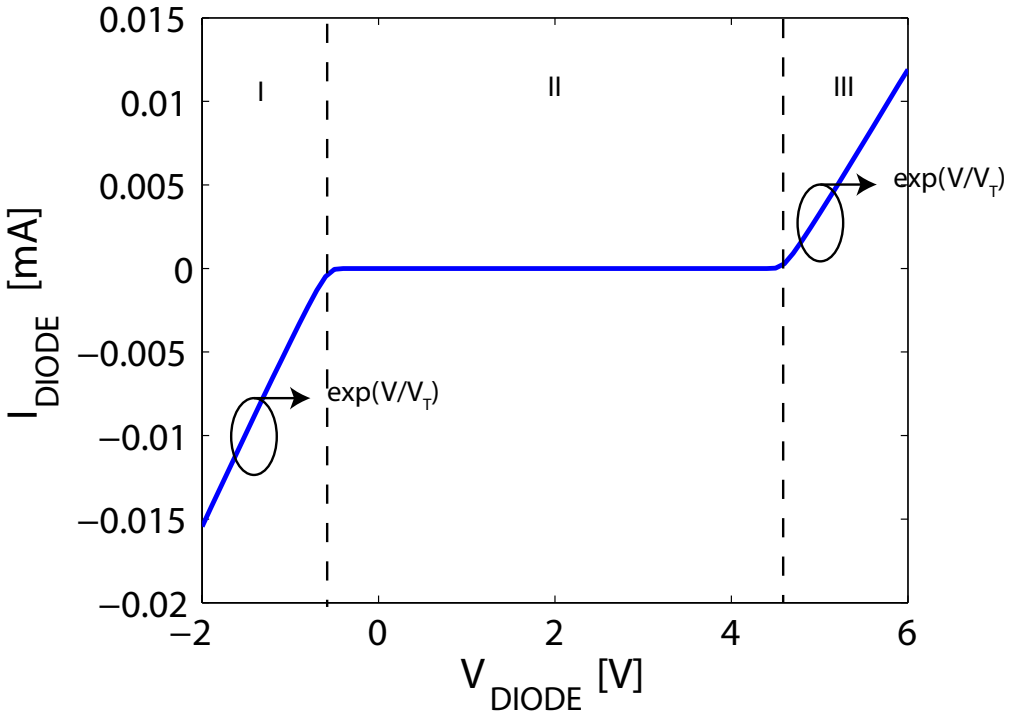


Figure 2.9: Simulation results of current-voltage characteristics in our ESD protection circuits. In Region I, ggNMOS turns on, and gcPMOS turns on in Region III, and finally ggMNOS and gcPMOS remain turned off in Region II. The circuit is biased at the supply voltage of 4V. Current-voltage transfer curves in Region I and III follows the Shockley diode equations.

2.4 Experimental Demonstration of Chaotic Oscillation

2.4.1 Experimental Setup

Fig. 2.10 depicts the experimental setup for measuring real-time output voltages, input voltages, and DC supply currents in order to understand the circuit's susceptibility to the chaotic oscillation in depth. An Agilent E8257D analog signal generator is used to generate a periodic sinusoidal signal. A bias tee is used to measure the detected DC voltage at the circuit input. In this experiment, no DC offset is superimposed on the RF power since chaotic oscillation caused solely by microwave excitation is our primary concern. Data acquisition is performed simultaneously using a computer program, Agilent VEE, for output voltage, input voltage, and supply current. RF power and its frequency are also varied as the tuning parameters in this experiment. Input RF power ranges from -5 dBm to 20 dBm and its frequency is stepped up from 100 MHz to 1 GHz. The DC supply current is calculated from taking the time-averaged value of the AC current from the DC power supply, and the DC input voltage is calculated from taking the time-averaged value of the dynamic input voltage, measured across a large resistance. The time averaged value of the AC term is equivalent to taking the zeroth term of the signal.

$$I_{avg,DCsupply} = \frac{1}{T}\int_T I_{DC,supply}(t)dt \tag{2.9}$$

$$V_{avg,input} = \frac{1}{T}\int_T V_{input}(t)dt \tag{2.10}$$

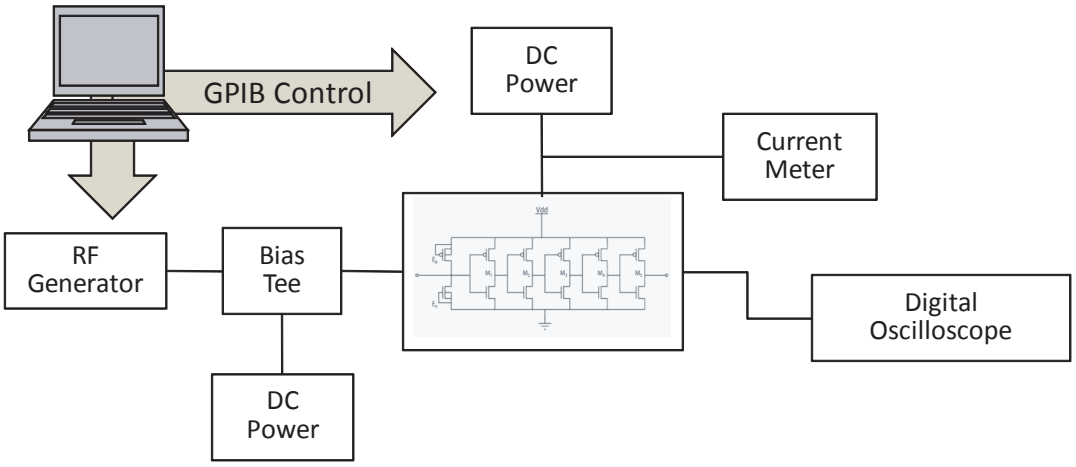


Figure 2.10: Experimental setup for measuring output voltage, supply current, and input rectified voltage. RF signal is directly injected at the input of device-under-test (DUT), mounted on the PCB, with varying RF power and frequency. The digital oscilloscope has a high sampling rate to measure the real time input and output voltages, and the DC supply current is measured with a current meter.

2.4.2 Packaging and Printed Circuit Board Design

The test ICs were first packaged using LCC 44 packaging, which is a surface mounted type. The test ICs has 44 bonding pads located at the outer periphery of the chip as shown in Fig. 2.8(a). Each pad from a silicon wafer is wire-bonded to the packaging using wire-bonding technology. When the circuit is operating in the RF region, this wire-bonding acts as a parasitic inductance, ranging from 1 nH to 5 nH, depending on the length of the wires.

Then, we carefully design a printed circuit board (PCB) using commercial software. The board is made of FR4 material, and trace lines are made of copper metal layers. For high frequency operation, a de-coupling capacitor of 0.1 muF is connected between the power trace and ground, located close to the power pin on the chip. This acts as a by-pass capacitor.

DC power is transferred via a surface mount type connector. To accommodate all the parasitic impedances from the elements introduced here, we separately measure the two port network impedance, and include this in the model.

A picture of the test circuit on the PCB board is shown in Fig. 2.3(b).

2.4.3 Experimental Results under Microwave Excitation

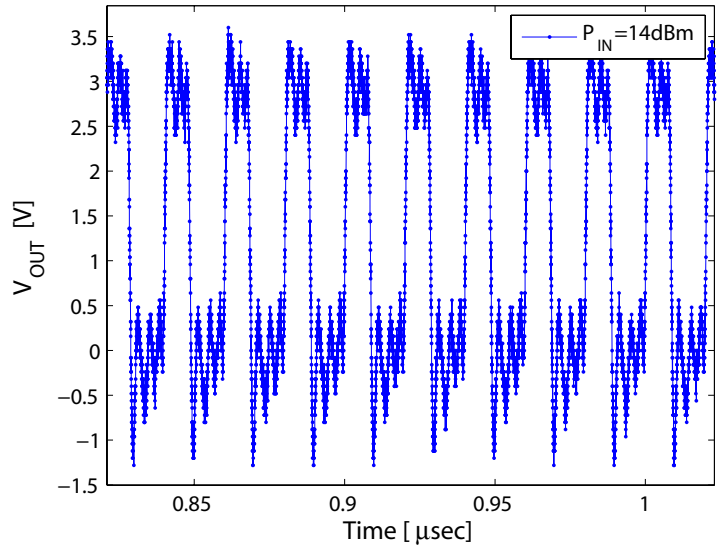
We acquire long time series data and then calculate the magnitude of the Fourier transform from them. Integrating the Fourier magnitude over a frequency window gives the power spectral density (PSD). The PSD is plotted as input RF power and frequency are varied. A high-impedance oscilloscope probe is used, having

a bandwidth higher than the maximum output frequency. The results show two distinctively different regions: a normal region and a region with possible chaotic dynamics.

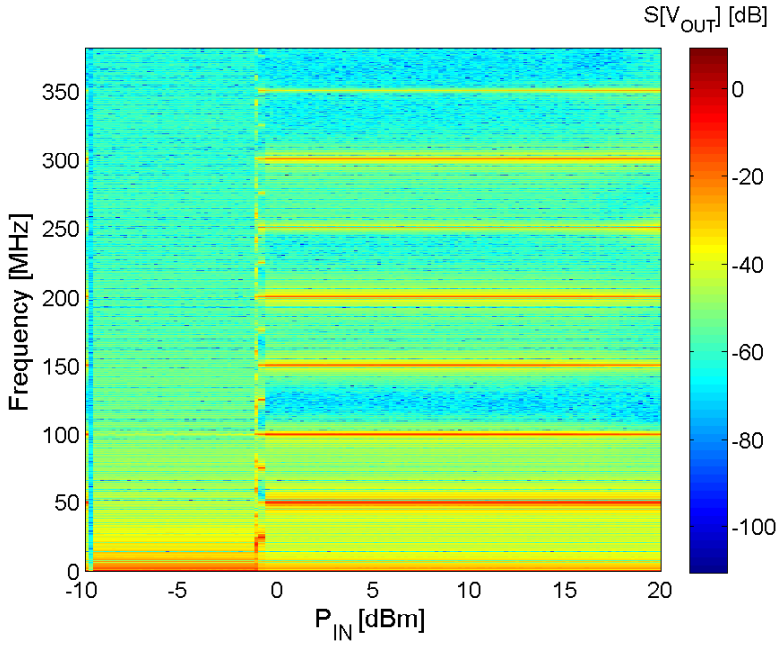
At an RF input frequency of 100MHz, the inverter operates in the normal regime. Fig. 2.11(a) shows the periodic time evolution of the output voltage. In the frequency spectrum of the signal in Fig. 2.11(b), there is a strong fundamental harmonic at 100MHz and numerous superharmonics at the integer multiples of 100MHz. When the RF frequency increases beyond the maximum oscillation frequency noted in Table 2.2, the circuit enters a possible chaotic region. Therefore, output voltages become aperiodic in the time domain, and in the frequency spectrum, numerous sub-harmonics are generated along with the fundamental harmonics, shown in Fig. 2.12(a) and (b). We observe some evidence of chaotic oscillation in Fig. 2.13, which is an enlarged view of Fig. 2.12(b). We observe a broadband power spectrum (BB) and complex spectrum.

2.4.4 Calculation of Lyapunov Exponents

Lyapunov exponents (LEs) are important parameters to quantify chaos. The largest Lyapunov exponents are often used to characterize the presence of chaotic oscillation. The technique for calculating LEs from differential equations is well-known and straightforward, introduced in many contexts [42]. However, calculating LEs for the experimental data require extra steps. Experimental data consists of only a single observable. The well-known technique of phase space reconstruction

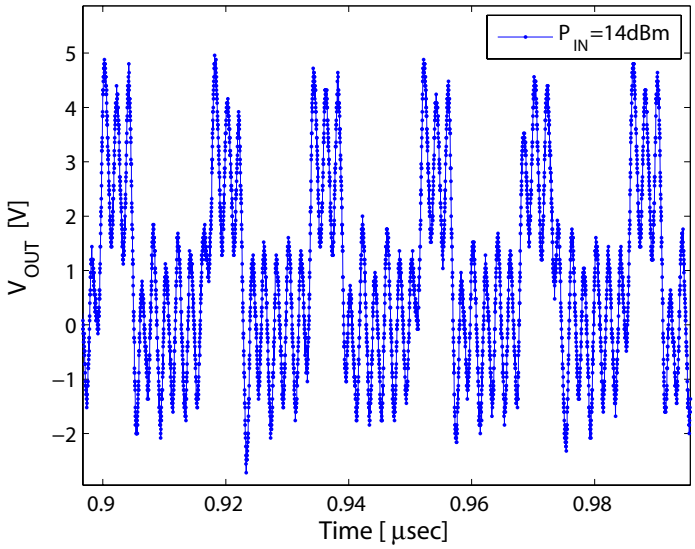


(a)

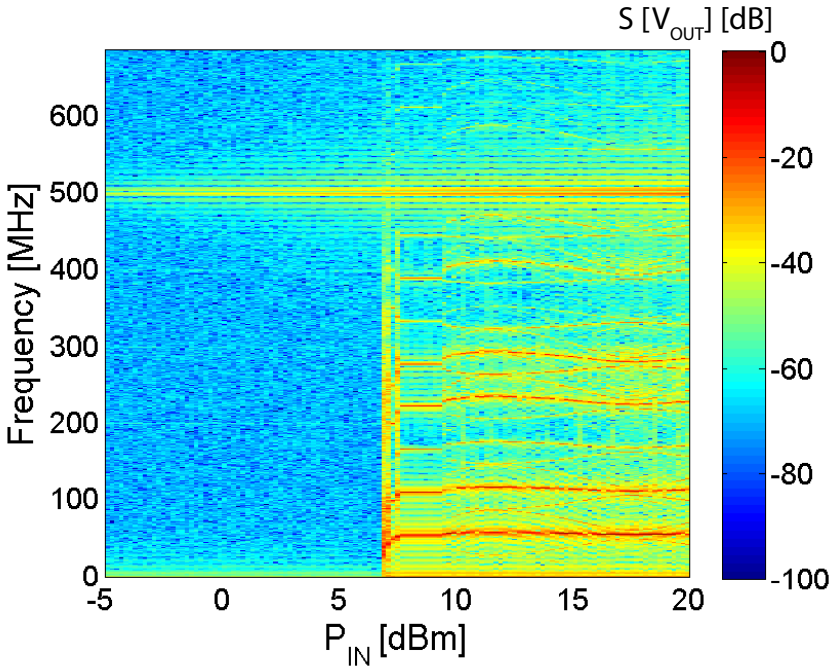


(b)

Figure 2.11: (a) Time evolution of output signal when input RF signal has power of 14 dBm and frequency of 100 MHz (b) Spectrogram of output voltage as input RF power is varied. Only the superharmonics are observed.



(a)



(b)

Figure 2.12: (a) Time evolution of output signal when input RF signal has power of 14 dBm and frequency of 500 MHz (b) Spectrogram of output voltage as input RF power is varied.

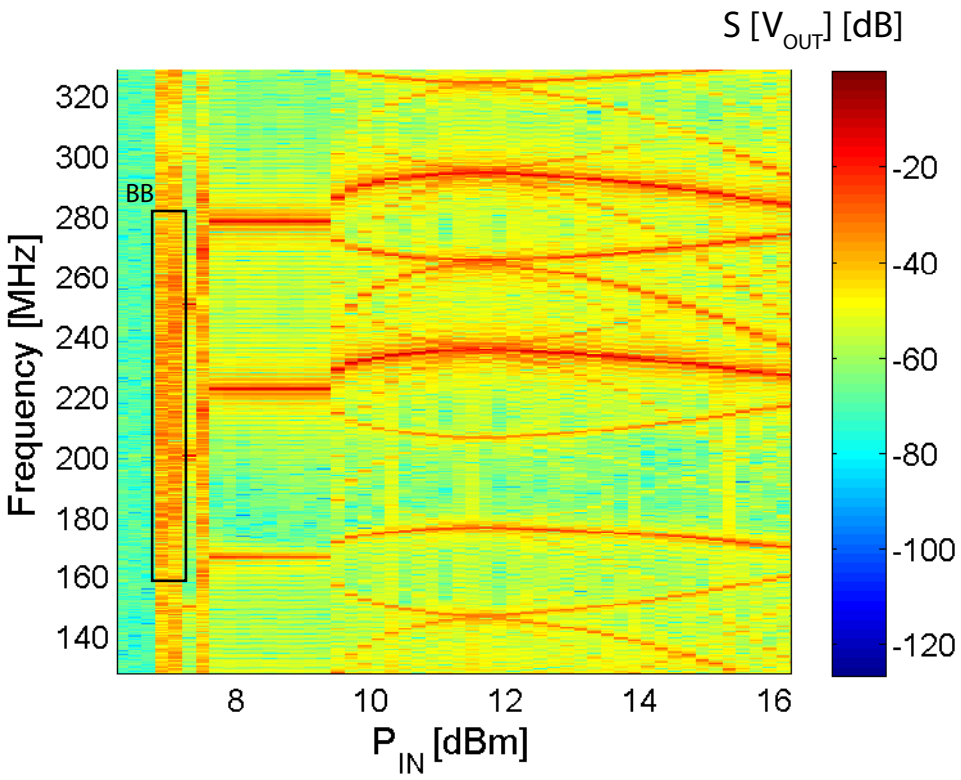


Figure 2.13: Evidence of chaotic oscillation such as complex spectrum and broadband spectrum (BB).

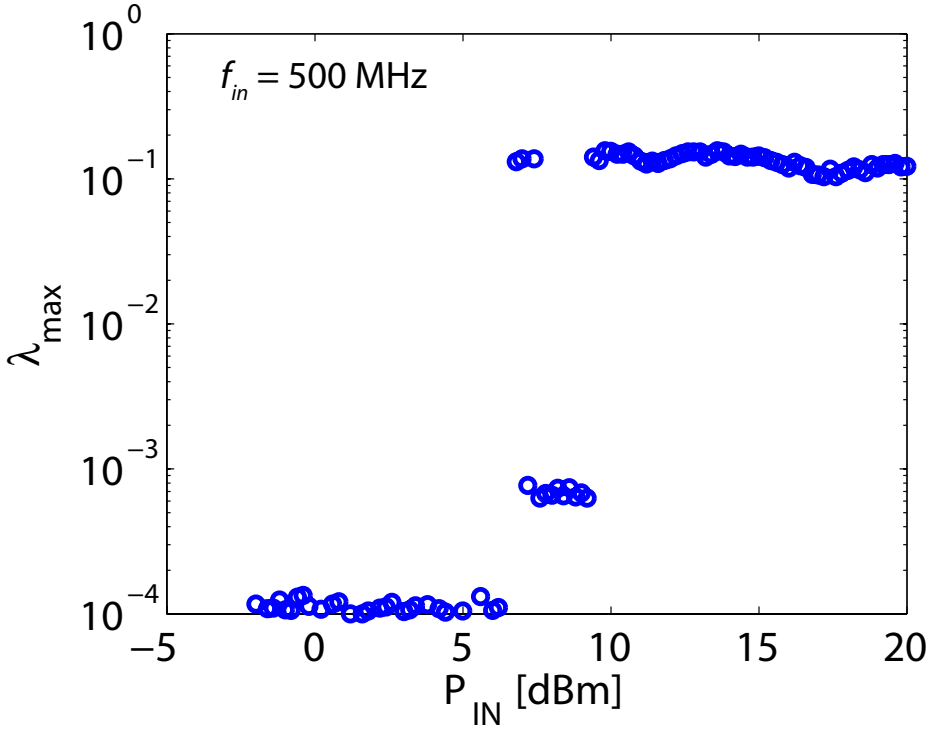


Figure 2.14: Largest Lyapunov exponents (λ_{max}) with varying P_{IN}. The measured data for each P_{IN} are calculated for λ_{max}. The circuit is driven with input RF signal with a frequency of 500 MHz, as in Fig. 2.12(b).

with the method of delay is used to correctly reconstruct the phase space. Then the nearest neighbor is found by searching for the points that minimize the distances to the reference points. More details of calculating LEs from experimental results is explained in [43].

Based on the measured time-series data, we compute the largest LEs. Fig. 2.14 shows the largest LEs when the input RF signal has a frequency of 500 MHz. The largest LEs are calculated for each P_{IN}. Positive LEs mean the signals are diverging from each other. Zero LEs indicates that the signals are periodic. Direct comparison can be made with the results shown in Fig. 2.12(b). The region with

complex spectrum shows λ_{max} with the positive numbers, whereas the other regions have λ_{max} close to zero.

2.5 Discussion : Theoretical Background of Nonlinear Sources

We now discuss analytically the nonlinear effects pertinent to our circuit. The nonlinear effects in our circuit are:

- *ESD Diode Rectification*, which causes a DC value to appear at the input of the inverter.
- *Non-quasi static Regime in PN-Junction*, which is due to a high input frequency comparable to the inverse of the reverse recovery time (t_{rr}).
- *LC Resonant Current of the Power Line.*

2.5.1 ESD-to-RFI Rectification

The RF input signal undergoes a rectification due to the ESD junction diodes, thus generating a DC offset for the inverting logic circuit. Fig. 2.15 shows the rectified DC input voltage as input frequency and the RF power changes accordingly. DC rectification is at first generated by the drain-body diode junction of the ggNMOS. As the amplitude increases, the gcPMOS also starts to rectify, resulting in a rectified DC voltage of 1.5 V. At high frequency, the symmetry of rectification breaks due to an uneven rectification efficiency of the ggNMOS and the gcPMOS. The shift in the rectified voltage is shown for higher input frequency for this reason in Fig. 2.15.

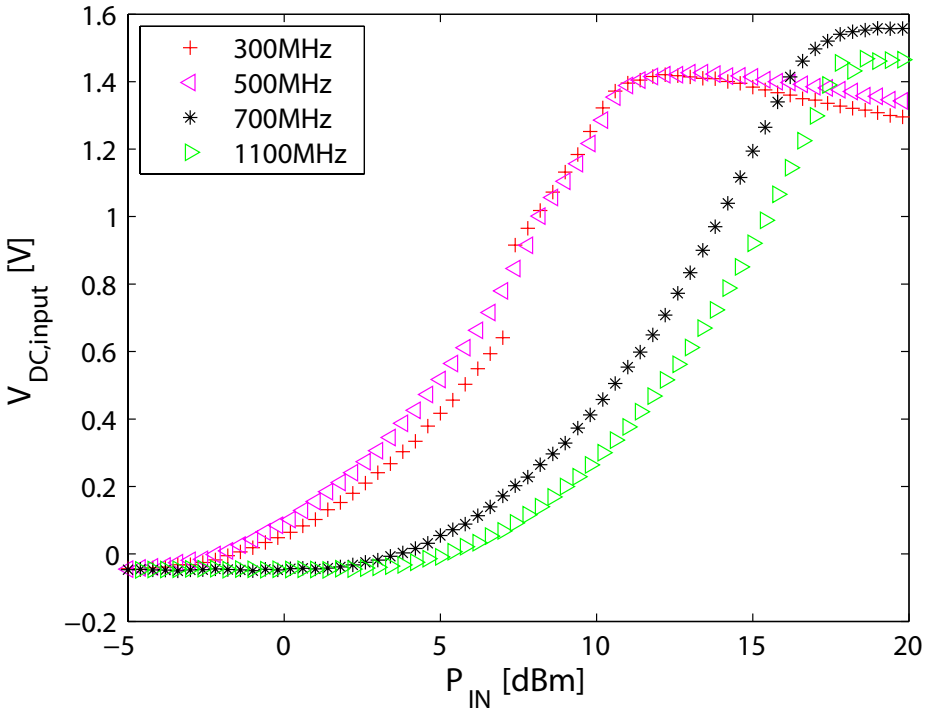


Figure 2.15: Experimental results of rectified DC input voltage (time-average values). Input voltage is measured across a large resistance connected at the bias tee. Input voltage is rectified at 1.4 V due to the rectification of ESD diodes, resulting in a DC offset at the circuit input.

We can mathematically derive the rectification of the AC signal by the PN-diode. From the well-known static diode current equation,

$$I_{diode} = I_s(e^{(V/V_T)} - 1), \tag{2.11}$$

A diode current, injected from sinusoidal RF signal, $V_o + v_{rf}cos(w_{rf}t)$, can be the equation below using Taylor expansion

$$\begin{aligned} I_{diode}(V_o + v_{rf}cos(\omega_{rf}t)) &= I_D(V_o) + v_{rf}cos(w_{rf}t)G_o(V_o) + \frac{(v_{rf}cos(w_{rf}t))^2}{2!}G'_o \\ &+ \frac{(v_{rf}cos(w_{rf}t))^3}{3!}G''_o + \frac{(v_{rf}cos(w_{rf}t))^4}{4!}G'''_o \\ &+ O(\cdot), \end{aligned} \tag{2.12}$$

where V_o is a DC term, v_{rf} is an AC amplitude, and $O(\cdot)$ is the sum of all the high-order terms for this Taylor expansion. Also, G_o is defined as the transconductance of the diode by taking the derivative of (2.11) with respect to V at one DC bias.

$$I_{diode}(V_o) = I_s(e^{(V_o/V_T)} - 1) = I_o \tag{2.13}$$

$$G_o(V_o) = \left.\frac{dI(V_o)}{dV}\right|_{V_o} = \frac{I_s}{V_T}e^{(V_o/V_T)} = \frac{(I_o + I_s)}{V_T} \tag{2.14}$$

Likewise the first derivative of G_o is

$$G'_o(V_o) = \left.\frac{d^2I(V_o)}{dV^2}\right|_{V_o} = \frac{I_s}{V_T^2}e^{(V_o/V_T)} = \frac{(I_o + I_s)}{V_T^2}. \tag{2.15}$$

Taking the time averaged value of (2.12), we get

$$\begin{aligned}\overline{I_{diode}(V_o + v_{rf}cos(\omega_{rf}t))} &= I_D(V_o) + \overline{v_{rf}cos(w_{rf}t)}G_o(V_o) + \frac{\overline{(v_{rf}cos(w_{rf}t))^2}}{2!}G'_o \\ &+ \frac{\overline{(v_{rf}cos(w_{rf}t))^3}}{3!}G''_o + \frac{\overline{(v_{rf}cos(w_{rf}t))^4}}{4!}G'''_o \\ &+ \overline{O(\cdot)}, \end{aligned} \tag{2.16}$$

where the odd terms of cos(·) becomes 0. Therefore, (2.12) simplifies to

$$\begin{aligned}I_{diode}(V_o + v_{rf}cos(\omega_{rf}t)) &= I_D(V_o) + \frac{(v_{rf}cos(w_{rf}t))^2}{2!}G'_o \\ &+ \frac{(v_{rf}cos(w_{rf}t))^4}{4!}G'''_o + O(\cdot). \end{aligned} \tag{2.17}$$

Taking only the DC terms of the diode current, the diode current from RF signal follows the square law, when an RF signal has a small amplitude, which is

$$I_{diode,DC} = I_D(V_o) + \frac{v_{rf}^2}{2! \cdot 2} \cdot \frac{I_s}{{V_T}^2} + \frac{v_{rf}^4}{4! \cdot 8} \cdot \frac{I_s}{{V_T}^2}. \tag{2.18}$$

2.5.2 Non-Quasi Static Analysis in PN-junction

Here, we examine the rectification and transient behaviors of the ESD PN-junctions. We define the non-quasi static (NQS) region of the PN-junction as follows. The quasi-static (QS) approximation for the PN-junction diode assumes that the minority carriers redistribute in a time that is short compared to the period of the RF input. Under this condition, an RF signal produces an ideal half wave rectified voltage drop. But, if the transition is very rapid, the QS breaks down, and the time it takes for the junction voltage to reach complete reverse bias must be considered. For the NQS case, the rectified voltage does not follow a square law and varies with

the input frequency. During the forward to reverse region switching, the minority carriers require a finite time to be removed. We can evaluate this effect by computing a minority carrier life time and a reverse recovery time.

Diode transients are governed by the transient in the minority carrier with respect to time. Likewise, the reverse recovery time is an important characterization parameter. The diffusion of minority carriers in the PN-junction is described by the time-dependent diffusion equation [37],

$$\frac{\partial n_p(x,t)}{\partial t} = D_n \frac{\partial^2 n_p(x,t)}{\partial x^2} + \frac{n_p(x,t) - n_{po}}{\tau_n} \tag{2.19}$$

where $n_p(x,t)$ is the minority carrier concentration, n_{po} is the minority carrier concentration at zero bias, D_n is the diffusion constant, and τ_n is the minority carrier lifetime. In our ESD junction, we assume a short-base diode approximation since the physical size of the ESD PN-junction has a short width. The minority carrier life time is defined,

$$\tau_{eff} = \frac{L_{eff}^2}{D_n} \tag{2.20}$$

where the diffusion constant is given by,

$$D_n = \frac{kT}{q}\mu_n \tag{2.21}$$

where k is Boltzmann's constant, T is temperature, and μ_n is the mobility of an electron.

For our given structure in the PN-junction, the minority carrier life time is estimated to be 234 ps for electrons and 658 ps for holes [44]. We share the same ESD protection circuit design as descirbed earlier. The numbers are different because

of the difference in electron and hole mobility. As a result of this difference, the rectification efficiency of ggNMOS and gcPMOS differs. Fig. 2.14 also demonstrates this effect by a dependence of the rectified voltage with the change in input frequency. Further analysis and details of this effect for our circuit are discussed in [44].

As the frequency becomes higher, the reverse recovery time, the time required to switch the PN junction diodes from the forward to the complete-reverse region, becomes comparable to the input frequency. For example, when the ESD diodes switch from the forward to the reverse region, minority carriers on the other side of the junction require a finite time to be removed. Under the QS regime, the reverse recovery time is very small compared to the period of the input signal. The junction will conduct only for half of the input period. Under the NQS regime, the diode will conduct more than half the period and the rectification efficiency of the diode decreases.

2.5.3 Low Frequency LC Resonant Current

A feedback current flows due to the LC path caused by the inductance of the bonding wires, and the nonlinear capacitance due to the ESD junction diodes. In addition, this feedback current usually has low frequency harmonics, whose frequency can be approximately estimated by an inverse of the product of the inductance and the nonlinear capacitance value of the ESD diodes. Since C is dependent on the voltage across the junction, the harmonic frequency varies with the applied bias. These harmonics are mixed with the fundamental driven harmonics, and these harmonics

are shown in the spectrogram in Fig. 2.12(b). When the ESD device is turned off, the resonant frequency of the LC current are higher than 3 GHz, because the equivalent capacitance of ESD device is an order of 1 pF. However, when the ESD device turns on, the resonant frequency of LC current comes down to our operating regime, since the equivalent capacitance of ESD diode becomes tens of pico farad.

2.6 Conclusions

We have effectively demonstrated in the experiment that the CMOS digital circuit shows chaotic oscillation. When there is a direct microwave excitation of a sinusoidal signal at the input, the strong aperiodicity, various bifurcations, and broadband spectrum are good indications of chaotic oscillation in this designed circuit.

We also analytically discuss the nonlinear effects in our circuit. A large RF signal is rectified, causing DC values to appear at the input of the inverter. Two other nonlinear effects are the non-quasi static regime operation of the PN-junction and a nonlinear LC resonant current.

A complete mathematical model of the feasibility of generating chaotic oscillation will follow in the next chapter. As stated above, we discuss the nonlinear effects which are a rectification of the DC signal due to the PN-junction of the ESD protection circuits, a nonlinear capacitance of the ESD protection circuits, and a generation of the low sub-harmonic components due to the coupling of parasitic inductance and nonlinear capacitance.

With mathematical modeling of the circuit, we can better demonstrate the possibility of chaotic oscillation. In the next chapter, a conceptual model, including all the nonlinearities, will be developed. We will also discuss the mathematical calculation of Lyapunov exponents, which is an efficient way of demonstrating the presence of chaotic oscillation.

Chapter 3

Modeling of Chaotic Oscillation in CMOS Digital Circuits

3.1 Overview

In the last chapter, we have demonstrated the experimental evidences of chaotic oscillation. Based on the discussion on the source of nonlinearity, here, we would like to build a numerical model to find chaotic oscillation in the given structure. In other words, the experimental evidence of chaotic oscillation such as the aperiodicity, bifurcations, and broadband power spectrum were a very good suggestion that the chaotic oscillation can occur in the driven CMOS inverter structure. By the definition of chaos requires the signal to be aperiodic and sensitive to initial conditions, and has to be deterministic, which means outputs are predictable from inputs.

The experimental results in the previous chapter suggest the presence of chaotic oscillation in our circuits. However, more mathematical evidence is needed to prove the existence of chaotic oscillation. Through building a mathematical model, we can prove the deterministic nature of chaotic oscillation as well as its sensitivity to initial conditions. In the numerical model, we intend to introduce all the nonlinearities discussed above.

In addition, compact modeling with the correct SPICE parameters is performed to build a model to predict the RF onset of chaotic oscillation. SPICE

modeling is useful in circuit design in predicting and modeling results of the actual circuits. There have been many developments in SPICE parameters to have a good match with the measured data. One of the standard transistor models is the Berkeley Short-channel IGFET Model (BSIM), and it has been proven to be valid in high speed operations up to several tens gigahertz. We intend to build a model that can predict the region of chaotic oscillation using BSIM parameters and additional features.

In Section 3.2, a transistor-based simulation is performed to predict the onset of microwave amplitude when the circuit enters the chaotic region. We explain the theoretical background of BSIM models and the simulation.

In Section 3.3, we discuss the derivation of a mathematical model. We review the nonlinear equations included in this model, and we compute the largest Lyapunov exponents to validate the presence of chaotic oscillation found in the previous chapter.

3.2 Transistor-Based Simulation : Compact Modeling

3.2.1 Non-Quasi Static features in the BSIM model

Recently, many traditional models for a MOSFET device have started to fall behind, since the operating frequency of the system has begun to enter the regimes close to their threshold or cutoff frequency limits. In other words, parameters or equations have to be modified to maintain good device models. There has been many efforts to improve current state-of-the-art models, mainly by introducing more

nonlinearities.

Among many accurate MOSFET device models, the Berkeley Short-channel IGFET Model (abbreviated as BSIM) has become an industry standard for both analog and radio frequency circuits. Here, we are interested in the non-quasi static nature of this model, and how this NQS features in the BSIM agree with the experimental results, described previously. A NQS region is defined by circuit operation near cut-off frequency or under a very rapid transient operation. Before comparing the simulation and experiment results, we introduce the developments of the BSIM in terms of NQS model.

BSIM3, published in [45], includes a basic NQS model, called the charge-deficit NQS model. Fig. 3.1 explains the basic operation of NQS models. R_{elmore} and $C_{(s,d)g}$ are added to model accurately the finite time for the channel charge to build-up. Both the transport and charging components of channel charges can be written as

$$I_{D,G,S}(t) = I_{D,G,S}(DC) + \frac{\partial Q_{d,g,s}(t)}{\partial t} \tag{3.1}$$

An internal node, Q_{def} is created to keep track of the amount of deficit and surplus channel charge necessary to reach equilibrium.

BSIM4 includes not only the features described above, but also a gate electrode and intrinsic-input resistance model and a substrate resistive network. The gate electrode model considers the relaxation time effect due to the distributive RC nature of the channel. This is more or less identical to the charge deficit NQS model of BSIM3.

Another important NQS feature is the substrate resistance network. It is

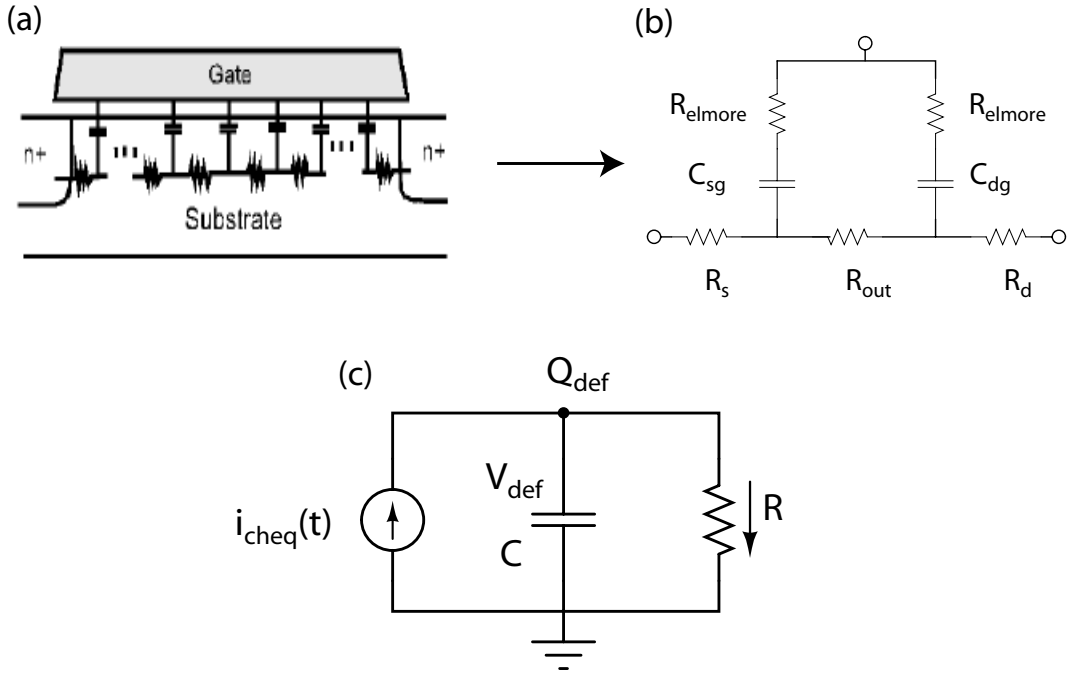


Figure 3.1: (a) Diagram of charge-deficit Non-Quasi-Static model. (b) Diagram shows an equivalent network for the channel of MOSFET. (c) NQS sub-circuit for transient analysis.

essential to consider the high frequency coupling through the substrate for RF circuit simulation. In short, this feature allows an accurate model of reverse recovery time. Fig. 3.2 describes the resistive network of the substrate to the channel coupling.

For accurate simulation, MOSIS provides the list of BSIM parameters after fabrication. The full list of BSIM parameters is attached in Appendix A. To turn on the NQS features described here, the model selectors, such as *trnqsMod* and *rbodyMod*, are turned on. In addition to the NQS features in the BSIM MOSFET device, we add the two port network parameters in the simulation. This linear parasitic elements can give rises to resonances, which may influence the input voltage.

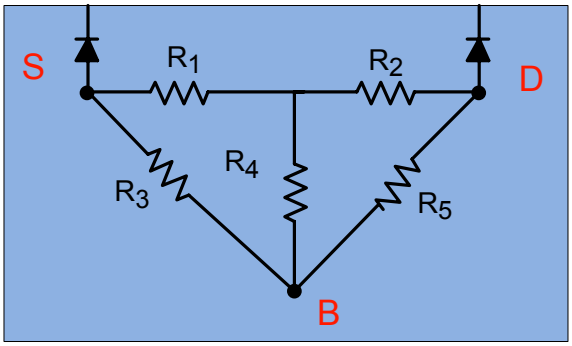


Figure 3.2: Diagram for Berkeley Short-channel IGFET Model 4 substrate resistance network, which models non-quasi static region. This resembles a reverse recovery time of ESD junction diodes during switching.

The parasitic impedances includes the ball bond wires, PCB traces, lead frames, and impedance introduced from the experimental apparatus. This effect is more pronounced as the operating wavelength becomes comparable to the lumped elements.

3.2.2 Simulation Results

With the commercial software tool, Agilent Advanced Design System (ADS), we perform a harmonic balance simulation on the circuits. A harmonic balance (HB) simulation allows us to perform time and frequency domain analysis over varying circuit parameters simultaneously. This HB simulation is widely used in calculating the steady state solutions for the RF circuits containing nonlinear components. The Fourier series can represent periodic voltages and currents in circuits as the summation of harmonics.The HB method works for a circuit that can be separated

into linear and nonlinear portions. The advantage of harmonic balance is that the node voltages for all the linear elements are calculated in the frequency domain, while nonlinear elements are calculated in the time domain. In addition, the HB simulation allows us to look at time and frequency analysis over varying parameters with the faster simulation time. However, the detailed transient oscillation of the circuit can only be observed by transient simulation with fine and accurate time steps and a long simulation time. Besides, the HB simulation allows an inclusion of the supplementary custom models to accurately simulate the circuit such as S-parameters of parasitics. The input to the nonlinear circuit is treated as

$$v_{in}(t) = Real\left[\sum_{k=0}^{K} V_k \exp(j2\pi kft)\right], \tag{3.2}$$

where f is the fundamental frequency of the input, the V_k is the complex Fourier coefficients, the K is the order of harmonics.

Here, we measure the scattering parameters for the input linear parasitics mentioned in the previous section for the true input voltage to the circuit. We design the same PCB board without the DUT and measure 2 port scattering parameters in order to observe S_{21}, the forward transmission coefficient, and S_{11}, the forward reflection coefficient. The scattering parameters are complex values at each frequency point, measured from the network analyzer. Fig. 3.4 plots the measured S_{21} and S_{11}.

This result corresponds to Fig. 3.5, which shows a resonance around 700 MHz when the input RF power is 10 dBm.

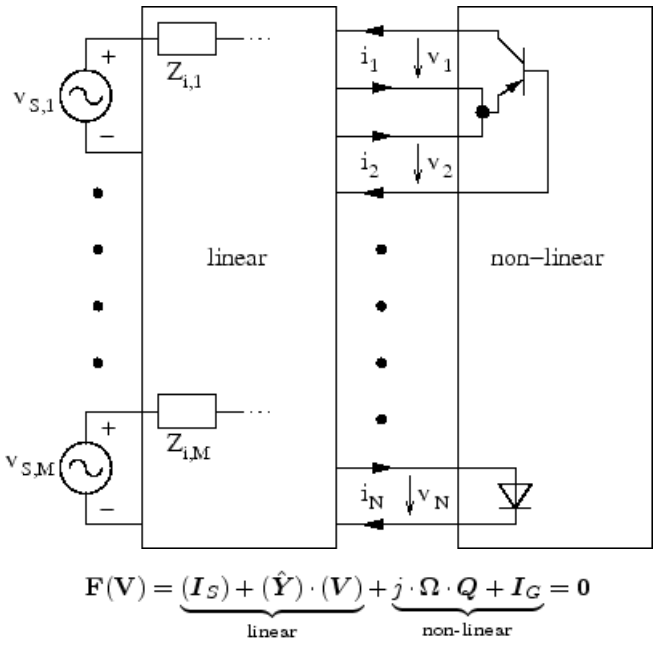


Figure 3.3: Schematic diagram explaining how the harmonic balance simulation operates. $F(V)$ solves the nonlinear and linear parts separately. Y is the transadmittance matrix for the linear parts, and Q and I_G are the frequency-domain factors for the nonlinear circuits.

This effect of linear parasitic impedances from the traces in the PCB, and bond wires in the chip package, can be significant to generating extra harmonic components. Usually, when we design circuits operating at high frequency, it is common practice to build passive matching circuits. However, for the case of external microwave excitation, the input is not perfectly matched to the correct frequency.

Fig. 3.6 is a complete circuit diagram for the simulation. There are two device models used in this circuit simulation - BSIM4 and BSIM3. Because the BSIM4 features the NQS features explained previously, we set the ESD protection circuits with BSIM4. The current version of BSIM4 consists of both the charge-deficit model and substrate resistive network model, whereas the BSIM3 consists of only

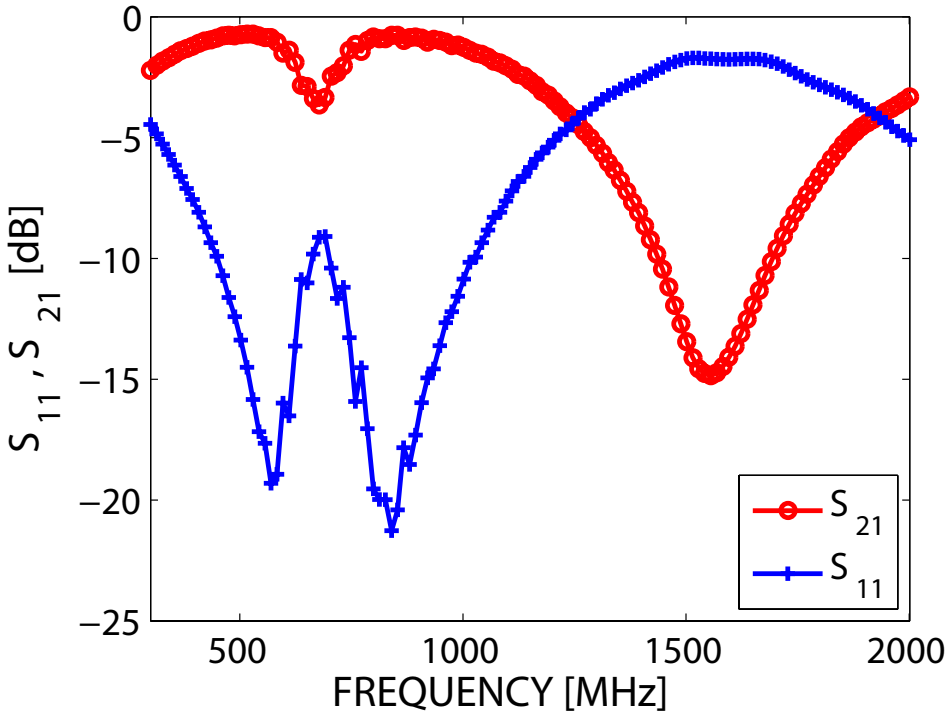


Figure 3.4: Forward transmission coefficient S_{21} (red) and forward reflection coefficient S_{11} (blue). Notice there is a 4dB decrease in S_{21}, meaning less than half of input power is transmitted at the frequency around 700 MHz.

the charge-deficit model. The rest of the transistors are modeled with BSIM3. At the input the circuit, we include the measured scattering parameters. The harmonic balance simulation is performed along with the parametric sweep on the fundamental input frequency.

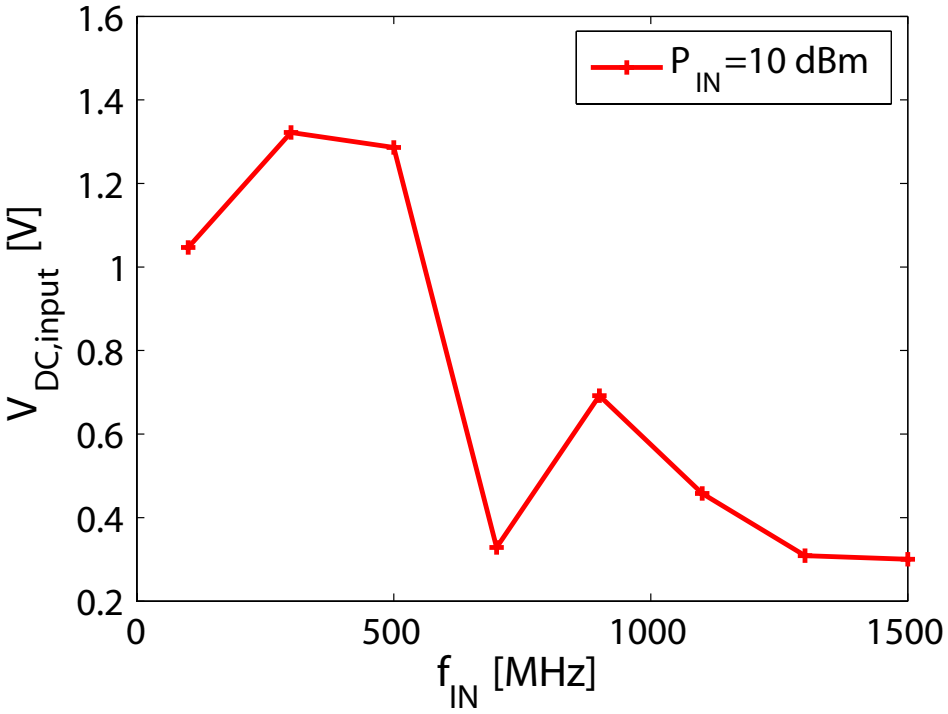


Figure 3.5: DC detected input voltage as frequency of input is changing and RF amplitude is fixed at 10 dBm. The trough around 700 MHz corresponds with the decline of forward transmission coefficient in Fig. 3.4

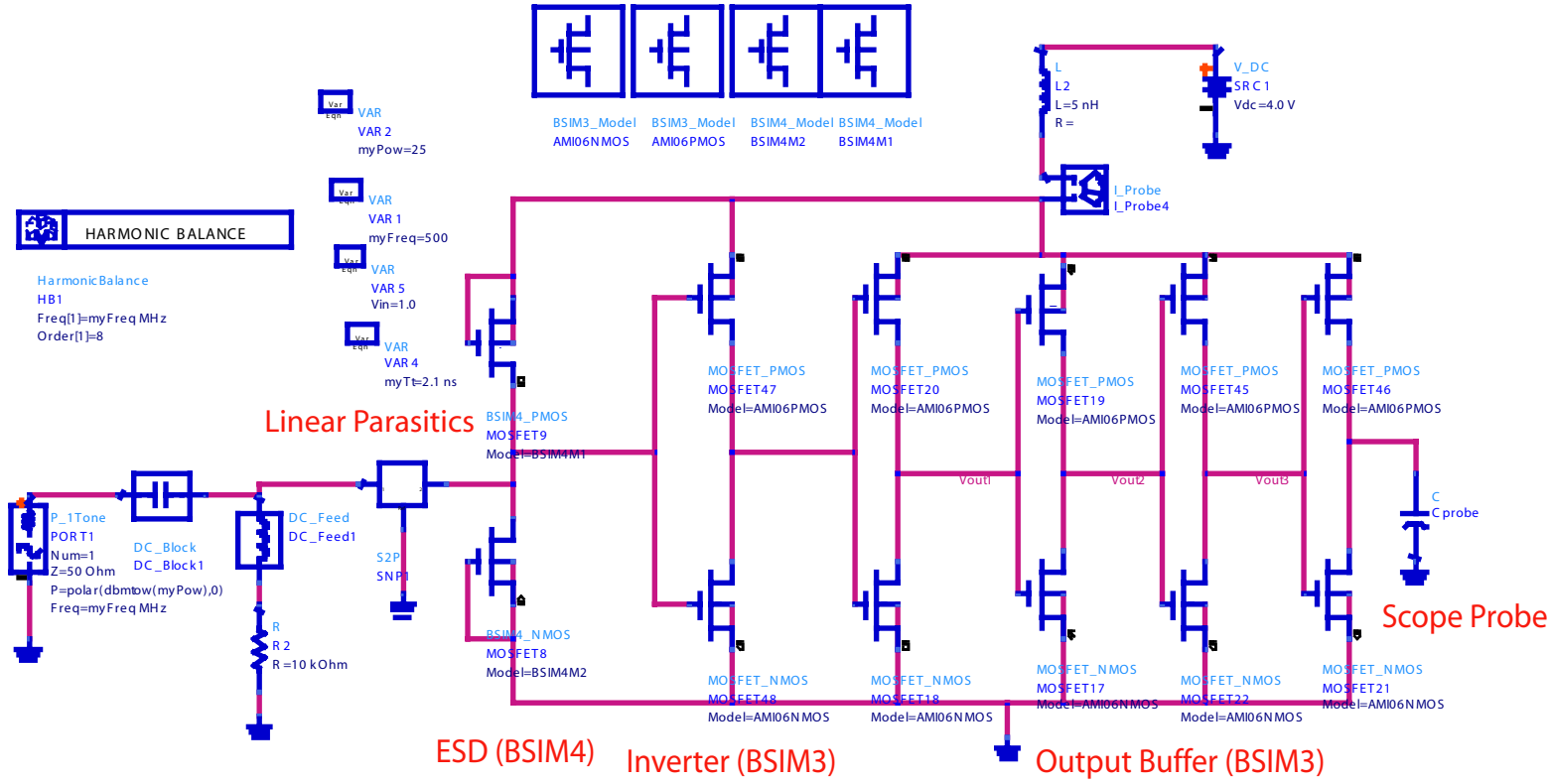


Figure 3.6: A complete schematic created with ADS software. The BSIM 4 model is included as well as the input parasitic model. The BSIM SPICE parameters are extracted from test results provided from the foundry.

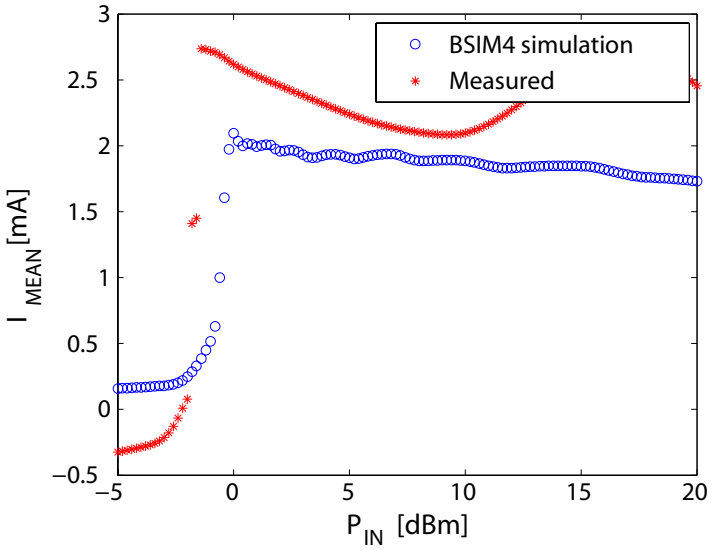
Another comparison between experimental and simulation results is the rise of supply current when there is a chaotic oscillation. There are noticeable agreements between mean supply currents and RF power onsets of chaos bifurcation. Fig. 3.7 shows time-averaged supply currents for a normal regime and a chaotic regime. In both the experimental and simulation results, the supply current starts to increase above a certain RF power. A clear distinction between two cases is that a mean supply current in the chaotic regime increases higher than the peak current in Fig. 2.5, whereas the mean current in the normal regime is kept within the peak current in Fig. 2.5.

A disagreement is noticeable in the high RF power region of the chaotic case. This is because the NQS effect of the PN junction is not correctly modeled in BSIM4. The NQS effect of channel charging and discharging time of MOSFET is correctly modeled in BSIM4, but the NQS effect in the PN-junction inside a MOSFET is not. We still require further investigations on the mismatching between the simulation and the measured. However, we are able to predict the onset of chaotic oscillation, and this is very important if one wants to build a system resistant to chaotic oscillation.

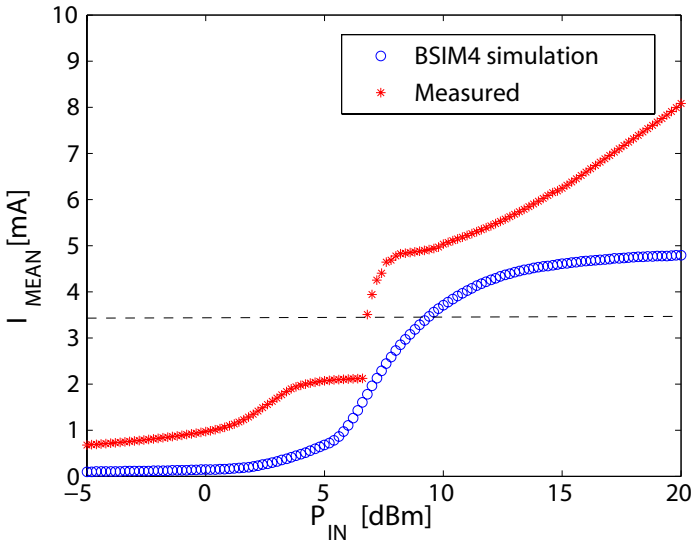
3.3 Ordinary Differential Equations : Numerical Modeling

3.3.1 Nonlinear Sub-Functions in ODEs

Traditionally, ordinary differential equations (ODEs) are important tools to describe chaotic dynamics in a circuit. Setting up an ODE model allows one to



(a)



(b)

Figure 3.7: Comparison of experimental and simulation results of time-averaged DC supply current as RF power is varied for input drive frequency of (a) 100 MHz (Linear regime) and (b) 500 MHz (NQS regime). The simulation accounts for the BSIM4 NQS feature and reflective impedance. Notice the jumps at 7 dBm appears both in experiment and simulation. Supply current never exceeds DC peak current 3.5 mA (dotted line) for (a) but supply current exceeds DC peak current as it enters the chaotic region in (b). Such comparison can also be made for Fig. 2.12, in terms of RF power onset of chaotic oscillation.

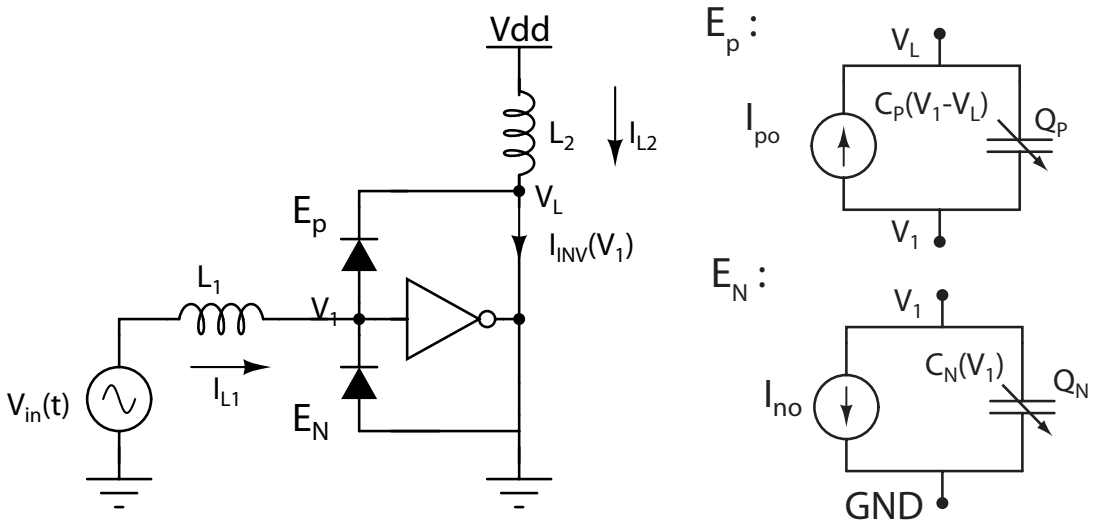
examine the sensitivity of the output signal to small changes in initial conditions, via Lyapunov exponents. In addition, to characterize the deterministic of the signal, setting up a predictable model is a good practice. In general, for N first-order autonomous ODEs, N has to be greater than or equal to three in order for chaos to be possible [42]. The model may not reflect the exact design of the actual circuit, but the basic nonlinearities discussed in Section 2.3 are included in order to represent the source of chaotic oscillation. The purpose of the mathematical model is to prove the presence of chaotic oscillation in this dynamical system.

Here, we simplify the circuits above into Fig. 3.8, which includes the basic elements of the nonlinearities, and write down the circuit equations based on nodal analysis and charge analysis. The global parameters are power supply voltage, fixed at 4 V, and parasitic inductance L_1 and L_2. There are four state variables, including V_1, V_L, I_{L1}, and I_{L2}. The flowchart in Fig. 3.9 explains the general algorithm of the numerical modeling.

The nonlinear equations for these nonlinear functions, such as nonlinear capacitance of diodes, rectification of AC signals, short current of the CMOS inverter, and dynamic current of ESD circuit, are all included in building these numerical equations. First, the nonlinear transfer function of a CMOS inverter is described by

$$I_{INV} = \frac{2I_{MAX}}{1 + exp(\frac{(V_{IN}-1.5)^2}{\alpha})}, \tag{3.3}$$

where I_{MAX} and α are fitting parameters. Second, the nonlinear dynamics of ESD switching is described by the sum of the static diode current and the dynamics



(a) (b)

Figure 3.8: (a) Simplified circuit diagram of a CMOS inverter coupled with ESD circuits for numerical modeling. $L_{1,2}$ is an equivalent parasitic impedance around 5 nH. (b) Dynamics of ESD protection circuit for gcPMOS and ggNMOS.

current due to nonlinear capacitances as shown in Fig. 3.8(b).

$$I_{P,N} = I_{P0,N0} + C_{P,N} \cdot \frac{dV}{dt} \tag{3.4}$$

The nonlinear capacitances $C_{P,N}$ are measured using a quasi-static technique, provided by a semiconductor parameter analyzer [46], and used a mathematical fitting method to illustrate the nonlinearity as (3.5),

$$C_{P,N} = \begin{cases} C_0 \cdot exp(V/\beta) & \text{V} > 0 \\ C_0 & \text{V} < 0. \end{cases} \tag{3.5}$$

where C_0 and β are fitting parameters. Then, the model is able to capture the rectification of the AC signal due to the ESD diode. The mathematical derivation

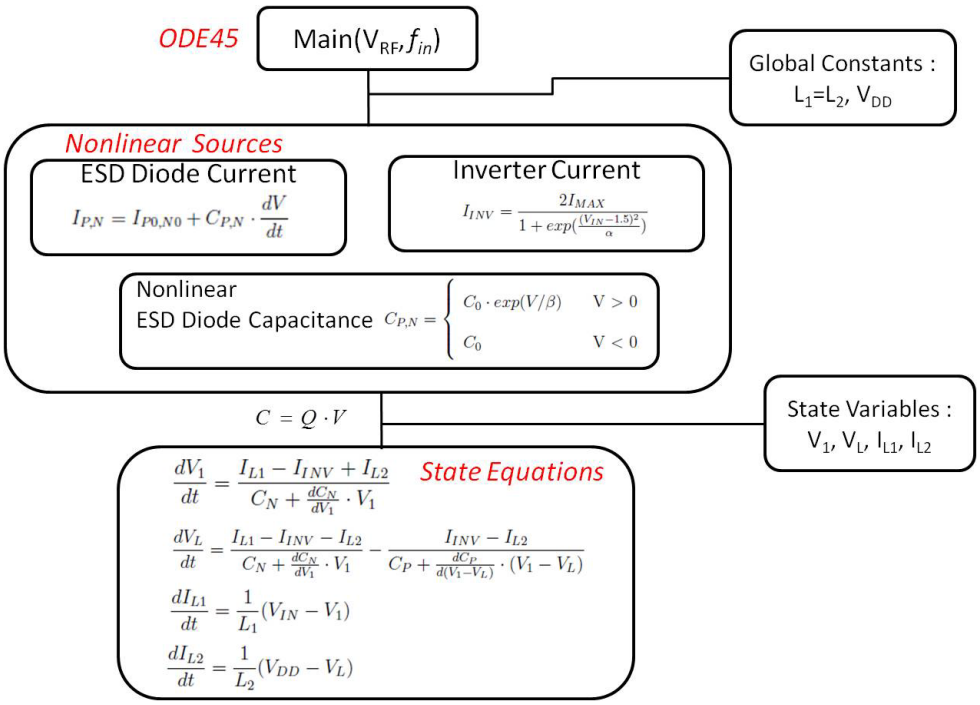


Figure 3.9: Flowchart for numerical modeling. The system of ODE is solved using 4th order Runge-Kutta method with the nonlinear source listed, such as nonlinear diode equations, nonlinear transconductance of the inverter, and nonlinear ESD diode capacitance.

of this rectification is validated in numerous papers [34]. However, we did not include the DC bias shift effect due to a NQS nature of PN-junction diodes here, also discussed in Chapter 2. In the an actual circuit, DC rectified voltage changes with the frequency of the input RF signal.

To write down the ODE, the state variables are first defined as V_1, V_L, I_{L1}, I_{L2}, Q_P, and Q_N. Notice that Q_P and Q_N are eliminated during the later part of derivations, thus the problem becomes a first-order system of four coupled ODEs.

To begin, the charges on one of the nonlinear ESD capacitances are described as,

$$Q_P = C_P \cdot (V_1 - V_L), \tag{3.6}$$

where Q_P is a charge across the nonlinear capacitance C_P, and V_1 and V_L are the voltages at the input and power source, respectively. Taking time derivatives on both sides and using the chain rule,

$$\frac{dQ_P}{dt} = \frac{dC_P}{dt} \cdot (V_1 - V_L) + C_P \cdot \frac{d(V_1 - V_L)}{dt} \tag{3.7}$$

$$= \frac{dC_P}{d(V_1 - V_L)} \cdot \frac{d(V_1 - V_L)}{dt} \cdot (V_1 - V_L) + C_P \cdot \frac{d(V_1 - V_L)}{dt}. \tag{3.8}$$

Thus, the dynamic part of I_P becomes

$$I'_P = [C_P + \frac{dC_P}{d(V_1 - V_L)}(V_1 - V_L)] \cdot (\frac{dV_1}{dt} - \frac{dV_L}{dt}). \tag{3.9}$$

Additionally, the charges on the bottom nonlinear ESD diode capacitance are written as

$$Q_N = C_N \cdot (V_1 - 0), \tag{3.10}$$

where Q_N is a charge across the nonlinear capacitance C_N. Again, taking time derivatives on both sides and using a chain rule.

$$\frac{dQ_N}{dt} = C_N \cdot \frac{dV_1}{dt} + \frac{dC_N}{dt} \cdot V_1 \tag{3.11}$$

$$= C_N \cdot \frac{dV_1}{dt} + \frac{dC_N}{dV_1} \cdot \frac{dV_1}{dt} \cdot V_1. \tag{3.12}$$

Thus, the dynamic part of I_N becomes

$$I'_N = \frac{dV_1}{dt} \cdot (C_N + \frac{dC_N}{dV_1} \cdot V_1). \tag{3.13}$$

As mentioned earlier, the total ESD diode current $I_{P,N}$ becomes a sum of the static diode current $I_{P0,N0}$ and the dynamic current $I'_{N,P}$

$$I_{P,N} = I_{P0,N0} + I'_{P,N}, \tag{3.14}$$

where a static diode current follows

$$I_{P0,N0}(V) = I_s(e^{(V/V_T)} - 1). \tag{3.15}$$

Then, (3.13) can be converted to

$$\frac{dV_1}{dt} = \frac{I_N}{C_N + \frac{dC_N}{dV_1} \cdot V_1}. \tag{3.16}$$

After substituting (3.16) into (3.9), (3.9) becomes,

$$\frac{dV_L}{dt} = \frac{I_N}{C_N + \frac{dC_N}{dV_1} \cdot V_1} - \frac{I_P}{C_P + \frac{dC_P}{d(V_1 - V_L)} \cdot (V_1 - V_L)}. \tag{3.17}$$

Using node equations (3.18) and (3.19), (3.16) and (3.17) can be further simplified to (3.20) and (3.21).

$$I_P + I_{L2} = I_{INV} \tag{3.18}$$

$$I_{L1} = I_P + I_N \tag{3.19}$$

$$\frac{dV_1}{dt} = \frac{I_{L1} - I_{INV} + I_{L2}}{C_N + \frac{dC_N}{dV_1} \cdot V_1} \tag{3.20}$$

$$\frac{dV_L}{dt} = \frac{I_{L1} - I_{INV} - I_{L2}}{C_N + \frac{dC_N}{dV_1} \cdot V_1} - \frac{I_{INV} - I_{L2}}{C_P + \frac{dC_P}{d(V_1 - V_L)} \cdot (V_1 - V_L)} \tag{3.21}$$

Lastly, the two current equations are

$$\frac{dI_{L1}}{dt} = \frac{1}{L_1}(V_{IN} - V_1) \tag{3.22}$$

$$\frac{dI_{L2}}{dt} = \frac{1}{L_2}(V_{DD} - V_L). \tag{3.23}$$

3.3.2 Simulation Results

(3.20), (3.21), (3.22), and (3.23) give us a system of four ODEs that can be numerically solved by the fourth-order Runge-Kutta method (RK4). MATLAB contains a built-in function called $ODE45$, to solve ODEs, with the RK4 method. We plot for the load voltage (V_L) in the time domain in Fig. 3.10 (a) and (c). This shows a clear distinction between periodic and chaotic signals. Fig. 3.10 (b) and (d) show the delay phase space diagrams, correspondingly. In Fig. 3.10(b), the phase space diagram evolves around a fixed point, but in Fig. 3.10(d), a chaotic attractor is shown.

To observe changes in the circuit's dynamics, we plot the spectrogram of output voltages as the input RF power varies in Fig. 3.11. We observe the broadband spectrum at the region around 11 dBm. We can make a direct comparison with the results shown in Fig. 2.12(b). Both spectrogram show broadband and compex spectrums. However, there is a disagreement in two parts. First, in Fig. 3.11, the circuit exhibits the broadband spectrum after the RF power becomes 11 dBm,

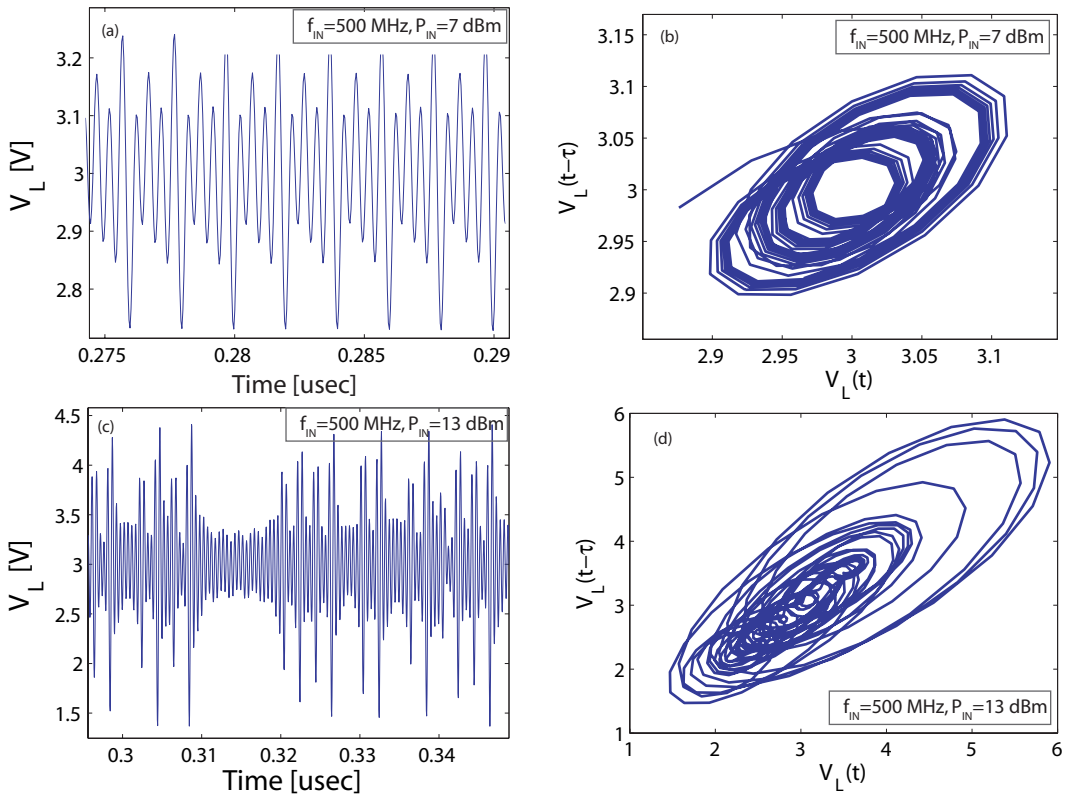


Figure 3.10: (a) Time evolutions of load voltage V_L (b) Delay phase space diagram, when the circuit is excited by the input RF signals with the frequency of 500MHz and RF power of 7 dBm. (c) Time evolutions of load voltage V_L (d) Delay phase space diagram, when the circuit is excited by the input RF signals with the frequency of 500MHz and RF power of 13 dBm.

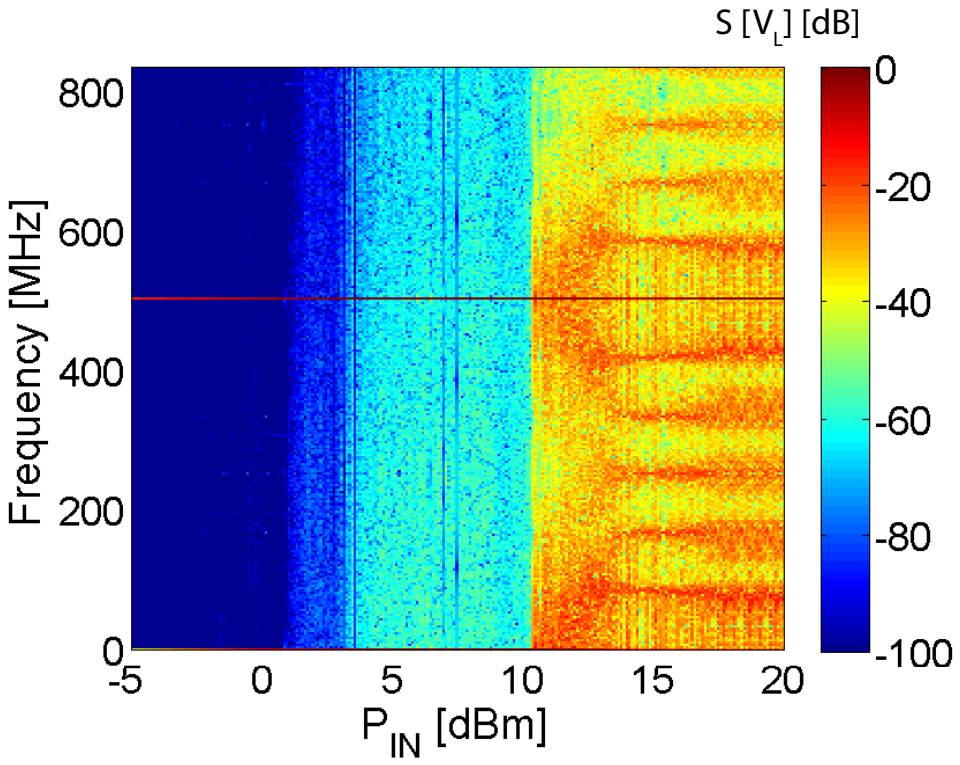


Figure 3.11: Numerical results of spectrogram of load voltage, when the circuit is excited by input RF signal with a frequency of 500 MHz as RF power is varied.

whereas the experimental result shows the onset around 7 dBm. Second, the exact circuit dynamics do not match between the time domain signals.

3.3.3 Calculation of Lyapunov Exponents

Another way to verify the existence of chaotic oscillation is to check whether nearby trajectories separate exponentially fast, at least while the distance between them is small [47, 43]. The hypothesis we want to check is whether the average distance (δ) between trajectories (j) obeys (3.24) after i discrete time steps. Slopes of logarithmic distance indicate the Lyapunov exponents (LE) after numerically

computing several nearby trajectories with small deviations in initial conditions. Positive LEs mean the signals are diverging from each other, which is a chaotic oscillation. Negative LEs mean that the signals are converging, and a zero LE indicates that the system is in a steady state mode. The largest Lyapunov exponent (λ_{max}) is defined by (3.26) using a least-square fit method, averaged over many nearby trajectories. Fig. 3.12 shows the the calculation of the largest LEs when the circuit is driven by an input RF signal with a frequency of 500 MHz and a RF power of 11 dBm.

$$\delta_j(i) = C_j \cdot exp(\lambda_1 \cdot (i\Delta t)) \tag{3.24}$$

$$\ln(\delta_j(i)) = \ln(C_j) + (\lambda_1 \cdot (i\Delta t)) \tag{3.25}$$

$$\lambda_{max} = \lim_{\delta \to 0} \left\langle \frac{\partial \ln \delta}{\partial t} \right\rangle_j \tag{3.26}$$

3.4 Summary

We developed a mathematical model for the CMOS inverter, driven under microwave excitation. This mathematical model is developed not to compare with the experimental results, but to prove mathematically that chaotic oscillation occurs in a simple CMOS digital circuit under such circumstance. Although this model is only a behavior model, it is valid because it includes the basic nonlinear dynamics discussed in the last chapter. This ODE model is used in computing the chaotic

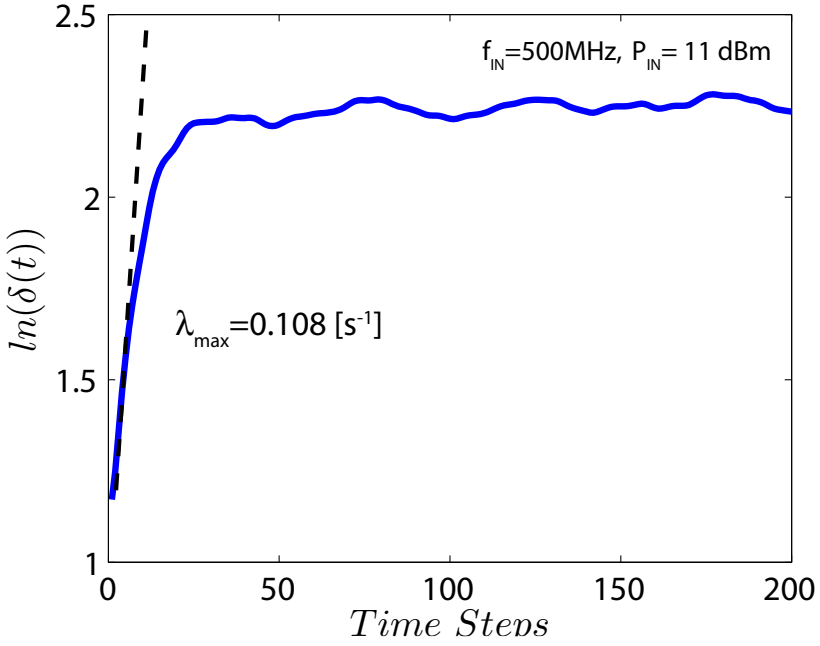


Figure 3.12: Average logarithmic distance between trajectories corresponding to Fig. 3.10(b). The initial positive slope (the positive largest Lyapunov exponent) and a long time saturation of the average distance indicate chaotic dynamics.

dynamics, especially the largest Lyapunov exponents. In addition to a mathematical model, we develop a compact model based on transistors. In this compact modeling, we include the BSIM transistor model, and the linear parasitic input impedance at the input of microwave signal injection. From this compact modeling, we can predict the RF amplitude at which the circuit enters the chaotic region.

Chapter 4

Design of On-Chip CMOS Boolean Chaotic Oscillator

4.1 Overview

In Chapters 2 and 3, we discussed chaotic oscillation as a means of upset in the CMOS integrated circuit (IC). To secure stability of CMOS ICs under electromagnetic interference, it is important to understand the circuit dynamics generating chaotic oscillation. Chaotic oscillation is detrimental to circuit stability, and may lead to a temporary reset or freezing of the circuit. On the other hand, chaotic oscillation in CMOS ICs has expanded its use in various applications, one being random number generation. More details on the random number generator is introduced in next chapter, and here, we would like to focus on new mechanism of generating chaos, Boolean Chaos, and its implementation using CMOS technology.

Among many sources of generating chaotic oscillators, Boolean chaos [25] is a phenomenon in an autonomous network which shows a high dimensional chaotic oscillation, exponential sensitivity to initial conditions, and has a broadband power spectrum. This unique behavior was first described by a group of mathematicians, using a Boolean delay equation [30]. The circuit node includes Boolean-like state transitions with a fast transition time and a feedback loop with incommensurate delay inputs that lead to Boolean chaotic oscillation. Another advantage we envision in this Boolean chaotic oscillator is that an integrated circuit (IC) can be implemented

with an all transistor-based circuit, which is more compatible to a system-on-chip solution for cryptographic application, compared to other previously developed IC chaotic oscillators.

In Chapter 4 and 5, we report on a random number generator whose randomness originates from a Boolean chaotic oscillator, designed and fabricated as an integrated circuit. According to numerical analysis of the Boolean delay equation, a single node network generates chaotic oscillation when two delay inputs are incommensurate numbers and transition time is fast. To test this hypothesis physically, a discrete Boolean chaotic oscillator is implemented. Using CMOS 0.5 μm process, a CMOS Boolean chaotic oscillator is built, which consists of a core chaotic oscillator and a source follower buffer. Chaotic dynamics are verified using time and frequency domain analysis, and maximum Lyapunov exponents are calculated. The quality of the measured bit sequences is verified for a feasible randomness source, using NIST standard statistical tests after subsequent post-processings.

Our approach in building this RNG IC is first to test the mathematical hypothesis that chaotic oscillation occurs as described by the Boolean delay equation via numerical modeling. Then, we build a prototype circuit to test the nature of the Boolean chaotic oscillator, and then we design this Boolean chaotic oscillator using integrated circuit technology.

In Section 4.2, we focus on the numerical analysis of Boolean chaos, identifying the mathematical conditions for which chaotic oscillation is generated.

In Section 4.3, we test our hypothesis using discrete parts.

In Section 4.4, we design the CMOS Boolean chaotic oscillator with the con-

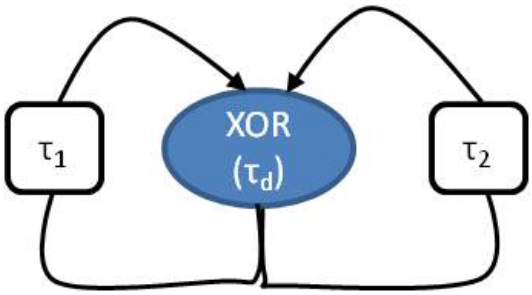


Figure 4.1: Example of Boolean Chaos. Two delays (τ_1 and τ_2) are inputs of XOR with response time (τ_d).

ditions tested in previous sections and analog circuit design.

4.2 Numerical Analysis of Boolean Chaos

The mathematical description from the Boolean delay equation [30] has led us to believe that chaotic oscillation is generated from an autonomous Boolean network, with n state nodes in (4.1).

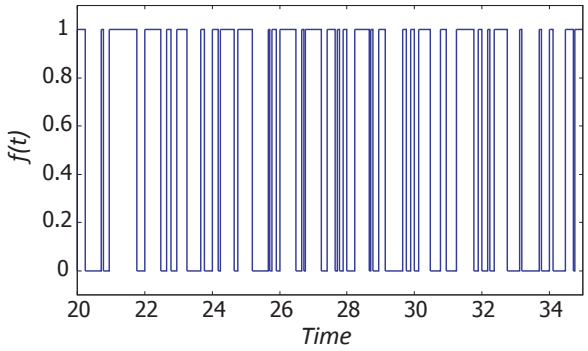
$$x_n(t) = f_n[t, x_1(t-\tau_{n1}), x_2(t-\tau_{n2}), \ldots, x_n(t-\tau_{nn})], \tag{4.1}$$

where τ_{nn} is a delay time from n^{th} node to n^{th} node, $x_n(t)$ is a Boolean logic state at n^{th} node at time t, and f_n is a logic function for n^{th} node.

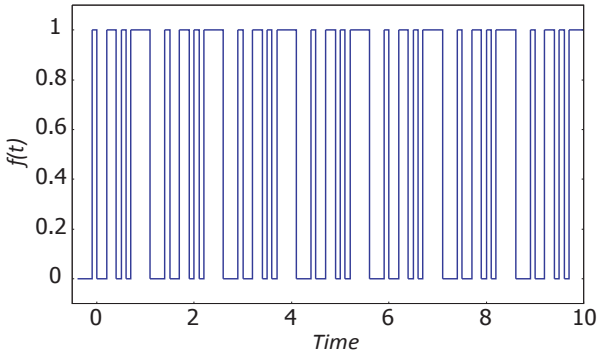
We have numerically tested this hypothesis with the simple Boolean network in Fig. 4.1. In this single-state network, there are two different delay inputs (τ_1, τ_2) of exclusive-OR (XOR) (transitional delay, τ_d) whose output is fed back as delay inputs again. Fig. 4.2 illustrates chaotic oscillation in numerical analysis. We have written simple numerical codes to test the feasibility of generating chaotic oscillation from

the Boolean delay equation [48]. To calculate a trajectory, we construct a queue of the discrete times t_m, to keep track of the transitions. If t_1 is the earliest time in the queue it has processed, this generates two possible transitions at times $(t_1 + \tau_1)$ and $(t_1 + \tau_2)$. These transition candidates are then compared to every transition in the queue to see if there are any collisions. If any transition t_k has the same value as one candidate, that specific transition is removed from the queue and the candidate is discarded. We call this phenomenon a collision between t_k and the tentative transition $(t_1 + \tau_1)$ or $(t_1 + \tau_2)$. If one of the candidates does not collide with any transitions in the queue, the candidate is added to the queue, and the transition t_1 from which it originated is saved on a record of transitions that actually occur and it is removed from the processing queue. We take the next value from the queue and repeat the process until the desired time or number of transitions is reached.

In Fig. 4.2(a), we observe the chaotic oscillation that occurs when two delay inputs have incommensurate numbers, and transition delay of XOR is zero. However, in Fig. 4.2(b) and (c), a periodic oscillation occurs when two delays are commensurate, and when the transition delay is relatively slow, respectively. For an irrational pair of delays, assuming an ideal state transition time, there are no states that occur at the same time. However, as the transition time of the state increases, a short-pulse rejection [49] plays a role in preventing pulses shorter than a minimum duration from passing through the gate, thus inhibiting a chaotic oscillation. This method of numerical analysis keeps track of the transitions, and also incorporates the short-pulse rejection.



(a)



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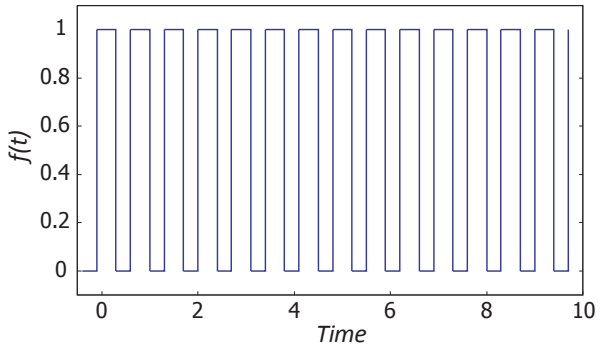


(c)

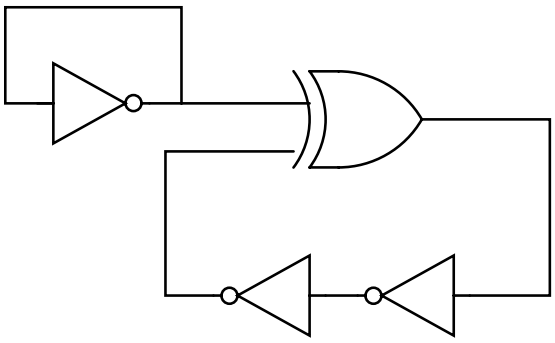
Figure 4.2: Numerical results from XOR (a) when τ_1 and τ_2 is incommensurate, and τ_d is 0 (Boolean chaos), (b) when τ_1 and τ_2 is incommensurate, and τ_d is 0.1 (period 4), and (c) when τ_1 and τ_2 is commensurate, and τ_d is 0 (period 1). Boolean chaotic oscillation is observed when state transition occurs with no response time and two incommensurate delays inputs. When two delays are commensurate and response time of XOR is large, periodic transition is observed.

4.3 Discrete Boolean Chaotic Oscillator

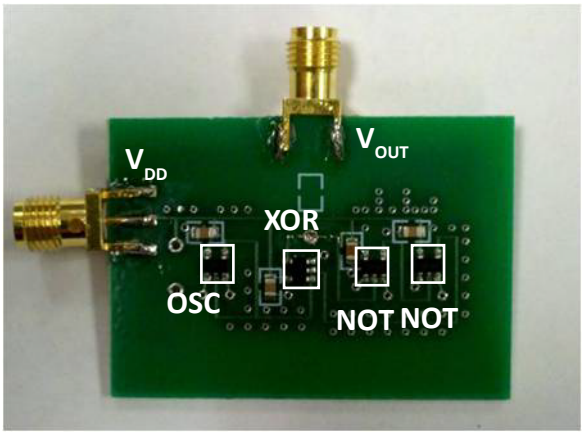
To test mathematical hypothesis developed in previous numerical simulations, we build a Boolean chaotic oscillator using commercial logic gates. Fig. 4.3 depicts a schematic diagram and a picture of the Boolean chaotic oscillator on a printed circuit board. A ring oscillator and cascaded inverters play an important role in generating incommensurate inputs and XOR has a fast response time. We use the SN74AUC-series Texas Instrument logic gates whose propagation delay time is around 2 ns (at C_L=30pF). The output is measured using a high-sampling rate oscilloscope at the output of XOR.

To characterize the chaotic dynamics in this circuit, we analyze the results in various ways, including time domain analysis, frequency spectrum, and calculating maximum Lyapunov exponents (LE) (λ_{max}). In Fig. 4.4, we plot the time evolutions of output voltage for both periodic and chaotic regions, and the frequency spectrum. The observed aperiodicity and broad spectrum are dominant features in a chaotic oscillator.

Next, to verify the existence of chaotic oscillation, we compute the maximum Lyapunov exponents for the entire dynamics domain. The Lyapunov exponent determines how sensitive the signal is to initial conditions, and it is a good way to measure chaotic dynamics. The hypothesis we check is whether the average distance (δ) between trajectories (j) obeys (4.2) after i discrete time steps. Furthermore, maximum Lyapunov exponents (LE) are calculated after taking slopes of logarithmic distance, following the algorithm in [43]. The maximum Lyapunov exponent



(a)



(b)

Figure 4.3: (a) Diagram of circuit which generates Boolean chaotic oscillation. This circuit consists of an XOR(τ_d), a ring oscillator(τ_1), and a delay(τ_2) (b) Picture of the circuit implemented on printed circuit board (PCB), consisting of commercial logic gates.

(λ_{max}) is defined by (4.4) using a least-square fit method, averaged over many nearby trajectories. While a traditional means of calculating LE involves the use of differential equations, here, to calculate average distance between trajectory from the experimental result, we find the nearest neighbor distance, $\delta_j(i)$, from reference trajectories to reconstructed trajectories. This reconstructed trajectory is formed by

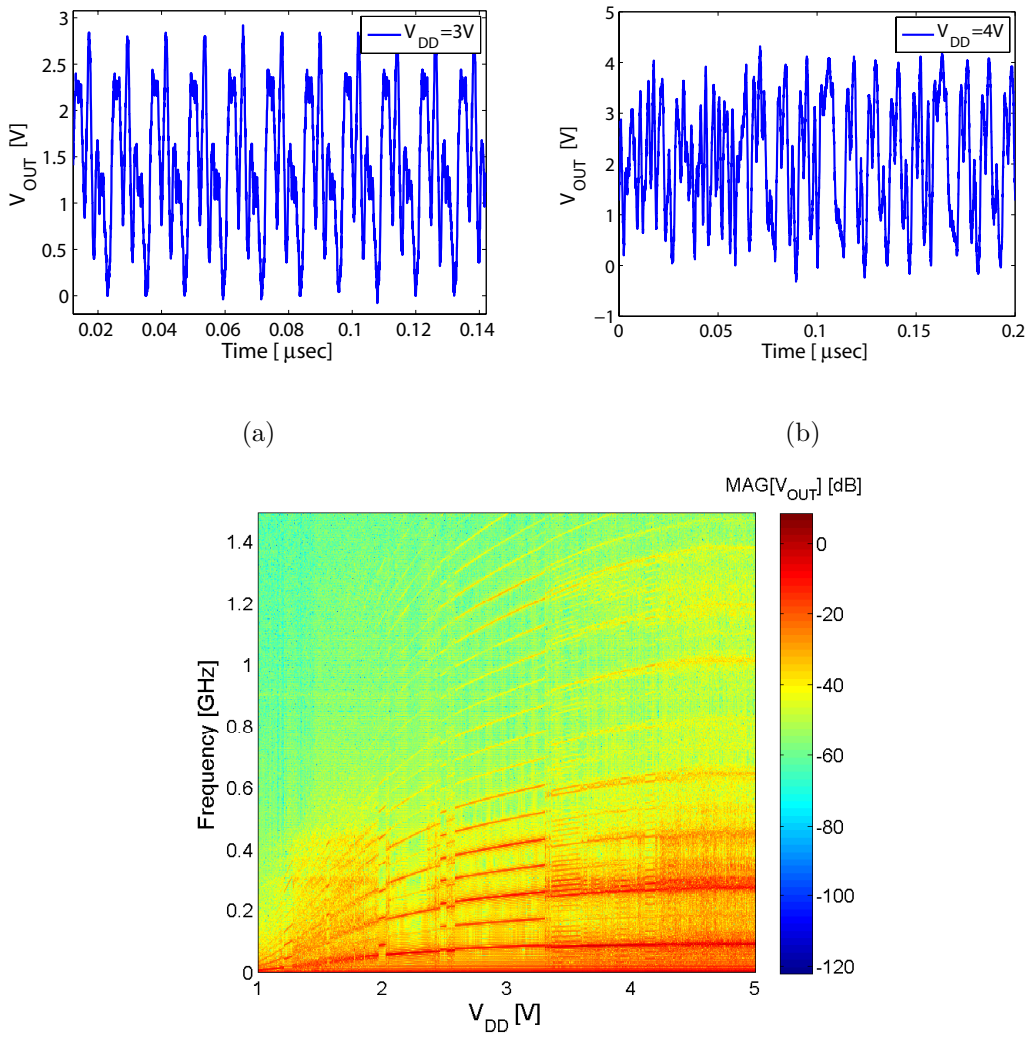
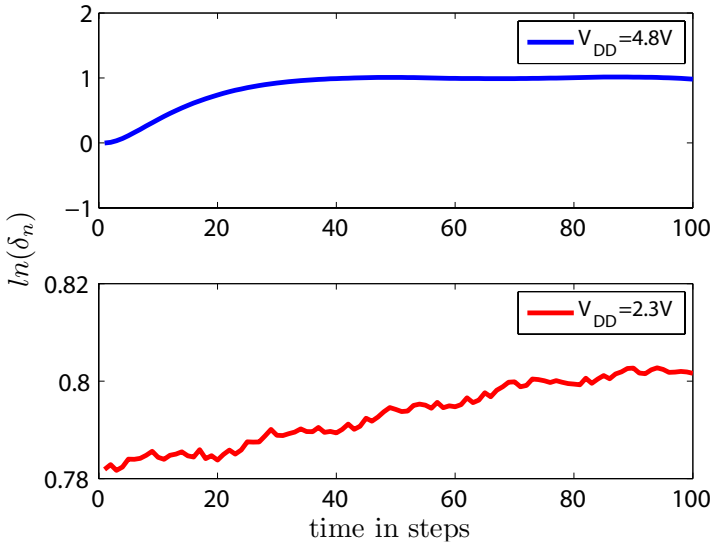
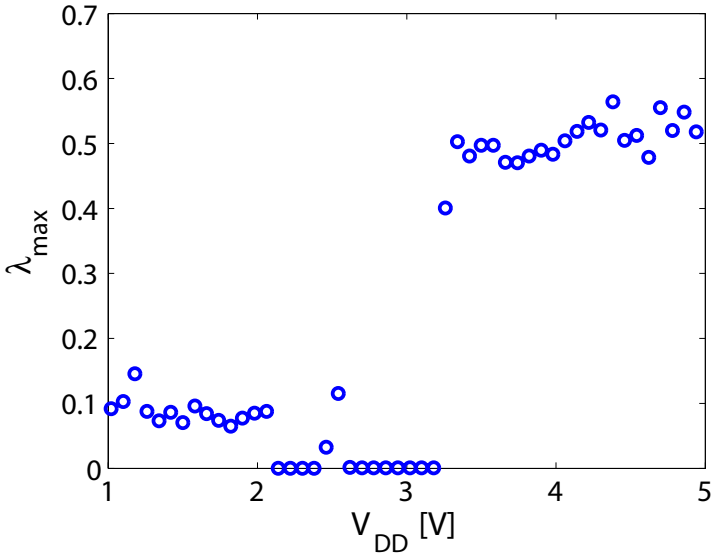


Figure 4.4: (a) Time evolution of periodic oscillations when the circuit is biased at 3V. (b) Time evolution of chaotic oscillations when the circuit is biased at 4V. (c) Frequency spectrum of output voltage signal with varying V_{DD}. A broad spectrum with numerous subharmonics is observed, reaching from DC to 500 MHz.

carefully choosing the delay dimension [43]. Fig. 4.5(a) illustrates the two different cases for the periodic and chaotic oscillation. The slopes of Fig. 4.5(a) indicate strong positive LEs for the chaotic dynamics and near-zero LEs for the periodic



(a)



(b)

Figure 4.5: (a) Average logarithmic distance between trajectories when V_{DD} is 4.8V (top) and 2.3V (bottom). Top figure shows a positive slope while the bottom has a slope close to zero. (b) Maximum Lyapunov exponents (λ_{max}) with varying V_{DD} as the measured data for each V_{DD} are calculated for λ_{max}. After V_{DD} reaches 3.3V, the circuit enters chaotic region, resulting in positive λ_{max}.

dynamics. The entire LE spectrum illustrates the trend of chaotic dynamics as we take V_{DD} as a bifurcation parameter.

$$\delta_j(i) = C_j \cdot exp(\lambda_1 \cdot (i\Delta t)) \tag{4.2}$$

$$\ln(\delta_j(i)) = \ln(C_j) + (\lambda_1 \cdot (i\Delta t)) \tag{4.3}$$

$$\lambda_{max} = \lim_{\delta \to 0} \left\langle \frac{\partial \ln \delta}{\partial t} \right\rangle_j \tag{4.4}$$

4.4 IC realization of the CMOS Boolean Chaotic Oscillator

4.4.1 Circuit Design

Based on the results in the previous section, we design a CMOS Boolean chaotic oscillator using the On-Semiconductor 0.5μm process. This circuit consists of two parts, namely the chaotic oscillator and the output buffer. Fig. 4.6(a) shows a microphotograph of the circuit, and Fig. 4.6(b) and (c) show circuit schematics of the core chaotic oscillator and output buffer, respectively. The number of stages and dimensions of CMOS pairs in the oscillator are carefully chosen to follow the algorithm of Boolean chaos developed in the previous sections. We perform SPICE simulation with proper device models to predict the output signal. As a result, the core chaotic oscillator consists of 5 stages of ring oscillators, 1 push-pull type XOR circuit, and 27 stages of delay inverter chains.

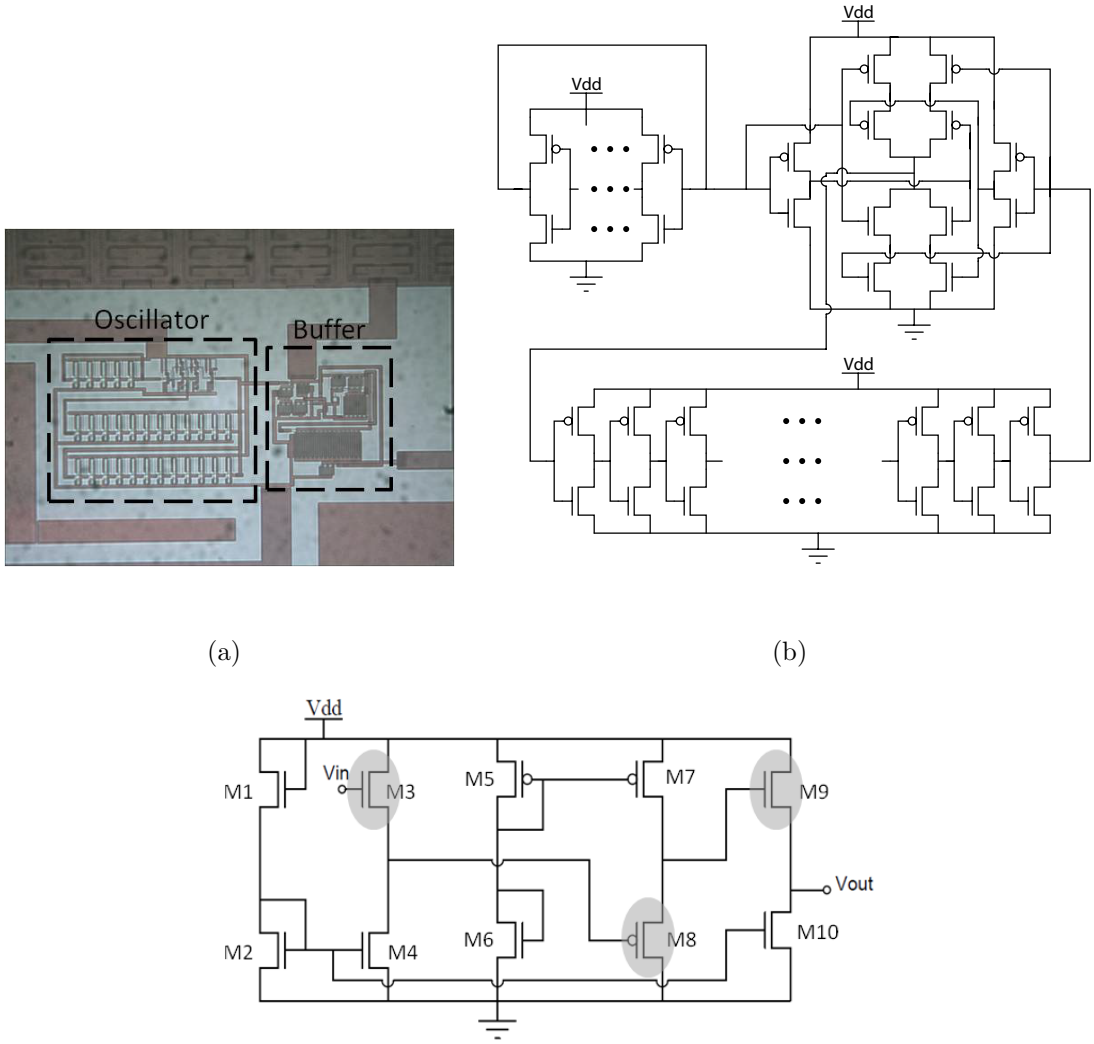


Figure 4.6: (a) Microphotograph of our CMOS Boolean chaotic oscillator, consisting of (b) a chaotic oscillator and (c) a source follower type buffer. The chaotic oscillator includes a ring oscillator, cascaded inverter chains, and an XOR circuit. Numbers of the stages of the ring oscillator and cascaded inverter chains are adjusted after numerical simulation of Boolean chaos and transistor-based simulation. For each stage of common drain amplifiers (M3, M8, and M9), currents are either sourced or sinked.

To drive a load directly, a unity gain output buffer is designed. In general, source followers are used as the output buffers whose output impedance is lowered. We design three stages of source follower buffer with near-unity gain and the bandwidth close to 300MHz. The large signal gain is derived from multiplying the voltage gain of each stage of source follower. The large signal gain of the first stage source follower is

$$A_{v1} = \frac{((1/g_{mb})||r_{o3}||r_{o4})}{((1/g_{mb})||r_{o3}||r_{o4}) + 1/g_{m3}}, \tag{4.5}$$

where g_{mb} is the body-transconductance, g_m is the gain-transconductance, and r_o is the output resistance. The second stage of PMOS source follower is

$$A_{v2} = \frac{(r_{o7}||r_{o8})}{(r_{o7}||r_{o8}) + 1/g_{m8}}. \tag{4.6}$$

The last stage of the source follower is identical to (4.5), but the amplifier size is different.

$$A_{v3} = \frac{((1/g_{mb})||r_{o9}||r_{o10})}{((1/g_{mb})||r_{o9}||r_{o10}) + 1/g_{m9}} \tag{4.7}$$

Overall the large signal voltage gain is close to 1,

$$A_v = A_{v1} \cdot A_{v2} \cdot A_{v3}. \tag{4.8}$$

However, unity gain of the buffer falls apart as transistors enter triode regions. The dominant pole in the frequency response is approximately [50],

$$\omega_{p1} \approx \frac{g_m}{C_L + C_{GS}} \tag{4.9}$$

where C_L is the loading capacitance, and C_{GS} is the small signal capacitance between source and gate node. Therefore, the bandwidth of this buffer is determined by increasing g_m,

$$g_m = \sqrt{\frac{2I_D k_n W}{L}} \tag{4.10}$$

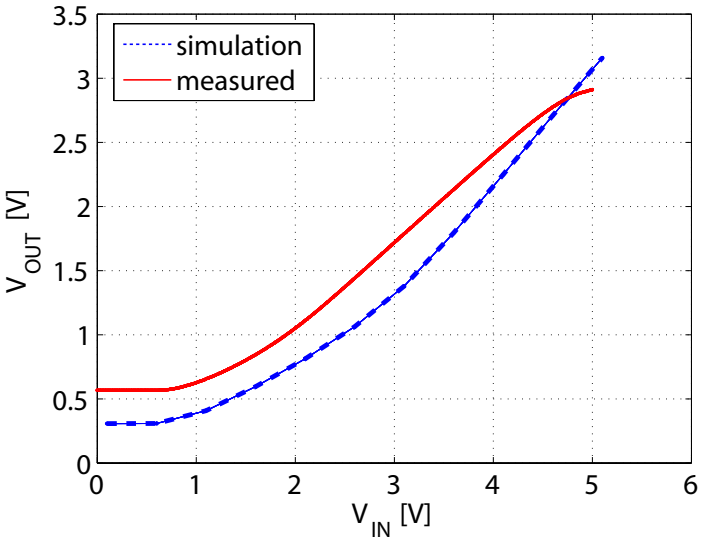
which in turn, is determined by large drive current, I_D.

4.4.2 Results

First, DC and RF responses of the output buffer are measured and simulated. This buffer has a wide dynamic range of unity gain, in Fig. 4.7(a), and a 3dB bandwidth of 300 MHz, in Fig. 4.7(b). This output buffer allows the chaotic oscillation generated in the previous stage to be seen at the load without any distortion, and is capable of driving the capacitive load.

In Fig. 4.8, we also measure time evolution of output signal as V_{DD} varies. We subsequently Fourier-transformed to observe the frequency spectrum. This chaotic oscillator is highly aperiodic and a broad frequency spectrum is observed, reaching up to 300 MHz.

The Lyapunov exponent determines how sensitive the signal is to initial conditions, and it is a good way to measure chaotic dynamics. The hypothesis we check is whether the average distance (δ) between trajectories (j) obeys (4.11) after



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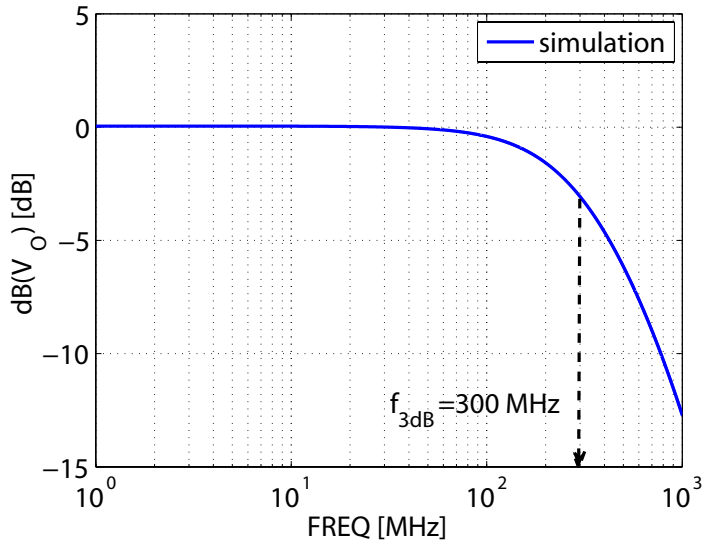
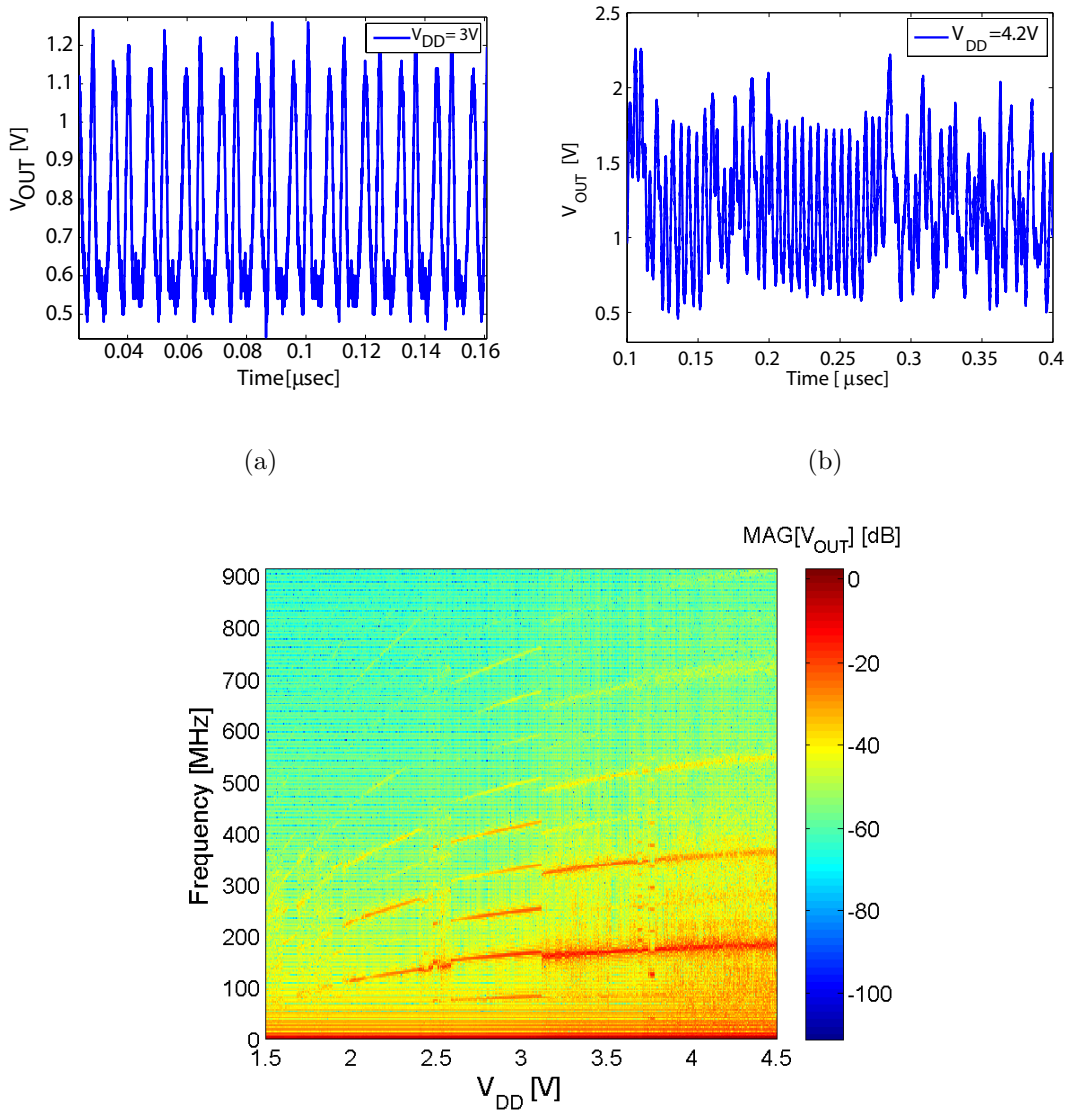


(b)

Figure 4.7: (a) Transfer characteristics of the buffer for measurement and simulation. (b) Bode plot of simulated output voltage of buffer. This buffer is capable of 3dB cut-off frequency of 300 MHz and has wide input ranges for unity gain. The cutoff frequency of the buffer is determined from the amount of current flowing through amplifiers and loading capacitance.



(a)

(b)

(c)

Figure 4.8: (a) Time evolution of periodic oscillation when the circuit is biased at 3V. (b) Time evolution of chaotic oscillation when the circuit is biased at 4.2V. (c) Frequency spectrum of output voltage signal with varying V_{DD}. Broad spectrum with numerous subharmonics, reaching from DC to 300 MHz, is observed.

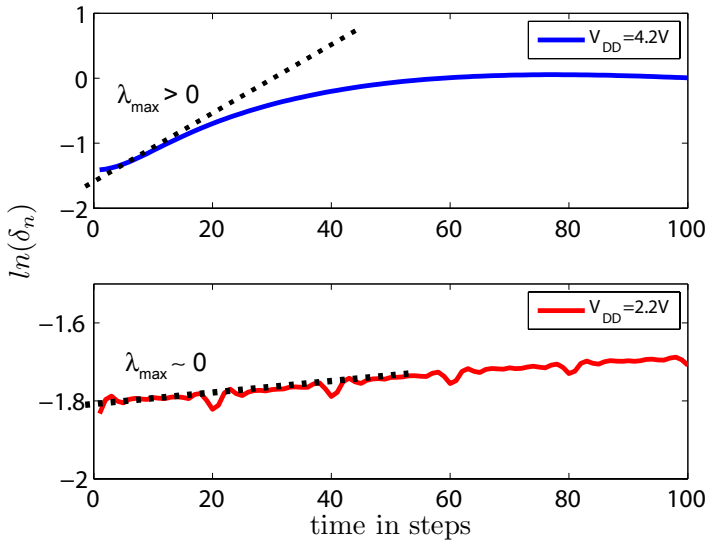
i discrete time steps. Furthermore, maximum Lyapunov exponents (LE) are calculated after taking slopes of logarithmic distance, following the algorithm in [43]. The maximum Lyapunov exponent (λ_{max}) is defined by (4.13) using a least-square fit method, averaged over many nearby trajectories. While a traditional means of calculating LE involves the use of differential equations, here, to calculate average distance between trajectory from the experimental result, we find the nearest neighbor distance, $\delta_j(i)$, from reference trajectories to reconstructed trajectories. This reconstructed trajectory is formed by carefully choosing the delay dimension [43].

$$\delta_j(i) = C_j \cdot exp(\lambda_1 \cdot (i\Delta t)) \tag{4.11}$$

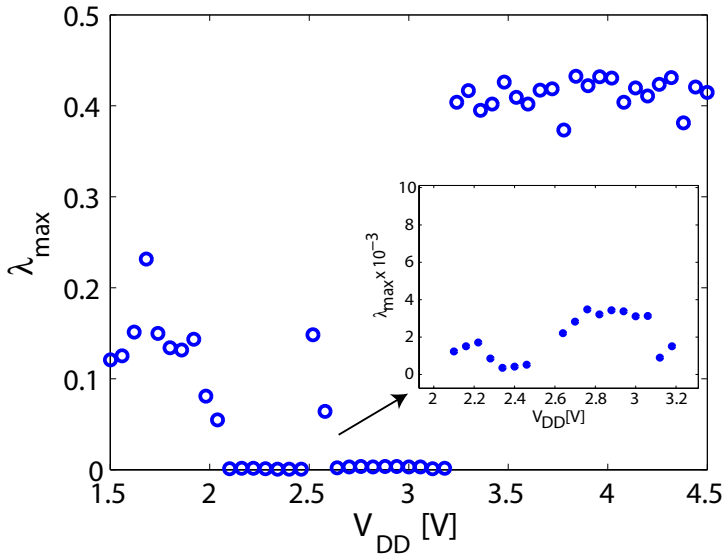
$$\ln(\delta_j(i)) = \ln(C_j) + (\lambda_1 \cdot (i\Delta t)) \tag{4.12}$$

$$\lambda_{max} = \lim_{\delta \to 0} \left\langle \frac{\partial \ln \delta}{\partial t} \right\rangle_j \tag{4.13}$$

In Fig. 4.9(a), we observe an initial positive slope for the chaotic dynamics and a zero slope for the periodic dynamics, respectively. Comparing with the frequency spectrum in Fig. 4.8(c), the same trend of chaotic dynamics is observed, in the Lyapunov spectrum in Fig. 4.9(b) as V_{DD} is varied accordingly. The region with the positive LEs corresponds with the region with the broad spectrum which shows chaotic dynamics. Periodic output exhibits discrete harmonics in the frequency spectrum, and the maximum LE is close to zero.



(a)



(b)

Figure 4.9: (a) Average logarithmic distance between trajectories when V_{DD} is 4.2V (top) and 2.2V (bottom). Top figure shows a positive slope while the bottom has a slope close to zero. (b) Maximum Lyapunov exponents (λ_{max}) with varying V_{DD} as the measured data for each V_{DD} are calculated for λ_{max}. After V_{DD} reaches 3.3V, the circuit enters chaotic region, resulting positive λ_{max}. An inset in (b) indicates near-zero λ_{max} for periodic oscillation.

4.5 Summary

We demonstrate CMOS Boolean chaotic oscillation, whose chaotic dynamics are described by a Boolean delay equation. This equation indicates that chaotic oscillation is possible when we have incommensurate delay inputs and a relatively small transition time in autonomous networks. This Boolean chaotic oscillator produces a chaotic oscillation output, whose bandwidth extends from DC to 300MHz. Its chaotic dynamics are tested through time evolution, frequency spectrum, and maximum Lyapunov spectrum of output signals. This circuit is the first integrated circuit implementation of the Boolean chaotic oscillator, which can be widely used in building a CMOS integrated circuit for a true random number generator. In the next chapter, we will study the feasibility of this circuit for random number generation.

Chapter 5

Cryptographic Physical Random Number Generator

5.1 Overview

We report on a random number generator whose randomness originates from a Boolean chaotic oscillator, designed and fabricated as an integrated circuit in Chapter 4. Random number generators (RNGs) are important for a variety of applications, including encryption, random key generation, and Monte-Carlo simulations [51]. Successful random number generation is crucial in improving the results and security of these applications.

A true random number generator needs a naturally occuring source of randomness. The potential origin of randomness in this physical true RNGs includes non-deterministic [52, 53], deterministic sources [54, 55], as well as numerical pseudo-RNGs. Examples of non-deterministic sources in RNGs are thermal noise and stray electromagnetic waves. These sources are highly sensitive to the semiconductor manufacturing process, and thus are not reliable in generating outputs. The noise must be amplified to a level where it can be accurately converted as digital bits. There are few reports on the implementation of RNGs based on the noise source [56, 53]. However, it is hard to implement as a CMOS IC because this work requires an adequate shielding from power supply and substrate signals. On the other hand, examples of deterministic sources include the frequency instability of a free

running oscillator, and a chaotic oscillator. They can be built on integrated circuits and their outputs are kept shielded from process variations and test conditions, compared to non-deterministic sources. In addition, this type of RNGs requires no post-processing steps before analog-to-digital (ADC) conversions. Last, numerical pseudo-RNGs can also be candidates in building true RNGs. Designing a RNG with a numerical pseudo-RNG is even more difficult process than doing with a hardware, and requires a complex algorithm to generate RNGs [51]. Most of the numerical pseudo-RNGs are built with the very large scale device (VLSI) device like a field-programmable gate array (FPGA). Table 5.1 compares the different RNGs with the different sources. Here, we exploit the randomness from chaotic dynamics of the Boolean chaotic oscillator.

It is almost impossible to give mathematical proof that a signal is truly random. Among many tests, a statistical test from National Institute of Standards and Technology (NIST) is the most trusted in the field. [51]. The test describes the probabilistic weakness the generator may have. This is accomplished by taking analog output, and converting to digital signal, and subjecting it to various statistical tests.

We report here on random number generation with our IC Boolean chaotic oscillator, using only minimum post-processing techniques such as threshold detection and bit generation. These bits pass through the NIST statistical test [13], a standard way to validate the properties of RNG for cryptographic application.

In Section 5.2, we focus on the post-processing methods of digitizing the outputs of the CMOS Boolean chaotic oscillator.

Table 5.1: Comparison of different random number generator sources

Source	Thermal Noise	Chaotic Oscillator	Numerical Pseudo-RNG
CMOS compatibility	Bad	Good	PC, FPGA
Reliability	Bad	Very Good	Very Good
Randomness	Good	Good	Very Good
Post-Processing *	Noise Amplification	Not Required	Complex
No. of Transistors	<100	<100	>1 million
References	[56, 53]	[55, 57], this work	[51]

*excluding analog-to-digital conversion (ADC).

In Section 5.3, we perform various statistical tests of the validity of the random number generator, including the NIST statistical test.

5.2 Random Number Generation

A deterministic type of random number generator uses chaotic oscillation as a source to produce true randomness in RNGs. Fig. 5.1 shows a scheme to generate digitized random bits from the circuit developed, in Chapter 4. Data acquired from the oscilloscope passes through the functions in the software. Most random sources may suffer, in that the output bits may be biased or correlated. Among various

techniques for generating truly random bit sequences, such de-skewing is necessary as shown Fig. 5.1. The de-skewing process has two steps.

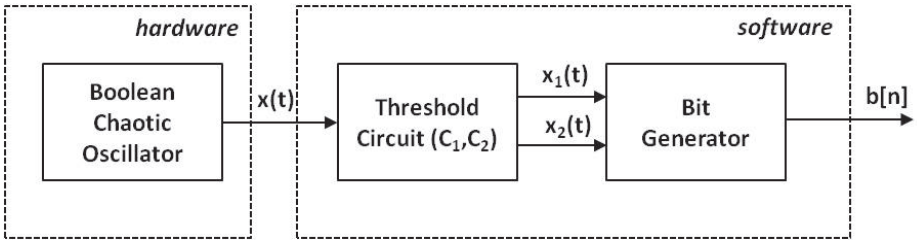


Figure 5.1: Schematic diagram of random number generation using CMOS boolean chaotic oscillator.

First, analog signals from the CMOS Boolean chaotic oscillator directly pass through the threshold function with threshold inputs, C_1 and C_2. This block is described by

$$x_1(x(t)) = \begin{cases} 0 & \text{if } x(t) > C_1 \\ 1 & \text{if } x(t) \leq C_1 \end{cases} \tag{5.1}$$

$$x_2(x(t)) = \begin{cases} 0 & \text{if } x(t) > C_2 \\ 1 & \text{if } x(t) \leq C_2. \end{cases} \tag{5.2}$$

This threshold circuit can be achieved using the circuit shown below in Fig. 5.2. Next, a bit is generated when the signal passes the subspace S_1 region or the subspace S_2 region through subspace S_0. This bit generation is described by

$$b(x_1, x_2) = \begin{cases} 0 & \text{if } x_1{=}0,\ x_2{=}0 \uparrow 1 \\ 1 & \text{if } x_2{=}1,\ x_1{=}0 \uparrow 1. \end{cases} \tag{5.3}$$

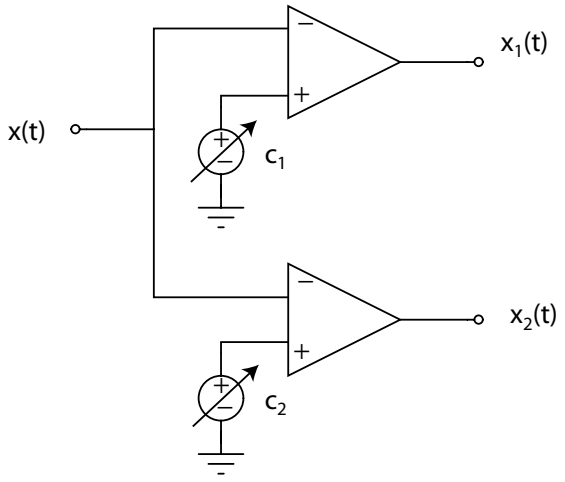


Figure 5.2: Diagram of circuit for generating binary sequences.

This post-processing is equivalent to dividing the entire phase space of chaotic dynamics into the subspaces, S_0, S_1, and S_2, and then keeping track of transitions of one subspace to another. A measure of entropy(H) with respect to threshold values is tested to give the most uncertainty. Fig. 5.3 shows that H achieves its maximum when C_1 and C_2 are at 1.4 and 1.2, respectively.

$$H = -\sum_{i=1}^{n} p(x_i) ln(p(x_i)) \tag{5.4}$$

After the final de-skewing process, the bit sequence generated is shown in Fig. 5.4. In addition, Fig 5.5 plots the greyscale image of output sequences. The output array is converted to the square matrix, and bit 1 is represented by a black pixel whereas bit 0 is represented by a white pixel. Fig 5.5 shows randomness in the given output.

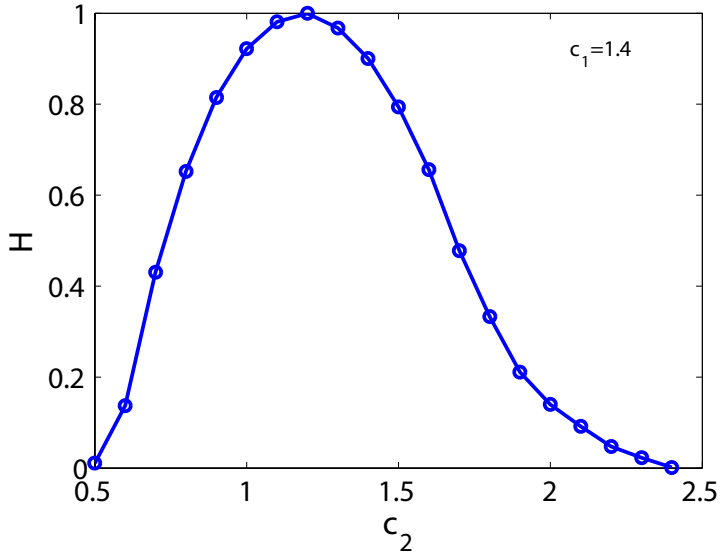


Figure 5.3: Calculated entropy as a function of threshold C_2. We evaluated the binary sequence of $C_2 = 1.2$ for statistical properties of random processes using the NIST statistical test.

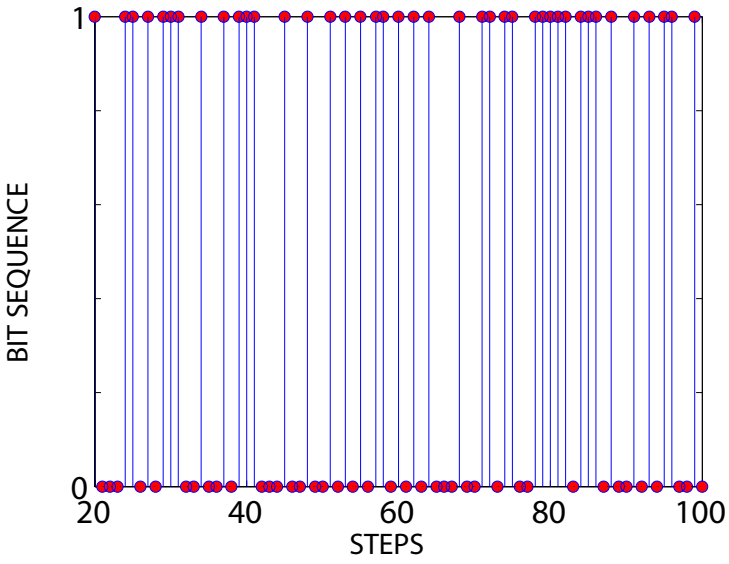
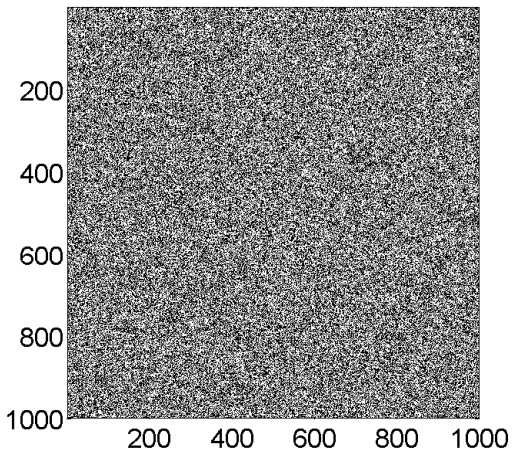
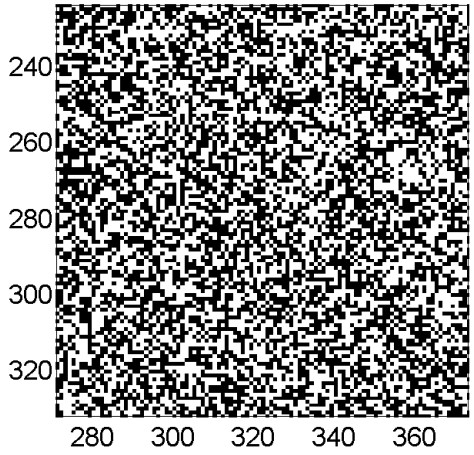


Figure 5.4: Bit sequence generated after post-processing. The closed circles represent the actual bits.



(a)



(b)

Figure 5.5: (a) Grayscale plot for output bit sequence after converting to square matrix. (b) Inset of (a). Black pixels represent 1, and white pixels respresent 0.

5.3 Statistical Tests

Statistical hypothesis testing is a method of making decisions using data. A statistical test is performed to test a specific null hypothesis (H_0). The null hypoth-

esis in this case is that the sequence being tested is random. For each applied test, often developed to test the randomness of a sequences, a decision is made whether to accept or reject the null hypothesis. Under the null hypothesis, such a test generates a distribution of test values. During the test, the test value is compared to a critical value, computed from a given theoretical reference distribution. However, there are two errors associated this statistical hypothesis testing. Table 5.1 explains the type of errors.

Table 5.2: Type I and II error in Statistical hypothesis testing

SITUATION	CONCLUSION	
	Accept H_0	Reject H_0
Data is random (H_0 is true)	No error	Type I error
Data is not random (H_0 is false)	Type II error	No error

If the test statistic value is S and the critical value is t, then a Type I error is defined by $P(S > t \mid H_0\ is\ true)$=$P(reject\ H_0 \mid H_0\ is\ true)$, and describes a tendency to conclude it is not random while the sequence is in fact random. A Type II error is also defined by $P(S < t \mid H_0\ is\ false)$=$P(accept\ H_0 \mid H_0\ is\ false)$, and describes a tendency to conclude it is random while the sequence is in fact not random. The test statistics calculates a $P-value$, a strength of the evidence against the null hypothesis. If the $P - value$ is 1, then the bit sequence is truly random. A $P - value$ of 0 indicates the sequences is non-random. Here, a significance level α is chosen. Therefore, if the $P - value$ is greater than α, the sequence is random,

with a confidence level of α. On the other hand, if the $P-value$ is less than α, the sequence is not random, with a confidence level of α. For example, for a $P-value$ greater than 0.001 and α of 0.001, a sequence would be random with a confidence of 99.9 percent.

We evaluate the statistical properties of the random process using the NIST statistical test suite. The NIST test suite contains 15 functions of statistical tests. The interpretation of test results examines two features; the distribution of p-values to the check the uniformity, noted as P-value, and the proportion of sequences that pass a statistical test. A thousand sequences of a 1 Mbit sample pass through each test in the NIST test suite and then return a single P-value, and furthermore, from 1000 individual p-values, the number of test that satisfies $p > \alpha$ is computed.

For a truly random sequence, p-values must exceed the level of significance α chosen. The P-value, should be larger than 0.0001 and the proportion number should also be greater than 0.98 for a given number of sequence and level of significance. Table 5.2 summaries the results of NIST statistical tests for the level of significance 0.01.

5.4 Summary

In summary, a random number generator using chaotic oscillator has many technical advantages over other random number generators based on in-deterministic sources. Moreover, Boolean chaotic oscillator can be easily built using a current CMOS technology. With complete design summary in the previous chapter, here,

we described the post-processing technique to convert the analog output to digital outputs. We carefully choose test parameters of post-processing as we monitor the entropy functions of every test parameter. Then, we use the NIST statistical test to verify its feasibility as a random number generation source.

Table 5.3: Results of NIST statistical test α=0.01

Statistical Test	P-value	proportion	Result
Frequency	0.6329	0.9823	success
Block frequency	0.8905	0.9870	success
Cumulative sums*	0.8846	0.9820	success
Runs	0.8949	0.9910	success
Longest runs	0.6308	0.9880	success
Ranks	0.3976	0.9900	success
FFT	0.2812	0.9850	success
Nonoverlapping templates*	0.0140	0.9830	success
Overlapping templates	0.6931	0.9890	success
Universal	0.1503	0.9920	success
Approximate entropy	0.2467	0.9910	success
Random excursion*	0.022	0.9803	success
Random excursion var*	0.0817	0.9803	success
Serial*	0.3085	0.9930	success
Linear complexity	0.1756	0.9920	success

*The worst case number is chosen for the multiple sub-tests.

Chapter 6

Conclusions and Future Research

6.1 Conclusions

The thesis consists of two parts. First, we demonstrate in an experiment and models that chaotic oscillation is present in standard CMOS integrated circuits when it is driven under electromagnetic source. Next, we design a CMOS Boolean chaotic oscillator, a well-suited entropy generator in building a random number generator.

6.1.1 Chaotic Oscillation as HPM effect in CMOS ICs

Chaotic oscillation is a phenomenon with implications for many fields of science and technology. High power microwave effect is a behavior of CMOS ICs when the circuit is exposed to intentional and directed high power microwave signals. Besides some of the reported effects, chaotic oscillation has only been conjectured as an instability and never been proven.

We have demonstrated chaotic oscillation is present in standard CMOS ICs. First, we design and fabricate a conventional CMOS digital inverter circuit that consists of a logic circuit, an output buffer, and an electrostatic discharging protection circuit. The building blocks used in our test circuit all come from the library of foundry services. To be able to investigate the chaotic dynamics in standard CMOS ICs, we have chosen the basic CMOS structures. In a direct RF injection experi-

ment, we have observed some evidences of existence of strong nonlinear dynamics in the power frequency spectrum such as broadband spectrum and various kinds of bifurcations. Next, we have analytically given some nonlinear features occurred from this HPM injection circumstance. Important nonlinearities are the followings. Large RF signals are rectified from junction diodes of ESD protection circuits, and this rectification enters a non-quasi static regime as the period of RF signal becomes comparable to the reverse recovery time of the ESD diodes. In addition, a nonlinear LC current from the parasitic inductances and a nonlinear capacitance of junction diodes play a role in generating numerous subharmonics. Further, we validated the presence of chaotic oscillation by computing the positive largest Lyapunov exponents from numerical models. The presence of chaotic oscillation is validated as we verify the three aspects in the definition of chaotic signal. Aperiodicity is characterized by the broadband power spectrum, deterministic nature of the signal is verified by the setting up the dynamical equations, and further its sensitiveness to the initial condition is analyzed through computing positive largest Lyapunov exponents.

The importance of this work is that another effect mechanism, chaotic oscillation is discovered in standard CMOS integrated circuits, which long been only conjectured. Having studied the dynamics of nonlinear features in the circuit, we can better understand the causes of chaotic oscillation. Due to the general CMOS circuit we design, this study can also apply to any CMOS digital circuits which consist of general structures discussed in this thesis. Last, this work is a credit to a high power microwave community, one can disrupt and force the system to failure, if the circuit is driven to chaotic oscillation. This work may reflect that the CMOS

digital circuit is highly vulnerable to chaotic oscillation under high power microwave excitation.

In summary, our approach towards this topic is that we have experimentally observed some evidences of chaotic oscillation, and finally numerically validate the presence of chaotic oscillation in the circuit.

In Chapter 2, we explained the design procedure of CMOS Inverter integrated circuits and the experiment procedure of RF signals coupling to the designed circuit. To demonstrate the experimental evidences of chaotic oscillation, we analyzed the output voltages in time and frequency domains. We analytically discussed the sources of nonlinearity contributing to the generation of chaotic oscillation.

In Chapter 3, we further showed the presence of chaotic oscillation using the numerical models. The mathematical model consists of nonlinear functions of the circuit, and the largest Lyapunov exponents are calculated to show the existence of chaotic oscillation. We build a transistor-model to predict the RF onset of chaotic oscillation when the circuit enters the chaotic region. This agrees with the measured results in Chapter 2.

6.1.2 Chaotic Oscillation in Cryptographic Random Number Generation

Boolean chaos is a new mechanism for generating chaotic oscillation. Chaotic oscillation is generated in a network whose transition is highly Boolean and in which the state nodes are connected with different delays. In cryptographic purposes, a

random number generator is built from many randomness sources such as thermal noise, stray electromagnetic waves, and even metastability of the circuit. Chaotic oscillation is a good candidate for building a randomness source because its signal is easy to control and deterministic. We designed the CMOS Boolean chaotic oscillator, and tested it for feasibility as a random number generator. Compared to other chaotic oscillators, this type of Boolean chaotic oscillator is favored due to the integration with the CMOS technology. In validating the feasibility of random number generation, a NIST statistical random number test is generally used.

In Chapter 4, we numerically and experimentally test the hypothesis that the Boolean delay equation leads to chaotic oscillation. Using CMOS 0.5 μm technology, we designed a CMOS Boolean chaotic oscillator.

In Chapter 5, using the statistical NIST random number test, we verify the feasibility of the designed circuit in the random number generator (RNG). Our RNG has passed all the tests in the NIST statistical test.

6.2 Future Directions

The research presented in this thesis can be considered as a starting point for a deeper exploration of chaotic oscillation in the CMOS integrated circuit. For future research, we would like to head into some important directions.

First, we point out the PN junction modeling in the BSIM model. Although much literature and research has guaranteed the recent version of BSIM to work up to hundreds of GHz operations, this high frequency modeling only takes care

of charging and discharging of the channel in MOSFET. For stability under large signal electromagnetic excitation, the nonlinear dynamics in the PN-junctions are more important. The PN-junction in the BSIM model is an important contributor to the generation of chaotic oscillation, but in BSIM, no valid modeling exists. One way to avoid this problem is to use another version of the DIODE model, but this needs extra work, namely, converting our ESD protection circuit based on MOSFET to the correct diode model parameters.

Second, we concluded that the design of the ESD protection circuit is highly susceptible to electromagnetic interference in generating chaotic oscillation. The ESD protection circuits we used in the circuit is a generic ESD protection circuits, provided by the MOSIS foundry. Research should be carried on as to find other types of ESD protection circuits to reduce this effect. An important area to explore is the study of ESD protection circuits which are highly compatible with chaotic oscillation.

Third, the speed of the CMOS design of the Boolean chaotic oscillator is limited by the technology node, the frequency response of the output buffer, and a load impedance of oscilloscope. For a high speed random number generator, we need an output buffer design with higher cutoff frequency response, and small loading impedance.

6.3 Closing Remarks

In closing the work, there is no doubt that chaotic oscillation is a complex and difficult problem to deal with especially in CMOS integrated circuits. It was long traditions that electrical engineers have long neglected the importance of the chaotic oscillation in their electronics. However, when it comes down to HPM effects, this regime can no longer be neglected. The fundamental work presented here provides an essential background to people studying the stability of their system under electromagnetic source, and at the same time, defines chaotic oscillation as a new effect mechanism under high power microwave coupling into CMOS integrated circuits. As a result, the presence of chaotic oscillation in standard CMOS integrated circuit will bring lots of attentions to the researchers looking at the high-order instability as well as researchers developing such EMI-hardened or HPM-hardened systems.

In addition, the development of chaotic oscillators has gained lots of attentions in communications and cryptography. Surely, this work of building random number generator using CMOS Boolean chaotic oscillator will be another asset for circuit designers who are developing CMOS ICs using chaotic dynamics, especially in the fields of random number generations.

Appendix A

BSIM Parameters

MODEL CMOSN NMOS LEVEL = 49

VERSION = 3.1 TNOM = 27 TOX = 1.38E-8

+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.5931459

+K1 = 0.879253 K2 = -0.0968711 K3 = 22.6428645

+K3B = -9.849049 W0 = 2.636842E-8 NLX = 1E-9

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.6755795 DVT1 = 0.27608 DVT2 = -0.4974617

+U0 = 454.8293133 UA = 1E-13 UB = 1.306857E-18

+UC = 6.003353E-12 VSAT = 2E5 A0 = 0.5426773

+AGS = 0.1060338 B0 = 1.852719E-6 B1 = 5E-6

+KETA = -2.682846E-3 A1 = 0 A2 = 0.3

+RDSW = 856.9792774 PRWG = 0.1467648 PRWB = 0.0170317

+WR = 1 WINT = 2.058331E-7 LINT = 6.416175E-8

+XL = 1E-7 XW = 0 DWG = 2.559387E-10

+DWB = 2.956012E-8 VOFF = 0 NFACTOR = 0

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 1.691727E-3 ETAB = -2.990578E-4

+DSUB = 0.0620642 PCLM = 2.1398211 PDIBLC1 = 1.636689E-4

+PDIBLC2 = 1.72093E-3 PDIBLCB = 0.0944082 DROUT= 3.292468E-3

+PSCBE1 = 3.840311E8 PSCBE2 = 3.949241E-6 PVAG = 0

+DELTA = 0.01 RSH = 81.6 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 1.88E-10 CGSO = 1.88E-10 CGBO = 1E-9

+CJ = 4.189612E-4 PB = 0.8362037 MJ = 0.4268727

+CJSW = 3.511622E-10 PBSW = 0.8 MJSW = 0.2006042

+CJSWG = 1.64E-10 PBSWG = 0.8 MJSWG = 0.2019414

+CF = 0 PVTH0 = 0.0862532 PRDSW = 84.413531

+PK2 = -0.0885087 WKETA = -0.0164054 LKETA = 1.749206E-3

.MODEL CMOSP PMOS LEVEL = 49

+VERSION = 3.1 TNOM = 27 TOX = 1.38E-8

+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9152268

+K1 = 0.553472 K2 = 7.871921E-3 K3 = 2.8768851

+K3B = 2.0233456 W0 = 5.780172E-7 NLX = 1.005775E-9

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.4714461 DVT1 = 0.1852157 DVT2 = -0.3

+U0 = 201.3603195 UA = 2.48572E-9 UB = 1.005454E-21

+UC = -1E-10 VSAT = 1.051486E5 A0 = 0.7471706

+AGS = 0.1277893 B0 = 7.349251E-7 B1 = 2.776521E-8

+KETA = -4.865785E-3 A1 = 3.090478E-4 A2 = 0.5651395

+RDSW = 3E3 PRWG = -0.0219617 PRWB = -0.0909377

+WR = 1.01 WINT = 2.212303E-7 LINT = 9.977278E-8

+XL = 1E-7 XW = 0 DWG = -4.82616E-10

+DWB = -1.585E-8 VOFF = -0.0619165 NFACTOR = 0.2482253

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 9.384854E-3 ETAB = -0.2

+DSUB = 1 PCLM = 2.3408026 PDIBLC1 = 0.0767278

+PDIBLC2 = 4.024702E-3 PDIBLCB = -0.0443178 DROUT = 0.2659121

+PSCBE1 = 8E10 PSCBE2 = 8.966681E-8 PVAG = 0.0149502

+DELTA = 0.01 RSH = 105.9 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 2.35E-10 CGSO = 2.35E-10 CGBO = 1E-9

+CJ = 7.015391E-4 PB = 0.8644163 MJ = 0.4849925

+CJSW = 2.448774E-10 PBSW = 0.8 MJSW = 0.2031512

+CJSWG = 6.4E-11 PBSWG = 0.8 MJSWG = 0.2261452

+CF = 0 PVTH0 = 5.98016E-3 PRDSW = 14.8598424

+PK2 = 3.73981E-3 WKETA = 0.0140638 LKETA = -0.0170643

Appendix B

Code for Numerical Models

We present the MATLAB code for simulating chaotic oscillation in the given model in Chapter 3. Section B.1 shows main function which uses 4th Runge-Kutta method to solve the set of the ordinary differential equations. Section B.2 consists of nonlinear functions, including transconductance of the inverter, static diode current, nonlinear capacitance,

B.1 Main Function

```
function [tset,VL,IL]=inv_ode(dBm)
% clear all;
% clc;

x0=[3 0];
t_step = 10^-11;
t_end = 1.5*10^-7;
tspan = 0.1e-7:t_step:t_end;

global Cjj
global I_inverter
global I_diode
global Vdiode
global tt
global VVin
global VLL
global Vold

Cjj=[];
I_inverter=[];
I_diode=[];
Vdiode=[];
tt=[];
VVin=[];
VLL=[];
Vold = 0;

[t,x]=ode23(@example,tspan,x0,[],dBm);
tset(:,1)=t(:,1);
VL(:,1)=x(:,1);
IL(:,1)=x(:,2);
```

```
function [xprime] = example(t,x,fi,dB)

global Cmp
global Cmn
global I_inverter
global tt
global VVin
global VLL
global V1
global deri_Cmp
global deri_Cmn

VDD=3; %V
L2=2e-9; %H

%% RF input %%%
dBm=dB;
omega = 2*pi*fi;
Vdc = 0;
vac = sqrt( (10^((dBm/10)-3)) * 50 ); %conversion of dBm to V
Vin = Vdc +  vac*sin(omega*t) ;


%% monitor interior variables %%
V1(end+1,1)=x(1);
VLL(end+1,1)=x(2);
VVin(end+1,1)=Vin;
tt(end+1,1)=t;

%% Nonlinear elements %%
Cmp(end+1,1)= Cjp(x(1)-x(2));
deri_Cmp(end+1,1)=deri_Cjp(x(1)-x(2));
Cmn(end+1,1)= Cjn(x(1)-0);
deri_Cmn(end+1,1)=deri_Cjn(x(1)-0);
I_inverter(end+1,1) = Iin(x(1));

%% ODE %%
xprime
=[(x(3)-I_inverter(end)+x(4))/(Cmn(end)+(deri_Cmn(end)*x(1)));
((x(3)-I_inverter(end)-x(4))/(Cmn(end)+(deri_Cmn(end)*x(1))))
- (I_inverter(end)-x(4))/(Cmp(end)+deri_Cmp(end)*(x(1)-
x(2))) ; (1/L1)*(Vin -x(1));(1/L2) * (VDD-x(2));];

end
```

B.2 Subfunctions

```
function [I_inverter] = Iin(Vin)

% global I_inverter

Imax= 2.5e-3;
alpha = 0.2;

I_inverter = 2*Imax ./( 1+exp( ( (Vin-1.5).^2 )./alpha));

end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [Idiode]=Id(Vd)

Io=1e-12;
Vt=0.025;%V
n=1.2;

if Vd > 0.7
    Idiode=10e-5*Vd^n -0.0000602 ;
else
    Idiode=-Io;
end

end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

function [Cjj]=Cjn(Vd)

    Cjo=1e-10;
    beta=2;

    if Vd < -0.7
        Cjj=Cjo*exp(-Vd/beta);
    else
        Cjj=Cjo;
    end
end
```

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