ABSTRACT

Title of Document:	RELIABILITY ASSESSMENT OF VOIDED MICROVIAS IN HIGH DENSITY INTERCONNECT PRINTED CIRCUIT BOARDS UNDER THERMO MECHANICAL STRESSES
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Microvias allow signal and power transmission between layers in high density interconnection printed circuit boards. Presence of voiding in filled microvias due to defective manufacturing process has raised concerns in industry. Voids can vary widely in shape and size and have been observed in both stacked and single-level microvias. IPC standards have addressed the presence of voids in microvias using void size as the acceptance criterion. The purpose of this study is to determine how voiding affects the degradation of microvias; if void size is the only parameter that needs to be taken into consideration or void shape is important as well. Voided as well as non-voided microvias were tested using liquid-to-liquid thermal shock to understand the difference between behavior of voided and non-voided microvias under thermo-mechanical stresses.

RELIABILITY ASSESSMENT OF VOIDED MICROVIAS IN HIGH DENSITY INTERCONNECT PRINTED CIRCUIT BOARDS UNDER THERMO MECHANICAL STRESSES

By

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Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park, in partial fulfillment
of the requirements for the degree of
Masters of Science
2013

Advisory Committee:

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Dr. Michael Azarian

Dedication

To my parents and sisters who have always supported me throughout my life

Acknowledgements

I would first like to thanks Professor Pecht and Dr. Azarian for the opportunity to do this research as well as the time and guidance provided. Additionally, I would like to thank the other member of the advisory committee, Professor Dasgupta for all his input and help improving this work.

I would also like to thank all the members of CALCE specially the ones in Professor Pecht and Professor McCluskey`s research group for their advice, and friendship. Special thanks to Hannes, Amir, Ali, Thomas, Anshul, Xiaofei, Sony, Anto, Ranjith, Rob and Rayhoo. Even bigger thanks to Yan, for providing me with so much help during this research.

I have to add another special thanks to all the student and staff members of Professor Pecht`s research group for providing their feedback on the research on the morning meetings and also all the knowledge I gained thorough attending the morning meeting sessions.

Additionally, I need to thank CALCE for the use of equipment and facilities, especially to Bhanu, Swapnesh and Adam for help and guidance provided during my work in the laboratories.

Finally, I would like to thank my parents and both of my sisters for the love and support, as well as always lending a listening ear and be with me throughout all the ups and downs.

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1. INTRODUCTION

With the increase in the number of I/O pads and I/O pad density while package body size keeps decreasing at the same time, the printed circuit board (PCB) industry is required to find ways to increase the interconnection density of the PCB. A via is a physical piece of metal that makes electrical connection between layers in the PCB and carries signals or power between layers [1]. Figure 1 shows the schematic of a microvia. High density interconnection (HDI) PCBs have a higher wiring density, finer lines and spaces (≤100µm), smaller vias (≤150µm) and capture pads (≤400µm), and higher connection pad density (>20 pads/cm2) than what is employed in conventional PCB technology [2][3].

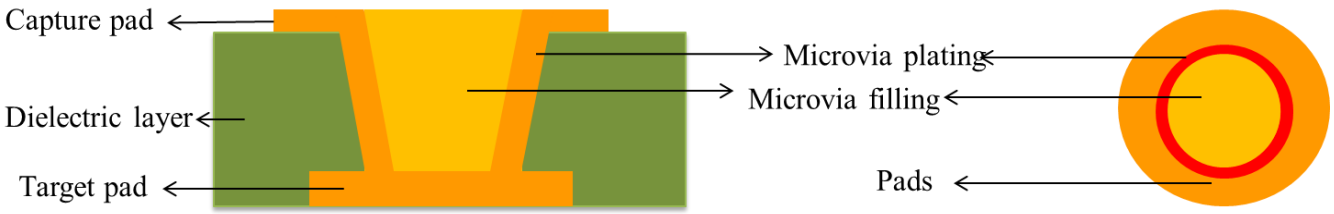

Figure 1- Schematic of microvia

Microvias have a smaller aspect ratio compared to plated through holes, for Microvias, the aspect ratio (AR) is less than 1:1 (0.5:1- 0.7:1) whereas for through holes it is larger than 6:1, even as high as 20:1. Figure 2 illustrated the aspect ratio in Microvias.

Microvia AR= $\frac{h}{a}$

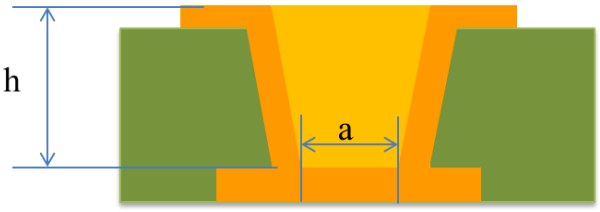

Figure 2- Illustration of microvia aspect ratio

The target pad is defined as the land on which a micro-via ends and makes a connection whereas the capture pad is where microvia starts [4]. Based on IPC-2315 [3] microvia diameter on target pad has to be between 100 to 150 µm while it is 125 to 200 µm for capture pad

Depending on the location of the Microvias, they are defined by IPC-2226 standard [4] as two main types, blind and buried vias, the buried Microvias are the ones that make connection between the inner layers of the board and do not have any connection to the surface mount component whereas for blind vias, one end is connected to the outer layer of the PCB while the other end is in contact with the inner layers. With the advancement in HDI technology, more than one layer of micro via was needed. In the multi-layer HDI boards, microvias can be stacked or staggered. Staggered microvias, were the initial design for the multi-layer HDI boards were several single layer microvias were put together in different layers in a staggered formation however with further advancement in technology, multi-layer stacked microvias were introduced were several single layer microvias are put on top of each other and form stacked formation. Figure 3 is an illustration of different types of Microvias.

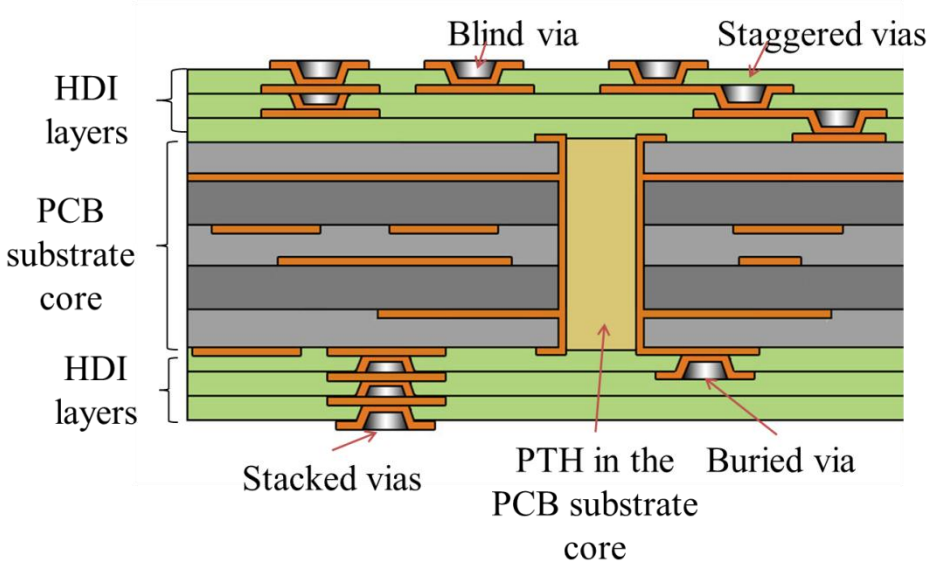

Figure 3- Schematic of different types of microvias

The number of layers in an HDI board can be presented in X+N+X format where X represents the number of HDI layers and N represents the number of the core layers. An optical image of a 3+6+3 board can be seen in Figure 4. Where top and bottom 3 layers representing the HDI layers where the middle 6 layers are the traditional PCB design board. It has to be mentioned that here we cunt the number of copper traces so, there are 12 layers of copper trace and 11 layers of board in the middle of them. Out of 5 layers of traditional board we have here, there are 3 prepreg layers that are used to contain the two core layers.

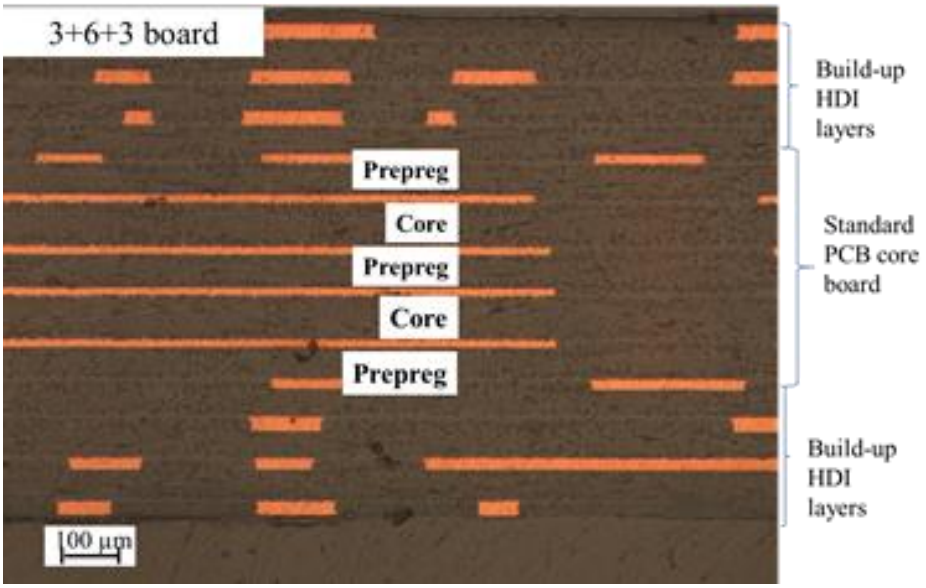

Figure 4- A 3+6+3 HDI board

Prepreg stands for pre impegrated and is uncured fiberglass-epoxy resin (which will harden when heated and pressed) used to stick the core boards together and isolate the copper layers from each other. Some may define a specific thickness range to identify the prepreg from core however thickness of the layers are set to give the electrical characteristics and may vary from manufacturer to manufacturer and it is not correct to use it as an identification criterion. The best way to identify the prepreg is to see which direction is the smooth side of the copper trace is facing. Every copper trace has a rough side and a smooth side. The rough side is better with cohesion and core layers do not have the stickiness that prereg have so the rough side of the copper trace is facing the core layer to hold it.

The boards under the current study are boards for hand held application as it can be seen of figure 5 and as it is shown in Figure 4, they are 3+6+3 HDI boards having both buried and blind vias. They can be single layer, two layers and three layers stacked microvias with copper filling.

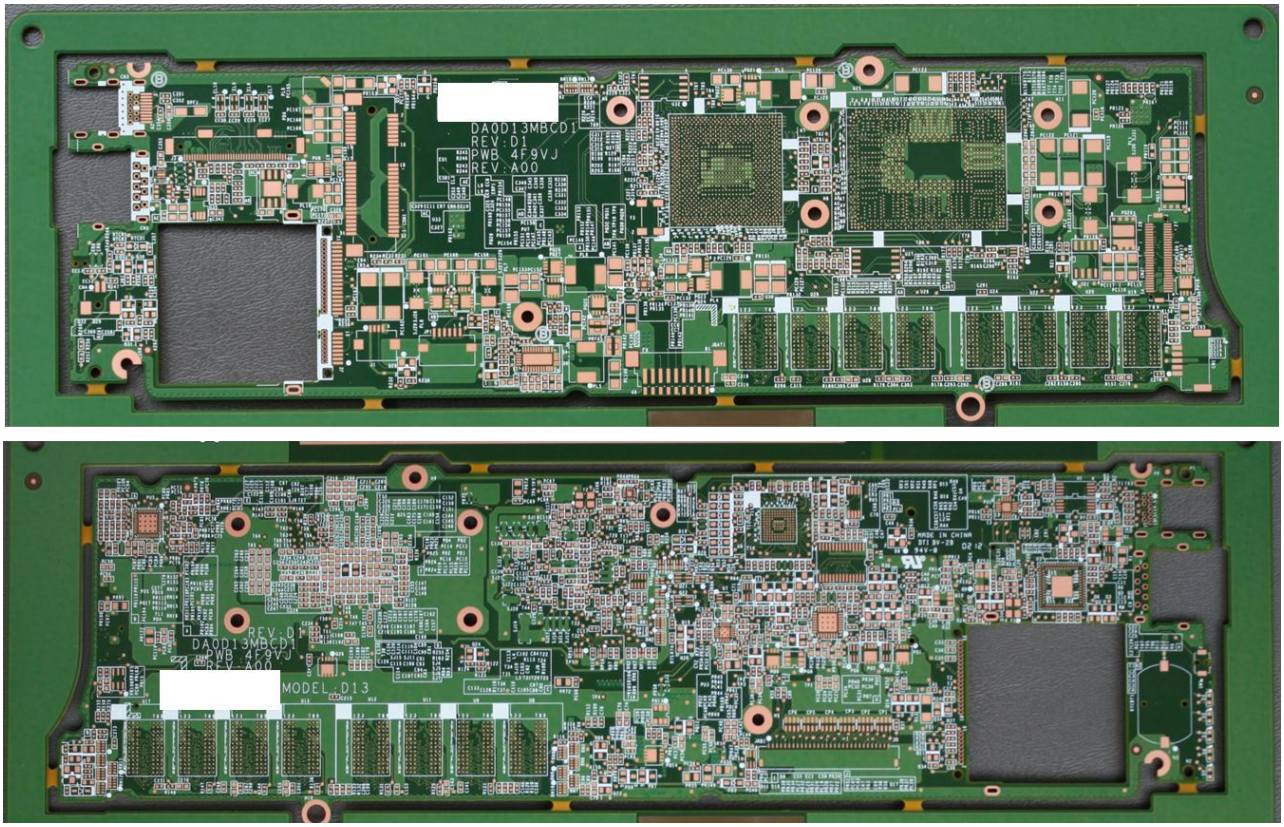

Figure 5- Boards under investigation

2. MOTIVATION

During the manufacturing and due to defective process, some defects might be introduced to the boards and in the case of this study, the microvias are not completely copper filled and there are some voids in them. Further screening using x-ray shows the presence of this voiding in the micorivas clearly. These voiding do not have any specific pattern to follow and they can be seen all over the board at any locations. Sometimes they can be seen in the adjacent microvias whereas sometimes they are on the microvias on different planes. Figure 6 shows an x-ray image of the board.

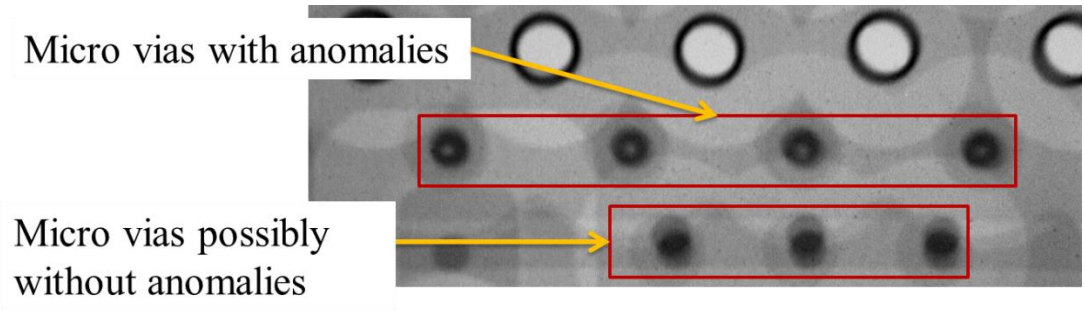

Figure 6- X-ray image of the micovias

As it can be seen from the bottom row, the Microvias are expected to be dark circles which represents the copper filling however as it can be seen from the top row, there are bright spots within the dark circles which shows that there are some material is missing. Further investigation of the boards through cross-sectioning reveals that the x-ray inspection can only detect relatively bigger voids while smaller voids remain unnoticed under x-ray inspection. In other words, the bottom row in figure 6. can still have voids and x-ray inspection is not able to detect them. Boards from two different manufacturers were investigated, one with excessive number of these anomalies in their Microvias (results of cross-sectioning shows almost 50% of the Microvias have voids) while the other board has less number of voided Microvias (results of the cross-sectioning shows about 25% of the Microvias are voided).

3. LITERATURE REVIEW:

In this part we investigate the current literature related to our case. This section is consisted of three main sub-sections. Microvias in PCBs, microvias in surface mount substrates and plated through holes. A fourth section is also dedicated to the IPC standards regarding the acceptability and quality assurance of PCBs in general with a focus on the standards that are out there exclusively about HDI boards.

2.1. Micro Vias in Printed Circuit Boards

Ji et al. [5] investigated the failure mechanism of the printed circuit boards in cell phones. The investigation was conducted after some devices failed in the field and returned to manufacture to find the root cause of the failure. The HDI printed circuit boards in this study contain single layer blind microvias. The failure site was observed as the target pad where it experiences larger stresses when thermally and mechanically loaded. In some of the cases micro cracks were observed whereas in other cases, a complete crack with delamination from the pad was seen. Figure shows an example of the delamination on the microvia pad that was observed by Ji et al. [5]

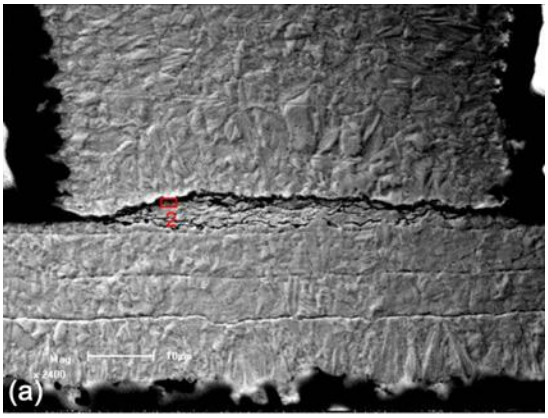

Figure 7- Delamination at the microvia pad [5]

These cracks result in open circuit and the discontinuation of the current. The results show that exceeding current density decreased the ductility of the plating layer under which condition cracking happened. The low ductility of the material is related to the presence of sulfur which was detected during the EDS analysis. The sulfur is a part of the cleaning material that was used during the plating process and after cleaning. Excessive use of the cleaning solutions

led to the introduction of additional sulfur on the surface which later on segregated into the copper. The brittle sulfides such as Cu_2S at the grain boundaries acted as nucleation sites which grew as a set of three dimensional islands of CuS or Cu_2S which were the location of crack initiation.

Liu et al. [6] investigated the effect of geometry on the reliability of single layer microvias, 5 different microvia diameters were used in this study. 25µm, 50µm, 75µm, 100µm and 125 µm. in order to assess the reliability, liquid to liquid thermal shock test (-55 to 125 ˚C) was used. The dwell time at each temperature extreme was chosen as 5 minutes with 10 seconds of transition time between the cold bath and hot bath. The test vehicle was ITRI-2.4 from Interconnect Technology Research (ITRI). The microvias were built in daisy chains structures which were made of made up of 4 subsets of 50 vias for a total of 200 vias per chain with via diameters of 25 µm, 50 µm, 75 µm, 100 µm, and 125 µm. A .375mm diameter capture pad was used for all the microvias. The fabrication was in a way that electrical resistance of each coupon could be measures separately. At the same time on each coupon the resistance of each row was measureable. The test vehicles were taken out of the chamber every 100 cycles for electrical resistance measurement. A 10% increase in electrical resistance was considered as failure. After 2000 cycles, one Microvias of 50 µm diameters failed while the rest passed the 2000 cycles. Table show the results of Liu et al. [6] work.

Table 1- Thermal shock results of Liu et al. [6]

Cycles	50 µm	75µm	100 µm	125 µm
2,000	1st failure at 1,000 cycles	Pass	Pass	Pass

After detection the failures, the test vehicle was taken out, cross sectioned and a failure analysis performed on it. Cracks were observed at the target pad of the failed sample. It is well known that CTE mismatch between the dielectric film and the copper on via walls is one of the main causes of microvia interconnect failure. It was also observed that incomplete cure of the polymer dielectric material was a potential source of failures and substrate rejects. Partially cured dielectric films may result in delamination and other instabilities during subsequent metallization and processing. Curing processes need to be monitored to fully cure the interlayer dielectric based on the equipment in use, in addition to the material vendor's recommendation. As for the samples that did not fail, the cross sectioning shows that the copper plating on the via wall and bottom in this case is uniform and the thickness is comparable to the surface plating thickness. This resulted in a much more reliable microvia interconnect structure.

Liu et al. [7] investigated the reliability of single layer blind vias. The test vehicle was 1+2+1 board designed for process development and reliability characterization. Three types of interconnect daisy chain structures were designed for process evaluations and thermal reliability tests: embedded through holes, blind microvias, and combinations of blind vias and through holes. In order to observe individual blind via behavior changes during thermal reliability assessment, the daisy chains were divided into 10 sub-chains. A large pad was designed for the entire daisy chain test. A small pad was designed for the sub chain test. In the design of the daisy chain interconnect structures, the blind via diameters were 25, 40 and 50ìm and the through hole was fixed at 50 µm.

The accelerated testing method for this experiment was r air to air thermal shock test (-55 to 125˚C). Samples were taken out of the chamber and checked for failure every 100 cycles. Electrical discontinuity was considered as failure mode. For unfilled microvias first failure was

observed on 500 cycles whereas for filled microvias, the first failure observed on 800 cycles. Failure analysis on failed samples found that there was a very thin layer of dielectric residue remaining on the bottom of via. The residual dielectric material increased via resistance and caused via failures during testing.

2.2. Micro Vias in Surface Mount Substrates

Ramakrishna et al. [8] investigated the effect of dielectric material and geometry parameters most importantly the wall thickness on the reliability and thermo mechanical behavior of single layer blind microvias. Test vehicle consisted of 28 test coupons fabricated on both sides of a board. Each test coupon had 8 rows of 17 microvias of the same diameter microvias. Electrical resistance probing was used as the monitoring the failure mode method. The design of the board was in a way that besides the entire daisy chain, the electrical resistance of the individual rows could also be measured in order to find the individual failures. Four different micro via structures consisting of diameters 50µm, 75µm, 100µm and 125µm were selected for the test.

Air to air thermal shock test (-55 to 125 ˚C) with 10 minutes dwell times at each temperature extreme with 10 seconds of transition time between the hot and cold chambers was chosen in order to perform the accelerated testing. After 2000 cycles, no failure was found on the samples with 125µm whereas 14.3% of 100µm and 73% of the 75µm samples were failed during this period. Cross sectioning was performed on the failed samples in order to isolate the failure sites and investigate the failure mechanisms. The failure mechanism observed was crack propagation in two primary regions. The first one is the interface between the capture pad and the wall and the second region is the interface between the target pad and the microvia wall. Results of the investigation show that the electroplating of the wall near the base pad of the

microvia is not as thick as that of the wall thickness in the other regions. This could be one reason; attributed to the acceleration of this failure mechanism. The thermal shock condition introduces cyclic tensile and compressive stress. These stresses and their corresponding strains are causes due to strained that were caused by the geometry of microvia and also the effect of the dielectric material. The latter one is the source of CTE mismatch between the microvia and the surrounding epoxy layers. Some regions of the microvias experiences plastic strains which make them susceptible to low cycle fatigue and early life failure. The conclusion is different process parameters that affect geometry and yield in the microvias, affect the reliability of the boards. The thickness of the dielectric material and the microvia geometry parameters are the key factors that can enhance the thermo mechanical behavior of the boards.

Xiong et al. [9] investigated the effect of an increase in the interface area between microvias and underneath copper layer on reliability of microvias. Figure 7 shows the standard contact of the microvia (a) and the microvia contact with additional etching (b) to see how the extended surface affects the reliability of the microvias.

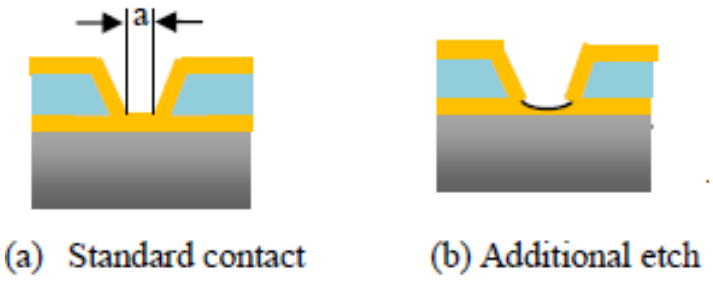

Figure 8-the width of the interface changed to see the effects of area on microvia reliability [8]

Temperature cycling (-65 to 150˚C) was chosen as the accelerated testing method, samples were taken out every 100 cycles to check the electrical connection. Electrical discontinuity was selected as the failure mode. Results of the single microvias samples show that

the increase in the interface area increases the number of cycles to failure. Additional etching which led to extra interfacial contact area reduced the induced cyclic tensile and compressive strains that happened during the cycling because of the CTE mismatch between the microvias and the surrounding epoxy material.

2.3. Plated Through Holes

Reliability of plated through holes which are the means of power and signal transportation in non-HDI layers are worth of investigation too. CTE mismatch between copper and dielectric material leads to localized strains and cracking in PTH circumferential copper metallization [10], [11] Lowering the aspect ratio of PTH helps to reduce the maximum stress on the PTH which increases the number of cycles to failure [11], [12].

2.4.IPC Standard on Microvias

Several sections of IPC standard address the microvias is HDI boards.

IPC/JPCA-2315, “Design Guide for High-density Interconnect Structures and Microvias” [3] provides guideline of HDI technology, explains the definition of common terms in microvia structure such as target pad and capture pad, goes over the process of micrvia formation such as laser ablated vias, wet/dry etched vias and photoelectric vias. Other materials that this standard covers are the basic design aspects of the microvis such as wiring capacity and wiring factors, I/O variables and finally the product classifications based on HDI type.

IPC-2226, “Sectional Design Standard for High-density Interconnect (HDI) Printed Boards” [4] establishes requirements and considerations for the design of organic and inorganic HDI printed boards and the forms of component mounting and interconnecting structures.

IPC/JPCA-4104, “Qualification and Performance Specification for Dielectric Materials for High-density Interconnect Structures (HDI)” [13] discusses the qualification methods for dielectric material in HDI boards, dimensional, mechanical, electrical, chemical and environmental requirements for dielectric and conductive materials. It also goes over the inspection requirements of test equipment and lab facilities along with inspection of products for delivery and statistical process control of the production lines.

IPC-6016, “Qualification and Performance Specification for High-density Interconnect (HDI) Structures” [14] establish the specific requirements for organic HDI layers with microvia technology. These requirements are about all the components and also the process that are involved in the production of the board. Some examples of these requirements are the ones for materials, laminates (both rigid and flexible), metal foils, plantings and coatings, solder resist, hole fill material, marking inks, edges, solder ability and adhesion, surface dielectric imperfections, workmanship structural integrity, solder resist requirements, insulation resistance and so on. This standard also discusses about the reliability and quality test methods for HDI printed circuit boards, the methods that are discussed in this manuscript are thermal stress methods, thermal and mechanical shock, vibration, environmental testing, impedance testing, fungus resistance and cleanliness.

The most important IPC standard for this work is however IPC-6012 [15] “Qualification and Performance Specification for Rigid Printed Boards,” this standard, discusses so many

aspects that were already expressed in the IPC 6016 such as the requirements for different materials and processes. Different types of reliability testing. However the most important aspect that IPC-6012 mentions is the acceptability of the micro vias.

IPC 6012D states that in copper filled microvias, voids "shall be acceptable provided they are completely encapsulated, in total do not exceed 25% of the area of the filled microvia." Figure 9 is an illustration of this criterion.

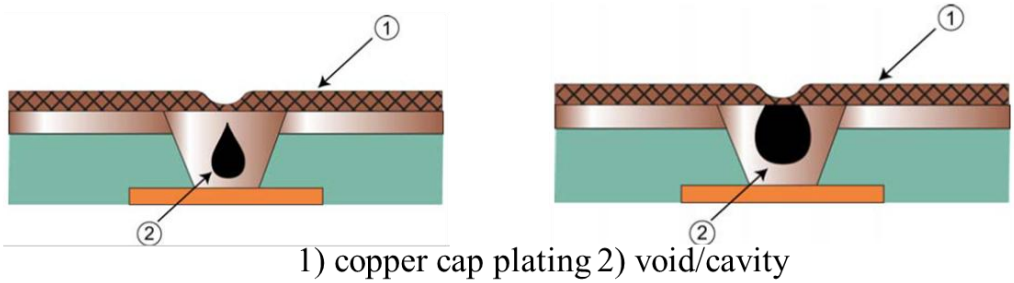

Figure 9- acceptance criterion for voids based on IPC 6012 D [15]

This acceptance criterion that is mentioned in the IPC standard is highly vague and unclear. For example nowhere in this standard is discussing about the shape of the void. As it is clear triangular and rectangular and in general shapes with sharp angles have stress concentration on these locations which with continuous loading and unloading during the life cycle conditions, these stress concentrations will lead to tensile and compressive strains, these strains are the major source of failure. On the other hand, shapes with round corners experience less stress concentration compared to shapes with sharp angles which make them more reliable.

Another aspect that is not addressed in this acceptance criterion is the location of the void and more importantly the wall thickness around the void. As it was discussed in the previous

literature, one of the most susceptible locations on the microvias are where the wall thickness is the lowest. The thin walls experience the highest stress concentration which sometimes can lead to plastic deformations which will result in early life failure or in other words low cycle fatigue.

In general, qualifying the microvias based on the void area ratio is not the best approach. If we assume that the standard measures the area of the void on a cross sectioned sample which is ground up to half of the diameter of the microvia, there is no insurance that at this location the void has its maximum diameter, in other words the void is not symmetric so the maximum area can happen at any given plane. Another issue is it doesn`t address the voids on the edges of the microvia and if they have to be counted in this formula or not. Also multiple voids on the microvia is not addressed either.

And the last problem is, it does discuss voiding in the stacked microvias between different layers. What would be the situation if there are multiple voids on different layers for example one void on layer one and another void on layer two? How this situation should be handled? For example the whole stacked microvia is considered one and then the voiding area is the cumulative area of the voiding or the voiding in each of the layers treated independently from other layers? And treat the stacked microvias like several single layers one.

4. EXPERIMENT PROCEDURE:

As it was seen from the literature, presence of voiding in the stacked microvias and their effect on the reliability of the board was not investigated.

Cross sectioned samples were made from two different board manufacturers in order to be subjected to thermal shock test. There are 10 samples, 5 from each manufacturer containing all different possible combination of microvias. The samples were ground and polished based on

the instructions of IPC-TM-650-2.1.1 “Test Methods Manual-Micro Cross Sectioning” [16]. The cross sectioning was performed up to the half of the diameter of the microvias in order to get the maximum stress concentration so the maximum strains. Samples were chosen in a way that there is a row of microvias rather than a single microvia, this row contains microvias with voids and without voids. Figure 10 shows an x-ray image of a cross sectioned sample. As it can be seen, the last two microvias on the right do not have any voids whereas the other four microvias on the left are voided.

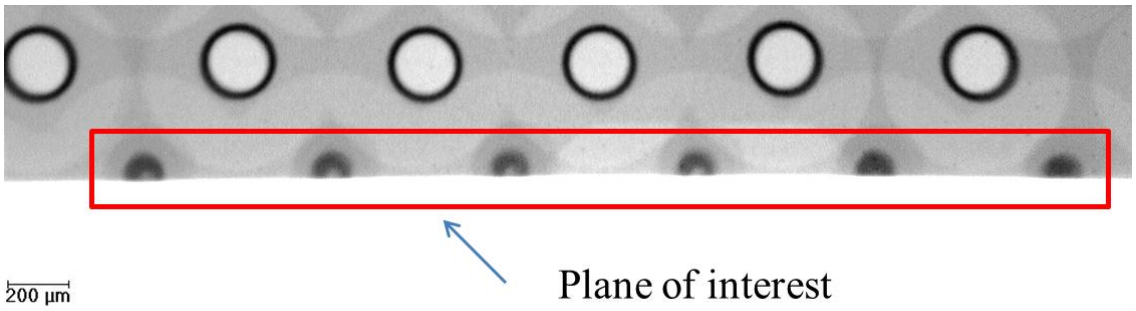

Figure 10- X-ray image of the cross sectioned sample

After grinding and polishing the samples, the were etched based on the instruction of the IPC-TM-650-2.1.1 “Test Methods Manual-Micro Cross Sectioning” [16] standard using a solution containing 25 ml of hydrogen peroxide with concentration of 5% and 25 ml of ammonium hydroxide with the concentration of 30% in order to remove the copper residuals from the surface of the samples that were made during the cross sectioning process. **Table 2** represents the details of the samples that were used in this study. The terms single-layer, two-layer and three-layer microvias are referring to the number of board layers that microvias are connecting to. For example figures 9-11 show a cross sectioned images of one to 3 layer microvias.

Table 2-Summary of microvias information

Sample #	# of microvias	# of 3 layer microvias	# of voids in 3 layer microvia	# of non voided microvia in 3 layer microvia	# of 2 layer microvias	# of voids in 2 layer microvia	# of non voided microvia in 2 layer microvia	# of 1 layer microvias	# of voids in 1 layer microvia	# of non voided microvia in 1 layer microvia	# of non voided microvias	# of voids
150	12	10	7	4	0	0	0	2	1	1	5	8
152	5	4	4	1	0	0	0	1	0	1	2	4
153	13	9	4	6	0	0	0	4	1	3	9	5
155	9	9	6	5	0	0	0	0	0	0	5	6
156	12	0	0	0	12	3	10	0	0	0	10	3
204	4	4	0	4	0	0	0	0	0	0	4	0
208	6	3	0	3	3	0	3	0	0	0	6	0
222	18	16	10	8	0	0	0	2	0	2	10	10
223	8	8	0	8	0	0	0	0	0	0	8	0
224	7	7	5	2	0	0	0	0	0	0	2	5
Total	94	70	36	41	15	3	13	9	2	7	61	41

The first 5 samples which are 100 numbers are from board vendor 1 and the last 5 samples which are 200 numbers are from board vendor 2.

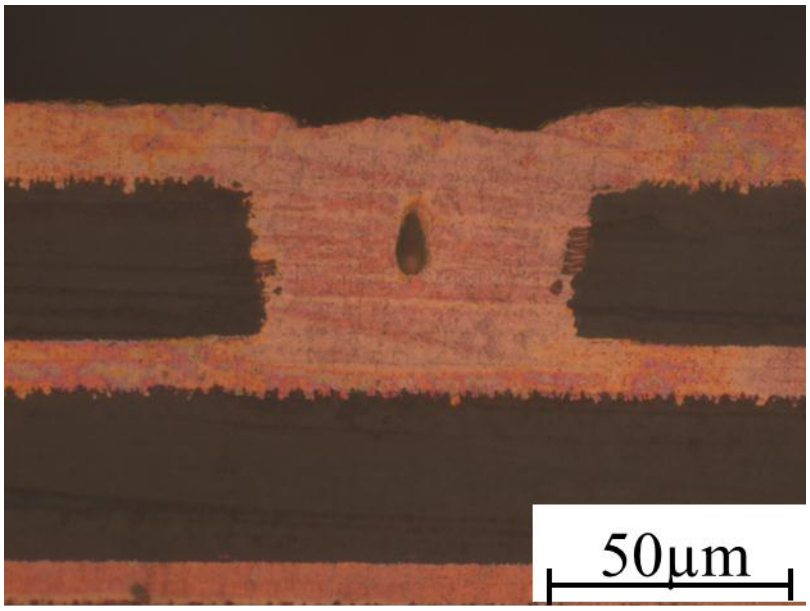

Figure 11- One-layer cross sectioned sample

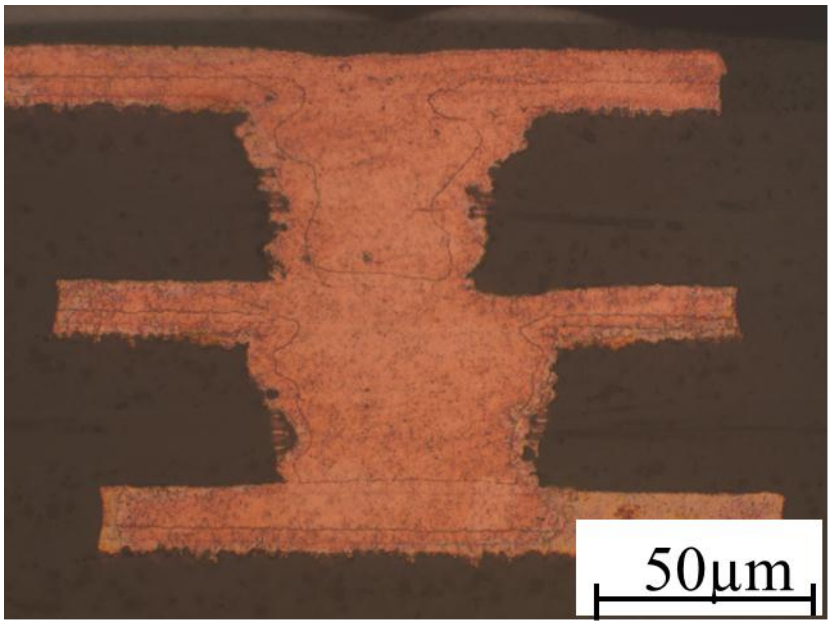

Figure 12- Two-layer cross sectioned sample

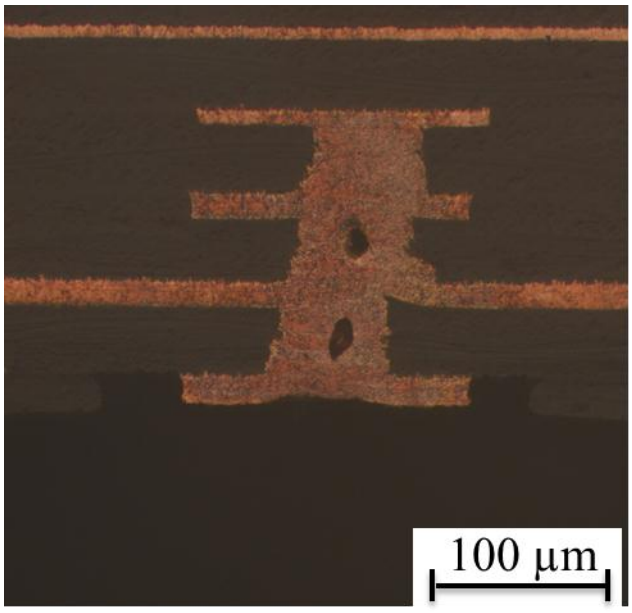

Figure 13- Three- layer cross sectioned sample

Some observations:

1. Voids are present in all 1-layer, 2 layer and 3-layer microvias from board vendor 1
2. There are no voids in 2-layer microvias from board vendor 2
3. There are no voids in 1-layer microvias from board vendor 2
4. For boards from both vendors there are 3-layer microvias which have 2 voids

In order to evaluate the robustness of the printed circuit boards, an accelerated testing method is needed to evaluate the effects of the voiding on the microvias reliability. The acceleration mechanism for reliability testing of printed circuit boards is a function of parameters such as thermal coefficient of expansion (CTE) of the materials used in the board along with the temperature difference of the hot and cold baths. These parameters determine the stresses introduced to the board and the reliability acceleration that is provided. Thermal shock conditions are made by moving the samples between the two temperature extremes in a short transition time to get the maximum possible stress and before stress relaxation of the samples in the ambient temperature.

In order to choose the maximum temperature of the thermal shock test, the glass transition temperature (T_g) of the board had to be measured. To avoid testing artifacts, such as material delamination and breakdown, the maximum temperature in the test should be lower than the glass transition temperature (Tg) of the dielectric materials. T_g can be obtained by performing thermo-mechanical analysis (TMA) test. The procedure and requirements of the TMA test are presented in the IPC-TM-650, 2.4.24C standard. Figure 12 shows the results of the TMA test on the board and it can be seen that the glass transition temperature is 154 ˚C.

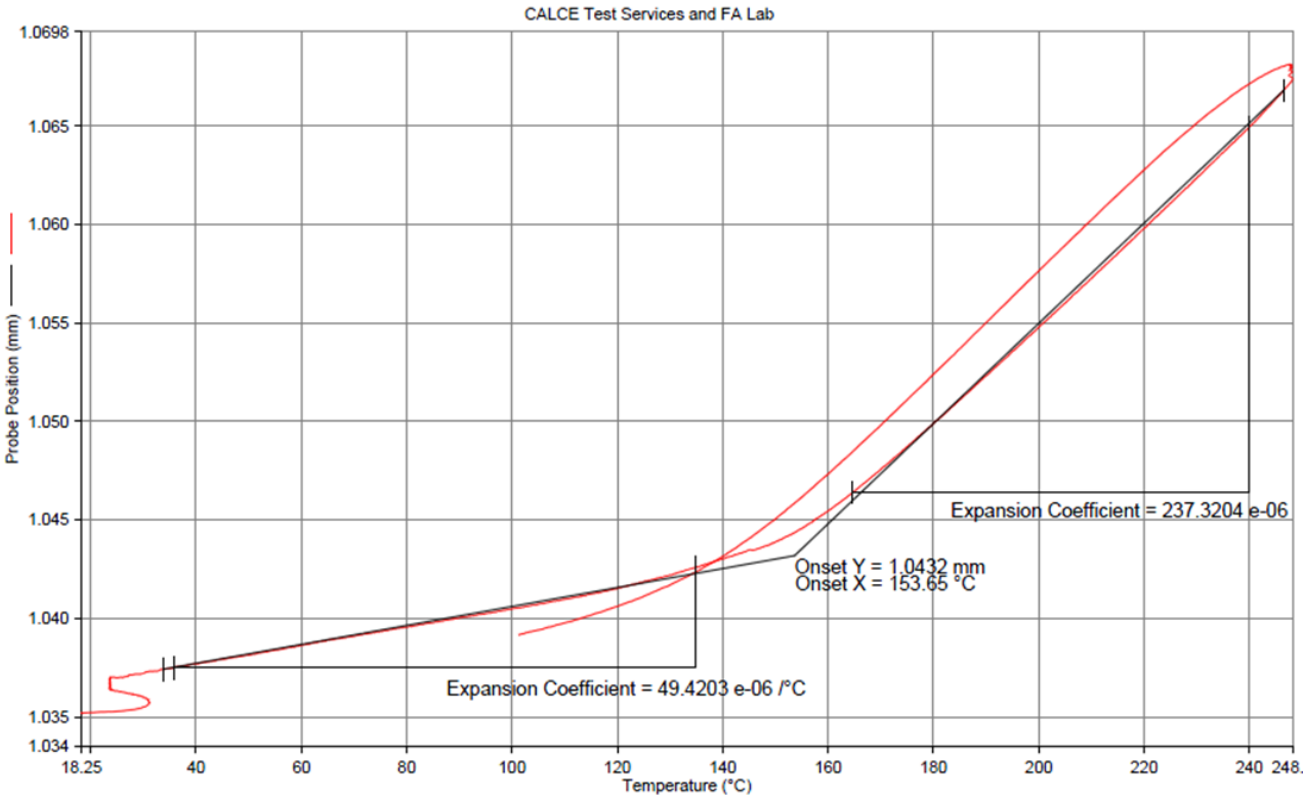

Figure 14- TMA results of the PCB

Glass transition temperature of 154 ˚C means that any extreme temperature below this number is appropriate for the test without damaging the dielectric material of the boards.

Liquid to liquid thermal shock test conditions were chosen based on IPC-TM-650-2.6.7.1 [17] standard as -55˚C to 125˚C with 15 minutes dwell time at each temperature extreme and transition time between cold and hot bath of 9 seconds. Figure 15 shows the configuration of the shock test for one cycle.

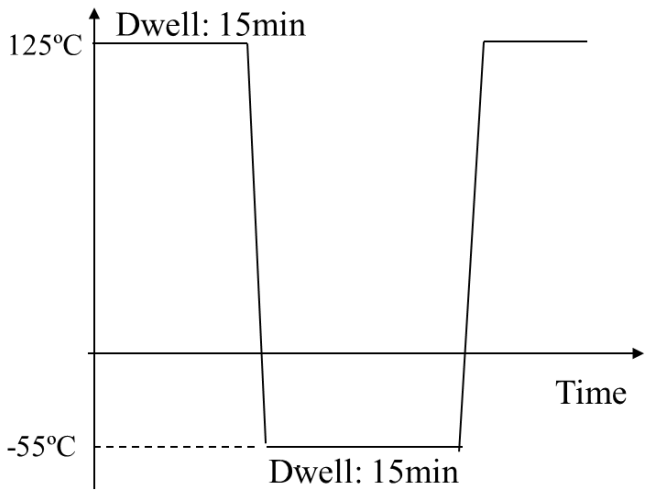

Figure 15- configurations of the thermal shock test for one cycle

As for the chamber ESPEC TSB 2.5 liquid to liquid shock chamber available at Center for Advanced Life Cycle Engineering (CALCE) failure analysis labs was used for the accelerated testing.

Samples were taken out of the chamber on certain intervals for optical inspection. Figure 16 shows these time intervals.

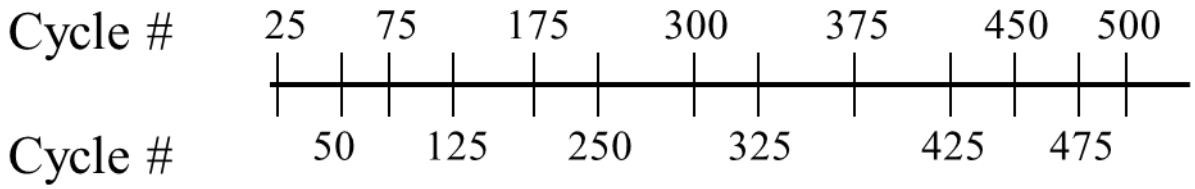

Figure 16- Time intervals for sample inspection

It has to be mentioned that, the usual approach in performing the test on microvia reliability as it was seen earlier in the literature review is using the daisy chain samples with a certain number of rows of microvias and monitor the electrical resistance change as the failure

mode in order to detect the failure. In these tests the whole board was subjected to thermal shock conditions and after detecting the failure, boards were taken out and cross sectioned in order to perform the failure analysis however in our case, since the test specimens are actual field boards and not daisy chain test vehicle the approach has to be different. First of all on the whole board it is impossible to isolate a single microvia or a single row of microvia on the board in order to measure the resistance. For example figure 17 shows one location of the whole board and as it can be seen there are numerous number of microvias both next to each other and also on top of each other and finding a single current path between the is not feasible.

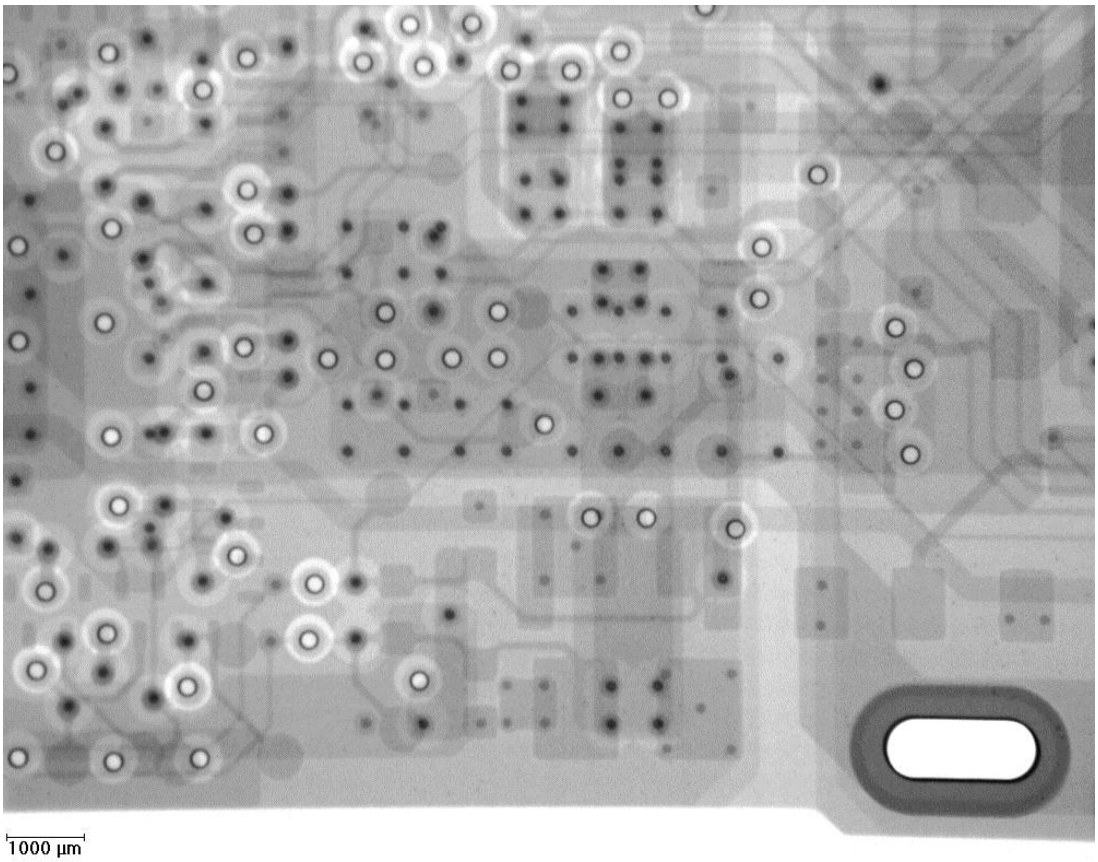

Figure 17- It is impossible to isolate microvias on the whole board

Second of all, after cutting the board and make the cross section samples, even in the cross sectioned samples, isolating a single microvia or a single row of microvia is almost impossible since in almost all the cases there is another microvia right behind the row of interest with an electrical connection to the main microvias which makes alternative path for the electrical current if the failure happens. This can be easily seen in the figure 18. If the probing performed on the front row, the current still can go through the back row of microvias.

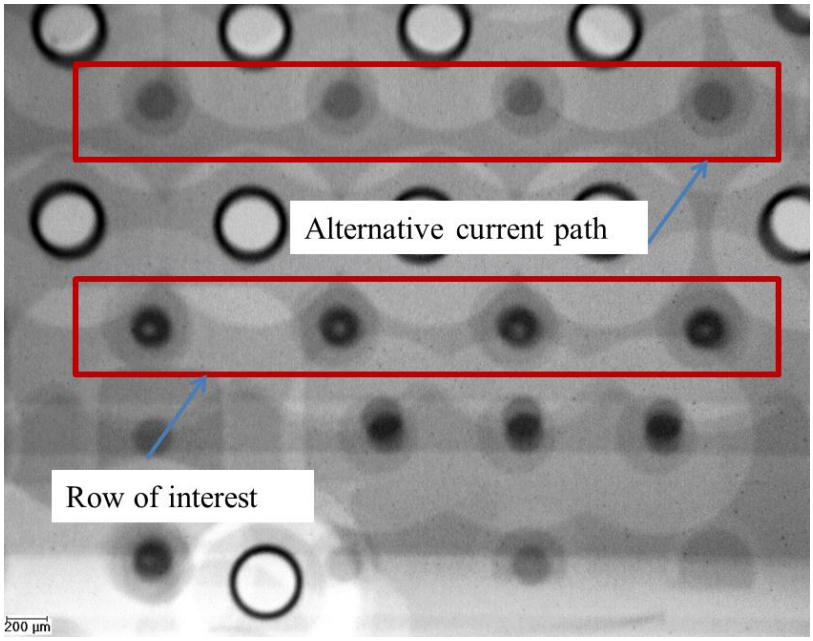

Figure 18- Alternative current path behind the row of interest

Also in the cross sectioned sample, current can go through parallel routes which is shared among the microvias, so if a failure happens, the current goes through an alternative route and failure cannot be detected. Figure 19 is a cross sectioned optical image of a sample which illustrates this concept along with the concept of another row behind the row of interest.

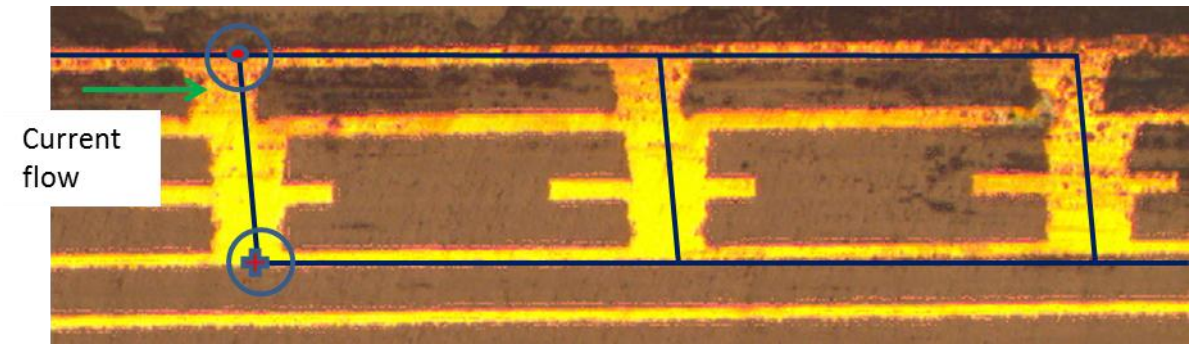

Figure 19- Cross section illustration of alternative current paths

Another issue with electrical resistance probing is the effect of probing tips on the surface of the samples. Using probes on the cross sectioned samples is not considered a nondestructive test, the probe tips put marks and scratches on the surface which may affect the stress concentration and time to failure. Also these scratched, will change the electrical resistance over the time too.

As a result, the best approach for detecting failures was making the cross sectioned samples, grinding, polishing and etching them as it was explained earlier and inspect them after specific number of cycles through optical microscopy in order to monitor all the changes that happen to the surface of the samples. By putting optical images of the samples from different stages of the test and comparing them, any change to the sample surface could be detectable. All the sample pictures were taken at 20X magnification while for so many samples depending on the stage of the test and dimensions of the microvias, other magnifications such as 50X and even 100X were used to detect all the minor changes to the samples. Based on the literature, failure modes such as cracking were expected to see in the samples.

5. RESULTS:

The liquid thermal shock test was performed for 500 cycles using 10 samples from two different board manufacturers. Samples were chosen in a way that the population covers all the possible scenarios such as 1-layer, 2-layer and 3-layer microvias, all these samples were both voided and non-voided so the effect of voiding could be detected on the reliability. Test samples were taken out of the chambers after certain number of cycles and inspected using optical microscopy to detect any changes on the surface. If any changes were observed, Environmental Scanning Electron Microscopy or E-SEM analysis was performed on them to confirm the changes. The following three failure modes were observed:

1. Initiation of cracks
2. Expansion of voids
3. Formation of new voids

The earliest cycle that the failure mode was observed was at 325 cycles. Figure 20 shows the sample 153 from vendor 1, there are two voids present in this sample, one on the first layer and another one on the second layer. At the initial condition of the test (0 cycles), there was no crack observed at the surface of the sample, optical images of the state of the sample at 175 cycles shows that still there are no signs of failure on the sample surface however the images from 325 cycle reveal that there is a change on the surface is happening at the bottom of the top void. There is some sign of a crack that is forming at the sharp corner of the void and is moving towards the sharp corner at the bottom void.

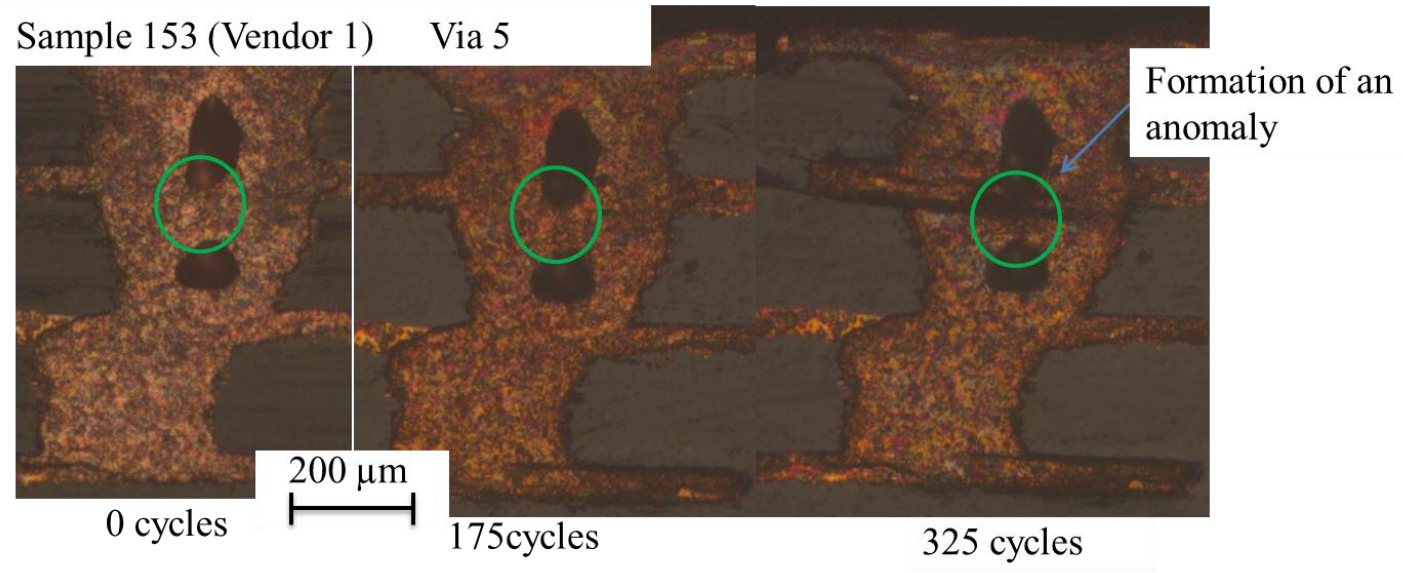

Figure 20-Formation of a void after 325 cycles

It has to be mentioned that during all the imaging process, the same microscope settings was used in order to be able to track the changes because if different settings were used, one to one comparison between the pictures from different states was impossible cause some of the changes on the surface could be related to the changes of the optical settings and different lights and filters that were reflected on the surface of the samples during different observations. For example if you take a look at the images on the figure 20, it can be seen from the color of the resin material that the optical settings were taken constant cause the resin color is almost the same however if you pay attention to the color of the copper, it can be easily seen that after 175 cycles there is a color change happening to the microvia. The reason for this color change is the oxidation of the copper due to exposure to the thermal shock conditions. It can be seen from the picture of 325 cycles, after the initial oxidation, the copper reaches a steady state and further discoloration occurs on the surface of the sample as it was seen at the earlier stages of the thermal cycling.

The 20X optical microscopy do not give a detailed image of the phenomena, in order to get a more detailed view of the anomaly; optical microscopy was performed at a higher magnification in order to get a better and more detailed of the surface change. Figure 21 shows an optical image of the samples 153 at its state at 325 cycles with 50X magnification. As it can be seen in this picture, it is clear that there is a crack initiating from the bottom of the upper void and is moving down towards the top corner of the bottom void.

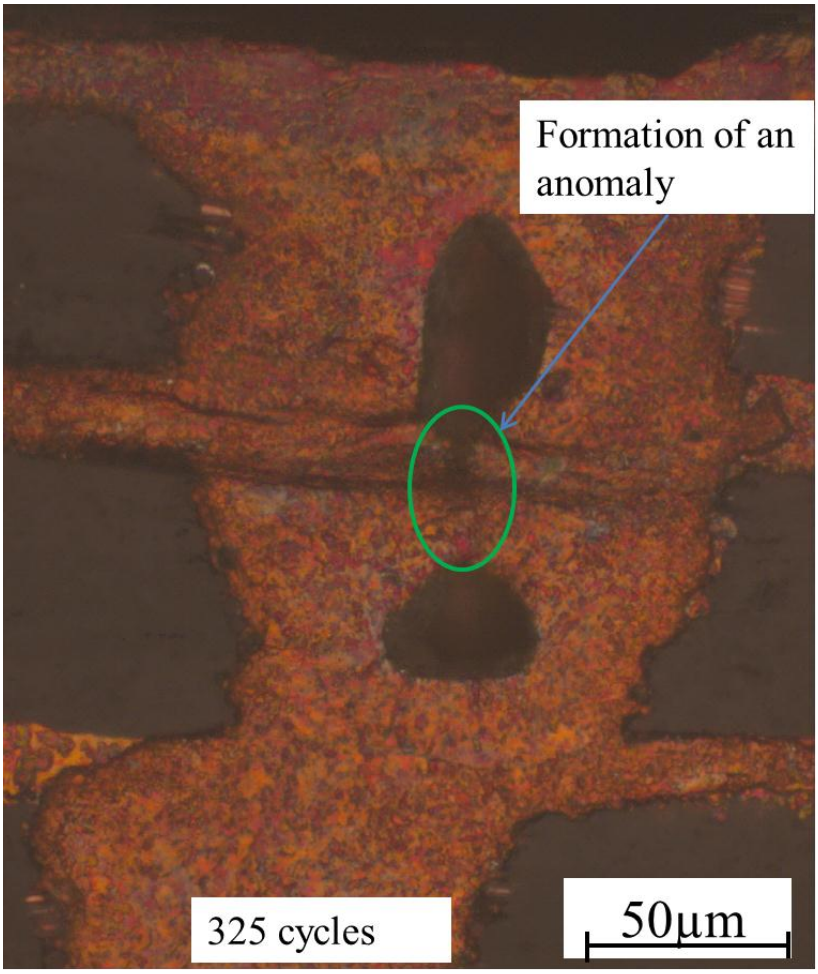

Figure 21- High magnification image of the sample 153

It is clear on the high magnification picture that is shown in the figure 21 that the anomaly which was detected in the lower resolution is initiating from the upper void, in this

image this anomaly is circulated with green and the anomaly is a darker line at the bottom of the void.

To further investigate this anomaly and make sure that it is a crack initiation, extra nondestructive test was performed. E-SEM analysis was used for the confirmation. Figure 22 shows an image of the failure at the bottom of the upper void.

Figure 22-Initiation of the crack at the bottom of the void

In order to get a better understanding of the crack, another higher magnification E-SEM picture was taken which is shown in figure 23. From this picture the shape and initiation of the crack can easily be observed.

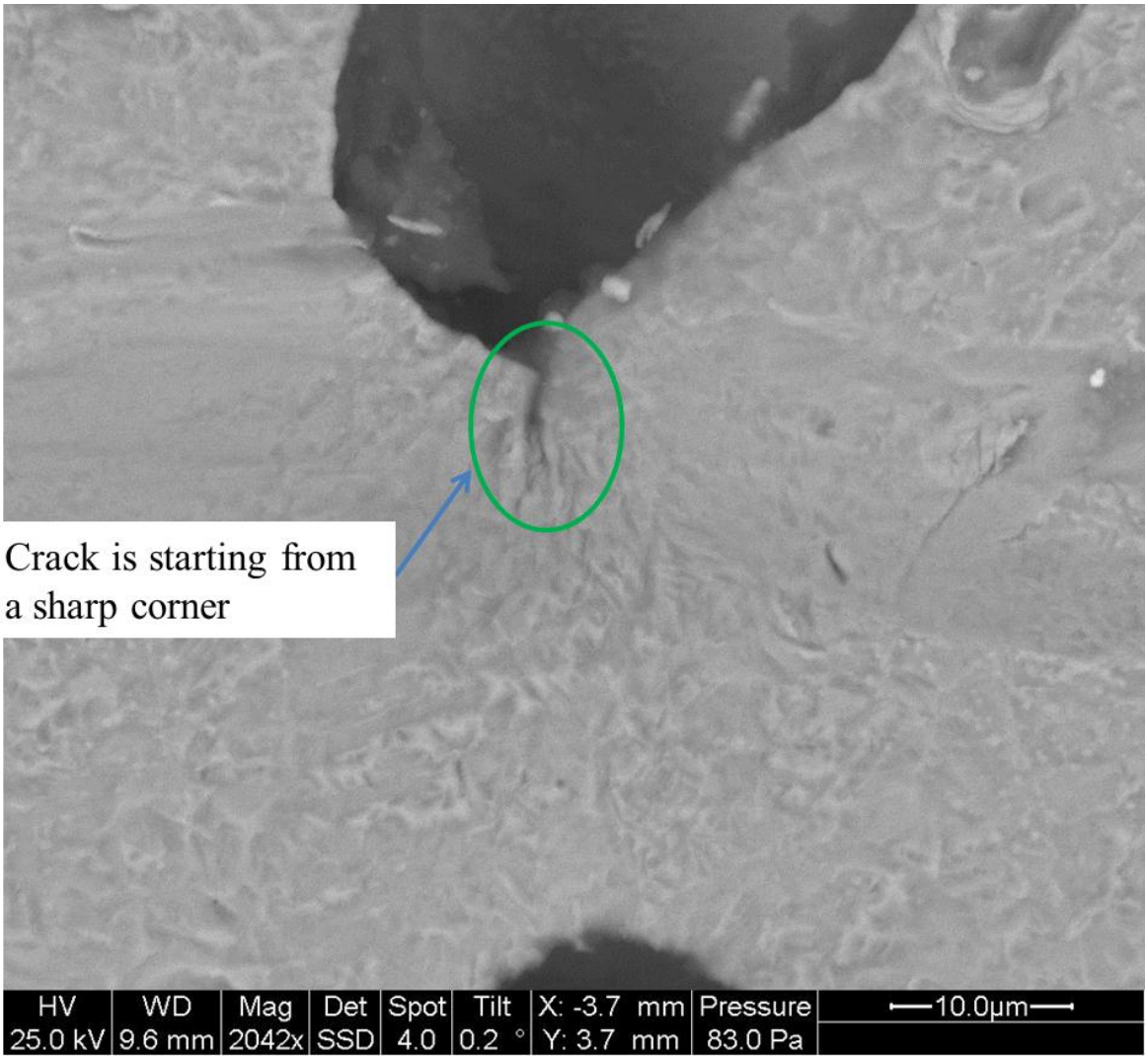

Figure 23- Higher magnification E-SEM image of the crack

Another form of the failure mode that was observed was the expansion of the voids. Figure 24 shows sample 156 which is a two-layer microvia. This microvia had two voids at the initial state of the cycling. As it can be seen from the 0 cycle's picture, there exists a crack at the bottom of the upper void.

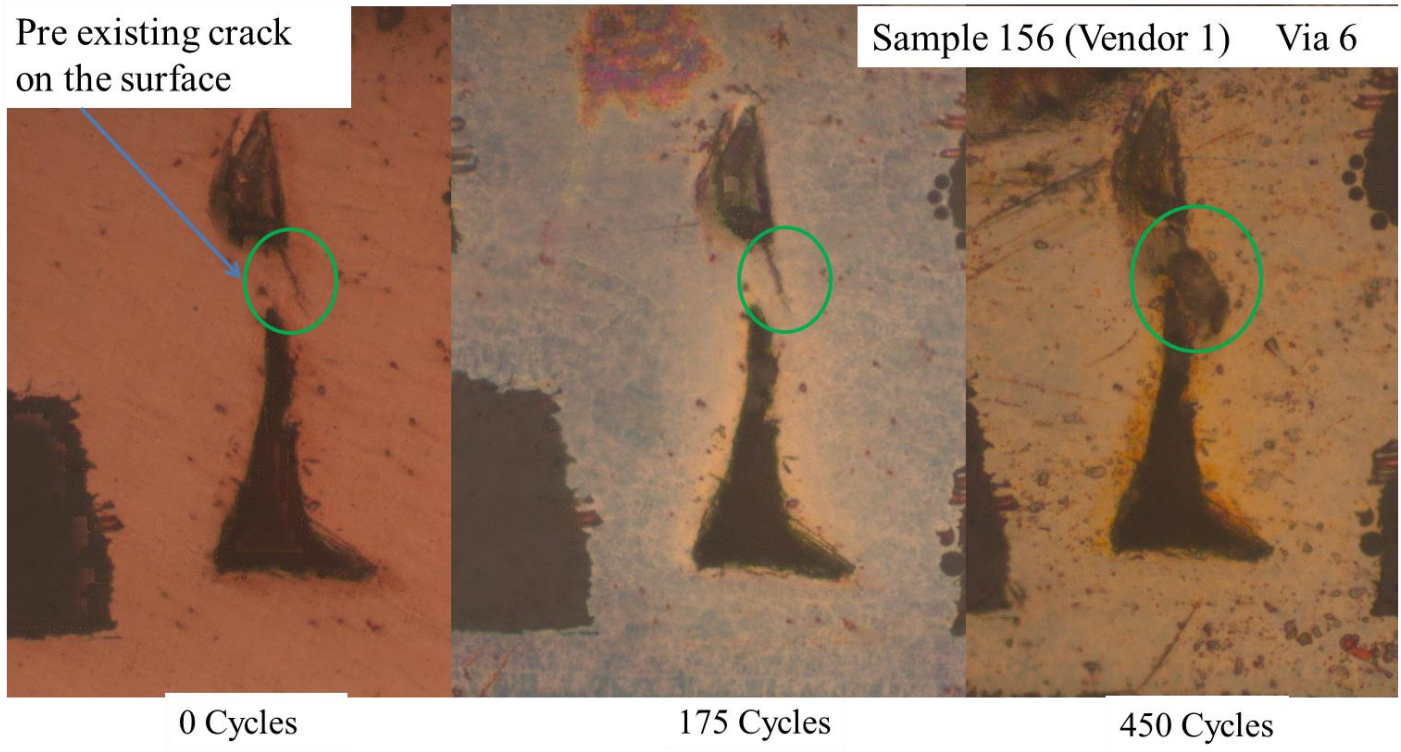

Figure 24- Sample 156 shows a crack propagation after 450 cycles

As it can be seen from the pictures, with further cycling the crack propagates and gets bigger, this crack propagation is a result of the stress concentration of surface of the initial crack.

From 0 cycles to 175 cycles there is a color change observed on the surface of the samples, it can be seen that, it turned from the reddish color of copper to a purplish color. The reason behind the color change is the usage of the methanol on the surface for the cleaning purpose. After taking out the samples from the liquid to liquid shock chamber, there are always

droplets of liquid left on the surface of the sample that sometimes seat on the surface of the sample and prevent getting a clear picture. In order to solve this problem, cotton swaps dipped in methanol which is a non-reactive alcohol with copper is used to remove the liquid leftovers. Most of the time this using this method successfully removes all the contamination but there are cases that contamination wasn`t removed from the surface. Traces of liquid still can be seen on some of the pictures.

In order to get a better image expanded crack, a higher 100X magnification picture was taken which can be seen on figure 25.

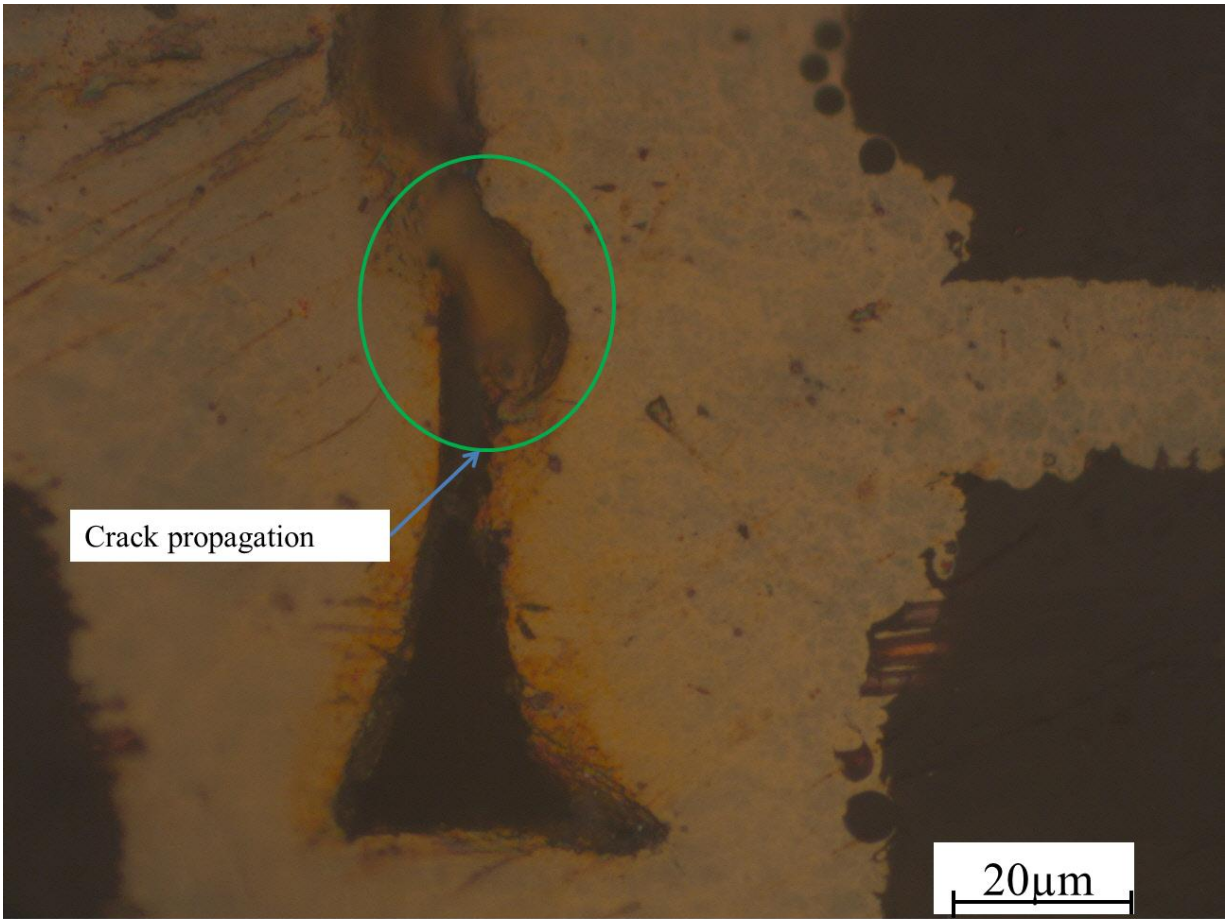

Figure 25- Higher resolution picture of the crack

As it can be seen from figure 25, the new opening is shallower than its surroundings voids. This indicates that is a newly formed void.

One the challenges of these experiments as it was mentioned earlier was the left overs of the liquid from the liquid to liquid thermal shock chamber. One persistent problem with this issue was sometimes these transparent liquids looked like new voids because they let the light pass through them during the optical microscopy and because of the light fraction, the looked blurry or in other words out of focus surface, something that was always seen in the voids. In order to confirm that what was seen in the sample 156 was crack propagation and not a light deflection because of the present of the contamination on the surface, E-SEM analysis was performed on the surface of the sample.

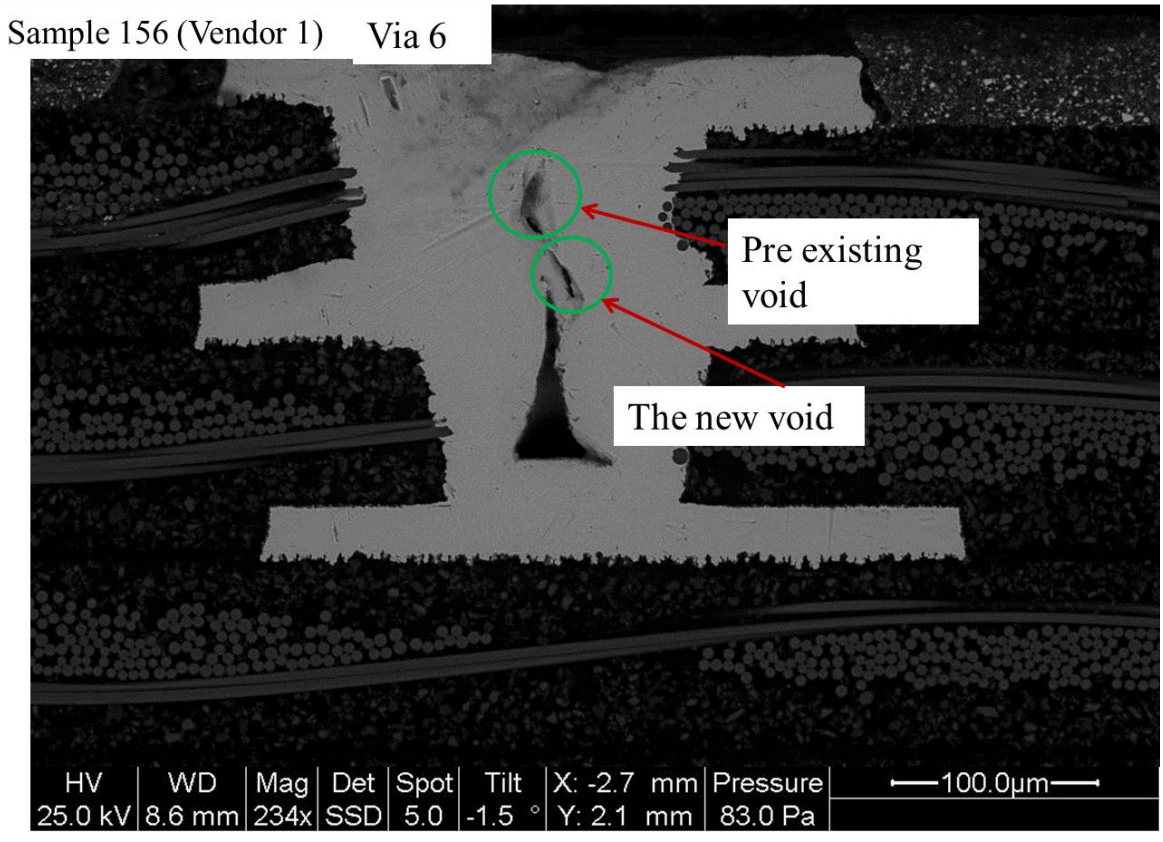

Figure 26- E-SEM image of sample 156 shows the crack propagation

A higher magnification E-SEM image was also taken to see the propagation of the crack in detail.

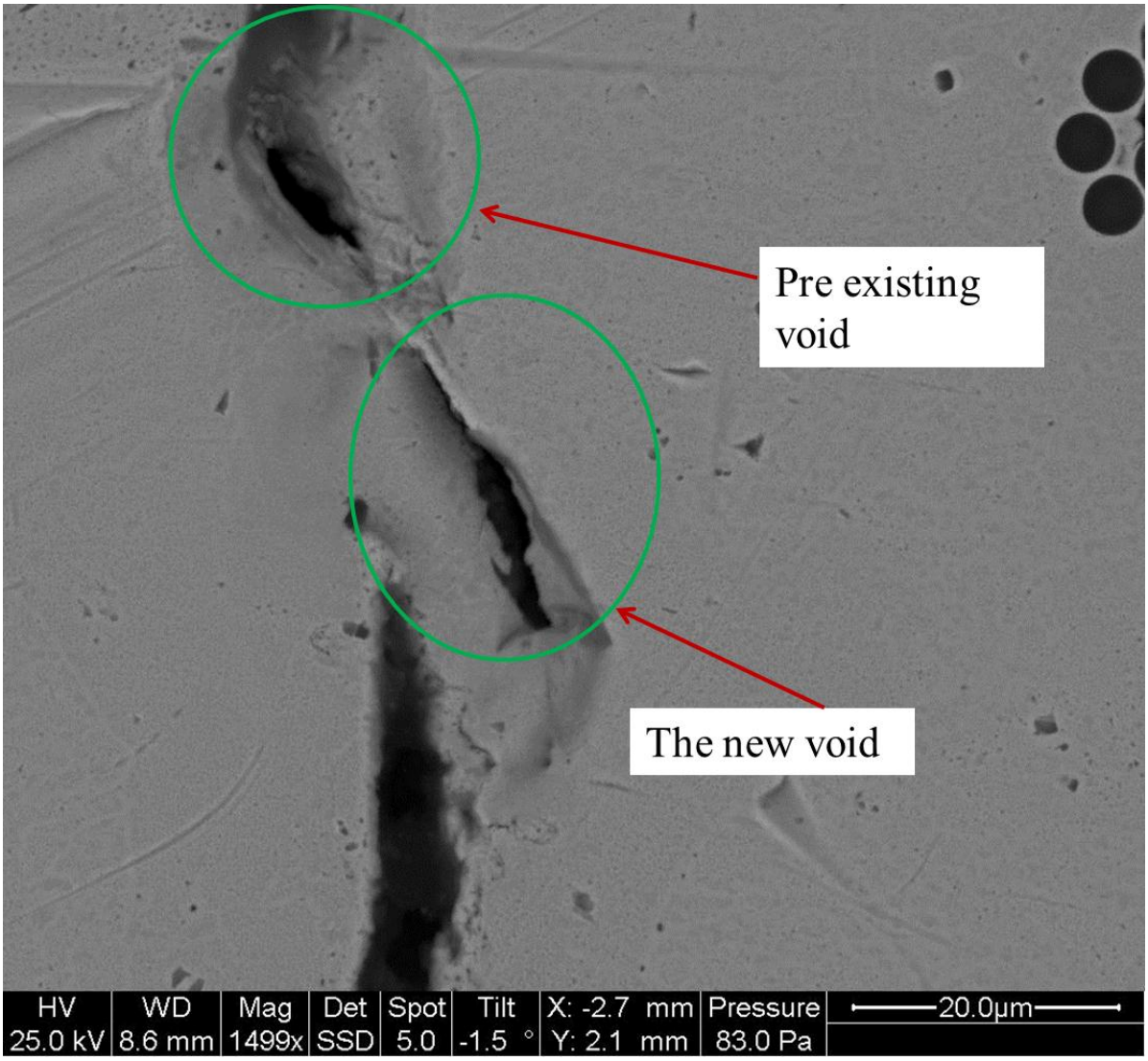

Figure 27- High magnification E-SEM image of the sample 156

As it can be seen in figure 27, the new void is in the same location of the initial void at 0 cycles. The new void is initiating from the upper void and moves toward the lower void, however at this stage of the test new void and the bottom void are not yet connected.

The last example that is going to be discussed in this thesis is the 3rd failure mode that was observed after 500 cycles of liquid to liquid thermal shock testing. This failure mode is the formation of new voids which was seen on a non-voided single layer microvia.

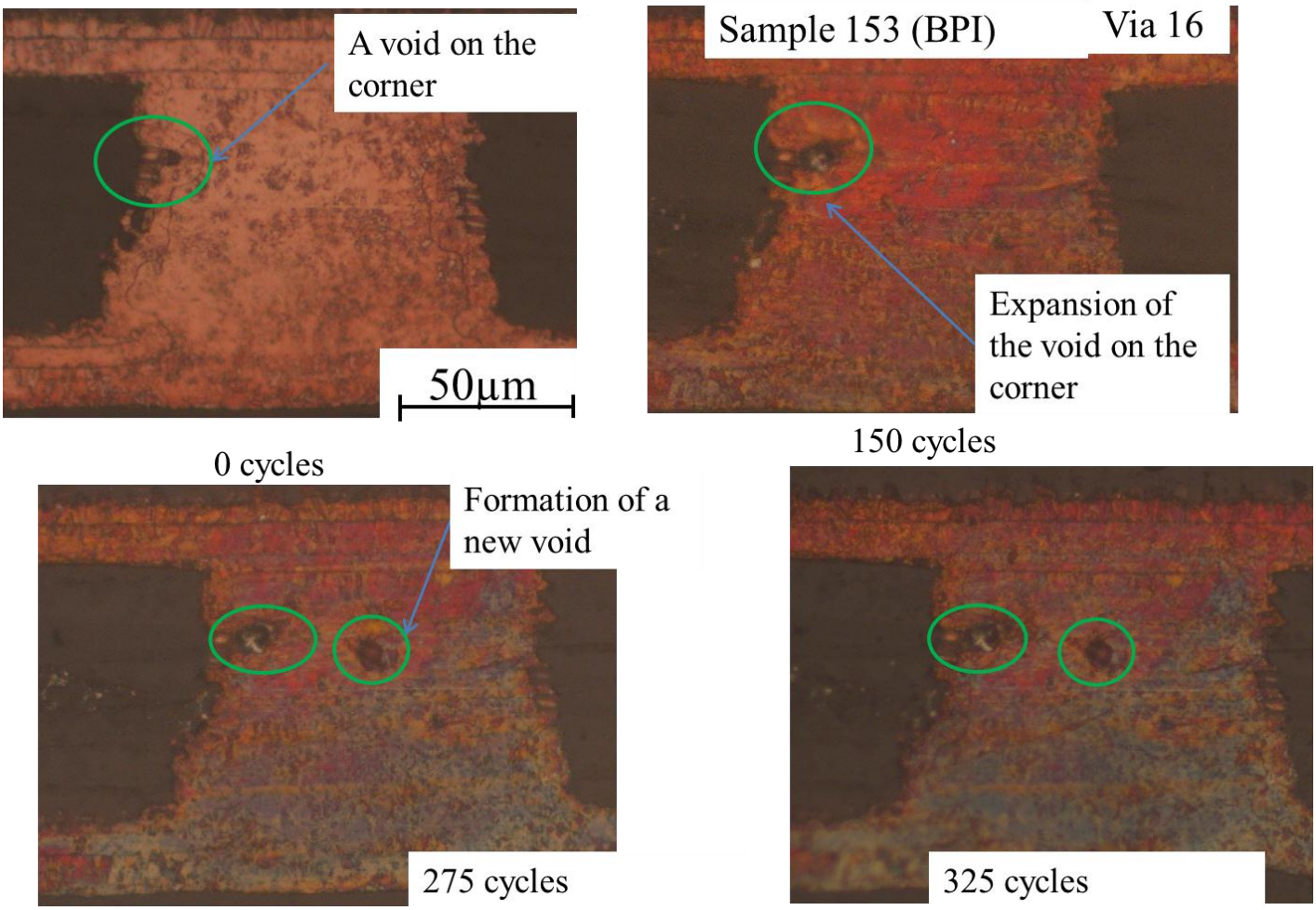

Figure 28- Formation of the new voids in the samples

Figure 28 shows the state of a single layer microvia at different stages of thermal shock testing. It can be seen that at 0 cycles there was a small void on the corner of the microvia. Further cycling shows that this void expands and gets even bigger; this phenomenon can be seen

after 150 cycles. In order to confirm this expansion of the void E-SEM analysis was performed on the samples. Figure 29 shows the E-SEM image of the new void.

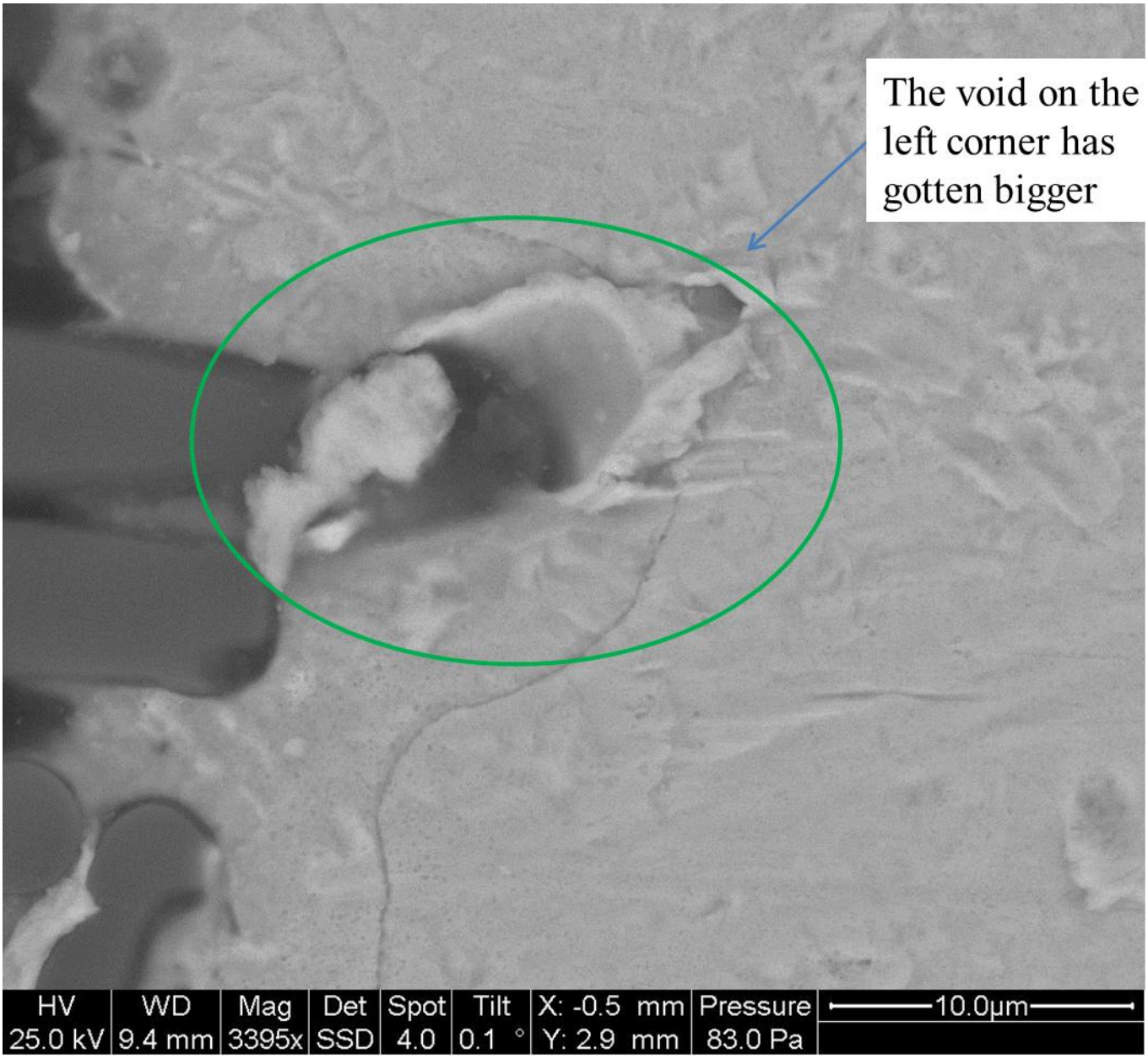

Figure 29- Void expansion after 150 cycle on the single layer microvia

As it can be seen on the E-SEM image, the right corner of the void is less shallow than the left corner which shows that the propagation direction of the void is towards right as it was expected since stress concentration is on the left corner.

The other phenomenon that was observed on this sample was the formation of a new void that wasn`t existed on the sample before prior to testing. Going back to figure 28 it can be seen that there is no void in the middle of the sample whereas after 275 cycles, a new void is detected. E-SEM analysis was performed to confirm the formation of the new void. The image can be seen on figure 30.

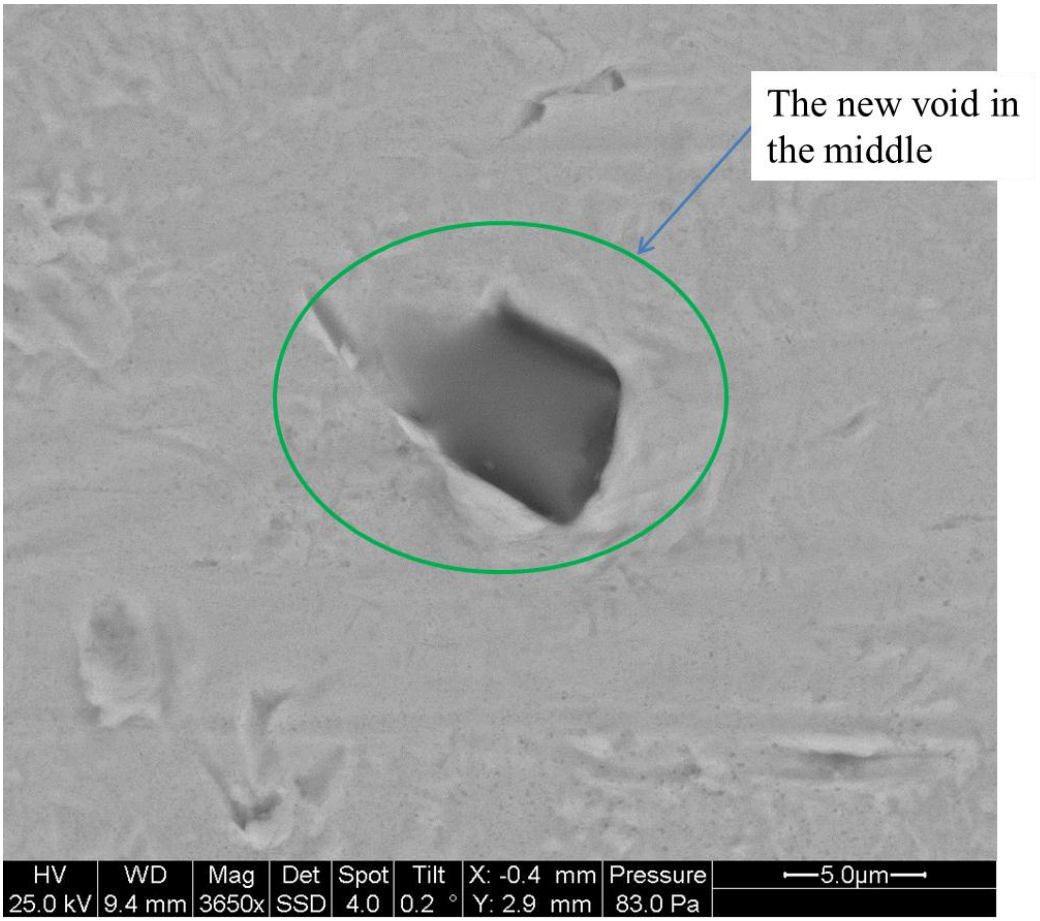

Figure 30- Formation of new void

This phenomenon (formation of a new void) has been observed in several samples. One of the possible reasons could be fracking of copper. The most possible scenario is these are pre-existing voids that were covered with a thin layer of copper. This thin layer of copper failed after a certain number of thermal-shock cycling due to intense tensile and compressive stresses. The hypothesis is these voids could be revealed with further grinding of the sample in the sample preparation procedure. This is not point that the voids are not symmetric and do not always happen at the middle of the microvia cause these microvas are ground and polished up to the half of the diameter and since these voids are not seen in the first half, it shows that they are small ones that happened in the second half of the microva.

6. DISCUSSION:

All the failures that were observed in these sets of experiments fall under one of these three categories as it was stated before:

1. Initiation of cracks
2. Expansion of voids
3. Formation of new voids

During the thermal shock from -55˚C to 125˚C the microvias experience extensive cyclic tensile and compressive stresses. These stresses and their corresponding strains are caused due to different reasons. One reason could be the effect of the geometry of the microvias and the voids. As it can be seen from the failed samples, the number of the failed samples was much bigger for the stacked microvias compared to single layer microvias. Also samples with larger voids failed earlier than the samples with smaller voids.

Table 3 and **Error! Reference source not found.** summarize the degradations observed fter 500 cycles.

Table 3- Summary of the observed degradations

Sample No.	Cycle Degradation Observed	Number of Levels	Voided
150	325	3	N
150	450	3	Y
150	325	3	Y
155	475	3	Y
156	450	2	Y
153	325	3	Y
153	275	3	Y
153	275	1	Y
204	325	3	N

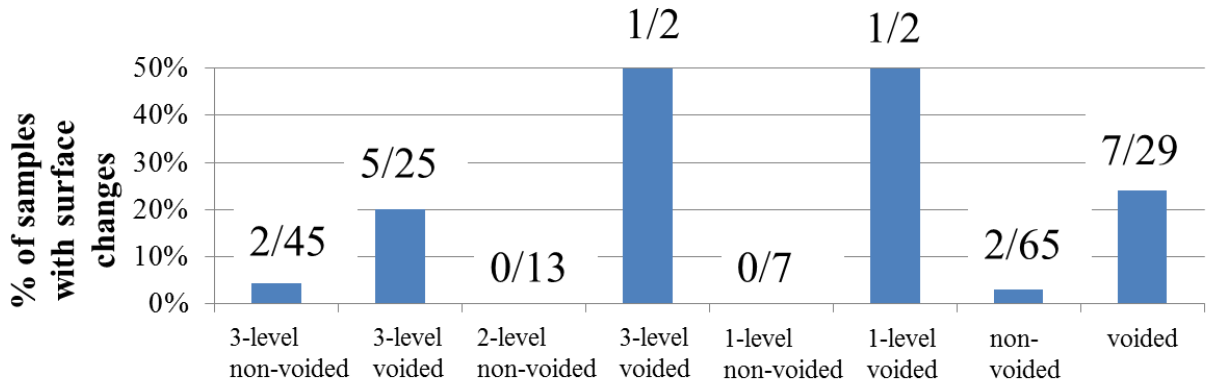

Figure 31-Percentage of the sample that showed signs of surface change based on different types of microvias (the numbers at top of each bar represents the number of microvias that showed the surface change divided by the total number of microvias

The second and more important reason of the failure of microvias is the effect of dielectric material. Coefficient of thermal expansion (CTE) of dielectric varies in different plans –in other word, it is orthotropic and not homogeneous- and these CTE of dielectric material is also different from the CTE of copper. Table 3 shows the CTE of different material that was used in the boards under the study.

Table 4- CTE information of the material used in the boards under investigation

Material	CTE (ppm)
Copper	17.3
FR4 (x-direction)	13.8
FR4 (y-direction)	16.8
FR4 (z-direction)	49.4

The total strain that the materials especially copper experience is an important parameter that affects the fatigue life of the microvia. The total strain consists of both elastic strain range and plastic strain range.

Due to effect of CTE mismatch especially in the z-direction, materials can experience plastic strains and therefore be prone to low cycle fatigue during the thermal shock cycling as it was seen in sample 153 microvia 5 that the crack started in the z-direction. The failure results from the thermo mechanical stresses caused by large differences in the CTE between the dielectric layers and the copper. The principal failure mechanisms are ductile fracture of the copper and low cycle fatigue as it was mentioned earlier caused by thermal shock.

Error! Reference source not found. shows the statistical analysis of the samples that howed degradation during the cycling.

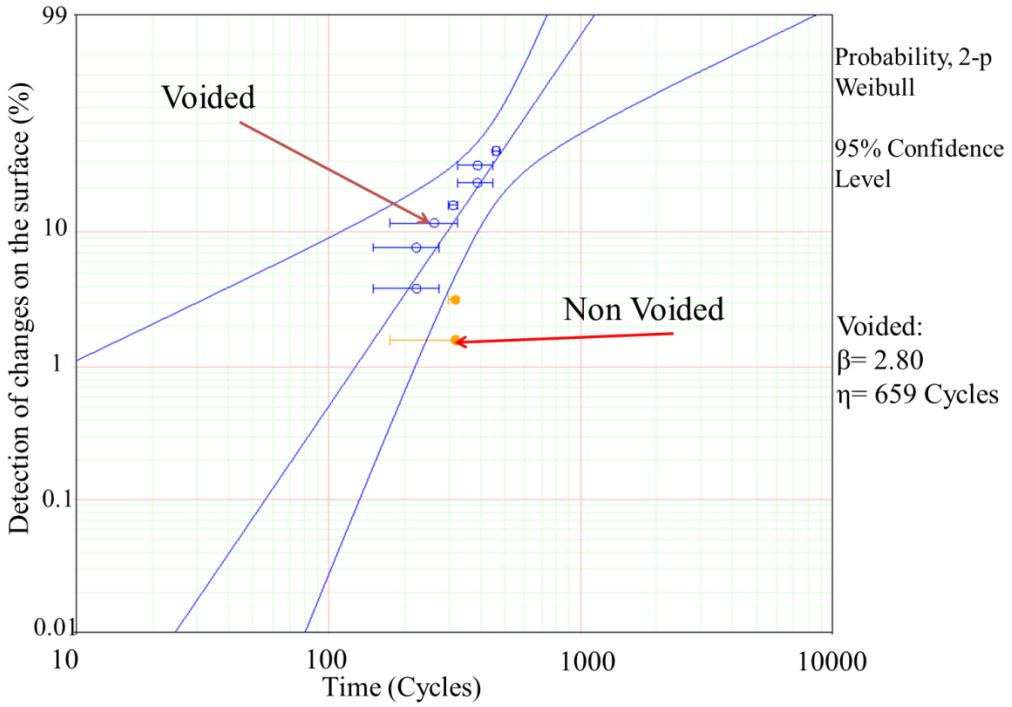

Figure 32- Weibull plot of the results

The following conclusions can be made from the statistical results:

1. Samples are experiencing only one failure mechanism, this failure mechanism is low cycle fatigue due to occurrence of plastic deformation on locations where there is a stress concentration
2. Beta value over one indicates that these are wear out effects and not infant mortality
3. Characteristic life indicates that 63.2% of microvias will show signs of surface degradation after 659 cycles.
4. Lack of enough data for non-voided samples makes it impossible to make a conclusive judgment about their reliability other than the fact that they have less susceptibility to cracking compared to the voided samples.

7. CONCLUSION

With the advancement of electronics technology and introduction of hand held devices the size of the packages keeps shrinking. The higher I/O pad density introduced the high density interconnect printed circuit boards which use microvias as the connection between layers. Single layers microvias has been studied vastly in the literature however stacked multi-layer microvias are a new concept.

Presence of voiding in the stacked microvias can reduce the reliability of the board. This study determined that void or voids in the stacked microvias are the source of crack initiation and further failure of microvias. The failure mode was observed were the maximum stress concentration happens which is the sharp corners of the voids. The failure mechanism is low cycle fatigue due to plastic deformation of the copper which comes from CTE mismatch between the copper and the surrounding dielectric material.

8. CONTRIBUTIONS

- Determined the susceptibility of the HDI boards with the presence of voiding in the stacked HDI layers compared to boards with completely filled microvias.
- Identifying the failure mode, mechanism and site of the voided microvias in stacked HDI layers.

9. REFERENCES

[1] "PCB Structures: Vias, Pads, Lands, Dimensions, Traces, and Planes," 03-Aug-2012. [Online]. Available: http://www.pcbdesign.org.

[2] K. Jonsson and B. Andersson, "HDI = High Density Interconnect." NCAB Group, IPC prestentation.

[3] IPC/JPCA-2315, "Design Guide for High Density Interconnects (HDI) and Microvias." Jun-2000.

[4] IPC-2226, "Sectional Design Standard for High Density Interconnect (HDI) Printed Boards." Apr-2003.

[5] L.-N. Ji, Y. Gong, and Z.-G. Yang, "Failure investigation on copper-plated blind vias in PCB," *Microelectronics Reliability*, vol. 50, no. 8, pp. 1163–1170, Aug. 2010.

[6] F. Liu, J. Lu, V. Sundaram, D. Sutter, G. White, D. F. Baldwin, and R. R. Tummala, "Reliability assessment of microvias in HDI printed circuit boards," *IEEE Transactions on Components and Packaging Technologies*, vol. 25, no. 2, pp. 254 –259, Jun. 2002.

[7] F. Liu, V. Sundaram, H. Chan, G. Krishnan, J. Shang, J. Dobrick, J. Neill, D. Baars, S. Kennedy, and R. Tummala, "Ultra-high density, thin core and low loss organic system-on-package (SOP) substrate technology for mobile applications," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 612 –617.

[8] G. Ramakrishna, F. Liu, and S. K. Sitaraman, "Experimental and numerical investigation of microvia reliability," in *The Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2002. ITHERM 2002*, 2002, pp. 932 – 939.

[9] B. Xiong, K. W. Loo, and K. Nagarajan, "Microvia reliability improvement for high density interconnect substrate," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 138 –141.

[10] F. Su, R. Mao, J. Xiong, K. Zhou, Z. Zhang, J. Shao, and C. Xie, "On thermo-mechanical reliability of plated-through-hole (PTH)," *Microelectronics Reliability*, vol. 52, no. 6, pp. 1189–1196, Jun. 2012.

[11] J. Xie, R. Kang, Y. Zhang, and G. Guo, "A PTH Reliability Model Considering Barrel Stress Distributions and Multiple PTHs in a PWB," in *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International*, 2006, pp. 256 –265.

[12] S. M. Bhandarkar, A. Dasgupta, D. Barker, M. Pecht, and W. Engelmaier, "Influence of Selected Design Variables on Thermo-Mechanical Stress Distributions in Plated-Through-Hole Structures," *Journal of Electronic Packaging*, vol. 114, no. 1, p. 8, 1992.

[13] IPC/JPCA-4104, "Qualification and Performance Specification for Dielectric Materials for High-density Interconnect Structures (HDI)." .

[14] IPC-6016, "Qualification and Performance Specification for High-density Interconnect (HDI) Structures." May-1999.

[15] IPC-6012D, "Qualification and Performance Specification for Rigid Printed Boards." .

[16] IPC-TM-650-2.1.1, "Microsectioning, Manual Method." Mar-1998.

[17] IPC-TM-650, "Thermal Shock - Conformal Coating." Jul-2000.

[18] R. Iannuzzelli, "Predicting plated-through-hole reliability in high temperature manufacturing processes," in *Electronic Components and Technology Conference, 1991. Proceedings., 41st*, 1991, pp. 410 –421.

[19] S. Mahalingam, S. Hegde, J. Ahmad, R. V. Pucha, V. Sundaram, F. Liu, G. White, R. Tummala, and S. K. Sitaraman, "Materials, processes and reliability of mixed-signal substrates for SOP technology," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, vol. 2, pp. 1630 – 1635 Vol.2.