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Learning-based Grid Impedance Shaping Method Applied for High-Accuracy Power Hardware-in-the-Loop

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***Abstract*-- Future power and energy systems integrate cutting-edge technologies such as power converter-interfaced distributed generation and energy storage systems and responsive loads organized as microgrid clusters. The performance evaluation of these complex systems requires flexible testbeds to provide relevant information under different operational scenarios. Thus, this paper proposes a Power Hardware-in-the-Loop (PHIL)'s power interface algorithm that uses a digital twin system (DTS) implemented through a learning-based virtual impedance control approach to provide high-accuracy experiments and enhance system stability. Experimental results obtained from a PHIL laboratory setup demonstrated the effectiveness of the proposed method.**

***Index Terms*-- Power hardware-in-the-loop, virtual impedance, artificial intelligence, grid impedance estimation, brain emotional learning.**

I. Introduction

Renewable Energy Sources (RESs) have been steadily developing worldwide to address the energy shortage and the low-carbon motivations. However, the RESs such as the photovoltaic and wind generations largely depend on environmental conditions and exhibit intermittent and uncertain behavior. RESs are interconnected to the power grid through power converters operating as current- or voltage- controlled sources. These active front-end systems could modify the grid dynamics, addressing undesired stability issues. These effects are generally correlated to the impedance interaction among the grid and multiple grid-connected power converters [1]. The insertion of Grid-Forming Converters (GFCs) could overcome these drawbacks and enhance grid stability [2]. However, the insertion of GFCs into the network should be previously tested to forecast their operational constraints and the local and global stability. For secure reasons, it is impossible to perform tests and analyses directly in the power grid, particularly in complicated grids with many stakeholders and a heightened degree of distributed generation. Hence, the challenges for widespread power system integration with RESs require advanced analysis and simulation methods to evaluate their effectiveness and stability [3], [4].

Hardware-in-the-Loop (HIL) system is usually used to test specific networks connected with various applications in the industry. It employs a controller board to perform a real-time network simulation, interconnected to the hardware under test through control and measurement signals. This setup provides enough information for evaluating embedded control boards or parts of equipment without power exchange. On the contrary, Power Hardware-in-the-Loop (PHIL) systems have been demonstrated to be attractive for testing RESs and their integration with the power system, with reduced cost and associated risk compared with their realization on large and complex power systems' testbeds [5], [6]. The use of PHIL as a power testbed avoids losses due to the possible design choices or specifications changing. Moreover, it produces precise and realistic testing conditions before installation, mitigating possible integration mismatches [4]. Differently of the HIL, PHIL deals with real power exchange between the Digital Real Time Simulator (DRTS) and Equipment under Test (EUT) by using a Power Amplifier (PA) normally implemented by a power converter as shown in Fig. 1. PHIL testing procedures have been used in several applications, such as electric ships [3], [5], nonlinear power electronics-based equipment [6], [7], renewable energy systems [8], [9], and energy storage systems [10]. However, although PHIL's testing and verification provide significant benefits, some drawbacks still arise due to its hybrid nature, resulting in accuracy and stability issues. For example, the required signal interchange, provided by an interface algorithm, results in closed-loop paths, inserting significant impacts on the PHIL's experiment stability [11]. In this context, nonideal characteristics such as time delay and bandwidth inherent to power amplifiers (PA), signal acquisition interfaces, output, and aliasing filters should also be considered [12], [13] in the design approach. In most applications, the representation of voltage and current variables in the DRTS or PA employs controlled voltage or current sources based on average models that neglect possible switching frequency effects. It reduces the computational burden but generates experimental results far from the real operation conditions. Further, the required stability and accuracy

occur when a virtual impedance is inserted into the simulated model with the same value as the physical system's internal impedance [3]. Thus, estimating EuT equivalent impedance can improve the PHIL experimental system stability. In this sense, this paper proposes a PHIL power interface algorithm (PIA) based on a twin digital system implemented through a learning-based Virtual Impedance (VI) control approach to overcome the drawbacks mentioned earlier. The proposed learning method continuously adjusts virtual impedance during the experiment based on impedance measurements of the EUT. The experimental results obtained from a PHIL laboratory setup demonstrate the effectiveness of the proposed method.

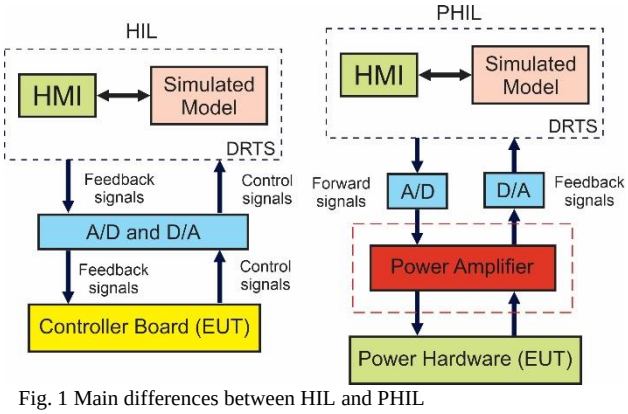

Fig. 1 Main differences between HIL and PHIL

II. Configuration of the Proposed PHIL Setup

Fig. 1 shows the block diagram of the PIA used in the proposed PHIL. It is based on a hybrid twin system that interconnects the DRTS simulated model and EuT by interchanging the point of connection (PoC) voltages (u_g) and EuT output voltages and currents (u_e and i_e). The PHIL experimental setup includes the following main components: (1) DRTS - OPAL-RT - OP5600; (2) Power Grid Emulator and PA - CINERGIA; (3) EuT - Semikron Two-Level Voltage Source Inverter (VSI), DC Power Supply, Drive Unit, LC Filter, and LEM Sensors; (4) Control Fast Prototype System - dSPACE Microlab 1202; (5) AC/DC Controlled Load - CINERGIA. This setup is realized based on RT-LAB environment of Opal-RT and dSPACE control desk environment in MATLAB/Simulink. A windows-based host computer interconnects both OP5600 and DS1202 through TCP/IP protocol. OP5600's fast analog-digital (i.e., ADC or DAC converters) or digital output-input interfaces (i.e., I/O) interface OP5600 and DS1202. In the DS1202, the interconnection with the power converter or OP5600 employs I/O ports and BNC connectors. In contrast, DB-37 rear connectors access the I/O ports and AD/DA converters. For that reason, a dedicated PCB was manufactured to interconnect those connectors to BNC's cables, as presented in Fig. 2. This adaptation permits that BNC cables interconnect OP5600 with the DS1202 or power grid emulator (i.e., CINERGIA). In this setup, the real-time simulations are executed synchronously in both systems (i.e., OP5600 and DS1202-CINERGIA), demanding bidirectional communications of measurements and commands. The control algorithms executed in both systems (i.e., OP5600 and DS1202) employ a sampling rate of 20μs. The interconnection between the OP5600 and DS1202 follows the concept of twin systems for permitting the simultaneous dynamic evaluation of both systems with the same power conditions.

A grid-connected voltage source converter, operating as a GFC, implements both EuT and DRTS. The EuT is interconnected to the PA through the line impedance (z_s). The implementation of the GFC incorporates a VSI connected to the PCC via an LC filter, regulated by a PI controller and a voltage regulator, according to Fig. 1. The details about the modeling and control strategies employed in the proposed GFC is addressed in next section. In addition, PIA employs a learning-based impedance shaping approach for assuring system stability. The proposed impedance shaping approach comprises an equivalent grid impedance estimator block, a VI profile definition block, adaptive VI system block and an intelligent method based on brain emotional learning (BEL), as shown in Fig. 2. In this scheme, the PIA is based on an ideal transformer model, in which the controlled voltage sources u'_e and u'_g represent the interaction between EuT and PoC. The controlled current source refers to the EuT output current used for emulating the virtual impedance. In Fig. 2, $z_e = r_e + jx_e$ is the estimated equivalent impedance; r_v and x_v are VI components. x_{v2} is implemented through the BEL approach and added to x_{v1} to reach the X/R control objectives.

III. Modeling and Control

The voltage control loop uses a nested-loop control approach using conventional controllers in which the inner loop controls the filter current, and the outer loop controls the output voltage of the GFC [14]. Considering the GFC shown in Fig. 2 in the DRTS part, the power exchange between the VSI and grid can be written as follows:

$$P_{e,DRTS} = \frac{u_g u_S}{z_s}\cos(\varphi - \theta) - \frac{{u_S}^2}{z_s}\cos(\varphi) \quad (1)$$

$$Q_{e,DRTS} = \frac{u_g u_S}{z_s}\sin(\varphi - \theta) - \frac{{u_S}^2}{z_s}\sin(\varphi) \quad (2)$$

where V_g and V_S represent the root-mean-square (RMS) of voltages of the VSI, and the grid, respectively; θ is power angle; and $z_s < \varphi$ is line impedance. When the line impedance represents an inductive profile with a slight value of θ, (1) and (2) can be given as:

$$P_{e,DRTS} = \frac{u_g u_S}{X_s}\theta \quad (3)$$

$$Q_{e,DRTS} = \frac{u_g}{X_s}(u_g - u_s) \quad (4)$$

where $X_s = \omega l_s$ is the reactance of the line impedance.

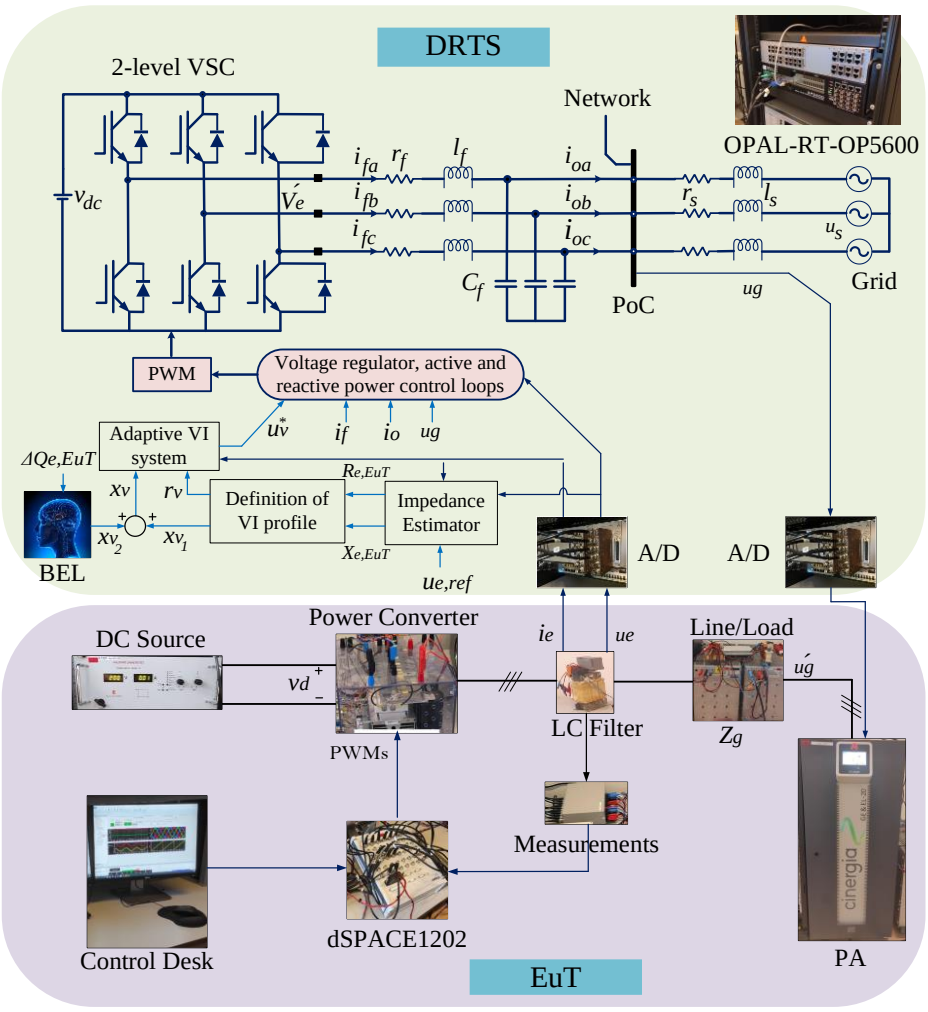

Fig. 2 Configuration of the proposed PHIL setup

Proportional-integral (PI) controllers are commonly used to regulate signals with constant reference for reaching zero steady-state errors and could also be used in active and reactive power control loops. Traditionally, the gains of PI controllers are tuned for providing a control action with a fast and damp response. However, a modified controller tuning method should be employed to achieve the required inertia feature [15]. The control diagram of the active power loop is shown in Fig. 3. When the transfer function of a PI controller used, the active power regulating transfer function becomes

$$\frac{P_{e,DRTS}}{P_{ref}} = \frac{2\xi\omega_n+{\omega_n}^2}{s^2+2\xi\omega_n+{\omega_n}^2} \tag{5}$$

in which

$$\xi = \frac{\frac{u_g u_s}{X_s}k_p}{2\omega_n} \tag{6}$$

$$\omega_n = \sqrt{\frac{u_g u_s}{X_s}k_i} \tag{7}$$

where k_p and k_i are the controller gains of the PI employed in the active power control loop. This controller is named the Energy-PI controller [15] since it uses the concept of power synchronizing, which distinguishes it from the objectives of a standard PI regulator. The reactive power control loop also employs a PI controller to suitably regulate the GFC's voltage.

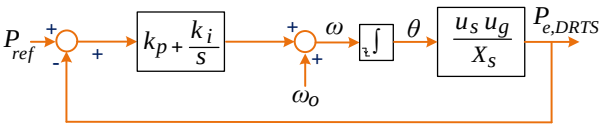

Fig. 3 Control block diagram of the active power control loop

IV. Learning-Based Impedance Shaping Approach

As mentioned earlier, the proposed impedance shaping approach includes an equivalent grid impedance estimator block, a VI profile definition block, BEL-based VI system block. The output current and voltage of the EuT is used for emulating the VI in the DRTS. The following section describes their functionalities and how their integration adaptably shapes the equivalent grid impedance in the DRTS.

A. Equivalent Grid Impedance Estimation

In order to estimate the equivalent impedance with a virtual impedance, the following procedure can be used [14]:

Initially, active and reactive powers related to the equivalent impedance can be calculated as:

$$P_s = \delta v_{s\alpha} i_{e\alpha} + \delta v_{s\beta} i_{e\beta} \quad (8)$$

$$Q_s = \delta v_{s\alpha} i_{e\beta} - \delta v_{s\beta} i_{e\alpha} \quad (9)$$

where $\delta v_{s\alpha\beta} = u_{e\alpha\beta,ref} - u_{e\alpha\beta}$ is the voltage difference between the reference and output voltages of the EuT; and $i_{e\alpha}$ is the current measurements at the PCC in the EuT part. Given that the system is balanced and symmetric, the module of the equivalent impedance could be estimated as follows:

$$Z_{e,EuT} = \frac{u_{e\alpha,ref}(rms)}{I_{e\alpha}(rms)} = \frac{u_{e\beta,ref}(rms)}{I_{e\beta}(rms)} \quad (10)$$

The resistance and reactance components of Z_e denote its real and imaginary parts, which can be given as:

$$R_{e,EuT} = \frac{Z_e P_s}{S_a} \quad (11)$$

$$X_{e,EuT} = \frac{Z_e Q_s}{S_a} \quad (12)$$

where $S_a = \sqrt{{P_s}^2 + {Q_s}^2}$ is the apparent power corresponding to the equivalent impedance. The proposed procedure reasonably estimates the resistive and reactive parts of the EuT's equivalent impedance. Then, it is used to find the suitable VI in the DRTS needed for achieving accuracy for PHIL experiments.

B. Definition of VI profile

The VI profile definition block represents the VI profile to achieve the same X/R ratio in the EuT based on its impedance estimation and availability of inverter power. The VI implementation uses an RL branch comprising virtual resistance and inductance. The error metric of (13) can then be calculated directly from the estimated impedance of the EuT ($Z_{e,EuT} = R_{e,EuT} + jX_{e,EuT}$) and the estimated impedance of the DRTS ($Z_{g,DRTS} = R_{g,DRTS} + jX_{g,DRTS}$). It should be noted that the procedure defined in section IV.A with u_e and i_e replaced by u_g and i_o (voltage and current measurements at the PCC in the DRTS part) can be employed to estimate the equivalent grid impedance in DRTS.

$$Z_{dif} = ||Z_{e,EuT}| - |Z_{g,DRTS}|| \quad (13)$$

Given the calculated metric, the value of virtual resistance and reactance (r_v and x_v) is calculated by

$$r_v = \mu \times Z_{dif} \quad (14)$$

$$x_v = \gamma \times Z_{dif} \quad (15)$$

where μ and γ are the reduction factors and determined based on the inverter stability limits and minimum error metric. The value of x_v is shared into two parts determined using a distribution factor λ, which results in $x_{v2} = \lambda x_v$ and $x_{v1} = (1-\lambda)x_v$. The virtual reactance x_v uses a variable structure scheme, in which, x_{v1} follows the standard implementation and x_{v2} uses a BEL-based approach for compensating unmodeled disturbances and considering possible grid impedance variations and estimation inaccuracies of the EuT.

C. BEL-based virtual impedance control approach

Motivated by the limbic system in the human brain, computer-based models can be designed to simulate various characteristics of the emotional system. This method is constituted of Amygdala, which is in charge of emotional learning; Orbitofrontal cortex, sensory cortex, and Thalamus [16], [17]. The model is provided with two inputs including sensory input (SI) and emotional signal (ES). Preprocessing on SI signal such as filtering or noise reduction is performed by the Thalamus. The sensory cortex receives the Thalamus output and then submits it to the Amygdala and Orbitofrontal cortex. A simplified layout of the BEL method employed in this study is shown in Fig. 4. The details about this approach can be found in [17]. To achieve the promising execution of the BEL method, making a relation between SI, ES, and output (x_{v2}) is critical. The SI and ES inputs for the BEL to produce x_{v2} are written as follows.

$$SI = \tau_1(Q_{ref} - Q_{e,EuT}) + \tau_2 \int (Q_{ref} - Q_{e,EuT})\, dt$$

$$ES = \tau_3(Q_{ref} - Q_{e,EuT}) + \tau_4 \int (Q_{ref} - Q_{e,EuT})\, dt + \mu_5 x_{v2} \quad (16)$$

where the weighting factors τ_1, τ_2, τ_3, and τ_4 are calculated via a trial-and-error procedure. The functions *S* and *ES* are chosen as the outputs of a PI block in response to reactive power error ($Q_{ref} - Q_{e,EuT}$) in EuT part.

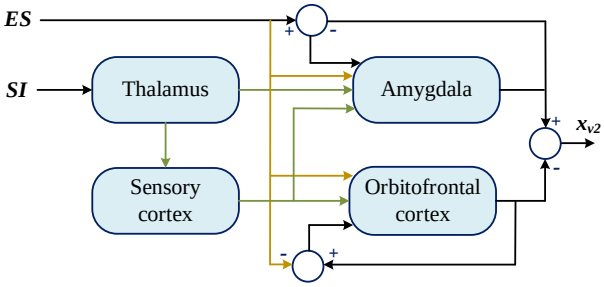

Fig. 4 A simplified structure of BEL method

V. Experimental Results

Experimental results obtained from a PHIL laboratory setup composed of DRTS, OP5600, and an EuT implemented by a GGC, controlled by a dSPACE, DS1202, have been carried out to validate the proposed method. The parameters of the system are given in Table 1. In the beginning, the DRTS sends the reference to the PA in an open-loop condition.

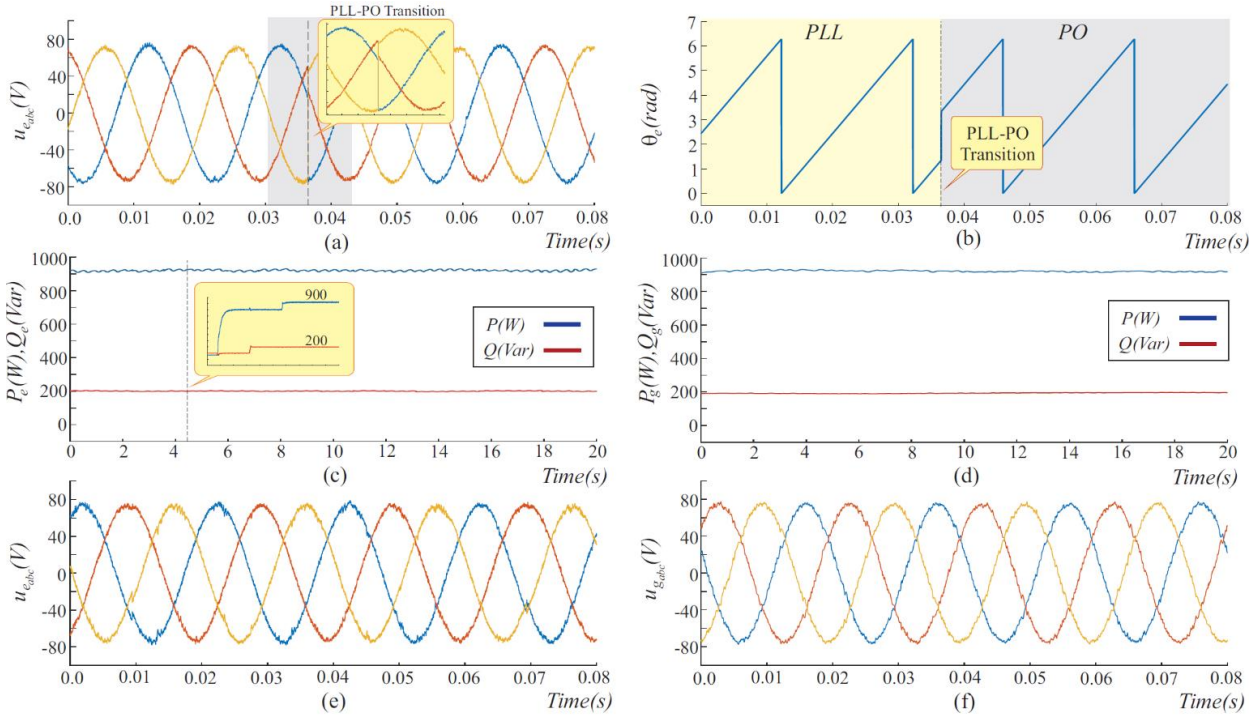

Fig. 5 PHIL experimental results; (a) EuT voltage waveforms during the startup procedure, (b) EuT voltage vector angle during the startup scheme, (c) EuT steady-state active and reactive powers, (d) DRTR simulated-model, steady-state, active and reactive powers, (e) EuT steady-state voltage waveforms, and (f) DRTS voltage waveforms.

Table 1 Parameters of the setup

Description	Value
Grid voltage (RMS)	70
Grid's nominal angular speed	100 πrad/s
Nominal frequency	100 πrad/s
Line impedance	3.6 mH and 0.2πΩ
LC-filter	2.4 mH and 15 μF
Inverter rating	1 kW
Voltage magnitude reference (RMS)	70
DC-side voltage	200
Switching frequency	20 kHz
Sampling time	20 μs

Then, the EuT synchronizes to the PA by using a synchronous- reference-frame phase-locked-loop (SRF-PLL). Thus, a transition scheme is employed to substitute the PLL to the power oscillator (PO) scheme to generate the suitable voltage vector, providing the required EuT power delivery. Figs 5(a) and 5(b) present the EuT voltage waveforms and voltage vector angle during this procedure. Also, the controlled active and reactive powers values follow the imposed voltage vector angle determined by the PLL (i.e., 80 W and 100 VAr). After that, positive and negative power steps are inserted in both EuT active and reactive reference power values for reaching the steady-state condition with P_e = 900 W and Q_e = 200 VAr, as shown in Fig. 5(c). The PIA reproduces the same power conditions at DRTS, as depicted in Fig. 5(d). Finally, Figs. 5(e) and 5(f) present the three-phase voltage waveforms in the steady-state condition for both EuT and DRTS systems. The results demonstrate the accuracy and coherence of the experimental results obtained from the EuT and DRTS simulation.

VI. Conclusion

This paper has proposed a PHIL power interface algorithm based on a digital twin system, implemented through a learning-based virtual impedance control approach. The suitable impedance value is determined by estimating the EuT equivalent impedance. The proposed PIA uses a power converter model with the same EuT control approach in the DRTS simulation, in which a virtual scheme is employed for inserting the system's required impedance, thereby assuring the required stability. Experimental results obtained from the PHIL laboratory setup validate the proposed solution and demonstrate its effectiveness. The main features of the proposed PHIL testbed are: 1) Flexible DRTS for covering device-level studies (e.g., power converters) to system-level evaluations (e.g., full-scale energy systems); 2) Co-simulation of multiple power/energy networks through web interconnection; 3) Emulation of several operation scenarios such as faults, asymmetries, harmonic conditions, and frequency variation; 4) Interface EUT – DRTS implemented using digital twin systems; 5) Interconnection of different load types and energy storage

systems (ESS) with different technologies and dynamic behaviors.

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