ABSTRACT

Title of Dissertation: INVESTIGATION OF RELIABILITY IN GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS USING EQUIVALENT CIRCUIT MODELS FOR USE IN HIGH POWER, HIGH FREQUENCY MICROWAVE AMPLIFIERS

Benjamin D. Huebschman, Doctor of Philosophy, 2010

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Gallium Nitride (GaN) is beginning to emerge as an alternative to the Gallium Arsenide in high power, high frequency microwave communications. Other novel semiconductors show potential at higher frequency applications. The largest obstacles to GaN emerging as the dominant microwave semiconductor are the issue of cost, which could be reduced through volume, and question of reliability.

A new approach to the analysis of reliability has been developed based on the periodic generation of equivalent circuit models while a device is stressed in a manner that is similar to performance likely to be seen during commercial operation. Care was made in this research to ensure that the stress measurements used to induce degradation are as close as possible to those that would degrade a device in real world applications.

Equivalent circuit models (ECM) can be used to simulate a device in computer aided design (CAD) software, but these models also provide a picture of the physical

properties within the device at a specific point in time. The periodic generation of ECMs allows the researcher to understand the physical changes in the device over time by performing non-destructive electronic measurements. By analyzing the changes in device performance, the physical mechanism of device degradation can be determined. A system was developed to induce degradation and perform measurements of sufficient detail to produce a large signal ECM. Software for producing the ECM was also created. The changes in the ECM were analyzed to diagnose the physical changes in the device under test (DUT) and to identify a method of degradation. The information acquired from this system can be used to improve the device manufacturing process at the foundry. It can also be used to incorporate device degradation into the operation of systems.

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By

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Dedication

To my patient family and friends

Acknowledgements

I am grateful to the many people who provided guidance, assistance, mentoring, and support during my long journey in scholarship at the University of Maryland. First and foremost, I would like to thank my advisors, Professor Wes Lawson who welcomed me to the University of Maryland and allowed me to work on his projected and later Professor Neil Goldsman who guided me during my research that would later prove to be my PhD dissertation. I would like to thank the numerous members of the faculty for their excellent instruction.

I would like to thank all my friends and colleagues at the Army Research Laboratory. I am grateful to my friend Dan Judy for his patient instruction. Ed Viveiros and Dr. Romeo Del Rosario provided me with the time and space to perform my research. I am grateful Dr. Ken Jones for sharing his knowledge of semiconductor physics and to Dr. Pankaj Shah for sharing his experience in academic research. Dr. Ali Darwish provided me with sound counsel on research of interest to the academic community, how to communicate that research, and the best procedures for conducting that research. This work would not have been possible without the vision, dedication, and support of the scientists and engineers at the Defense Advanced Research Projects Agency.

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Chapter 1: Introduction

1.1 Motivation

The development of semiconductor-based technologies has revolutionized virtually every aspect of modern life. Silicon (Si) is by far the dominant semiconductor with its ubiquitous applications in digital logic, signal processing, optical communications, among many others. Other semiconductors, like gallium arsenide (GaAs), a leading semiconductor used for power RF communications, and gallium nitride (GaN), the semiconductor used in white light emitting diodes (LEDs), have application-specific markets. GaN has also begun to emerge as an increasingly viable source for high power and high frequency microwave amplifiers. Commercially available GaN amplifiers are already beginning to find a niche market in moderate power, high frequency microwave systems [1].

Many novel semiconductors have interesting material properties that could improve the performance of semiconductor devices. Unfortunately, a great deal of investment is required for these novel semiconductor devices to reach a level of maturity that would allow them to realize their full commercial potential. The goal of the research described in this dissertation is to increase the rate of development of novel semiconductor devices through two complimentary techniques. The first technique would provide a reliability diagnostic tool for determining the physical mechanism by which a device's performance degrades during operation under stressful conditions. The second method makes use of the knowledge gained from the first method. Once the changes in a

device as its performance degrades are understood, a matching network can be created that is optimized for the device's characteristics at a later stage. The goal of the second part of the project is to allow designers to understand the tradeoff between reliability and performance. An accurate understanding of how limited reliability can be mitigated in the design process may allow promising materials and technologies to find commercial applications during the maturation process of the technology, when reliability concerns are still an issue. Using such information to realize commercial applications of a material early in the development process should act as an incentive for industrial research, resulting in positive feedback between research and commercial utilization.

Figure 1.1 shows a graph of reported breakdown voltages plotted against the threshold frequencies for commercially viable semiconductor devices and materials. From a performance perspective, frequency can be thought of as the metric that determines the maximum data rate for a communication system or the level of resolution in a radar system, and breakdown voltage can be thought of as an indicator of the maximum range. Breakdown voltage is also highly correlated with efficiency.

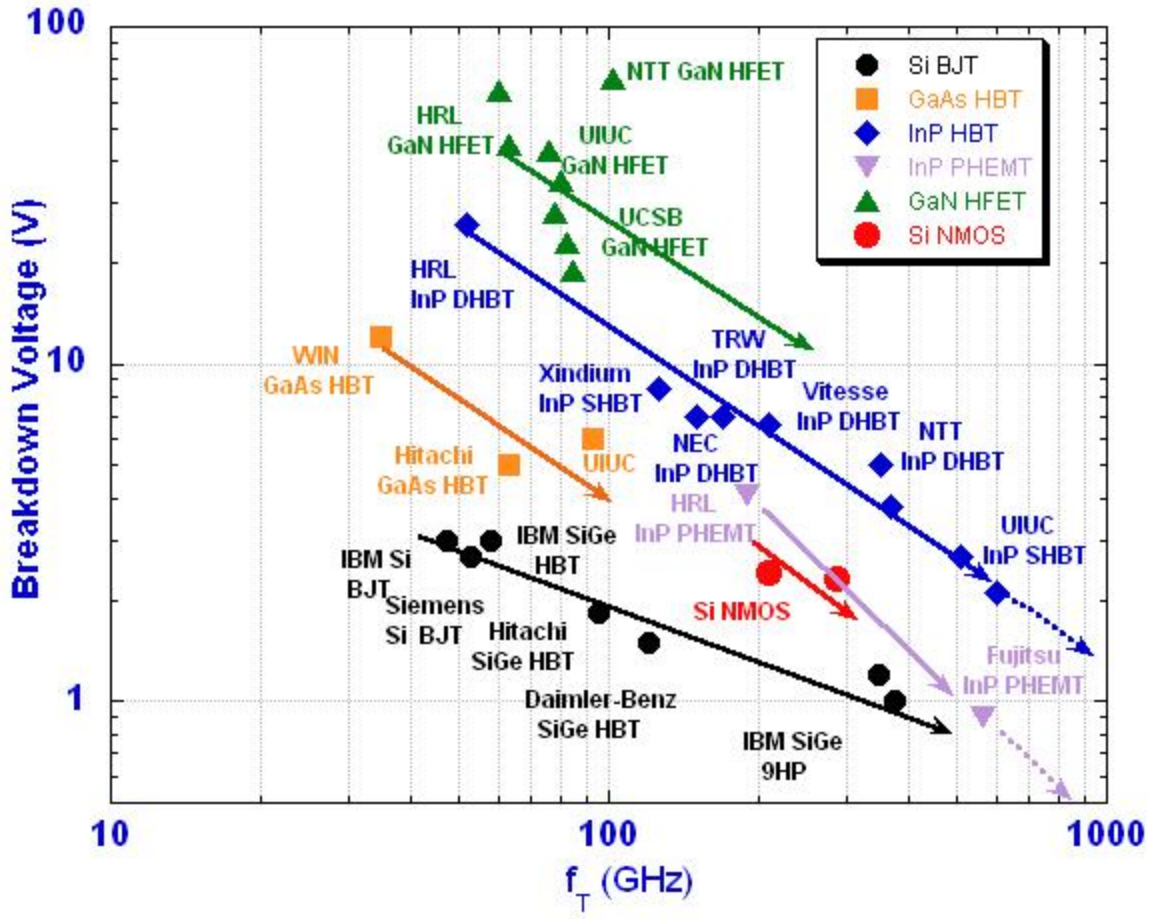


Figure 1.1. Threshold frequency vs. breakdown voltage for possible RF semiconductor materials and devices [2].

This research centers on device reliability and the analysis of degradation of device performance. In order to degrade a well-made device, it must be stressed. Devices are stressed by operating them under conditions of high power, at high temperatures, while exposed to strong electric fields, or some combination of all of these. As can be seen in figure 1.1, GaN heterostructure field-effect transistors (HFETs) have the highest breakdown voltage of the semiconductors surveyed in the figure. This is due to the material's large bandgap, a characteristic of that semiconductor that allows it to operate at the high power and high temperatures that are conducive to reliability tests. For this reason, the devices used in this research are GaN high electron mobility field effect transistors (HEMTs), which is another name for HFETs. GaN has a number of properties

that makes it a promising candidate for high-power, high frequency, and low noise applications. These qualities will be discussed in greater detail in chapter 2.

1.2 History of HEMT

The HEMT was first conceived by Takashi Mimura in 1979, when he saw an opportunity in using a field effect to control the two-dimensional electron gas (2DEG) that forms at the heterojunction interface in a semiconductor superlattice structure [3]. At that time, GaAs was being investigated by Fujitsu Laboratories for applications in metal-oxide semiconductor field-effect transistors (MOSFETs) due to its high electron mobility. The GaAs MOSFET proved difficult to develop due to the high density of surface traps that prevented accumulation [3]. The modulation doped heterojunction being investigated at Bell Laboratories proved to be an excellent structure for producing 2DEG. It was later found that 2DEG current channel could be modulated by using a gate structure similar to other field-effect devices [4]. The first report on a functional depletion mode HEMT was published in 1980. It detailed a depletion mode device fabricated on a semiconductor stack of aluminum gallium arsenide (AlGaAs) on GaAs. HEMT integrated circuits were developed shortly thereafter in 1981 [5]. Over the succeeding decades, GaAs HEMTs have proved very useful in low noise and high-power applications in communication electronics. In 1991, Khan *et al.* fabricated an AlGaN/GaN heterostructure that demonstrated the superior electron mobility of the material [6]. Original uses for AlGaN/GaN focused on optical applications due to its large bandgap and the fact that it is a direct bandgap material. The high electron mobility of the electrons within the 2DEG of GaN also suggested its utility in field-effect devices such as HEMTs. The same group who developed the AlGaN/GaN heterostructure

manufactured the first GaN HEMT in 1994.

The HEMT has been referred to by a number of names in the literature, such as modulation doped field effect transistor (MODFET), two-dimensional gas field effect transistor (TEGFET or 2DEGFET), and HFET. All these names provide some insight to the operation of the device. Modulation doping produces a heterojunction that forms a two dimensional electron gas in a low doped or undoped region of the semiconductor that, in turn, leads to the high mobility of electrons confined in the two dimensional electron gas (2DEG). While all these names had some merit, HEMT has emerged as the preferred moniker of the device in question and is the name that will be used for the remainder of the dissertation.

1.3 Overview

In this study, the performance of GaN HEMTs was monitored while the devices were under stress at high power at a range of temperatures. A number of measurements were performed periodically while the device was being stressed including measurements sufficient to produce a small signal model and a large signal model. These data were used to diagnose the internal electrical effects on the device. Using this information, a delayed optimal match was determined and applied to a device, which was then operated under stress conditions with the goal of mitigating device degradation by using the carefully selected match. This dissertation is organized into ten chapters. The first chapter describes the scope of the endeavor. The second chapter reviews the operation and device physics of GaN HEMTs. Chapter 3 outlines the layout of the experimental apparatus. The operation of this system and measurements used in model extraction are explained in

Chapter 4. The small signal model extraction procedures are explained in Chapter 5. In Chapter 6, the large signal model and the parameter extraction techniques are explained. The effects of elevated temperature on device performance are discussed in Chapter 7. Chapter 8 contains a survey of reported degradation mechanisms and techniques used to determine reliability. Chapter 9 details the results of the extended lifetime experiment. Chapter 10 provides the conclusion and presents options for future work.

Chapter 2: Device Physics of GaN HEMTs

2.1 Review of the Principles of a Band Diagram

Before discussing the material properties of AlGaN and GaN, the information represented in a semiconductor band diagram will be briefly reviewed. For most band diagrams of devices, the horizontal axis represents a specific spatial dimension. Conceptually, the vertical axis can have several interpretations; however, since the diagram is supposed to represent energy bands, for the purposes of this dissertation, the vertical axis represents energy. More precisely, the positive vertical axis represents increasing energy for electrons and the negative vertical axis represents decreasing energy for electrons. For holes, this is reversed: the positive vertical axis represents decreasing energy for holes and the negative vertical axis represents increasing energy for holes. Voltage is the state function of potential energy from electrical fields on electrical charges; therefore, for the horizontal lines in the band diagram, changes in the vertical axis are changes in voltage. There are three lines that run roughly parallel to the horizontal axis. The bottom line is the upper limit of the valence band. The top line is the lower limit of the valance band. The middle line is the Fermi level. The vertical separation between the valence band and the conduction band is the bandgap and represents both a region in which there are no allowed states in the bulk crystal and the amount of energy, or voltage, for a charged particle that is required to make the transition from one band to the other. A change in the conduction and valence bands with respect to the location on the horizontal axis indicates a change in voltage. According to Poisson's equation with regard to electrical fields (2.1), a change in voltage, by definition, is caused by an electric field:

where is E is the electric field and φ_E is the electric potential. In other words, the potential energy that comes from a position in an electric field is called voltage. From (2.1), it follows that a change in the conduction and valence bands is caused by an electric field and the slope of the valence and conduction bands is proportional to the electric field.

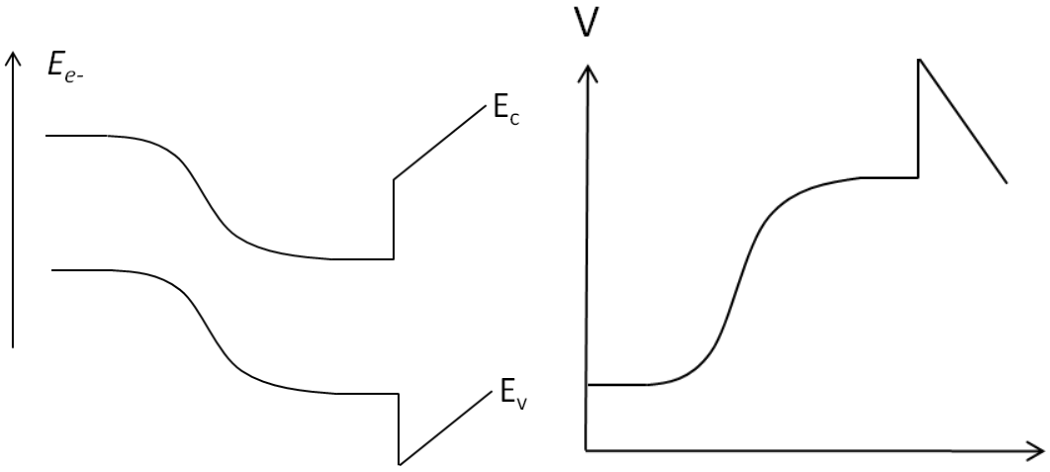
To determine the sign convention (+/-) of the electric field, we must remember what the band diagram represents. The band diagram is the projection of the molecular or atomic orbitals for the crystal lattice over a region of space. Moving in the positive direction on the vertical axis results in an increase in energy for electrons. Electrons have a negative charge; therefore, if the vertical direction on the band diagram indicates increasing energy for electrons, then it also indicates decreasing voltage for the conduction and valence bands. The vertical axis does not necessarily represent decreasing voltage for electrons, because all electrons in a given band are considered to be at the same potential. The difference between the bottom of the conduction band and an electron in an allowed state on the vertical axis is the kinetic energy of that electron.

If the slope of the conduction and valence bands is caused by an electric field, then from Gauss' law (2.2), we know that for the steady-state operation of a semiconductor device, the change in the slope is caused by charges in the semiconductor.

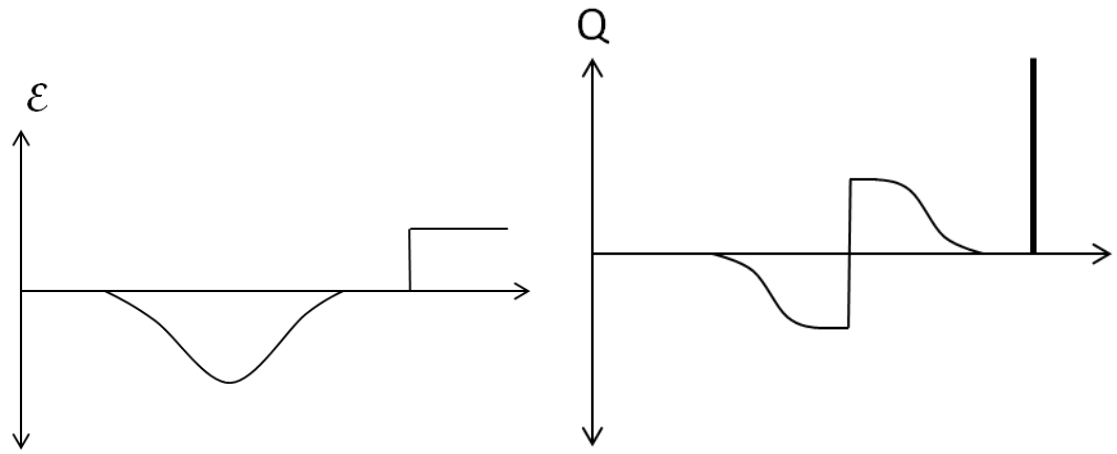
$$\nabla \cdot E = \frac{\rho}{\varepsilon_0} \tag{2.2}$$

Figure 2 displays a graphic representation of the principles of semiconductor band diagrams. Note: This is not an actual device; the band diagram is for illustrative purposes only. A semiconductor with a positive and negative charge distribution (possible from a

PN junction) is shown in contact with a larger band gap semiconductor creating a heterojunction. The semiconductor band diagram is shown in Figure 2.1(a) and the potential is shown in Figure 2.1 (b). As can be seen, the potential has the opposite slope of the band diagram due to the charge convention on the electron. Differentiating the potential as described in (2.1) give us the electric field in Figure 2c. A second differentiation produces the charge distribution in Figure 2d. What appears to be a discontinuity in the slope of the band diagram and the potential (2.1(a)–(b)) is actually a thin sheet of charge, in this case, at the surface of a heterojunction. This level of charge, concentration usually occurs at metal semiconductor junctions, but it can occur in semiconductors like AlGaN and GaN that have strong polarization effects.



(a) (b)



(c) (d)

Figure 2.1. Properties of the band diagram: (a) a band diagram with a heterojunction, (b) potential of the band diagram, (c) electric fields in the semiconductor, and (d) charge distribution.

2.2 Material Properties

While GaAs HEMTs have matured as a technology for high frequency circuits and have found many applications in communication devices and radar, GaN possesses properties that suggest it could be a superior material for high frequency, high-power microwave applications. One of its most attractive features is its wide bandgap. The bandgap of GaN is 3.4 eV, which is considerably larger than Si (1.1 eV) and GaAs (1.4 eV). This wide bandgap, in turn, leads to a higher breakdown voltage, which allows GaN devices to handle a greater amount of power before device failure. The high thermal conductivity of GaN allows it to dissipate the heat produced by high-power amplifiers. While the bulk mobility of GaN is less than other commonly used semiconductors, the mobility within the 2DEG compares favorably with some semiconductors, such as silicon and silicon carbide (SiC). These factors indicate the potential of GaN to operate at high power and relatively high frequencies. Engineers working on the development of GaN as a material for monolithic microwave integrated circuits (MMICs) expect to benefit from the amount of investment in material

development that goes into the much larger GaN optical market [7].

Table 2.1 provides a comparison of semiconductors and the properties useful for microwave amplifiers. Baliga's figure of merit (BFOM) measures the conduction losses of a device, which contributes to the efficiency of power amplifiers [8].

Property	Si	GaAs	4H-SiC	GaN
Bandgap, E_g (eV)	1.12	1.42	3.25	3.4
Dielectric constant, ε	11.8	12.8	9.7	9
Breakdown field, E_c (MV/cm)	0.3	0.4	3	4
Electron mobility, μ (cm^2/V s)	1500	8500	1000	1250
Maximum velocity, Vs (10^7 cm/s)	1	1	2	3
Thermal conductivity, k (W/cm K)	1.5	0.5	4.9	2.3
Tmax	300 C	300 C	600 C	700 C
BFOM	1	1.8	400	1600
JFOM	1	14.6	548	1507

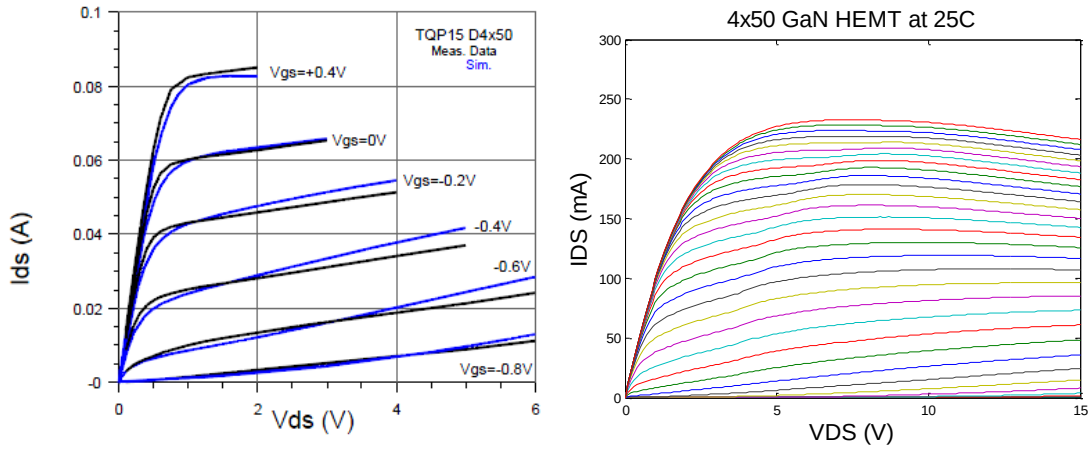
Table 2.1. A comparison of semiconductors and the properties useful for microwave amplifiers. [8,9]

Johnson's figure of merit (JFOM) is intended to measure the ultimate high frequency capability of a material [8]. The equations for these metrics are given in (2.3) and (2.4):

$$\mathrm{BFOM} = \frac{E_c^2 V_s^2}{4\pi^2} \tag{2.3}$$

$$\mathrm{JFOM} = \varepsilon \mu E_c^3 \tag{2.4}$$

Both of these values are normalized so that silicon has a value of one in Table 2.1. The data shows that, based on the metrics of the table, GaN outperforms all of the semiconductors listed. The practical effects of this material can be seen by comparing the load lines of a GaAs HEMT and a GaN HEMT. A comparison of current-voltage (I-V) curves of AlGaAs and aluminum gallium nitride (AlGaN) HEMTs is shown in Figure 2.2.



(a) (b)

Figure 2.2. Comparison of I-V curves of an AlGaAs HEMT with an AlGaN HEMT from Triquint: (a) 4x50 µm AlGaAs HEMT device performance [10] and (b) 4x50 µm AlGaN HEMT device performance.

Figure 2.3 shows a simplified circuit diagram, in which the FET is modeled as a voltage supply in series with an internal impedance.

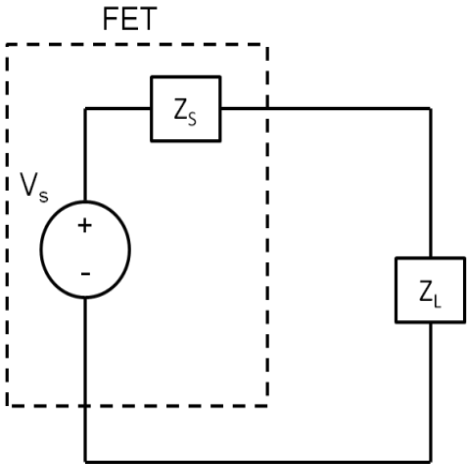


Figure 2.3. Circuit for determining power transfer with HEMT modeled as voltage source and series resistance.

Assuming that the device is operating at resonance in which $Z_L = Z_S^*$, the loads can be treated as being purely resistive. The RF power absorbed by the load is given in (2.5).

$$P_L = V_{RMS} I_{RMS} = \frac{1}{2} \Delta V_{Lpeak} \Delta I_{peak} \tag{2.5}$$

but since we can choose to operate at resonance and maximum power transfer,

$$\Delta V_{Lpeak} = \frac{R_L}{R_S+R_L}\,\Delta V_S = \frac{1}{2}\,\Delta V_S \tag{2.6}$$

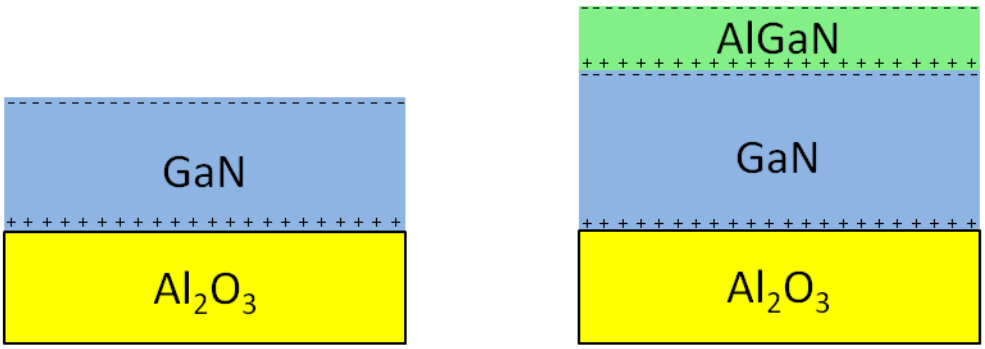
A similar calculation can be performed on the current to determine that with a matched load the total current supplied is reduced by half or $\Delta I_{peak} = ½\ \Delta I_{source}$. So the power to the load becomes

$$P_L = \frac{1}{8}\Delta V_S \Delta I_S \tag{2.7}$$

By visually inspecting Figure 3a, an RF engineer could select 4 V as the drain bias point. The knee voltage of the AlGaAs/GaAs HEMT is around 0.8 V. Therefore, one half of the RF voltage sweep is 3.2 and the total voltage sweep would be 6.4. The current change goes from 0 mA to 80 mA. Using (2.7), the first order approximation for the power transmitted to the load of the AlGaAs/GaAs HEMT presented Figure 3a can be calculated to be 0.125×6.4×0.08 or 64 mW. Using the same procedure for the AlGaN/GaN HEMT shown in Figure 3b, the value of the knee voltage can be determined to be 4 V, the bias point can be chosen to be 13 V (leading to a voltage sweep of 18 V), and the current sweep can be seen to be 230 mA. The power of the GaN HEMT can be calculated to be 0.125×18×0.23 or 517.5 mW. This simplified low frequency examination shows that a GaN HEMT supplies approximately eight times as much power as a similarly sized GaAs HEMT. This analysis does not compare the efficiency and frequency performance characteristics of the devices, which also favor GaN devices.

One of the superior properties of GaN that is not listed in table 2.1 is the fact that GaN is the only one of these materials that does not require doping with impurities to produce a two dimensional electron gas. When wurtzite AlGaN or GaN is grown on a

substrate, a spontaneous polarization is produced [11]. The substrates that have proven to produce GaN and AlGaN of sufficient quality to produce high frequency high-power HEMTs are silicon carbide and sapphire [9]. The spontaneous polarization is a result of the polarization of the bond between the gallium and the nitrogen. The bond is not fully covalent and the electron has a greater probability density with one atom compared to the other. Gallium has three electrons in its outer orbital and accepts and electron, which causes the gallium face of the crystal to have a negative polarity. The nitrogen face of the crystal has a positive charge, so the polarization vector points from the nitrogen face to the gallium face of the GaN crystal. Figure 2.4 shows the surface charge on the GaN crystal grown on a sapphire substrate.



(a) (b)

Figure 2.4. Charge sheets on GaN and AlGaN as it is grown: (a) charge polarity of GaN on sapphire and (b) charge polarity of AlGaN\GaN on sapphire.

The current in the HEMT is confined to the 2DEG layer in the GaN. This layer is located in a potential well in the GaN near the heterojunction with the AlGaN. Since charges are prevented from moving in the direction normal to the surface of the heterojunction, the number of dimensions that charges can move in the bulk are reduced by one, therefore, leaving an electron gas free to move in two dimensions, ergo a 2DEG. The term “two dimensional electron gas” is used to differentiate these types of devices (HEMTs), which

have their charges confined in the manner previously described, from other devices, in which charges are more distributed throughout the bulk of the device.

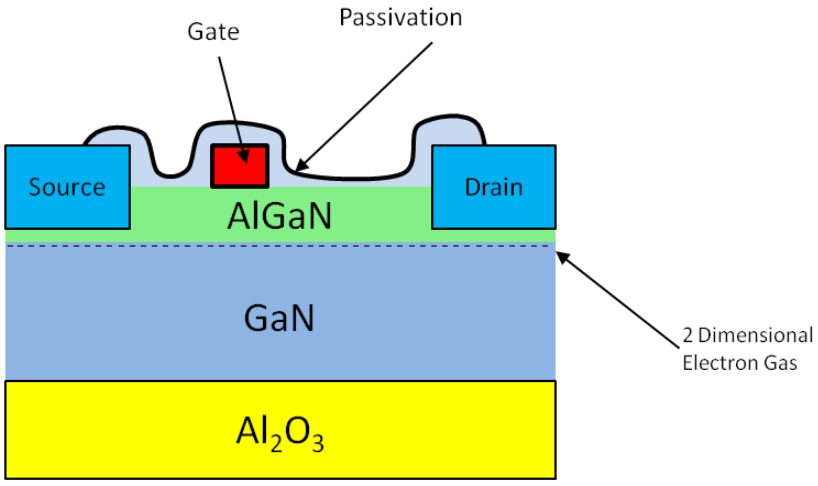
The surface charges on GaN and AlGaN are the sum of the spontaneous charge produced by electrical polarity inherent in the crystal and the piezoelectric charge, which is produced by the strain from growing the semiconductor on a mismatched lattice [12, 13]. The spontaneous surface charge on GaN is –2.9e-2 C/m^2, which amounts to 1.18e13 electrons/cm^2 [14]. The bound charge at the heterojunction interface is the sum of the negative charge on the GaN and the positive charge on the AlGaN and results in a net positive charge. Because these charges are opposite in sign, their sum results in a smaller charge than would exist on a pure crystal, if such a crystal were possible to produce. The spontaneous polarization charge and the lattice mismatch, which determines piezoelectric charge, are both a function of the aluminum content in the AlGaN. The total of all charges on the interface was determined theoretically to be the equation shown in (2.8):

$$|\sigma(x)| = P_{pz-Al_xGa_{1-x}N} + P_{sp-Al_xGa_{1-x}N} + P_{sp-GaN} + P_{sp-GaN} \quad (2.8)$$
$$= [(3.2x - 1.9x^2) \times 10^{-6} - 5.2 \times 10^{-6}x] C/\ cm^2$$

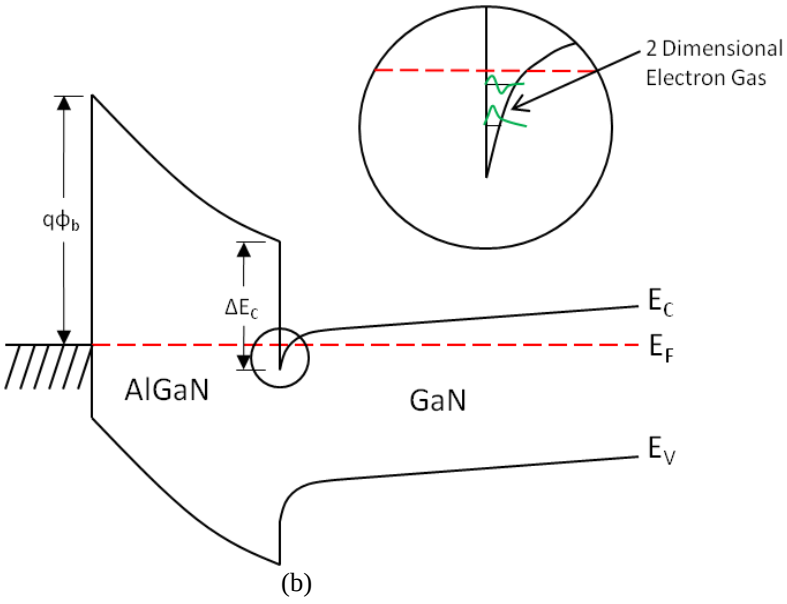
The negative charge sheet attracts positive ions from ambient environment, which can result in trapping states at the surface that create instabilities during device operation [14]. Other sources of trapping states include dangling bonds and dislocations. The effects of these surface states can be mitigated by shielding the AlGaN with a passivation layer of a material, such as silicon nitride (SiN) or aluminum nitride (AlN), which protects the AlGaN from the environment [14].

2.3 Device Cross Section and Band Diagram

It has been said that if a person cannot draw the band diagram of a semiconductor, then that person does not understand how that device works. To that end, a cartoon cross section of a semiconductor HEMT is shown in Figure 2.5(a) with the corresponding bandgap of a cross section of the device through the gate shown in 2.5(b).



(a)



(b)

Figure 2.5. (a) Basic AlGaN/GaN HEMT device cross section and (b) basic AlGaN/GaN HEMT band diagram.

The semiconductor stack of sapphire, GaN, AlGaN, and the passivation layer is shown in Figure 2.5(a). The HEMT is a three-terminal field effect device. The source and drain are embedded and make an ohmic contact with the AlGaN, GaN, and the current channel. Titanium and aluminum can be optimized to make good ohmic contact with GaN [15]. The gate is deposited on top of the AlGaN and forms a Schottky barrier that can be seen at the metal AlGaN junction in Figure 2.5(b). The band structure of the three materials, metal (Au), AlGaN, and GaN, is also visible in figure 2.5(b). The discontinuity in the slope at the metal-AlGaN junction is caused by the negative surface charge on the AlGaN. The strong electric field in the AlGaN can be seen in the slope of the bandgap in the material. The net positive charge at the AlGaN-GaN junction causes the slope to bend up steeply creating a potential well in the conduction band that is filled with electrons in the 2DEG. The high negative charge density of the 2DEG decreases the electric field over a short distance. The negative charge of the 2DEG decreases the slope at the heterojunction.

The Schottky barrier height of gate is given in (2.9) [16]:

$$q\varphi_b = \Phi_m - \chi \tag{2.9}$$

where Φ_m is the work function of the metal and χ is the electron affinity of the AlGaN. The work function of gold is 5.1 eV. The electron affinity of GaN is 4.1 eV, and the electron affinity for AlN is 0.6 eV [17]. An equation reported to be the work function of AlGaN is shown in (2.10) [18]:

$$\chi_{AlxGa1-xN} = 4.2 - 2.15\ x\ eV \tag{2.10}$$

The equation for the step height is shown in (2.11) [13]:

$$\Delta E_C = \left|\chi_{AlxGa1-xN} - \chi_{GaN}\right| \text{ eV} \tag{2.11}$$

The bandgap of $Al_xGa_{1-x}N$ is given by (2.12) [19,20]:

$$E_{g,AlxGa1-xN}(x) = x \cdot E_{g,AlN} + (1-x) \cdot E_{g,GaN} - b \cdot x \cdot (1-x) \text{ eV} \tag{2.12}$$

where b is the bandgap bowing parameter that has been determined to be 0.35 eV through simulation. The bandgap energy of AlN is 6.46 eV. Evaluating (2.12) numerically gives the bandgap of AlGaN as a function of aluminum content as in (2.13):

$$E_{g,AlxGa1-xN}(x) = 3.43 + 2.68\,x + 0.35\,x^2 \text{ eV} \tag{2.13}$$

With an understanding of the band structure, we can begin to look at the equations that govern the distribution of charges in the 2DEG.

2.4 Schrödinger Equation

We begin with the wave equation. If we assume that there is symmetry along the *z*-axis, we can write the wave function as

$$\Psi_m(x,y,z) = \xi_n(z)e^{j\theta}e^{jk_1x+jk_2y} \tag{2.14}$$

Using this we can write the Schrödinger wave equation as

$$-\frac{\hbar}{2}\frac{\partial}{\partial z}\left(\frac{1}{m^*}\frac{\partial \xi_n}{\partial z}\right) + \frac{\hbar^2(k_1^2+k_2^2)}{2m^*}\xi_n + V^*(z)\xi_n = E\xi_n \tag{2.15}$$

In this equation, E is the energy, m^* is the effect mass of the electron, k is the wave number, and V is the potential as a function of z. The potential is a function of the band structure, the surface charge at the heterojunctions, and also the distribution of charges in the semiconductor including the 2DEG. Assuming symmetry in the *x* and *y* dimensions,

we can write the potential as

$$V^*(z) = -e\,\phi(z) + \Delta E_C\,U(z) \tag{2.16}$$

where $\phi(z)$ is the potential as a function of space, e is the charge on the electron, and $U(z)$ is the unit step function. For this equation, the heterojunction is defined as z=0. Within a bandgap, the change in voltage is a caused by an electric field as seen in (2.1), and a change in electric field is caused by the distribution of charges (2.2).

The charge distribution of the electrons in the 2DEG will have the form of

$$\rho(z) = -q\sum n_m|\Psi_m(z)|^2 \tag{2.17}$$

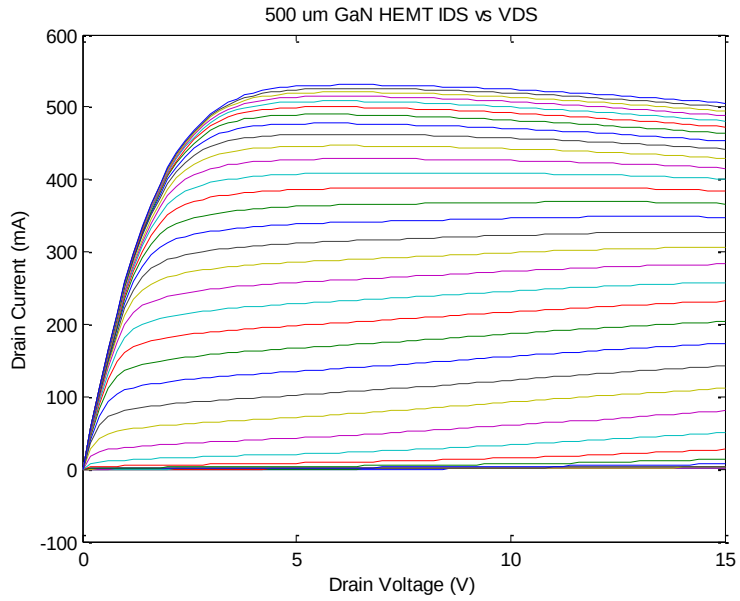
where ρ is the two-dimensional charge density, ψ is the solution to the wave function in the quantum well, and n is the number of allowed states for a given Eigen function. A number of variables determine the value of n_m, including the density of states of that function, the energy level of each solution, and the probability that a given energy level will be filled, which is determined by the Fermi-Dirac probability distribution function. By making simplifying assumptions, the wave function can be solved explicitly, but in order to produce results that are meaningful to practical applications like fabricated devices, these equations must be solved numerically. Theory and experiment have shown that the electron density of the 2DEG at the AlGaN/GaN can rise as high as 10^{13} cm^{-2} or a charge density of around 2^{-5} C/cm^2 [21–23]. The mobility of the 2DEG has been measured to be 1200–1500 cm^2/Vs [8, 23]. The high current densities of AlGaN/GaN HEMTs are of interest to device physicists, but this characteristic would be useless were not also possible to turn off the current. The solution to these equations can also be modified by altering the boundary values of the potential. This is, in effect, what happens

as the device is biased. The voltage on the edge of the gate metal is adjusted, which, in turn, increases or decreases the potential well at the heterojunction, causing a modulation of the current.

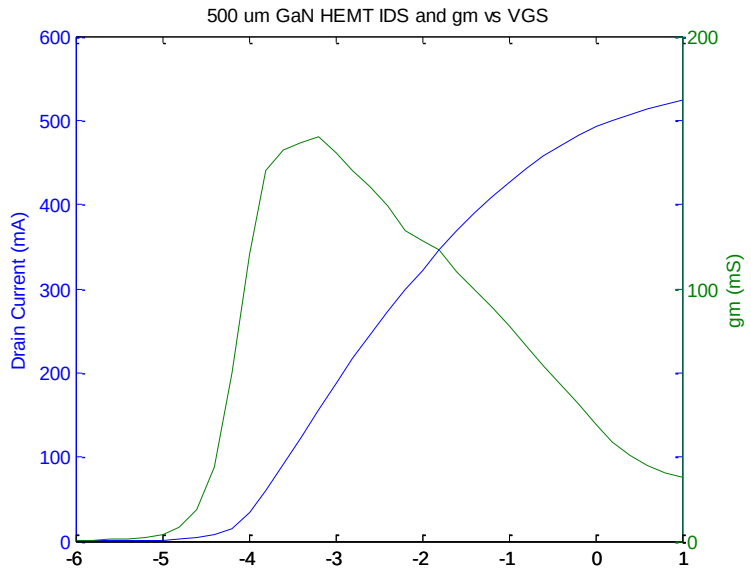
During operation, the drain is positively biased with respect to the source causing current to flow through the channel created by the 2DEG. The channel is controlled by the gate. When the gate is grounded or allowed to float, the channel conducts current freely. As the gate is biased negatively with respect to the source, the depth of the quantum well decreases and the current flowing from drain to source is reduced. GaN HEMTs that behave in this manner are depletion (normally on) mode devices and are by far the most common type currently being developed. The ability of a HEMT to operate as a switch or amplifier is based on its ability to turn small changes in gate voltage into large changes in drain current. The definition for transconductance is shown in (2.18):

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{2.18}$$

Figure 2.6 shows the relationship between current and voltage for a 500μm gate width AlGaN/GaN HEMT.



(a)



(b)

Figure 2.6. (a) I-V characteristics for measured 500-µm GaN HEMT, showing the (b) drain current vs. drain voltage over a range of gate voltages and the drain current vs. gm.

The drain current–drain voltage curve for this device is shown in Figure 2.6(a). Figure 2.6(b) shows the drain current–gate voltage along with the transconductance for the same device at a drain voltage of 10 V.

2.5 Frequency

Up to this point, although the fact that GaN has improved high frequency performance has been mentioned, the device has only been examined during steady-state operation. For high frequency devices, there are two important metrics for measuring device performance: cutoff frequency (f_t) and frequency of maximum oscillation (f_{max}). The cutoff frequency is defined as the frequency at which the current gain is unity. The equation for this is shown in (2.19) [24]:

$$f_t = \frac{g_m}{2\pi\,(C_{gs}+C_{gd})} \tag{2.19}$$

where gm is the transconductance, C_{gs} is the gate-source capacitance, and C_{gd} is the gate-drain capacitance. The maximum frequency of oscillation is the frequency at which the unilateral power gain is equal to unity. A first order approximation for this is shown in (2.20) [24]:

$$f_{max} = \frac{f_t}{2}\sqrt{\frac{R_o}{R_{in}}} \tag{2.20}$$

As can be seen from these equations, both of these parameters are geometry dependant. This means, for a given technology and fabrication process, one device will have a specific f_t and f_{max} and another device with a different total gate width will have a different f_t and f_{max}. The ratio between f_t and f_{max} will also change with the gate width. Microwave engineers who design MMICs factor the size dependence of these critical frequencies when deciding whether to combine several devices or to scale up to a larger single device. The parameter values used to calculate f_t and f_{max} in (2.19) and (2.20) are not always well known. In general, f_t and f_{max} can be extracted explicitly from measured

data. An equation for h_{21} is shown in (2.21) [25]:

$$h_{21} = \frac{-2S_{21}\sqrt{R_1 R_2}}{(1-S_{11})(Z_2^* + S_{22}Z_2) + S_{12}S_{21}Z_2} \tag{2.21}$$

where Z_j is the normalized impedance of the jth port and R_j is the real component of that impedance.

An equation for unilateral power gain is given in (2.22) [24]:

$$U = \frac{|y_{21} - y_{12}|^2}{4(Re[y_{11}]Re[y_{22}] - Re[y_{12}]Re[y_{21}])} \tag{2.22}$$

The S-parameters from the device in Figure 2.6 were measured at a drain voltage of 10 V and a gate voltage of –3.2 V. Using this data, the unilateral power gain and h_{21} were calculated and plotted in Figure 2.7.

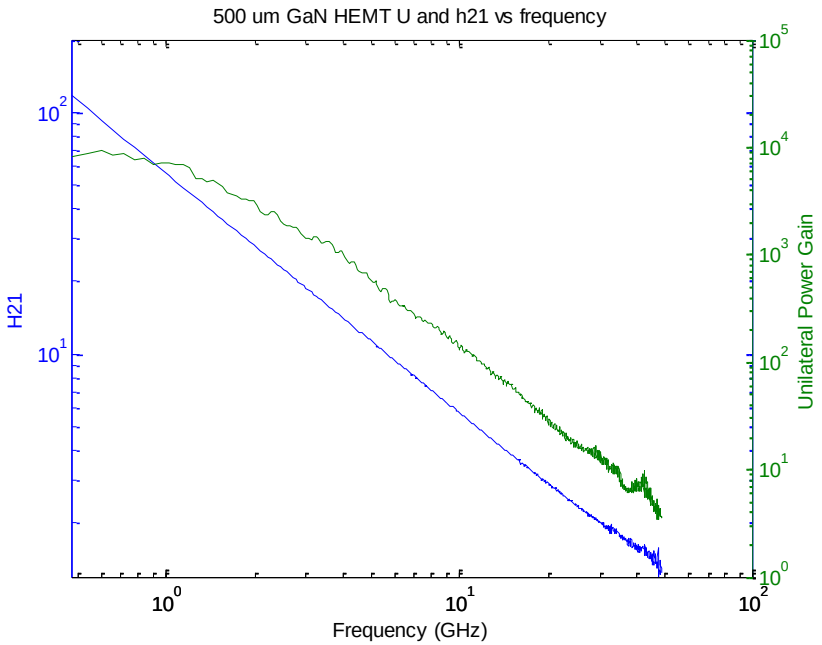


Figure 2.7. Critical frequency parameters of a 500µm GaN HEMT. h_{21}, and unilateral power gain plotted as a function of frequency.

By plotting the parameters on a logarithm scale in amplitude and frequency, a linear

relationship is observed between frequency and amplitude. This is then extrapolated linearly until the lines cross zero on the logarithmic scale. The point at which h_{21} crosses zero is the cutoff frequency, for this 500μm AlGaN/GaN HEMT device, it was calculated to be 61.8 GHz. The point at which U crosses zero is the maximum frequency of oscillation, and was calculated to be 104.2 GHz for this device.

Chapter 3: Experimental Apparatus

Now that we have established a basic understand of the technology being investigated, it is now necessary to look at the means by which it will be investigated. In this section, the equipment used to make the measurements and the measurements themselves will be described. The ARL Lifetime Extended Reliability Test Station (ALERTS) is a combination of hardware used to make measurements and the software used to control the system and analyze the data. An understanding of the system begins with a review of the instruments used to make the measurements.

3.1 System Overview

ALERTS is an on-wafer measurement system capable of making DC, the scattering parameter (S-parameter), and RF power measurements over a range of temperature from –30 °C to +175 °C. A photograph of the system is shown in Figure 3.1.

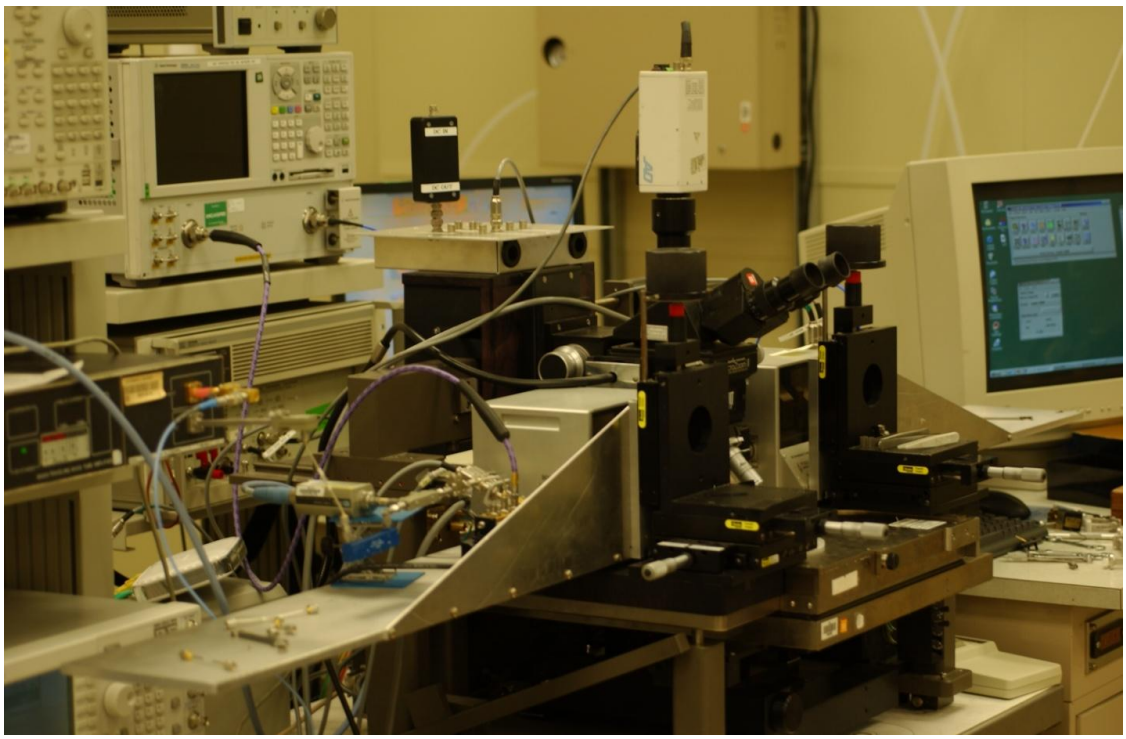


Figure 3.1. Photograph of the Lifetime Extended Reliability Test Station taken at ARL's semiconductor design and test laboratory.

The block diagram of the test station is shown in Figure 3.2.

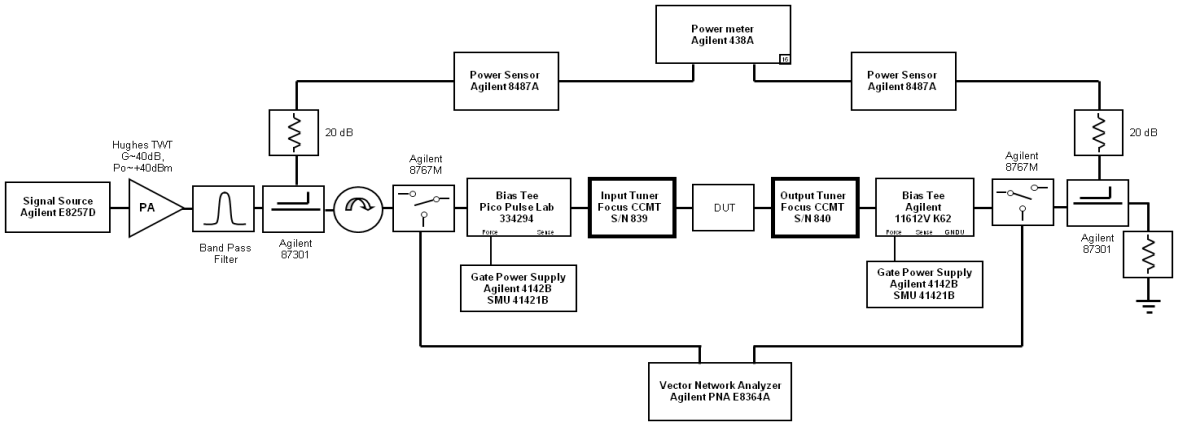


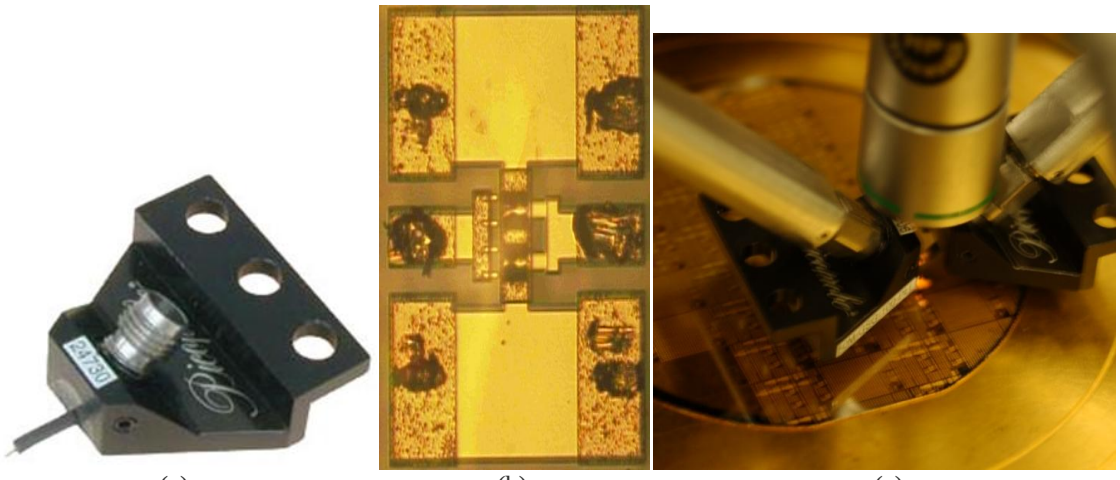
Figure 3.2. Block diagram of ALERTS.

All instruments in the system that collect data or apply voltage or RF energy to the device were networked using general purpose interface bus (GPIB) cables and controlled centrally by a computer. The software controlling the system uses MATLAB to communicate with the equipment, collect data, and process the data. The system controller is not shown in the block diagram. The instruments that make up the system will be discussed as the measurements the system performs are discussed.

3.2 Direct Current Control and Measurement

A simple measurement from which a great deal of information can be extracted is the current-voltage (I-V) measurement. The HEMTs being investigated in this research are three-port devices. In order to test these devices, it is necessary to be able to apply an arbitrary bias voltage to two separate ports on the device under test (DUT) with the third port being used as a reference. The devices examined in this research were designed to be measured using ground-signal-ground on wafer probes with a pitch (with a spacing

between the probe tips of 100 µm). The probes used were procured from GGB Industries. The model of the probes was 50M-GSG-100-PLL with a 45° angle for the 2.4-mm coax connector. These probes use a geometry designed to minimize losses, and are specified to have an insertion loss of less than 1.0 dB with a typical loss of 0.85 dB [26]. A photograph of a GGP picoprobe is shown in Figure 3(a) [26]. A typical FET designed to be tested by GSG probes is shown in Figure 3(b). The marks are visible on the FET indicate where a probe was used to make contact with the device during measurement. A device being tested on-wafer by ALERTS is shown in Figure 3(c).



(a) (b) (c)

Figure 3.3. (a) Photograph of GGB picoprobe, (b) the GaN HEMT designed to be tested with on wafer probes, and (c) the GaN HEMT wafer being tested using picoprobes during reliability measurements.

The majority of the DC measurements were made using a HP 4142B Modular DC Source/Monitor, which is a programmable and expandable power supply capable of housing and controlling up to eight separate modular power units. This system makes use of a controller that communicates with external systems and controls the modular units. The ALERTS system used two power supply modules in the HP 4142B. The modular power component providing the gate voltage is the HP 41421B Medium Power Source/Monitor Unit (MPSMU). The MPSMU is capable of a peak voltage of ±100 V

and a peak current of ±100 mA, though these peaks cannot be achieved simultaneously. The drain voltage is provided by the HP 41420A High Power Source/Monitor Unit (HPSMU), which is also housed in the HP 4142B. The peak voltage achievable by the unit is 200 V and the peak current is up to 1 A, again these peaks cannot be achieved at the same time. The DC voltage is applied to the RF coax using a bias T. The bias T is a simple device that combines an RF power source with a DC power source so that both components can be applied to a DUT. On the RF path of the bias T, a large capacitor serves as a block for the DC power while passing RF power. In the DC path, a large inductor conducts DC power while presenting a high impedance to the RF path. The bias T's in the system used to conduct this research are capable of conducting RF from 400 MHz to 50 GHz. After the bias T, the RF and DC paths are combined. The bias voltage is conducted through the inner coax of the microwave tuners. These are connected to coax air lines to which the GGB probes are mounted. The components of the system used during DC measurements are shown in the block diagram shown in Figure 3.4. The actual instruments used in the DC path are highlighted in blue.

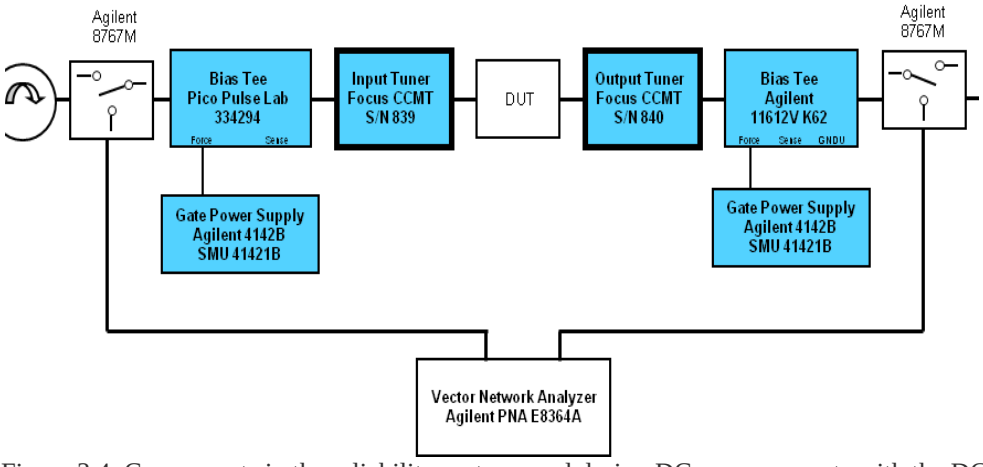


Figure 3.4. Components in the reliability system used during DC measurements with the DC path highlighted.

3.2.1 DC Calibration

The power modules of the HP 4142B are equipped with Force and Sense lines. The Force line is designed to be the high current line. As a result, if there is any voltage drop along the Force line, the Sense line, which is low current, will measure and correct for the loss. Unfortunately, the Force and Sense lines connect with the bias T, and the correction for voltage loss in the transmission lines does not account for the voltage drop in the bias T or from the bias T to the DUT [27].

Resistances of tenths of ohms to several ohms in transmission lines have been measured in laboratory systems from the power supply to the DUT. The high current HEMTs being measured can draw currents of several hundred milliamps. In this situation, the voltage drop in the transmission lines may be as much as several tenths of volts. In order to properly characterize the DUT, the losses in the transmission line and the voltage drop across the line must be measured and accounted for. Thus, a procedure was developed to measure the DC transmission line resistances between the voltage source and the DUT. Once these values are known, it is necessary to apply a transform to the raw measured data to determine the actual voltages on the device of interest. A simple MATLAB code for determining the DUT current and voltage behavior was developed to use when the raw I-V data and transmission line resistances are known. In order to use the procedure described, the Sense line should not be used.

A circuit diagram of the DC conduction path showing the transmission line resistances is shown in Figure 3.5(b). As can be seen in Figure 3.5(b), the four unknown resistances that need to be determined are RP1, RC1, RP2, and RC2. This will require four separate

measurements and four corresponding equations. For each measurement configuration, a separate resistance was recorded.

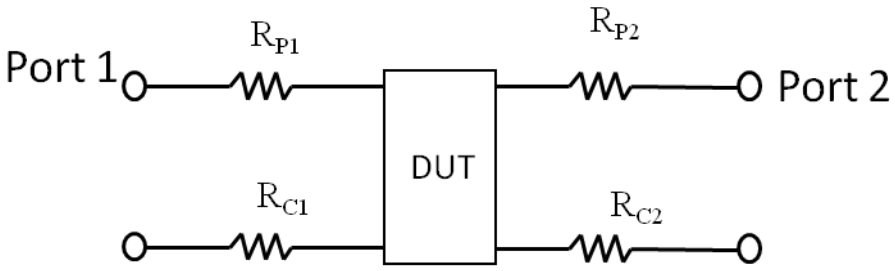
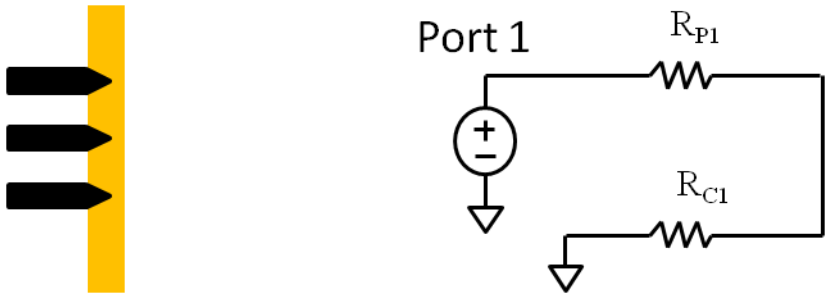


Figure 3.5. Circuit diagram of DC measurement system.

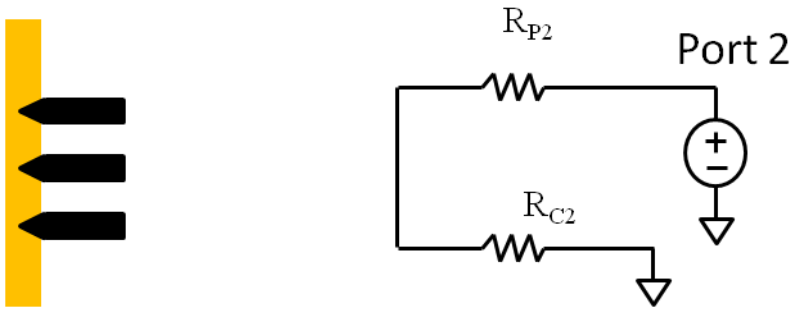
The first measurement is made by shorting the probe on port 1. Figure 3.6(a) shows a picture of how to land a GSG probes onto a metallic standard. The black signifies the probes and the yellow signifies the metallic standard. Figure 3.6(b) shows the circuit diagram of the measurement. The resistance for this measurement is R1 and is measured by sweeping the voltage across a range of values while recording the current.



(a) (b)

Figure 3.6. Determination of R1 (a) picture of proper probe placement for short across probe for port 1 and (b) the circuit diagram for measurement of R1.

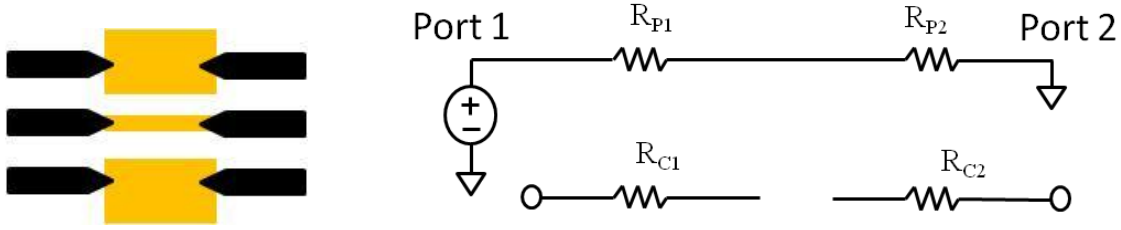
The second measurement is made by shorting the probe on port 2. Figure 3.7(a) shows a picture of how to land a GSG probes onto a metallic standard. Figure 3.7(b) shows the circuit diagram of the measurement. The resistance of this measurement is labeled R2 and it is measured by determining the slope of the I-V measurement on this port.



(a) (b)

Figure 3.7. Determination of R2 (a) picture of proper probe placement for short across probe for port 2 and (b) the circuit diagram for measurement of R2.

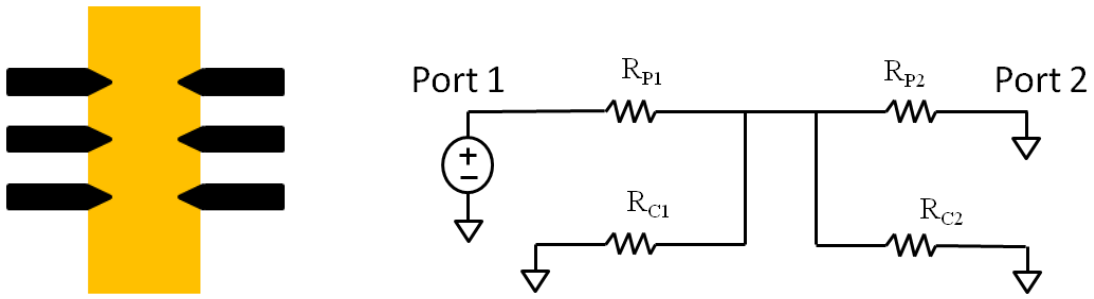
The third measurement is made by landing the probes on a through standard, like the kind typically used in a thru-reflect-line (TRL) S-parameter calibration. Figure 3.8(a) shows a picture of how to land a GSG probes onto a metallic standard. Figure 3.8(b) shows the circuit diagram of the measurement. The resistance is measured by setting one of the ports to ground and sweeping the voltage across a range of values while recording the current. This resistance is labeled as R3.



(a) (b)

Figure 3.8. Determination of R3 (a) picture of proper probe placement for thru measurement from port 1 to port 2 and (b) the circuit diagram for measurement of R3.

The final measurement is made by landing both probes on a solid metallic standard. Figure 3.9(a) shows a picture of how to land a GSG probes onto a metallic standard. Figure 3.9(b) shows the circuit diagram of the measurement. The resistance for this measurement is R4 and is measured be setting the voltage on port 2 to 0 V and sweeping the voltage on port 1 across a range of values while recording the current.



(a) (b)

Figure 3.9. Determination of R4 (a) picture of proper probe placement for shorting all probe tips and (b) the circuit diagram for measurement of R4.

There are other options for generating the required four equations; however, these are the ones used in the procedure described in this dissertation. It is also possible to make use of the ability to measure current from both ports in the final measurement.

3.2.1.1 Calculation of Resistances

The equations for each of the measured resistances are shown below.

$$R1 = R_{P1} + R_{C1} \tag{3.1}$$

$$R2 = R_{P2} + R_{C2} \tag{3.2}$$

$$R3 = R_{P1} + R_{P2} \tag{3.3}$$

$$R4 = R_{P1} + \frac{1}{\frac{1}{R_{P1}} + \frac{1}{R_{C1}} + \frac{1}{R_{C2}}} \tag{3.4}$$

When these are solved for the desired transmission line resistances, we find the equations for these to be

$$R_{P1} = \frac{R1\,R3 + R2\,R4 - R3\,R4 \pm \sqrt{R2\,(R1 + R2 - R3)\,(R1 - R4)\,(R3 - R4)}}{R1 + R2 - R4} \tag{3.5}$$

$$R_{C1} = \frac{R1^{\,2} + R1\,R2 - R1\,R3 - R1\,R4 - R2\,R4 + R3\,R4 \pm \sqrt{R2\,(R1 + R2 - R3)\,(R1 - R4)\,(R3 - R4)}}{R1 + R2 - R4} \tag{3.6}$$

$$R_{P2} = \frac{R2\ R3 - R2\ R4 \pm \sqrt{R2\ (R1 + R2 - R3)\ (R1 - R4)\ (R3 - R4)}}{R1 + R2 - R4} \quad (3.7)$$

$$R_{C2} = \frac{R2^{\,2} + R1\ R2 - R2\ R3 \pm \sqrt{R2\ (R1 + R2 - R3)\ (R1 - R4)\ (R3 - R4)}}{R1 + R2 - R4} \quad (3.8)$$

3.2.1.2 Procedure for determining DUT voltages

Once the transmission line resistances are know, it becomes possible to mathematically determine the voltage on the DUT. Figure 3.10 shows the circuit diagram of a FET with the transmission line resistances included.

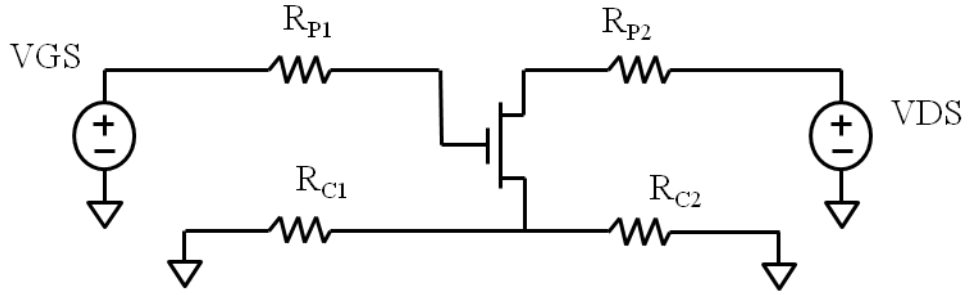


Figure 3.10. Measurement of FET with transmission line resistances.

From Figure 3.10, it can be seen that the voltages on the DUT are given by

$$VGS_{DUT} = VGS_{Source} - I_g\ R_{P1} - (I_g + I_d) \cdot (R_{c1} \| R_{c2}) \quad (3.9)$$

$$VDS_{DUT} = VDS_{Source} - I_d\ R_{P2} - (I_g + I_d) \cdot (R_{c1} \| R_{c2}) \quad (3.10)$$

This produces a set of voltages that are slightly different from the power supply voltages. Current voltage curves are, by tradition, normally presented as currents dependant on equally spaced voltages. The voltages calculated when accounting for transmission line loss are not equally spaced. It is possible to use interpolation to find the current at the supplied voltage points.

3.2.1.3 Results

The measurements described were performed on our system with the results shown below:

$R1 = 5.42\,\Omega$

$R2 = 0.92\,\Omega$

$R3 = 6.16\,\Omega$

$R4 = 0.79\,\Omega$

Using these values the following transmission line resistances were calculated:

$R_{P1} = 5.38\,\Omega$

$R_{C1} = 0.04\,\Omega$

$R_{P2} = 0.78\,\Omega$

$R_{C2} = 0.14\,\Omega$

The DUT voltages for a typical I-V curve were calculated in a MATLAB program by removing the voltage drop across the transmission line resistances from raw measured I-V data. The same program interpolated the current to the original power supply voltages. Figure 3.11 shows a plot of the original measured current and the interpolated current.

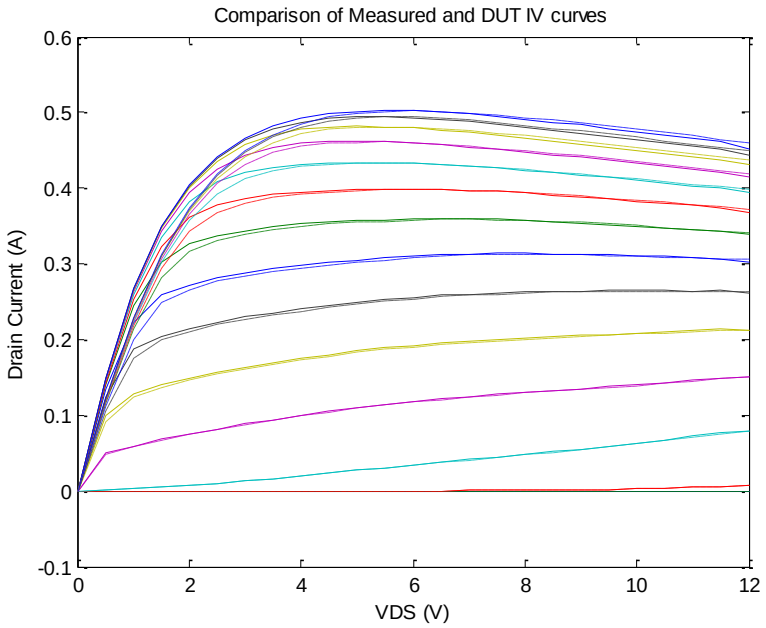


Figure 3.11. Measured I-V curve (dash line) plotted besides calculated.

As can be seen in figure 3.11, there is a non-trivial difference between the measured I-V characteristics and the actual I-V characteristics of the DUT. This is especially true in the linear (ohmic) region of device operation.

3.2.2 Direct Current Measurements

With the procedures for determining the DUT voltages established, we can now look at the measurements that can be made using the DC measurement instruments. By using the RF switches, the measurements system can switch from a configuration for making RF-power measurements and a configuration for making S-parameter measurements. The DC voltage bias is unaffected by the switching. The DC measurement can be made in either configuration.

There are two measurements performed on the DUT that are can be considered to be made by the DC system. These are the I-V curve measurement and the gate current measurement. In theory, these can be performed in either the RF or S-parameter

configuration; however, during a reliability test these measurements are always performed in the S-parameter configuration to minimize the effects of RF noise from the traveling wave tube (TWT) on the current of the DUT. The I-V measurement sweeps the drain voltage while measuring the drain current. The process is repeated over a range of gate values, making it possible to determine the effect of the gate voltage on the drain current. During this measurement, the voltage and current for both the gate and drain are recorded.

The gate current measurement is a simplified version of the I-V curve measurement. The drain voltage is set to zero during the gate measurement putting it at the same voltage as the source. The gate is biased to a negative value several volts below the voltage required to pinch off the device. The voltage on the gate is gradually increased to a positive voltage sufficient to record the turn-on behavior of the gate diode. The gate current is recorded during these measurements. Examples of these measurements are shown when the Extended Reliability Measurement Algorithm is discussed in the next chapter.

3.3 S-parameter Measurements

One of the fundamental measurements in RF and microwave engineering is the S-parameter measurements. The instrument used to measure S-parameters in ALERTS is an Agilent E8364A PNA. The PNA is used to characterize microwave components used during the RF power measurements. It is also used to directly measure the S-parameters of the DUT. The configuration for ALERTS during S-parameter measurement is shown in Figure 3.12.

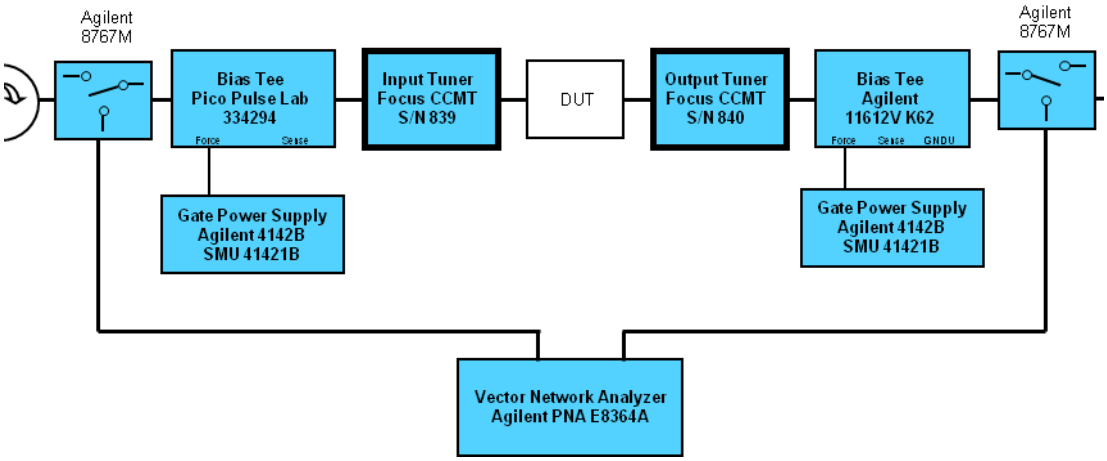


Figure 3.12. Components in the reliability system used S-parameter measurements.

All of the components used in the DC measurement are used in the S-parameter measurement. This is necessary to bias the DUT to the desired conditions during the measurement. The Load Pull/Source Pull Tuners are put into their initialized state to prevent them from interfering with the RF calibration. The Agilent 8767M RF switches are used to switch between the RF power configuration and the S-parameter configuration. When measuring S-parameters, the RF switches serve to isolate the TWT from the DUT and PNA. The RF power from the power supply is reduced to the lowest level and turned off. This decreases the power from the TWT to the noise floor of that device. The PNA must be calibrated prior to being used to measure the microwave components of the system. This was done by using a custom designed calibration kit from Focus Microwaves. The parameters of this kit were entered manually into the PNA. To measure the DUT, a separate on wafer calibration is conducted to characterize the S-parameter block between the ends of the flexible coax cables connected to the PNA and the on-wafer probe tips.

3.3.1 S-parameters

The S-parameters are a measurement of the ratio of the output voltage on a port divided by the incident voltage on a port normalized for the port impedance. Although there is talk of nonlinear S-parameters, the S-parameter is an inherently linear measurement and the results of the measurement are only valid in the small signal scale. The HEMTs are three-port devices; however, the source was always grounded during this research. As a result, all of the S-parameter measurements made were two-port measurements, and the discussion of the theory of S-parameters will be constrained to two ports. A generalized mathematical definition of S-parameters is given in (3.11) [28].

$$S_{ij} = \left.\frac{V_i^- \sqrt{Z_{0j}}}{V_j^+ \sqrt{Z_{0i}}}\right|_{V_k^+ = 0 \text{ for } k \neq j} \tag{3.11}$$

where S_{ij} is by definition the value of the scattering matrix element in position i, j; and V_n is the voltage on port n. The plus and minus signs are the convention for incident and transmitted or reflected power, respectively. The reference impedance of port n is given by Z_{0n}. For all S-parameters used in this research, the reference impedance used was 50 Ω. This simplifies (3.11) to (3.12).

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+ = 0 \text{ for } k \neq j} \tag{3.12}$$

When S-parameters are graphed on a logarithmic scale, they are normalized to provide a power ratio. Since, power is proportional to the square of voltage, when S-parameters are plotted on the dB scale the following relationship will be used:

$$S_{dB} = 20 \times \text{Log}_{10}\left|S_{comp}\right| \tag{3.13}$$

where S_{dB} is the decibel value of the S-parameter and S_{comp} is the actual complex scattering parameter.

One of the reasons S-parameters are such an effective representation of the RF behavior of a microwave component or device is that they can be plotted on the Smith Chart. The Smith Chart is a conformal mapping of the impedance (or admittance) plane to the unit circle. Using the Möbius Transformation, shown in (3.14), any three points in one plane can be mapped to any three points in another plane [29].

$$T(z) = \frac{(z-z_1)(z_2-z_3)}{(z-z_3)(z_2-z_1)} \tag{3.14}$$

where T is the transform; z is the complex variable; and z1, z2, and z3 are three arbitrary points in the *z* plane. To map one plane to another, we must generate a Möbius Transformation for each plane using the points that will be projected onto the map. These points are then set equal to each other. With the new equation, it is possible to solve for the desired variable of the new plane. In the case of the Smith Chart, 50 in the impedance plane is mapped to the origin in the Smith Chart, 0 in the impedance plane is mapped to -1 in the Smith Chart, and infinity in the impedance plane is mapped to +1 in the Smith Chart. The Möbius Transformation for each is shown below:

$$T(z) = \frac{(z-z_1)(z_2-z_3)}{(z-z_3)(z_2-z_1)} = \frac{(z-50)(0-\infty)}{(z-\infty)(0-50)} = \frac{(z-50)}{-50} \tag{3.15}$$

where z1 is 50, z2 is 0, and z3 is infinity

$$W(\Gamma) = \frac{(\Gamma-\Gamma_1)(\Gamma_2-\Gamma_3)}{(\Gamma-\Gamma_3)(\Gamma_2-\Gamma_1)} = \frac{(\Gamma-0)(-1-1)}{(\Gamma-1)(-1-0)} = \frac{2\Gamma}{(\Gamma-1)} \tag{3.16}$$

where ρ1 is 50, ρ 2 is 0, and ρ 3 is infinity.

These equations are set equal to each other and solved for the variable in the new plane, which in this case is Γ.

$$\frac{2\Gamma}{(\Gamma-1)} = \frac{(z-50)}{-50} \tag{3.17}$$

Solving for Γ gives us

$$\Gamma = \frac{Z-50}{Z+50} \tag{3.18}$$

which is the equation for a point on the Smith Chart for a given impedance. (3.18) is also the equation for the reflection coefficient for a port. From the definition of S-parameters in (3.12), we can see that the reflection coefficient of port n is S_{nn}. This means that by measuring the S-parameters of a system, we have already determined the impedance of a component and, by extension, the optimal match for minimizing loss, since reflection loss is minimized by terminating a port with the complex conjugate of the impedance of that port.

Scattering parameters are a useful tool for displaying the RF properties of a system, and they completely characterize a component's linear behavior for a given set of operating conditions, such as bias or temperature; however, despite the prevalence of displaying S-parameters in matrix form, these are not matrices upon which it is possible to perform matrix algebra and produce an answer that is meaningful for microwave systems. Since a scattering matrix completely characterizes the linear behavior component, it is possible to transform it into any of a family of matrices that also characterize the component. Furthermore, it is possible to cascade some of these matrices through matrix multiplication. Two of the representations that produce matrices that can

be cascaded are the T-parameters and the ABCD parameters. T-parameters were selected to be used in this research. Several other types of parameters were used to represent two-port networks in this research in order to determine the component parameters of the equivalent circuits models for different microwave components. These parameters are the admittance parameters (Y), impedance parameters (Z), and Hybrid Parameters (H). Appendix A has the conversions used to convert between two-port matrices that were used in this research [30, 31].

3.3.2 TRL Calibration

The calibration performed on the Agilent E8364A PNA was accomplished by using application-specific calibration standards from Focus Microwaves. The calculations for calibrating the PNA were performed using Agilent's internal software [32]. This calibration allows the PNA to correct for losses and phase shifts between the output ports on the PNA and the ends of the cables. The Focus Microwaves software also contains calibration algorithms to correct for unknowns between the cable ends and the tips of the on-wafer GSG probes; however, at various points in this research, it was necessary to implement our own calibration algorithm in the software. In order to determine the performance of a device, it is necessary to have a method to use measurements on the ports of the vector network analyzer (VNA) to describe the RF state at the DUT. Typically, components are modeled as matrix blocks and de-embedded to the desired reference plane. There is an input block and an output block. It is a non-trivial exercise to determine the S-parameters of these blocks, though a number of techniques exist to do so. The one described in this document is the Thru-Reflect-Line (TRL) technique. The VNA has built-in software that allows the user to employ a calibration kit to de-embed

the measurements to the tips of the cable. The Focus Microwaves software has an algorithm to de-embed the measurements to the probe tips using an on-wafer calibration standard. Both the Focus Microwaves software and the Agilent VNA contain algorithms to perform a TRL calibration. In addition to these, a TRL calibration procedure was implemented using the following calculations in MATLAB.

TRL is a well-known calibration technique, and is included here for completeness, because often when it is encountered in literature or publications it is incorrectly explained or contains an error. The TRL calibration requires four measurements and produces two S-parameter blocks, one for each of the blocks on the two ports of the measurement system [33]. Figure 3.12 shows the measurement system used to perform the TRL calibration. The input block, called block A, is on the left side of the system in the block diagrams between the VNA and the DUT. The output block, or block B, is on the right side of the system from the DUT to the PNA.

The four measurements are taken from well-known standards. The measurements are as follows:

1. thru line
2. delay line
3. short-circuit measurement on port 1
4. short-circuit measurement on port 2

To mathematically manipulate the blocks, they must be converted from S-parameters, which contain information in an easily readable format, to matrices, which can be

cascaded using standard matrix algebra. In this case, the previously mentioned T-parameters were used.

We assume our calibration standards have the following S-parameters:

$$S_{THRU} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{3.19}$$

$$S_{LINE} = \begin{pmatrix} 0 & e^{i\theta} \\ e^{i\theta} & 0 \end{pmatrix} \tag{3.20}$$

The unknown arbitrary phase shift of the delay line is θ. The short circuits have a reflection coefficient of negative one. Using (3.19), the following T-matrices for the thru and the line were calculated:

$$T_{THRU} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \tag{3.21}$$

$$T_{LINE} = \begin{pmatrix} e^{-i\theta} & 0 \\ 0 & e^{i\theta} \end{pmatrix} \tag{3.22}$$

With the goal of determining the S-parameters of the input and output blocks, the inputs to this calculation are the theoretic values for the calibration standards and the measured values for these standards cascaded with the input and output blocks. The notation for these will be A and B for the input and output blocks, respectively, and ML for the measured line and MT for the measured thru. Therefore,

$$T_{MT} = T_A T_{THRU} T_B = T_A\, T_B \tag{3.23}$$

since the thru T-matrix is the identity matrix. Likewise the line equation can be represented by

$$T_{ML} = T_A T_{LINE} T_B \tag{3.24}$$

Solving for the output block transfer matrix using (3.23), we get

$$T_B = T_A{}^{-1} T_{MT} \tag{3.25}$$

If we substitute for T_B in (3.24), we derive the following equation:

$$T_{ML} = T_A T_{LINE} T_A{}^{-1} T_{MT} \tag{3.26}$$

which can be written as

$$T_{ML} T_{MT}{}^{-1} = T_A T_{LINE} T_A{}^{-1} \tag{3.27}$$

and

$$T_{ML} T_{MT}{}^{-1} T_A = T_A T_{LINE} \tag{3.28}$$

We use the following notation for the product of the measured line matrix and the inverse of the measured thru:

$$T_{ML} T_{MT}{}^{-1} = T_{LT} \tag{3.29}$$

This substitution in (3.28) gives

$$T_{LT}\, T_A = T_A\, T_{LINE} \tag{3.30}$$

which can be written as

$$\begin{pmatrix} T_{LT11} & T_{LT12} \\ T_{LT21} & T_{LT22} \end{pmatrix} \begin{pmatrix} T_{A11} & T_{A12} \\ T_{A21} & T_{A22} \end{pmatrix} = \begin{pmatrix} T_{A11} & T_{A12} \\ T_{A21} & T_{A22} \end{pmatrix} \begin{pmatrix} e^{-i\theta} & 0 \\ 0 & e^{i\theta} \end{pmatrix} \tag{3.31}$$

or written in equation form as

$$T_{LT11}\, T_{A11} + T_{LT12}\, T_{A12} = T_{A11}\, e^{-i\theta} \tag{3.32a}$$

$$T_{LT21}\, T_{A11} + T_{LT22}\, T_{A21} = T_{A21}\, e^{-i\theta} \tag{3.32b}$$

$$T_{LT11}\, T_{A12} + T_{LT12}\, T_{A22} = T_{A12}\, e^{i\theta} \tag{3.32c}$$

$$T_{LT21}\,T_{A12} + T_{LT22}\,T_{A22} = T_{A22}\,e^{i\theta} \tag{3.41d}$$

(3.32a) divided (3.32b) can be written as

$$T_{LT21}\left(\frac{T_{A11}}{T_{A21}}\right)^2 + (T_{LT22} - T_{LT11})\frac{T_{A11}}{T_{A21}} - T_{LT12} = 0 \tag{3.33a}$$

(3.32c) divided by (3.32d) can be written as

$$T_{LT21}\left(\frac{T_{A12}}{T_{A22}}\right)^2 + (T_{LT22} - T_{LT11})\frac{T_{A12}}{T_{A22}} - T_{LT12} = 0 \tag{3.33b}$$

Upon inspection, we see that the coefficients are the same; however, we know that the two variable terms are uniquely defined. Quadratic equations have two solutions. From these facts, we can determine that one of the answers is $\frac{T_{A12}}{T_{A22}}$ and the other is $\frac{T_{A11}}{T_{A21}}$.

From (3.19), we know by definition

$$S_{a11} = \frac{T_{A12}}{T_{A22}} \tag{3.34}$$

Likewise, substitution allows us to determine that

$$\frac{T_{A11}}{T_{A21}} = S_{A11} - \frac{S_{A21}S_{A12}}{S_{A22}} \tag{3.35}$$

We expect that our blocks will be designed primarily to facilitate transmission of power to the DUT. From this, it follows that S_{A11} will be much smaller than S_{A12} and S_{A21}. Using this principle, we can consistently assign the smaller magnitude quadratic root of (3.33a-b) to be the S_{A11} term while the larger magnitude quadratic root is shown in (3.35).

Therefore, the difference of the roots can be written as

$$\frac{T_{A12}}{T_{A22}} - \frac{T_{A11}}{T_{A21}} = S_{A11} - \left(S_{A11} - \frac{S_{A21}S_{A12}}{S_{A22}}\right) = \frac{S_{A21}S_{A12}}{S_{A22}} \tag{3.36}$$

A similar derivation can be used to isolate the parameters of the output block.

To begin, we start with (3.32) and (3.33), and isolate T_B instead of T_A:

$$T_A = T_{MT} {T_B}^{-1} \tag{3.37}$$

Substituting into (3.33), we get

$$T_{ML} = T_{MT} {T_B}^{-1} T_{LINE} T_B \tag{3.38}$$

and

$${T_{MT}}^{-1} T_{ML} = {T_B}^{-1} T_{LINE} T_B \tag{3.39}$$

Replacing the left hand side with the definition of

$${T_{MT}}^{-1} T_{ML} = T_{TL} \tag{3.40}$$

$$T_{TL} = {T_B}^{-1} T_{LINE} T_B \tag{3.41}$$

or

$$T_B T_{TL} = T_{LINE} T_B \tag{3.42}$$

in matrix form, produces the following:

$$\begin{pmatrix} T_{B11} & T_{B12} \\ T_{B21} & T_{B22} \end{pmatrix} \begin{pmatrix} T_{TL11} & T_{TL12} \\ T_{TL21} & T_{TL22} \end{pmatrix} = \begin{pmatrix} e^{-i\theta} & 0 \\ 0 & e^{i\theta} \end{pmatrix} \begin{pmatrix} T_{B11} & T_{B12} \\ T_{B21} & T_{B22} \end{pmatrix} \tag{3.43}$$

Expanding into equations, we get

$$T_{TL11}\, T_{B11} + T_{TL21}\, T_{B12} = T_{B11}\, e^{-i\theta} \tag{3.44a}$$

$$T_{TL12}\, T_{B11} + T_{TL22}\, T_{B12} = T_{B12}\, e^{-i\theta} \tag{3.44b}$$

$$T_{TL11}\,T_{B21} + T_{TL21}\,T_{B22} = T_{B21}\,e^{i\theta} \tag{3.44c}$$

$$T_{TL12}\,T_{B21} + T_{TL22}\,T_{B22} = T_{B22}\,e^{i\theta} \tag{3.44d}$$

Putting these into quadratic form yields the equations below:

$$T_{TL12}\left(\frac{T_{B11}}{T_{B12}}\right)^2 + (T_{TL22} - T_{TL11})\frac{T_{B11}}{T_{B12}} - T_{TL21} = 0 \tag{3.45a}$$

$$T_{TL12}\left(\frac{T_{B21}}{T_{B22}}\right)^2 + (T_{TL22} - T_{TL11})\frac{T_{B21}}{T_{B22}} - T_{TL21} = 0 \tag{3.45b}$$

Solving we get

$$S_{B22} = -\frac{T_{B21}}{T_{B22}}, \tag{3.46}$$

which is the root that should have the smaller magnitude. The root with the larger magnitude is

$$\frac{T_{B11}}{T_{B12}} = -S_{B22} + \frac{S_{B21}\,S_{B12}}{S_{B11}} \tag{3.47}$$

The difference between the two is

$$\frac{T_{B11}}{T_{B12}} - \frac{T_{B21}}{T_{B22}} = -S_{B22} + \frac{S_{B21}\,S_{B12}}{S_{B11}} + S_{B22} = \frac{S_{B21}\,S_{B12}}{S_{B11}} \tag{3.48}$$

Now, we use this information along with the measured values for the reflections to determine the rest of the S-parameters. A well-known one-port reflection equation is shown below:

$$\Gamma_{MA} = S_{A11} + \frac{S_{A21}\,S_{A12}\,\Gamma_R}{1 - S_{A22}} \tag{3.49}$$

The left side of the equation is the measured value of port one when the probes are on the reflection standard. Gamma R is the nominal reflection coefficient. In this technique, the reflection coefficient is not assumed to be known, but rather is isolated and eliminated. As a check, when the S-parameters are known, the predicted value for the reflection coefficient can be inserted into the equation to verify that each side balances.

If we solve for the reflection coefficient and substitute for the known values already determined, we get

$$\Gamma_R = \frac{1}{S_{A22}} \frac{\frac{T_{A12}}{T_{A22}} - \Gamma_{MA}}{\frac{T_{A11}}{T_{A21}} - \Gamma_{MA}} \tag{3.50}$$

The same is applied to the port two equations:

$$\Gamma_{MB} = S_{B22} + \frac{S_{B21}\, S_{B12}\, \Gamma_R}{1 - S_{B11}}, \tag{3.51}$$

which can be turned into

$$\Gamma_R = \frac{1}{S_{B11}} \frac{S_{B22} + \Gamma_{MA}}{\frac{T_{B11}}{T_{A21}} + \Gamma_{MA}} \tag{3.52}$$

Setting (3.59) and (3.61) equal to each other, we get

$$S_{A22} = S_{B11} \frac{S_{A11} - \Gamma_{MA}}{\frac{T_{A11}}{T_{A21}} - \Gamma_{MA}} \frac{\frac{T_{B11}}{T_{A21}} + \Gamma_{MA}}{S_{B22} + \Gamma_{MA}} \tag{3.53}$$

All of these values are known, except for S_{A22} and S_{B11}. We can use our measurement for the reflection on the thru measurement to get another equation relating S_{A22} and S_{B11}:

$$S_{A22} = \frac{1}{S_{B11}} \frac{S_{A11} - \Gamma_{MAT}}{\frac{T_{A11}}{T_{A21}} - \Gamma_{MAT}} \tag{3.54}$$

where Γ_{MAT} is defined as

$$\Gamma_{MAT} = S_{THRU11} \tag{3.55}$$

Multiplying (3.62) with (3.62), we get.

$$S_{A22} = \frac{S_{A11} - \Gamma_{MA}}{\frac{T_{A11}}{T_{A21}} - \Gamma_{MA}} \frac{\frac{T_{B11}}{T_{A21}} + \Gamma_{MA}}{S_{B22} + \Gamma_{MA}} \frac{S_{A11} - \Gamma_{MAT}}{\frac{T_{A11}}{T_{A21}} - \Gamma_{MAT}} \tag{3.56}$$

The sign of S_{A22} can be determined by inserting determined values into (3.49) and ensuring that the equation balances when the reflection coefficient is the predicted value.

With S_{A22} known, we can determine S_{A11} from (3.54). Using S_{A22} and S_{B11} with our previously known data, the remaining unknown S-parameters can be extracted from (3.36) and (3.48) when written as shown below. It is impossible to mathematically isolate the transfer terms (S_{12} and S_{21}).

$$S_{A12}S_{A21} = \left(S_{A11} - \frac{T_{A11}}{T_{A21}}\right) S_{A22} \tag{3.57a}$$

$$S_{B12}S_{B21} = \left(\frac{T_{B11}}{T_{B12}} - S_{B22}\right) S_{B11} \tag{3.57b}$$

With the four S-parameters of the input and output blocks, we can calculate T-matrices that can be de-embedded from our measurements to determine performance of the DUT.

3.4 Power RF Measurements

Under specific bias conditions and for small signal input power, the HEMTs behave as linear devices; however, power amplifiers achieve their greatest efficiency when they are biased well into compression. Most network analyzers are not designed to

provide the input power required to measure the output power produced by the DUTs in this research. The Agilent E8364A PNA was used to make the S-parameter measurements necessary to calibrate the system and measure the DUT. This instrument has a nominal maximum output power of 0 dBm at 30 GHz and a maximum test port input power damage level of 30 dBm [32]. A typical input power for a DUT used in this experiment is 24.5 dBm with a corresponding output power of 32 dBm or greater for the device operated at peak power-added efficiency (PAE). From these numbers, it is clear that the network analyzer is an inadequate power supply and measurement tool for the devices in question. However, the network analyzer is incapable of presenting an arbitrary load and source impedance to the DUT. Thus, a separate measurement system power RF measurements was implemented. The configuration for ALERTS during the power RF measurements is shown in Figure 3.13.

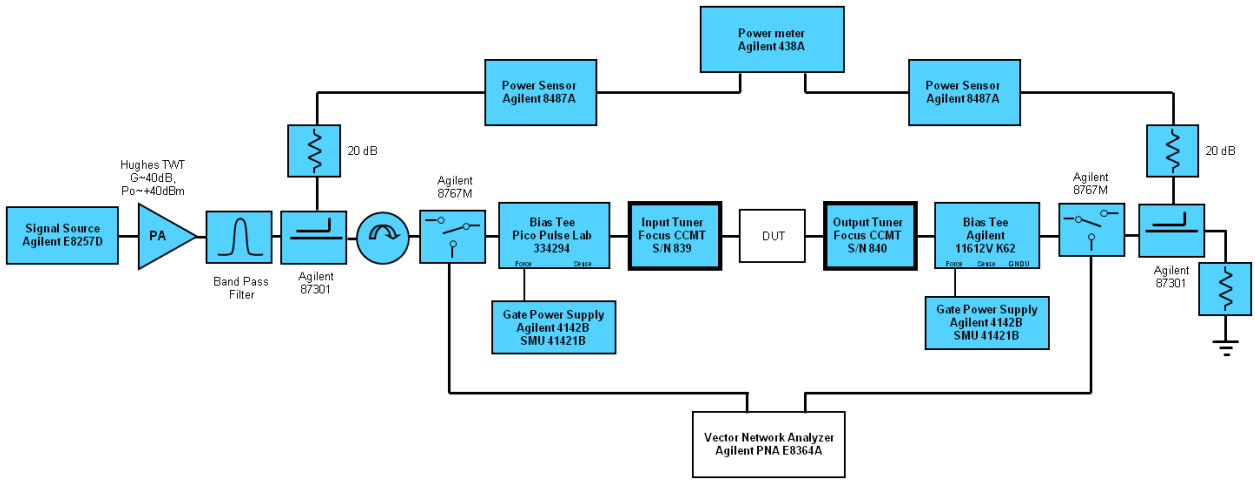


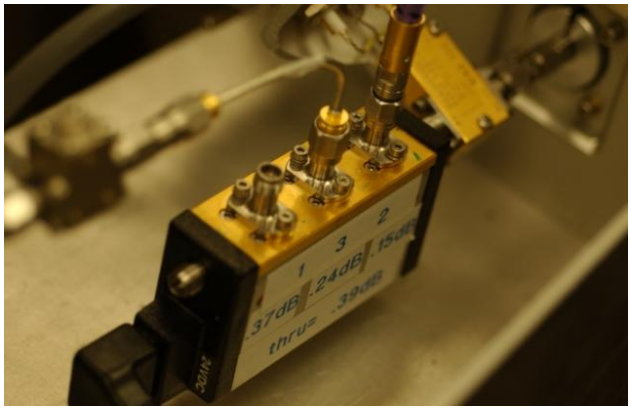
Figure 3.13. Components in the reliability system used during large signal power RF measurements.

The system is controlled from a computer running a MATLAB script that commands the instruments and records the data. The RF energy is produced by an Agilent E8257D Analog Signal Generator. This instrument controls the power level and frequency of the RF power. A Hughes 8010H12F000 TWT Microwave Amplifier is used to amplify the

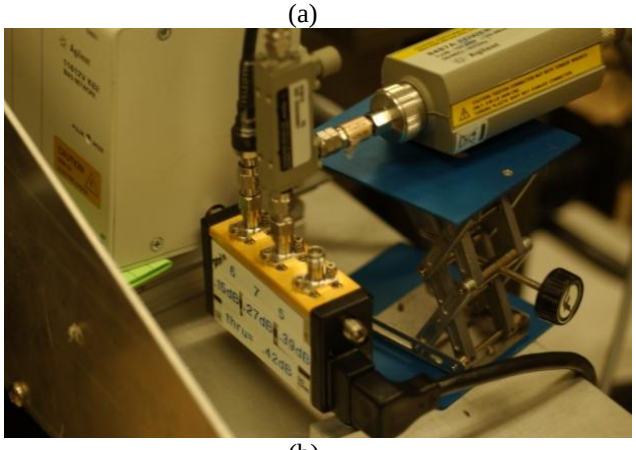
output of the signal source to the power level required to drive the DUT. The rated output power level of the TWT is 10 W, which is accurate to within 3 dB. The input and output of the TWT are WR-28 rectangular microwave fixtures. The rest of the system uses 2.4-mm coax. An HP R281A 2.4 mm to WR-28 waveguide adapter was used to connect the WR-28 to the coax. The TWT has a rated gain of 30 dB from 26.5 to 40 GHz. For measuring devices at lower frequency, several different solid-state amplifiers were built to provide the RF amplification. When the TWT was used, noise limited the dynamic range of the amplifier. To mitigate the effect of the noise, a Reactel 7W8-31.25G-882X band-pass filter was used. The filter was able to extend the dynamic range of the system by 12 dB.

After the filter, an Agilent 87301E dB directional coupler is used to split the RF power. The coupled port is fed to an Agilent 8487A Power Sensor that is monitored by an Agilent 438A Power Meter. The thru port of the directional coupler feeds into an isolator, which protects the power meter and TWT from reflections and presents a stable impedance to the tuner. The isolator connects to the switching system. During RF power measurement, the switch to the RF path is closed and the switch to the network analyzer is open. The distance from the input switch to the DUT and from the DUT to the output switch the RF path is the same as it is during S-parameter measurements, with the exception that the source and load tuners will present a desired impedance to the DUT. The input on the output coupler is connected to the RF switch. The coupled port feeds into an attenuator, which brings the power down to a level that the output power meter can read. Unlike the input coupler, the output coupler is not used to split the RF path. Its function in the system is merely to attenuate the power, and the thru path of the output

coupler is terminated in a 50-Ohm load that is rated to absorb the types of power levels that the DUT can provide. The input RF switch assembly is shown in Figure 3.14(a). The isolator and a semi-rigid coax cable can be seen connecting the high-power RF path to the connector labeled "3." The network analyzer is connected to the switch port labeled "2." Between the RF switch and the tuner is a low loss bias T. Figure 3.14(b) shows the output switch assembly. The bias T connects directly with the switch input. The first output port, labeled "6" in the photograph, is connected to the VNA. The RF path output (port "7") connects directly with the coupler. The coupled port can be seen connecting to the attenuator and the power sensor.



(a)



(b)

Figure 3.14. Input (a) and output (b) switch assembly for the reliability system.

3.4.1 Power Measurements

Section 3.3 described the anatomy of the RF power system, this section covers the physiology. In order to determine the high-power RF performance of a DUT, it is necessary to know the power incident on the input or gate of the DUT and the output power of the DUT. It is not possible to directly measure the RF power going into the gate. Likewise, there is significant attenuation between the output of the DUT and the output power sensor. To measure the input power on the DUT, is necessary to measure the RF power at a point on the input path and establish a correlation between that power level and the power at the DUT. To measure the output power of the DUT, the losses between the probe tips and the power sensor must be known. These tasks are complicated by the automatic tuners whose losses and reflections will change with each change in impedance

The procedure for calibrating the RF power measurement system consists of the following steps:

1. Calibrating the two-port network.

2. Calibrating the tuner.

3. Measuring the input coupled port S-parameter.

4. Measuring the input thru port S-parameter.

5. Measuring the output path S-parameter.

The process begins with performing a two-port network calibration; the TRL calibration described previously is one type of two-port network calibration.

Calibrating the tuners is more complicated. Prior to describing what the Focus Microwaves software does during tuner calibration, the theory behind the tuner operation is presented. The purpose of the tuners is to present an arbitrary impedance at the input and output port of the DUT. This is accomplished by inserting a probe into a slotted coaxial air line. A cartoon representation of the tuner is shown in Figure 3.15(a).

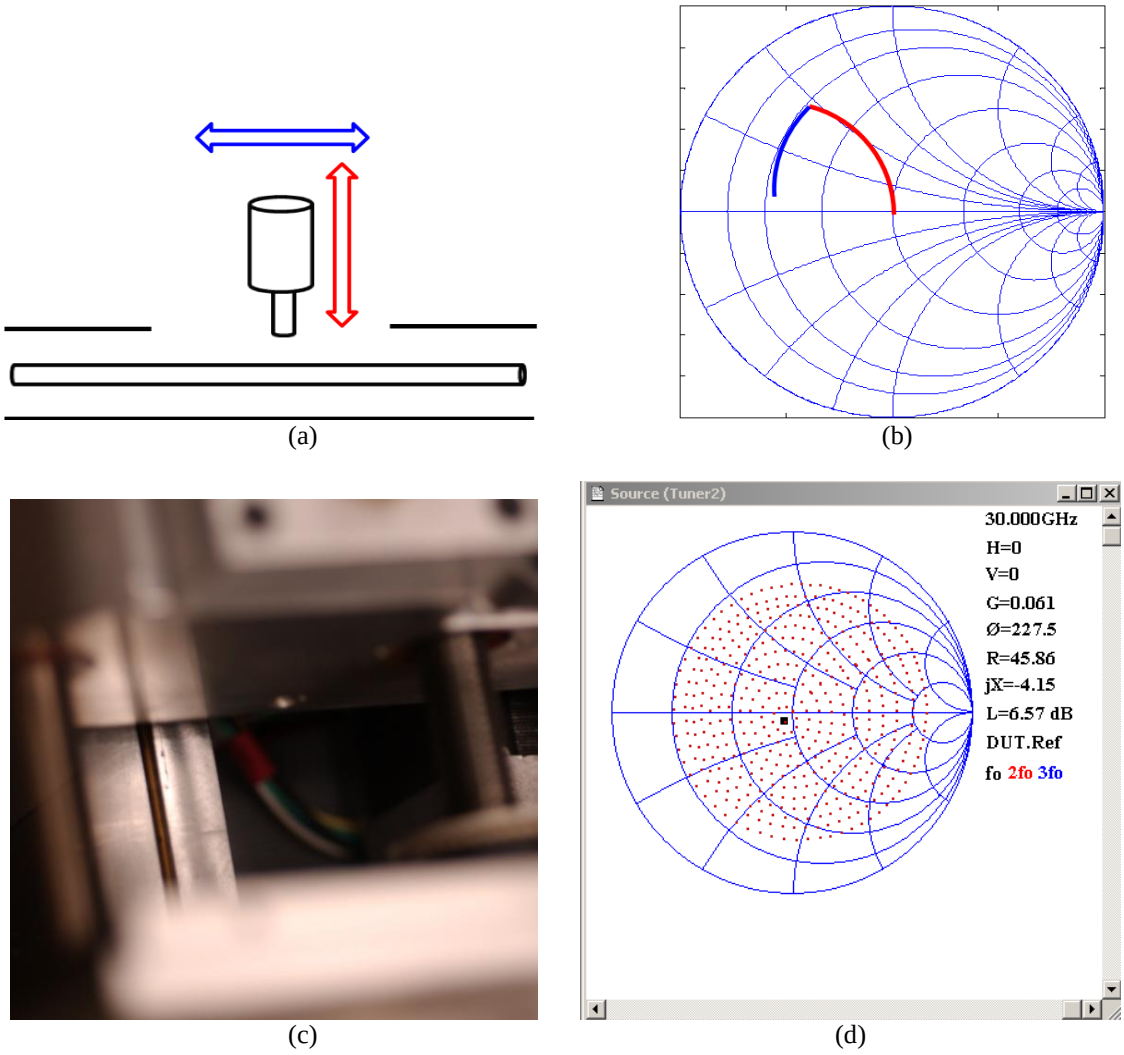


Figure 3.15. (a) Cross section of tuner, (b) a graphical representation of tuner location on the smith chart, (c) the tuner, and (d) a screen capture of the Focus Microwaves software used to calibrate the tuner.

As the probe is inserting into the air line, the reflection coefficient of the perturbation increases. As the probe slides along the air line, the phase of the reflection coefficient

changes. By making use of these two degrees of freedom, it is possible to produce the desired arbitrary impedance. The effects of the probe location is demonstrated in Figure 3.15(b) and shows the effect on impedance of moving a probe toward and away from the inner coax is shown along the red arc and the effect on impedance of moving a probe along the length of the coax is shown on the blue arc. A photograph of the tuner with the lid removed is shown in Figure 3.15(c). The open slotted coax airline can be seen in the photograph. The tuner S-parameter block in the initialized position is determined during the TRL calibration; however, the impedance and losses of the tuner need to be determined over a large range of impedances to perform load pull or source pull measurements. By keeping one tuner in the initialized state, the second tuner can be measured in an arbitrary position. When the S-parameter block of the initialized tuner is de-embed from the combined S-parameter measurement, the S-parameters of the tuner in the non-initialized state can be determined and recorded. The procedure is repeated for a large number of points until the desired section of the Smith chart has been characterized. A screen capture of the Focus Microwaves software used to calibrate the tuner is shown in Figure 3.15(d).

When the tuners are fully calibrated, there are two additional measurements needed to determine the power incident on the DUT. The first of these measurements is the S-parameter block between the input port of the coupler and the input power sensor. This S-parameter matrix is called $S_{IN\ COUP}$. The S-parameters between the input port on the coupler and the port on the RF switch used to calibrate the tuners are measured. This S-parameter block is called $S_{IN\ THRU}$. $S_{IN\ THRU}$ is cascaded with the measured S-parameter block of the tuner in its tuned position.

The output S-parameter block between the RF switch and the power sensor is also measured. These S-parameters are called $S_{OUT\ THRU}$. This block is cascaded with the S-parameters measured from the output tuner in the tuned position. When the measurements are completed, the system is assembled. The power sensors are measured. The equation for the input power at the DUT is given in (3.58):

$$P_{IN\ DUT} = P_{IN\ SENSOR} - L_{IN\ THRU} + L_{IN\ COUP} \tag{3.58}$$

where $P_{IN\ DUT}$ is the input power at the DUT in dBm; $P_{IN\ SENSOR}$ is the power measured at the input power sensor in dBm; $L_{IN\ THRU}$ is the transmission loss in dB of the combination of $S_{IN\ THRU}$ and the S-parameters of the tuner in the tuned position; and $L_{IN\ COUP}$ is the loss in dB of $S_{IN\ COUP}$. The equation for the power at the output of the DUT is given in (3.59):

$$P_{OUT\ DUT} = P_{OUT\ SENSOR} + L_{OUT\ THRU} \tag{3.59}$$

where $P_{OUT\ DUT}$ is the output power at the DUT in dBm; $P_{OUT\ SENSOR}$ is the power measured at the output power sensor in dBm; and $L_{OUT\ THRU}$ is the transmission loss in dB of the combination of $S_{OUT\ THRU}$ and the S-parameters of the tuner in the tuned position.

The gain of the DUT in dB is simply the difference in dB between the output power and input power at the DUT:

$$G_{DUT} = P_{OUT\ DUT} - P_{IN\ DUT} \tag{3.60}$$

3.4.2 Calibration and Verification of Automated Tuners

When working on components at the frequencies of interest to this research with standard VNAs and RF power equipment, one must have an understanding of the calibration and verification process in order to be aware of the factors that would lead to

erroneous measurements. At the higher frequencies the system becomes increasingly sensitive to mechanical deformation. Often measurements that appear valid could, in fact, be inaccurate. When representing this data, an engineer must be able to speak intelligently about the calibration, verification, and measurement process to establish confidence in the results of the measurement. A calibration and verification procedure was developed at ARL to certify the measurements in support of the research presented in this dissertation and the Wide Band-gap Semi-Conductor Technology Initiative (WBSCTI).

The method of verifying our calibration involves measuring the gain of our system with the probes landed on a thru line while the tuners are swept through a load pull and a source pull. The measured gain at every point is compared to the calculated gain.

The transducer gain of an arbitrary DUT can be written as

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{3.61}$$

where G_T is the transducer gain; Γ_S is the source reflection coefficient as seen from the reference plane of the DUT; Γ_L is the load reflection coefficient as seen from the reference plane of the DUT; and the S-parameter notation refers to the S-parameters of the DUT. The term Γ_{IN} is the input reflection coefficient of the DUT:

$$\Gamma_{IN} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1-S_{22}\Gamma_L} \tag{3.62}$$

During the verification procedures, the DUT is a thru. The S-parameters for a thru, as previously mentioned, are

$$S_{THRU} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{3.63}$$

Filling these values into (3.71), this equation simplifies to

$$\Gamma_{IN} = \Gamma_L \tag{3.64}$$

and (3.70) simplifies to

$$G_T = \frac{(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_L\Gamma_S|^2} \tag{3.65}$$

This is the equation we use when discussing our load pull verification.

Tuner calibration is controlled by the Focus Microwaves software. The tuners sweep through a range of reflection coefficients by inserting a metal probe into an air line and moving the probe different distances from the DUT. At each position of the tuner, the S-parameters of that block are measured. This is accomplished through a simple de-embedding calculation. The tuner not being measured is moved to its initialization configuration. This configuration corresponds to the S-parameter block measured in the TRL calibration. With the opposite block in a well-known state, the S-parameters of each tuner configuration can be calculated by measuring the total S-parameters in each configuration and de-embedding the known values.

In order to verify the calibration of the tuners, a load/source pull measurement is performed by the system while the probes are in contact with a thru calibration standard. The purpose of the load/source pull measurement is to accomplish two tasks: determine the error correction factors and verify the tuner calibration by establishing a figure of merit for the load/source pull sweep. The procedure for the load/source pull verification

is very similar to that of the tuner calibration. The difference is that the turners are calibrated using the VNA and are verified using the power meters. The power measurement system is assembled into its operational configuration during verification. The tuners are moved into their initialization position. A load pull or source pull is performed with the opposite tuner in the initialized position. The data are recorded into a file. The predicted transducer gain is calculated for each tuner position and is compared to the measured data by a computer program. The difference between the calculated and measured transducer gain is called delta GT and serves as our metric for the validity of the calibration. The mean of the delta GT values is used to determine the error correction factors for the system. The variance of the delta GTs is used as verification for the system and the error correction factors. With the corrections applied, the mean delta GT of each tuner must be less than a tenth of a dB for the verification to be valid. Typical values range from 0.05 to 0.09 dB. The variance of the delta GT is the metric for the verification of each tuner. The variance must be less than 0.15 dB. Typical values range from 0.08 to 0.12 dB.

The theory behind S-parameters requires that the system be linear. Unfortunately, the universe is highly nonlinear. There is a finite range over which the tuners will perform in a linear manner. The source of the nonlinearity is suspected to cause thermal heating as the resistive losses exceed the system's ability to dissipate power thermal expansion is thought to mechanically deform tuning components. Nonlinear effects become more pronounced at higher gammas when the tuning probe is greatly perturbing the air waveguide.

The validity of a tuner point for measuring power sweeps can be determined by examining the range over which the power sweep at that point is linear. The tuner condition for this verification has one tuner in the configuration to be tested while the other is in the initial position. A power sweep is performed in this configuration. The criterion for success is that over the range to be measured, the peak-to-peak value is less than 0.2 dB and at high power the delta GT is less than 0.2 dB. These values are usually very easy to attain, and results are usually well within tolerances. This measurement can be used to determine the range over which a power sweep is valid in addition to determining the validity of the measurement itself.

3.4.3 Efficiency Measurements

In addition to DC measurements, output power, and gain, there are hybrid measurements that incorporate RF and DC measurements. These include efficiency measurements. Maximum output power determines the communication range of a wireless system, but efficiency is also of key concern to system designers for a number of reasons, including battery life and the requirements of a system to dissipate heat.

There are types of efficiency typically reported in the literature: Power Added Efficiency (PAE) and Collector Efficiency or Drain Efficiency (CE/DE). The term Collector Efficiency was originally applied to bipolar junction transistors. Drain Efficiency is a more appropriate term for Field Effect Devices, but Collector Efficiency is often used interchangeably. Drain Efficiency is a measure of the transistors ability to transduce DC power into RF power. The equation for DE is given in (3.66) [33]:

$$\mathrm{DE} = \frac{P_{OUT}}{I_{DS} \times V_{DS}} \tag{3.66}$$

where P_{OUT} is the output RF power in watts, I_{DS} is the drain source current in amps, and V_{DS} is the drain source voltage in volts.

PAE is a ratio of the difference between the output power and the input power divided by the DC power. The equation is given in (3.67) [34]:

$$\text{PAE} = \frac{P_{OUT} - P_{IN}}{I_{DS} \times V_{DS}} \tag{3.67}$$

P_{IN} is the input RF power in watts.

Of the two efficiencies, PAE is often of more interest because it also factors in the amount of power required to drive the device.

Chapter 4: Operation of the Lifetime Extended Reliability Test Station

When the system is fully calibrated, a series of measurements are combined in a process designed to periodically produce equivalent circuit models of the DUT while that device is being operated under conditions that will stress the device. As the device is stressed in a manner that replicates the type of operation that it will likely be exposed to during commercial operation, its performance will change. These changes can be quantified in device models and used to diagnose the physical mechanisms of the changes. The procedures involved in the setup and operation of the test system are discussed in this chapter. This chapter also focuses on the functioning of the device during operation.

4.1 Setup and Test Procedures

Prior to the initiation of the automated test procedure, one must calibrate the system and determine the operating conditions. The calibration was described in chapter 3. The device in this study is operated in Class AB mode, which provides a good combination of gain and efficiency. Other than output power, these are the two of the most important characteristics of a power amplifier.

The bias on the device is set by pinching off the gate to –7 V. The drain voltage was positively biased to 20 V, and the gate voltage was adjusted in a positive direction toward zero until the drain current reached 100 mA, which was between 20% and 25% of the drain saturation current. The drains saturation current is, by definition, the current

through the drain with the gate set to 0 V. For our 500-µm GaN HEMTs, this was about 500 mA or 1 A per millimeter.

Once the device was properly biased, the S-parameters of the device are measured and recorded. This measurement is performed for two reasons: the measurement will reveal if the there is an error in the S-parameter calculations or if the device is defective. After the S-parameter measurement, the RF switch is switched to the power measurement configuration. The next step in the process of setting up the reliability system is to find the optimal match for the input and output tuner. From experience, an approximate match for each port is known. The input and output port of the devices are set to their nominal impedances. The input power is set at a level that is in the linear range of the devices operation, a value well below compression. The Focus Microwaves software is used to perform an optimization search for the optimal input match, which is the input impedance at which the device's gain is maximized. Once the optimal input impedance that maximizes gain is applied to the input, the power to the DUT is increased to the point that would drive the device several decibels into compression. The input power is held constant while a peak search is performed on the output to find the optimal power match, which is the impedance at which the maximum power is transferred from the device to the output port. The input gain peak search is repeated on the input port to see if the optimal gain match has changed when the output impedance changed. Combining an optimal gain match on the input and an optimal power match on the output is an effective way to find a good approximation of an optimal efficiency match.

The RF power is applied to the biased DUT with the previously determined impedances set on the tuners. The device is measured to ensure that it is functioning

properly, and the extended reliability MATLAB script is initiated. This program will continue to run until it is terminated by the operator. During this research, it was allowed to run for several days or until the device failed. A flowchart showing the steps of the process is shown in Figure 4.1. The program operates in two separate modes: a performance stress mode and a device characterization mode. For the majority of the time, the device is being stressed by operating it as a high-power and high-frequency amplifier with a high voltage across the drain and sufficient RF power to drive it several dB into compression. After the specified interval has elapsed, the performance of the DUT is measured and recorded. For most of the measurements used in this research, the measurement interval during device stress was five minutes. The second key time interval in the experiment is the interval between device characterization measurements. At different phases of the research, this has been between four and six hours. When this time has passed, the device initiates a series of tests that when combined together are selected to provide an overview of the device's physical state. The operator can choose to include or omit any of the tests during the setup prior to the initiation of the measurement process.

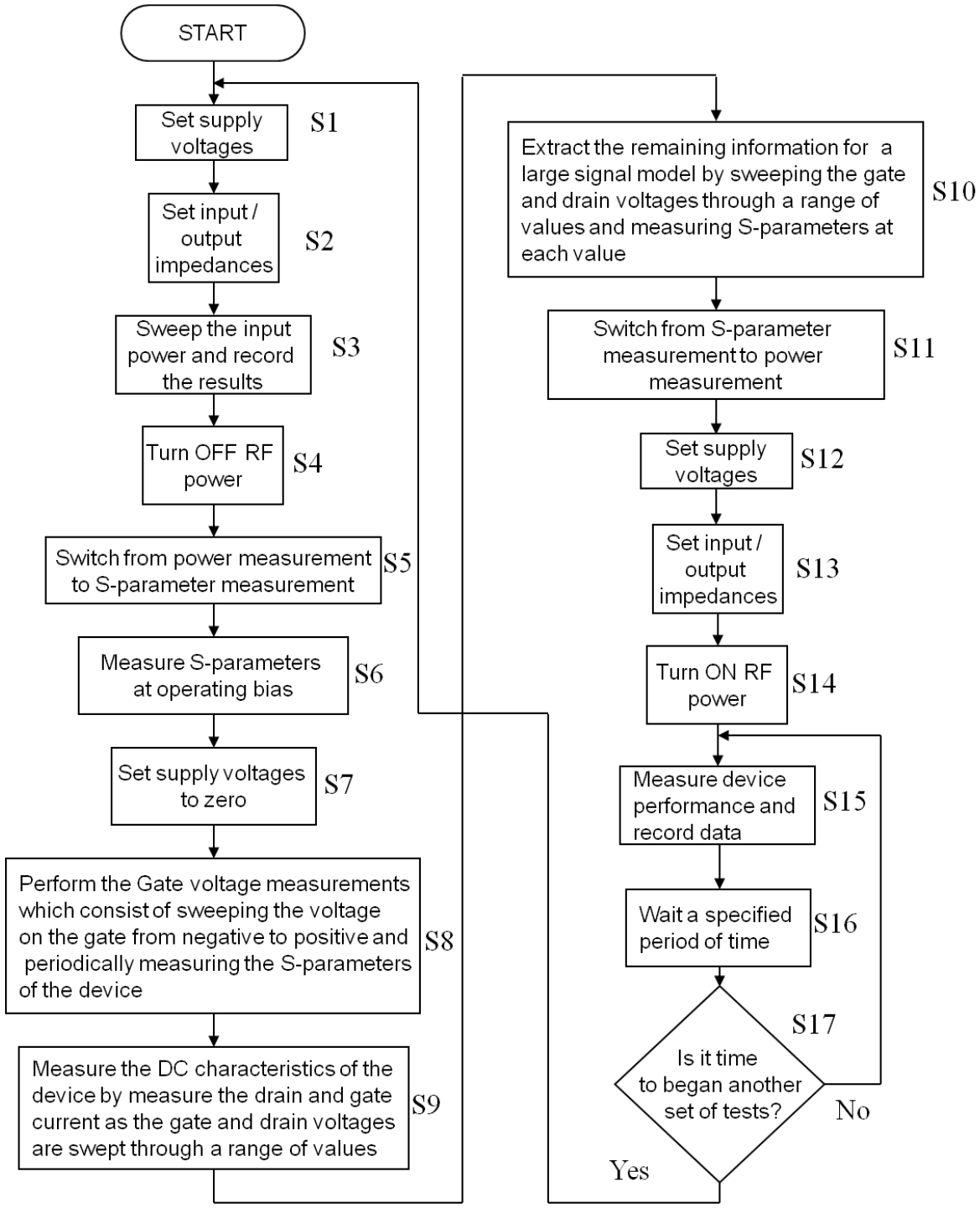


Figure 4.1. Flow chart of the operation of the Extended Reliability Test Station.

In figure 4.1, each step is numbered sequentially from S1 to S18. When the program is started, it launches the device characterization tests.

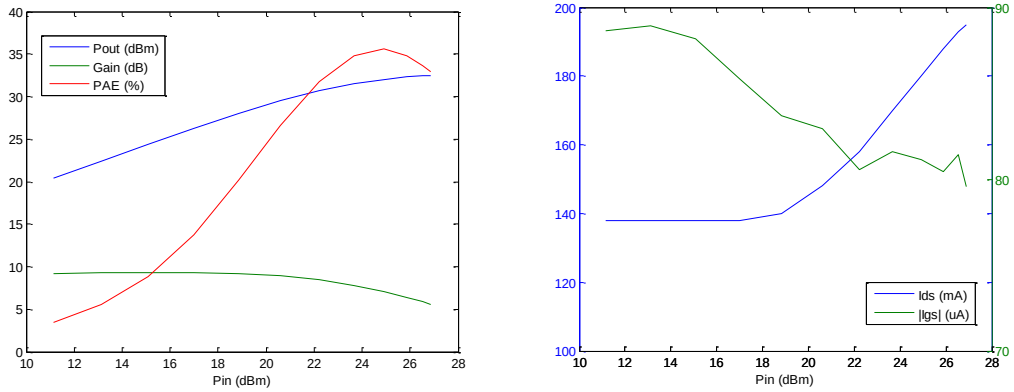
4.2 Periodic Device Characterization

The device characterization begins by ensuring that the system is in the proper configuration to perform the power measurement. The first step (S1) sets the voltage: the gate voltage is set first, followed by the drain voltage. During normal operation, gate and drain will always be at the proper voltage when this step begins. If this is the case, no change is made. The software then commands the tuners to apply the proper impedances to the DUT (S2). Again, the tuners should already be in this state and this step is merely included to correct for changes that have occurred.

4.2.1 Power Sweep

After the system has commanded the tuners and power supply to be in the proper configuration and has confirmed that they are correct, the input RF power is swept from the linear region of operation into compression (step S3). Appendix B4 includes a data set of a power sweep. Other data files from measurements are also recorded in Appendix B. While the power is swept, the computer records the values for input power (Pin), output power (Pout), gain (G), gate current (Igs), gate voltage (Vgs), drain current (Ids), drain voltage (Vds), drain efficiency (DE), power added efficiency (PAE), and source power. The source power is the RF power in dBm provided by the signal source. Source power does not provide information on the DUT, but it can be used to determine if the behavior of the system is anomalous. Likewise, the gate voltage and drain voltage are set and should remain constant as the power is swept. If the bias voltages change, it usually indicates that the power supply has reached its current limit. The usual cause of this is a failed DUT. Figure 4.2(a) shows the Pout, gain, and PAE of a representative 500 μm

GaN HEMT as it is driven into compression. The drain current and gate current of the device are shown in Figure 4.2(b).



(a) (b)

Figure 4.2. Device performance during input power sweep, showing a (a) plot of output power, gain, and PAE; and (b) plot of drain current and gate current.

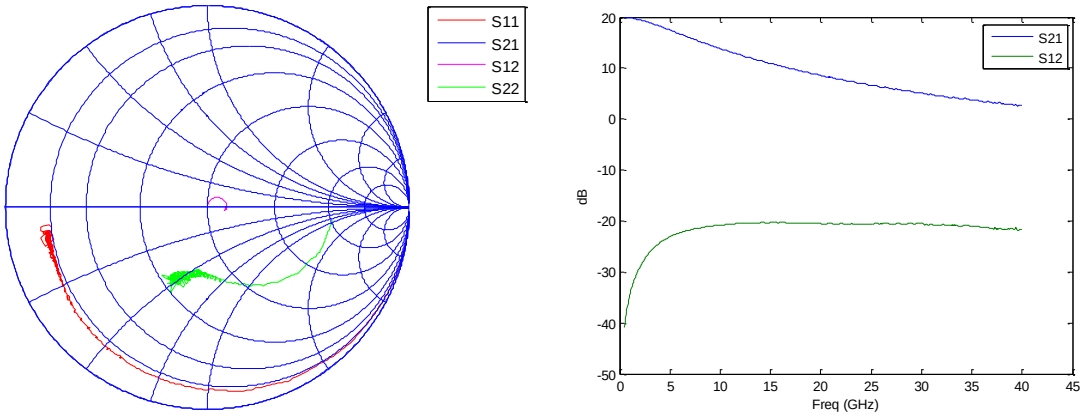
As the device is driven further into compression, the gain continues to decrease. At some point the decline in gain reaches a point that PAE begins to decrease. Peak PAE is a useful metric in characterizing a transistors ability to function as a power amplifier. We can also see that as the input RF power increases, the drain current also increases. This is caused by self rectification across the gate and has the effect of driving the device from Class AB operation toward more of a Class A operation, which increases the gain. This phenomenon has been observed in FETs and bipolar devices [35].

4.2.2 S-parameter Measurement at Bias

When the power sweep is completed, the power is turned down to a value below the minimum power used during the sweep. Then, the power is turned off (S4). In order to switch over to RF measurement (S5), the tuners must be set to their initialized state for the S-parameter calibration to be valid. After the tuners are initialize, the RF switch

switches from power measurement to RF measurement. The DUT is still at the same bias conditions that it was at during operation.

The computer controller commands the network analyzer to measure the S-parameters of the DUT in S6. Figure 4.3 shows the results of one of these S-parameter measurements.



(a) (b)

Figure 4.3. S-parameters of a 500-µm GaN HEMT at 20 V DC with a drain current of 100 mA (a) Smith Chart plot and (b) logarithmic plot of S21 and S12.

The S-parameters are plotted on the Smith Chart in Figure 4.3(a). S_{21} has a magnitude that is too large for it to appear on the Smith Chart from 500 MHz to 40 GHz. A plot in dB of S_{21} and S_{12} is shown in Figure 4.3(b).

4.2.3 Gate Measurements

The S-parameters are the last measurements made during the characterization process under the bias conditions used during operation. The gate is pinched off by applying a strong negative voltage that reduces the drain current to leakage levels. With the gate pinched off, the drain voltage is reduced to 0 V. Then, the gate voltage is reduced to zero. This process completes device turn off in S7. While biasing the device, it is

important to do so gradually in order to avoid high voltage transient peaks forming on the transmission line. This process does not need to take a great deal of time. Adjusting 20 V over a period of one or two seconds is sufficient to suppress transients of sufficient magnitude to damage the DUT.

The next step in the characterization process is the gate characterization measurements (S8). With the drain voltage set to zero during the entire measurement, the gate is set to a large negative voltage. This voltage can be set by the operator when the program is initiated. A typical value for the beginning gate voltage used during this experiment for the gate measurements was -7 V. The voltage is applied and the S-parameters of the device are measured.

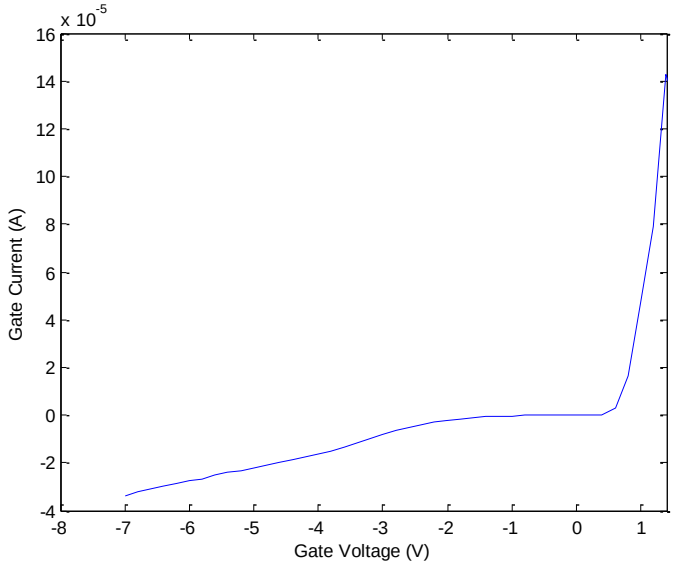
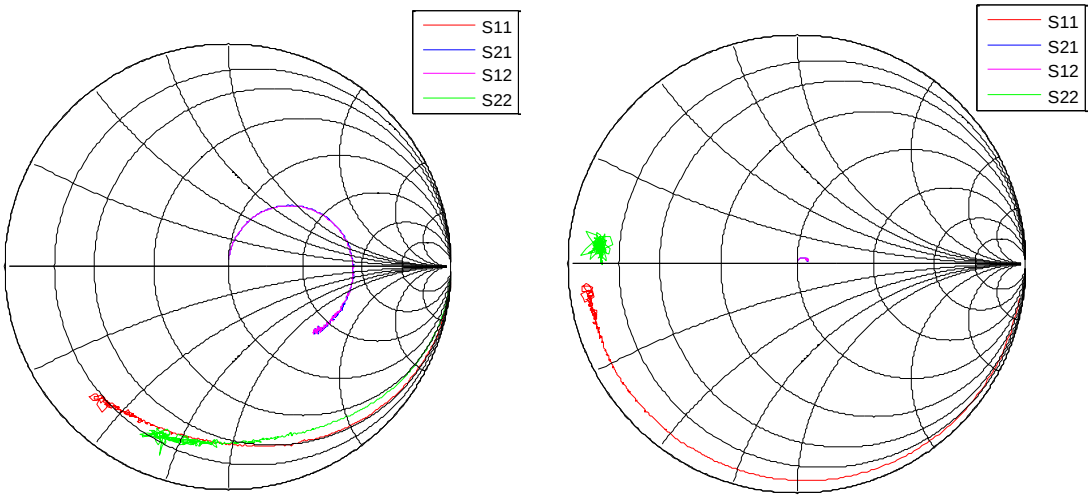


Figure 4.4. I-V behavior on the gate while the drain is held at 0 V.

The gate voltage is gradually increased, and the current is recorded. A plot of the gate I-V behavior is shown in Figure 4.4. During this process, the S-parameters are recorded at specified voltage intervals. The goal of measuring the S-parameters during the gate measurement is to determine the parasitic device parameters. Figure 4.5(a) shows the S-

parameters of the device while at a strong negative voltage. The S-parameters of a device when the gate is forward biased and conducting current can also be seen in Figure 4.5(b).

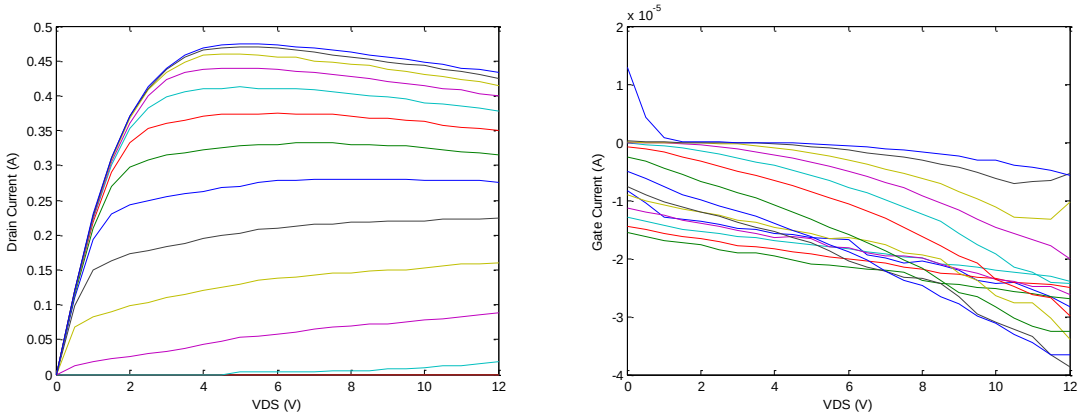


(a) (b)

Figure 4.5. S-parameter measurement of a 500-µm GaN HEMT during gate measurements with the gate (a) negatively biased and (b) forward biased into the conducting region.

4.2.4 DC Measurements and S-parameter IV

At this point, an accurate I-V curve measurement is performed on the DUT. During this measurement, both the gate current and the drain current are recorded as part of step S9. Because GaN HEMTs are both high power and high current devices, the voltage range on the I-V curve must be limited to a much lower level than the operating voltage in order to keep the I-V measurement from damaging the DUT. Figure 4.6(a) shows the tradition I-V curve of the DUT with the drain current plotted over a range of drain voltages at a number of different gate voltages. Figure 4.6(b) shows the gate current plotted over the same range of voltages.



(a) (b)

Figure 4.5. DC measurement of a 500-µm GaN HEMT with the gate (a) negatively biased and (b) forward biased into the conducting region.

The final measurement of the device characterization is by far the most time consuming. The S-parameters of the DUT in various regions of operation are recorded in step S10. The gate voltage and drain voltage are applied, and the S-parameters are recorded at each step of the curve. Three separate regions are investigated in this way. The first region is the voltage drain sweep (VDS). In this sweep, the gate voltage is set to a voltage near the gate bias during operation. The drain voltage is swept along the full range of drain voltage used during the I-V measurement. This sweep is repeated with a slight positive and negative perturbation to the gate voltage. The S-parameters are measured at each step. A similar process is completed for the voltage gate sweep (VGS) with the gate and drain voltages reversed. The final S-parameter I-V curve sweep is performed on the low voltages to characterize the turn on characteristics of the DUT. Figure 4.6 shows the three separate voltage sweep regions.

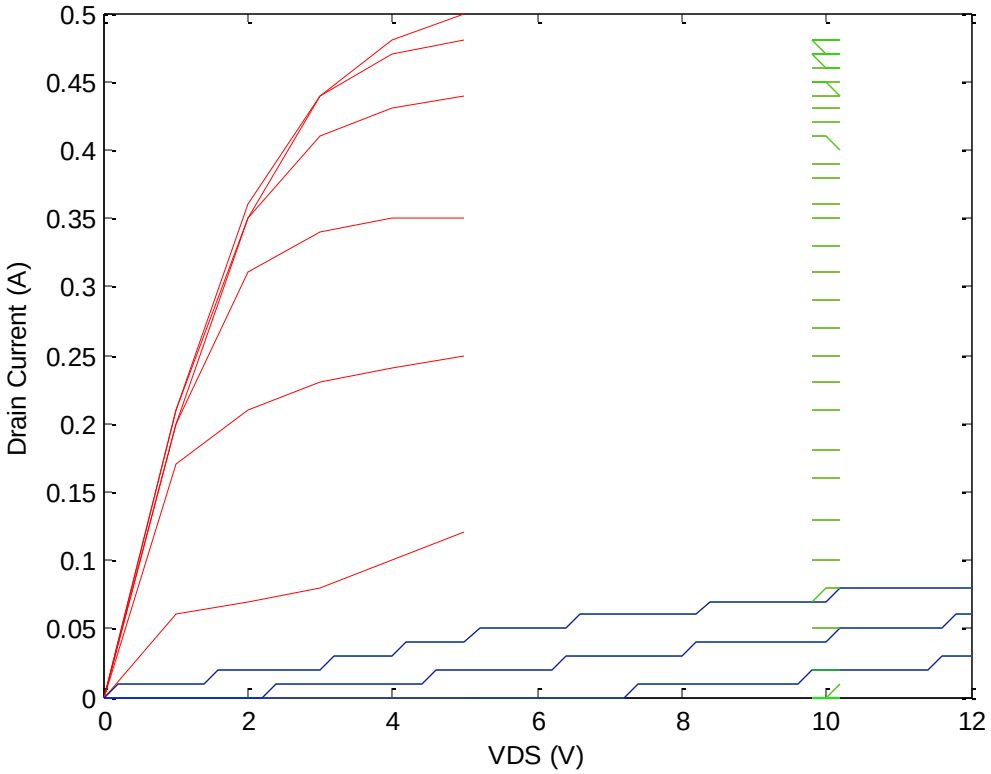


Figure 4.6. DC and S-parameter measurement of a 500-µm GaN HEMT with three separate characterization regions. The turn on region is shown in red, the VGS sweep is shown in green, and the VDS sweep is shown in blue.

These measurements were used to characterize the small signal changes in device performance over a range of values.

4.3 Extended Reliability Measurements

The majority of the operating time of the ALERTS is spent stressing the device and measuring the device's operation. After the final measurement of the device characterization is made, the system shuts off power to the DUT. The RF switches are switched to the power configuration. The previously determined optimal input and output impedances are applied to the tuners. The DUT is pinched off by applying a large negative voltage to the gate. The drain voltage is gradually increased to the level used during operation. When the drain is at the correct voltage, the voltage on the gate is

gradually increased to the correct level. The RF power is turned on from the signal source at a low level and increased until the device is driven into compression.

When the device is biased at the correct gate and drain voltages with the proper impedance on the source and drain ports and the proper input power is driving the device, the measurement timer is started. The timer commands the system to periodically measure the DUT. The operator can adjust the measurement period, but a typical value is 5 minutes. The system records the measurement and the times at which the measurement was made. The periodic measurement records VDS, VGS, and input power (Pin), which should not change during operation. The dependant variables that are recorded are drain current (IDS), gate current (IGS), output power (Pout), gain, drain efficiency, and power added efficiency. If the data is suspect or internal diagnostics suggest that the accuracy of the calibration has drifted, the timer can be stopped and restarted at any point during the operation. While the timer is stopped, the system can be recalibrated without compromising the accuracy of the data.

Chapter 5: Parasitic and Small Signal Model Extraction

The equivalent circuit small-signal model is an effective way to represent the linear performance of a device across a broad range of frequencies; however, the small-signal equivalent circuit model is valid under only very specific operating conditions. There are equivalent circuit models of varying complexity. More complicated models can often do a better job of incorporating subtle changes in S-parameters or incorporating the complexity of the fabrication process into the equivalent model [36]. In general, if the S-parameter behavior of the DUT does not require additional complexity, then additional complexity should be avoided. Simplicity is preferred in order to avoid problems associated with ambiguity. When used in this context, ambiguity refers to the problem that arises when there are multiple solutions to a single problem. In this case, when for a single equivalent circuit model, different parameter values reproduce S-parameters that are virtually identical and that closely agree with those of the measured DUT. For this research, the simplest model that does an effective job of representing a device's S-parameters is used. The small-signal equivalent circuit model used in this research is shown in Figure 5.1.

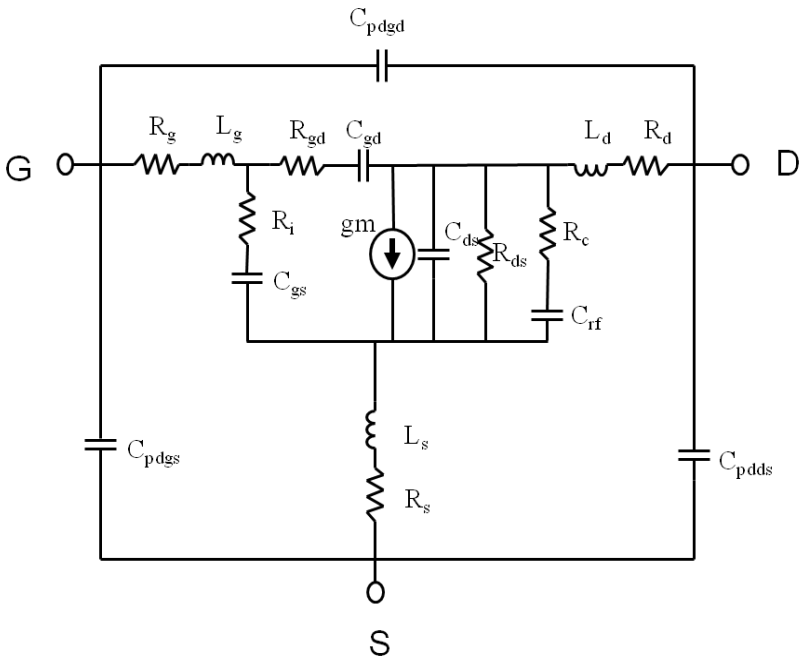


Figure 5.1. Small signal equivalent circuit model for the AlGaN/GaN HEMT, including parasitic components.

5.1 Parasitic Parameter Extraction

Existing semiconductor models are based primarily on modeling the active components of the intrinsic device [24]. To accurately model the intrinsic device, a mechanism for extracting external parasitics is needed. A well-known procedure for measuring external parasitics [36-38] has been implemented with a modification. The results observed from using the extraction technique suggest that it is a reliable method for determining parasitic elements.

The difficulty in determining the component values of the equivalent circuit model of either a large-signal or small-signal model comes from ambiguity. For the purposes of this report, the term ambiguity, in the general case, refers to a calculated result that may result from several different inputs. In the specific case, ambiguity refers

to a set of S-parameters that could be the result of different equivalent circuits or multiple instantiations of a single equivalent circuit using different sets of component values. The key to eliminating ambiguity and solving for a single unique solution is being able to perform experiments capable of isolating different parts of the circuit model so that they can be measured separately. This isolation is done by applying a bias to a device that causes it to behave in a predictable manner. Outside of the normal operating regime of the device, a high electron mobility transistor can be forced to behave as either a short circuit or an open circuit. Figure 5.2 shows the model for the external parasitics that is used.

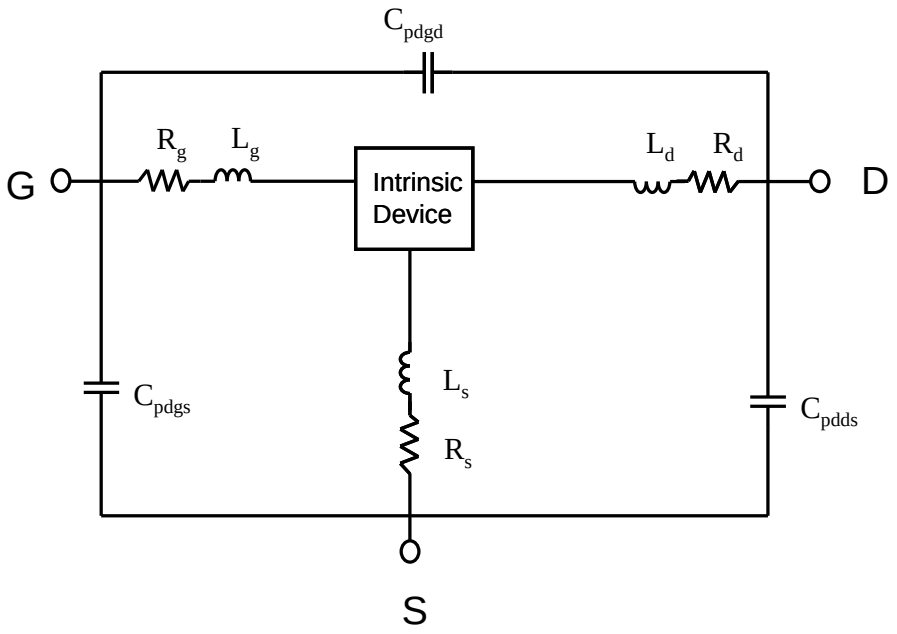


Figure 5.2. External parasitic equivalent circuit model.

Only limited knowledge of the intrinsic device model is needed to characterize the parasitic components of the circuit. During the cold FET measurements, the source and the drain are both held at 0 V. When biased in this manner, the device behaves like a diode.

5.1.1 Reverse Bias: Shunt Parasitic Capacitor Extraction

The device is reversed biased by setting the drain and source to zero volts and applying a negative voltage to the gate. When the device is reversed biased, the intrinsic device small-signal low frequency behavior can be modeled as an open circuit. In this case, it behaves like a diode that has been reverse biased, and the device is shut off. This setup allows the equivalent circuit model to be represented as a set of capacitors in parallel, as shown in Figure 5.3.

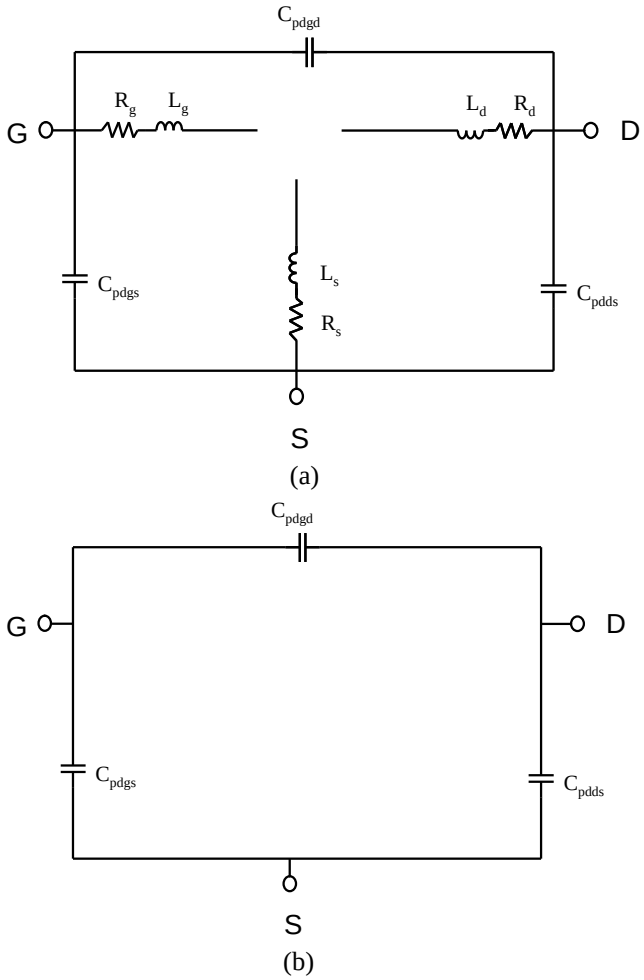


Figure 5.3. (a) Simplified equivalent circuit model of the reverse biased device and (b) with the series components removed.

The circuit then becomes a three-terminal system connected by shunt capacitors. The equivalent Y-parameter model is shown in Figure 5.4 [39].

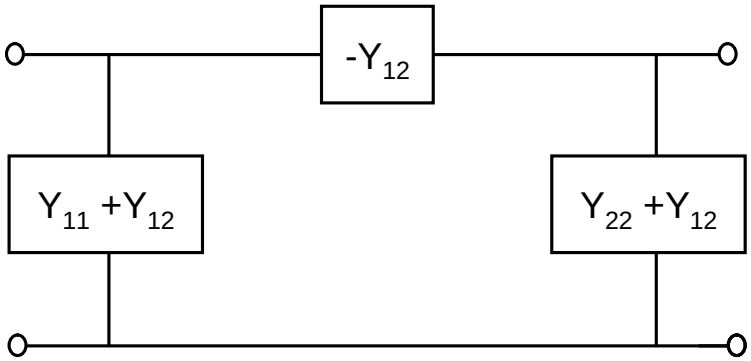


Figure 5.4. Admittance matrix equivalent circuit model.

The procedure for calculating the parasitic capacitances is shown below:

1. Apply a sufficiently negative bias to the device to pinch off the gate and drain.
2. Measure the S-parameters of the device.
3. Convert the S-parameters into admittance parameters.
4. Calculate the parasitic capacitances using the admittance parameters.

Equations 5.1–5.3 are used to calculate the parasitic capacitance for a given set of admittance parameters:

$$\mathrm{Cpdg} = \mathrm{Im}\left(\frac{-Y_{12}}{\omega}\right) \tag{5.1}$$

$$\mathrm{Cpgs} = \mathrm{Im}\left(\frac{Y_{11}}{\omega}\right) + \mathrm{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{5.2}$$

$$\mathrm{Cpds} = \mathrm{Im}\left(\frac{Y_{22}}{\omega}\right) + \mathrm{Im}\left(\frac{Y_{12}}{\omega}\right) \tag{5.3}$$

5.1.2 Forward Bias: Series Parasitic Component Extraction

The procedures for the extracting the series parasitic component values from the forward-biased device are analogous to those for the reversed-biased device but are more complicated and include several additional considerations. When the device is forward biased, the intrinsic device behaves like a short circuit. Measurement has shown that at high frequencies, a residual gate capacitance is present on the device and must be included in the model when extracting the parasitics. Figure 5.5 shows the model used to extract parasitics when the device is forward biased.

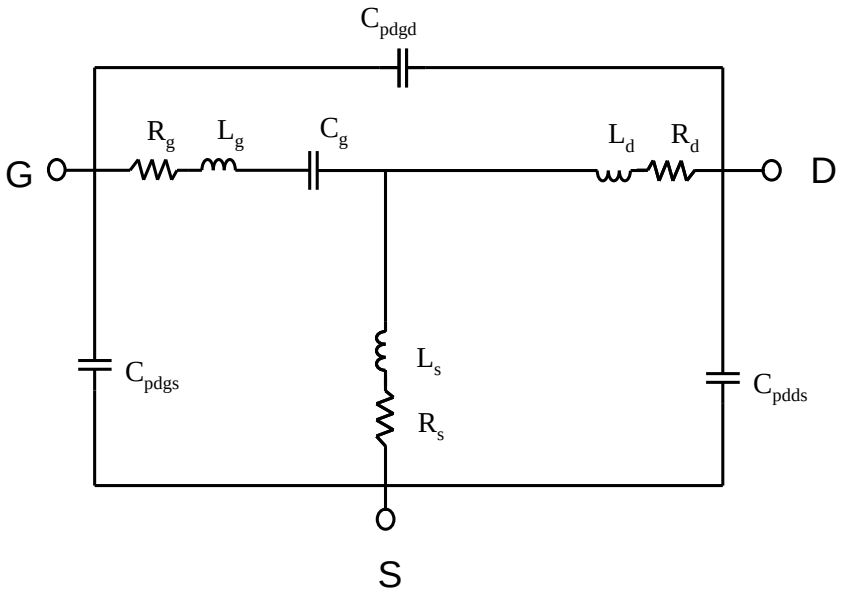


Figure 5.5. High frequency model of the forward-biased device.

The procedure for calculating the parasitic capacitances is as follows:

1. Apply a positive voltage to the gate to drive sufficient current through the device to put the diode into the "on" state but not enough current to damage the device.

2. Measure the S-parameters of the device.

3. Convert the S-parameters to Y-parameters.

4. Subtract the shunt parasitic capacitances.

5. Convert the S-parameters to Z-parameters.

6. Calculate the component values of the series elements.

In step 4, the admittance of the shunt capacitors are subtracted from the extrinsic Y-parameters. The equations used for subtracting the Y-parameters are shown below:

$$Y_{11}' = Y_{11} - j\,\omega\,(Cpgs + Cpgd) \quad (5.4)$$

$$Y_{22}' = Y_{22} - j\,\omega\,(Cpds + Cpgd) \quad (5.5)$$

$$Y_{21}' = Y_{21} - j\,\omega\,Cpgd \quad (5.6)$$

$$Y_{12}' = Y_{12} - j\,\omega\,Cpgd \quad (5.7)$$

Following this, the admittance parameters with the parasitic capacitances removed are converted into impedance parameters. The equivalent circuit with the parasitic capacitance removed is shown in Figure 5.6.

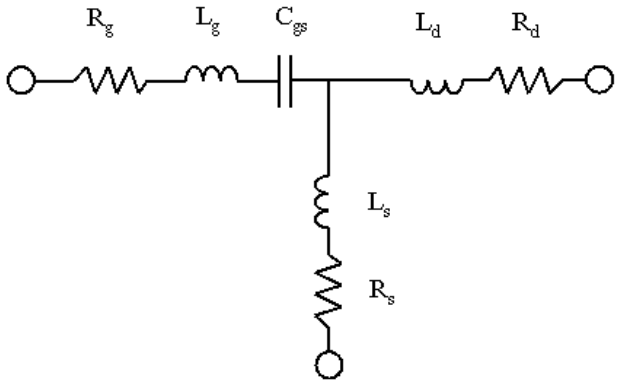


Figure 5.6. High frequency model of the forward-biased device with parasitic capacitances de-embedded.

This model shows a three-terminal passive device. A well-known technique for determining the Z-parameters of such a system is shown in Figure 5.7 [39].

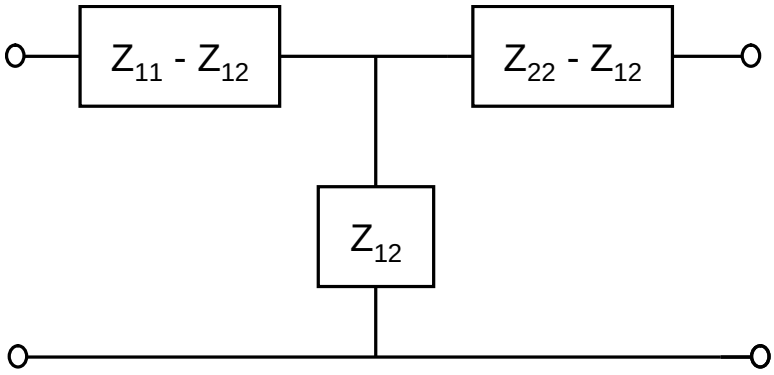


Figure 5.7. Impedance matrix equivalent circuit model.

From this, we can determine the impedance parameters of the model. Equations 5.9–5.11 show how to calculate the impedance parameters of the model in Figure 5.6 [37]:

$$z_{11} = R_g + R_s + j\,\omega\,(L_g + L_s) - \frac{j}{\omega\,C_{gs}} \tag{5.8}$$

$$z_{12} = z_{21} = R_s + j\,\omega\,L_s \tag{5.9}$$

$$z_{22} = R_d + R_s + j\,\omega\,(L_g + L_s) \tag{5.10}$$

Based on these equations, the parameter values can be calculated:

$$R_s = \mathrm{Re}(z_{12}) \tag{5.11}$$

$$R_g = \mathrm{Re}(z_{11}) - R_s \tag{5.12}$$

$$R_d = \mathrm{Re}(z_{22}) - R_s \tag{5.13}$$

$$L_s = \frac{\mathrm{Im}(z_{12})}{\omega} \tag{5.14}$$

$$L_d = \frac{\mathrm{Im}(z_{22})}{\omega} - L_s \tag{5.15}$$

$$L_g = \frac{\mathrm{Im}(z_{11})}{\omega} - L_s + \frac{1}{\omega^2\,C_{gs}} \tag{5.16}$$

These values are directly calculated from the measured data with the exception of the last equation. C_{gs} is an unknown value. With the knowledge of C_{gs}, the entire set of series parasitic elements can be determined. There are several useful techniques for calculating C_{gs}. One can calculate C_{gs} using a polynomial fit function on the reactive component of the impedance. Others have used knowledge of the fabrication process to estimate C_{gs}. This component can also be determined by examining the resonance properties of that branch of the T junction.

A technique has been developed that uses differentiation to isolate elements that have different frequency dependence. The technique for determining C_{gs} is shown below:

$$X_{11} = \mathrm{Im}(z_{11}) \tag{5.17}$$

$$\frac{X_{11}}{\omega} = \left(L_s + L_g\right) - \frac{1}{\omega^2 C_{gs}} \tag{5.18}$$

$$\frac{\partial \frac{X_{11}}{\omega}}{\partial \omega} = \frac{2}{\omega^3 C_{gs}} \tag{5.19}$$

$$C_{gs} = \frac{2}{\omega^3 \frac{\partial \frac{X_{11}}{\omega}}{\partial \omega}} = \frac{2}{\omega^3 \frac{\Delta \frac{\mathrm{Im}(z_{11})}{\omega}}{\Delta \omega}} \tag{5.20}$$

The numerical differentiation of $\mathrm{Im}(z_{11})/\omega$ was performed using the following equation:

$$\frac{\Delta x_i}{\Delta \omega} = \frac{x_{i+1} - x_{i-1}}{2\Delta \omega} \tag{5.21}$$

The modified extraction process was performed on several devices from several different wafers. A comparison of the values of L_g as determined by different methods is shown in Figure 5.8. The calculations differ by the manner in which C_{gs} is calculated. The method described in [40] assumes measurements will be made at frequencies where C_{gs} is

negligible. In [39], C_{gs} is calculated based on the knowledge of the fabrication process of the device. The numerically determined value follow the procedure described previously.

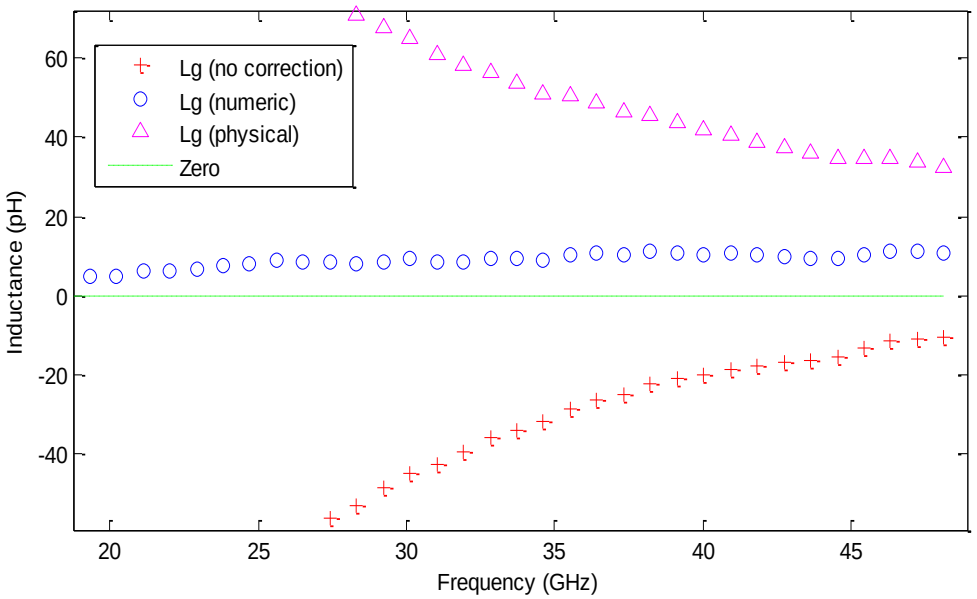


Figure 5.8. Comparison of calculated gate inductance as determined by different methods.

The series parasitic values are plotted as a function of frequency in Figure 5.8. As can be seen in Figures 5.8 and 5.9, the value L_g when calculated using this technique does not show a frequency dependence, which is consistent with a linear equivalent circuit model.

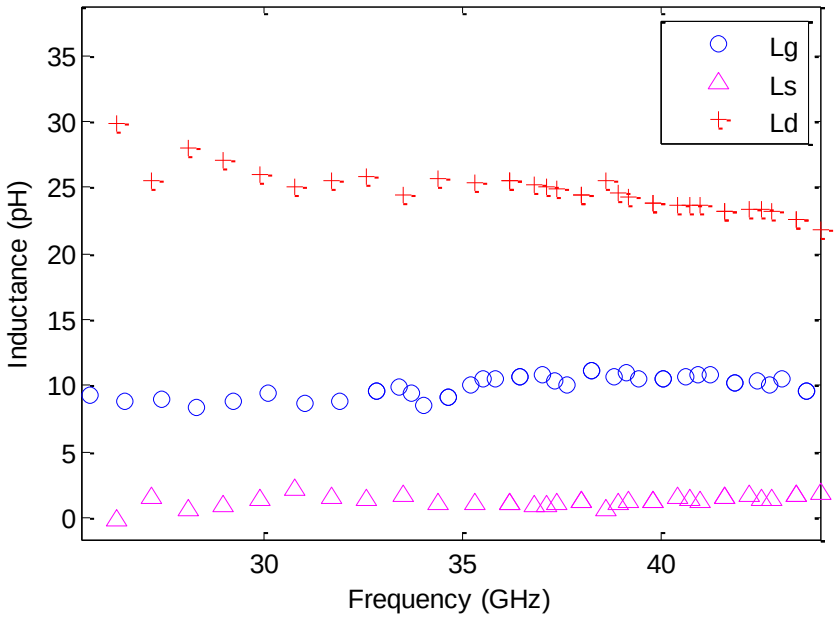


Figure 5.9. Comparison of calculated gate inductance as determined by different methods.

The extracted values were used in the model shown previously to reproduce the S-parameters. The parasitic shunt capacitances were embedded. The modeled S-parameters are compared to the measured S-parameters of the forward-biased device and close agreement is observed as shown in Figure 5.10.

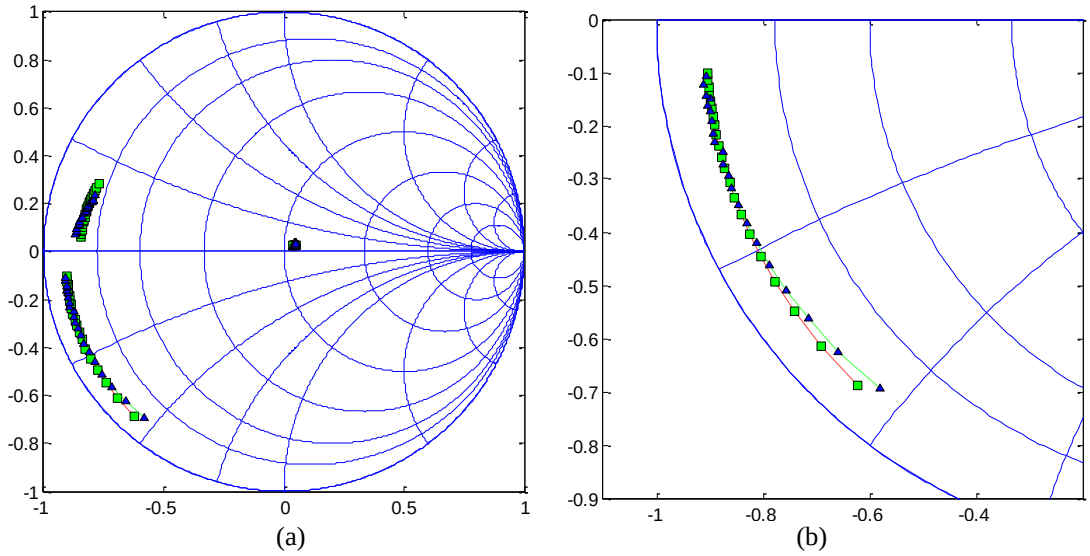
The new technique has a number of advantages:

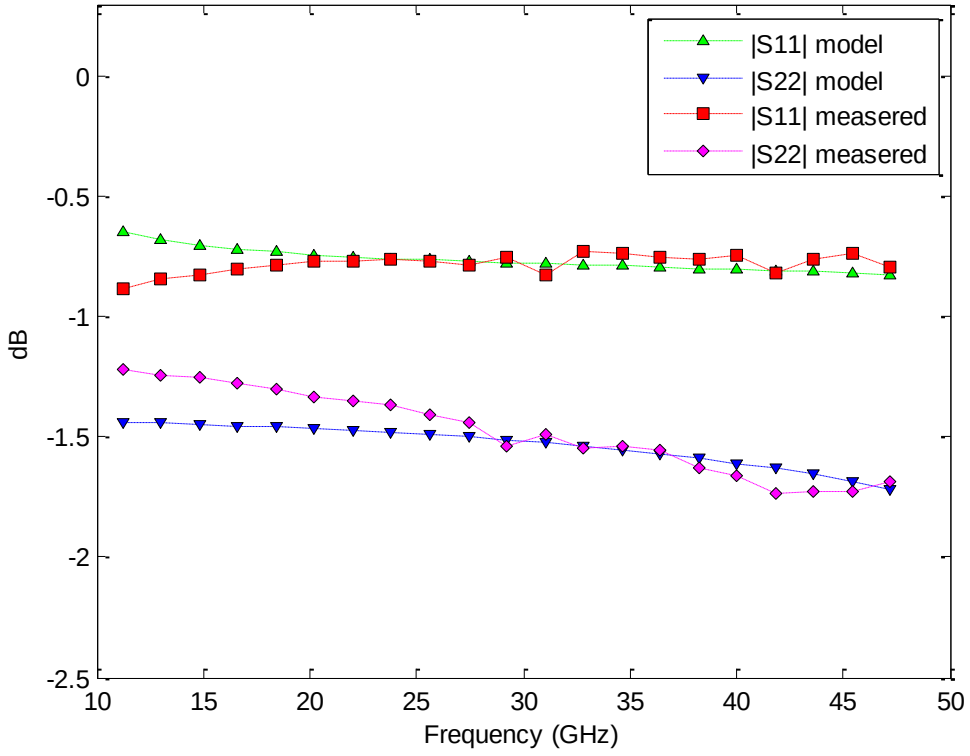
1. The calculated value of Lg does not show the frequency dependence that is observed when Lg is determined by the other methods. This is more consistent with the linear model of the inductor when used in the equivalent circuit model.

2. This method determines the gate inductance based on the frequency response of the Z-parameter and does not require any special information about the device or additional measurement to determine Cgs.

3. The lack of frequency dependence in the calculated value of Lg has the effect that the measurement can be performed at lower frequencies without requiring a Q-band VNA. This reduces the capital requirements to perform the measurement.

4. This method is generic for RLC circuits. The example provided demonstrates the usefulness when extracting parasitics from GaN HEMTs, but the method described could be applied to any unknown series RLC circuit.



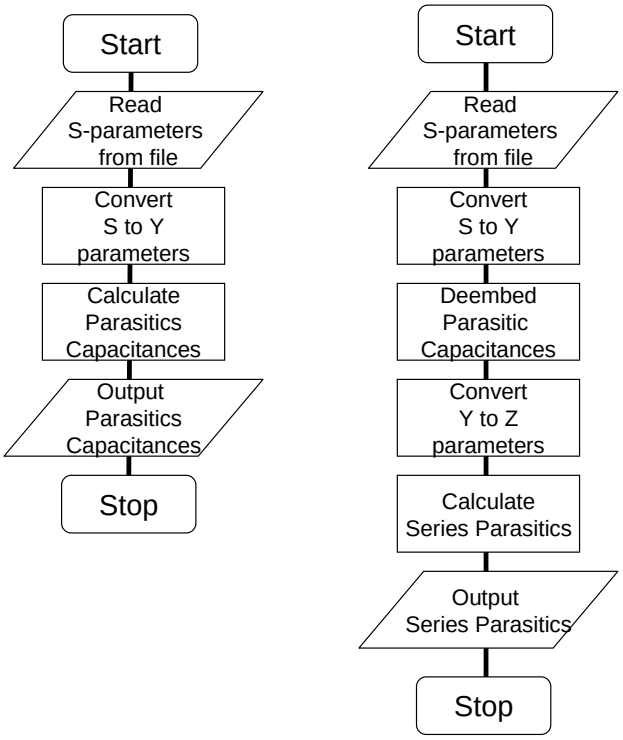


(c)

Figure 5.10. Modeled S-parameters compared with the (a) measured and modeled S-parameters plotted on the Smith chart and (b) measured and modeled S11 plotted on the Smith chart, and (c) the magnitude (dB) for S11 and S22 from 10 to 50 GHz

A new method for determining the residual gate capacitance based on the frequency dependence of the impedance value for Cgs is used to calculated a series gate inductance that does not depend on frequency. The results of the model reproduced from the

equivalent circuit model agree well with the measured data. The method described can be applied generally to determine the component values for a RLC for which the impedance parameters are known or can be determined. Figure 5.11 shows a flowchart of the programs used to perform the parasitic component extraction using the cold FET procedure.



(a) (b)

Figure 5.11. Flowchart for cold FET programs: (a) parasitic capacitance calculation and (b) series parasitic calculation.

5.1.3 Results of Parasitic Component Extraction

The procedure was performed on a number of devices. The values of the components in the equivalent circuit model were extracted and S-parameters for the equivalent circuit model were calculated. A representative example of these calculations is presented. Agilent's Advanced Design System (ADS) computer aided design program

was used to compare measured data with modeled data. Figure 5.12 shows the circuit used to compare the reverse bias measured data with the modeled data.

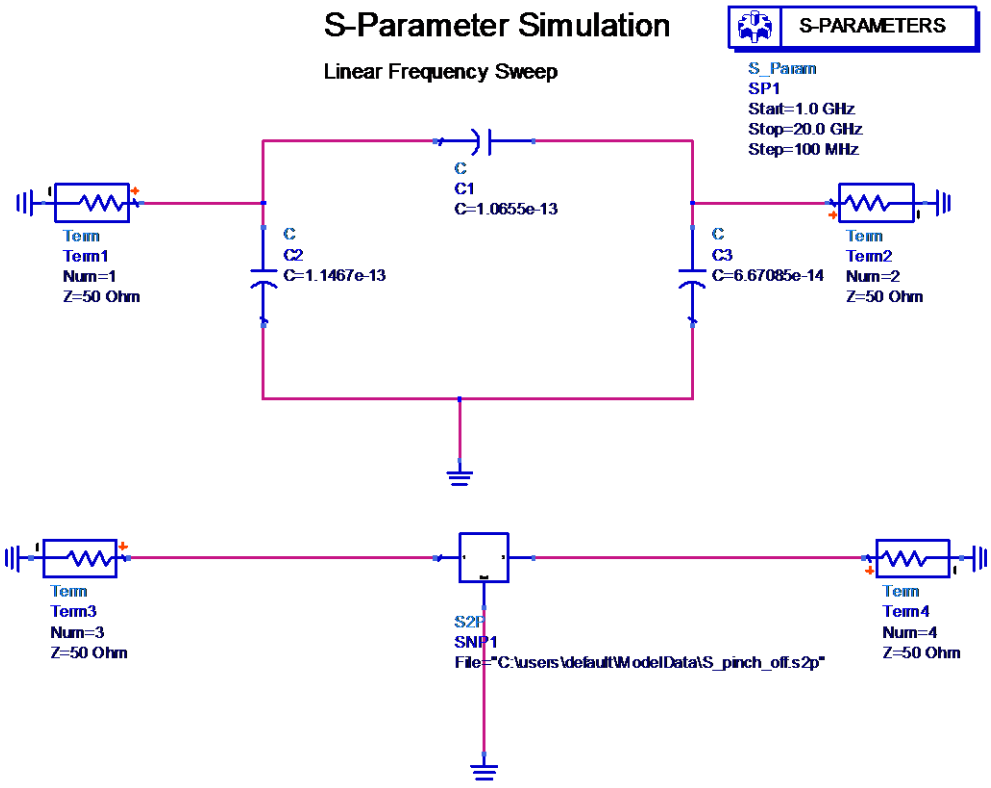
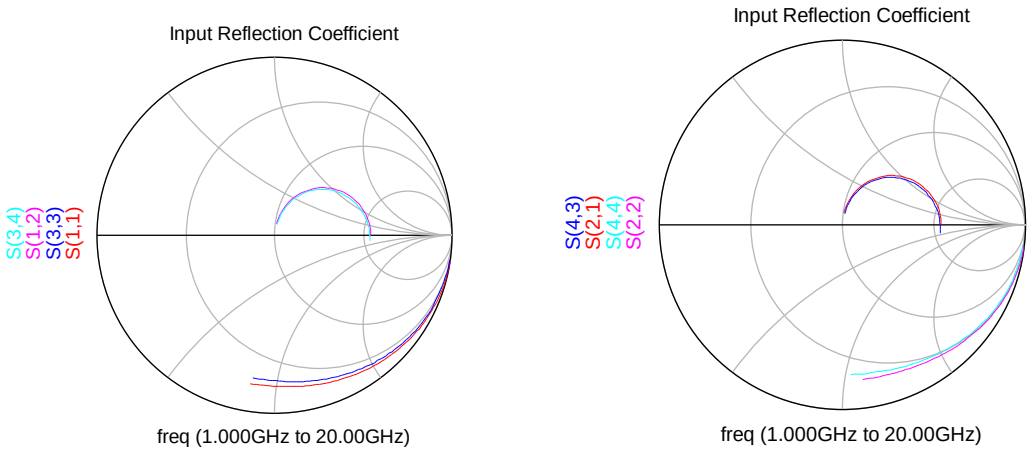


Figure 5.12. ADS circuit used to compare measured data with the model for the reverse biased device.

Figure 5.13 shows the comparison of the measured and modeled data from 1 to 20 GHz.



(a) (b)

Figure 5.13. Reverse-biased measured and modeled S-parameters comparing (a) S_{11} and S_{12} and (b) S_{22} and S_{21}.
Note: The lower numbered (1,2) S-parameters are modeled and higher numbers (3,4) are measured.

The circuit used to model the forward-biased devise is shown in Figure 5.14.

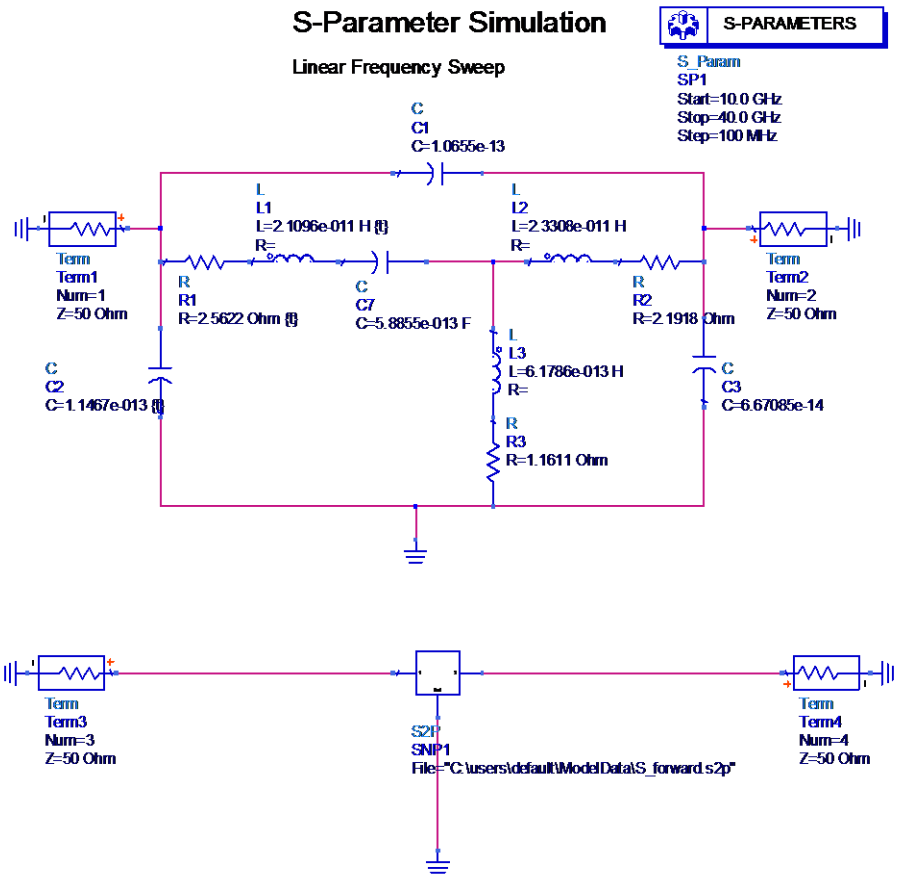
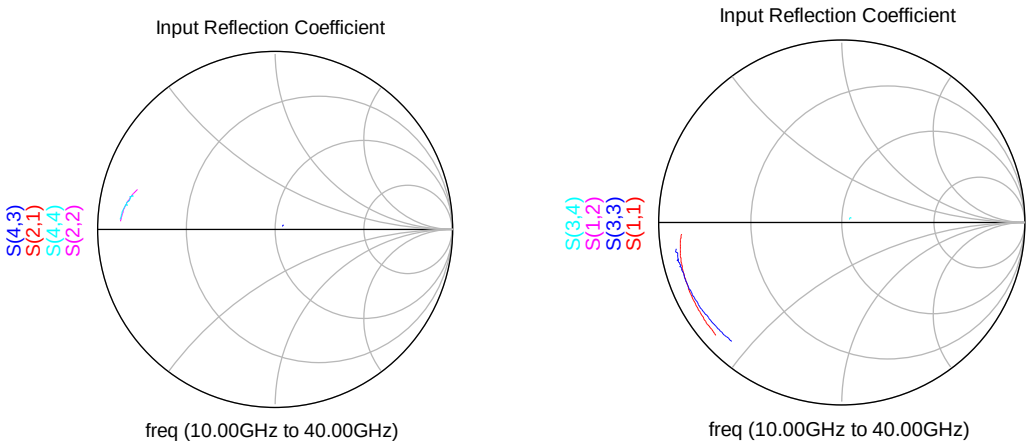


Figure 5.14. ADS circuit used to compare measured data with the model for the forward-biased device.

In Figure 5.14, the measured S-parameters for the forward-biased device are compared to those of the modeled device from 10 to 40 GHz. The frequency ranges shown in Figures 5.13 and 5.14 were selected to be where the parasitics being measured would have the largest effect. These ranges are low frequencies for capacitors and high frequencies for inductors.

The error was calculated by taking the absolute value of the difference between measured and calculated values divided by the absolute value of the measured value. The average error for S_{11} and S_{22} for the reverse-biased model was less than 6%. The error

for the S_{11} and S_{22} for the forward-biased model was less than 7%. The forward and reverse transmission parameters (S_{12} and S_{21}) were higher but on average less than 15%. The magnitude of the transmission parameters was much smaller than the reflection coefficients. This aspect makes them more susceptible to measurement errors. These errors are from the directly extracted values, and we have successfully reduced these values by using optimization algorithms. Optimizing the parasitic elements together with the small-signal model of the device resulted in errors of less than a few percent.



(a) (b)

Figure 5.13. Forward-biased measured and modeled S-parameters comparing (a) S_{22} and S_{21} (b) S_{11} and S_{12}. Note: The lower numbered (1,2) S-parameters are modeled and higher numbers (3,4) are measured.

The ability to isolate and determine the parasitic capacitances of a DUT is a crucial step in generating either small-signal or large-signal device models. A well-known parasitic extraction algorithm that determines the component values of a device model that reliably reproduce the measured data was implemented. The technique used builds upon existing parasitic extraction algorithms by numerically determining the residual intrinsic device gate capacitances.

5.2 Intrinsic Device

With the knowledge of the parasitic circuit elements of the device, these components can be de-embedded from the S-parameters and the intrinsic device examined. The small-signal device model provides significant information about the device and forms the basis of the large-signal model. Using the small-signal model shown in Figure 5.14, the parameter values of the equivalent circuit model component can be directly extracted.

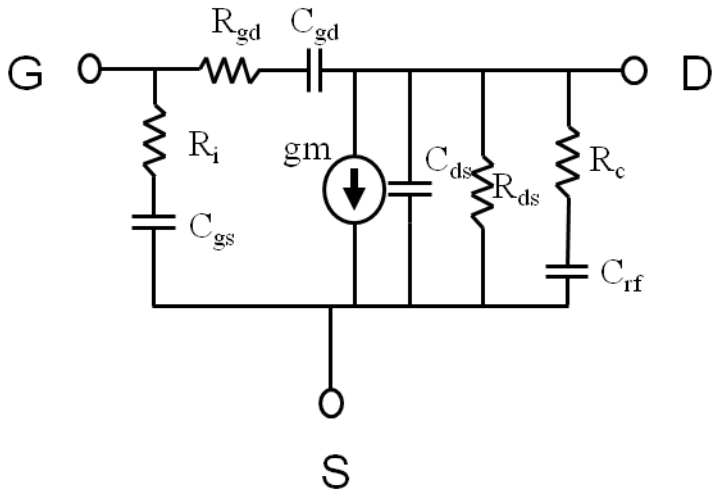


Figure 5.14. Small-signal intrinsic equivalent circuit model.

The equations for the component parameter values are shown below [41, 42]:

$$C_{gd} = -\mathrm{Im}\left(\frac{Y_{12}}{\omega}\right) \times \left(1 + \frac{\mathrm{Re}\,(Y_{12})}{\mathrm{Im}\,(Y_{12})}\right)^2 \tag{5.22}$$

$$C_{ds} = \frac{1}{\omega} \times \mathrm{Im}(Y_{22} + Y_{12}) \tag{5.23}$$

$$C_{gs} = \frac{1}{\omega} \times \mathrm{Im}\left(\frac{1}{Y_{11}+Y_{12}}\right)^{-1} \tag{5.24}$$

$$g_d = \mathrm{Re}(Y_{22}) + \mathrm{Re}(Y_{12}) \tag{5.25}$$

$$R_i = \mathrm{Re}\left(\frac{1}{Y_{11}+Y_{12}}\right) \tag{5.26}$$

$$R_{gd} = -\frac{\mathrm{Re}(Y_{12})}{\mathrm{Im}(Y_{12})} \times \left[\left(1+\frac{\mathrm{Re}(Y_{12})}{\mathrm{Im}(Y_{12})}\right)^2\right]^{-1} \tag{5.27}$$

$$g_m = \left|\frac{Y_{11}-Y_{12}}{Y_{11}+Y_{12}}\right| \times \left(\frac{1}{Y_{11}+Y_{12}}\right)^{-1} \tag{5.28}$$

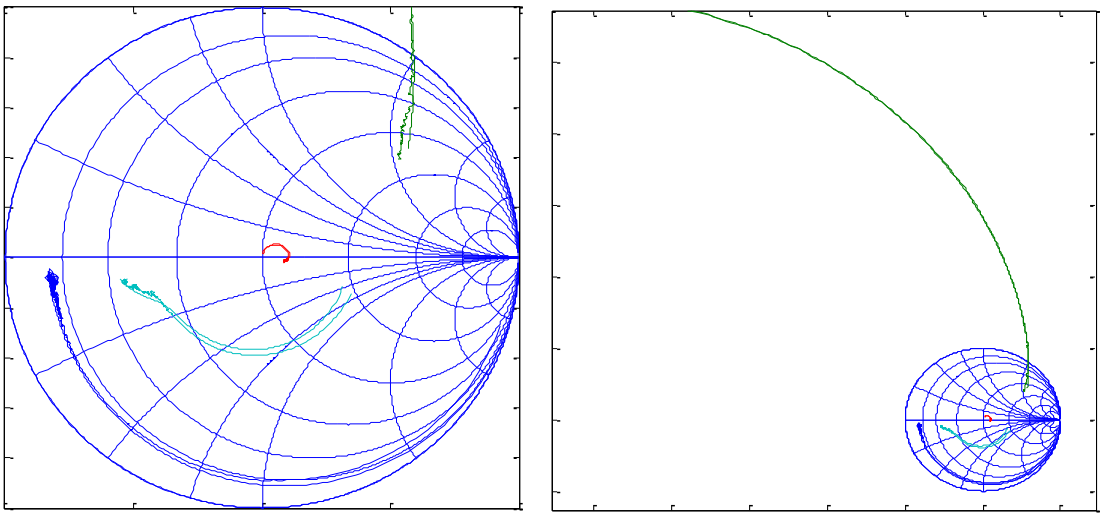
These calculations determine the parameter values of all the components in the small-signal model with the exception of R_c and C_{rf}. These components are added to the model in order to include a frequency-dependant component to the transconductance. The procedure for calculating R_c and C_{rf} is straightforward. The components are used to determine the S-parameters of the equivalent circuit model of the intrinsic device. The measured S-parameters of the intrinsic device are determined by de-embedding the parasitic components from the DUT. Both sets of S-parameters are converted to Y-parameters. In this form, the admittance between the drain and the source is given by Y_{22}. The difference between the two admittances can be determined by simple subtraction. This value is the admittance of the RC branch. The impedance of this branch is the inverse of the difference. The equation for each component of the RC branch is given by

$$R_c = \mathrm{Re}\left(\frac{1}{Y_{22\_Measured} - Y_{22\_Model}}\right) \tag{5.29}$$

$$C_{rf} = \frac{1}{\omega} \times \mathrm{Im}\left(\frac{1}{Y_{22\_Measured} - Y_{22\_Model}}\right) \tag{5.30}$$

If there are other frequency dependencies associated with the transconductance, additional RC shunt branches can be added. For this research, which was confined to the frequencies of interest (500 MHz to 40 GHz), a single RC circuit was sufficient.

Once the final equivalent circuit model parameters are calculated by direct extraction, an optimization can refine the difference between the measured S-parameters and the modeled S-parameters. A cost function is generated by creating a weighted sum of normalized mean squared errors of the difference between the measured and modeled S-parameters. The optimization routine works by varying the circuit component parameters with a goal to minimize the cost function. Figure 5.15 shows the measured and modeled S-parameters as generated by the MATLAB function used to perform the calculations used during the model extraction.



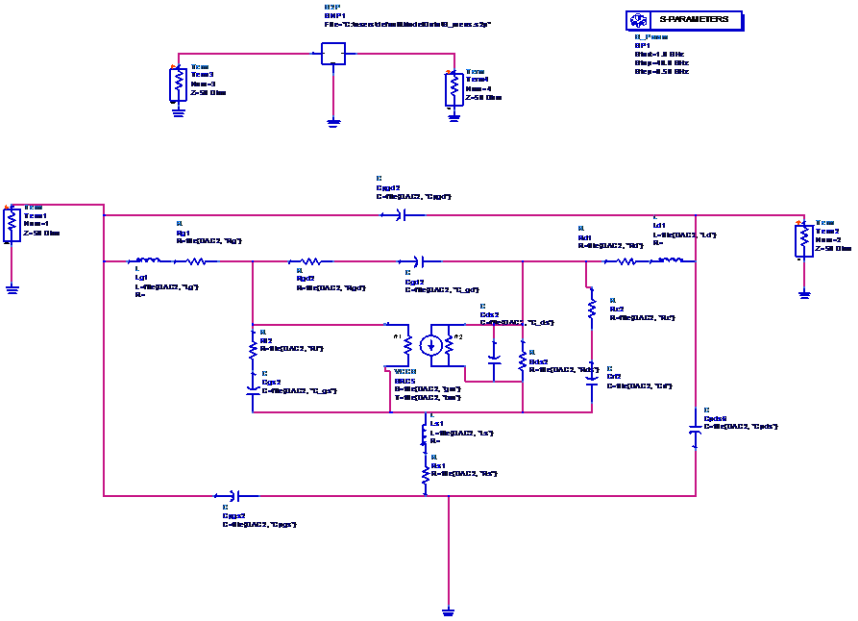
(a) (b)

Figure 5.15. S-parameters produced by the equivalent circuit model plotted superimposed on measured S-parameters on the Smith Chart for (a) the unit circle and (b) an expanded plot to show the agreement of S21.

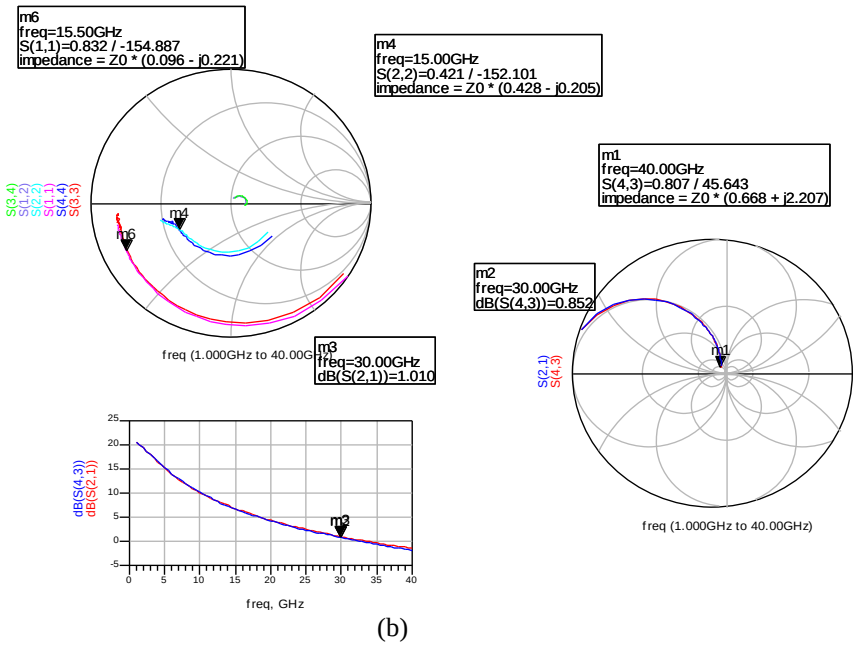
To verify the accuracy of the modeling the simulation was reproduced using Agilent ADS, which is Agilent's microwave computer aided design software. Figure 5.16(a) shows the circuit layout in ADS used to compare measured and modeled data.

The modeled data, which agree exactly with that computed in our MATLAB simulator, are shown in Figure 5.16(b). With the ability to extract the circuit parameters

that go into a small-signal model, we can begin to examine the much more complicated task of large-signal models.



(a)



(b)

Figure 5.16. ADS circuit (a) layout for small-signal modeling simulations and (b) the results.

Chapter 6: Large-Signal Modeling

A mathematical model of a device will always be an imperfect representation of that device's performance. The large-signal model can be differentiated from a small-signal model by the scope of operation over which that model does an adequate job of modeling the real device. The small-signal model attempts to represent the device behavior over a range of frequencies for a device operating at a specific bias for input RF power levels that are small enough that they do not significantly alter that device's bias condition. The large-signal model attempts to recreate the electrical response of the modeled device for a broad range of frequencies over all bias conditions with an arbitrary input power level.

A large-signal model can be considered accurate if it can reproduce the S-parameters of the device being modeled under a large number of bias conditions while simultaneously being able to reproduce the large-signal behavior such as output power, efficiency, and compression. These results should change with changes in impedance in the same way that the device changes with changes in impedance. Additional functionality can be incorporated into the large-signal model to incorporate other operating conditions, such as operating at elevated temperatures. The measurements used to make the large-signal model were described in Chapter 4. This chapter focuses on the calculations used to transform this data into a functional model. The core large-signal model used in this research was the Angelov (Chalmers) Model [43-47]. The equivalent circuit model is shown in Figure 6.1.

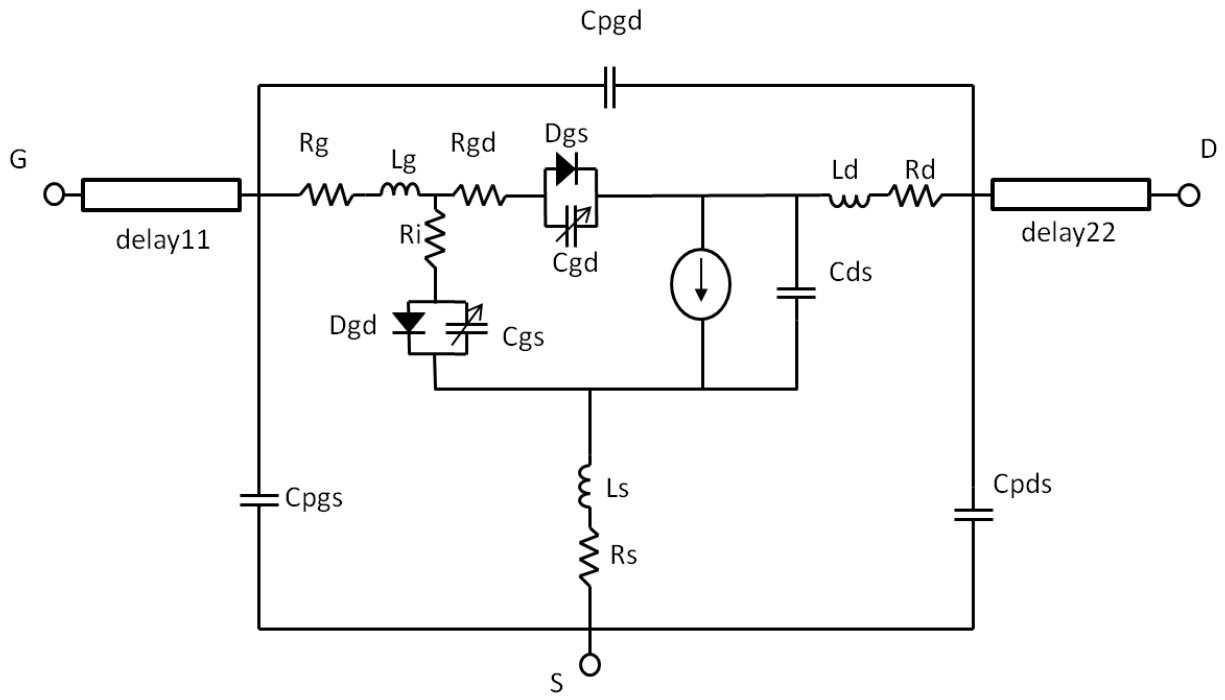


Figure 6.1. Large-signal model based on the Angelov (Chalmers) model as implemented in Agilent ADS.

One simple modification to the model that can be seen in Figure 6.1 is the addition of delay lines at the input and output. These lines can correct for phase error in the calibration process and keep external phase changes from manifesting as additional parasitic component values. The source of the phase error is usually attributed to probe pads on the device and errors from the use of transmission lines of finite length as the through standard during calibration.

6.1 Gate Behavior Modeling

The large-signal model process begins the same way that the small-signal model process begins. The external parasitics are determined. This procedure is described in detail in section 5.1 in the previous chapter. The only addition that has not been described is the inclusion of the short transmission lines to correct for phase shift delay. The original calculation of the delay lines occurs after the parasitic capacitances are determined. The

Y-parameters of the parasitic capacitances are calculated using the previously determined values for the capacitances. The equations for the Y-parameters with the active device pinched off are given by the following equations:

$$Y_{11} = j\,\omega\,Cpgs + j\,\omega\,Cpgd \quad (6.1)$$

$$Y_{22} = j\,\omega\,Cpds + j\,\omega\,Cpgd \quad (6.2)$$

$$Y_{12} = Y_{21} = -j\,\omega\,Cpgd \quad (6.3)$$

The Y-parameters are converted to S-parameters. The phase change along the delay line is simply one half the difference in the angle between the measured S-parameters and the S-parameters calculated by the using the equivalent circuit model. The Agilent ADS only allows transmission lines to be represented as lengths and not as phase changes. To convert from angle in radians to length in meters, the phase change is divided by the angular frequency (ω or $2\,\pi\,f$) and the speed of light.

The large-signal model needs to account for the current behavior of the gate terminal as well. The Agilent Angelov Model that was chosen for this research uses the following equations to model the gate current [43].

$$Igs = IJ \times (\exp(PG \times \tanh(2 \times (Vgsc - VJG))) - \exp(PG \times \tanh(-2VJG))) \quad (6.4)$$

$$Igd = IJ \times (\exp(PG \times \tanh(2 \times (Vgdc - VJG))) - \exp(PG \times \tanh(-2VJG))) \quad (6.5)$$

IJ is the gate forward saturation current, PG is the gate current parameter, VJG is the diode turn on voltage, Vgsc is the voltage across the gate source diode, and Vgdc is the voltage across the gate drain diode. The characterization of the gate junction is

accomplished by determining the values of these parameters. The diode modeled is ideal in the reverse bias condition, and therefore, the model does a poor job of characterizing the current behavior of the reverse bias after the onset of reverse breakdown.

The diode parameters are determined in two steps: direct extraction and optimization. PG is determined by taking one half the maximum of the differentiation of the logarithm of the gate current with respect to the gate voltage. VJG is the turn-on voltage of the diode. This is select to be the point at which the gate current first reaches 5% of the maximum gate current. With the knowledge of PG and VJG, a start value for IJ can be determined from the following equation:

$$IJ = \frac{Ig_{measured}}{\exp(PG \times \tanh(2 \times (Vgdc_{measured} - VJG))} \quad (6.6)$$

With the directly extracted values to use as input, the model equation is used in an optimization routine and compared to the measured data. For the positive portion of the I-V curve, good approximation of the measured data can quickly be realized. Figure 6.2 shows a comparison of the measured and modeled data for the gate current model.

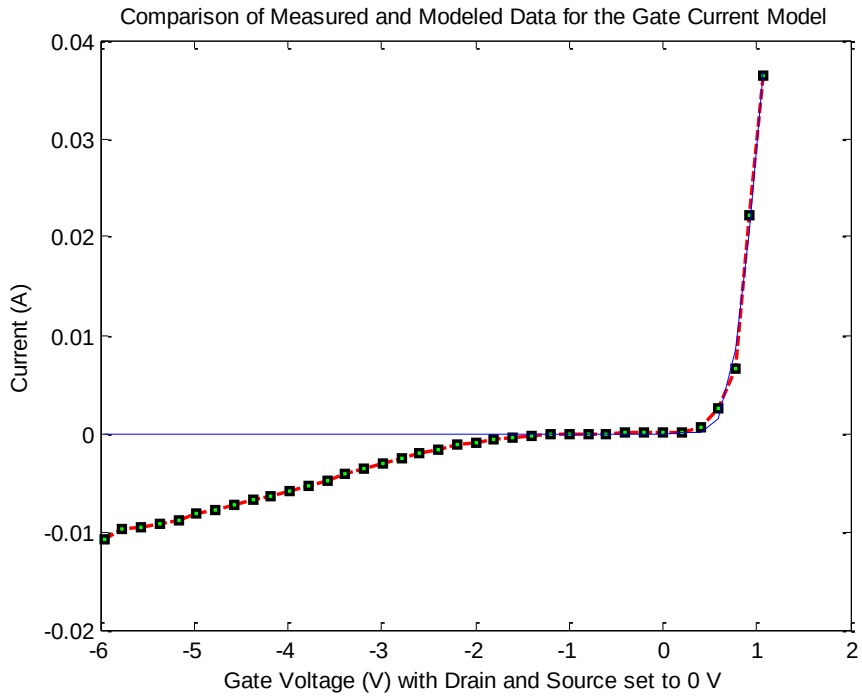


Figure 6.2. Measured (show with squares) and modeled (blue line) gate current data for the DUT.

As can be seen in Figure 6.2, the reverse breakdown behavior is not included in the gate current model

6.2 Small-Signal Model Generation

After the gate current behavior has been characterized and the values of the extrinsic parasitic components have been determined, the next step in the large-signal model development process is to generate a set of small-signal models for the three regions of bias conditions for which the S-parameters have been measured. To review from Chapter 3, these three regions are the turn-on region (TO), the gate voltage sweep (VGS), and the drain voltage sweep (VDS). By converting the S-parameters of these regions into equivalent circuit models, it is possible to see how the parameter values of the biases change with voltage and to determine equations for those changes.

From Figure 6.1, it can be seen that there are five voltage-dependant components in the large-signal model. The first two are the gate-drain diode and the gate-source diode. During normal operation, these diodes are operated below turn-on and their conductive properties change little. As a result, they behave largely as open circuits, which do not need to be modeled in the small-signal models. The capacitive changes of the diodes are represented as the variable capacitors Cdg and Cgs. The final element that changes with bias condition is the voltage-controlled current source (VCCS). This element changes as a function of gate voltage and drain voltage. In the small-signal model in Figure 5.1, the VCCS is represented by gm and Rds. For the large-signal model Rds will be represented by gd, which is 1/Rds.

The small-signal model extraction is accomplished in several stages. The initial stage allows the small-signal model extraction routine to select the best equivalent circuit model for each voltage; however, this allows all of the equivalent circuit model components to vary with voltage. For the large-signal model, only four values are allowed to vary with voltage. These values are Cdg, Cgs, gm, and gd. All the other model parameters are fixed. The best fixed values from the first stage of small-signal model selection must be selected. The best values are those that minimize error, which is defined as a weighted sum of the normalized difference between the measured S-parameters and the modeled S-parameters. The fixed values that simultaneously minimize error are averaged to select the best possible value.

Once the fixed values are selected, the small-signal optimization is repeated. This time, the only values that are allowed to change are the four voltage-dependant variable values. At this point, we have raw data of how the voltage-dependant variables change as

the bias changes. In order to model the device, we need equations to relate these parameter values with the independent variables, in this case, the bias voltages.

The variations due to bias conditions of key components of the small signal models are shown in the following figures. The transconductance in the small signal models at each bias condition is plotted as a function of the gate voltage in Figure 6.3.

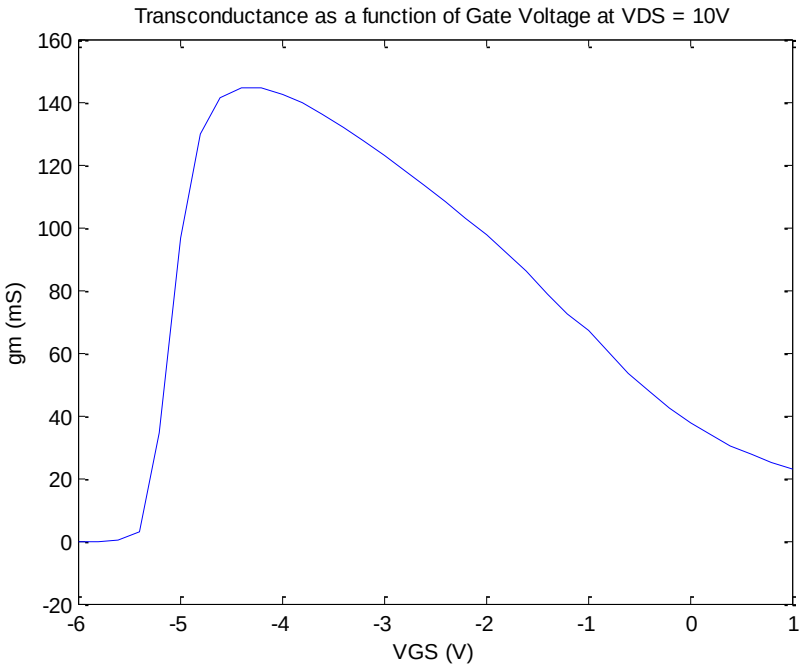
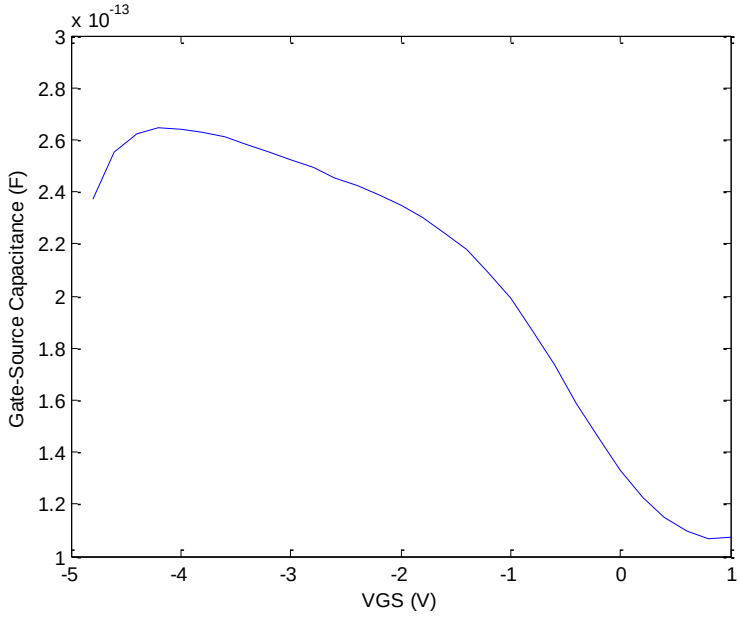
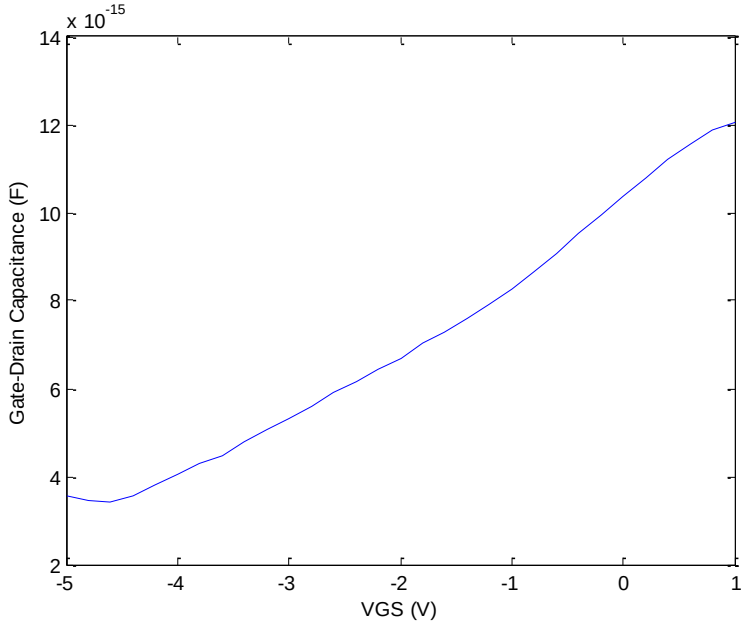


Figure 6.3. Small-signal model transconductance vs. gate voltage.

The behavior of the gate-source capacitance and the drain source capacitance for the same values of gate voltage are shown in Figure 6.4.



(a)



(b)

Figure 6.4. Small-signal model (a) gate-source capacitance vs. gate voltage and (b) gate-drain capacitance vs. gate voltage.

The drain admittance of the small signal model is plotted as a function of drain voltage in Figure 6.5.

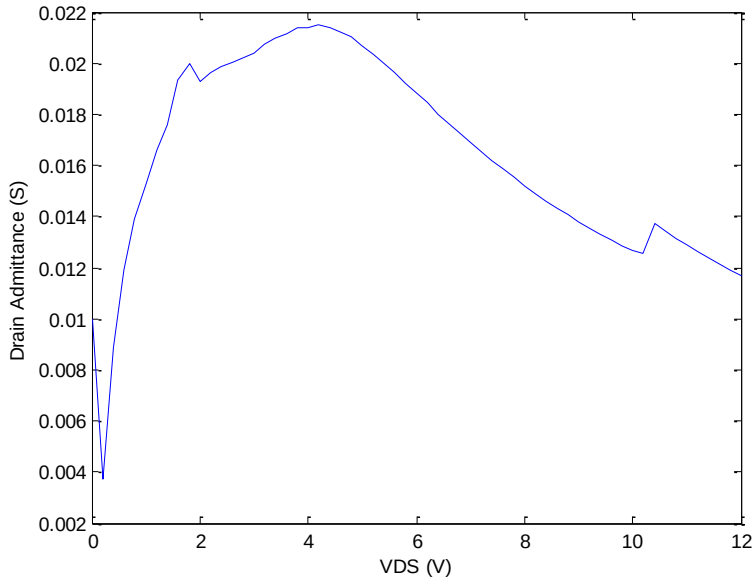


Figure 6.5. Small-signal model drain admittance vs. drain voltage.

6.3 DC Behavior Modeling

The most crucial aspect of the large-signal model is the correct modeling of the gate and drain dependence of the VCCS. This component determines the drain admittance (gd) and the transconductance (gm). The equation for the drain current in the VCCS for the Angelov model in ADS using the default setting is given by (6.7) [43]. When possible, the parameter names are chosen to coincide with the names used by ADS in order to avoid confusion.

$$\mathrm{Ids} = \mathrm{Ipk0}\ \times (1 + \tanh(\Psi)) \times \tanh(\alpha\,\mathrm{Vds})) \times (1 + \mathrm{Lambda} \times \mathrm{Vds}) \qquad (6.7)$$

In this equation, both α and Ψ depend on the gate voltage. Lambda (λ) is the channel length modulation parameter. The equation for Ψ is the following polynomial:

$$\Psi = \mathrm{P1}\ \times (\mathrm{Vgs} - \mathrm{Vpkm}) + \mathrm{P2}\ \times (\mathrm{Vgs} - \mathrm{Vpkm})^2\ + \mathrm{P3} \times (\mathrm{Vgs} - \mathrm{Vpkm})^3 \qquad (6.8)$$

In this equation P1, P2, and P3 are polynomial coefficients, and Vpkm is the gate voltage for maximum transconductance. The equation for α is give in (6.9).

$$\alpha = \text{AlphaR} + \text{AlphaS} \times (1 + \tanh(\Psi)) \quad (6.9)$$

AlphaR and AlphaS combine to produce the saturation voltage parameter. Because the devices being investigated dissipate significant power during operation, the effects of self heating also needed to be addressed. The thermal effects are discussed in greater detail in a later section, but in order to produce the DC model certain aspects of self heating effects must be discussed now because their effects are so pronounced in the current models. The equation used to model thermal effects on current is given in (6.10) [47].

$$\text{Ipk0}' = \text{IPK0} \times (1 + \text{TCIPK0} \times (\text{Temp} - \text{Tnom})) \quad (6.10)$$

or

$$\text{Ipk0}' = \text{IPK0} \times (1 + \text{TCIPK0} \times \Delta\text{T}) \quad (6.11)$$

TCIPK0 is a scaling factor that increases (or decreases) the drain current with changes in temperature. Tnom is the nominal temperature, which for this research is 25 °C. The change in temperature due to self heating is shown below [48]:

$$\Delta\text{T} = \text{R}_{\text{th}}\,\text{P}_{\text{diss}} \quad (6.12)$$

where P_{diss} is the dissipated power (determined by multiplying the drain current and the drain voltage) and R_{th} is the thermal resistance. In the absence of substantial gate current or incident RF power, the power dissipated is the product of the drain current and the drain voltage. The thermal capacitance is a parameter that when multiplied with the thermal resistance produces the thermal time constant. Typically, the thermal time constant is on the order of a fraction of a millisecond. This is a very short time constant from the perspective of DC and a very long time constant from the perspective of the

frequency of the RF voltage oscillation incident on the gate. From the DC perspective, the equation for the non-transcendental drain current that accounts for self heating is derived below:

$$\mathrm{IDS} = \mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS}, \mathrm{VDS}) \times (1 + \mathrm{TCIPK0} \times \Delta\mathrm{T}) \tag{6.13}$$

$$\mathrm{IDS} = \mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS}, \mathrm{VDS}) \times (1 + \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{IDS} \times \mathrm{VDS})$$

$$\frac{\mathrm{IDS}}{\mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS},\mathrm{VDS})} = (1 + \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{IDS} \times \mathrm{VDS})$$

$$\frac{\mathrm{IDS}}{\mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS},\mathrm{VDS})} = (1 + \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{IDS} \times \mathrm{VDS})$$

$$\frac{\mathrm{IDS}}{\mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS},\mathrm{VDS})} - \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{IDS} \times \mathrm{VDS} = 1$$

$$\mathrm{IDS} \times \left(\frac{1}{\mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS},\mathrm{VDS})} - \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{VDS}\right) = 1$$

$$\mathrm{IDS} = \left(\frac{1}{\mathrm{IPK0} \times \mathfrak{F}(\mathrm{VGS},\mathrm{VDS})} - \mathrm{TCIPK0} \times \mathrm{Rth} \times \mathrm{VDS}\right)^{-1} \tag{6.14}$$

Using equation (6.7–6.14) with the proper equivalent circuit model parameters, we can recreate the current behavior of the DUT. The goal of the model extraction process is to determine the value of these parameters that will do an effective job of recreating that current behavior.

The drain current model extraction begins by importing the measured current and voltage from a recorded file into the program's work space. The voltage sweeps (VDS and VGS) become one-dimensional vectors, and the current becomes a two-dimensional matrix. The voltage drop across the extrinsic parasitic resistors is de-embedded from the

current to produce the I-V characteristics of the intrinsic device. A plot comparing the I-V behavior before and after this de-embeding process is shown in Figure 6.6.

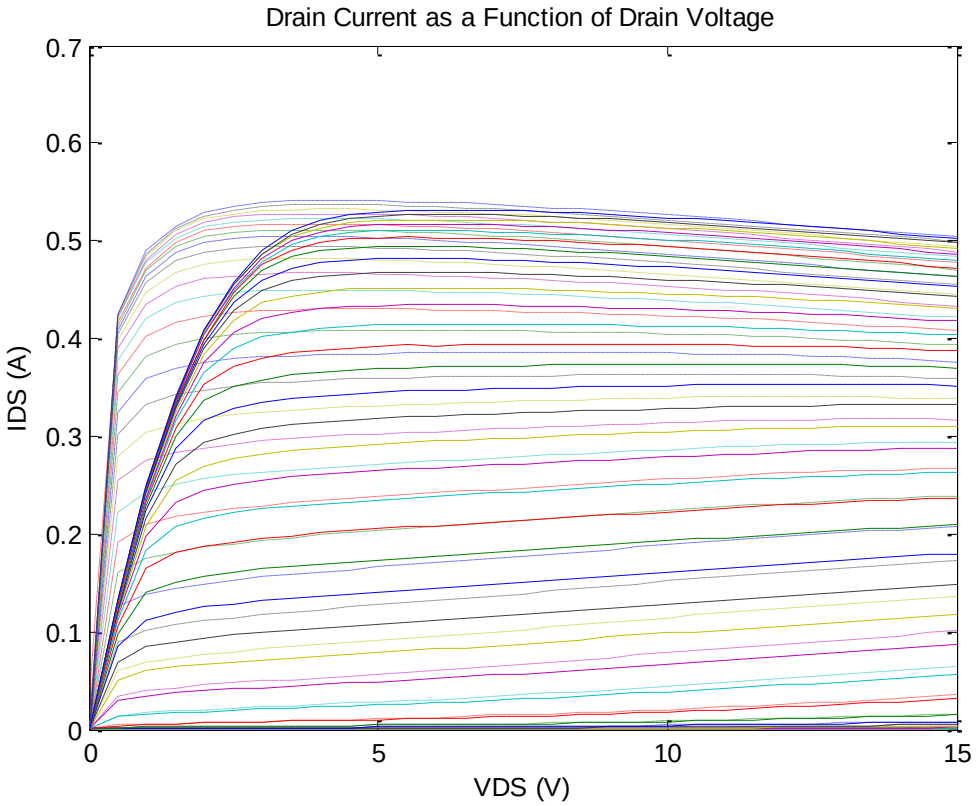
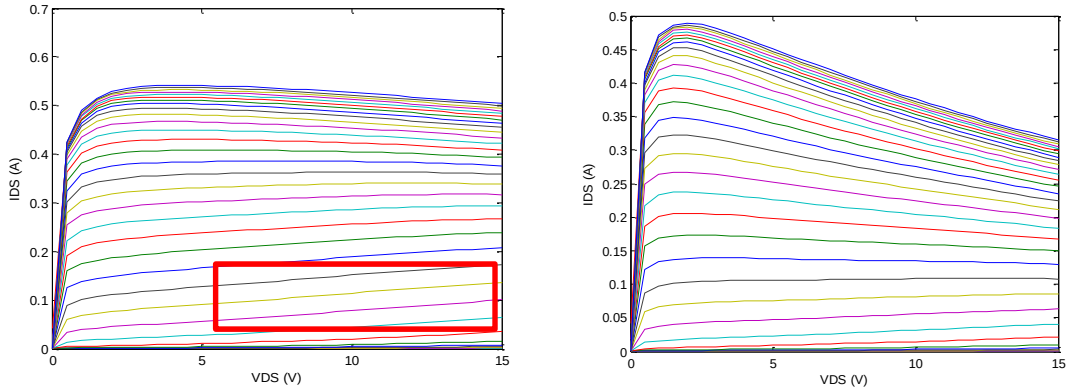


Figure 6.6. Comparison of intrinsic (dotted line) and extrinsic (solid line) I-V device behavior before and after parasitic resistances are removed.

Once the data for the intrinsic device is determined, it is possible to begin extracting the model parameters.

The first parameter to be determined is the channel length modulation parameter (lambda or λ). This parameter can be directly extracted by examining the region in which the current behavior is dominated by λ. This is the portion of the saturation region where self heating is negligible. Figure 6.7 shows this part of the I-V curve. The calculation for λ is shown in (6.15):

$$\lambda = \frac{\Delta IDS}{IDS \times \Delta VDS} \tag{6.15}$$



(a) (b)

Figure 6.7. (a) I-V behavior of the GaN HEMT with the region used to determine channel length modulation parameter outlined in the red box and (b) the intrinsic I-V curve with channel length modulation parameter removed

A similar technique is used to determine the thermal resistance. TCIPK0 can be determined by comparing the I-V behavior of a device at several different temperatures. Once the gate modulation parameter is known, its effect on the current can be calculated out. A plot of the I-V curve with the effects of the channel length modulation parameter mathematically removed is shown in Figure 6.7(b). The first order approximation of the thermal resistance over a small change in current is given in (6.16):

$$\text{Rth} = \frac{\Delta\text{IDS}}{\text{IDS}\times\Delta\text{VDS}\times\text{TCIPK0}} \tag{6.16}$$

Channel length modulation effects and self heating effects can be isolated and mathematically removed from the current behavior of the DUT. A plot of the current after the removal of these components of the drain current behavior is shown in Figure 6.8.

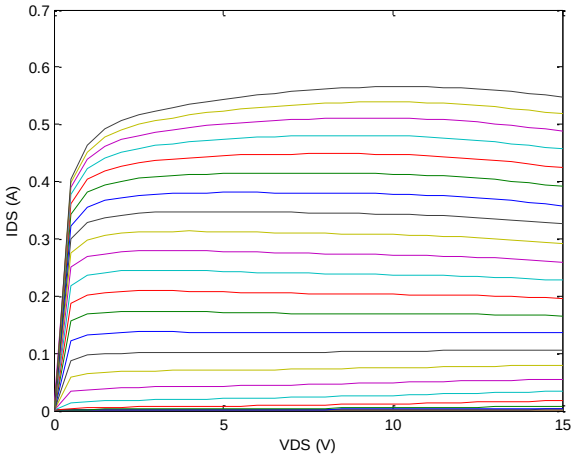


Figure 6.8. (a) I-V behavior of the GaN HEMT with the channel length modulation parameter effects and self heating effects mathematically removed.

Using this data and (6.7), it is possible to determine IPK0 by setting it equal to one half of the maximum of peak IDS. Vpkm is the gate voltage at which there is a maximum transconductance. To determine Dvpks, the transconductance at two separate drain voltages is compared to determine the change in peak transconductance across the ohmic region.

The process to determine the polynomial coefficients, P1, P2, and P3, begins by examining the drain current as a function of gate voltage in the saturation region of the device. A plot of this is shown in Figure 6.9.

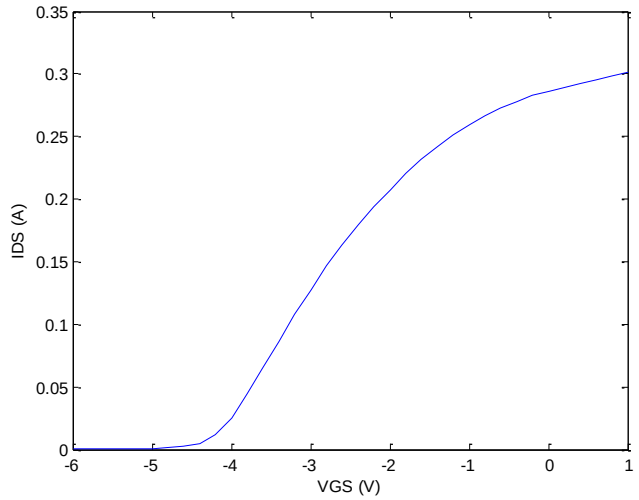


Figure 6.9. Plot of drain current as a function of gate voltage at 10 V VDS.

This is value is normalized to unity, and the arc tangent of this number is determined. This produces a curve that is nominally the value Ψ in (6.7). To determine the polynomial coefficient a third order polynomial fit is applied to the raw data. This can also be optimized to produce a close fit between the measured and modeled data.

A comparison showing the extracted and modeled Ψ is shown in Figure 6.10.

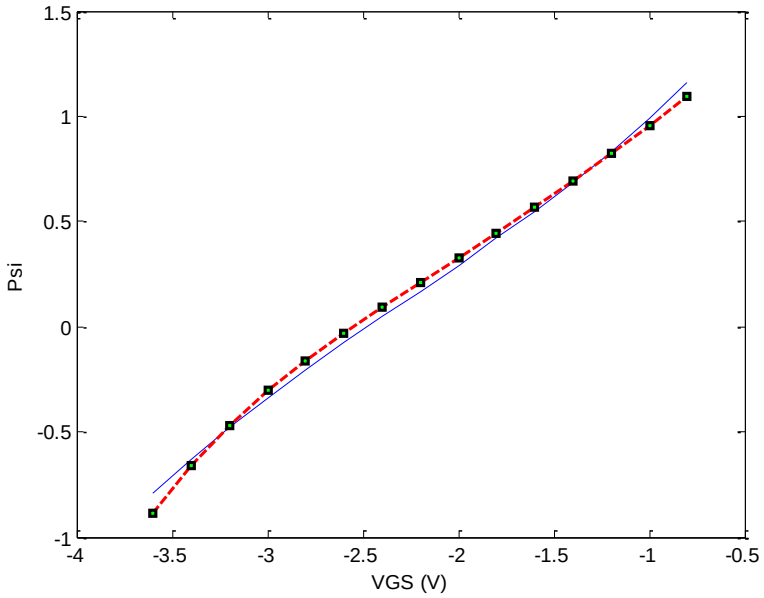


Figure 6.10. Comparison of measured (red line with green markers) and modeled psi, which is the arctangent of the normalized drain current vs. gate voltage.

After determining the polynomial coefficients, the saturation region of the model is completed. In order to characterize the ohmic region, we need to determine AlphaR and AlphaS. Prior to this, we need to determine α, which is a function of AlphaS, AlphaR, VDS, and VGS. The equation for α is given by (6.17):

$$\alpha = \text{arcTanh}\left(\frac{\text{IDS}_{\text{norm}}}{\text{VDS}}\right) \tag{6.17}$$

where IDS_{norm} is the normalized drain current. The default assumption is that the dominant component of α is in AlphaS. Based on this assumption, the equation for AlphaS is given by (6.18):

$$\text{AlphaS} = \frac{\alpha}{(1+\tanh(\Psi))} \tag{6.18}$$

The remaining component of α not represented in AlphaS is the remaining gate voltage-independent component of α, which is AlphaR. The equation for the direct extraction is given in (6.19):

$$\text{AlphaR} = \alpha - \text{AlphaS}\,(1 + \tanh(\Psi)) \tag{6.19}$$

At this point, the full set of drain current parameters have been determined. The modeled drain current is calculated, and the parameters are optimized against the measured data until the error between the two values is minimized. Figure 6.11 shows the measured and modeled drain current after the optimization routine. The data shown in Figure 6.11 is of the total device, including extrinsic parasitic resistances.

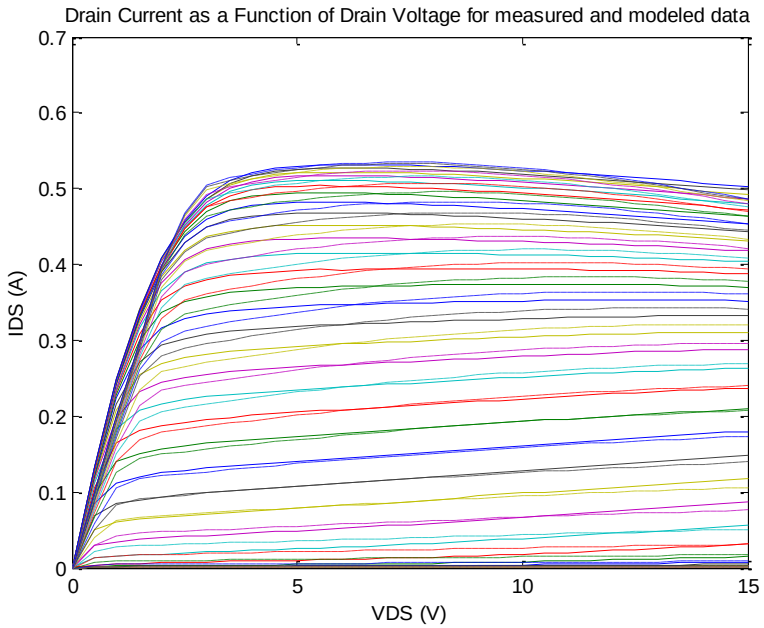


Figure 6.11. Drain current comparison of measure (solid lines) and model (dashed lines).

As can be seen in Figure 6.11, this procedure, followed by selective component optimization, can provide very close agreement between the measured and modeled values.

A final optimization is performed to reduce the discrepancy between the measured RF transconductance, which has been extracted from the small-signal models, and the RF transconductance of the modeled device. The thermal time constant of these devices has been determined to be on the order of milliseconds. From the perspective of the DC measurement, this is a very short time and the self heating effects can be considered to be instantaneous. From the perspective of the RF signal, this is a very long time and for small signals the self heating effects can be considered to be unchanged from the bias conditions.

An optimization is run to simultaneously minimize the difference between measured and modeled data for the RF transconductance and the drain current. A

comparison of the final measured and model RF transconductance is shown in Figure 6.12.

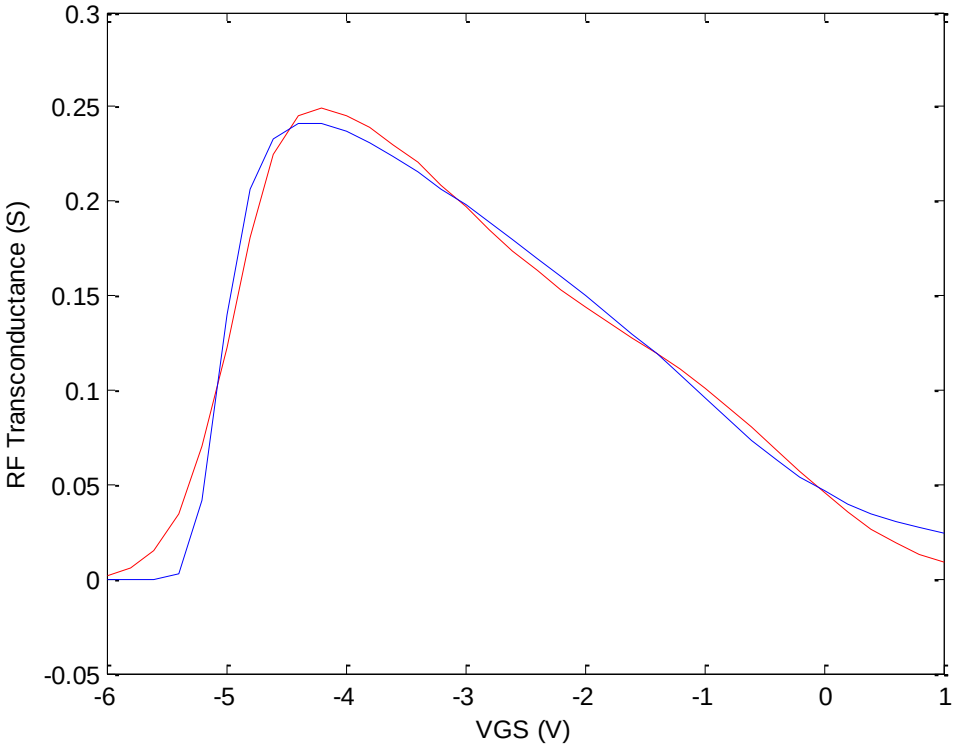


Figure 6.12. RF transconductance comparison of measure (blue solid) and model (red dashed).

6.4 Reactive Large-Signal Components

Once the DC behavior of the device is determined, the next step in producing the large-signal model of the device involves determining the intrinsic component parameters. These are in addition to the extrinsic parasitic components whose extraction was described in chapter 5. The intrinsic parasitic components can be separated into two separate categories. These are the fixed value components and the voltage-dependent components. In Figure 6.1, the voltage-dependent components are represent with arrows through them. For the Angelov Model as implemented in Agilent ADS, the only voltage-dependent components are the gate-drain capacitor (Cgd) and the gate-source capacitor

(Cgs). These are the capacitors associated with the gate diodes. The equations for the capacitances are given by (6.20) and (6.21) [43]:

$$\mathrm{Cgs} = \mathrm{Cgspi} + \mathrm{Cgs0} \times (1 + \tanh(\mathrm{Phi1}) \times (1 + \tanh(\mathrm{Phi2}) \quad (6.20)$$

$$\mathrm{Cgd} = \mathrm{Cgspi} + \mathrm{Cgs0} \times (1 + \tanh(\mathrm{Phi3}) \times (1 + \tanh(\mathrm{Phi4}) \quad (6.21)$$

The phi terms are defined as follows:

$$\mathrm{Phi1} = \mathrm{P10} + \mathrm{P11} \times \mathrm{Vgsc} \quad (6.22)$$

$$\mathrm{Phi2} = \mathrm{P20} + \mathrm{P21} \times \mathrm{Vds} \quad (6.23)$$

$$\mathrm{Phi3} = \mathrm{P30} + \mathrm{P31} \times \mathrm{Vds} \quad (6.24)$$

$$\mathrm{Phi4} = \mathrm{P40} + \mathrm{P41} \times \mathrm{Vgdc} \quad (6.25)$$

In these equations, Vgsc and Vgdc refer to the voltages across the capacitors.

Determining the fixed components is accomplished by selecting a range of biases over which the device is expected to operate and analyzing the small-signal models. Models whose error is below one standard deviation above the median are used. The fixed component values of these components are averaged and used as the extracted value for the fixed component. Later, all values are optimized.

A start value for Cgs and Cgd are also extracted in this manner; however, these components are expected to vary as the gate voltage and drain voltage change. The DC model allows the transconductance and the drain admittance to be calculated. The fixed component values for the intrinsic and extrinsic components have already been determined. An optimization routine was run to minimize the error between the measured

and calculated S-parameters. In this optimization, the only parameters allowed to vary are the diode capacitances. This calculation provides matrices of how the variable capacitances change with voltage. Figure 6.13 show the calculated values of how the gate-source capacitance changes with changes to the gate voltage.

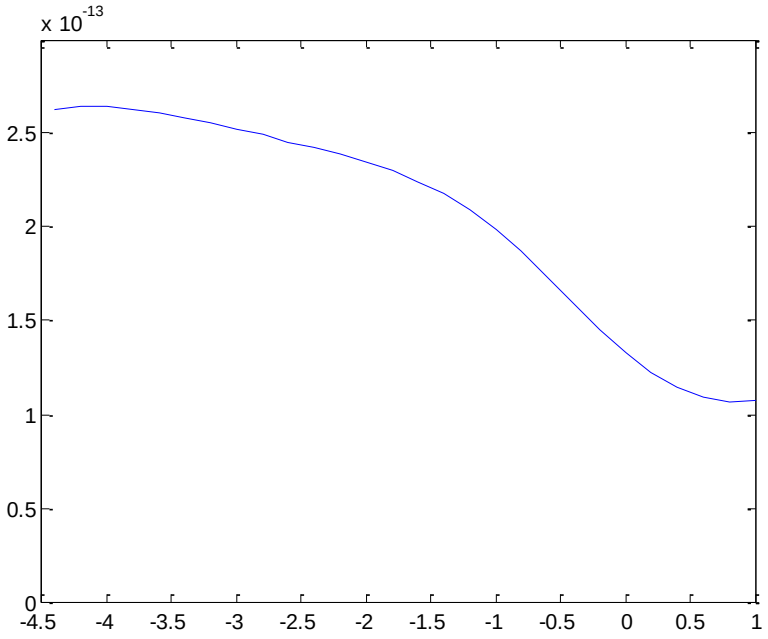


Figure 6.13. Extracted gate-source capacitance vs. gate voltage.

Using this data, we can determine the parameters that make up Phi1, i.e., P10 and P11. To start with Cgs0 is determined to be one half of the difference between the maximum and minimum of the capacitance. Cgspi is simply the minimum capacitance. The next step is to normalize the capacitance by subtracting the Cpspi from the measured data, dividing by Cgs0, and subtracting unity. The arc hyperbolic tangent of this is the term Phi1 from our equation for Cgs. Mathematically this is shown in (6.26):

$$\text{Phi1} = \text{arctanh}\left(\frac{\text{Cgs}-\text{Cgspi}}{\text{Cgs0}} - 1\right) \tag{6.26}$$

A plot of Phi1 is shown in Figure 6.14. It can be seen in (6.22) that Phi1 is allowed to be a polynomial of degree one. The data shown in Figure 6.14 can be seen to be a function of higher polynomial, but the best fit using the current model is used.

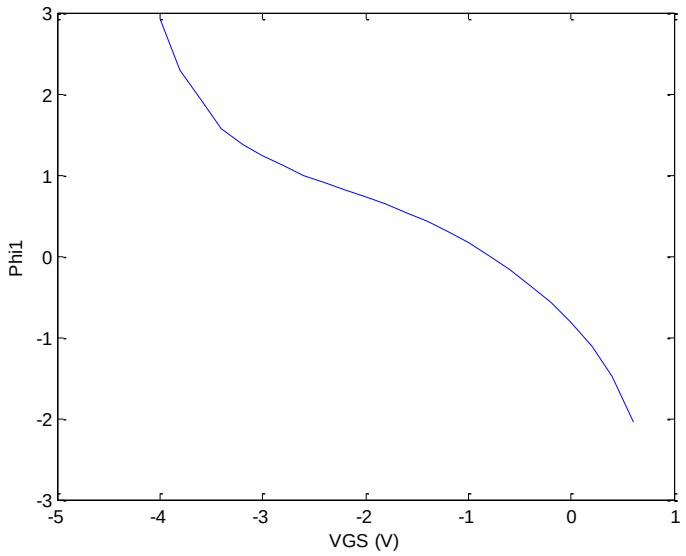


Figure 6.14. Small-signal model gate-source capacitance vs. gate voltage.

The measured and calculated gate-source capacitance is shown in Figure 6.15. The measured data is shown with a solid blue line and the modeled data is shown with a dashed green line.

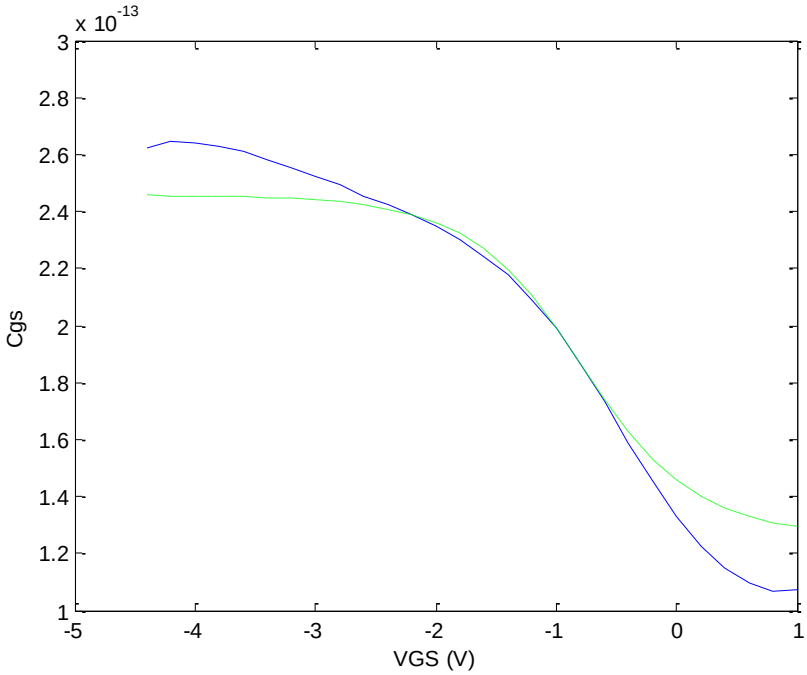


Figure 6.15. Comparison of measured (solid) and modeled (dashed) gate-source capacitance as a function of gate voltage.

This procedure is repeated for Phi2, P20, and P21 to determine the dependence of the gate capacitance on the drain voltage. A similar algorithm is used to extract P30, P31, P40, and P41 for the gate-drain capacitor.

6.5 Final Re-optimization

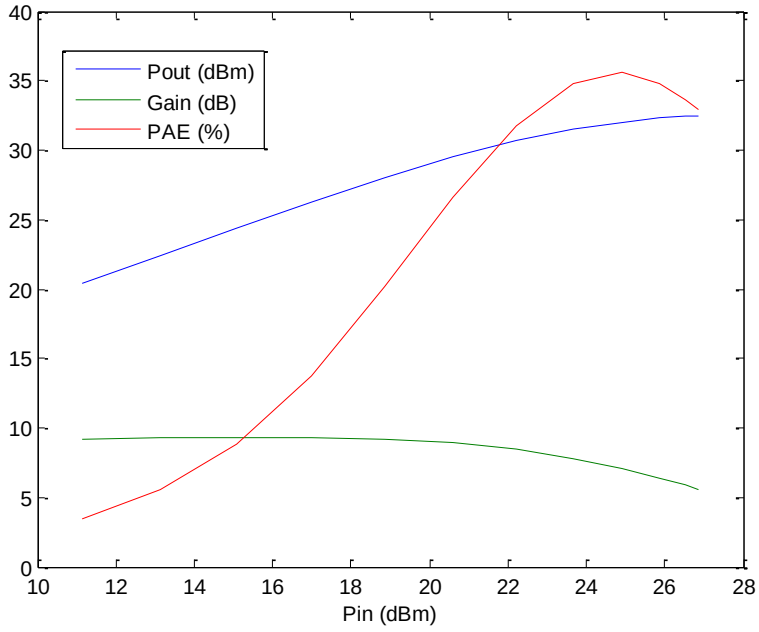
At this point in the model development, an extraction procedure has been use to determine a value of each component parameter used in the large-signal model. At least one optimization routine has been run for each component value to minimize the difference between the measured and modeled S-parameters. A final optimization is run on all component values.

The measured S-parameters of the gate voltage sweep and the drain voltage sweep are stored in two four-dimensional matrices. The dimensions of these matrices are

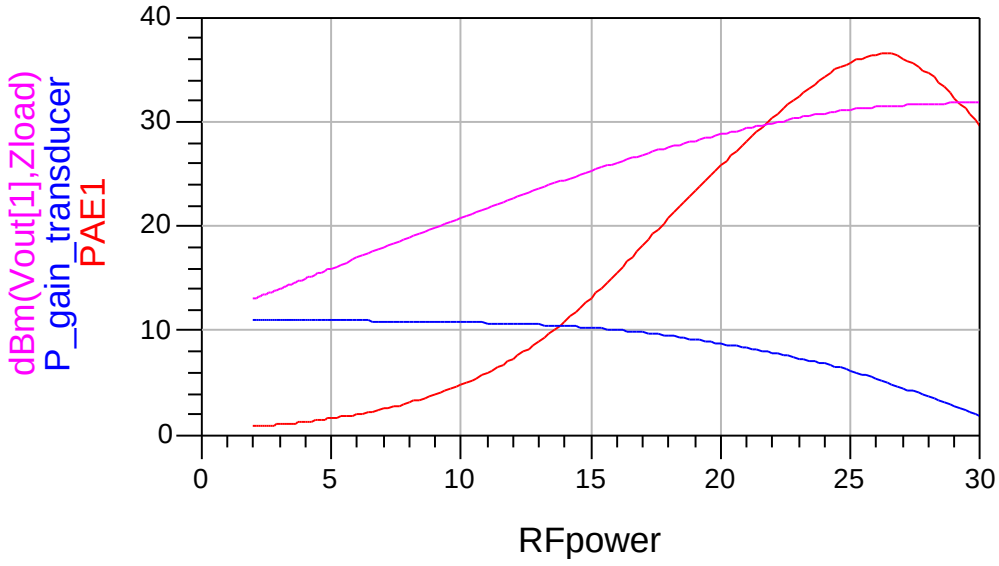
frequency, S-parameter (s11, s21, s12, and s22), gate voltage, and drain voltage. A final optimization is run to simultaneously minimize the error between the measured data of both of these matrices and the data produced by the now complete large-signal model.

6.6 Simulation of a Large-Signal Model Using Computer Aided Design Tools

Scattering parameters have been used extensively to generate the large-signal model of the device at this point. However, scattering parameters assume linear behavior, and the utility of the large-signal model comes from its ability to predict nonlinear behavior. The results of a power sweep measurement from the device in Figure 4.2 are shown for comparison in Figure 6.16(a). The large-signal model produced by the procedure described in this chapter was used to simulate the device performance at the input impedance (12.28 + 6.91j Ω) and output impedance (16.16 + 32.31j Ω) at which the original measurement was made. The simulation was performed using the Agilent ADS program from which the large-signal model was taken. The simulated performance of the device is shown in Figure 6.16(b).



(a)



(b)

Figure 6.16. Comparison of a 500-µm GaN HEMT (a) power sweep performance compared to the (b) the Harmonic Balance simulation of the large-signal model of the same device simulated in Agilent ADS.

As can be seen the large-signal model does a reasonable good job at reproducing the behavior of the device. The model has a gain that is ~0.6 dB greater than the measured data, but this can be explained by unexpected losses in the power measurement that were not accounted for in the calibration. With an accurate large-signal model, MMICs that make use of the device can be designed.

Chapter 7: Thermal Effects on Device Performance

The degradation analysis procedure that was used to characterize physical changes to the device while it is being stressed involves making measurements at several different temperatures and comparing them against each other. For these comparisons to be meaningful, the effects of changes in temperature on device performance must be well understood. This chapter describes the observed effects of temperature on a device. Three separate large-signal model measurement sequences were done on at three separate temperatures in the reliability experiment: 25, 75, and 125 °C. The effects of elevated base plate temperature on the device behavior were observed and recorded.

The negative conductance at increasing voltage has already been mentioned when it was needed to model this effect caused by self heating. The same behavior is observed when the temperature of the base plate on which the DUT is mounted is increased. Current is a product of the carrier and velocity. For the HEMT, these parameters become sheet charge density and electron velocity, which can be written as [50]

$$\mathrm{Ids(T)} \propto \mathrm{N_{sheet}(T)}\ \nu_s\mathrm{(T)} \tag{7.1}$$

where N_{sheet} is the sheet charge density and ν_s is the saturation carrier velocity. The temperature dependence of both terms contributes to the change in current as temperature changes. Some references claim that the dominant term is saturation velocity [51]. As the device temperature increases, the phonon density increases [52]. The increased phonon density results in an increase frequency of scattering events between the channel electrons and the phonons, which reduces the carrier velocity and the current. Other authors have conclude that change in sheet charge density makes a larger contribution to

the total current change [50, 53]. This conclusion has been corroborated through Monte Carlo simulation and measured data. This result is largely due to the effect of the temperature on semiconductor bandgaps. The total temperature coefficient can be thought to be a sum of the temperature coefficient from the saturation velocity and the temperature coefficient from the two-dimensional electron gas sheet density. This is represented mathematically in (7.2) [50]:

$$\mathrm{TC}_{\mathrm{Ids}} = \mathrm{TC}_{\mathrm{Nsheet}} + \mathrm{TC}_{\mathrm{vs}} \tag{7.2}$$

According to the version of the Angelov model implemented in Agilent's ADS, the parameters that change within the model as a function of temperature include the drain current (IPK0), the first order polynomial coefficient for the gate parameter (P1), and the gate capacitances. The equations for the thermal effects on these parameters are shown below [43]:

$$\mathrm{Ipk0} = \mathrm{IPK0} \times (1 + \mathrm{TCIPK0} \times (\mathrm{Temp} - \mathrm{Tnom})) \tag{7.3}$$

$$\mathrm{P1} = \mathrm{P1} \times (1 + \mathrm{TCP1} \times (\mathrm{Temp} - \mathrm{Tnom})) \tag{7.4}$$

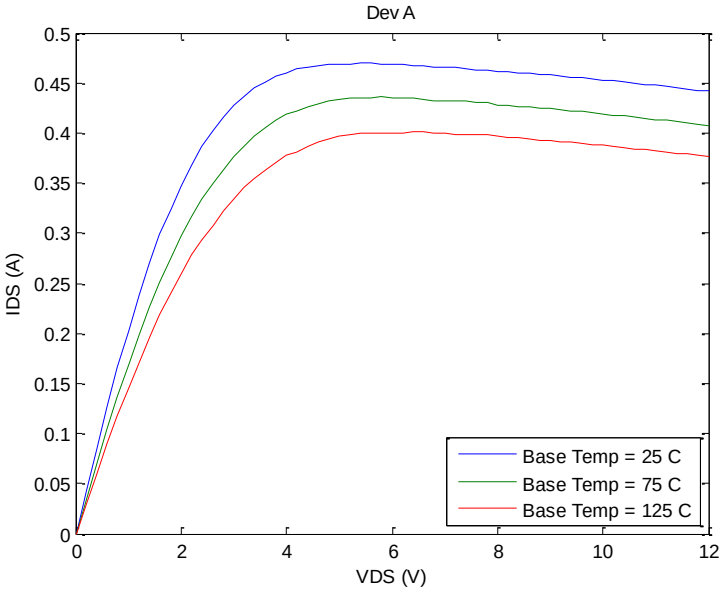
$$\mathrm{Cgs0} = \mathrm{CGS0} \times (1 + \mathrm{TCGS0} \times (\mathrm{Temp} - \mathrm{Tnom})) \tag{7.5}$$

$$\mathrm{Cgd0} = \mathrm{CGD0} \times (1 + \mathrm{TCGD0} \times (\mathrm{Temp} - \mathrm{Tnom})) \tag{7.6}$$

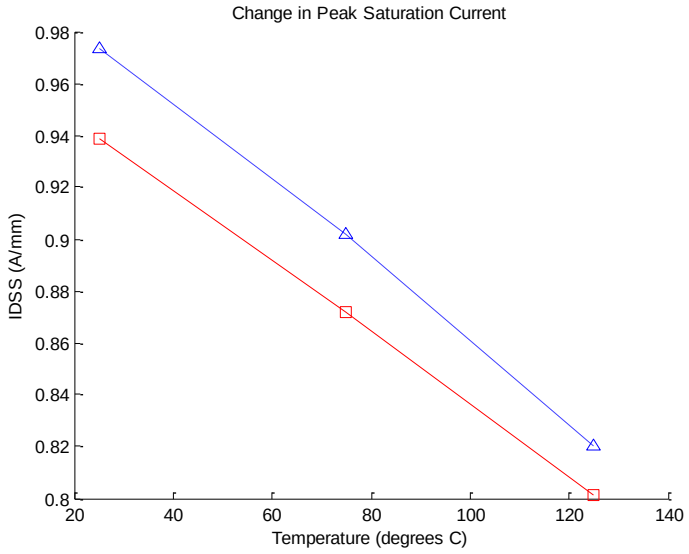
The temperature constants are the parameters that begin with TC. Temp is the base plate temperature. For all these equations, the nominal base plate temperature (Tnom) is 25 °C. In these equations, the parameter in capital letters is the default nominal temperature value, and the parameter to the left of the equal sign is the value modified by the temperature change.

7.1 Observed DC Behavior Caused by Elevated temperature

The drain current temperature coefficient was calculated by comparing the drain current at different temperatures. Figure 7.1 show the drain current with a gate voltage set at 0 V for the 500-µm GaN HEMT measure at 25, 75, and 125 °C.



(a)



(b)

Figure 7.1. Temperature behavior of drain current for a 500-µm GaN HEMT (a) saturation drain current plotted across a range of temperatures and (b) peak Idss as a function of temperature.

To calculate the current temperature constant, the current is normalized by dividing all the currents by the current at the nominal temperature. Then the currents are subtracted from each other. This method allows the fractional change in current per degree to be calculated. The equation for this is

$$\mathrm{TCIPK0} = \frac{\mathrm{IDS}_{\mathrm{Temp}} - \mathrm{IDS}_{\mathrm{Tnom}}}{\mathrm{IDS}_{\mathrm{Tnom}} \times (\mathrm{Temp} - \mathrm{Tnom})} \tag{7.7}$$

For the device shown in 7.1(a), the TCIPK0 was determined to be -0.00144/°C.

Figure 7.1(b) is a plot of the change in saturation current per millimeter as a function of base plate temperature. Device A is a device that has been through a full three-day multi-temperature stress process. Device B is a fresh, unstressed device. The change in TCIPK0 between the stressed device and the fresh device was less than 6%. This is much less than the reported standard deviation between devices [50]. Based on this datum, the change in temperature constant due to stress was determined to be statistically insignificant.

Some authors have reported a change in pinch-off voltage as a function of temperature. This leads to a zero-temperature coefficient (ZTC) point on the gate voltage sweep. At the zero-temperature-coefficient, the drain current does not change with temperature. This point is often conveniently located near the peak gain for the device and can be selected by engineers as an optimal bias point for [50]. This reported phenomenon was not observed in the device used in these experiments. Figure 7.2 is a plot of the drain current at the three different temperatures with the drain voltage set at 10 V while the gate voltage is swept from pinch off to forward bias.

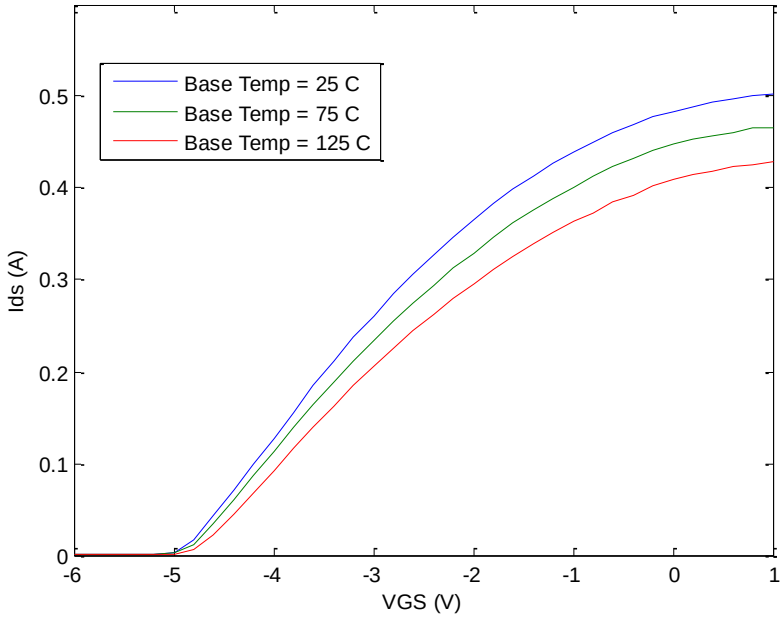


Figure 7.2. Temperature behavior of drain current for a 500-µm GaN HEMT as a function of gate voltage.

The pinch-off voltage remains constant as temperature changes for the devices investigated in this research.

The effect on transconductance due to temperature is also determined by TCIPK0. Figure 7.3 shows how the RF transconductance changes with temperature. A calculation similar to the one show in (7.7) was performed to determine a TCIPK0 for the RF transconductance. The results showed that temperature dependence for the RF transconductance was slightly higher than that of the drain current.

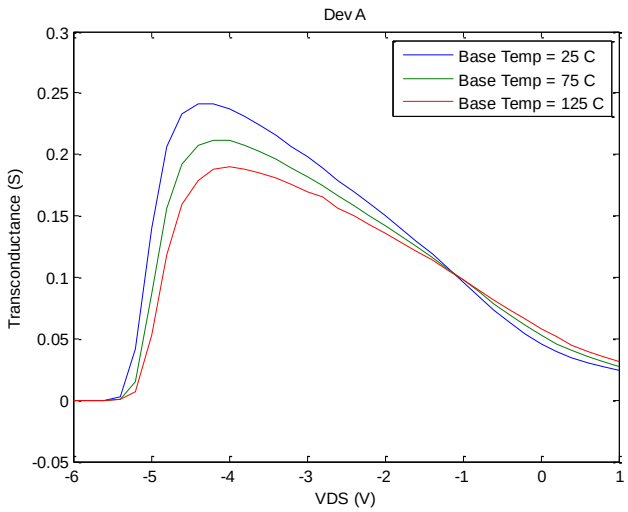


Figure 7.3. Temperature behavior of RF transconductance for a 500-µm GaN HEMT as a function of gate voltage.

A transconductance zero-temperature coefficient (gm ZTC) is clearly visible on this plot; however, this point is far from the peak transconductance. The gm ZTC bias point is at a gate bias that draws a large current. From an amplifier design perspective, high current and low gain are undesirable attributes for a microwave amplifier. As a result, the gm ZTC would be of little interest to device designers.

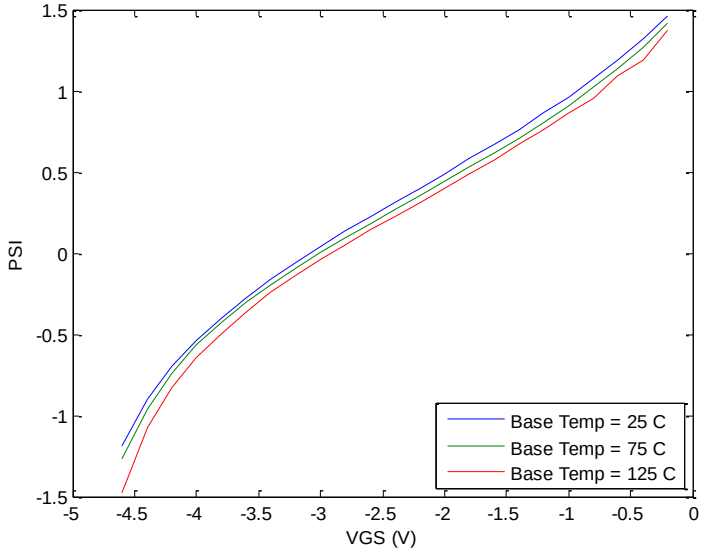


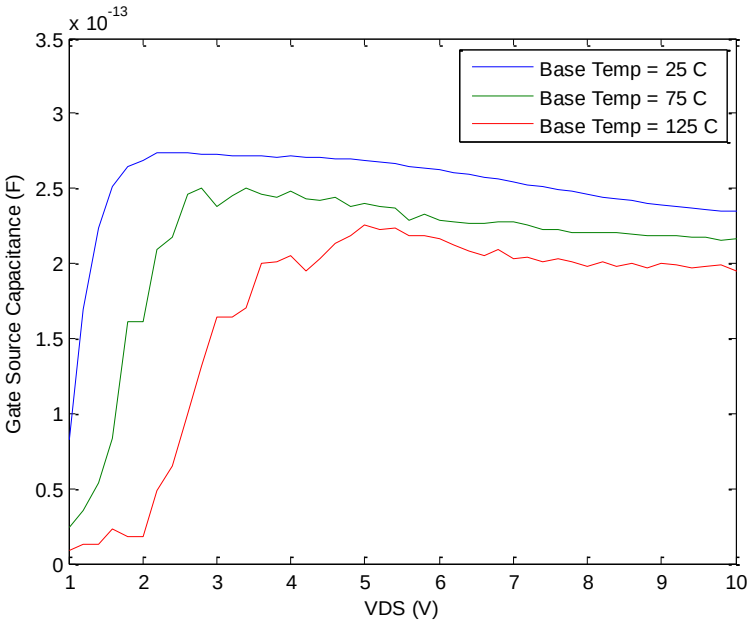
Figure 7.4. Temperature behavior of arctangent of the normalized drain current (Ψ) for a 500-µm GaN HEMT as a function of gate voltage.

The other temperature dependent parameter that affects current is the first order polynomial component for the equation parameter Ψ, which was described in chapter 6. The plot of Ψ can be seen in Figure 7.4. Curve of Ψ for each of the three separate temperatures is almost exactly the same. The only difference is a slight shift in voltage. The temperature-dependent component of Ψ is P1, which determines the slope of the curve. It is possible to confirm visually and mathematically that the slope of these curves does not change when temperature changes, and therefore, TCP1 was considered to be zero for the models used in this research.

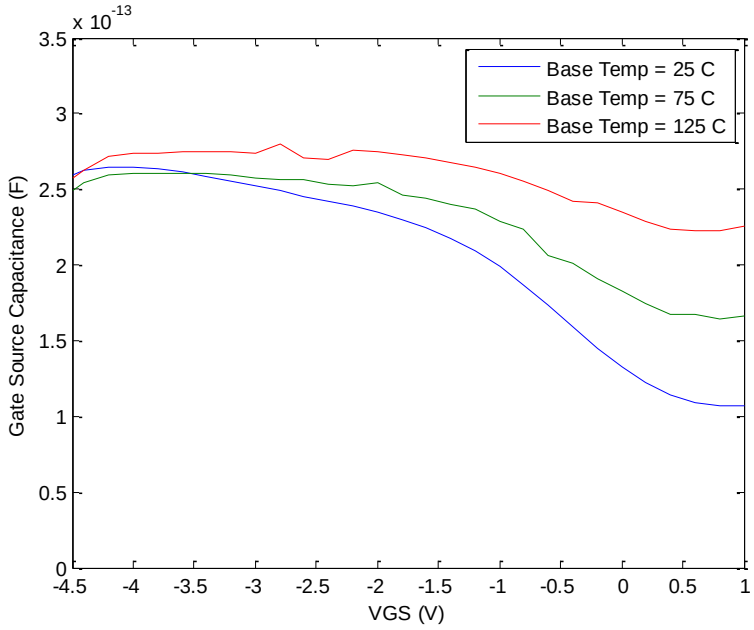
7.2 Dependence of Capacitance on Temperature

Temperature influences a number of components that affect capacitance. These include the changes to the bandgap structure of the semiconductors, stresses on the heterostructure interface, and population of carriers in the energy bands. Similarly to the manner in which different factors combine to create a single temperature coefficient for drain current, the different factors influencing capacitance can be combined into a single capacitance temperature coefficient for each the capacitors associated with the gate diodes. These are the voltage controlled capacitors from the large-signal model (Cgd and Cgs).

Figure 7.5 shows the temperature dependence of the gate-source capacitance.



(a)



(b)

Figure 7.5. Temperature behavior of the gate-source capacitance as a function of (a) drain voltage and (b) gate voltage.

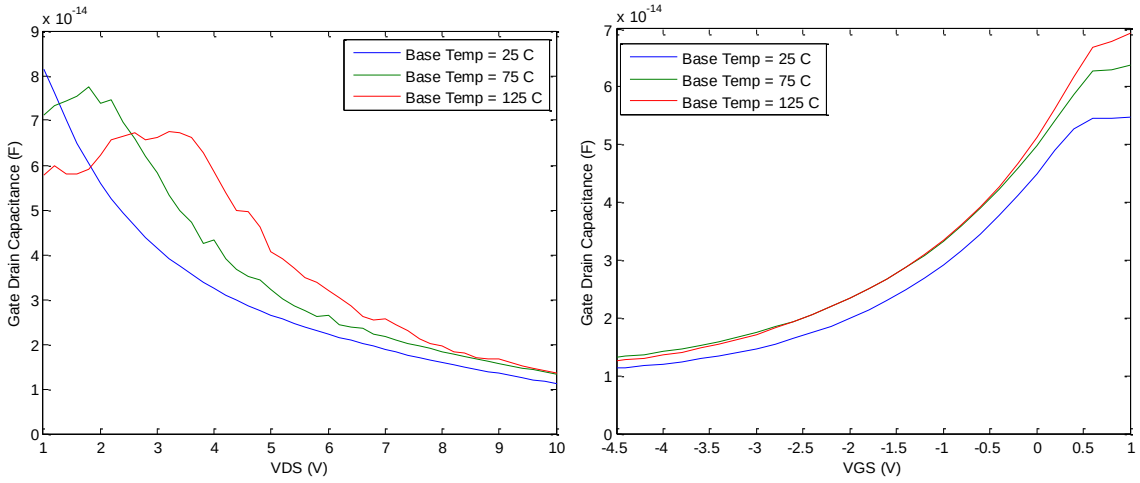
In figure 7.5(a), the gate-source capacitance as a function of drain voltage is plotted for the three temperatures at which the device was measured. A transition between two capacitance values is clearly visible in the ohmic region while the device moves into saturation. The transition occurs at different voltages for different temperatures. Once the

device is in saturation, a change in capacitance with temperature can be seen to be approximately evenly spaced. The change in gate-source capacitance with voltage is shown in figure 7.5(b). The capacitor has two separate regions of operation and an even spacing between capacitances by temperature. The equation that was used to determine the gate-source capacitor temperature constant is shown in (7.8):

$$\mathrm{TCGS0} = \frac{\mathrm{CGS0_{Temp}} - \mathrm{CGS0_{Tnom}}}{\mathrm{CGS0_{Tnom}} \times (\mathrm{Temp} - \mathrm{Tnom})} \tag{7.8}$$

This equation was used to calculate TCGS0, which was determined to be -0.00397/°C.

Figure 7.6 shows the gate-drain capacitance as function of (a) gate voltage and (b) drain voltage.



(a) (b)

Figure 7.6. Temperature behavior of the gate-drain capacitance as a function of (a) drain voltage and (b) gate voltage.

The voltage dependence is again visible; however, the temperature dependence of the components is not evenly spaced. There appear to be two separate operating regions. There is one at the nominal temperature and one at the elevated temperature. Because the temperature effects are not well behaved and small in magnitude, the temperature change

for the gate-drain capacitor was not modeled in this experiment. This is does not create a large problem in producing accurate models for one reason. The value of the capacitor and its impedance is much smaller than other equivalent circuit model components.

In this chapter, the changes in device performance that change with temperature were reported and quantified. The component parameters that represent device temperature effects were calculated. With an understanding of how the device performance changes with temperature, it is possible to compare measurements of the same device at different temperatures. This principle makes it possible to diagnose devices at elevated temperatures during the accelerated degradation process.

Chapter 8: Survey of Degradation Mechanisms, Electrical Effects, and Reported Reliability Research

The key goal of the research described in this document is to develop a holistic measurement system and procedure to diagnose degradation mechanisms. In this chapter, the dominant degradation mechanisms that have been reported in the peer reviewed literature are discussed. This discussion allows us to identify the dominant degradation mechanisms when they are observed during the analysis of the data. This chapter considers two topics. The first is the degradation mechanisms that have been observed in GaN HEMTs. The second topic is the current reliability measurements used by industry and being reported in peer-reviewed literature.

8.1 Degradation Mechanisms

Because of the potential shown by GaN HEMTs, a great amount of time and effort by many researchers at diverse organizations around the world have been devoted to the investigation of the fail mechanisms of these devices with the goal of improving their reliability. In order to realize the full potential of this novel wide bandgap material, GaN HEMTs must be operated at electric fields, temperatures, and frequencies to which previous semiconductors would not normally be exposed. This requirement creates previously unseen challenges in reliability. Figure 8.1 shows a graphic summary of some of the degradation mechanisms that occur in HEMTs.

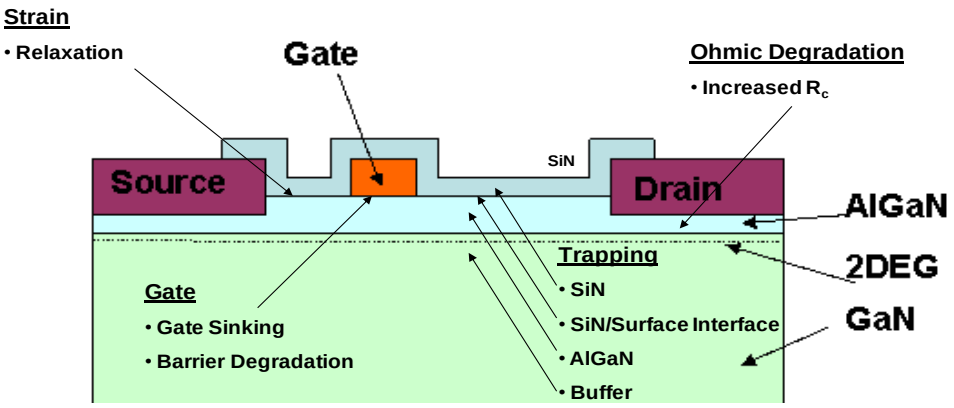


Figure 8.1. Graphic representation of reported degradation mechanisms of AlGaN/GaN HEMTs showing the location in which they occur.

The mechanisms that have been reported for GaN HEMTs can be broken down into three broad categories based on the cause of the degradation: mechanisms caused by hot electrons, mechanisms that are thermally activated, and mechanisms resulting from the piezoelectric properties of GaN and polarization charge at the heterostructure interface [54]. The degradation mechanisms caused by hot electrons are the trap generation in the silicon nitride passivation layer and the trap generation in the AlGaN layer. The thermally activated mechanisms include the delamination of the passivation layer, metal interconnect degradation, and ohmic contact degradation. The trap generation in the GaN bulk is caused by a defect generation resulting from a combination of temperature, strain, and high electric field strength. The physical defect generation at the edge of the gate may be caused by the high electric field strength at the corner of the gate [54]. The defect generation in the gate would be accelerated by temperature.

8.1.1Gate Sinking

One of the phenomena that has been observed in GaAs HEMTs and has caused considerable difficulty to device designers is gate sinking. The term “gate sinking” refers to the intermetallic diffusion of gate material into the wide bandbap material. This

reduces the spacing between the gate metal and the channel [55]. There are a number of reported electrical effects of gate sinking in both GaAs HEMTs and InP HEMTs [56, 55]. These include a decline in current, a decrease in transconductance, and a change in the gate voltage at which the peak transconductance occurs [55]. In some devices, the drain current and transconductance decrease is preceded by a brief interval with a slight increase in current and gain [57]. Researchers who have investigated the possibility of gate sinking as a mechanism for degradation in GaN HEMTs have reported that they have not observed the phenomenon [58].

8.1.2 Hot Electron Effects

In the most general definition, the term "hot electron" refers to electrons that are not in thermal equilibrium with the rest of the crystal lattice. Typically, this is due to acceleration in an electric field. In HEMTs, hot electrons can acquire sufficient kinetic energy from the strong electric field in the vicinity of the gate to move to regions of the device where there is an energy band that would prohibit the presence of electrons that are closer to thermal equilibrium. The interaction of hot electrons in these locations can produce traps and other defects.

Experiments investigating the reliability of GaN HEMTs have reported generation of traps at the AlGaN barrier. Electroluminescence (EL) measurements have been performed on GaN HEMTs in conjunction with reliability measurements. The results of the measurements revealed that the rate of degradation occurred fastest with bias conditions at which the intensity of EL was highest [58]. The researchers' analyses lead them to conclude that the intensity of the illumination measured by EL was a correlated

with the presence of hot electrons. By correlating degradation with the hot electrons, Menegghesso *et al.* concluded that it was the hot electrons that caused the degradation. The reported electrical effects of degradation caused by traps generated from hot electrons was a reduced drain current and reduced transconductance [59].

8.1.3 Thermally Activated Mechanisms

The thermally activated degradation mechanisms are associated with the fabrication process. These are not characteristic of GaN but have been observed in other semiconductor technologies such as Si, SiGe, GaAs, and others. It is much more likely to encounter these degradation mechanisms in a research-quality device or an immature technology than to see these in a commercially viable foundry process.

Because these are precisely the devices that will be seen in novel technologies, it is necessary to be able to identify these defects when they occur. Delamination of the passivation layer has been reported to occur in GaN HEMTs [60]. Its presence can be detected by EL. The creation of this defect is accelerated by current and temperature. In devices with a passivation layer that has not been delaminated and is in proper condition, electron trapping at the surface of the AlGaN states is reduced [61]. The delamination of the passivation layer reverses the benefits gained from passivation in the region between the gate and the drain where the delamination occurs. This creates a virtual gate in this region and reduces channel current and transconductance.

Degradation of ohmic contacts and gate or feed metal interconnect degradation have similar symptoms in their electrical behavior. As these components begin to degrade, their resistance will increase [62]. A frequency dependent component in the resistance

has been reported [62]. This means that the RF resistance may begin to show the degradation while the DC behavior initially remains unchanged.

8.1.4 Piezoelectric and Polar Charge Mechanisms

One of the most widely reported degradation effects is the presence of crystallographic defects in the AlGaN barrier under the gate edge on the side closest to the drain [54, 59, 63-65]. If the failure mechanism is present in the device, the gate edge defect will be triggered when the reverse bias on the gate reaches a certain voltage, called the critical voltage by Joh and del Alamo of MIT [63]. The presence of gate edge defects greatly increases the gate current often by several orders of magnitude.

The presence of this defect after being detected electrically has been confirmed by other measurement techniques [54]. These include deep levels transient spectroscopy (DLTS), which allows the determination of the energy levels traps in the AlGaN. The gate defects have been observed visually in images produced by transmission electron microscopy (TEM) [64]. The physical defect in the gate creates a channel through the AlGaN and, in turn, accelerates trap generation in the AlGaN material. While the physical damage may appear severe, the effect on performance of devices with gate edge defects may only be marginal. The electrical effects of edge defects is an immediate increase in gate current and, over time, a gradual decline in drain current and transconductance.

The other degradation mechanism that may be a product of the polarization charge and piezoelectric effect in GaN is the production of traps and defects in the bulk material. The production of these defect is a result of strain and the rate of production is

accelerated by poor material quality, lattice mismatch, and elevated temperature [66]. These increase scattering and decrease the average channel velocity, resulting in an increase in the channel resistance and a decrease in the drain current [67].

8.2 Reliability Tests

In order to identify the mechanisms previous described researchers have developed a number of measurement procedures. The research covered in this dissertation outlines a new measurement technique that expands on measurements that have been reported. The reported measurement procedures are described below.

8.2.1 DC stress tests

One of the simplest tests that can be applied to a semiconductor device is to determine the device's steady-state I-V behavior. This is typically referred to as a DC measurement. Quite a lot can be determined about a device given only the DC behavior. Some advantages of the DC stress test are that this measurement procedure is the easiest to perform, requires the least amount of preparation, produces data that is less subject to calibration or instrument errors, and requires the least amount of capital measurement equipment. The DC measurement was described in section 4.2.4. The DC stress test consists of applying a bias voltage to the gate and drain and periodically measuring the currents at these terminals of the device. This measurement may be performed at an elevated temperature to accelerate degradation. By combining several of these measurements, a complete Arrhenius Lifetime Measurement (described below) can be conducted. By selecting the bias point, the researcher can attempt to isolate the source of degradation. For example, an experiment in which the device is operated at a high voltage

close to pinch-off would determine if the degradation was caused by strong electric fields. If the device was operated at high current and high voltage, that experiment would determine if a combination of thermal effects and current were the source of degradation. Kim *et al.* verified the effectiveness of SiN passivation by stressing a passivated and unpassivated GaN HEMT at a relatively high voltage (20 V) while pinched off (VGS = -8) [68]. The period of stress was relatively brief, lasting only 12 hours, but this was sufficient to show a radical bifurcation in reliability between the passivated and unpassivated device. The specific bias conditions used allowed the authors to identify the source of degradation as hot electrons.

8.2.2 Step stress

The step stressing measurement procedure was used extensively by Joh and del Alamo at MIT [59, 63, 69]. This is similar to the DC stress test in that it relies on direct current; however, in the step stress measurement, a series of different biases are applied to the device and the current behavior in the DUT is recorded. The data recorded using this procedure shows the transient response of the device and the effect of each marginal increase in electric fields on the current. In some measurements, the devices were allowed to recover to its steady-state behavior. By doing this, the presence of new traps that are more easily populated can be observed in the transient behavior of the DUT [59]. While one could argue that this procedure does not actually measure reliability, it is effective in determining the voltage levels at which the device is permanently altered. Figure 8.2 shows the plots reported by Joh and del Alamo using their step stress test [63].

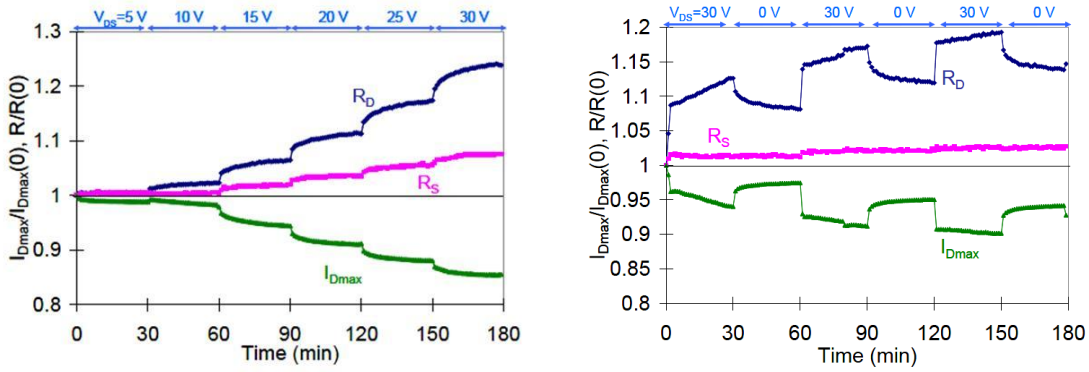


Figure 8.2. Report performance of step stress measurements showing increase to source and drain resistances: (a) incremental step stress and (b) interval stress and recovery test [63].

Using this procedure, the authors were able to determine the critical voltage at which the device first begins to break down. The rate of change in current at a specific voltage can be calculated as well. By examining the transition between the relaxed state and stressed state, the time constant associated with trap occupation can be calculated.

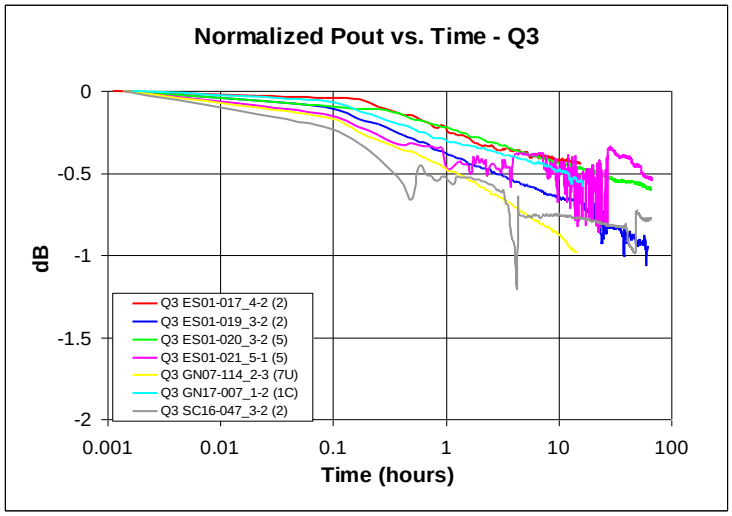
8.5.1 RF Power

The RF reliability power measurement was described in section 4.3 of this document. To review, the input and output power of the device are recorded along with the bias and current conditions of the device. Typically for power devices, the DUT has in input RF power sufficient to drive the device into compression. The drain and gate voltages can be chosen to maximize gain, output power, or efficiency. The experimenter may choose a suboptimal bias point with the goal of reducing degradation.

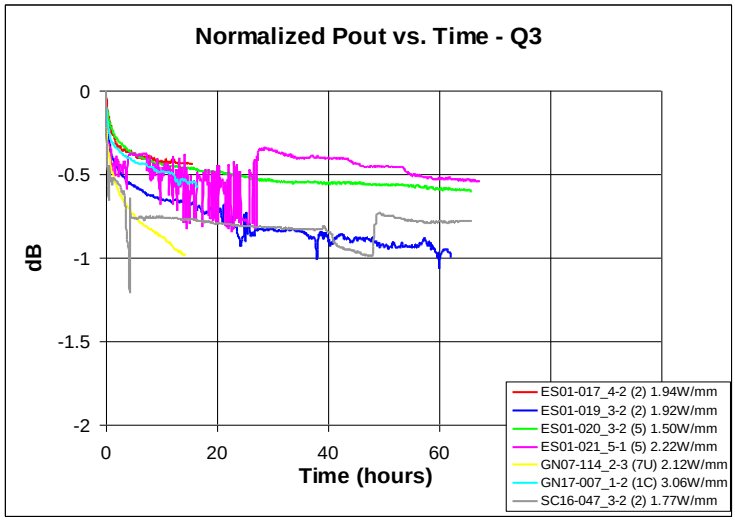
The RF power measurement differs from the previous measurements in one crucial aspect. The RF power measurement operates the HEMT in a manner that it would be operated commercially. While the other reliability measurements may provide insight into possible degradation mechanisms of the device, if the DUT does not degrade in this manner during normal operation information gained by the experiment is of less interest

than determining the mechanism for degradation that occurs when the device is operating as a microwave amplifier. If it can be shown that a DC measurement reproduces the same degradation as the RF measurement, it might be possible to substitute the DC measurement for the RF measurement.

Figure 8.3 shows reliability RF Power measurements made at the U.S. Army Research Laboratory. The devices measured were seven GaN HEMTs with a gate width of 500 µm operated at a drain voltage of 24 V with a gate voltage set to bias the device at 200 mA/mm. The input RF power was set to maximize efficiency.



(a)



(b)

Figure 8.3. RF power reliability results for of 8 GaN HEMTs with total gate width of 500 µm showing the output power normalized to the initial condition (a) plotted against logarithmic time and (b) linear time.

In Figure 8.3(a), the logarithmic decline in power (on the dB scale) appears to have a linear relationship with the logarithm of time.

8.5.2 Mean Time to Failure (MTTF)

The dominant existing standard for reliability across a number of industries and technologies is the Arrhenius Lifetime Measurement. This technique uses the Arrhenius Equation (shown in 8.1) to estimate the mean time to failure.

$$k = A_0 e^{-E_a/kT} \tag{8.1}$$

where A is the scale factor or pre-exponent factor, E_a is the activation energy, k is the Boltzmann constant, and T is the temperature. This equation is used to calculate the rate constant for a chemical reaction at a given temperature. The Arrhenius Lifetime Measurement replaces the rate constant with the mean time to failure. The equation in (8.1) is re-written in (8.2).

$$MTTF = A_0 e^{-E_a/kT} \tag{8.2}$$

This equation has two unknowns, A_0 and E_a. The assumption with applying the Arrhenius equation to reliability is that the degradation mechanism is fundamentally chemical in nature, and the rate of failure is governed by the same relation to temperature as a chemical reaction. This assumption has proved remarkably valid.

In order to perform this measurement, the engineer needs three populations of components to be tested at three separate temperatures. The time required for half the

population to fail is considered to be the mean time to failure. Because the test conditions and failure criteria are arbitrary the Arrhenius

With two equations, it is possible to solve for the two unknowns. The equation for each of the constants is shown in (8.3) and (8.4).

$$Ea = Ln\left(\frac{MTTF_2}{MTTF_1}\right) \times k \times \left(\frac{1}{T_2} - \frac{1}{T_1}\right)^{-1} \tag{8.3}$$

$$A_0 = \left(\frac{MTTF_2{}^{T_1}}{MTTF_1{}^{T_2}}\right)^{\frac{T_2}{T_1}} \tag{8.4}$$

The subscripts refer to two separate experimental populations with different MTTF at different temperatures. The third population measured at a third temperature is used to confirm that the constants that were determined from the first two populations. The dominant parameter in determining reliability with these types of measurements is the activation energy. Theoretically this should correlate with the bandgap. Since gallium nitride is a wide bandgap semiconductor, it should have a superior reliability. Figure 8.4 shows graphically how the activation energy can be calculated using three experimental populations and how it is possible to extrapolate the mean time to failure a chosen temperature.

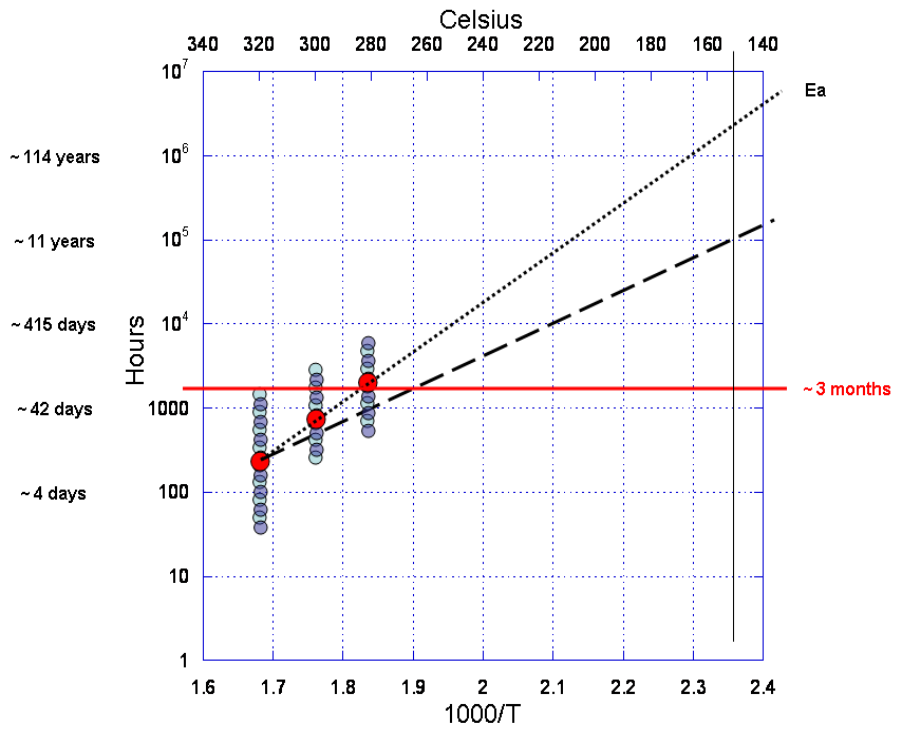


Figure 8.4. The MTTF (in red) for the theoretical sample populations is used to calculate the activation energy and predict MTTF at other temperatures.

Although there is some criticism regarding the Arrhenius Lifetime Measurement, this equation has proven to be an adequate predictor for a number of number of failure mechanisms including semiconductor devices, corrosion induced mechanical failure, mechanical strain, frequent mechanical deformation, and the lifetime for paper manuscripts [70]. Using the Arrhenius Life Test, researchers have reported reliabilities that are commercially viable GaN HEMTs with a MTTF in excess of 10^6 hours [71]. Typically, these devices do not push the material limits of the device with regards to frequency, but they have shown high efficiencies at S-band. This makes them ideal for existing wireless protocols such as the IEEE 802 series. The research on these devices did not establish a statistical sample that was robust enough to establish a MTTF of the type that has been extensively used to quantify GaAs reliability [72].

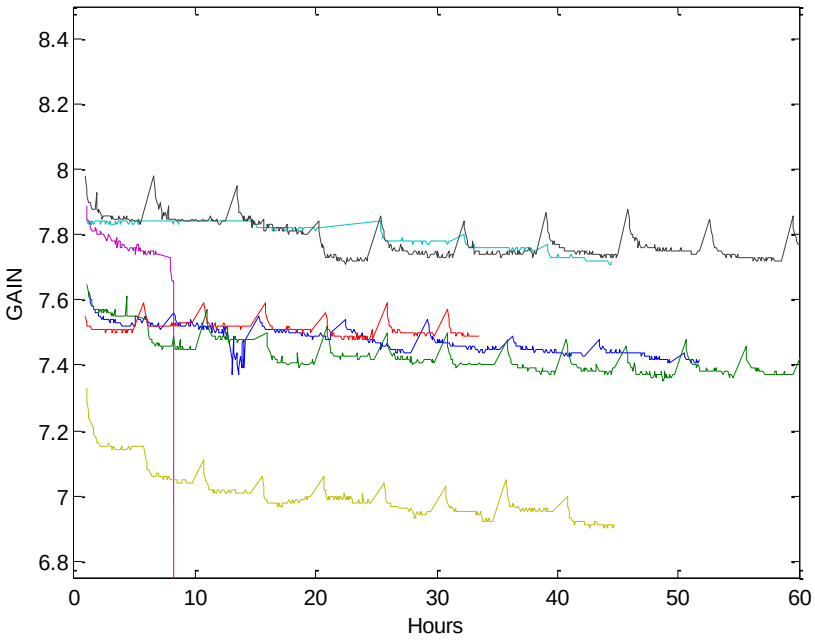
In this chapter, a survey of possible degradation mechanisms was discussed. Possible degradation mechanisms were presented in conjunction with the reported experimental reliability measurements being developed by the GaN community. The dominant industry standard for reliability measurements was described with its theoretical justification.

Chapter 9: Report of Experiment and Analysis of Degradation Data

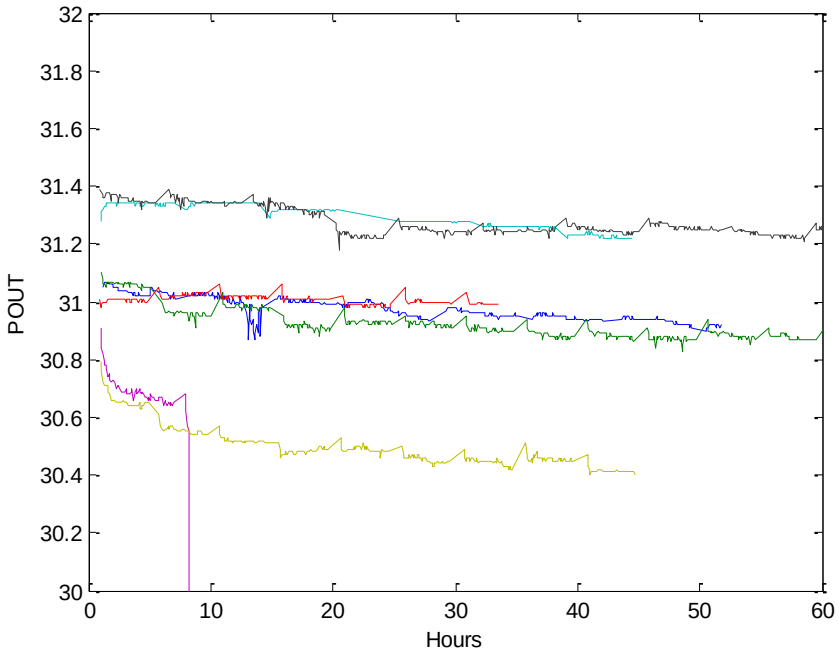
According to DARPA's program description of the Wide Bandgap Semiconductor Technology Initiative (WBGSTI), the goal of the project was to " enable new RF applications and capabilities through the development and exploitation of the material, device, and circuit properties of wide bandgap semiconductors" [73] . The Army Research Laboratory together with our triservice partners, NRL and AFRL, served as the honest brokers of the device performance for the contractors participating. The contractors developed the material and devices and the triservice verified their reported performance. This was crucial in determining whether key benchmarks had been met by the contractors. The program was broken into three phases with each phase lasting several years.

While operating in this role, researchers at ARL measured over 2400 AlGaN/GaN HEMTs on 251 separate wafers from four contractors. A diverse set of measurements were performed including those described in this research such as s-parameter measurements, IV curve measurements, power sweeps, and Arrhenius reliability measurements. A variety of other data was also collected and reported to the contractors and DARPA program managers. This data include material quality data, device noise figures, gate pinchoff voltages, and gate breakdown voltages. Engineers and solid state physicists at ARL have the Wide Band Gap Semiconductor Center of Excellence, which has been recognized by senior Department of Defense officials responsible for research and development.

The diagnostic and reliability measurements described in this research were performed on nineteen devices across six wafers. There were a total of nine catastrophic failures. One test was terminated early due to electrical failure. Four of the functional tests were conducted during the development stage of the project; and as a result, they failed to acquire sufficient data to constitute a complete model. Three of the tests were rejected do to procedural errors. There are currently two devices that have completed the full cycle of reliability measurements and are in possession of a full set of data. One of these devices will be analyzed in detail. Figure 9.1 shows the gain and output power performance of a sample of devices measured with the ALERTS. The device used as a representative sample is shown in blue. The measurements were made with a chuck temperature set to 25 C with performance conditions like those described in chapter 4.



(a)



(b)

Figure 9.1. Reliability behavior of 500µm GaN HEMT of a set of similar devices on the same wafer (a) Gain (dB) versus Time and (b) Output power (dBm) versus Time.

The periodic structures are a product of the periods during testing when the reliability test is suspended and detailed device measurements are performed.

9.1 Characteristic Device

A representative example of the tests performed by the ALERTS is described below. The data will be presented and then analyzed to determine that changes in the DUT. The measurement consisted of running the system for 51 hours and 44 minutes at 25 C, 46 hours and 25 minutes at 75 C, and 93 hours and 47 minutes at 125 C. Following the final reliability measurement, the chuck temperature was reduced to 25 C and a final characterization was made. Each detailed measurement took approximately ninety minutes. The interval between detail measurements during which the device is stressed lasts six hours. The output power of the DUT at three separate temperatures is shown in Figure 9.2 over the duration of the test. The periods during which the detailed device

measurements were performed have been removed. Only the periods during which the device is actually being stressed are plotted.

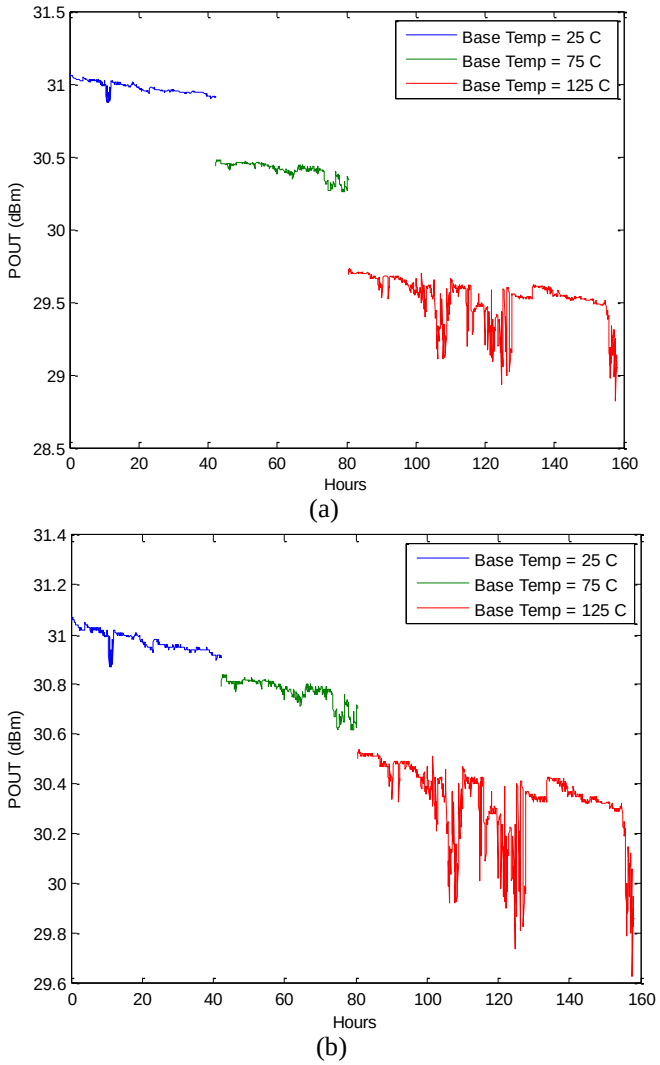


Figure 9.2. Output power during reliability measurement of 500µm GaN HEMT at three separate temperatures (a) directly measured data (b) data with elevated temperatures adjusted to account for temperature effects between measure temperature and nominal temperature (25C)

Figure 9.2(a) shows the raw output data. The thermal effects on output power can be seen in this plot. Figure 9.2(b) shows the temperature adjusted output power. In this plot, the output power of the DUT has been adjusted back to the nominal temperature using the values calculated from the procedure described in Chapter 7. There is still a discontinuity

between the different chuck temperatures. This suggests that the corrections that are being used for thermal effects do not completely account for all the behavior of the device when it is being driven into compression at an elevated temperature. A similar plot for gain and drain current is shown in Figure 9.3.

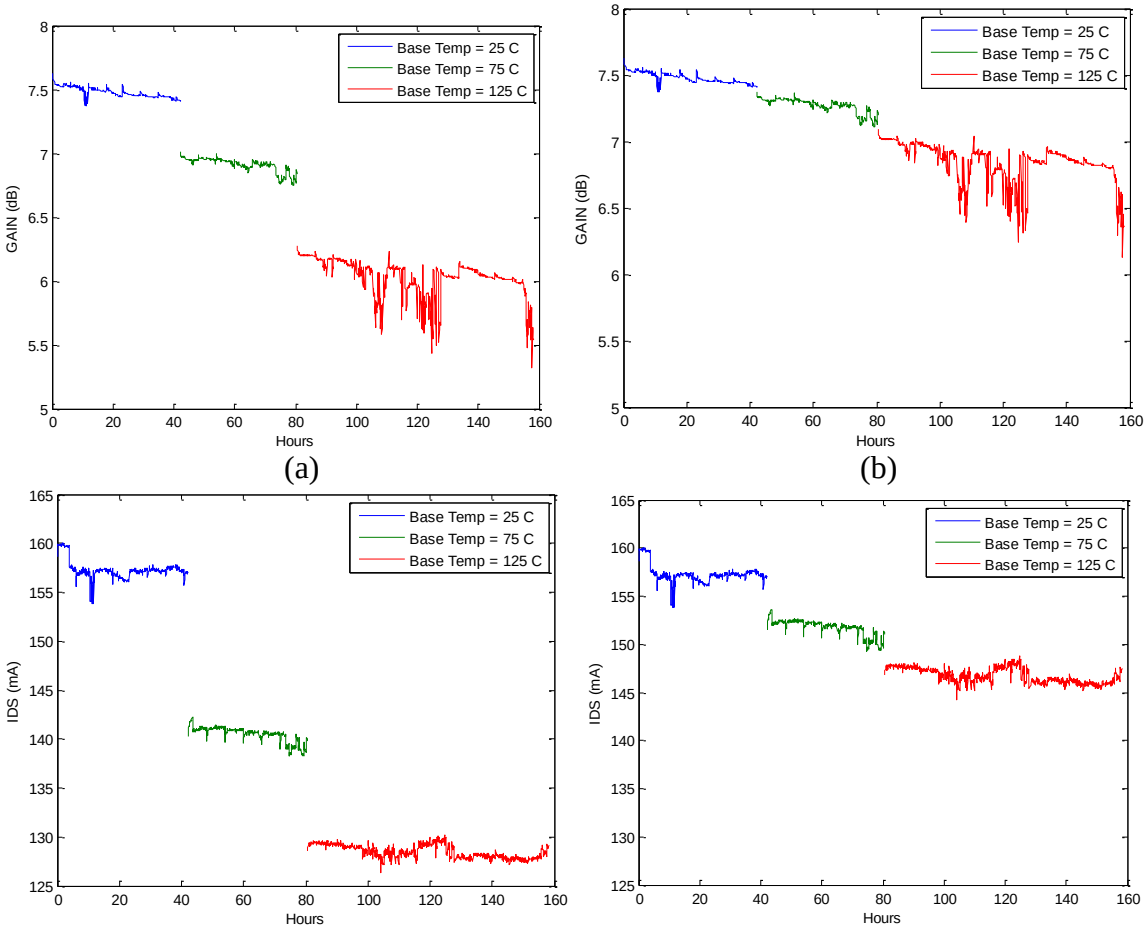


Figure 9.3. Reliability measurement of 500µm GaN HEMT at three separate temperatures (a) directly measured Gain data (b) Gain data with temperature effects correct to 25C (c) directly measured drain current data (d) drain current data with temperature effects correct to 25C.

9.1.1 Power Sweep Data

The detailed device measurement begins with a power sweep at bias. Plots of the each of the power sweeps from the periodic detailed device measurements at all three temperatures are shown in Figure 9.4.

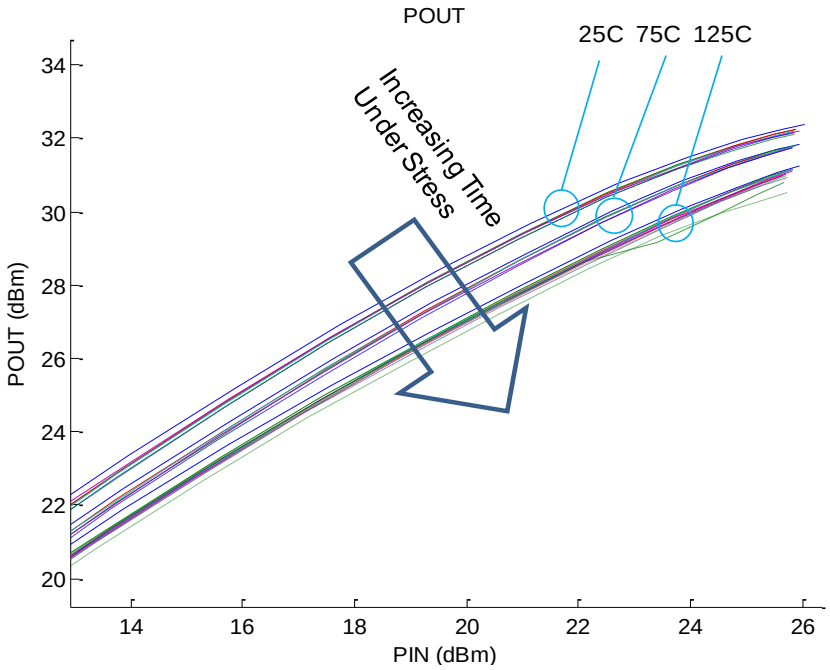
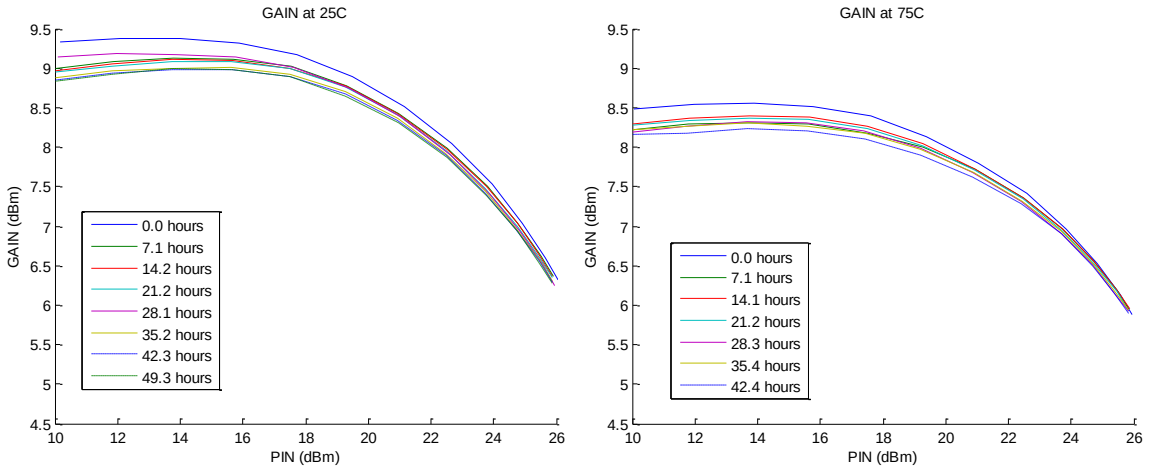


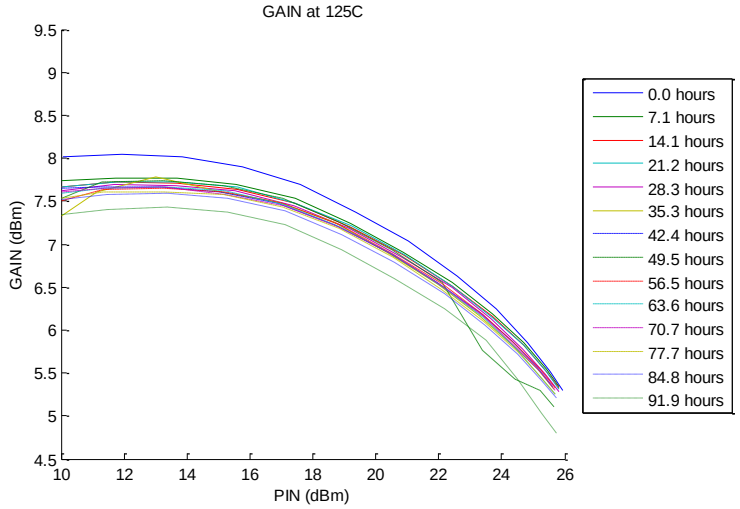
Figure 9.4.Output power from power sweeps performed at periodic intervals while the DUT is being stressed during high power operation and in later instances at elevated temperature.

The performance from the power sweeps are what would be predicted from observing the reliability power measurement. There is a slight decline in power performance with time that similar to that seen in the reliability data. The gain measured during the periodic power measurements of the DUT is shown in Figure 9.5.



(a)

(b)



(c)

Figure 9.5. Gain from power sweeps during performed measurements at (a) 25C at (b) 75 C and at (c) 125 C.

The behavior seen in the gain and the output power is repeated in the drain current. Power added efficiency is a combination of several measurements; and therefore, it is more sensitive to changes in multiple measurements. Figure 9.6 shows the swept values for PAE.

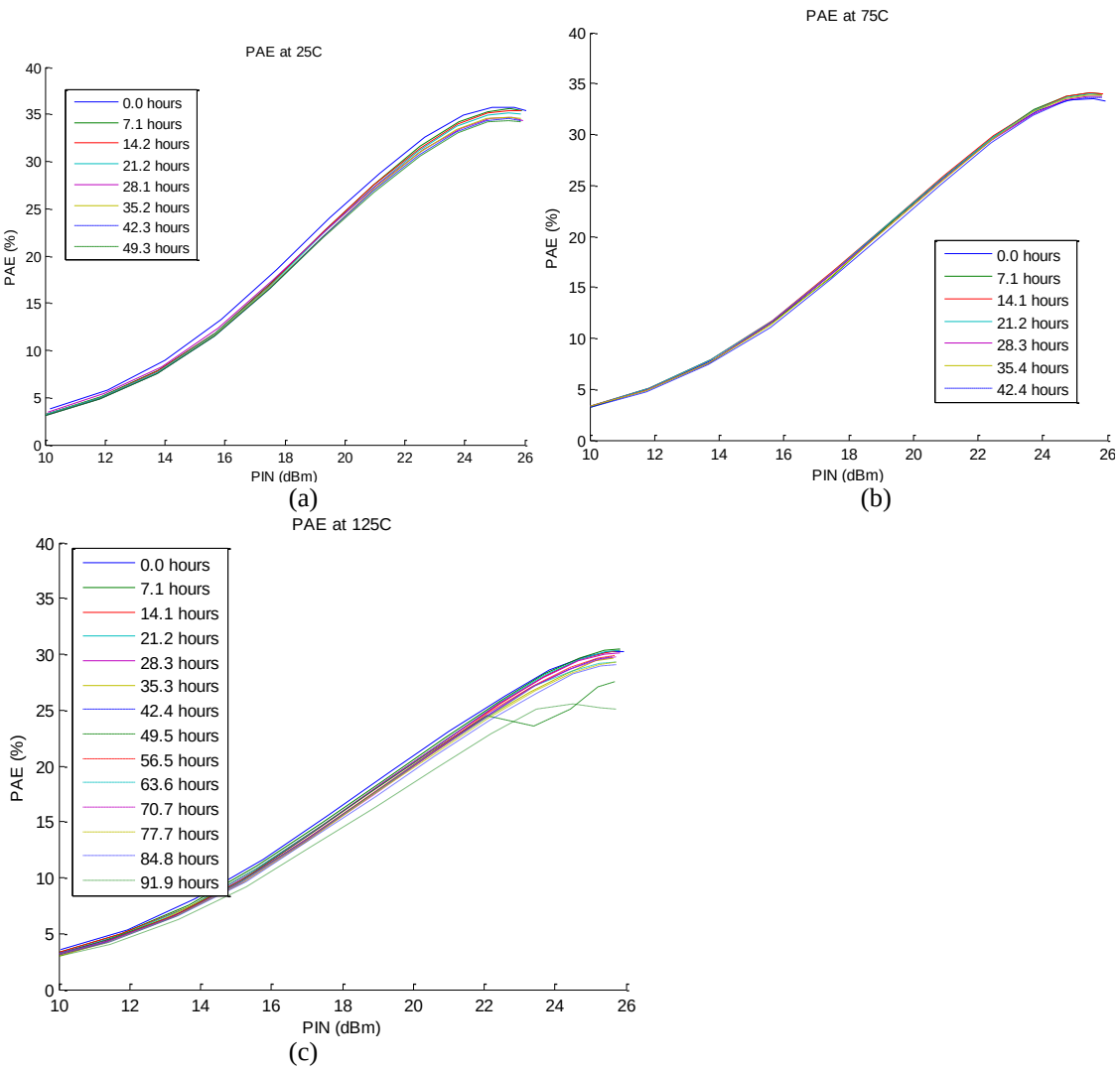
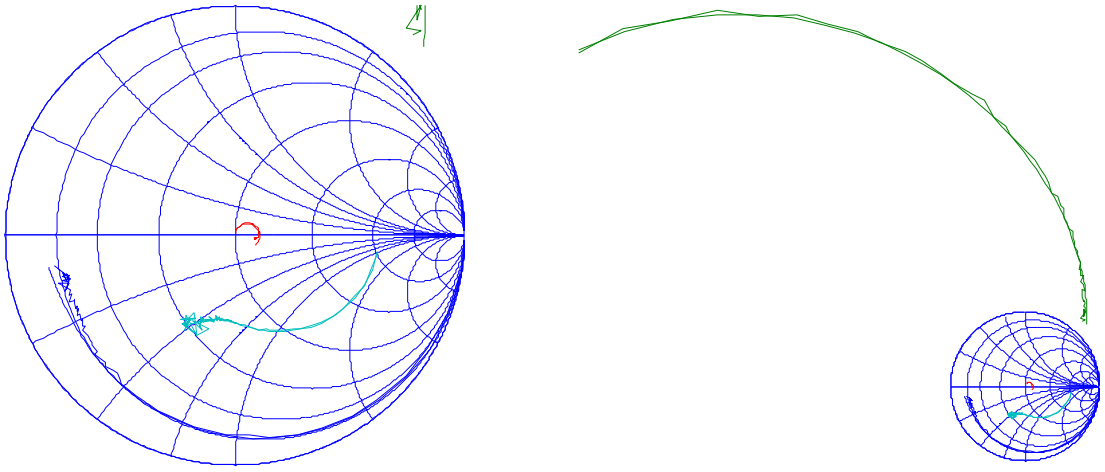


Figure 9.5. Power added efficiency from power sweeps during performed measurements at (a) 25C at (b) 75 C and at (c) 125 C.

9.1.2 Small Signal Model at Bias

While the DUT is still under bias, the RF power is turned off. The RF switches move from the power measurement configuration to the S-parameter measurement configuration. The vector network analyzer measures the S-parameters of the DUT. The parasitic elements will be determined from a subsequent measurement. Using these parasitic values, the small signal equivalent circuit model was produced. As has been stated, the algorithm that was developed to create small signal models for the device

under test can with a high degree of consistency produce model that agree closely with measured data. Figure 9.6 shows a plot of data calculated from the equivalent circuit model superimposed on top of the measured data.

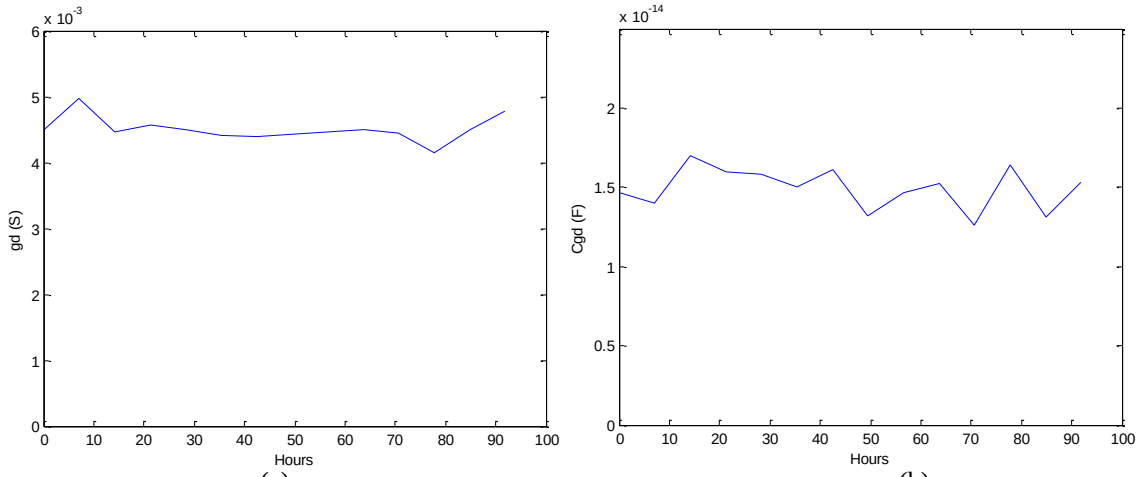


(a) (b)

Figure 9.6. Measure data and data from the equivalent circuit model (a) plotted on the Smith Chart within the unit circle (b) plotted on the expanded Smith Chart

There is close agreement between the two data sets. When the s-parameters and the component values are inspected to see how they change over time, the most obvious characteristic is their consistency.

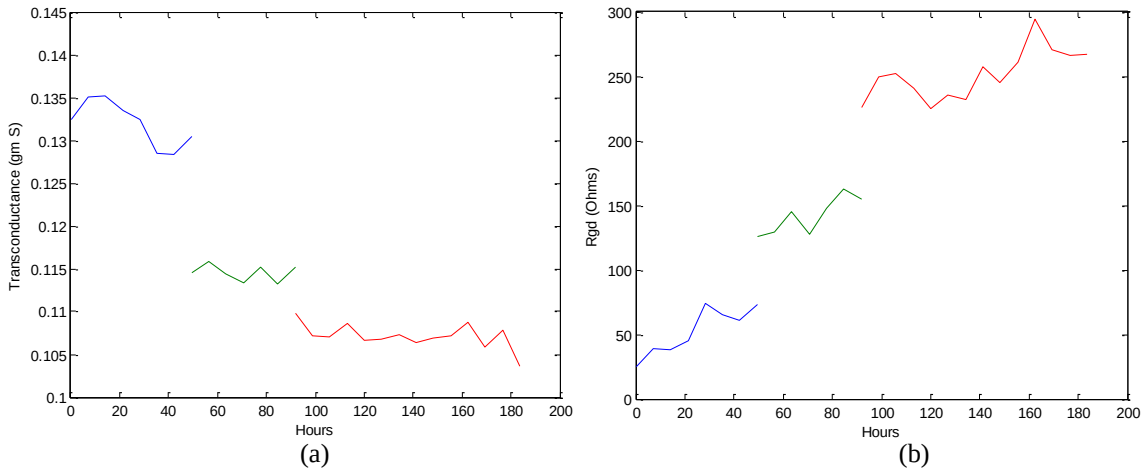
An example of this is shown in Figure 9.7. The equivalent circuit model parameter gd, which is the drain admittance, and the gate drain capacitance can be used as examples of the stability of the majority of the equivalent circuit model parameter component values over the period during which the device is stressed.



(a) (b)

Figure 9.7. The behavior of small signal equivalent circuit model parameters while the device is being stress (a) drain admittance (gd) (b) gate drain capacitance.

There were two prominent exceptions to this. These are the transconductance (gm) and the resistance value associated with the gate-drain diode (Rgd). Figure 9.8(a) is a plot of gm from the small signal model over the full duration of the test. There is a slight decline over time that has also been seen in other data from the device that shows the change in performance.



(a) (b)

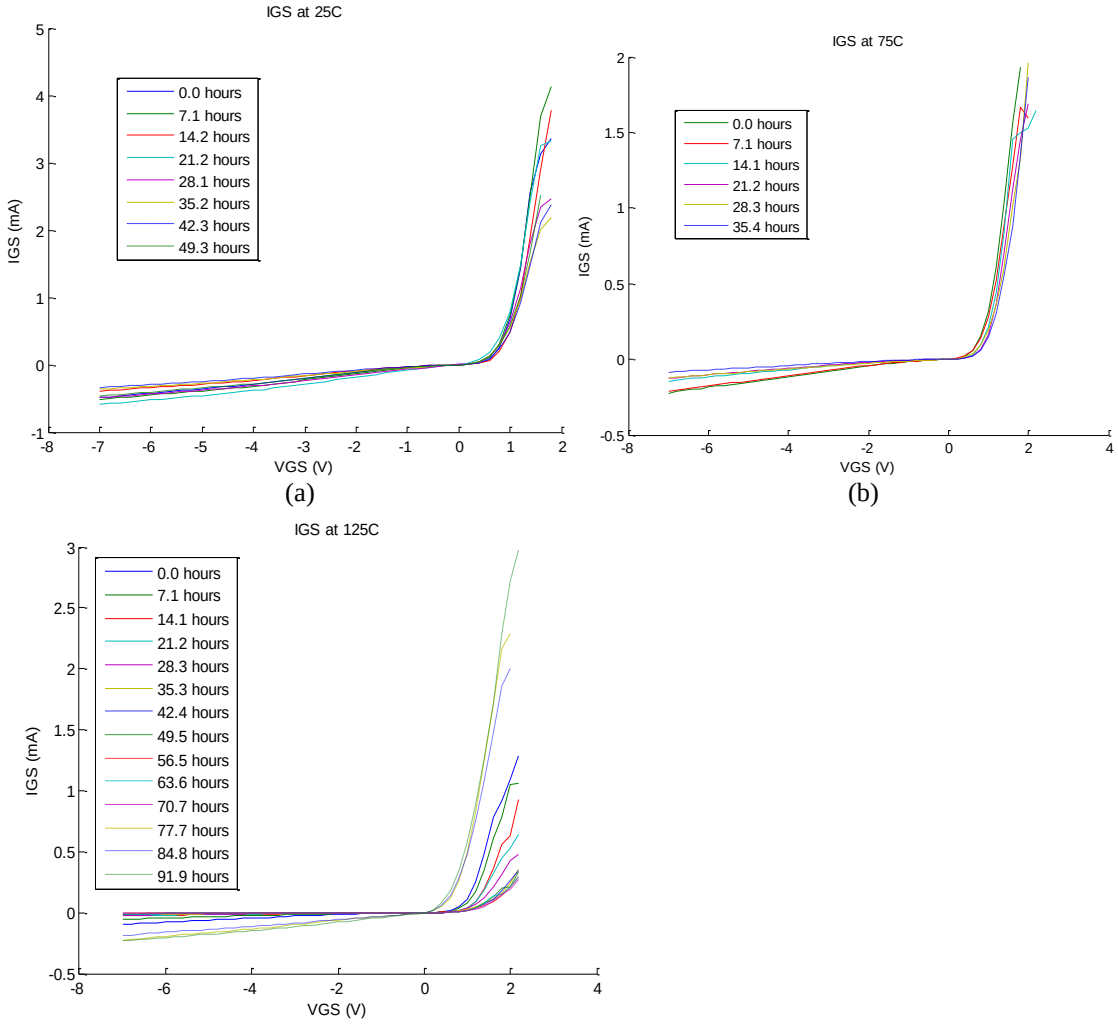
Figure 9.8. The behavior of small signal equivalent circuit model parameters while the device is being stress (a) transconductance (gm) (b) gate drain capacitor resistance.

The change in the gate drain resistor also has been seen in increase over time. It is important to remember when looking at the small signal parameters that these values

represent the device performance at high frequencies and that frequency dependent behavior will be represent in the device values.

9.1.3 Gate Measurements

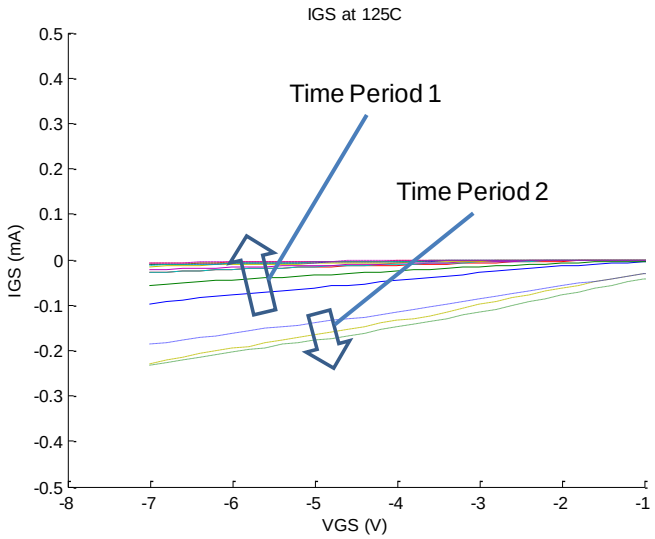
The periodic gate measurements consist of measuring the current, voltage, and s-parameters while the gate voltage is swept. The s-parameters are used to determine the parasitic components. These are represented in the large signal model and the small signal model, and they will not be discussed in this section. The gate current is shown plotted as a function of gate voltage for all the gate current sweeps in Figure 9.9.



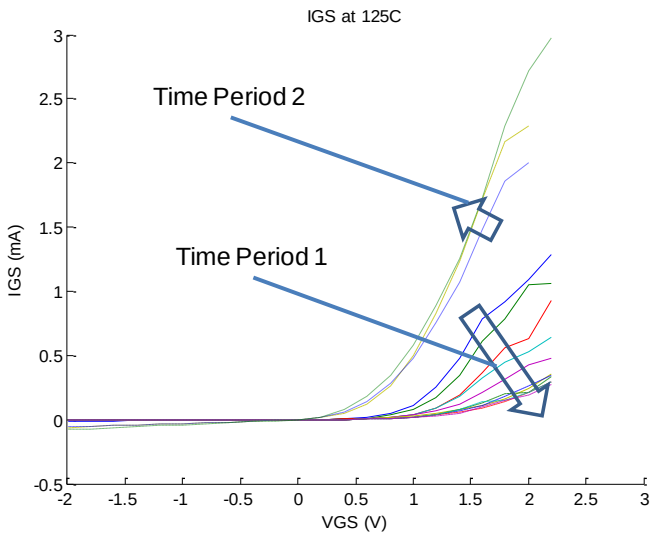
(c)

Figure 9.9. Gate current-voltage behavior measured periodically while the DUT is operated under stress at (a) 25C (b) 75C and (c) 125C.

In during the measurements made at a chuck temperature of 25C and 75C, the change in behavior follows a direct pattern. The leakage current decreases over the long term, and the forward biased current increases over the long term. The measurements made at 125C continue this pattern initially; however, performance undergoes a dramatic change between the 70.7 hour measurement and the 77.7 hour measurement. After this time, the current is dramatically different. The device has a different turn-on voltage, and the trend of change over time reverses itself. This can be seen in Figure9.9(c) and in greater detail in 9.10.



(a)



(b)

Figure 9.10. Detailed view of gate current-voltage behavior measured periodically while the DUT is operated under stress at 125C (a) showing the reverse bias behavior and (b) the forward bias behavior.

9.1.4 Detailed IV Curves and Large Signal Model

The detailed IV curve and s-parameter measurement described in section 4.2.4 is used to generate the final large signal model of the DUT. In Chapter 5, Chapter 6, and Chapter 7, the forty-eight parameters used to generate the large signal model are described along with the technique used to extract them. As described in the previous sections, the performance of the DUT over the period of the stress test changes only slightly. Most of the model parameters are remarkably consistent between measurements. The exceptions to this provide insight into the changes of the DUT. This is particularly true of the reactive components of the model.

Two of the parameters that change during the stress test are the drain admittance and the transconductance. The drain admittance from the periodic measurements over the full scope of the test is shown in Figure 9.11.

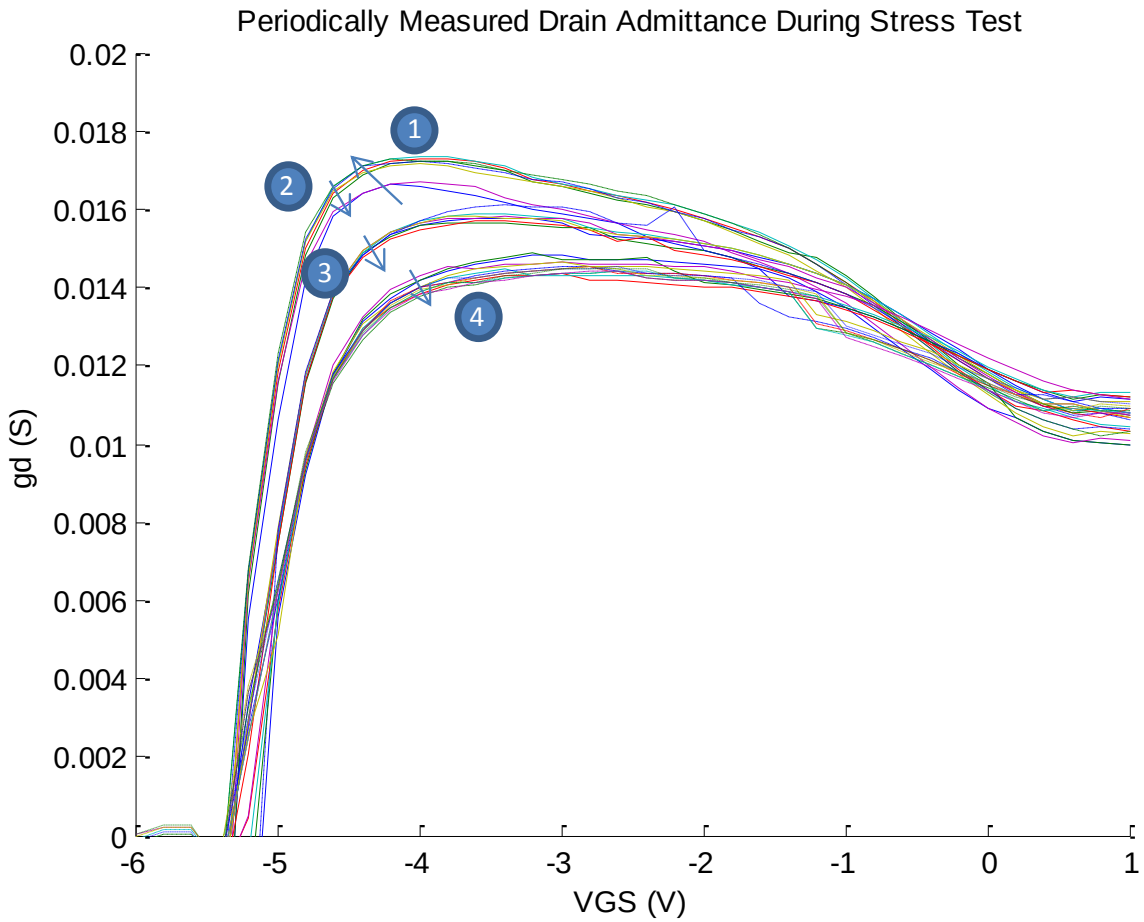


Figure 9.11. Drain admittance of periodic large signal models while the device is stressed at different temperatures illustrating long term trends.

This measurement does not correct for thermal effects on gd. There are four separate behavior regions. The initial behavior (region 1) has the peak gd increase in magnitude and decrease in bias voltage. This occurred in the first 12 hours of operation. Early dramatic changes like these are usually considered to be burn in behavior. This could be thought of as the final post processing of the device, and the researchers do not consider it to be part of the long term device behavior. The remaining three regions (2-4) represent the device behavior at each of the temperatures being investigated. The degradation behavior is consistent. Peak gd occurs at increasing gate voltage and has a decreasing magnitude.

This behavior is also seen in the transconductance shown in Figure 9.12.

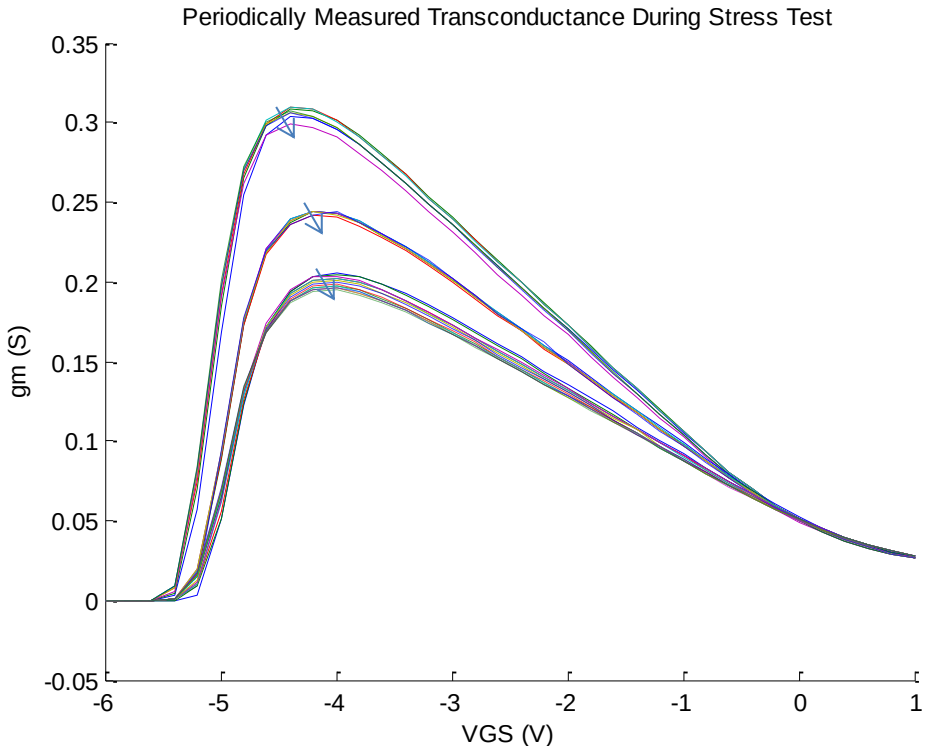


Figure 9.12. Transconductance as a function of gate voltage of periodic large signal models while the device is stressed at different temperatures illustrating long term trends.

The long term trend is for the magnitude of the transconductance to decrease and the peak transconductance to occur at increasing gate voltage. Figure 9.13 shows the peak transconductance over time.

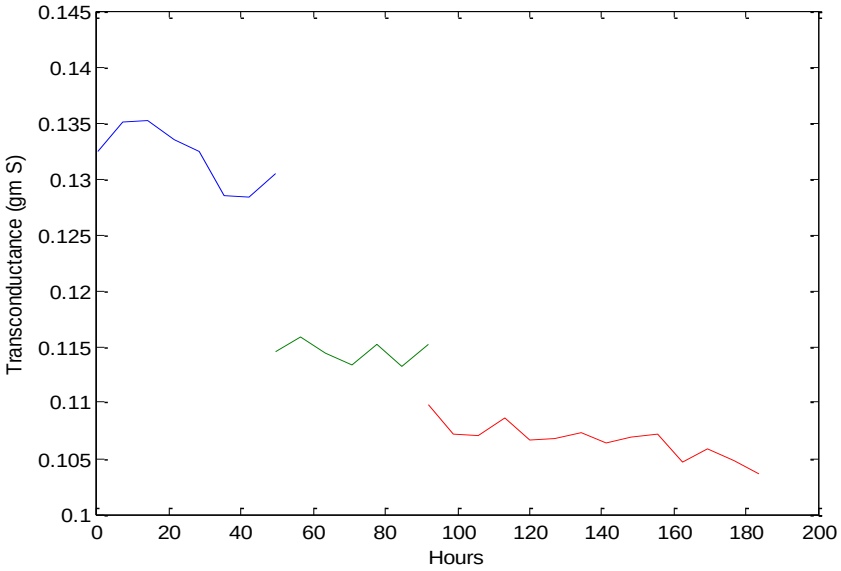


Figure 9.13. Peak transconductance of periodic large signal models while the device is stressed at different temperatures illustrating long term trends.

Another large signal parameter that has shown consistent change over the life of the test is the first coefficient of the drain current source polynomial. The behavior of this large signal parameter is shown in Figure 9.14. This is the dominant term that determines the slope of the drain current as a function of gate voltage. The derivative of the drain current function with respect to the gate voltage is the definition of the transconductance.

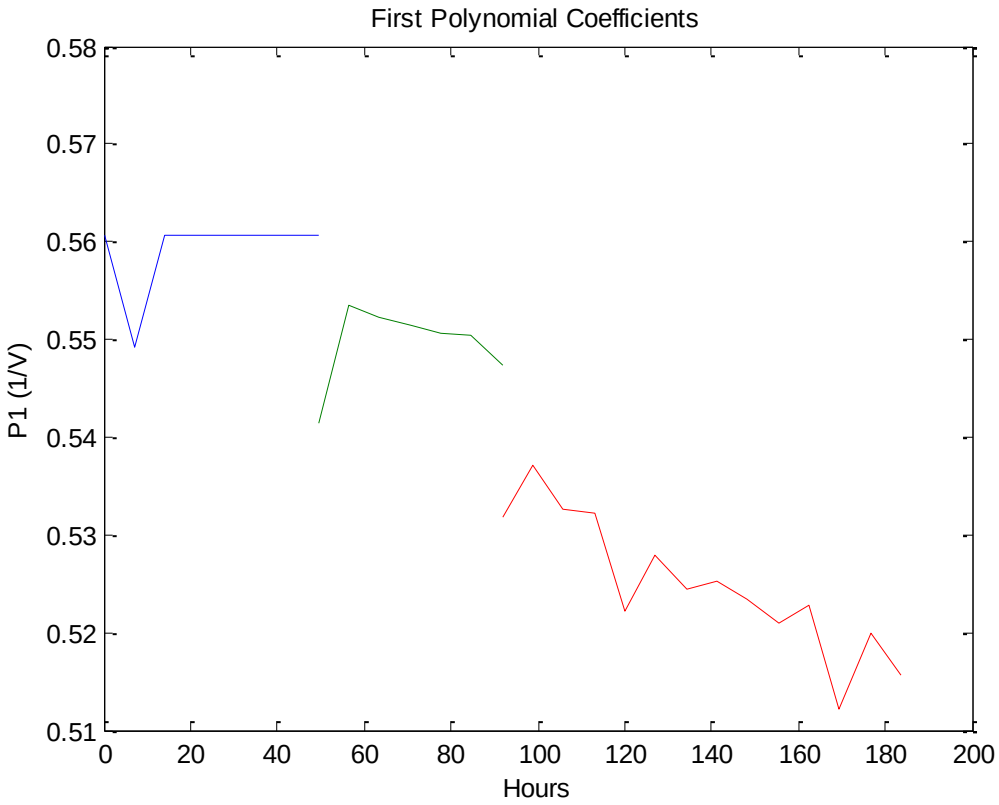


Figure 9.14. Behavior of the first polynomial constant from the Angelov Large Signal Modes while the device is stressed at different temperatures illustrating long term trends.

Other component changes to the large signal model will be discussed in the next section that discusses diagnostics.

9.2 Analysis of Degradation

A great deal of data has been reported. For that data to prove useful, it must be analyzed to determine its significance. The author in conjunction with engineers and scientists at ARLs Wide Band Gap Semiconductor Center of Excellence examined the results of this data [74-76]. The descriptions below summarize their analysis.

9.2.1 Source Resistance

One of the parameters that showed a consistent measureable change that could be correlated with a degradation mechanism was the source resistance. The degradation of

ohmic contacts in GaN has been reported in the literature [77]. Figure 9.14 shows the changes in the equivalent circuit model source resistance determined during the large signal model tests that were conducted periodically during the stress measurement.

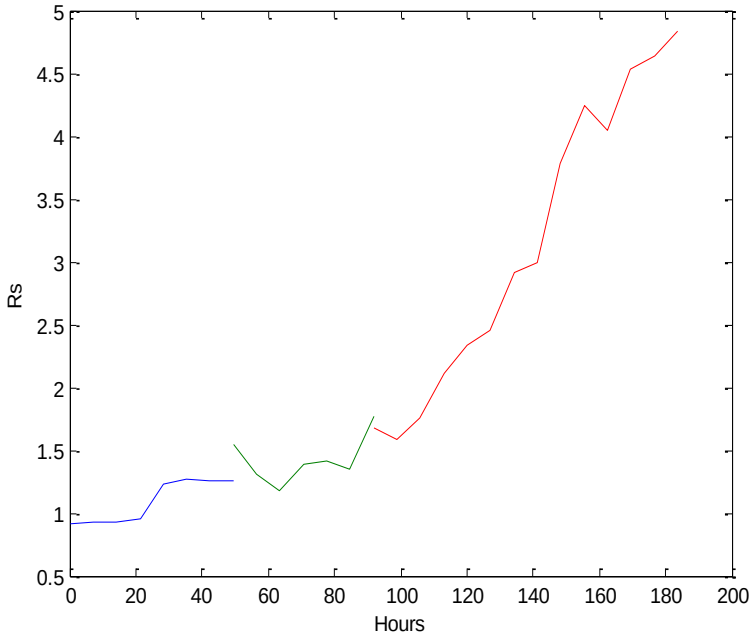


Figure 9.15. Change in source resistance from periodic large signal models while the device is stressed at different temperatures.

The source resistance was determined using the parasitic element extraction techniques described in Chapter 5. There is a strong correlation between the base plate temperature and the change in source resistance source resistance. The other parasitic resistances, Rg and Rd, did not show a significant change throughout the duration of the reliability test.

9.2.2 Channel Resistance

Both the change in magnitude of the transconductance in Figure 9.12 and Figure 9.13 and the change in drain admittance in Figure 9.11, can be explained by a gradual increase in channel resistance. The effects of an increase in channel resistance can be differentiated from traps (described below) by their behavior over time. The amount of

decline from which the device recovers with the stress conditions are removed can be attributed to traps. However, when the device is allowed to relax, not all of the decline in behavior can be recovered from. Permanent decrease in the current and gain that is not correlated with other performance parameters is attributed to increase in channel resistance.

9.2.3 Gate Traps

A number of independent observations indicate the presence of trapping in the gate region. One of the results of traps in the gate region would be the creation of a virtual gate. The effect on the device of this would be a change in the bias conditions of the DUT. This could be seen in the change in the gate voltage at which the peak transconductance occurs. The trend in Figure 9.12 shows that over time the peak transconductance decreases, the gate voltage at which peak transconductance occurs moves to the right.

The effect of traps is shown in Figure 9.15. The plot shows the transconductance behavior of the same device at three different times. The transconductance is shown for the initial unstressed device, for device immediately following the conclusion of the stress measurements, and for the post-stress device that has been allowed to recover for a day.

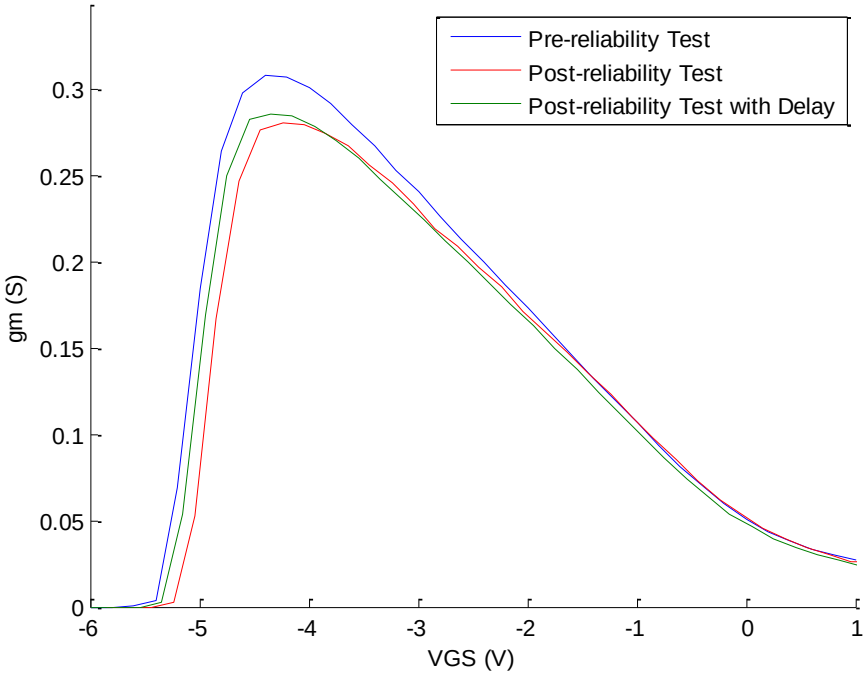


Figure 9.15. A comparison of transconductance performance of the device before being stressed (blue), the device immediately after the conclusion of stress measurements (red), and the device after the conclusion of stress measurements and subsequent period of time in the absence of electric fields (green).

The device after the delay recovers 3% of its transconductance from the same device immediately post stress. The voltage at which peak transconductance occurs can be seen to move toward the value of the unstressed device.

The gradual change in the gate current is also believed to be causes by traps in the gate. Figure 9.16 shows the long term gate current of the DUT during the reliability test.

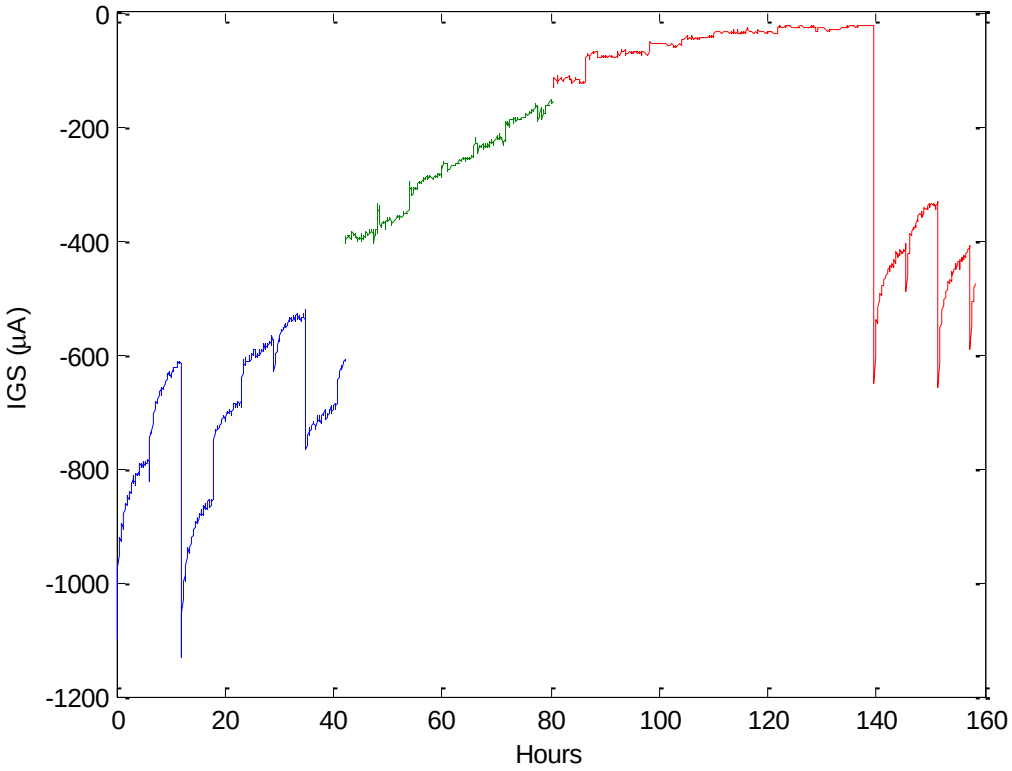


Figure 9.16. Gate current measured during the reliability measurement of 500μm GaN HEMT at three separate temperatures.

Both the gradual degradation and the sporadic behavior of the gate current are believed to be caused by traps in the gate. The slow change is not thought to be caused by a change in resistance because the magnitude of the change in the resistance has not been observed in any components.

While it has been hypothesized in this research that the measured effects are caused by trapping, this theory could be corroborated by confirming this through one or more alternative methods. A simple and effective technique that has been used extensively to facilitate the investigation of reliability in transistors and HEMTs is to visually inspect the devices or the images produced by such techniques as scanning electron microscopy [78]. This could be used to identify gross changes to the metal of the source contact to determine if the air bridges or other metallization are the source of the

increase in source resistance. One procedure used to detect traps that is similar to the measurement system previously described and that could probably be implemented without the use of additional hardware is the capacitance-voltage measurement. The vector network analyzer could measure the high frequency behavior of the carriers using s-parameter measurements. The low frequency behavior could be measured with the HP4142 pulsed behavior on the gate. The time constant on the traps should be long enough that the charges in the traps could not respond to the high frequency signal. For similar reasons, observed hysteresis in the capacitance would also be an indicator of traps. There are several techniques to directly measure traps. These include deep-level transient spectroscopy (DLTS) measurements. DLTS as originally conceived by its inventor was "a capacitance transient thermal scanning technique [79]." The measurement is performed by recording capacitance transients while the temperature is changed. Ideally this change will be from a very low temperature (~-190C) up to room temperature or higher. It is possible to measure the time constant of this transient as a function of temperature and obtain the thermal emission properties for a trap as well as the activation energy. This has been extensively described in the literature [79, 80]. By monitoring the change in the magnitude of the peaks produced by the DLTS measurement, the change in the trap density and the type of trap could be directly measured. If this measurement was repeated over time, the rate of trap formation could be measured.

In addition, some researchers have correlated a change in the electric field profile with evidence of traps. The change in electric field profile has been observed through a change in electroluminescence. The belief being that increased trapping results in decrease peak field strength and consequently decreased electroluminescence cause by

hot electrons [58, 71]. A technique developed to investigate the transient behavior of traps in silicon carbide (SiC) MOSFETs made use of measuring the pulsed current response and comparing it to complex simulation solution to the Poisson and current continuity equations [81]. By observing the rate at which traps are filled the researchers were able to determine the trap density and trap cross section. Related research successfully modeled the effect of traps on the electric field profile in SiC MOSFETs [82]. Simulated DC models were produced by the researchers that had a close agreement with measured data. By correlating simulation with measured data, the researchers were capable of determining trap density of states and the thermal behavior of traps. The technique for characterizing the transient behavior of gate traps in these devices is also described in another paper [83]. This procedure makes use of relatively long (1 ms) pulsed IV measurements from which can be extracted the initial drain current, the final drain current, and the time constant associated with the transient behavior. The previously described research was done on MOSFETs. By adapting their techniques to GaN HEMTs, it should be possible to reproduce their results and analytically determine the number of traps during each detailed measurement period, the change in traps with time and as a result a rate for defect creation.

The dramatic change in gate current that is observed in Figure 9.16 corresponds to the dramatic change in the diode behavior of the gate in Figure 9.9 and Figure 9.10. The effect of the change on power and efficiency is shown in Figure 9.17.

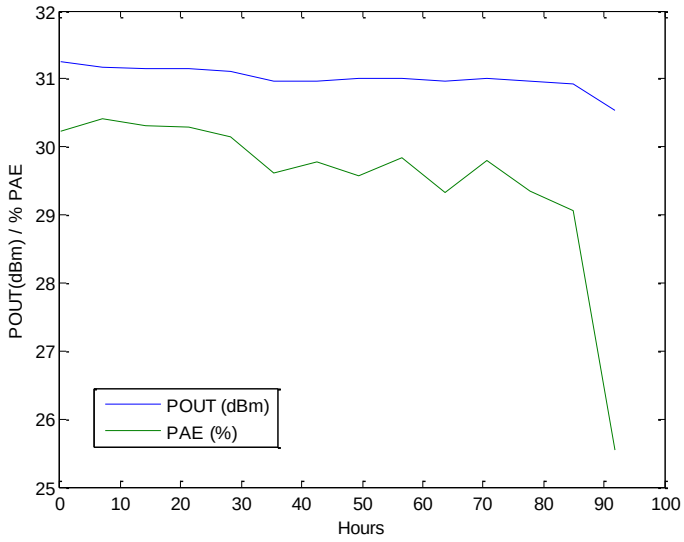


Figure 9.17. Measure peak values for output power (POUT) and power added efficiency (PAE) of periodic power sweep for 500µm GaN HEMT at 125 C.

It is unclear if this phenomenon is related to the trapping behavior or if it is indicative of a different degradation mechanism. One line of reasoning is that the trapping reaches some critical value and this causes a dramatic change in device behavior. For example, a small number of traps may create a virtual gate behavior while a large number of traps could create a trap channel through the gate. The other line of reasoning is that the gradual change in gate current and the dramatic change in gate behavior are separate phenomenon. The gradual change could be the previously describe trapping, while the dramatic change could be the physical cracking of the gate material.

Of the three degradation mechanisms discuss, the easiest to correct in the fabrication process is the Source Resistance. This will also do the most to preserve the long term performance of the device.

Chapter 10: Conclusion and Future Work

A technique for determining the device performance changes while a device is stressed under normal operating procedures has been proven. This technology has aided in the diagnosis of the degradation mechanisms of experimental Gallium Nitride HEMTs.

10.1 Accomplishments of this Research

In this research, a new technique of diagnosing the degradation of semiconductor devices has been developed. To accomplish this task, several supporting tasks had to be completed. These include:

- The design and construction of a system capable of applying an arbitrary impedance to the source and load of a device, making power measurements, and switching to make DC and S-parameter measurements while the probes remained in contact with the DUT.
- The development of software to control and monitor such a system.
- The development of software capable of manipulating and displaying S-parameters.
- The development of software capable of producing small and large signal equivalent circuit models.
- A procedure to compare device performance and models from different temperatures.

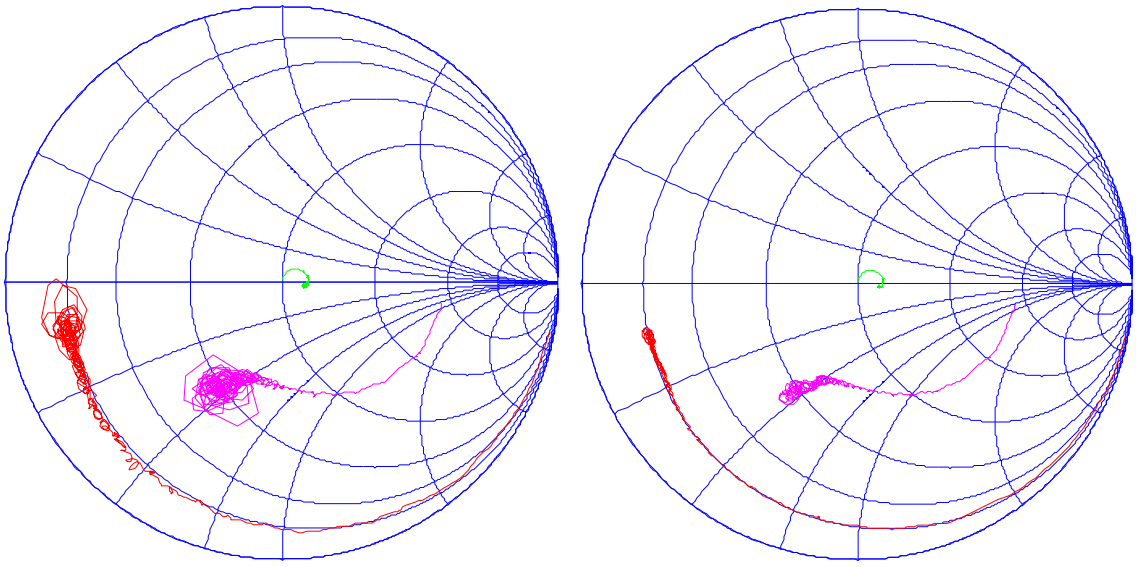
The resulting volume of data produced by this technology using this technique provides a holistic view of the device over time. Instead of looking for a deliberate degradation mechanism, this system measures a broad variety of performance characteristics. By generating equivalent circuit models, small changes in device performance have be localized to aid in the diagnostic process.

10.2 Future Work

This novel research has opened many opportunities to continue its progress along several parallel paths of development. Some of them are listed below.

10.2.1 Incorporated Device Changes into MMIC Design

Originally when I began this research, I thought that optimal impedance match of the DUT might change significantly during the reliability process. If this were the case, part of the decline in performance would be the result of an increasing mismatch between the MMIC designed to the initial state of the DUT and the degraded state of the DUT. After investigating the degradation behavior of several GaN HEMTs, is has been observed that the optimal input and output impedance matches do not change significantly during the degradation process. Figure 10.1 shows the s-parameters of a device before and after stress.



(a) (b)

Figure 10.1. Comparison of s-parameters for a 500µm GaN HEMT (a) before reliability test and (b) after.

Even after several days of being operated several dB into compression S11 and S22 are virtually unchanged from the initial condition.

It has been determined that more than half of the decline in gain is due to shift in the transconductance caused by what appears to be a virtual gate effect created by traps. By periodically changing the bias of the DUT to compensate for traps, this decline in performance can be corrected. Another identified cause of the decline in performance is an increase in source resistance. By changing the fabrication process to eliminate this cause, the degradation can further be reduced.

This diagnosis applies to a single wafer of a single fabrication process. Different production runs or different technologies might have more pronounced changes to optimal impedance match. These could benefit from a change in the optimal match. Regardless of the impedance match, MMIC designers can benefit from knowledge of how the device changes over time and can incorporate mitigating mechanisms.

10.2.2 Improve Device Modeling Using Pulsed IV Measurements

The ability to determine the electrical performance of the DUT without observing thermal effects would be very valuable during the generation of device models. This has been accomplished have been demonstrated by researchers developing GaN models [74]. The system that was developed for this research was able to determine the thermal properties by examining device behavior at different temperatures and correlating that behavior with power dissipation. A pulse IV power supply would allow the direct measurement of electrical behavior which could lead to even more accurate device models and a superior system for measuring DUT self heating effects.

10.2.3 Implementation of the System on an Industrial Scale

The system described in this research did an effective job at characterizing a single device. The measurement lasted for several days during which much of the equipment sat idle. For the measurements to be statistically significant to use on an industrial scale, a large number of devices from a commercial foundry process must be characterized. This can be done by altering the system so that the measurements are performed in parallel with some measurement, such as those performed by the network analyzer, staggered in time. This will increase the amount of time that the network analyzer is being used resulting in a more efficient allocation of capital equipment. Figure 10.2 shows a schematic of what and industrially scaled up system might look like.

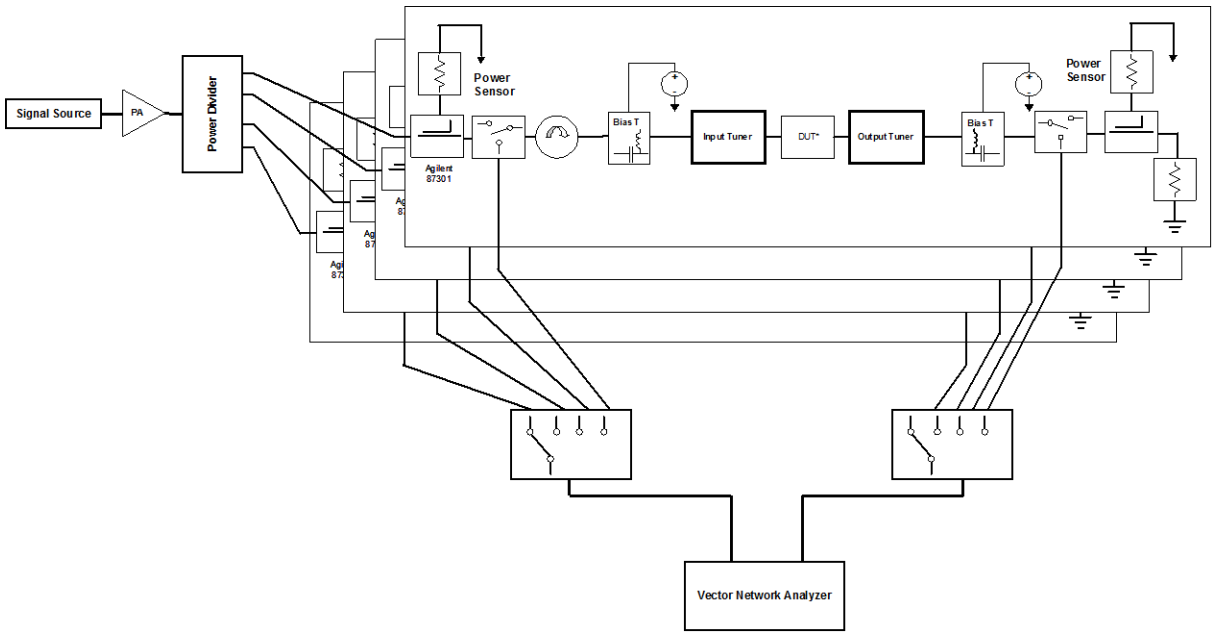


Figure 10.2. Multi-device ALERTS that makes use of a switching system to all the network analyzer to measure multiple devices.

This system could be created with a moderate capital investment.

10.2.4 Modify System to Work with existing Technologies and Other Novel Materials

The proof of concept for this system was a wide band gap semiconductor material that is at the threshold from transitioning from a research material to one that is widely commercially available; however, the system could be used on both less mature technologies and more mature technologies. Silicon Germanium (SiGe) is an attractive material because of its ability to be integrated into existing silicon fabrication technologies. The parameters of the system could be modified to determine the degradation mechanisms of this material. Devices made from other novel materials, such as indium phosphide (InP), could be investigated. Mature technologies like GaAs and silicon could be analyzed to establish a time based reliability of their models.

The measurement procedure algorithm would have to be significantly altered to measure devices other than field effect transistors, but that is a possible future endeavor. Heterostructure Bipolar Junction Transistors (HBTs) have also proven to be effective when used as power amplifiers. By changing the model development algorithm to produce HBT models, it would be possible to research the degradation mechanisms of these devices.

10.2.5 Compare DC stress measurements and Degradation as a Function of Frequency

By design the DUT was stressed in a manner to reproduce conditions that the DUT would observe when operated as a microwave amplifier. As a result, a body of data was produced that describe how a device changes under these conditions. If it were

possible to reproduce the same changes using only direct current power supplies and measurements, the cost of performing these reliability measurements could be significantly reduced and the number of devices measured could be increased. One of the future avenues of research would be to determine if the same decline in device performance is produced when the DUT is operated at the same current and voltage levels using only DC power supplies.

If DC stresses do not reproduce the same type of degradation, this would indicate that RF power degrades the device differently than DC. If this is true, the next step would be to determine the relationship between the frequency of the incident power and reliability.

The new system developed in this research is capable of producing voluminous amounts of data during reliability measurements. This data has been useful to some material physicists, device designers, and microwave engineers. It is the hope of the author that the system will continue to prove useful in the future.

Appendix A: Matrix Conversions

This appendix contains the Conversions between two-port matrix linear representations that were used in this research

The conversion from S-parameters to T-parameters is shown in (A1) [31]:

$$T_{11} = \frac{1}{S_{21}} \qquad T_{12} = -\frac{S_{22}}{S_{21}} \tag{A1}$$

$$T_{21} = \frac{S_{11}}{S_{21}} \qquad T_{22} = S_{12} - \frac{S_{11}\,S_{22}}{S_{21}}$$

The reverse from T-parameters to S-parameters is shown in (A2) [31]:

$$S_{11} = \frac{T_{21}}{T_{11}} \qquad S_{12} = T_{22} - \frac{T_{21}\,T_{12}}{T_{21}} \tag{A2}$$

$$S_{21} = \frac{1}{T_{11}} \qquad S_{22} = -\frac{T_{12}}{T_{11}}$$

The conversion from S-parameters to Y-parameters is shown in (A3) [31]:

$$Y_{11} = Y_0 \frac{(1-S_{11})(1+S_{22})+S_{21}S_{12}}{(1+S_{11})(1+S_{22})-S_{21}S_{12}} \qquad Y_{12} = Y_0 \frac{-2\,S_{12}}{(1+S_{11})(1+S_{22})-S_{21}S_{12}} \tag{A3}$$

$$Y_{21} = Y_0 \frac{-2\,S_{21}}{(1+S_{11})(1+S_{22})-S_{21}S_{12}} \qquad Y_{22} = Y_0 \frac{(1+S_{11})(1-S_{22})+S_{21}S_{12}}{(1+S_{11})(1+S_{22})-S_{21}S_{12}}$$

where Y_0 is the characteristic admittance of the network.

The conversion between Y-parameters to S-parameters is shown in (A4) [32]:

$$S_{11} = \frac{(Y_0-Y_{11})(Y_0+Y_{22})+Y_{21}Y_{12}}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{21}Y_{12}} \qquad S_{12} = \frac{-2\,Y_{12}\,Y_0}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{21}Y_{12}} \tag{A4}$$

$$S_{21} = \frac{-2\,Y_{21}\,Y_0}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{21}Y_{12}} \qquad S_{22} = \frac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{21}Y_{12}}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{21}Y_{12}}$$

The conversion between S-parameters to Z-parameters is shown in (A5) [32]:

$$Z_{11} = Z_0\frac{(1+S_{11})(1-S_{22})+S_{21}S_{12}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}} \qquad Z_{12} = Z_0\frac{2\,S_{12}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}} \quad \text{(A5)}$$

$$Z_{21} = Z_0\frac{2\,S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}} \qquad Z_{22} = Z_0\frac{(1-S_{11})(1+S_{22})+S_{21}S_{12}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}}$$

where Z_0 is the characteristic impedance of the network.

The conversion between Z-parameters to S-parameters is shown in (A6) [32]:

$$S_{11} = \frac{(Z_{11}-Z_0)(Z_{22}+Z_0)+Z_{12}Z_{21}}{(Z_0+Z_{11})(Z_0+Z_{22})-Z_{21}Z_{12}} \qquad S_{12} = \frac{2\,Z_{12}\,Z_0}{(Z_0+Z_{11})(Z_0+Z_{22})-Z_{21}Z_{12}} \quad \text{(A6)}$$

$$S_{21} = \frac{2\,Z_{21}\,Z_0}{(Z_0+Z_{11})(Z_0+Z_{22})-Z_{21}Z_{12}} \qquad S_{22} = \frac{(Z_{11}-Z_0)(Z_{22}+Z_0)+Z_{12}Z_{21}}{(Z_0+Z_{11})(Z_0+Z_{22})-Z_{21}Z_{12}}$$

The conversion between S-parameters to H-parameters is shown in (A7) [31]:

$$H_{11} = Z_0\frac{(1+S_{11})(1+S_{22})-S_{21}S_{12}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}} \quad H_{12} = \frac{2\,S_{12}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}} \quad \text{(A7)}$$

$$H_{21} = \frac{-2\,S_{21}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}} \qquad H_{22} = \frac{1}{Z_0}\frac{(1-S_{11})(1+S_{22})+S_{21}S_{12}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}}$$

The conversion between H-parameters to S-parameters is shown in (A8) [31].:

$$S_{11} = \frac{\left(\frac{H_{11}}{Z_0}-1\right)(H_{22}\,Z_0+1)-H_{21}H_{12}}{\left(\frac{H_{11}}{Z_0}+1\right)(H_{22}\,Z_0+1)-H_{21}H_{12}} \quad S_{12} = \frac{2\,H_{12}}{\left(\frac{H_{11}}{Z_0}+1\right)(H_{22}\,Z_0+1)-H_{21}H_{12}} \quad \text{(A8)}$$

$$S_{21} = \frac{-2\,H_{21}}{\left(\frac{H_{11}}{Z_0}+1\right)(H_{22}\,Z_0+1)-H_{21}H_{12}} \quad S_{22} = \frac{\left(\frac{H_{11}}{Z_0}+1\right)(1-H_{22}\,Z_0)+H_{21}H_{12}}{\left(\frac{H_{11}}{Z_0}+1\right)(H_{22}\,Z_0+1)-H_{21}H_{12}}$$

There is also a simple conversion between two-port Z-matrices to the two-port Y-matrices (A9):

$$Y_{2\times2} = Z_{2\times2}{}^{-1} \tag{A9}$$

The ability to measure and manipulate S-parameters and other parameters used to characterize two-port networks is a basic required skill for the development of device models.

Appendix B: Data Files

This appendix contains data files that were generated by the ALERTs System.

B1. This is data from the extended stress measurement file. The data have been shortened in the interest of saving space.

10-Mar-2010 09:38:58

Date	Time	VDS	VGS	IDS(mA)	IGS(uA)	PIN	POUT	GAIN	ColecEff	PAEff
4281	20.00	-4.80	158.66	-1100.199951	23.41	31.05	7.63	40.12	33.15	
4581	20.00	-4.80	159.40	-1042.800049	23.46	31.07	7.61	40.11	33.10	
4881	20.00	-4.80	159.86	-1010.600037	23.48	31.07	7.59	40.01	32.99	
5181	20.00	-4.80	159.84	-989.060059	23.49	31.07	7.58	40.01	32.97	
5481	20.00	-4.80	159.76	-973.840027	23.49	31.06	7.58	39.99	32.95	
5781	20.00	-4.80	159.78	-951.859985	23.49	31.07	7.57	39.99	32.95	
6081	20.00	-4.80	159.76	-936.640015	23.49	31.06	7.57	39.94	32.90	
6381	20.00	-4.80	159.80	-934.640015	23.50	31.06	7.56	39.93	32.88	
6681	20.00	-4.80	159.84	-922.739990	23.50	31.06	7.56	39.91	32.86	
6981	20.00	-4.80	159.96	-926.820007	23.50	31.06	7.56	39.85	32.81	
7281	20.00	-4.80	159.76	-924.420044	23.50	31.05	7.55	39.89	32.83	
7581	20.00	-4.80	159.86	-917.200012	23.50	31.05	7.55	39.86	32.81	
7881	20.00	-4.80	159.90	-909.420044	23.50	31.05	7.55	39.81	32.77	
8181	20.00	-4.80	159.90	-897.440002	23.50	31.05	7.54	39.79	32.74	
8481	20.00	-4.80	159.88	-902.220032	23.50	31.05	7.55	39.79	32.75	
8781	20.00	-4.80	159.64	-908.520020	23.50	31.04	7.54	39.81	32.76	
9081	20.00	-4.80	159.90	-887.320007	23.50	31.04	7.54	39.72	32.67	
9381	20.00	-4.80	159.80	-880.279968	23.50	31.04	7.54	39.75	32.70	
9681	20.00	-4.80	159.80	-877.399963	23.50	31.04	7.54	39.76	32.71	
9981	20.00	-4.80	159.98	-868.500000	23.50	31.04	7.54	39.70	32.65	
10281	20.00	-4.80	159.78	-871.880005	23.50	31.04	7.54	39.75	32.70	
10581	20.00	-4.80	159.92	-867.440002	23.50	31.04	7.53	39.70	32.65	
10881	20.00	-4.80	159.88	-860.580017	23.50	31.04	7.54	39.70	32.66	
11181	20.00	-4.80	159.92	-865.979980	23.50	31.04	7.54	39.70	32.65	
11481	20.00	-4.80	159.92	-860.959961	23.50	31.03	7.54	39.66	32.62	
11781	20.00	-4.80	159.78	-846.760010	23.49	31.03	7.53	39.66	32.62	
12081	20.00	-4.80	160.06	-852.820007	23.49	31.03	7.54	39.59	32.57	
12381	20.00	-4.80	159.60	-851.119995	23.49	31.03	7.53	39.69	32.64	
12681	20.00	-4.80	159.76	-854.880005	23.50	31.03	7.53	39.63	32.59	
12981	20.00	-4.80	159.84	-845.340027	23.50	31.02	7.53	39.60	32.56	
13281	20.00	-4.80	159.62	-841.179993	23.50	31.03	7.53	39.71	32.65	
13581	20.00	-4.80	159.84	-843.340027	23.50	31.03	7.53	39.63	32.60	

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B2. The text below is from a measurement summary file that records the time when each detailed measurement begins.

Device Name: ##12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2
Measurement File Name: ##12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_meas.txt

Start number: 734207.402067
Start time: 10-Mar-2010 09:38:58
Measurement interval (minutes): 360
Measurement interval (hours): 6.0
Model measurement made: 8

Model Names:

GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_0	10-Mar-2010 09:39:02
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_1	10-Mar-2010 16:45:23
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_2	10-Mar-2010 23:49:36
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_3	11-Mar-2010 06:53:45
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_4	11-Mar-2010 13:46:30
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_5	11-Mar-2010 20:50:30
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_6	12-Mar-2010 03:54:41
GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_7	12-Mar-2010 10:58:52

B3. The text below is from a turn on region DC measurement file. The data for other DC files is recorded in a similar format with additional entries.

```
##12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_0_TO_sweep
!NAMES: Vds  -6.000 -5.000 -4.000 -3.000 -2.000 -1.000  0.000  1.000
!VIEW1: XY   -6.000 -5.000 -4.000 -3.000 -2.000 -1.000  0.000  1.000 @VERSUS Vds @XL Vds
 0.0000    0.00    0.00    0.00   -0.00   -0.00   -0.00   -0.00   -0.00
 1.0000    0.00    0.00    0.06    0.17    0.20    0.20    0.21    0.21
 2.0000    0.00    0.00    0.07    0.21    0.31    0.35    0.35    0.36
 3.0000    0.00    0.00    0.08    0.23    0.34    0.41    0.44    0.44
 4.0000    0.00    0.00    0.10    0.24    0.35    0.43    0.47    0.48
 5.0000    0.00    0.00    0.12    0.25    0.35    0.44    0.48    0.50
```

B4. The text below is from a power sweep file made at the beginning of the detailed device measurement.

!TITLE:
!HEADER: TEMP.SAT,Fri Nov 13 18:47:58 2009
!FREQUENCY: 31.020 GHz
!Char.Impedances = Source: 50.00 Ohm, Load: 50.00 Ohm
!COMMENT: Freq=31.020(GHz), Gs=0.580 <Gs=167.0(deg), Gl=0.610 <Gl=96.3(deg)
!GAMMA_SR: Gs1fo=0.580<167.0(deg)
!IMPED_SR: Zs1fo=13.44+j5.29
!GAMMA_LD: Gl1fo=0.610<96.3(deg)
!IMPED_LD: Zl1fo=20.85+j40.25
!Setup: AA_setup.set, DUT REF.
!PreMatch:
!XLABEL: Pin[dBm]
!NAMES: Pin[dBm] Pout[dBm] Gain[dB] Igs[uA] Vgs[V] Ids[mA] Vds[V] Collec.Eff[%] P.A.Eff[%] P.Source1[dBm]
!UNITS:

11.16	20.36	9.20	-88.662	-4.10	138.000	20.00	3.94	3.47	-30.00
13.13	22.39	9.26	-88.926	-4.10	138.000	20.00	6.29	5.54	-28.00
15.07	24.38	9.31	-88.168	-4.10	138.000	20.00	9.95	8.78	-26.00
17.00	26.31	9.32	-85.834	-4.10	138.000	20.00	15.51	13.69	-24.00
18.84	28.06	9.23	-83.712	-4.10	140.000	20.00	22.86	20.13	-22.00
20.60	29.55	8.95	-82.944	-4.10	148.000	20.00	30.46	26.57	-20.00
22.22	30.69	8.46	-80.564	-4.10	158.000	20.00	37.07	31.78	-18.00
23.68	31.51	7.82	-81.580	-4.10	170.000	20.00	41.62	34.75	-16.00
24.93	32.02	7.09	-81.142	-4.10	180.000	20.00	44.26	35.61	-14.00
25.87	32.29	6.42	-80.446	-4.10	188.000	20.00	45.06	34.79	-12.00
26.52	32.43	5.91	-81.426	-4.10	193.000	20.00	45.31	33.68	-10.00
26.88	32.48	5.60	-79.590	-4.10	195.000	20.00	45.39	32.90	-8.00

B5. The text below is from an S-parameter file in touchstone format. The data have been shortened in the interest of saving space.

```
# GHz S MA R 50
! S2Pwrite
! 10-Mar-2010
! FREQ
```

0.48	0.995732	-8.76023	0.00461482	83.8111	0.00463669	84.6946	0.863793	179.857
0.54	0.996188	-9.87994	0.00514357	82.8054	0.0052345	83.6397	0.863522	179.881
0.6	0.995329	-10.9661	0.00569764	82.5565	0.00575917	83.2855	0.863331	179.843
0.66	0.994654	-12.0021	0.00629379	82.82	0.00632213	82.4173	0.863291	179.825
0.72	0.993739	-13	0.00684227	81.9895	0.00684577	81.9254	0.863279	179.804
0.78	0.993171	-14.0316	0.00742147	81.6556	0.00737668	81.3554	0.863555	179.78
0.84	0.992934	-15.139	0.00797444	80.7515	0.00793131	80.8072	0.863553	179.775
0.9	0.992797	-16.3404	0.00854493	80.3387	0.00850626	80.7028	0.863498	179.772
0.96	0.992087	-17.388	0.00905944	79.9111	0.0089777	79.766	0.863621	179.765
1.02	0.992137	-18.4684	0.0095585	79.6525	0.00957239	79.6218	0.863935	179.794
1.08	0.992233	-19.4571	0.0101657	78.9341	0.0101117	79.2505	0.864071	179.788
1.14	0.992128	-20.5291	0.0107011	78.3679	0.0106772	78.6335	0.863847	179.832
1.2	0.991758	-21.6355	0.0112163	77.8287	0.0112326	77.9837	0.864175	179.883
1.26	0.991089	-22.6638	0.0117402	77.4948	0.0117344	77.5165	0.86385	179.925
1.32	0.990679	-23.8041	0.0122937	76.9791	0.0123136	77.0582	0.864033	179.924
1.38	0.989699	-24.8694	0.0128638	76.4648	0.0128327	76.3248	0.863738	179.92
1.44	0.989872	-25.8946	0.0134168	75.9847	0.013365	76.041	0.863657	-179.991
1.5	0.989311	-26.9169	0.0139093	75.4656	0.0138504	75.449	0.86364	-179.958
1.56	0.988977	-27.9825	0.0144205	74.7314	0.0143831	74.8699	0.863114	-179.941
1.62	0.988715	-28.9915	0.0149228	74.3091	0.0149004	74.3281	0.863339	-179.912
1.68	0.98738	-30.0735	0.0155172	73.7412	0.0154319	73.8909	0.863533	-179.891
1.74	0.986446	-31.0945	0.0159441	73.209	0.0159022	73.3316	0.86399	-179.905
1.8	0.986824	-32.0613	0.0165102	72.6678	0.0164331	72.9462	0.863199	-179.903
1.86	0.986495	-33.0358	0.0169706	72.2302	0.0169794	72.4238	0.862717	-179.926
1.92	0.986384	-34.0253	0.0175092	71.6962	0.0174922	71.8707	0.862184	-179.96
1.98	0.984575	-35.0344	0.0179942	71.3282	0.0179687	71.3553	0.862388	-179.974
2.04	0.983756	-36.0315	0.0184592	70.7752	0.0183514	70.6639	0.862801	-179.996
2.1	0.982753	-37.0273	0.018933	70.1932	0.0188826	70.267	0.862684	179.966
2.16	0.98235	-37.9984	0.019427	69.7752	0.0193716	69.6661	0.862361	179.917
2.22	0.98238	-38.9373	0.0198807	69.0799	0.0198593	69.1383	0.862682	179.87
2.28	0.982765	-39.8711	0.0203967	68.6521	0.0203394	68.8564	0.86272	179.862
2.34	0.982412	-40.8418	0.0208578	68.0918	0.0207625	68.2425	0.862494	179.861
2.4	0.98242	-41.7334	0.0212782	67.5575	0.0212367	67.7756	0.862267	179.851
2.46	0.981399	-42.6847	0.0217011	67.1507	0.0216627	67.3817	0.862319	179.856
2.52	0.980813	-43.668	0.022224	66.5463	0.0221125	66.7343	0.86258	179.818

B6. The text below is from an IV / S-parameter summary file. The data have been shortened in the interest of saving space.

Dev Name:!NAMES: GN12R-174_R3C2_GHW8500P_1GS1P5GD_25C_J26_2_0_VGS_sweep

VDS	VGS	IDS	IGS	RF gm(mS)	fT	fMax
9.80	-6.00	0.00	-0.00	0.37	8.33	0.09
10.00	-6.00	0.00	-0.00	0.37	8.29	0.08
10.20	-6.00	0.00	-0.00	0.36	8.25	0.09
9.80	-5.80	0.00	-0.00	0.37	8.16	0.09
10.00	-5.80	0.00	-0.00	0.37	8.13	0.09
10.20	-5.80	0.00	-0.00	0.36	8.10	0.09
9.80	-5.60	0.00	-0.00	0.39	7.95	0.23
10.00	-5.60	0.00	-0.00	0.40	7.93	0.25
10.20	-5.60	0.00	-0.00	0.41	7.89	0.28
9.80	-5.40	0.00	-0.00	4.82	8.34	7.79
10.00	-5.40	0.00	-0.00	5.36	8.55	9.31
10.20	-5.40	0.00	-0.00	6.14	8.79	10.87
9.80	-5.20	0.00	-0.00	33.01	24.78	51.55
10.00	-5.20	0.00	-0.00	36.33	27.06	55.87
10.20	-5.20	0.01	-0.00	39.15	28.86	59.15
9.80	-5.00	0.02	-0.00	73.32	50.86	90.84
10.00	-5.00	0.02	-0.00	75.45	52.11	92.78
10.20	-5.00	0.02	-0.00	77.11	53.00	94.19
9.80	-4.80	0.05	-0.00	92.86	62.74	105.06
10.00	-4.80	0.05	-0.00	93.55	62.98	105.63
10.20	-4.80	0.05	-0.00	94.08	63.20	106.36
9.80	-4.60	0.07	-0.00	99.23	66.48	108.35
10.00	-4.60	0.08	-0.00	99.52	66.44	108.88
10.20	-4.60	0.08	-0.00	99.76	66.41	109.25
9.80	-4.40	0.10	-0.00	100.77	67.37	108.33
10.00	-4.40	0.10	-0.00	100.92	67.31	108.60
10.20	-4.40	0.10	-0.00	101.11	67.19	108.98
9.80	-4.20	0.13	-0.00	100.36	67.16	106.94
10.00	-4.20	0.13	-0.00	100.48	67.01	107.27
10.20	-4.20	0.13	-0.00	100.59	66.90	107.59
9.80	-4.00	0.16	-0.00	98.98	66.45	105.00
10.00	-4.00	0.16	-0.00	99.09	66.34	105.28
10.20	-4.00	0.16	-0.00	99.21	66.21	105.69
9.80	-3.80	0.18	-0.00	97.07	65.54	102.74
10.00	-3.80	0.18	-0.00	97.16	65.43	103.06
10.20	-3.80	0.18	-0.00	97.25	65.33	103.37
9.80	-3.60	0.21	-0.00	94.79	64.50	100.08
10.00	-3.60	0.21	-0.00	94.87	64.38	100.41
10.20	-3.60	0.21	-0.00	94.97	64.25	100.83
9.80	-3.40	0.23	-0.00	92.22	63.26	97.30
10.00	-3.40	0.23	-0.00	92.31	63.06	97.53
10.20	-3.40	0.23	-0.00	92.39	62.86	97.88
9.80	-3.20	0.25	-0.00	89.46	61.77	94.22
10.00	-3.20	0.25	-0.00	89.52	61.64	94.71
10.20	-3.20	0.25	-0.00	89.63	61.56	95.03
9.80	-3.00	0.27	-0.00	86.51	60.39	91.30
10.00	-3.00	0.27	-0.00	86.58	60.29	91.62
10.20	-3.00	0.27	-0.00	86.64	60.21	91.92
9.80	-2.80	0.29	-0.00	83.39	58.95	88.04
10.00	-2.80	0.29	-0.00	83.46	58.84	88.44
10.20	-2.80	0.29	-0.00	83.54	58.77	88.83
9.80	-2.60	0.31	-0.00	80.16	57.42	84.78
10.00	-2.60	0.31	-0.00	80.25	57.40	85.18
10.20	-2.60	0.31	-0.00	80.32	57.30	85.54
9.80	-2.40	0.33	-0.00	76.80	55.81	81.42
10.00	-2.40	0.33	-0.00	76.88	55.78	81.85
10.20	-2.40	0.33	-0.00	76.94	55.71	82.23
9.80	-2.20	0.35	-0.00	73.28	54.10	77.90
10.00	-2.20	0.35	-0.00	73.39	54.11	78.30
10.20	-2.20	0.35	-0.00	73.47	54.06	78.73

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B7. The text below is from a gate sweep measurement data file

VGS	VDS	IGS	IDS
-7.0004	4e-005	-0.00048536	0.00016466
-6.8	4e-005	-0.000474	0.00016254
-6.5992	4e-005	-0.0004621	0.0001592
-6.4004	8e-005	-0.00044786	0.00015562
-6.2004	4e-005	-0.00043514	0.00015244
-6.0004	4e-005	-0.00042288	0.00014868
-5.8016	8e-005	-0.0004109	0.00014542
-5.6008	8e-005	-0.00039698	0.00014188
-5.4	4e-005	-0.00038472	0.0001396
-5.2012	4e-005	-0.0003726	0.00013494
-5.0008	4e-005	-0.0003609	0.00013182
-4.8008	4e-005	-0.00034808	0.00013872
-4.6	8e-005	-0.00033256	0.000100968
-4.4004	0.00016	-0.00032046	5.9614e-005
-4.2008	8e-005	-0.00030552	4.9792e-005
-4.0004	-4e-005	-0.0002884	4.152e-005
-3.8008	0.00012	-0.00027286	3.7544e-005
-3.6008	8e-005	-0.00025516	4.4684e-006
-3.4	0.00016	-0.00023654	3.3716e-007
-3.2012	0.00016	-0.00021772	-2.0362e-005
-3	0.00024	-0.0001986	-1.1988e-005
-2.8	8e-005	-0.00017938	-3.487e-005
-2.5992	0.00016	-0.00016054	-2.8756e-005
-2.3992	8e-005	-0.00014248	-2.6772e-005
-2.1992	8e-005	-0.00012528	-3.9658e-005
-2.00012	0.00024	-0.00010908	-3.6722e-005
-1.80012	-0.00016	-9.3206e-005	-4.5948e-005
-1.60016	0.00012	-7.7752e-005	-5.4368e-005
-1.4002	8e-005	-6.3474e-005	-7.8326e-005
-1.20032	-0.00012	-4.9232e-005	-6.539e-005
-1.00036	8e-005	-3.5994e-005	-6.5724e-005
-0.8002	-8e-005	-2.449e-005	-6.4722e-005
-0.60024	0.00016	-1.4988e-005	-7.702e-005
-0.4002	0.00016	-7.789e-006	-9.7752e-005
-0.20008	0.00016	-2.993e-006	-8.802e-005
0.00012	0.0002	1.1158e-008	-9.2506e-005
0.2	0.00024	4.1264e-006	-8.1552e-005
0.39996	0.00016	1.9602e-005	-8.9044e-005
0.6	0	7.8884e-005	-0.00011582
0.79988	8e-005	0.00025962	-0.00016138
1	8e-005	0.0006706	-0.00032306
1.20008	0.00012	0.0014354	-0.00058918
1.4	-8e-005	0.0025498	-0.00095878
1.59992	8e-005	0.0031256	-0.0011802
1.79996	4e-005	0.0033524	-0.0012042
2.00004	8e-005	0.0031566	-0.0012352
2.2008	8e-005	0.0014354	-0.00054156

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