ABSTRACT

Title of dissertation: CHARACTERIZATION OF METAL-OXIDE-SEMICONDUCTOR STRUCTURES AT LOW TEMPERATURES USING SELF-ALIGNED AND VERTICALLY COUPLED ALUMINUM AND SILICON SINGLE-ELECTRON TRANSISTORS

Luyan Sun, Doctor of Philosophy, 2008

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I incorporate an Al-AlO_x-Al single-electron transistor (SET) as the gate of a narrow ($\sim$ 100 nm) metal-oxide-semiconductor field-effect transistor (MOSFET). Near the MOSFET channel conductance threshold, Coulomb blockade oscillations are observed at about 20 millikelvin, revealing the formation of a Si SET at the Si/SiO_2 interface. Based on a simple electrostatic model, the two SET islands are demonstrated to be closely aligned, with an inter-island capacitance approximately equal to 1/3 of the total capacitance of the Si transistor island, indicating that the Si transistor is strongly coupled to the Al transistor. This vertically-aligned Al and Si SET system is used to characterize the background charges in a MOS structure at low temperature, which may also be sources of decoherence for Si quantum computation. A single charge defect, probably either a single charge trap at the Si/SiO_2 interface or a single donor in the Si substrate, is detected and the properties of the defect are studied in this dissertation.

CHARACTERIZATION OF METAL-OXIDE-SEMICONDUCTOR STRUCTURES AT LOW TEMPERATURES USING SELF-ALIGNED AND VERTICALLY COUPLED ALUMINUM AND SILICON SINGLE-ELECTRON TRANSISTORS

by

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To my wife and our parents $\cdots$

Acknowledgments

After a long time in graduate school, it has finally come to the point of writing this acknowledgement. When I look back, I realize this would not have been possible without the help and support from many others. I am truly indebted to them.

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List of Abbreviations

AC	Alternative Current
CTC	Center-To-Center
DI	Deionized
DC	Direct Current
DIP	Dual In-line Package
E-Beam	Electron Beam
ESR	Electron Spin Resonance
FEMLAB	Finite Element Method LABoratory
FET	Field-Effect Transistor
HMDS	Hexamethyldisilazane
IPA	IsoPropyl Alcohol
LS	Line Spacing
MBE	Molecular Beam Epitaxy
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NIST	National Institute of Standards and Technology
NPGS	Nanometer Pattern Generation System
op-amp	Operational Amplifier
PCB	Printed Circuit Board
PMGI	Polymethylglutarimide
PMMA	Poly-Methyl Methacrylate
QC	Quantum computer or Quantum Computing
QD	Quantum Dot
RFSET	Radio Frequency Single-Electron Transistor
RIE	Reactive Ion Etching
RPM	Round Per Minute
RTA	Rapid Thermal Anneal
RTS	Random Telegraph Signal
SEM	Scanning Electron Microscope
SET	Single-Electron Transistor
SOI	Silicon-On-Insulator
SRIM	the Stopping and Range of Ions in Matter
TLF	Two-Level Fluctuator

Chapter 1

Introduction

1.1 Manipulation of single donor electrons in silicon

As the miniaturization of semiconductor devices continues according to Moore's law, semiconductor technology will eventually reach a point where individual devices need to manipulate single atoms or electrons. Well before reaching that point, the laws of classical mechanics governing current microelectronics start to fail and quantum effects begin to show up. A quantum computer (QC), a computer composed of devices with explicit quantum properties, is considered as a natural and promising alternative to go beyond classical computers. Because of quantum entanglement and true parallel computation, a QC would be much more powerful than its classical counterpart for certain problems.[1, 2]

Quantum computers have been proposed based on a wide variety of physical systems, including superconductors,[3, 4] trapped ions,[5, 6] quantum dots,[7] molecules,[8] electron spins,[9] and nuclear spins.[10] Among them, semiconductor spin qubits are of particular interest because of their scalability and compatibility with well-established semiconductor techniques used for conventional computers. To realize quantum computation in semiconductors, logical operations need to be performed on isolated single electrons. Recently tremendous progress on manipulation of isolated electrons confined in electrostatically defined quantum dots (QD) has

been made in GaAs [11, 12] and in SiGe.[13] However, electrons can also be confined on isolated donors in silicon. In silicon, a donor such as phosphorus is a substitutional atom with an extra electron confined by a hydrogenic potential. Because the confinement potential an electron experiences at a donor site is well-defined, at least in principle all qubits can be identical, eliminating the variability inevitably present in the QD case. In addition, electron and nuclear spins in silicon have much longer coherence times than in GaAs for two main reasons: first, the spin-orbit interaction in silicon is much weaker than in GaAs; second, ^{28}Si, the most abundant isotope of silicon, has zero nuclear spins while neither Ga nor As has nuclear spin-free isotopes. The electron spin coherence time in isotopically purified ^{28}Si substrate can be as long as 62 ms,[14] while the coherence time of ^{31}P nuclear spins can exceed 1 s at 5.5 K.[15] A significant advantage of donor based QC architectures is that they can potentially be fabricated using conventional Si processing techniques and utilize SiO_2 as a barrier material.

One particularly important issue for all QCs is the final state readout. For spin-based QCs, readout is realized through a spin-to-charge conversion, a scheme to convert spin information to charge information through the Pauli exclusion principle, because direct measurement of single spins is difficult and slow [17] while detection of charge is much easier and faster. In a recent experiment in Marcus's group at Harvard,[11] a measurement of the spin state of a two-electron system in two closely coupled QDs in GaAs was demonstrated by detecting the presence or absence of a tunneling event between the two QDs. To establish the feasibility of a QC based on donor impurities in silicon, Kane proposed an experiment to measure the spin

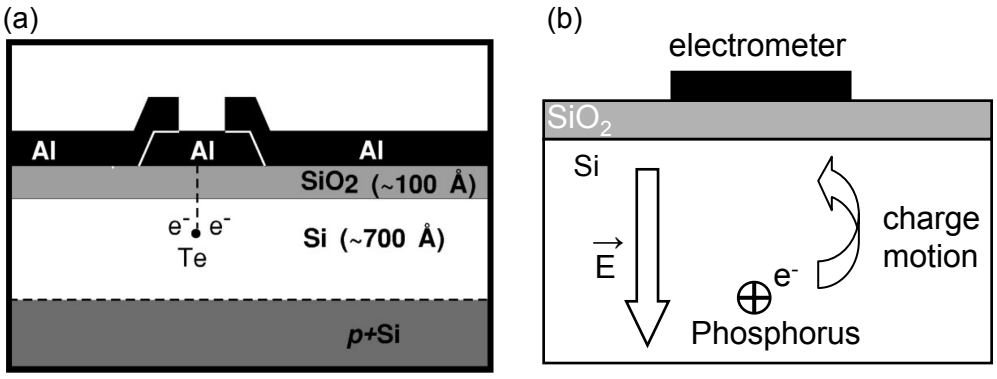


Figure 1.1: (a) Schematic of spin state detection of a two-electron system on a tellurium double donor in silicon with an Al single-electron transistor on the surface. The electric field required to ionize one of the electrons depends on whether the two electrons are in a singlet or triplet state. (b) Schematic of charge motion detection. Under an external electric field, the single donor electron could be ionized and be pushed towards the Si/SiO_2 interface. Such charge motion could be detected by a nearby sensitive electrometer, *e.g.* an SET. ((a) is reprinted from Reference [16].)

state of a two-electron system on a tellurium double donor in silicon [16] as depicted in Fig. 1.1(a). The electric field required to ionize one of the electrons depends on whether the two electrons are in a singlet or triplet state. The motion of the electron after it ionizes could be measured by a single-electron transistor (SET) on the surface. Clearly, in donor based Si QC architectures the ability to measure the motion of a single electron between a donor site and the interface is essential. For reasons of simplicity, work in our lab has focused on the detection of single phosphorus donors instead of tellurium in silicon as depicted in Fig. 1.1(b). Also our research has centered on the development of single charge sensors in the Si/SiO_2 system.

Ultimately, the charge detection of single donor electrons in Si/SiO_2 will be limited by intrinsic characteristics of this system. Due to the amorphous nature of SiO_2, there is inevitable disorder at the Si/SiO_2 interface or even trapped charges in the oxide. The unwanted imperfections will lead to two main obstacles for the charge motion detection of single donor electrons. First, the electric field at the donor sites is not precisely known, because any background charge motion could change the electric field locally and cause noise and hysteresis which will complicate the detection. Second, donor electrons have to be there in the first place for ionization measurement, but there is no certainty that donor sites are occupied. For example, the interface states or the residual acceptors can trap electrons from nearby donors, or the negative charges trapped at the interface or in the oxide can bend the silicon band to deplete the donor electrons. Therefore a way to control the Fermi level at the donor sites is required such that selective population or depopulation of individual

donor electrons can be performed.

1.2 Vertically coupled Al and Si SETs and characterization of MOS structures

The underlying physics of Si/SiO_2 systems has to be well understood before any charge detection can be performed. Locating and eliminating unwanted charge sources is not only important for the charge motion detection of single donor electrons and spin measurement, but also significant for the improvement of conventional and quantum logic devices as the device size scale approaches the single electron regime. For example, mobile charges or unpaired spins can lead to decoherence.[18, 19]

An SET coupling to a conducting channel at the Si/SiO_2 interface can provide a useful probe at low temperatures of the imperfections in the Si/SiO_2 system and of the channel behavior near the channel threshold. Furthermore, the Fermi level at the interface can be well controlled externally. Finally, because both the Al SET and the Si channel conductance can be measured independently, the Si channel conductance can yield extra information about the interface.

This thesis describes my efforts to study the background charges in a Si/SiO_2 system. To do this, I incorporate an Al-AlO_x-Al SET as the gate of a narrow silicon metal-oxide-semiconductor field effect transistor (MOSFET), as depicted in Fig. 1.2. Near the MOSFET channel conductance threshold, I find Coulomb blockade oscillations in the conductance, revealing the formation of an SET in the Si channel

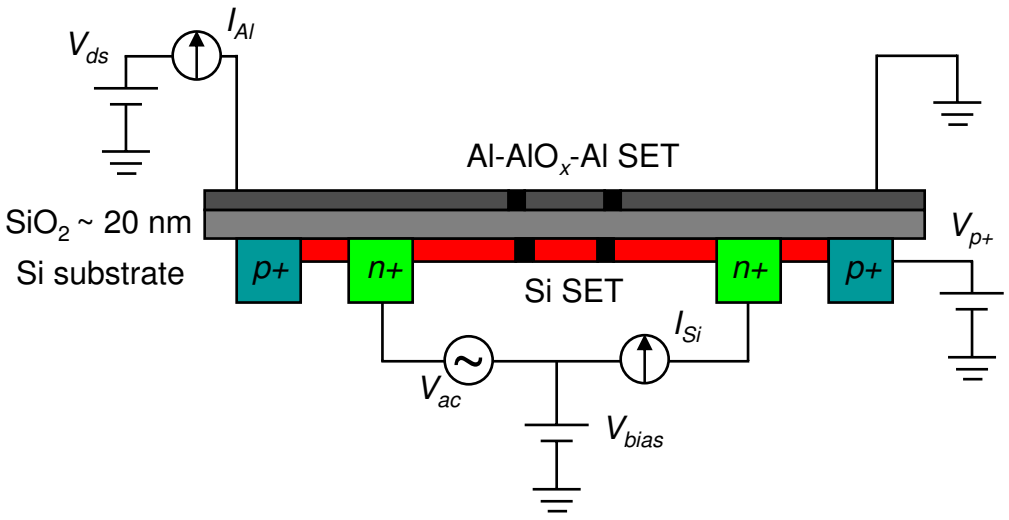


Figure 1.2: Schematic of back-to-back SETs (not to scale). Under proper relative bias V_{bias}, an Al-AlO$_x$-Al SET acts as the gate of a narrow silicon MOSFET and can induce a Si SET at the Si/SiO$_2$ interface which is vertically aligned with the Al SET. The n+ contacts provide an ohmic contact to the Si SET while p+ contacts can confine the Si SET between them. The current through each SET, I_{Al} and I_{Si}, can be measured independently using two external circuits under different biases V_{ds} and V_{ac} respectively.

at the Si/SiO_2 interface. The Si SET is proved to be vertically aligned with the Al SET with an inter-island capacitance approximately equal to 1/3 of the total capacitance of the Si SET island, indicating that the Si SET is strongly coupled to the Al SET. Strong coupling means the capacitance between the two SET islands is a significant fraction of the total capacitance of at least one of the islands. I use this SET sandwich architecture to probe and identify sources of defect charges in a MOS structure via a cross-correlation measurement between the two SETs. In particular, I detected and studied a single charge defect at the Si/SiO_2 interface. Results on the SET sandwich device will constitute the bulk of this dissertation.

1.3 Dissertation outline

Chapter 2 contains an introduction to SETs, followed by a brief review of Si SETs fabricated by different approaches in different groups. Then I discuss the calculation of the electrostatic energy of two capacitively coupled SETs using two methods: the conventional approach to calculate energies stored in capacitors, and a simpler approach based on charge and capacitance matrices. The difference between the two methods is also discussed. Finally, I discuss the resulting hexagonal phase diagram of the two capacitively coupled SETs with explicit formulas for all the important parameters associated with the hexagons.

In Chap. 3, I discuss the imperfections in a Si/SiO_2 system and review some properties of these imperfections, in particular the interface states and donor states in Si. I also review different approaches to probe these imperfections using a single

SET or coupled SETs.

In Chap. 4, I present details of my recipe for device fabrication and how I wire them up. All the steps are standard including Si thermal oxidation, ion implantations for electrical contacts, rapid thermal anneal for activation of dopants and double-angle evaporation of Al SETs.

In Chap. 5, I present results on a control experiment with an Al narrow wire instead of an Al SET as the top gate to test the integrity of the SiO_2 layer and the confinement of the electron channel within the outside p+ contacts. The experiment was performed in a dipstick at 4 K. The conduction of the dopants, the channel threshold, and the electron mobility are also addressed.

In Chap. 6, I incorporate an Al-AlO_x-Al SET as the gate of a narrow silicon MOSFET to induce a Si SET at the Si/SiO_2 interface near the channel threshold. A simple electrostatic model is used to describe the coupling between the Al and Si SETs. It is found that the two SET islands are closely aligned with an inter-island capacitance approximately equal to 1/3 of the total capacitance of the Si SET island. Possible explanations of the alignment are discussed, followed by a brief study of the channel in the high conducting regime which shows similar vertical alignment of an Al and Si SET system.

In Chap. 7, I present how I use the vertically coupled Al and Si SET system discussed in Chap. 6 to characterize a MOS structure at low temperature. I show that some charge motion is detected by both SETs. After ruling out a two-level-fluctuator in our system, I conclude that the charge motion corresponds to a single charge defect tunnel-coupled to the Si SET, probably either a single charge trap

at the Si/SiO_2 interface or a single donor in the Si substrate. Using a similar electrostatic model as in Chap. 6, the properties of the single charge defect are extracted and studied.

In Chap. 8, I present a different method to detect the ionization of single donor electrons in Si by using an Al SET gated by lateral PtSi Schottky gates. A PtSi Schottky gate can provide an abrupt transition from a conducting layer to intrinsic Si without introducing unwanted impurities. In addition, it has a barrier height about an order of magnitude smaller than SiO_2, allowing injection of electrons and holes into the Si substrate. By studying the Coulomb blockade period of the Al SET while sweeping the Schottky gates, I have identified the flat band voltage and accumulation of electrons and holes at the Si/SiO_2 interface under the Al SET island. PtSi Schottky gates seem promising for measurement of field ionization of single donors in Si, an essential ingredient for Si-based quantum computation and single spin measurement.

Finally, Chap. 9 summarizes my results and also addresses some ideas for future research.

Chapter 2

Single-electron transistors and electrostatics of capacitively coupled single-electron transistors

2.1 Single electron transistors

Single-electron transistors (SETs) can be used as very sensitive electrometers, able to detect a small fraction of an electron charge, with a sensitivity around $10^{-6}\ e/\sqrt{\text{Hz}}$ at frequencies above the 1/f noise floor.[20] They have been extensively studied for metrology [21] and may have applications in quantum information processing.[7, 9, 10, 16, 22, 23, 24, 25] Reference [26] is a good introduction to SETs.

An SET is a three terminal device consisting of an island (often but not necessary metallic) which is tunnel coupled to drain and source leads and capacitively coupled to a gate as depicted in Fig. 2.1(a). To observe Coulomb blockade effects in such a device, two requirements have to be met. First, the tunneling resistance R_T should be greater than the resistance quantum $R_Q = h/e^2 \cong 25.8\ \text{k}\Omega$, where $e = |e|$ is the absolute value of the charge of an electron and h is Planck's constant. The condition $R_T > R_Q$ ensures that the energy uncertainty $\Delta E \cong h/\tau$ of an excess electron on the SET island, associated with the lifetime $\tau = R_T C_\Sigma$ due to tunneling, is smaller than the charging energy $E_c = e^2/2C_\Sigma$, where C_Σ is the total capacitance of the SET island to the environment. This condition ensures that the wave function

of the excess electron is reasonably well-localized on the SET island.

Second, the island capacitance has to be small enough that the charging energy of a single excess electron on the island exceeds the thermal energy k_BT, where k_B is the Boltzmann constant. Nowadays, nanofabrication techniques can easily be used to fabricate a metal SET with a total island capacitance less than 1 fF, corresponding to $E_c \sim 1$ K, well above the base temperature (about 20 mK) of a dilution refrigerator .

When the above two requirements are met, the energy levels for discrete number of electrons on the SET island will be sharply quantized. Based on a constant interaction model,[27, 28] the electrostatics can be calculated as follows. The total energy of the SET island $U(N)$ biased as in Fig. 2.1(a) with N excess electrons on the island is given by:

$$U(N) = (-eN + V_{ds}C_1 + V_gC_g)^2/2C_\Sigma + \Sigma E_N \tag{2.1}$$

where ΣE_N is the sum of the occupied single-particle energy levels on the island and $C_\Sigma = C_1 + C_2 + C_g$. The effective charge on the island contains two parts: $-eN$ and the charge $(V_{ds}C_1 + V_gC_g)$ induced by the electrodes which can be tuned continuously. The electrochemical potential $\mu(N)$ is given by:

$$\mu(N) = U(N) - U(N-1) = (2N-1)E_c - 2E_c(V_{ds}C_1 + C_gV_g)/e + E_N \tag{2.2}$$

where $E_c = e^2/2C_\Sigma$ is the charging energy. The difference between the neighboring electrochemical potentials defines the so-called addition energy E_A:

$$E_A = \mu(N+1) - \mu(N) = 2E_c + \Delta E \tag{2.3}$$

where $\Delta E = E_{N+1} - E_N$ is the single-particle energy level spacing. For a sufficiently large metal island, the level spacing is small and we can ignore ΔE, so $E_A = 2E_c$ in this limit.

Figures 2.1(b) and 2.1(c) show the electrochemical potential levels in a low-bias regime $V_{ds} < E_c$, assuming $\Delta E \ll E_c$ and T = 0 K. $\Delta E \ll k_B T$ is normally the case for a metallic island with many electrons or for a relatively large semiconductor island. In this case, electron transport is possible only when there is a level within the bias window [Fig. 2.1(c)]. Otherwise there will be no current flowing through the SET [Fig. 2.1(b)]. As shown in Eq. 2.2, the electrochemical potential can be tuned continuously by gate voltage V_g, therefore the current that flows through the SET is a strong function of the electrostatic potential in the vicinity of the island, and it oscillates as a function of gate voltage V_g as shown in Fig. 2.1(d), a phenomenon known as Coulomb blockade oscillation. The period of the oscillation is

$$\Delta V_g = e/C_g \tag{2.4}$$

which can ultimately be obtained from Eq. 2.2 and Eq. 2.3.

At different V_{ds} biases, sweeping V_g will allow many Coulomb blockade oscillations to be measured. A so-called "diamond chart" of an SET can be obtained as shown in Fig. 2.1(e) by plotting the current through the SET I_{ds} as a function of V_{ds} and V_g. The shaded diamonds correspond to $I_{ds} \cong 0$. The height of each diamond (along the V_{ds} axis) is twice the charging energy of the SET divided by e, which is consistent with Eq. 2.3 with $\Delta E \ll E_c$ and ensures that there is an available level within the bias window. This is the easiest way to directly measure the charging

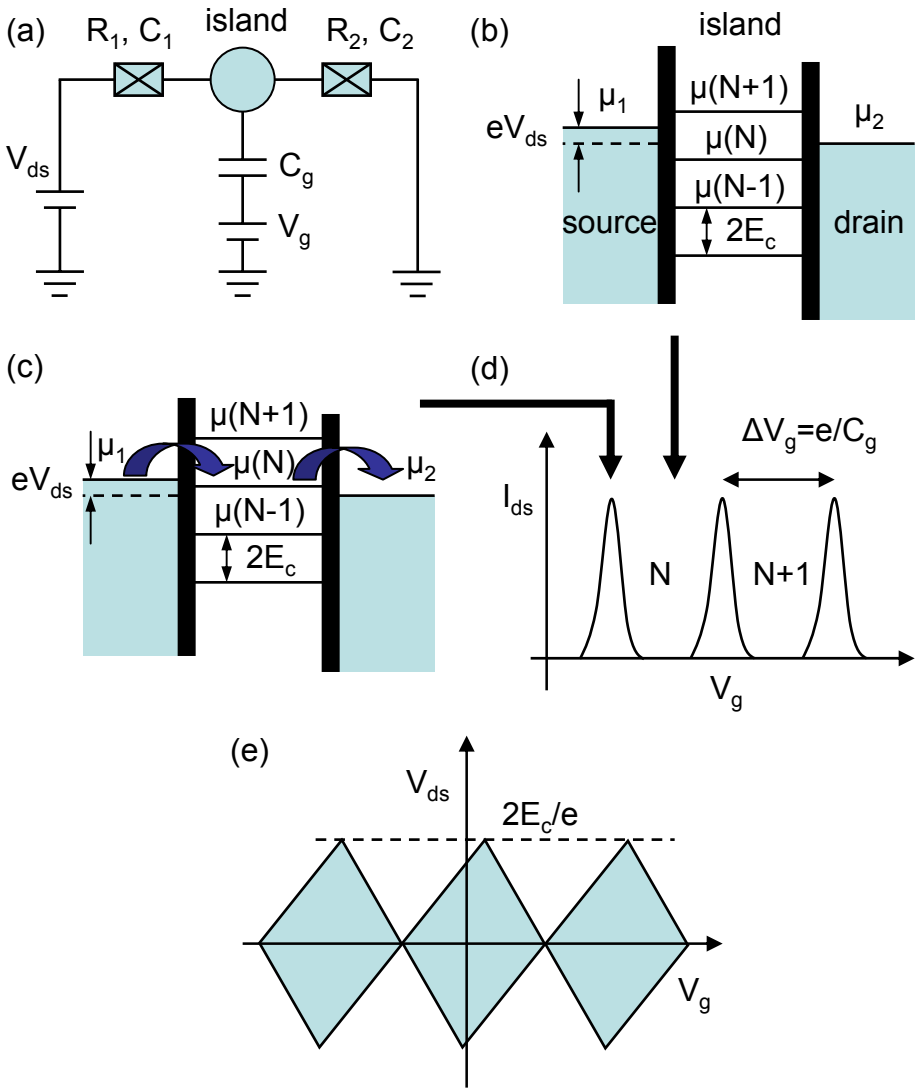


Figure 2.1: (a) Schematic of an SET under a bias V_{ds}. The island is tunnel coupled to the drain (R_1,C_1) and source (R_2,C_2) and capacitively coupled to a gate (C_g). (b) Schematic of the electrochemical potential levels of an SET in the low-bias regime and in a blocked state. (c) Schematic of the electrochemical potential levels of an SET with one available level within the small bias window (Coulomb blockade is lifted). In (b) and (c), $\mu(N)$ is the electrochemical potential with N electrons on the island. The level spacing is $2E_c$. (d) Coulomb blockade oscillations with a period of $\Delta V_g = e/C_g$. (e) Diamond chart of an SET with a height $= 2E_c/e$.

energy.

The period of the diamonds is the Coulomb blockade oscillation period $\Delta V_g = e/C_g$. The two slopes of the diamond correspond to the ratios between C_g and C_1 or C_2 and can be deduced as follows. Along the diamond edge with a positive slope S_1, the electrochemical potential is kept constant relative to the drain electrode. Based on Eq. 2.2, to have $\Delta\mu = -2E_c(\Delta V_{ds}C_1 + \Delta V_g C_g) = -e\Delta V_{ds}$, we have:

$$S_1 = C_g/(C_\Sigma - C_1) = C_g/(C_2 + C_g) \tag{2.5}$$

For the diamond edge with a negative slope S_2, the change of V_g and V_{ds} is to keep the electrochemical potential constant (relative to ground). Based on Eq. 2.2, to have $\Delta\mu = 0$, we have:

$$S_2 = -C_g/C_1 \tag{2.6}$$

Therefore, from the diamond chart we can extract all the parameters associated with the SET: C_g, C_1, C_2, C_Σ, and E_c.

2.2 Si SETs

While metal SETs are more common because of ease of fabrication (see Fig. 3.4 for a discussion of fabrication), Si SETs are desirable because of their better stability [29, 30, 31] and their ease of incorporation into Si fabrication processes and Si quantum computation architectures.[32, 33] Another potential advantage of Si SETs is that they can have a high enough operating temperature which enables potential room temperature applications. Many approaches have been used to fabricate Si

SETs. Reference [34] is a good review of silicon single-electron devices. Here I summarize some of the main techniques.

The first reported Si SET was formed in a Si inversion layer using a dual-gate geometry as depicted in Fig. 2.2(a).[35] Due to shielding of the lower gates, the universal top gate can only invert the Si band within the gap between the lower gates with a width of only a few tens of nanometers. Coulomb blockade oscillations were observed in the Si inversion channel. However, the tunnel barriers were attributed to effects from random charged impurities because there was no intentional formation of barriers from lithography and the oscillation period was not reproducible after thermal cycles to room temperature.

The dual-gate geometry has also been used by other groups.[36, 37, 38] In these devices, the conducting channels were also formed in the inversion layer on pure silicon by a top gate, but the tunnel barriers were defined electrostatically by lower gates and were tunable, as shown in Fig. 2.2(b). In the devices built by Angus *et al.*,[38] both top and lower gates are Al separated by a few-nanometer thick AlO_x dielectric layer. One of the challenges is that the AlO_x must be robust enough to not break down when a few volts is applied. These devices showed very regular Coulomb diamonds in the many-electron regime (~ 100 electrons). In the few-electron regime with ~ 10 electrons, they measured very clear excited states.

Most Si SETs have been fabricated in silicon-on-insulator (SOI) substrates because of the much stronger vertical confinement. An SOI is a structure in which a SiO_2 layer is sandwiched between a thin (5 nm to a few of tens nm) crystalline Si layer and a Si substrate. Some groups used Si etching technique and post-oxidation

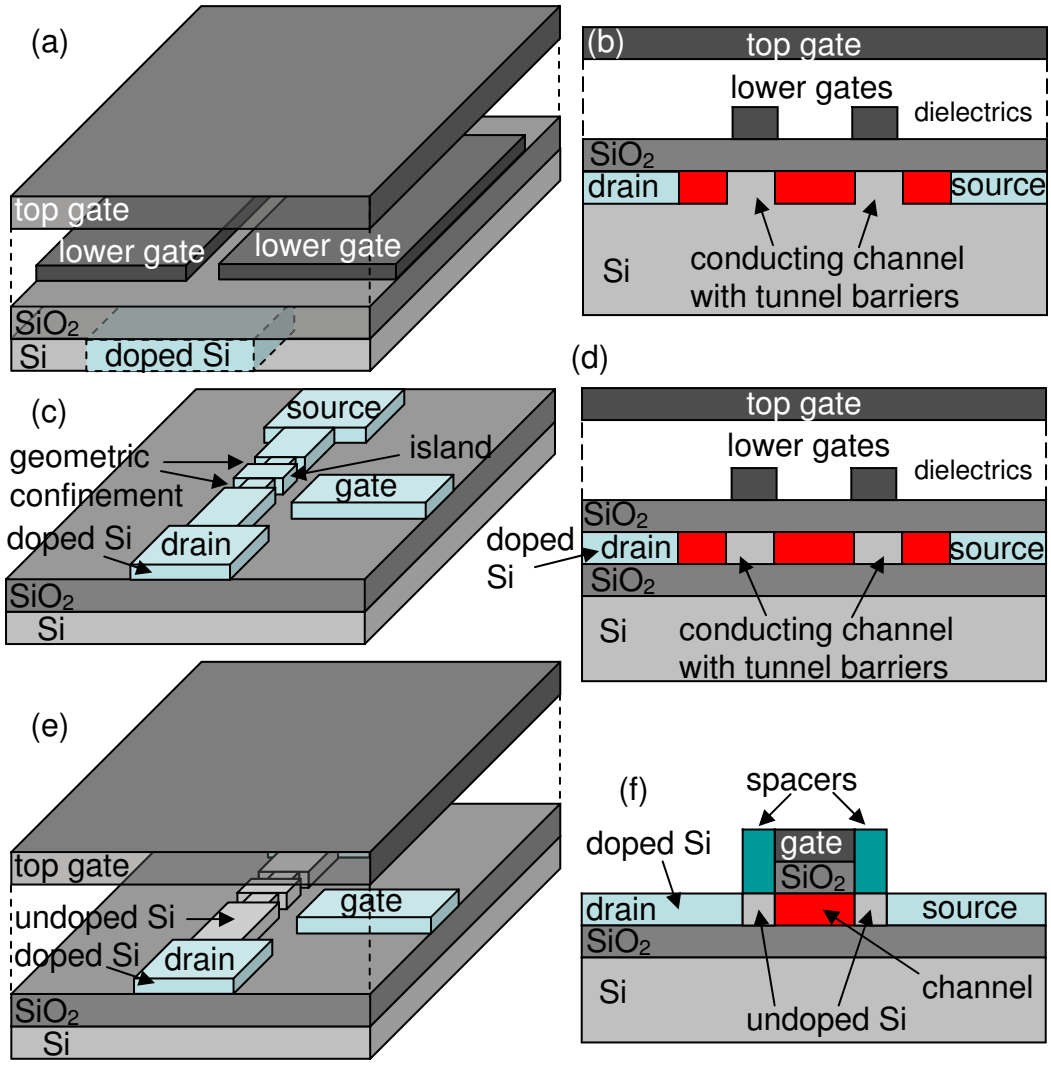


Figure 2.2: Different approaches to Si SETs. (a) Dual-gate geometry. Long and narrow Si channel is formed between the lower gates. (b) Dual-gate geometry (side view). Tunnel barriers are defined electrostatically. (c) Doped SOI substrate. Tunnel barriers are defined by patterning of Si layer. (d) Undoped SOI substrate (side view). Tunnel barriers are defined using electrostatic gates, similar to (b). (e) Undoped SOI substrate. Tunnel barriers are defined by geometric confinement. (f) Doped SOI nanowire (side view). Spacers prevent the Si nanowire underneath from doping to form fixed tunnel barriers.

to fabricate Si SETs on a highly doped [39, 40, 41] or even quasimetallic [42] SOI substrate as depicted in Fig. 2.2(c). Because the Si channel conducts at low temperature in this case, a gate is not required to induce carriers. However, the high density of dopants in the channel will typically form multiple tunnel barriers, so instead of just one SET, there could be many SETs in series in the channel. In this approach, a nearby gate (side, top, or bottom) potential has to be high enough to raise the Fermi level above the randomly formed tunnel barriers from dopants such that only barriers from the geometric confinement (the confinement of the channel by narrow lateral constrictions) or structural roughness remain active.

Other groups have used undoped SOI substrates and ion-implantation for the drain/source formation. In this case, a top gate has to be used to induce a conducting channel at low temperature. The tunnel barriers of the SET can be defined by multiple lower gates electrostatically, as in Fig. 2.2(d),[43] by geometric confinement as in Fig. 2.2(e),[44] or by dopant modulation spacers as in Fig. 2.2(f).[45] The benefit of the first case (to define tunnel barriers electrostatically) is the capability of tuning the barrier height externally, while in the other two cases the tunnel barriers are fixed. For the third case with dopant modulation spacers, only one top gate is required since the spacers can be made narrow enough for electrons to tunnel through.

2.3 Electrostatics of capacitively coupled SETs

In the previous sections I discussed the behavior of a single isolated SET. Here I discuss the case where two or more SETs are coupled together capacitively (see Fig. 2.3). The two SETs are biased relatively to each other, but each SET is under no drain-source bias, $V_{ds} = 0$. Because the drain and source leads of each SET are at the same potential, for simplicity, I will consider the two tunnel junctions of each SET to be just a single junction with resistance and capacitance, R_1, C_1 and R_2, C_2 respectively, where C_1 and C_2 are the sum of the two tunnel capacitances of each SET respectively.

2.3.1 Conventional approach

To analyze the case of two coupled SETs, I use a conventional capacitor network model to calculate the electrostatic energies. Reference [46] discusses the case for a single SET only. All parameters are defined as in Fig. 2.3. I assume that there are N_1 and N_2 excess electrons on the SET1 and SET2 islands, respectively. Then we have:

$$-N_1 e = -Q_1 + Q_3 + Q_c + Q_{g1}$$

$$-N_2 e = Q_2 + Q_4 - Q_c + Q_{g2}$$

For each capacitor, we simply have $Q = C\Delta V$, where ΔV is the voltage drop across the capacitor. Then the above equations become:

$$-N_1 e = C_1 V_1 + C_3(V_1 - V) + C_c(V_1 - V_2) + C_{g1}(V_1 - V_g)$$

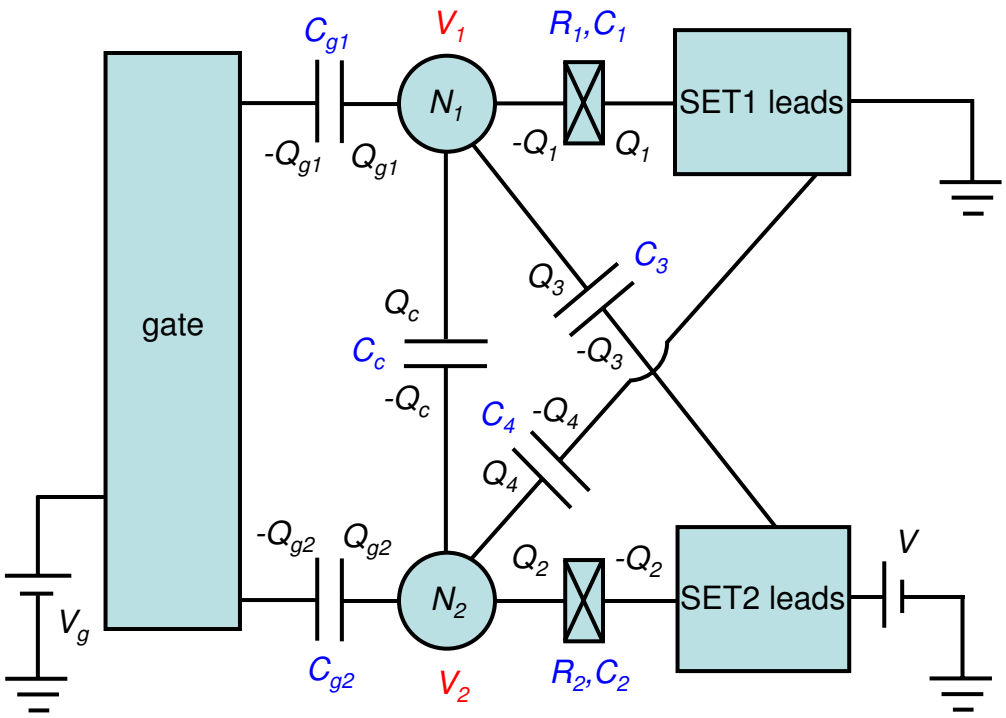


Figure 2.3: Schematic of two capacitively coupled SETs. The two circles represent the two SET islands, and for each SET, the two tunnel junctions are simplified to one, R_1, C_1 and R_2, C_2 respectively. N_1 and N_2 are the numbers of excess electrons on the two SET islands respectively. V is the relative bias between the two SETs, while V_1 and V_2 are the potentials of the two SET islands. C_{g1} and C_{g2} are gate capacitances to the two SET islands, and C_3 and C_4 are the cross capacitances between one SET leads and the other SET island. C_c is the coupling capacitance between the two SET islands. Q_i are the induced charges on the capacitor plates.

$$-N_2e = C_2(V_2 - V) + C_4V_2 - C_c(V_1 - V_2) + C_{g2}(V_2 - V_g)$$

where V_1 and V_2 are the potentials of SET1 island and SET2 island respectively. After rewriting the above two equations we have the following matrix form:

$$\begin{pmatrix} -N_1e + C_{g1}V_g + C_3V \\ -N_2e + C_{g2}V_g + C_2V \end{pmatrix} = \begin{pmatrix} C_{\Sigma1} & -C_c \\ -C_c & C_{\Sigma2} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{2.7}$$

Solving the above equation, we find the potentials on the two SET islands:

$$V_1 = \frac{-C_{\Sigma2}(-N_1e + C_{g1}V_g + C_3V)}{-C_{\Sigma1}C_{\Sigma2} + C_c^2} - \frac{C_c(-N_2e + C_{g2}V_g + C_cV)}{-C_{\Sigma1}C_{\Sigma2} + C_c^2} \tag{2.8}$$

$$V_2 = \frac{-C_c(-N_1e + C_{g1}V_g + C_3V)}{-C_{\Sigma1}C_{\Sigma2} + C_c^2} - \frac{C_{\Sigma1}(-N_2e + C_{g2}V_g + C_cV)}{-C_{\Sigma1}C_{\Sigma2} + C_c^2} \tag{2.9}$$

Once we extract V_1 and V_2, the total electrostatic energy stored on the capacitors can be calculated as:

$$\begin{aligned} U(N_1, N_2, V_g, V) &= \frac{1}{2}(C_1V_1^2 + C_{g1}(V_1 - V_g)^2 + C_3(V_1 - V)^2 + C_c(V_1 - V_2)^2 \\ &\quad + C_{g2}(V_2 - V_g)^2 + C_4V_2^2 + C_2(V_2 - V)^2) \end{aligned} \tag{2.10}$$

In most cases, the absolute value of the above total electrostatic energy is not as useful as the free energy change ΔG (see notation in reference [47]) when the charge configuration (N_1, N_2) change with no changes of the external voltage sources. Here I only consider one example (N_1, N_2)$\Rightarrow$(N_1, N_2+1). In this case:

$$\Delta G = U(N_1, N_2 + 1, V_g, V) - U(N_1, N_2, V_g, V) + W \tag{2.11}$$

where W is the work done by the voltage sources.[46]

To calculate the work W, the charge redistribution has to be found. For the charge configuration (N_1, N_2), the charge distribution is $Q_i = C_i\Delta V_i$, where ΔV_i's

are the voltage drops across the capacitors, which are known. After (N_1, N_2)⇒(N_1, N_2+1), the charge redistributes and:

$$\delta Q_i = Q_i(N_1, N_2 + 1) - Q_i(N_1, N_2) \tag{2.12}$$

For example, $Q_3 = C_3(V_1 - V)$ and $\delta Q_3 = (C_3 C_c/(-C_{\Sigma 1} C_{\Sigma 2} + C_c^2))e$. Then the work done by the voltage sources is:

$$W = eV + V_g(\delta Q_{g1} + \delta Q_{g2}) + V(\delta Q_2 + \delta Q_3) + 0 \cdot (-\delta Q_1 + \delta Q_4) \tag{2.13}$$

The first term eV comes from the tunneling of an electron to the SET2 island through tunnel junction C_2 which is the only path for charge transfer, and the last term is zero simply because the drain and source of SET1 are grounded.

2.3.2 Matrix form for electrostatic energy calculation

In this section I describe a simpler way to calculate the electrostatic energy using matrices. I will start from Eq. 2.7. This equation is nothing but a simple matrix equation $\mathbf{Q} = \mathbf{CV}$, where

$$\mathbf{V} = \begin{pmatrix} V_1 \\ \\ V_2 \end{pmatrix} \tag{2.14}$$

is the SET island potential matrix,

$$\mathbf{Q} = \begin{pmatrix} -N_1 e + C_{g1} V_g + C_3 V \\ \\ -N_2 e + C_{g2} V_g + C_2 V \end{pmatrix} \tag{2.15}$$

is the charge matrix including the actual number of excess electrons and induced charge by external voltage sources on the SET islands, and

$$\mathbf{C} = \begin{pmatrix} C_{\Sigma 1} & -C_c \\ -C_c & C_{\Sigma 2} \end{pmatrix} \tag{2.16}$$

Notice that the capacitance matrix is symmetric and has the total capacitance of each SET island as the diagonal elements and coupling capacitances as the off-diagonal elements. The SET island potential matrix can be solved as $\mathbf{V} = \mathbf{C}^{-1}\mathbf{Q}$. Then the electrostatic energy of the capacitor network can be expressed as:[48, 49]

$$E(N_1, N_2, V_g, V) = \frac{1}{2}\mathbf{V}^T\mathbf{C}\mathbf{V} = \frac{1}{2}(\mathbf{C}^{-1}\mathbf{Q})^T\mathbf{C}\mathbf{C}^{-1}\mathbf{Q} = \frac{1}{2}\mathbf{Q}^T\mathbf{C}^{-1}\mathbf{Q} \tag{2.17}$$

Equation 2.17 differs from Eq. 2.10 in that the latter contains more terms. However, it is the energy change between different charge configurations rather than the absolute value at certain charge configuration that determines the charge dynamics. If the total electrostatic energy is expressed as in Eq. 2.17, the free energy change for the same case $(N_1,\ N_2) \Rightarrow (N_1,\ N_2{+}1)$ is:

$$\Delta G = E(N_1, N_2 + 1, V_g, V) - E(N_1, N_2, V_g, V) + eV \tag{2.18}$$

where eV is the work done by the external voltage sources associated with the tunneled electron in this case. For a different charge distribution change, the work done by the external voltage sources has to be recalculated accordingly. For example, for the redistribution $(N_1,\ N_2) \Rightarrow (N_1 + 1,\ N_2)$, the extra work is $e \cdot 0 = 0$. Since the charge redistributions in Eq. 2.12 do not need to be known, the calculation is simplified dramatically.

The matrix form calculation for a capacitor network can be further generalized to multiple coupled quantum dots system ($n > 2$).[50] The generalized capacitance matrix is:

$$\mathbf{C} = \begin{pmatrix} C_{\Sigma 1} & -C_{12} & \cdots & -C_{1n} \\ -C_{21} & C_{\Sigma 2} & \cdots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n1} & \cdots & \cdots & C_{\Sigma n} \end{pmatrix} \tag{2.19}$$

where $C_{ii} = C_{\Sigma i}$ is the total capacitance of the i^{th} island and $C_{ij} = C_{ji}$ is the coupling capacitance between the i^{th} and j^{th} islands. The generalized charge matrix is:

$$\mathbf{Q} = \begin{pmatrix} -N_1 e + \Sigma C_{1\alpha} V_\alpha \\ -N_2 e + \Sigma C_{2\alpha} V_\alpha \\ \vdots \\ -N_n e + \Sigma C_{n\alpha} V_\alpha \end{pmatrix} \tag{2.20}$$

including the actual and virtual charge on the SET islands, where V_α are the external voltage sources. Then Eqs. 2.17 and 2.18 can be used to calculate the total electrostatic energy and free energy change. In Eq. 2.18 for the free energy change, only the work done by external sources associated with the tunneled electrons needs to be considered.

2.4 Phase diagram of capacitively coupled SETs

For measuring the electrical characteristics of the SETs, a bias voltage V_{ds} has to be applied to each SET. As long as V_{ds} is small enough compared to the charging

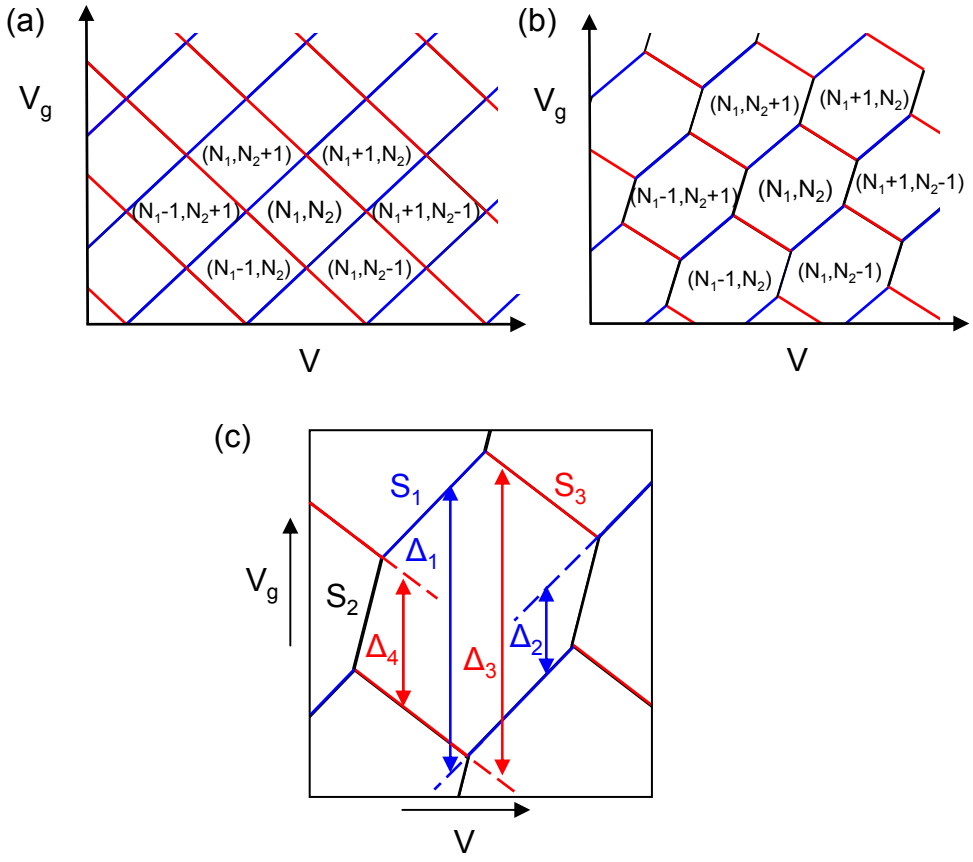


Figure 2.4: Schematic stability diagram of two capacitively coupled SETs for (a) no coupling $C_c = 0$. (b) $C_c \neq 0$. (N_1,N_2) in (a) and (b) is a stable charge configuration on the two SET islands. The red and blue lines represent the conductance peak traces of the two SETs respectively. (c) Detail of one hexagon. S_1, S_2, and S_3 are the slopes of the hexagon edges. Δ_1 and Δ_3 are the separations between the opposite parallel edges of the hexagon. Δ_2 and Δ_4 are the vertical shifts of the two SET conductance peaks.

energy, the drain and source leads of each SET can essentially be considered at the same potential. Then the coupled SET system can still be described by Fig. 2.3. This simplification will be used in Chaps. 6 and 7.

Figure 2.4(a) shows the expected phase diagram of the conductances of two SETs as a function of V and V_g with no coupling ($C_c = 0$). Each diamond has a stable charge configuration with two numbers in parenthesis representing the numbers of electrons on the two SET islands. The red lines are the conductance peak traces of SET1 and the blue lines are those of SET2. Both the red and blue lines are independent to each other. In this case of no coupling, the two SETs are electrostatically isolated from each other, so the conductance of each SET will trace out straight lines with a slope determined by the gate capacitance ratio, $dV_g/dV = -C_3/C_{g1}$ for SET1 and $dV_g/dV = (C_4 + C_{g2})/C_{g2}$ for SET2. The two SET conductance traces have slopes of opposite sign simply because V is the relative bias between the two SETs.

Now if the coupling between the two SETs is turned on, the electrostatic interaction will shift the conductance peaks (blue and red lines) whenever they meet each other, because each peak trace corresponds to a unit charge change in the number of electrons on the corresponding SET island. Further consideration [48] reveals that each vertex of the diamond in Fig. 2.4(a) will become a line (the black lines in Fig. 2.4(b)), resulting in hexagons in the voltage space, as depicted in Fig. 2.4(b). Along the black lines in Fig. 2.4(b), an excess electron on either SET island has the same electrostatic energy. Since this process only involves a transfer of electron between the two SET islands (NOT direct tunneling because there is no

tunneling path!) and does not involve a continuous transfer of electrons through either SET, no current through either SET is expected to be measured. Therefore, the black lines in Fig. 2.4(b) do not represent a conductance peak trace, but just a change in the stable charge state.

The regions denoted by (N_1,N_2) in Figs. 2.4(a) and 2.4(b) represent stable charge configurations in the two SET system. A conductance peak simply corresponds to a continuous transfer of electrons through an SET island, which means there is no energy cost for an electron to jump on and off the SET island. The energy degeneracy condition on the boundaries of the hexagons in Fig. 2.4(b) can be determined by setting $\Delta G = 0$, thus:

$$E(N_1, N_2, V_g, V) = E(N_1 + \delta N_1, N_2 + \delta N_2, V_g, V) + (\delta N_2)eV. \tag{2.21}$$

Here $\delta N_1 = 0, \pm 1$; $\delta N_2 = 0, \pm 1$; and $|\delta N_1 + \delta N_2| < 2$, and $(\delta N_2)eV$ is the extra work done by voltage source V when one electron tunnels through junction C_2.

Figure 2.4(c) shows some useful parameters in the hexagonal phase diagram. The slopes of the three sides of the hexagon are:

$$S_1 = \frac{C_{\Sigma 1}C_{\Sigma 2} - C_{\Sigma 1}C_2 - C_cC_3 - C_c^2}{C_{\Sigma 1}C_{g2} + C_cC_{g1}} \tag{2.22}$$

$$S_2 = \frac{C_{\Sigma 1}C_{\Sigma 2} + C_{\Sigma 2}C_3 + C_cC_2 - C_{\Sigma 1}C_2 - C_cC_3 - C_c^2}{C_{\Sigma 1}C_{g2} - C_{\Sigma 2}C_{g1} + C_{g1}C_c - C_{g2}C_c} \tag{2.23}$$

$$S_3 = -\frac{C_{\Sigma 2}C_3 + C_cC_2}{C_{\Sigma 2}C_{g1} + C_cC_{g2}} \tag{2.24}$$

The period of the blue and red lines in V direction are

$$\Delta_1 = \frac{eC_{\Sigma 1}}{C_{\Sigma 1}C_{g2} + C_cC_{g1}} \tag{2.25}$$

$$\Delta_3 = \frac{eC_{\Sigma 2}}{C_{\Sigma 2}C_{g1} + C_c C_{g2}} \tag{2.26}$$

respectively. The phase shift of each SET can also be calculated:

$$\Delta_2/\Delta_1 = \frac{C_c}{C_{\Sigma 1}} \tag{2.27}$$

$$\Delta_4/\Delta_3 = \frac{C_c}{C_{\Sigma 2}} \tag{2.28}$$

Therefore, the phase shift of each SET conductance is the coupling capacitance over the total capacitance of the other SET island.

In Chaps. 6 and 7, this electrostatic model of capacitively coupled SETs, Fig. 2.3, will be used to describe my vertically coupled Al and Si SET system. Equations 2.22 – 2.28 will play an essential role in extracting the capacitance parameters based on the measured slopes and phase shifts.

Chapter 3

Defects in Si/SiO_2 systems and detection of such defects

3.1 Importance of defects in the Si/SiO_2 system

Silicon field effect transistors (FET) are at the heart of semiconductor electronics because of numerous advantages of the Si/SiO_2 system. First, SiO_2, the thermal oxide of silicon, is more easily grown and thermally stabler than the oxide of any other semiconductor material. Second, SiO_2 has very low leakage, because SiO_2 has a huge energy bandgap (9 eV) and it provides both large energy barrier for electrons (about 3.25 eV) and holes (about 4.63 eV) in Si.[51] Finally, very low surface state density can be achieved by careful fabrication techniques, for example, by using hydrogen-passivation.

On the other hand, due to the amorphous nature of SiO_2, the Si/SiO_2 system has inevitable imperfections. Although the Si/SiO_2 system is the most important semiconductor-oxide system and has been extensively studied for decades, particularly at low temperature, the imperfections have not yet been fully understood.

For a Si-based solid-state quantum computer, background charge fluctuations can cause decoherence of the qubits and gate errors.[18, 19] For quantum computing, spins in solids may be better suited for use as qubits than charges, because they are better isolated from the environment and in turn can have longer coherence times. However, of some concern is that it takes more than just a long coherence time

to be useful as a qubit. Spins are magnetic and magnetic interactions are much weaker than Coulomb interactions. To get a two-spin operation done fast, which is required by quantum computing, one can use exchange coupling that is mediated by Coulomb interaction instead. However, in this case charge fluctuations in the environment will lead to gate errors and decoherence of spin qubits.

Also as nanoelectronic devices approach the few dopants regime, the functioning of these devices will be affected greatly by charging or discharging of individual defects. Therefore, understanding and potentially eliminating these imperfections is becoming more urgent than ever.

3.2 Imperfections in Si/SiO_2 systems

3.2.1 Intrinsic defects in Si/SiO_2 systems

There are four general types of charged defects associated with a Si/SiO_2 system, as depicted in Fig. 3.1.[52]

1. Interface trapped charge Q_{it} are either positive or negative charges located at the Si/SiO_2 interface, due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or bond-breaking processes. Their energies are within the silicon bandgap and they can exchange charge with the underlying silicon. Most interface trapped charge can be neutralized by low temperature (450°C) forming gas (H_2 + N_2) anneals.

2. Fixed oxide charge Q_f are positive charges located within about 2 nm from the Si/SiO_2 interface, due primarily to structural defects associated with the

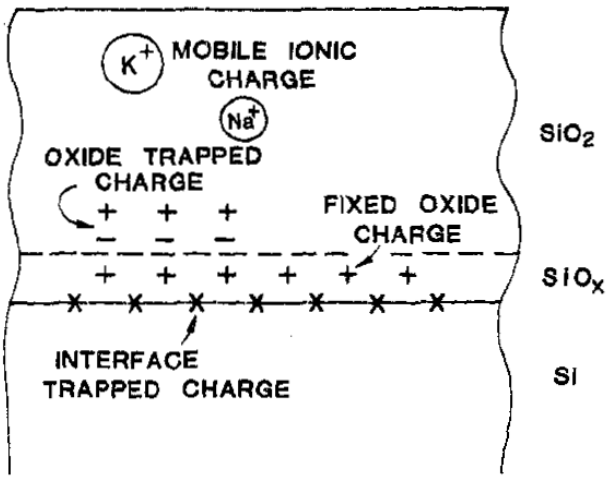


Figure 3.1: Terminology for defect charges in Si/SiO_2 systems and their locations. (Reprinted from Reference [52].)

oxidation process. They are immobile under an applied electric field and do not communicate electrically with the underlying silicon.

3. Oxide trapped charge Q_{ot} are trapped holes or electrons inside the oxide layer, which can be created by x-ray radiation or avalanche injection.

4. Mobile ionic charge Q_m are mainly ions of alkali metals and only mobile at high temperature, say room temperature or above.[53]

For Si-based quantum computing at low temperature (hundreds of millikelvin or below), however, most of these defects are irrelevant. Not only the fixed oxide charge but also oxide trapped charge and mobile ionic charge are expected to be frozen out. Even for interface states, only low energy states within a few k_BT around the Fermi level may pose a significant problem for quantum computing. Some paramagnetic states due to unpaired spins, however, can interfere with the spin qubits through direct magnetic interactions, even if they are isolated and deep

within the Si bandgap and incapable of exchanging charges. I will not address these paramagnetic states in this dissertation.

3.2.2 Interface states in Si/SiO_2 systems

Most interface states come from the lattice mismatch between crystalline silicon and amorphous silicon oxide. Reference [54] is a good review of Si/SiO_2 interface states. Detailed defect information obtained mainly by electron spin resonance (ESR) shows two types of Si dangling bonds – P_{b0} and P_{b1}.[55] Recently P_{b0} centers have been used to electrically probe ^{31}P donor electron spins analogous to the readout of the Kane quantum computer.[56]

These defects will contribute a density of states throughout the entire Si bandgap with a U-shape distribution, as shown in Fig. 3.2. It is generally believed that hydrogen atoms passivate the interface states by combining with the Si dangling bonds to form Si-H bonds. The density of interface states can be reduced to less than $10^{10}/cm^2 \cdot eV$ after careful hydrogen anneals. At a density of $10^{10}/cm^2 \cdot eV$, for a device area of 100 nm by 100 nm, there is only one state within the whole Si bandgap. Certainly for a small energy window of a few k_BT (say, order of 100 μV), the chance to have an interface state will be very small ($\sim 0.01\%$) if the density is uniform. Other data has found even lower defect densities. For example, Saks has shown a density as low as $5 \times 10^8/cm^2 \cdot eV$.[58] However, since all the density measurements are done at room temperature, the shallow states (say within a meV below the conduction band) are all thermally activated and are probably not measured.

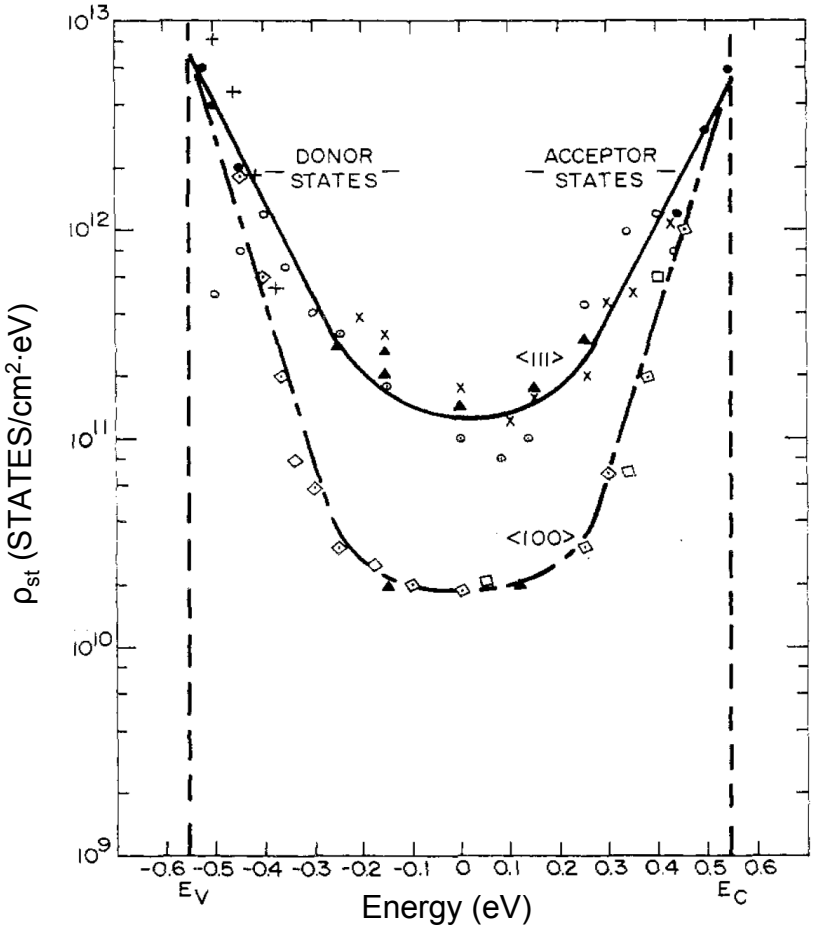


Figure 3.2: Density of interface states in silicon. E_V and E_C are the valence band maximum and conductance band minimum respectively. (Modified from Reference [57].)

So these shallow states may not be reflected in the measured low numbers. However, they will certainly be potential sources of decoherence for Si-based quantum computers at low temperature.

3.2.3 Donor states

Dopants in semiconductor have been intensively studied because of their control role in semiconductor devices. The density of residual dopants in a Si substrate can be very low, but one should expect they will inevitably contribute to charge noise. Phosphorus and arsenic in silicon are the two most studied donors. Each can be modeled as an artificial hydrogen atom as a first order approximation. The binding energies are $E_{D0} = 45.6$ meV and 53.8 meV for neutral P and As in bulk silicon (D^0 state), respectively.[59] The D^0 state can bind a second electron to form a D^- state with a binding energy of the second electron $E_{D-} \cong 2$ meV.[60] A schematic of the energy levels of D^0 and D^- states is shown in Fig. 3.3(a). The D^- state is of particular importance for the readout of Si-based quantum computing, because a D^0 state is able to bind a second electron only if the spin state of the coupled two-electron system is a singlet.[10]

Recently Sellier *et al.* detected both D^0 and D^- states through a transport measurement in a gated silicon nanowire as depicted in Figs. 3.3(c) and 3.3(d).[61] There was no direct tunneling between the source and drain if there were no intermediate available states between them because of the large width of the barrier. A dopant within the tunnel barrier can provide such intermediate states (both D^0

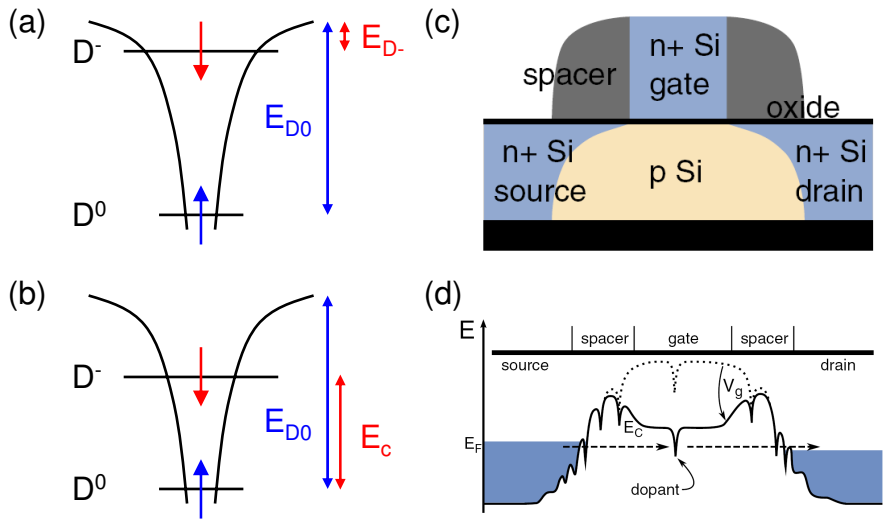


Figure 3.3: (a) Schematic of donor D^0 and D^- states in bulk Si (not to scale). (b) Due to electrostatic coupling between the charged D^- state with nearby electrodes, the charging energy of the 2^{nd} electron is reduced to E_c. (c) Schematic of a gated nanowire. (d) Schematic of conduction band profile corresponding to resonant tunneling through a single dopant in the channel. Figures (c) and (d) are reprinted from Reference [61].

and D^-) for electrons to tunnel through resulting in measurable conductance peaks. They identified the dopant to be an As donor based on the binding energy of the D^0 state. They argued that due to electrostatic coupling between the charged D^- state with the nearby electrodes, the charging energy of the second electron is reduced to $E_c = e^2/C_\Sigma$, the charging energy of a "quantum dot", as depicted in Fig. 3.3(b).

A similar experiment was done by Hofheinz *et al.* on a silicon nanowire with almost the same geometry as used by Sellier.[62] The only difference is that in Sellier's experiment they focused on the sub-threshold regime while Hofheinz *et al.* focused on the Coulomb blockade regime with a center island formed using a gate voltage. Anomalies associated with the Coulomb blockade diamonds were attributed to traps within the tunnel junctions. After ruling out interface traps as the sources simply because the interface trap density was thought to be too low, they inferred that most of the traps were As dopants, although they did not observe the D^- states.

3.3 Charge noise in single electron transistors

To study background charge motion directly, sensitive electrometers are necessary. Suitable detectors include SETs, FETs, and quantum point contacts (QPCs).

An SET is a typical readout device for research in spin-based solid state QCs.[7, 9, 10, 16, 22, 23, 24] They also have been used for metrology [21] and detection of nano-mechanical oscillators.[63] SETs are the most sensitive electrometers and can sense a tiny fraction of an electron charge in the vicinity of the SET island. The theory of SET operation has been discussed in Chap. 2, although not their

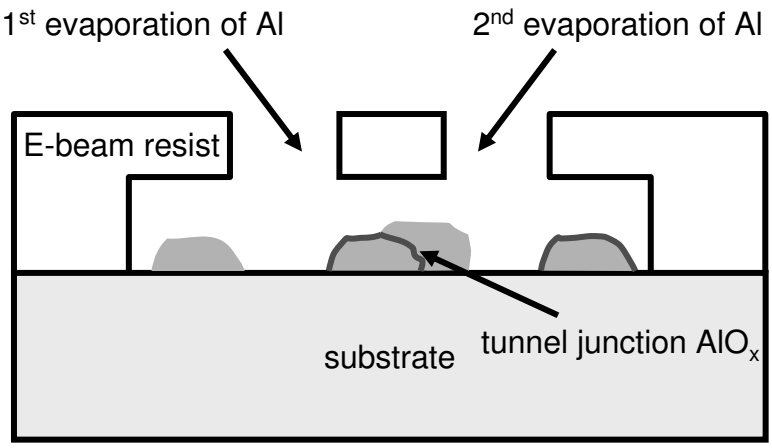


Figure 3.4: Schematic of an Al SET formed by double-angle evaporation. Al is first evaporated from one angle. Then the Al is oxidized in pure oxygen, followed by a subsequent evaporation at another angle. The regions where the two evaporations overlap form the tunnel junctions of the SET.

sensitivity. The most common SETs have Al metal islands fabricated using a shadow mask and self-aligned double-angle evaporation technique, as shown in Fig. 3.4.[64] In a double-angle evaporation, Al is first evaporated from one angle. Then the Al is oxidized in pure oxygen, followed by a second evaporation at another angle. The regions where the two evaporated films overlap create a tunnel junction.

The sensitivity of an SET at low frequencies is limited by random telegraph signals (RTS) and 1/f charge noise. 1/f noise is commonly present in many electronic devices.[65] There is a general belief that RTS come from a single dominant two-level fluctuator (TLF) in the environment associated with capture or emission of one electron or the motion of an ion while a 1/f noise spectrum comes from a large number of background charge fluctuations with a wide range of time constants.[66,

67] In contrast, a single TLF will make a Lorentzian contribution to the noise power spectrum.[68] Typically 1/f noise will limit the sensitivity of an SET at frequencies below 1 kHz.[69] A radio frequency SET (RFSET) [70] operating at 10 MHz – 100 MHz can operate above the 1/f noise knee and will be limited only by the intrinsic shot noise. A large RTS may cause more severe problems, *e.g.* it can completely drive an SET out of its operating point or mix up the expected signals.

There is no consensus yet for the exact location and source of the 1/f charge noise and RTS. They may be architecture or material dependent. Besides the four types of charges discussed in Sec. 3.2, the tunnel barriers of the SET, the substrate surface, and the SET island surface are possible locations for defect charges. Understanding the noise in an SET is important not only for realizing the SET's practical potential applications, but also for probing the background charges in the substrate, *e.g.* the Si/SiO_2 systems.

Verbrugh *et al*. studied the influence of SET island size on the operation of SETs and found that charge noise of the SETs increases with increasing island size.[71] Krupenin *et al*. cleverly designed their SETs such that the SET island sits almost entirely on the oxidized metal electrode and thus is effectively isolated from the substrate.[72, 73] They observed much lower 1/f noise level. Li *et al*. completely suspended the Al SET island from the substrate, and measured similar behavior.[74] All these experiments strongly suggest that the dominant noise source is from the substrate. This is also supported by other experiments. Zimmerman *et al*. studied the TLF noise in a particularly noisy Al SET. Based on the amplitude and duty cycle of the noise, and the non-periodic dependence on gate voltage of the switching

rates, they concluded that they were observing a cluster of TLFs somewhere on the surface of the substrate or the SET island.[75] One of their important findings is that even if the TLFs are not in the tunnel barriers, they can still cause significant fraction of 1 e (about 0.2 e) change on the SET island. In another experiment, Buehler *et al.* observed sub-microsecond RTS in a silicon MOS structure with an RFSET. Also by studying the switching of the TLF as the gate potential changed, they located the TLF either in the substrate or at the silicon oxide surface.[76]

Zimmerman *et al.* did a comprehensive study of the long-term charge offset drift in both Si and metal SETs fabricated by different groups but without addressing the location of the defects.[29] They found Si SETs are much more stable than metal SETs. Their explanation was that the TLFs in Si SETs are stable and non-interacting while those in metal SETs are unstable and interacting. A strategy they suggested to stabilize metal SETs is to avoid interaction between defects, *e.g.* to deposit stress-free metal films at elevated temperatures or on lattice-matched substrates.

3.4 Approaches to defect detection in Si/SiO_2 systems with SETs

3.4.1 Charge detection with a single SET or FET

In early work,[77] Brown *et al.* designed a wide lead Al SET incorporating a heavily doped backgate and a top gate, as depicted in Fig. 3.5. This allowed for independent control of the substrate and the Al SET island potentials. The wide lead of the Al SET can simplify the electrostatics of the device as three parallel

plates, as shown schematically in Fig. 3.5(b). Some fluctuators were identified and based on the response of the Al SET to the controlled charging of the Si/SiO_2 interface and from the large measured signal amplitude, it was concluded that the defects were located very near the SiO_2 surface. One possible source of charge noise was Al grains near the SET island due to the non-uniformity of the deposited Al film.

A similar conclusion was drawn in a recent experiment done by the Kafanov *et al.*[78] They observed two Lorentzians (two TLFs) superimposed on a 1/f spectrum in their Al SET. By studying the bias and gate voltage dependence of the noise, they suggested that the two TLFs were due to two small Al grains that were tunnel-coupled to one of the SET leads and capacitively coupled to the SET island.

Furlan and Lotkhov carefully designed an Al SET on oxidized Si substrate with four independent surface gates to study the background charge fluctuation.[79] This multiple gate geometry allowed them to identify the locations of TLFs by looking at the signal amplitude and the response of the fluctuator to individual gates. With the help of a numerical electrostatic simulation, they determined the TLF locations within a few nanometers from the SET island, in the oxide covering the island or in the substrate.

Recently in a remarkable experiment,[80, 81] Xiao *et al.* demonstrated an electrical detection of a paramagnetic trap near the Si/SiO_2 interface using an FET. The charging and discharging of a nearby trap can be detected by the electron channel at the Si/SiO_2 interface in terms of RTS whenever the Fermi level crosses the trap energy level. By studying the change in occupation between high and low

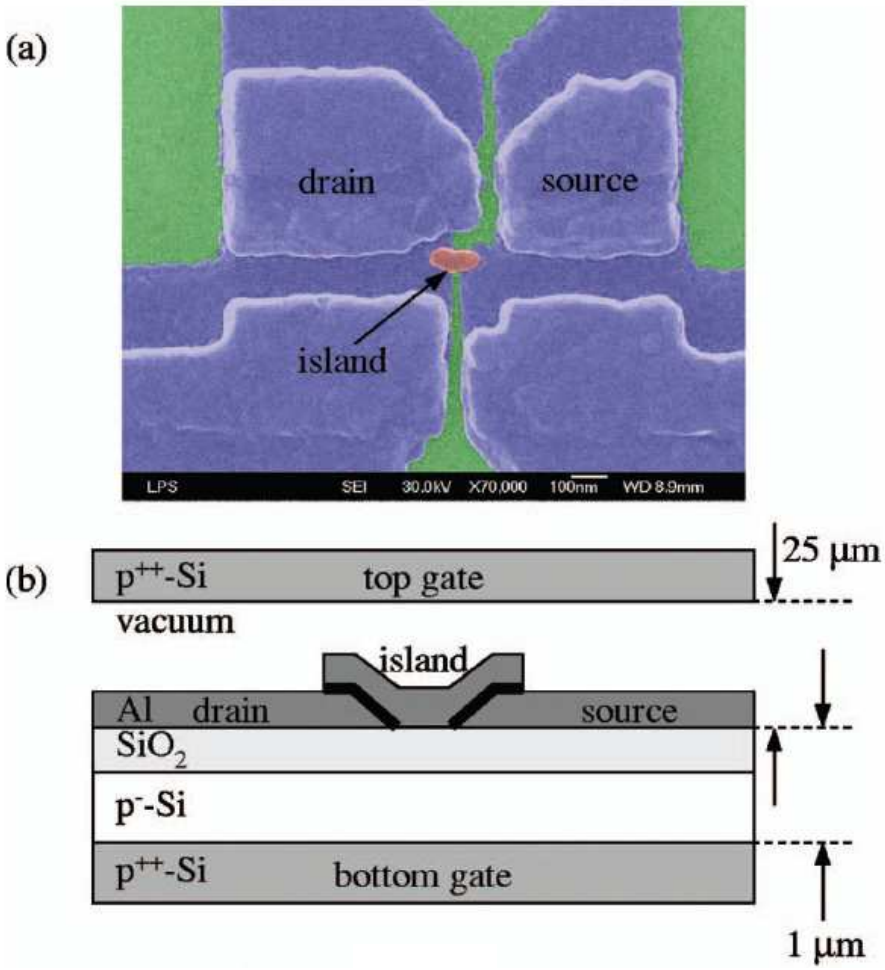


Figure 3.5: (a) SEM image of a wide lead SET. (b) Cross sectional schematic of the SET geometry. The heavily p-doped bottom gate is created through boron implantation. The top gate is suspended above the chip. (Reprinted from Reference [77].)

current levels as a function of gate voltage and magnetic field, they concluded they were observing a single paramagnetic center in the oxide that was about 0.2 nm away from the interface with a transition between $1e^-$ and $2e^-$ rather than $0e^-$ and $1e^-$. After carefully aligning the Fermi level with the trap level in a magnetic field, by studying the RTS caused by $1e^-$ to $2e^-$ transition at different fixed microwave frequencies, they successfully identified a peak in the $1e^-$ state occupancy change representing an electron spin resonance.

3.4.2 Charge detection with two coupled SETs

All the above described experiments were performed with a single SET. Two closely packed SETs, as depicted in Fig. 3.6, can have at least two advantages over the case with a single SET. First, defect charge motion in the substrate can be detected by two sensors, so twice the information about the sign and amplitude of the polarization can be obtained, and this may allow the defect location to be better pinned down. Second, the correlation between the two SETs outputs is sensitive to defect charge noise sources in the substrate and not sensitive to noise sources in the tunnel junction of one SET or on one SET island surface.

Zorin *et al*. first used two laterally coupled Al SETs with the two SET islands 100 nm apart to study the background charge noise of an Al_2O_3/Si substrate.[82] They measured the cross-spectrum power density of the two SETs, showed a correlation in the 1/f noises and got a correlation factor about 0.15. Based on a simple model for the two-SET system, they concluded that noise from the substrate dom-

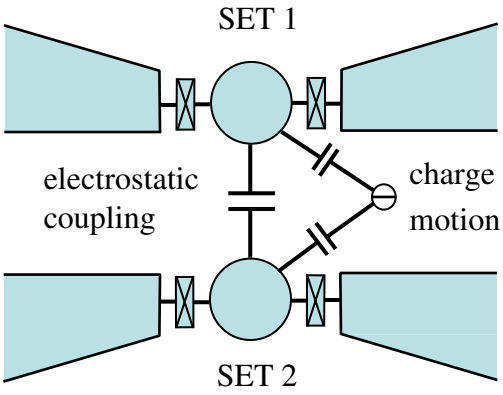


Figure 3.6: Schematic of correlated SETs for charge detections.

inates. Buehler *et al.* also used two RFSETs for correlated charge detection of a metal double dot, which mimics a charge dipole.[25] Although charge noise was present on each device, high readout fidelity was still achieved by correlating the signals from the two RFSETs, *e.g.* one SET detected the departure while the other one detected the arrival of one electron.

Another example of laterally coupled Coulomb blocked devices is two capacitively coupled quantum dots in a GaAs/AlGaAs heterostructure studied by Chan *et al.*[83] The two quantum dots are in a strongly coupled regime with the interdot capacitance about 16% (by correct calculation) of the total capacitance of each dot. Due to the fact that an additional electron in one dot can force the other dot completely on or off a Coulomb blockade peak, they argued that these strongly coupled quantum dots can be used as a switch.

A similar geometry of two laterally coupled quantum dots was realized by Hübel *et al.*[84] with even stronger interdot coupling; they obtained a coupling capacitance that was more than 1/3 of the total capacitance of each dot. Because

the two dots are only capacitively coupled with no inter-dot tunneling, at certain bias regions (degenerate points) the electrostatic interaction plays a dominant role such that it is energetically equivalent for an electron to be on either dot (see Sec. 2.4). This system will mimic a pseudospin realization of the Anderson impurity model, and possibly allow study of the Kondo effect. In this case – capacitively coupled double quantum dots, at the degenerate points a differential conductance peak is expected to be observed. Actually, the spinless Kondo effect was demonstrated by the same group a few years ago but on a vertically coupled quantum dot system.[85]

For most of the work described in this dissertation, I used a vertically coupled SET system to study background charge motion in the Si/SiO_2 system. One of the new things is that one SET is an Al SET while the other is a Si SET. There are several advantages to my approach:

First, in the above literatures for charge detection, the SETs are all on the device surface, so it is difficult to probe defect charges at the Si/SiO_2 interface and in the Si substrate. With a Si SET at the interface, the Si SET can detect charges at the Si/SiO_2 interface and in the Si substrate.

Second, this vertically coupled system can provide more information on the defect position in the vertical direction. Based on the signal amplitudes to both SETs, it is easy to tell if the defect charge is above or below the Si/SiO_2 interface.

Third, as in Xiao's experiment using an FET, the Si conducting channel at the interface can be a reservoir to supply electrons to tunnel on or off the defect center. Otherwise, it could be in a situation that the defect electron is ionized and the site has no chance to re-capture another electron.

Fourth, the SiO_2 layer between the Al and Si SET can be made very thin (a few nm) compared with lateral coupled SETs with a spacing at the order of 100 nm or more, so the coupling between the two SETs can be very strong and both SETs can probe the defect in the substrate even well below the Si/SiO_2 interface. Also new physics could be explored in this strong coupling regime.

As I will describe in the following chapters, I successfully detected a single charge defect that was coupled to both Al and Si SETs with a signal that was a significant fraction of 1 e. Based on the correlation of the two SETs, I was able to infer the defect to be tunnel-coupled to the Si SET and its location most likely was at the Si/SiO_2 interface, although I could not completely rule out the possibility that it was in the Si substrate.

Chapter 4

Device fabrication and wiring

4.1 Overview

In this chapter, I describe how I fabricated my devices and how I wired them up for the measurements in a dilution refrigerator.

Figure 4.1 shows schematic of the fabrication steps. The device fabrication started with the oxidation of a 3-inch, float-zone, p-type (boron), high purity Si (100) wafer ($\rho > 8,000\ \Omega$ cm, impurity density $< 10^{12}/\mathrm{cm}^3$) at 1000°C, yielding a SiO_2 thickness of about 20 nm. The wafer was selectively ion implanted with P at an energy of 50 keV and an areal density of 5×10^{14} /cm^2 to create n+ contacts. To limit the extent of the channel, p+ regions outside of the n+ contacts were created by another ion implantation of B at 18 keV with an areal density of 5×10^{14} /cm^2 [see Fig. 4.2(b)]. The peak densities of both dopants are high enough to allow conduction at 20 mK. Additionally, the doped regions reside close to the Si/SiO_2 interface. If the two implantations were interchanged, a p-channel device can be made instead, so that both polarities can be fabricated on a single chip. After both implantations, the wafer was annealed at 950°C for 60 seconds to activate the dopants and to repair implantation damage.

Electron-beam (e-beam) lithography and self-aligned double-angle evaporation were used to pattern resist for the leads and island of the Al SET,[64] as well as

an Al side gate, used to modulate the conductance of both the Al SET and the MOSFET channel [see Fig. 4.2(d)]. The final step in the fabrication process was to anneal the sample at 425°C in forming gas for 30 min to passivate dangling bonds at the Si/SiO_2 interface. Finally, the sample was wired up carefully and loaded in a dilution refrigerator for measurements. I will describe each step in detail in this chapter.

4.2 Oxidation

The oxidation was outsourced and was done at NIST, Gaithersburg, for the best quality. Their recipe was:

1. Standard RCA clean.
2. Oxide deposition at 1000°C, $\cong$ 13 min.
3. N_2 anneal at 1000°C, 20 min.

Five thickness measurements were taken on one of the wafers using a Nanospec. The average thickness was 215.8 Å and the uniformity was 1.67%, which is defined as 100×(max-min)/mean.

4.3 Ion implantation and activation

4.3.1 Boron implantation

After oxidation and before photolithography for the two separate ion implantations, alignment marks were etched in the Si substrate. The alignment marks were necessary for the two implantations and the subsequent e-beam lithography.

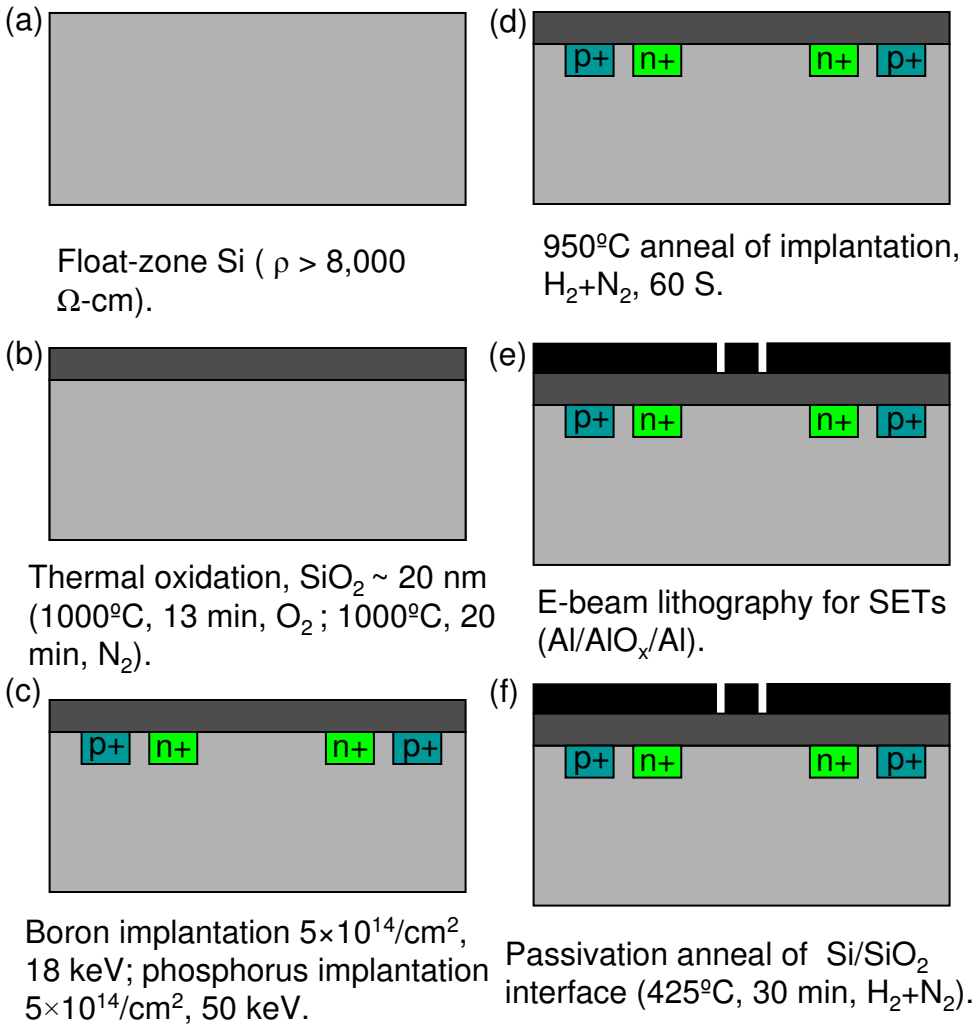


Figure 4.1: Schematic of device fabrication.

For boron implantation, I chose Al as the ion implantation mask to avoid the difficulty with removing photoresist which could get hardened after ion implantation. The first step was to evaporate Al on the wafer surface:

1. Al evaporation in CHA a e-beam gun evaporator, 300 nm at 0.5 nm/s, 1.8×10^{-6} Torr.

Followed by the alignment mark etch steps:

1. Spin HMDS adhesion promoter,[86] 3500 RPM, 60 sec.

2. Spin OiR 906-10 positive photoresist,[87] 3500 RPM, 60 sec.

3. Bake on hot plate, 90°C, 60 sec.

4. UV expose through a mask on a contact aligner, 12 mW, 5 sec.

5. Post bake on hot plate, 120°C, 60 sec.

6. Develop in OPD 4262,[88] 60 sec.

7. Rinse in deionized water (DI water), 1 min.

8. Al etch in 80-15-3-2 Al etchant,[89] 15 min. Patterns show up at about 7.5 min.

9. SiO_2 etch in reactive ion etcher (RIE), CHF_3+O_2 40 mTorr, 175 W, 2 min.

10. Silicon etch in RIE, SF_6 50 mTorr, 10 W, 6 min.

11. Surface cleaning in RIE, O_2 200 mTorr, 100 W, 10 sec.

12. Removal of photoresist in acetone, then in isopropanol (ultrasonic is optional).

At the end of this process, I measured the thickness of etched Al + SiO_2 + Si to be about 1.76 μm, which is thick enough to be seen under the optical microscope of the contact aligner and under the scanning electron microscope (SEM) in the

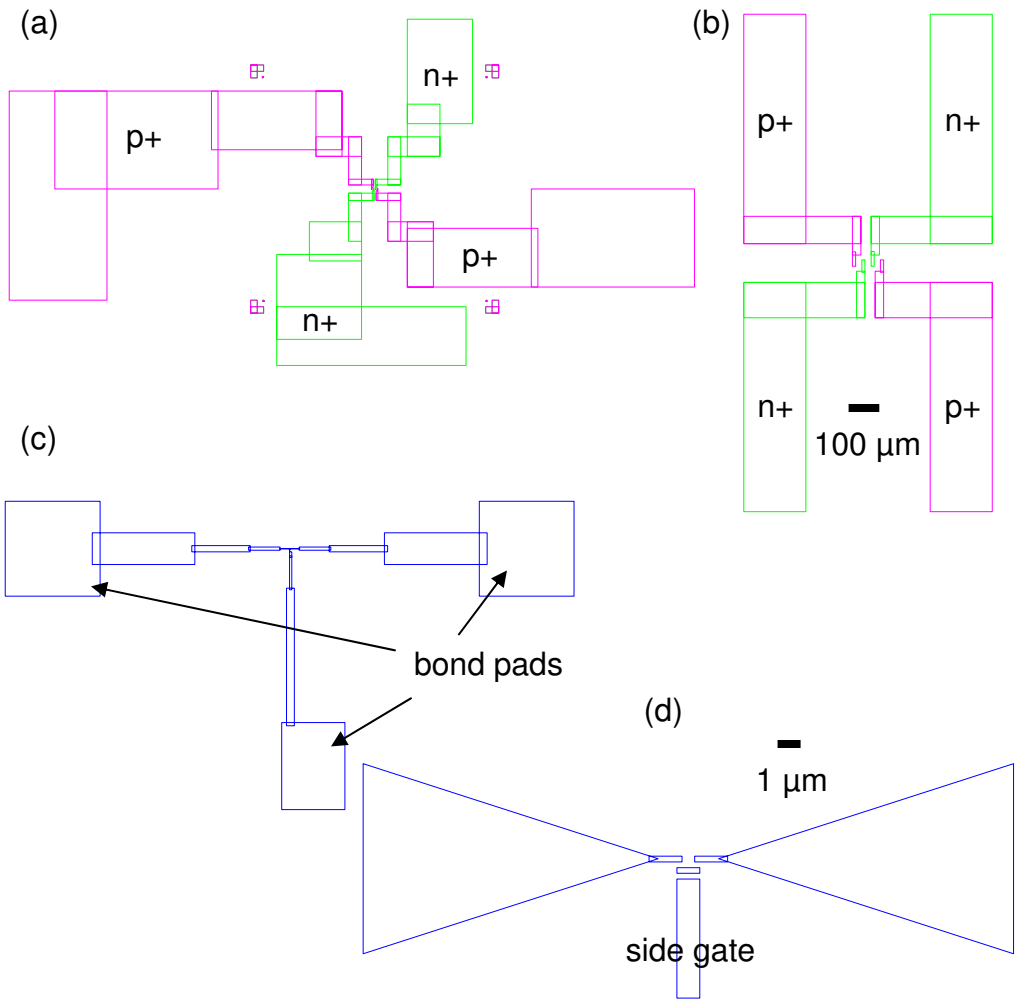


Figure 4.2: (a) and (b) The pink and green parts show the boron and phosphorus implantation patterns respectively. (b) Detailed view of the very center part of (a). (c) The e-beam lithography pattern. The entire pattern was written in three separate steps starting from the center fine structures to the large bond pads. (d) Detailed view of the very center part of (c).

subsequent lithography steps. The wafer was now ready to pattern for the first boron ion implantation to create the p+ contacts. The pink parts in Figs. 4.2(a) and 4.2(b) show the boron implantation patterns. The recipe was:

1. Spin HMDS adhesion promoter, 3500 RPM, 60 sec.

2. Spin OiR 906-10 positive photoresist, 3500 RPM, 60 sec.

3. Bake on hot plate, 90°C, 60 sec.

4. UV expose through a mask on a contact aligner, 12 mW, 5 sec. This step needs a pretty good alignment to the alignment marks, and should be within 1μm.

5. Post bake on hot plate, 120°C, 60 sec.

6. Develop in OPD 4262, 60 sec.

7. Rinse in DI water, 1 min.

8. Al etch, 15 min.

9. Removal of photoresist in acetone, then in isopropanol (ultrasonic is optional).

Then the wafer was sent to Core Systems [90] for a commercial boron implantation at 18 keV and an areal density 5×10^{14} /cm^2 with 7° tilt. The energy was chosen such that the boron density peak is in the Si substrate, but close to the Si/SiO_2 interface. A high dose was used to make sure that the boron peak density is well above the metal-insulator-transition value, even after a high temperature anneal (950°C, 1 min) to activate implanted ions, so it can conduct well at low temperatures. Figure 4.3 (a) shows a Monte Carlo simulation of the boron concentration as a function of depth beneath the surface run by the software SRIM (the Stopping and Range of Ions in Matter). At an areal density of 5×10^{14} /cm^2,

the peak density is about 6.5×10^{18} /cm^3, well above the metal-insulator-transition value.

4.3.2 Phosphorus implantation

After the wafer was back from boron implantation, the surface was cleaned for the second ion implantation as follows.

1. Al etch to remove the implantation mask, 20 min.

2. Cleaning with Acetone, methanol, and isopropanol in an ultrasonic bath, 5 min each.

This time I used OiR 908-35 [91] only as the implantation mask ($\cong$ 3.5 μm, much thicker than OiR 906-10, and thick enough to block the low energy ion implantation) and no Al was involved. The green parts in Figs. 4.2(a) and 4.2(b) show the phosphorus implantation patterns. The recipe was:

1. Spin HMDS adhesion promoter, 4000 RPM, 60 sec.

2. Spin OiR 908-35 positive photoresist, 4000 RPM, 60 sec.

3. Bake on hot plate, 90°C, 3 min.

4. UV expose through a mask on a contact aligner, 12 mW, 13 sec. This step also needs a pretty good alignment to the alignment marks (within 1μm).

5. Develop in OPD 4262, 60 sec.

6. Rinse in DI water, 1 min.

7. Hard bake on hot plate, 120°C, 3 min.

Note that OiR 908-35 can not be post baked right after UV exposure because

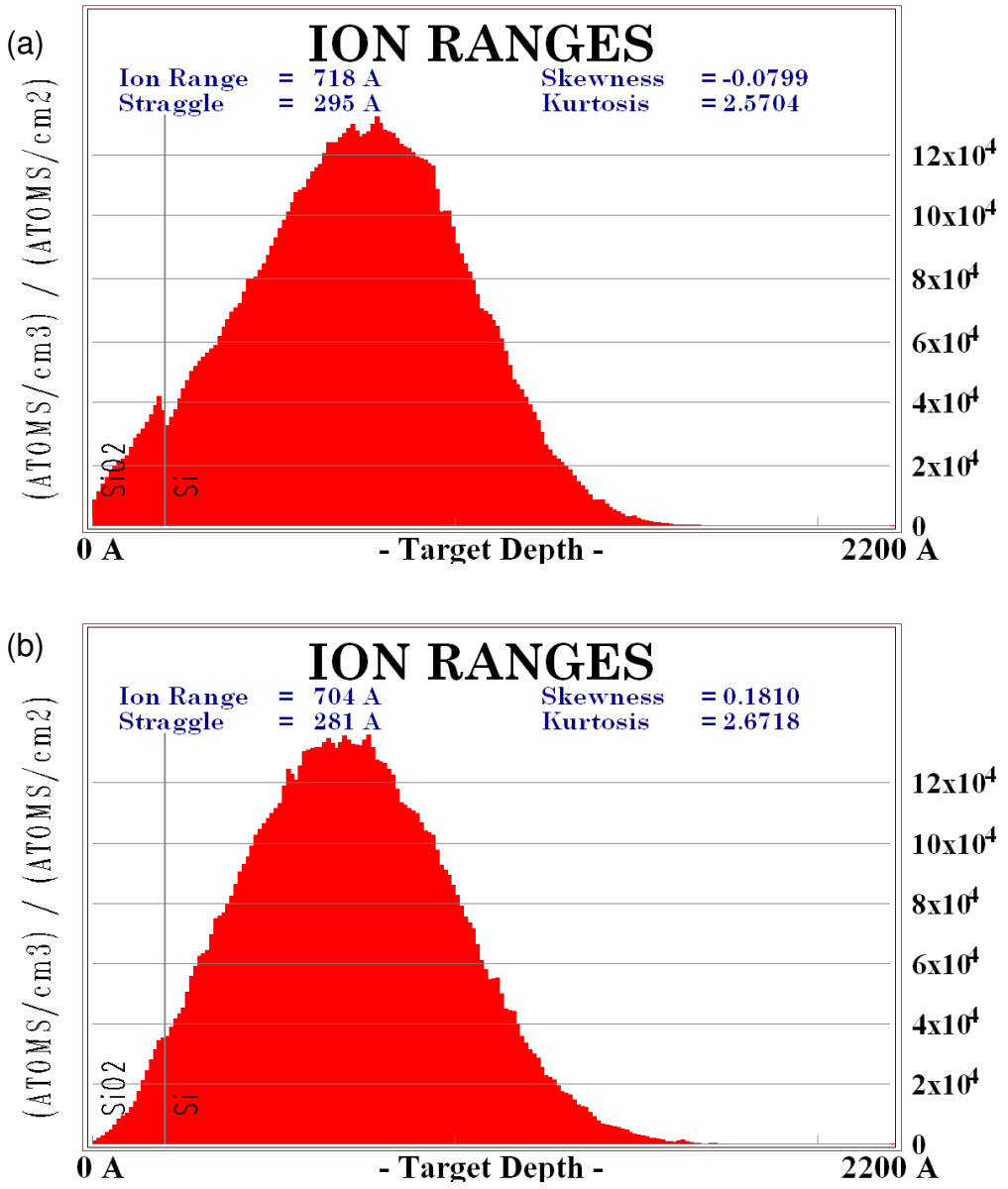


Figure 4.3: (a) Simulated boron concentration profile as a function of depth beneath the surface. (b) Simulated phosphorus concentration profile as a function of depth beneath the surface. At the an areal density of 5×10^{14} /cm^2, each peak density is about 6.5×10^{18} /cm^3, well above the metal-insulator-transition value.

of some unusual surface degradation. However, after development the resist can be baked harder, so it will not breakdown easily during implantation. The phosphorus ion implantation was also done by Core System but at 50 keV and an areal density 5×10^{14} /cm^2 with 7° tilt. The energy and density were chosen for the same reason as for boron implantation. Figure 4.3 (b) shows the calculated phosphorus concentration as a function of depth beneath the surface as found by a Monte Carlo simulation.

4.3.3 Activation of dopants

After phosphorus implantation, the wafer was dipped in an ultrasonic bath containing acetone, methanol, and isopropanol, each for 10 min. Most of the photoresist can be removed in this way, but not completely. There was always some residual resist at the implantation pattern edges. Before proceeding to the next step, a high temperature anneal (950°C) to activate the dopants, this residual resist must be removed, because the resist can not stand that high temperature.

I used the so called piranha clean to thoroughly remove all the residual photoresist. The recipe was:

1. 450 ml H_2SO_4 in quartz beakers heated on a hot plate to 100°C in a fume hood, 10 min.

2. Slowly add 150 ml H_2O_2 into H_2SO_4. The liquid should bubble nicely.

3. Immerse whole wafer with a Teflon holder into the solution, 15 min.

4. Take wafer out and immerse in DI water and then flush thoroughly with

DI.

5. Blow dry with N_2 gas.

After the piranha clean, all organic material should be removed from the wafer surface. The wafer was now ready to be activated with a rapid thermal anneal (RTA) at 950°C for 60 sec in $H_2 + N_2$. Note that after RTA, the implanted patterns should no longer be visible.

At this point, I diced the wafer into small rectangular chips with a size about 10 mm $\times$ 7 mm for an e-beam lithography of Al SETs. To protect the sample surface during dicing, I spun on thick photoresist again:

1. Spin HMDS adhesion promoter, 3000 RPM, 60 sec.

2. Spin OiR 908-35 positive photoresist, 3000 RPM, 60 sec.

3. Bake on hot plate, 90°C, 1 min.

After dicing, the small chips were stripped of resist one by one by dipping them in an ultrasonic bath of acetone, methanol, and isopropanol. The chips were then ready for e-beam lithography.

4.4 Fabrication of Al SETs

4.4.1 Why e-beam lithography only

E-beam lithography is normally too slow to write large leads and bond pads. The common way to overcome that is to use photolithography to define the large features and then to use e-beam lithography to write the small features such as the SETs. Since photoresist and e-beam resist are different, the metallization has to be

done separately for photo and e-beam lithographies. Noble metals like Au and Pt are commonly used for the first metallization after photolithography, because they do not get oxidized in air and can form good electrical contact with the subsequent metallization of Al after e-beam lithography. However this strategy is not suitable for our case, because neither Au/Al or Pt/Al can survive the subsequent high temperature process, a 425°C anneal in forming gas, which is required in our fabrication process to anneal the Si/SiO_2 interface and to eliminate damage introduced during the fabrication process, especially during e-beam lithography.

To overcome this problem, our group developed a novel process combining photolithography for the bond pads and e-beam lithography for the SETs into a single metallization step, thus eliminating the electrical contact between two different metals. In this process, a five layer resist stack was used: photo resist/Au/PMMA/Ge/PMGI. Au layer is used between the photo resist and e-beam resist to prevent intermixing. The basic idea is to transform both photo and e-beam lithography patterns to Ge layer as the shadow mask for the evaporation of Al. The fabrication recipe was discussed in detail in the Ph.D. dissertation [92] of Kenton Brown who was a former group member.

I found that this recipe did not work reliably for me. After putting all five layer materials, I found that not all would work well. I suspected that there was some contamination in our thermal evaporator which contaminated my sample when putting the Ge and Au later. In the end, I stopped using this recipe.

Eventually, I decided to use exclusively e-beam lithography for all the Al SETs, leads, and bond pads. To overcome the time issue, I did the lithography three

times with different currents: small current for Al SET to get the best spatial resolution, and big current for the large leads and bond pads which do not require good resolution. The whole writing time for one sample was about 20 min, which is not too bad, but I could only write one sample at a time.

4.4.2 E-beam lithography of Al SETs

I used a simple bilayer stack of e-beam resist for the e-beam lithography. I used PMGI SF8 resist [93] as the undercut layer because it can be easily developed in standard alkaline photoresist developers and the development can be done separately from the e-beam resist develop. I tried to avoid RIE dry etching in my recipe because of the worry of surface damage from the plasma. In my original recipe with RIE as the final step of undercut, after Al evaporation and lift-off, there was always some dark material along the Al pattern edges. I suspected that this material was associated with RIE.

I used the following recipe:

1. Spin PMGI SF8 resist, 5000 RPM, 60 sec, with a thickness about 400 nm.
2. Bake on hot plate, 180°C, 15 min.
3. Spin 950 PMMA A4,[94] 3000 RPM, 60 sec.
4. Bake on hot plate, 180°C, 5 min.
5. E-beam expose the pattern in SEM (see Table 4.1 for the parameters).
6. Develop PMMA in MIBK/IPA 1:3, 60 sec.
7. Rinse in IPA, 60 sec.

8. Blow dry with N_2 gas.

9. Undercut PMGI in OPD 4262, 20 sec.

10. Rinse in DI water, 60 sec.

11. Blow dry with N_2 gas.

The e-beam system I used is a JEOL 6500 SEM with Joe Nabity's NPGS system. Figure 4.2(c) shows the e-beam pattern which is written in three steps. Figure 4.2(d) shows the very center part of the Al SET with an island dimension about 80 nm $\times$ 180 nm. I always wrote this pattern during the first step with the smallest current for the maximum spatial resolution. During the e-beam lithography, I also did not place a short between the Al SET drain and source; it was not necessary to protect the SET against electrostatic discharge.

There were three sets of alignment marks already etched in the substrate (small, medium, and large), which were used to align the e-beam patterns for each writing. To overcome some deformation and offset of the SEM, I used a large overlap between steps. Table 4.1 gives the parameters of each e-beam lithography step.

4.4.3 Al evaporation and lift-off

After e-beam exposure, development of the PMMA, and undercut of PMGI, the chip was loaded into a thermal evaporation chamber. There is a load lock in the evaporator, so the pressure inside is maintained below 1.0×10^{-6} Torr for the least contamination. A standard double-angle evaporation technique [64] was used to fabricate the Al SET leads and island. I needed to be careful to align the chip

Table 4.1: Parameters of each e-beam lithography step. The electron beam was adjusted to have the best focus quality at 21 pA. When current was changed to write the medium leads, big leads, and bond pads, there was no further adjustment of the electron beam. To save writing time without worrying about the spatial resolution, much bigger center-to-center (CTC) and line-spacing (LS) values were used for the big features.

objects	current	magnification	CTC=LS	areal dose
Al SET island and leads	21 pA	×800	107.3 Å	450 (μC/cm^2)
medium leads	700 pA	×180	572.2 Å	450 (μC/cm^2)
big leads and bond pads	7 nA	×25	2059.9 Å	450 (μC/cm^2)

with the evaporator's rotation axis because in my e-beam pattern the island and leads are in a line. I also made sure that the Al SET island would come out in the second evaporation for a smaller dimension due to the slow pinch-off of features in the e-beam mask during the first evaporation. The evaporation steps were:

1. First evaporation of 35 nm of Al, +10°, 0.5 nm/s.
2. Oxidation in pure O_2, 100 mTorr–110 mTorr, 3 min.
3. Second evaporation of 80 nm of Al, -10°, 0.5 nm/s.

From this point on, I was very careful in handling the device because the SET is so fragile. The next step was the lift-off:

1. Immerse the chip in N-methyl pyrrolidone (NMP), 85°, 1 hour.
2. Rinse in DI water.
3. Spray acetone, methanol, and isopropanol.
4. Blow dry with N_2 gas.

Figures 4.4(a) and 4.4(b) show an optical image and an SEM image of one typical device, respectively. With the optical microscope, the implanted regions are completely invisible, but under an SEM they are easy to see.

4.4.4 Forming gas anneal

The next step was an anneal in forming gas (H_2 + N_2) at 425°C. This anneal will passivate the Si/SiO_2 interface and fix some damage created in the fabrication process. This process used to be very reliable, but I found that if the AlO_x layer thickness is too small (too low O_2 pressure or too short oxidation time), the forming

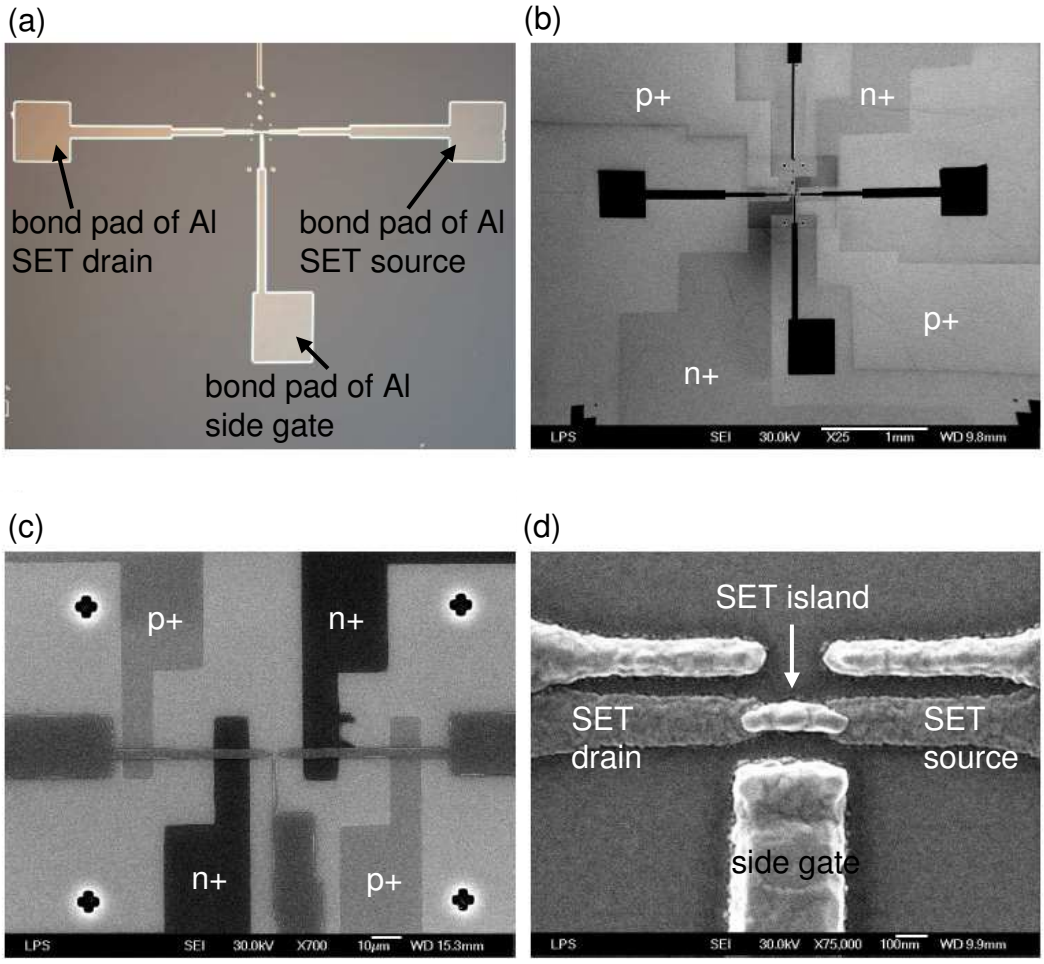


Figure 4.4: (a) Optical image of a typical device after lift-off. Note under an optical microscope the implanted regions are completely invisible. (b) An SEM image of a typical device. (c) and (d) are detailed views of (b). In (c), the implanted regions are easy to see.

gas anneal breaks down the AlO_x layer and the Al SET shorts out. On the other hand, if the AlO_x layer is thick enough to survive the anneal process, the Al SET resistance will increase by a factor of 3 – 8. This trend is consistent with the results in reference [95]. The forming gas anneal was done in a tube furnace as follows.

1. Place sample in furnace and ramp furnace to 150°C, in N_2, 20°C/min.
2. Stay at 150°C for 5 min to eliminate the moisture, in N_2.
3. Ramp furnace to 425°C, in N_2, 40°C/min.
4. Introduce forming gas at 425°C, 30 min.
5. Cool to room temperature, in N_2.

The above anneal process and the wiring up were time-consuming and a lot of care had to be taken, so before the anneal and before the final wiring, the Al SET was checked on a probe station. When using a probe station to make electric contact to Al SET bond pads, special care must be taken to prevent electrostatic damage. Initially the two probes needed to be shorted together through a breakout box; after the two probes touch down the Al SET, a switch was opened so the SET can be measured by a digital multimeter, which was in at least the MΩ range. For a working SET, the resistance has to be bigger than 25 kΩ. But before the forming gas anneal, the resistance can be lower than that, since it will increase dramatically after the anneal.

4.5 Wiring up

If I found out the SET was good after the forming gas anneal, the final step was to wire it up for measurements in a dilution fridge. This step was the most likely to break the SET, so extreme care needed to be taken. For example, during the wiring step, I grounded myself through a ground strip, the DIP socket to hold the DIP header had all its leads shorted together and grounded, and the solder iron tip and all the tweezers were grounded.

The first step in wiring was to put indium on the back of the sample chip and soldered the chip to a copper tape which was fixed on a 14-pin DIP header. The copper tape acted as a back gate and was then soldered to one pin of the DIP header.

I next wired up the implanted contacts. I used a scriber to scratch the top SiO_2 layer to expose the implanted contact pads (which are at the chip edges) to make the subsequent soldering easier. Then the exposed implanted contact pads were covered with indium and Au wires soldered to the DIP header.

In our old wiring process, we used a wedge bonder to bond the Al bond pads to the Au-plated DIP header pins directly using Al wires. The bonding was not that reliable. It was necessary to wire up many bond pads with sizes that were limited by the small chip size. However, for the devices I recently fabricated, there were only three bond pads–one side gate, one SET drain and one source. Soldering with indium proved to be much easier and more reliable. This final step will touch the Al SET drain and source, so everything including myself, solder iron, and tweezers

were grounded through thin metal wires.

After the sample was wired up, the DIP header with the sample was transported to another DIP socket which was soldered to a PCB board and the PCB board was then loaded on a copper holder which was connected to the mixing chamber of a dilution refrigerator. During transportation, all the DIP pins were kept grounded to protect the SET. Figure 4.5(a) shows two wired samples on a DIP header, and Fig. 4.5(b) shows the sample on the sample holder in the dilution refrigerator.

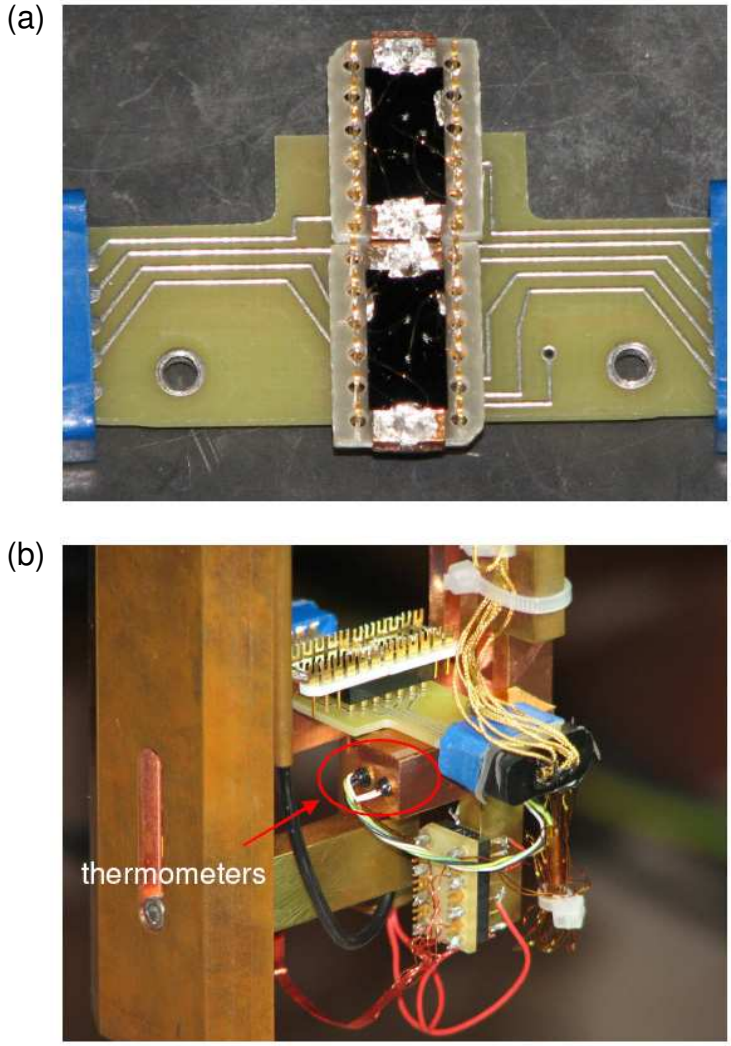


Figure 4.5: (a) Two samples wired up on a DIP header. (b) The two samples in a dilution refrigerator.

Chapter 5

Proof-of-concept experiments

5.1 Overview

In this chapter, a proof-of-concept experiment is described on an n-type (electron channel) test sample with a narrow aluminum wire instead of an Al SET as a top gate. There were two main motivations for doing this experiment. The first was to test whether the SiO_2 layer between the Al wire and the implanted regions could survive the low-energy high-density ion implantations without severe degradation. It must be able to handle a voltage higher than the channel threshold without breakdown. The second purpose was to test whether the two p+ regions could successfully confine the electron channel between them (Fig. 5.1) as I expected. Without this confinement, the electron channel would spread under the entire Al wire with two undesired consequences. First, the electrons can leak out at the bond pads, under which the oxide has a high chance of being broken during the wiring. Second, the capacitance between the channel and the Al wire is increased dramatically, which lowers the measurement bandwidth significantly.

This experiment was performed in a dipstick at 4 K. Both the Al top gate and side gate were wired up with coaxial wires, while all the other implanted contacts were wired up with twisted pairs. None of the wires were filtered. In this experiment, the conduction of the implanted regions, the channel threshold, and the electron

mobility were also studied. This can also help me to determine the working regime for a real SET device.

5.2 Leakage issues

The test sample (n-type) was fabricated as described in Chap. 4, except for the metallization step: a narrow Al strip was thermally deposited through a photoresist shadow mask instead of double-angle evaporations for an Al SET. Figure 5.1 shows a schematic of the proof-of-concept sample and the measurement circuit. Three source meters were used to apply bias voltages through a low-pass RC filter with a bandwidth of about 160 Hz. The narrowest part of the test sample had an aspect ratio of about 20/3 (length/width).

To have the highest possible quality of Si/SiO_2 interface, the low-energy ion implantations (both p+ and n+) were performed through the thermally grown SiO_2 layer. No removal and regrowth of the SiO_2 layer were done after the implantation to minimize the diffusion of the dopants and the potential re-deposition at the silicon surface of chemicals during the SiO_2 removal and of dopants during the regrowth process.

The first thing that I had to check was whether the gate oxide layer was leaky after implantation, because the ion implantation could cause pinholes in SiO_2. It turned out the gate oxide was very robust against the low-energy high-density ion implantations. I found only two samples that were leaky at the overlapped region between either n+ or p+ contacts and the Al top gate, and for all the other samples

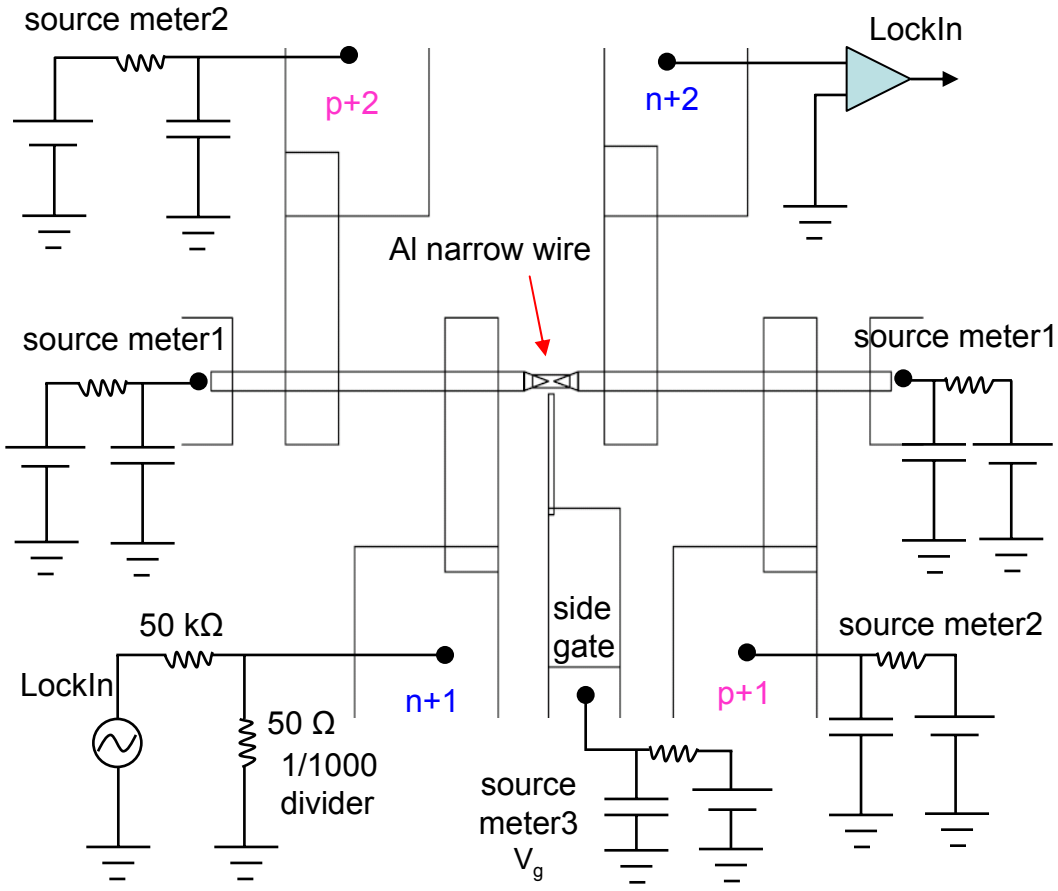


Figure 5.1: Schematic of proof-of-concept sample and the measurement circuit. Back gate is not shown. Source meters were used to apply bias voltages through a low-pass RC filter with a bandwidth about 160 Hz. For the channel conductance measurement, a lock-in amplifier (Stanford Research SR830) directly measured the channel current for better impedance matching.

(>10), there was no measurable leakage current (I<2 pA) from the Al top gate to all the other electrodes (Al side gate, n+, and p+ contacts). Figure 5.2 shows no gate oxide leakage up to $V_g = 8.0$ V with all other electrodes grounded. For $V_g < 0$, I only tried $V_g = -2.50$ V for three reasons: first, this was an n-channel electrons, for a real device, V_g should never go negative relative to the n+ contacts; second, in the negative direction, it was expected be to similar as in the positive direction; third, even for a p-type device, $V_g = -2.50$ V was enough to turn on the hole channel (data will be shown later).

All n+ and p+ contacts conducted well at 4 K, with a lead resistance estimated about $1 - 2$ kΩ. Figure 5.3 shows the diode behavior between the p+ and n+ contacts: no current was flowing when the p+ contacts were negatively biased relative to the n+ contacts; a leakage current started to flow only when $V_{p+} - V_{n+}$ was bigger than about 1.0 V. This diode behavior was expected and confirmed that the p+ contacts outside of the n+ contacts indeed can effectively confine the electron channel between them. In addition, as expected, both p+ contacts as well as both n+ contacts, behaved almost identically to each other; the characteristics were pretty symmetric when biased with n+ contacts relative to p+ contacts or with p+ contacts relative to n+ contacts [compare Fig 5.3(a) with Fig 5.3(b)].

Figure 5.4 shows the leakage current of the back gate with all the other electrodes grounded. Up to 11 V, there was no measurable leakage of the back gate, but it started to leak at $V_{bg} = -1.12$ V. The leakage source turned out to be the two p+ contacts, which was not too surprising because the substrate was p type. No leakage current was measured for the side gate within ± 10 V as expected, because

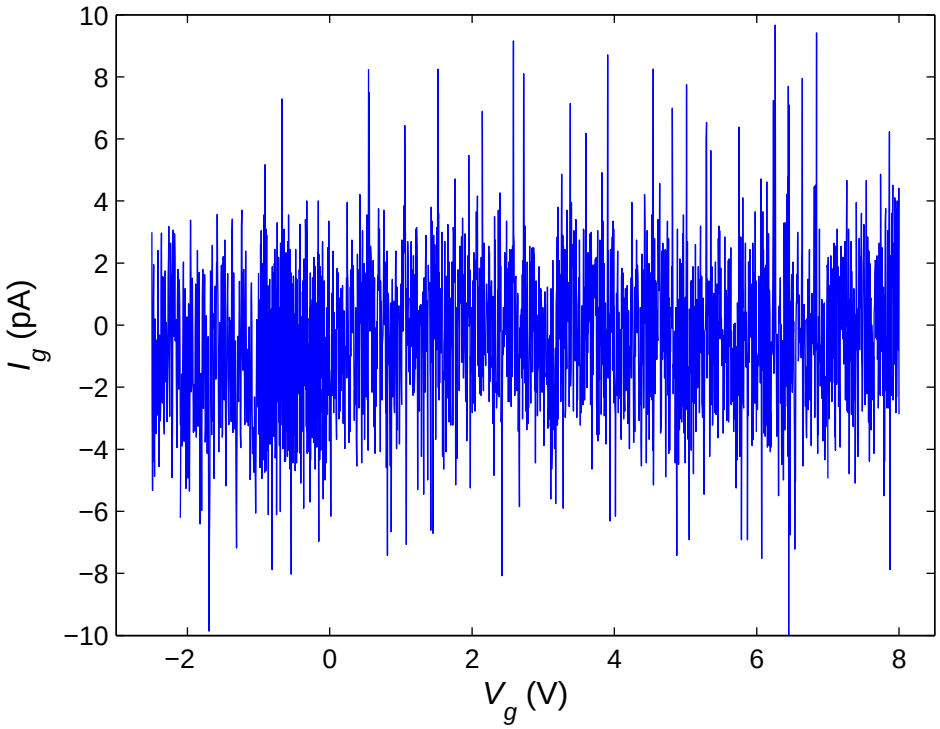


Figure 5.2: No gate oxide leakage (less than about 2 pA) up to $V_g = 8.0$ V with all other electrodes grounded. For V_g negative, the gate oxide was expected to show a similar negligible level of leakage.

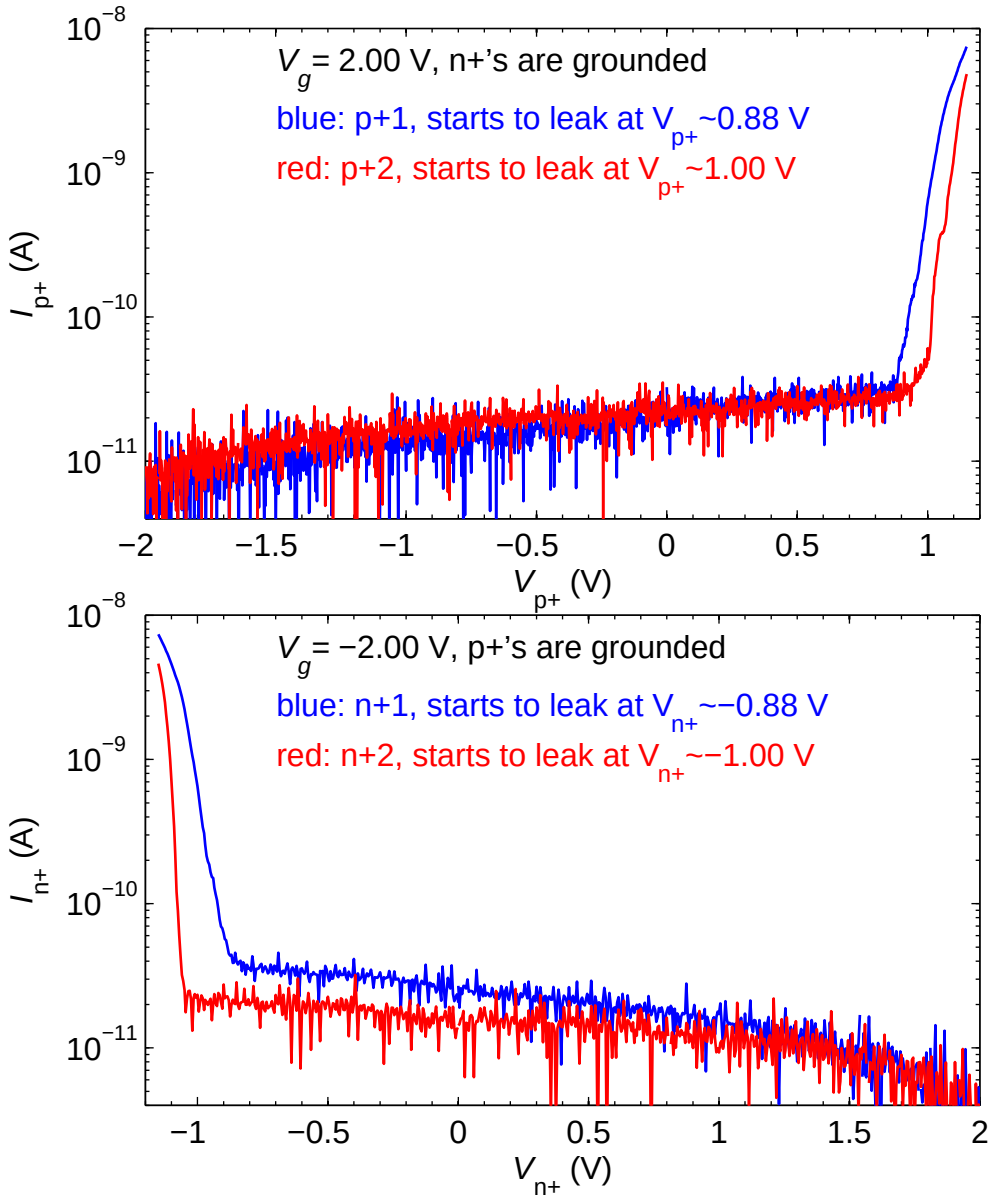


Figure 5.3: Diode behavior between the p+ and n+ contacts. As expected, both p+ contacts as well as both n+ contacts, behaved almost identically to each other; the characteristics were pretty symmetric when biased with n+ contacts relative to p+ contacts or with p+ contacts relative to n+ contacts. There was a leakage current between them only when $V_{p+} - V_{n+} > 1.0$ V. This diode behavior was expected and proved that the p+ contacts outside of the n+ contacts can confine the electron channel between them.

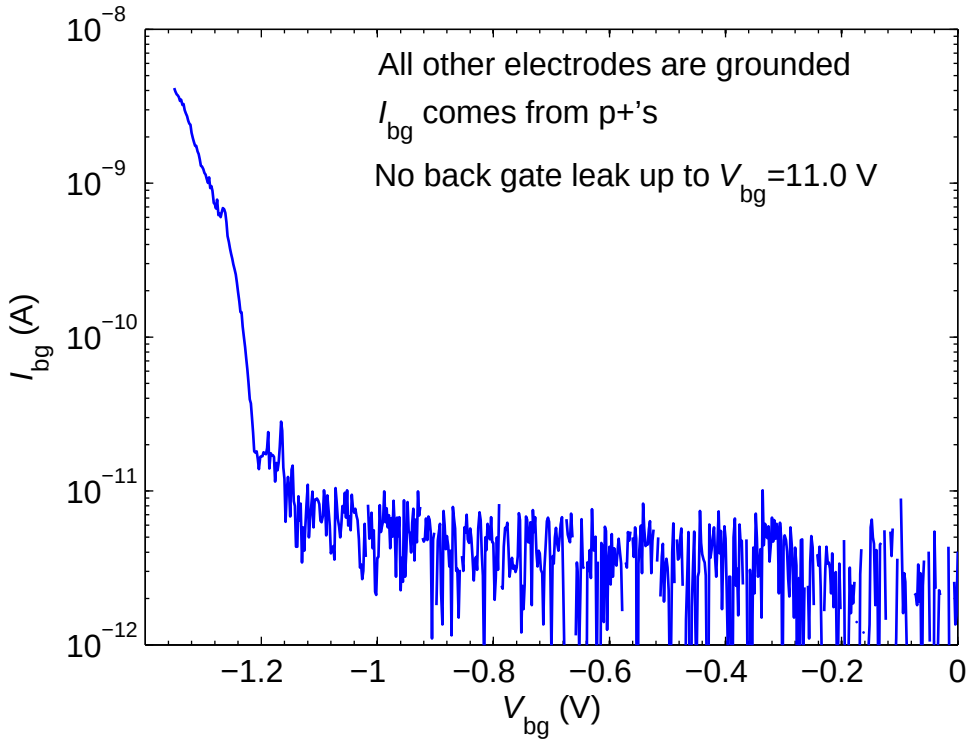


Figure 5.4: Leakage current of the back gate with all other electrodes grounded. Up to 11 V, there was no measurable leakage of the back gate, but significant leakage started to occur at $V_{bg} = -1.12$ V. The leakage source turned out to be due to the two p+ contacts making contact through the p-type substrate.

there was not touch of the silicon dioxide layer beneath the side gate.

5.3 Turn-on and electron mobility of the channel

To get the threshold of the electron channel and the electron mobility, I applied a small AC excitation (V_{ac} = 1 mV at f = 6.3 Hz) between the two n+ contacts with both p+ contacts grounded. The channel current was directly measured by a lock-in amplifier (Stanford Research SR830) in current mode for a better sensitivity. Figure 5.5 shows the Si channel conductance $G_{\rm ch}$ and $dG_{\rm ch}/dV_g$ as a function of V_g. The turn-on voltage is about $V_{\rm th}$ = 0.80 V. However, $V_{\rm th}$ varied between different thermal cycles, but it remained the same as long as the sample was kept cold.

The electron mobility μ can be extracted as follows. The conductivity of the electron channel is

$$\sigma = n \cdot e \cdot \mu \tag{5.1}$$

where n is the electron density, e is the electron charge. If n is the two-dimensional electron density, σ will be the sheet conductivity, which can be calculated from the channel conductance $G_{\rm ch}$:

$$\sigma = 1/\rho_{\Box} = \frac{L}{W} G_{\rm ch} \tag{5.2}$$

where L/W is the geometry factor. Using a parallel plate capacitor model, the two-dimensional electron density can be easily calculated as:

$$n \cdot e = \epsilon_0 \epsilon (V_g - V_{\rm th})/d \tag{5.3}$$

where d is the thickness of the SiO_2 layer with a permittivity ϵ = 4.0. Combining Eqs. 5.1, 5.2, and 5.3, we can write the channel conductance $G_{\rm ch}$ as a function of V_g

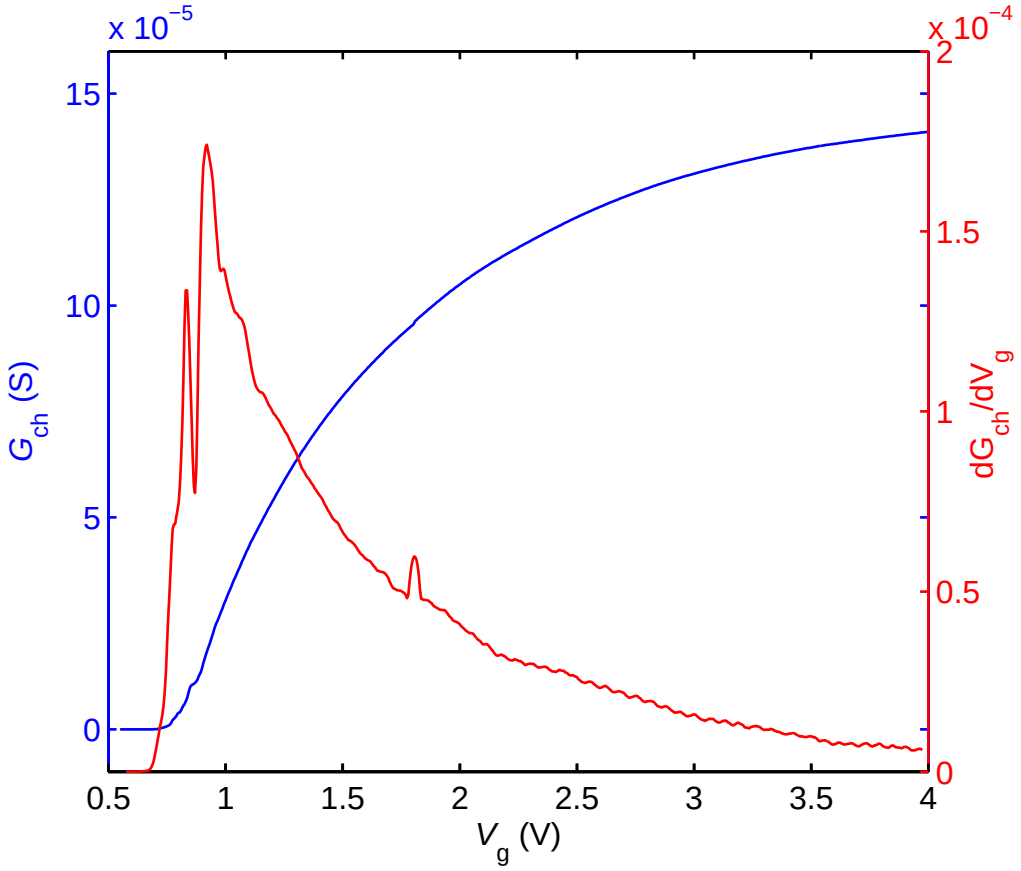


Figure 5.5: The Si electron channel conductance $G_{\rm ch}$ and $dG_{\rm ch}/dV_g$ as a function of V_g. The turn-on voltage was about $V_{\rm th} = 0.80$ V. $G_{\rm ch}$ started to saturate when $V_g > 3.0$ V, where the lead resistance started to dominate. $dG_{\rm ch}/dV_g$ was used to extract the electron mobility according to Eq. 5.5.

and μ:

$$G_{\rm ch} = \frac{W}{L}\frac{\epsilon_0\epsilon}{d}\mu\cdot(V_g - V_{\rm th}) \tag{5.4}$$

Since I was doing a two-probe measurement, the n+ and p+ lead resistance will play a big role when the channel was heavily conducting. This can be seen from the trend of $G_{\rm ch}$ saturation when $V_g > 3.0$ V, where the lead resistances started to dominate. Instead of calculating μ directly based on the value of $G_{\rm ch}$, to have a more accurate value of the electron mobility, the mobility can be extracted from $dG_{\rm ch}/dV_g$. From Eq. 5.4, we can show that:

$$\mu = \frac{L}{W}\frac{d}{\epsilon_0\epsilon}\frac{dG_{\rm ch}}{dV_g} \tag{5.5}$$

The red curve in Fig. 5.5 shows $dG_{\rm ch}/dV_g$ vs V_g. The peak value $dG_{\rm ch}/dV_g = 1.7\times10^{-4}$ gives a peak mobility $\mu = 6.4\times10^3$ cm^2/V·S based on a geometry factor L/W=20/3.

In this electron-channel sample, there was no measurable channel conductance to reveal the turn-on of the holes because the two p+ contacts can not talk to each other due to the two n+ contacts between them. Instead, by measuring the capacitance between each p+ contact and the Al top gate, I can tell the population of holes at the Si/SiO_2 interface. Figure 5.6 shows such a capacitance measurement of each p+ contact. I found that the two p+ contacts had about the same turn-on voltage $V_{\rm th} \cong -1.12$ V.

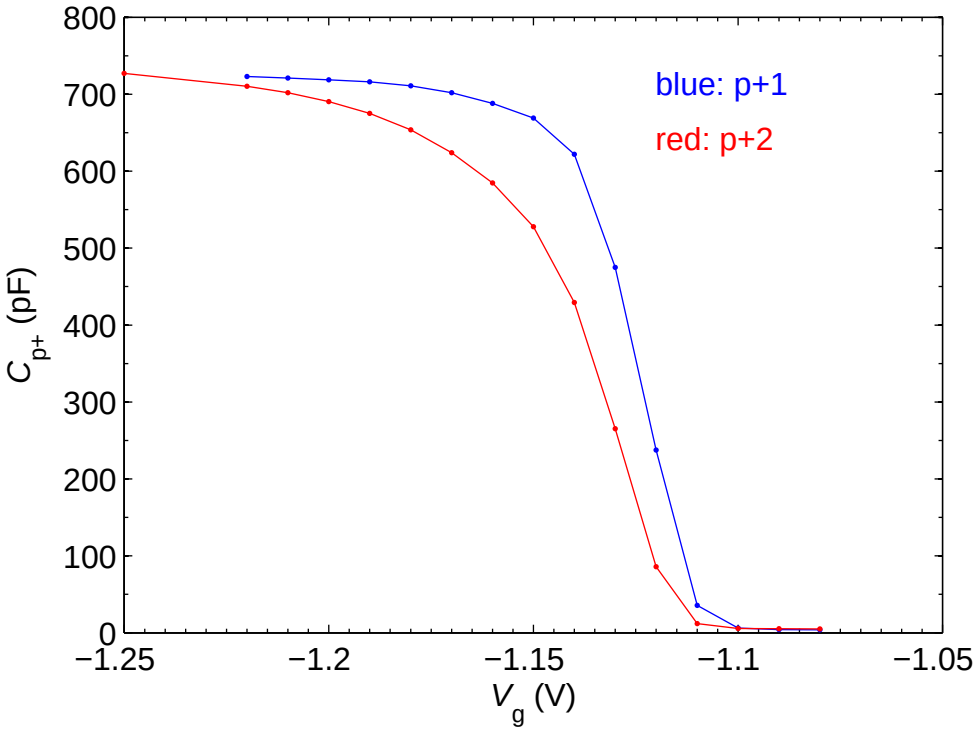


Figure 5.6: Turn-on of the 'hole channel' measured by a capacitance bridge. No measurable hole channel conductance was seen because of the two n+ contacts, which indeed can effectively block the hole channel. The two p+ contacts had about the same turn-on voltage $V_{\rm th} \cong -1.12$ V.

5.4 Conclusions

In conclusion, I have characterized an n-type proof-of-concept sample at 4 K. I found that all the implanted contacts conducted well at low temperature, and the gate oxide was robust against the low-energy high-density ion implantations. The expected diode behavior between the p+ and n+ contacts and the absence of measurable hole channel conductance, even with a population of holes at the Si/SiO_2 interface, confirmed the idea that the n+ region will effectively block the hole channel, and vice versa. The electron channel threshold voltage was measured to be about $V_{\text{th}} = 0.80$ V and based on the derivative of dG_{ch}/dV_g, a peak electron mobility $\mu = 6.4 \times 10^3$ cm^2/V·S, which is a decent mobility, was extracted.

Chapter 6

Vertically coupled Al and Si SETs

6.1 Overview

In this chapter, I describe experiments on a narrow ($\sim$ 100 nm) n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) incorporating an Al-AlO_x-Al single-electron transistor as the top gate. A p-channel MOSFET was fabricated as well, but it did not behave as regularly as the n-type one, probably because of the much lower mobility of holes. All of the measurements were done in a dilution refrigerator at a temperature of about 20 mK. A 1 T magnetic field was applied to keep the Al SET in the normal state.

Near the MOSFET channel conductance threshold I observe oscillations in the conductance associated with Coulomb blockade in the channel, revealing the unintentional formation of tunnel barriers in the channel and the creation of a Si SET. Abrupt steps present in sweeps of the Al transistor conductance versus gate voltage are correlated with single-electron charging events in the Si transistor, and vice versa. Analysis of these correlations using a simple electrostatic model demonstrates that the two single-electron transistor islands are closely aligned, with an inter-island capacitance approximately equal to 1/3 of the total capacitance of the Si transistor island, indicating that the Si transistor is strongly coupled to the Al transistor. I also discuss briefly the high carrier density regime: when the side

gate nearly pinches off the conducting channel, a similar vertically aligned Al and Si SET system is observed as well.

6.2 Characterization of the Al SETs, schematic and noise spectrum of the measurement setup

Two devices were fabricated as described in Chap. 4. Figure 6.1 shows the SEM images of the two devices, Device1 and Device2. The devices survived multiple thermal cycles to room temperature and displayed only small background charge offset variations between cycles. For simplicity, I will present data from a single cooldown.

6.2.1 Diamond chart of Al SETs

Figures 6.2(a) and 6.2(b) show the diamond charts of Al SET1 and Al SET2, respectively, measured under a DC bias with the silicon channel in the off state. For Al SET1, the diamond edges do not look as clean as those of Al SET2 because of much more random background charge motion in the vicinity of Al SET1 island. The charging energy, gate capacitance, and the two junction capacitances of Al SET1 can be extracted based on Eqs. 2.4, 2.5, and 2.6 in Sec. 2.1. I find the following: $E_c = 275\ \mu$V, $C_g = 8.51$ aF, $C_{11} = 102.2$ aF, and $C_{12} = 180.2$ aF. The extracted parameters for Al SET2 are: $E_c = 268\ \mu$V, $C_g = 7.64$ aF, $C_{11} = 125.1$ aF, and $C_{12} = 162.3$ aF.

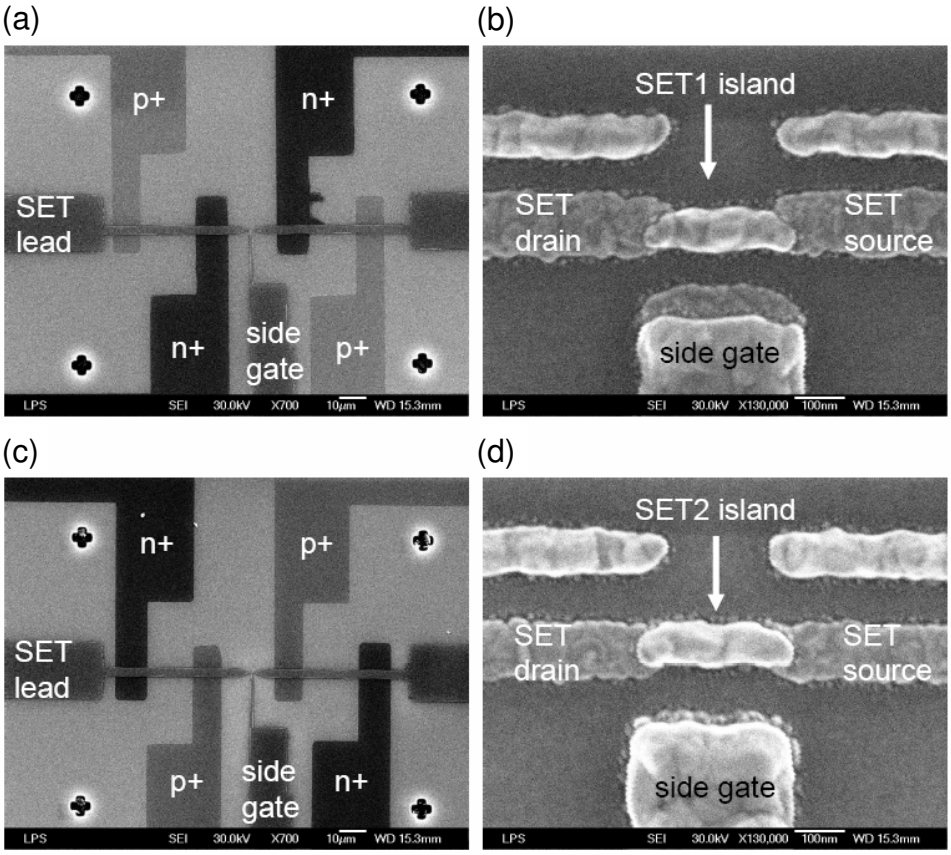


Figure 6.1: (a) and (b) SEM images of Device1, (c) and (d) SEM images of Device2. In (a) and (c), the darkest regions are n+ contacts, the gray regions are p+ contacts, and the four crosses at the four corners are the alignment marks for photo and e-beam lithographies. Note in (a) and (c) the n+ and p+ contacts are switched.

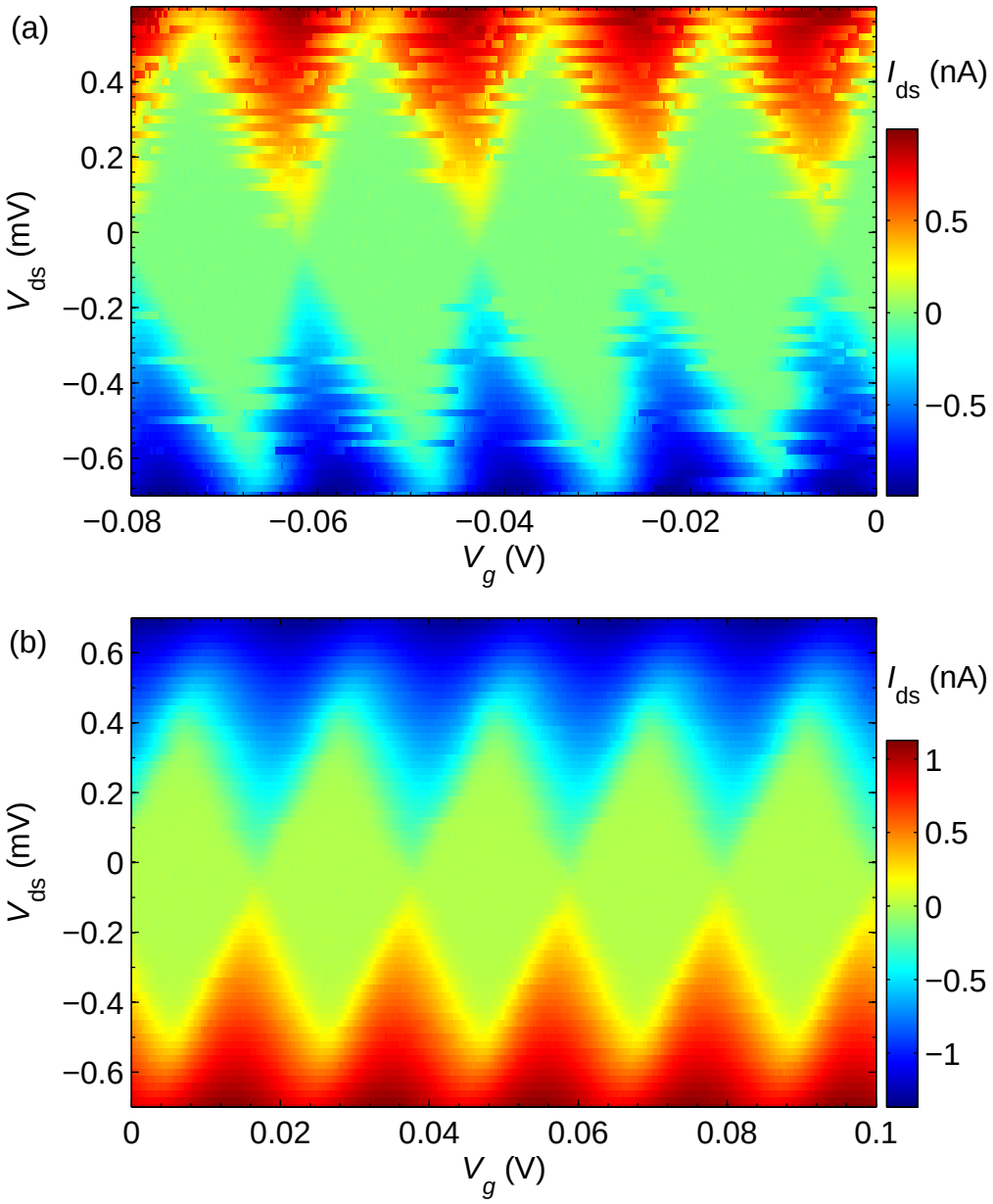


Figure 6.2: (a) Diamond chart of Al SET1. (b) Diamond chart of Al SET2. For both SETs, the drain-source current is measured using a room temperature trans-impedance amplifier. There was much more random background charge motion in Al SET1.

6.2.2 Schematic of measurement circuit

In Chap. 5, I discussed a preliminary experiment that showed that the silicon channel (n-type) is turned on at about $V_{\rm th} = 0.80$ V. Although this number could vary from one sample to the next, $V_{\rm th}$ will be at least a few hundred millivolts. However, the Al SET is not only a top gate, but also a sensitive electrometer (the reason it is put there in the first place) and I need to measure its conductance under a very small bias due to its small charging energy. To bias the Al SET and the Si channel relative to each other and to measure their conductances, one of them has to be measured using an amplifier with a floating input such that the source and drain can be lowered or raised simultaneously to a few hundred millivolts. Because the Al SET has such a small charging energy (less than 300 μV) and is more fragile than the silicon channel, I used a floating input amplifier to change the potential of the n+ contacts (for Device1, n-channel) or p+ contacts (for Device2, p-channel) to get a conducting silicon channel at the Si/SiO_2 interface, while leaving the Al SET essentially grounded.

Figure 6.3 shows a schematic of the measurement circuit for Device1 (n-channel). The setup is similar to Fig. 5.1 in Chap. 5. Both the Al SET and the Si channel conductances are measured simultaneously and independently. The two n+ contacts are dc biased at V_{n+} with the help of a room temperature floating input amplifier (Fig. 6.4). To avoid the offset voltage and extra noise from an adder, a bias-T (a high pass RC filter with a cutoff frequency 1.6 Hz) is used to apply an ac excitation $V_{\rm ac} = 10$ μV rms at 46 Hz between the two n+ contacts. The channel

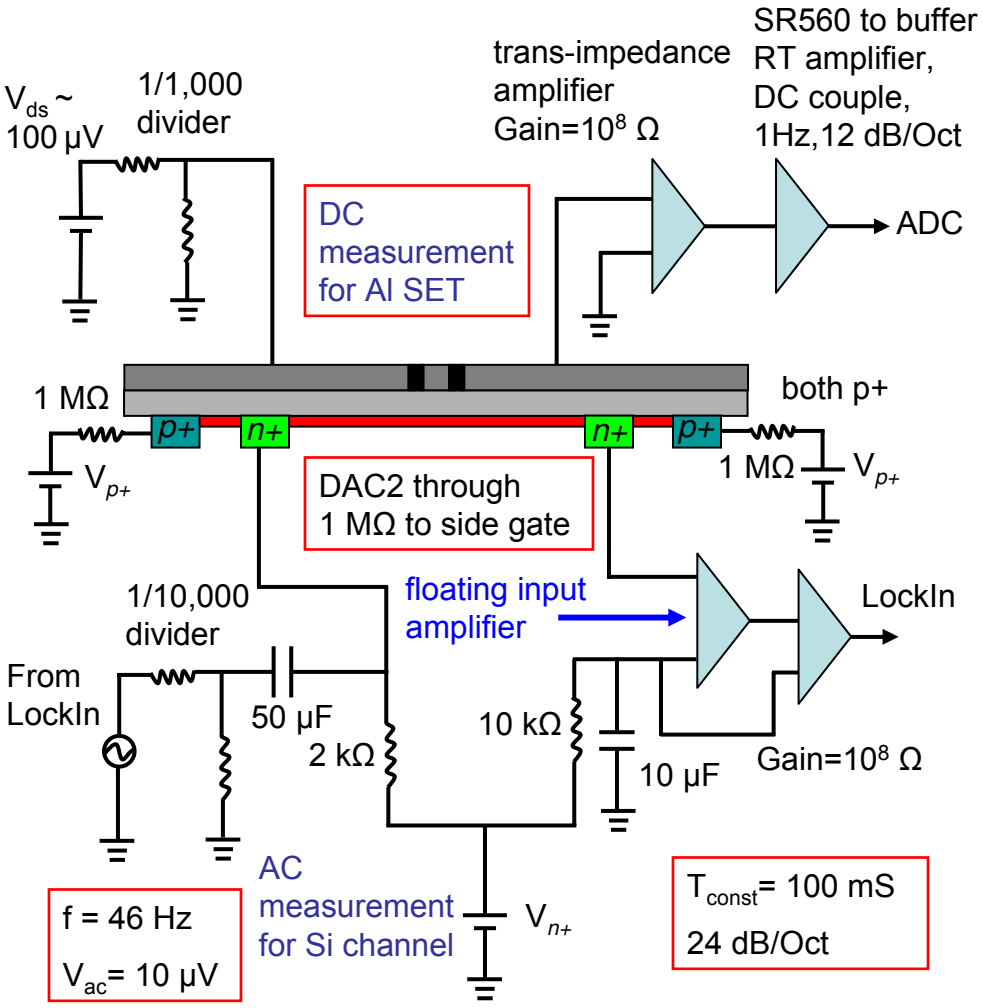


Figure 6.3: Schematic of the measurement circuit. Both the Al SET and the Si channel conductances are measured simultaneously and independently. The two n+ contacts are dc biased at V_{n+} with an ac excitation $V_{\rm ac} = 10\ \mu$V rms at 46 Hz applied through a bias-T between the two n+ contacts for a measurement of the channel differential conductance. The Al SET is dc biased with a small $V_{\rm ds} \cong 100\ \mu$V. The red region represents the MOSFET conducting channel confined between the two p+ contacts. To avoid leakage, V_{p+} is biased more negatively than V_{n+} under all circumstances.

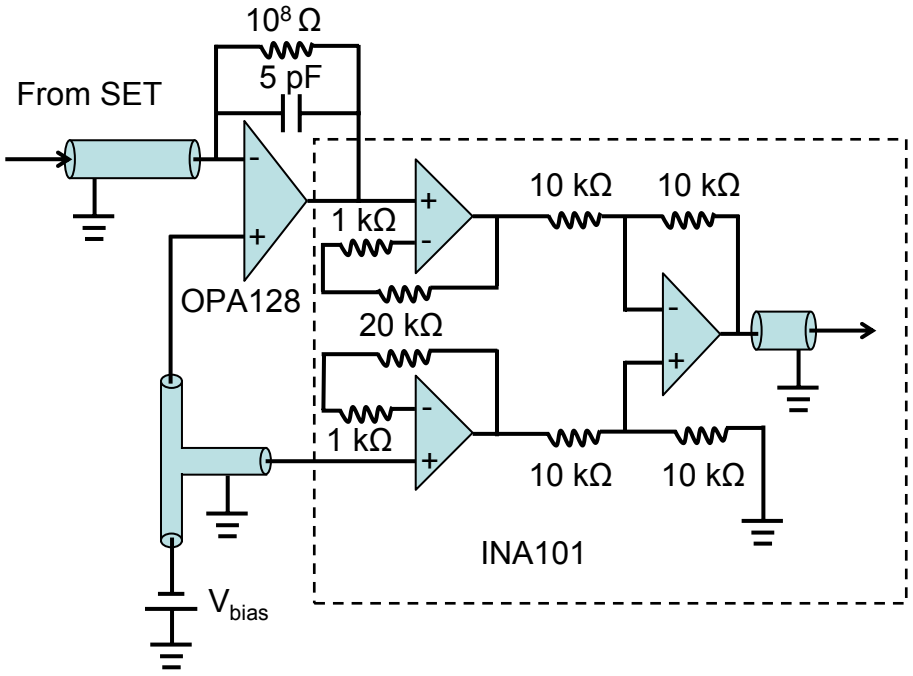


Figure 6.4: Floating input amplifier circuit. The input stage is a commercial OPA128 op-amp followed by an INA101 differential amplifier with a gain of 1.

differential conductance is measured by the floating input amplifier. The Al SET is dc biased with a small $V_{\rm ds} \cong 100\ \mu$V, and its conductance is measured through another room temperature virtual-ground trans-impedance amplifier. Each amplifier is powered by a battery at $\pm$ 15 V and has a current-to-voltage transfer function of $10^8\ \Omega$, but with different bandwidths limited by the capacitor in parallel with the feedback resistor: the one to measure the Al SET has a bandwidth of about 3 kHz; the one to measure the Si channel has a bandwidth of about 200 Hz.

The backgate is grounded all the time. To avoid leakage (see Fig. 5.3 in Chap. 5), the two p+ contacts are dc biased at potential $V_{p+} = -0.800$ V, which is more negative than V_{n+} under all circumstances. This confines the conducting channel to a small region between them.

The measurement circuit is identical for Device2 (p-channel), except that the potential of the p+ contacts V_{p+} is raised relative to the Al SET to create a hole channel at the interface. Similarly, to avoid hole leakage V_{n+} is biased more positively than V_{p+} under all circumstances.

6.2.3 Noise spectrum of measurement setup

Before I present the experimental data, I first discuss the noise level and the sensitivity of my setup. There are two main sources of current noise for this circuit — Johnson noise with a root mean square power spectral density given by:[96]

$$i_{n\_J} = \sqrt{4k_B T/R} \tag{6.1}$$

and shot noise with a root mean square power spectral density of:[96]

$$i_{n\_s} = \sqrt{2e\mathrm{I}} \tag{6.2}$$

For a feedback resistor $\mathrm{R}_{fb} = 10^8\ \Omega$, $\mathrm{i}_{n\_J} = 1.3{\times}10^{-14}\ \mathrm{A}/\sqrt{Hz}$. For a typical channel current I = 1 pA, $\mathrm{i}_{n\_s} = 5.7{\times}10^{-16}\ \mathrm{A}/\sqrt{Hz}$. So for a small channel current (I$< 10^{-10}$ A) Johnson noise of the feedback resistor will limit the smallest resolvable current. Note that this discussion ignores the amplifier noise.

Figure 6.5 shows the noise spectrum (dc component has been removed due to the ac couple to the spectrum analyzer) at the output of the floating input amplifier with the silicon channel in the off state (no channel current yet). The noise level is indeed from Johnson noise of the feedback resistor as expected. The slope of the noise spectrum floor comes from the input capacitance. Certainly, 1/f current noise, if it is present, has a very low knee frequency and is not an issue. The bumps round 20 Hz and above 80 Hz may come from mechanical vibration of the fridge or other unknown sources. Between 25 and 56 Hz, the noise spectrum is clean, so I choose 46 Hz as the excitation frequency.

To have the highest possible current sensitivity, the measurement bandwidth should be minimized, but at the expense of a long measurement time. Because the bias-T already has a time constant T = 100 ms, I set the lock-in amplifier after the floating input amplifier to have a time constant T = 100 ms with 24 dB/Oct rolloff (an equivalent noise bandwidth = 5/(64T) = 0.78 Hz). Then the final current sensitivity is $\mathrm{G}_n = 1.3{\times}10^{-14}\ \mathrm{A}/\sqrt{Hz} \times \sqrt{0.78\ Hz} = 1.15{\times}10^{-14}$ A. Because the measurement time scale is limited by the bandwidth of the lock-in amplifier, I try

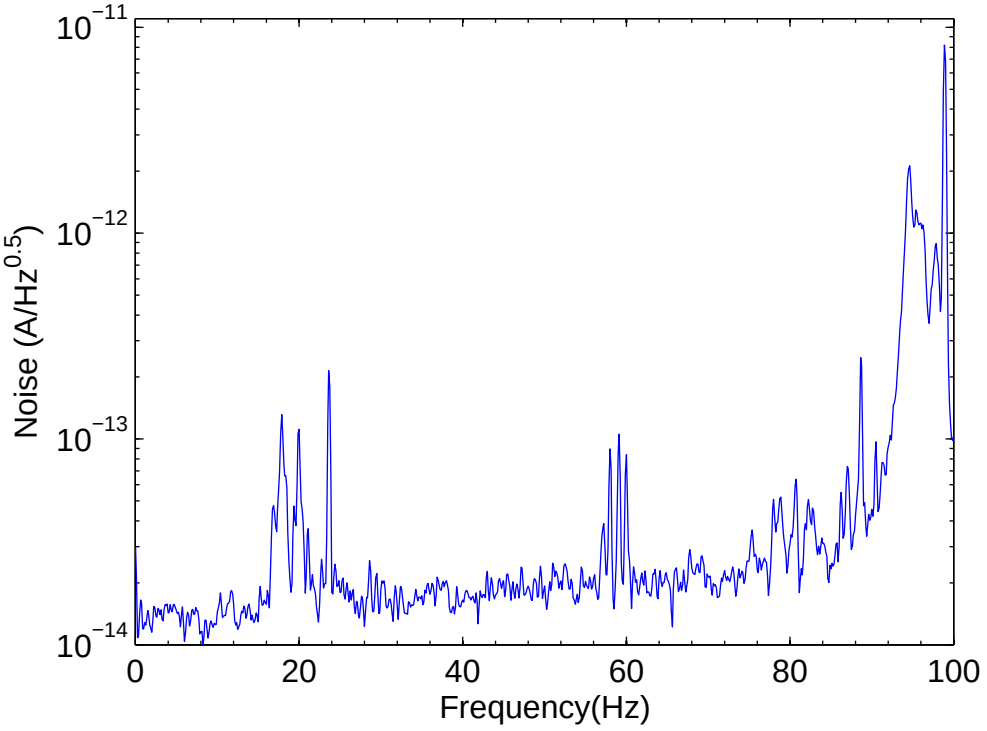


Figure 6.5: Noise spectrum at the output of the floating input amplifier with the silicon channel in the off state. The bandwidth of the amplifier is about 200 Hz. The noise level is dominated by Johnson noise of the feedback resistor.

to add a low-pass filter with a time constant of about 100 ms for a cleaner signal whenever a voltage was applied to some electrode, for example, the p+ contacts.

6.3 Experimental data and electrostatic model

Figure 6.6(a) presents typical data from Device1 for the channel differential conductance ($G_{\rm ch} = I_{\rm ch}^{\rm ac}/V_{\rm ac}$) as a function of V_{n+} at constant side gate voltage $V_g = -0.604$ V. Figure 6.6(b) presents typical data for Device2 at $V_g = V_{n+} = 1.000$ V. The appearance of Coulomb blockade oscillations is surprising, because no tunnel barriers are deliberately engineered in the channel. The oscillations seen in Device2 are not as great as those in Device1, in terms of periodicity and regularity, probably because of the much lower mobility of holes. Therefore, I will mainly focus on Device1.

In order to determine the coupling strength between the two SETs in Device1 and to infer the proximity of the islands, I do systematic sweeps of V_g and V_{n+} while the conductances of both SETs are measured. Figure 6.7(b) shows the Al SET conductance ($G_{\rm Al} = I_{\rm ds}/V_{\rm ds}$), and Fig. 6.7(d) shows the channel SET differential conductance versus V_g and V_{n+}. If each SET were electrostatically isolated from the other, the conductance maxima would trace out straight lines in these graphs as depicted in Fig. 2.4(a). Deviations from this straight-line behavior evident in Figs. 6.7(b) and 6.7(d) are a signature of discrete charging events close to the SET islands, events we would expect to observe if the two islands were in close proximity.[83, 84, 97] To confirm this hypothesis, the maxima in Figs. 6.7(b) and

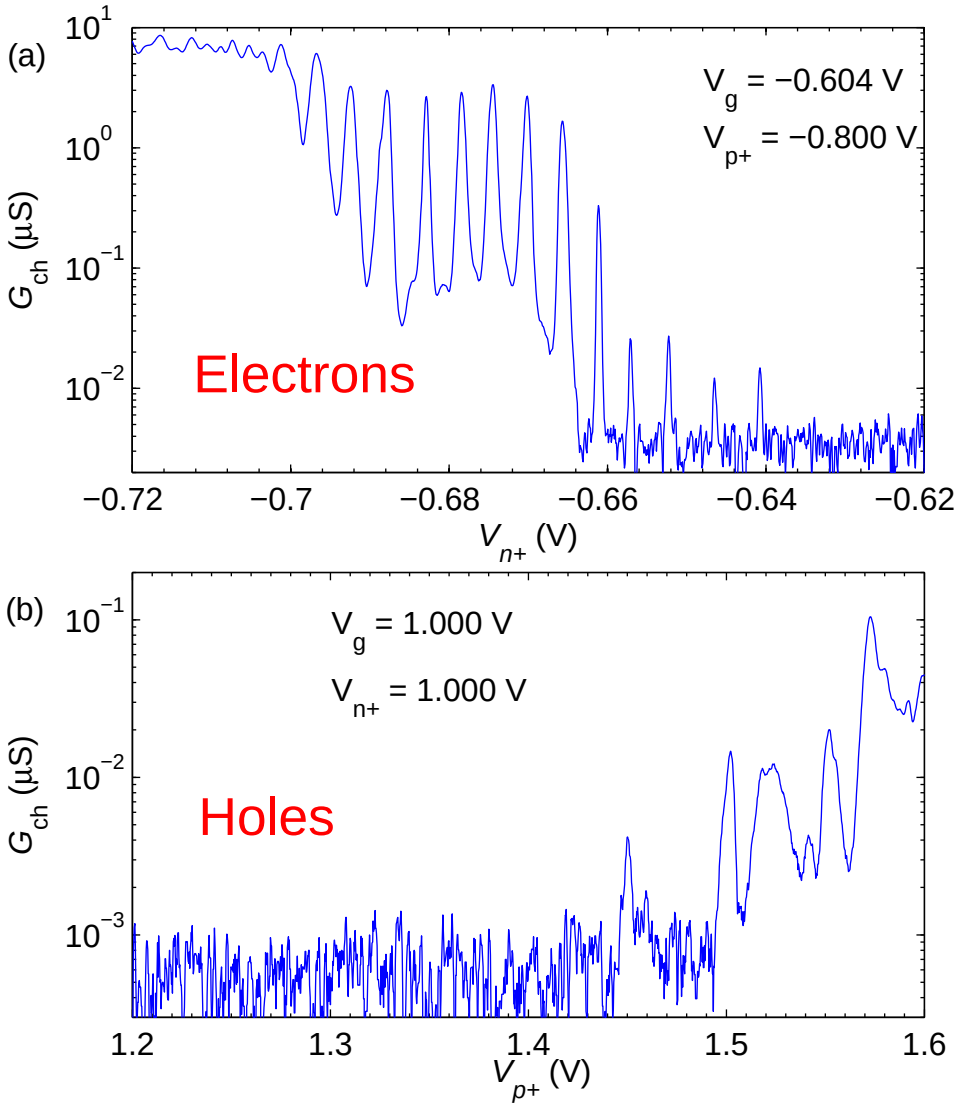


Figure 6.6: (a) and (b) Coulomb blockade oscillations of the Si SET differential conductance of Device1 and Device2 as a function of the relative bias V_{n+} and V_{p+} between the Al SET and the Si SET respectively. The Coulomb blockade oscillations of Device2 are not as great as those of Device1, in terms of periodicity and regularity, probably because of the much lower mobility of holes.

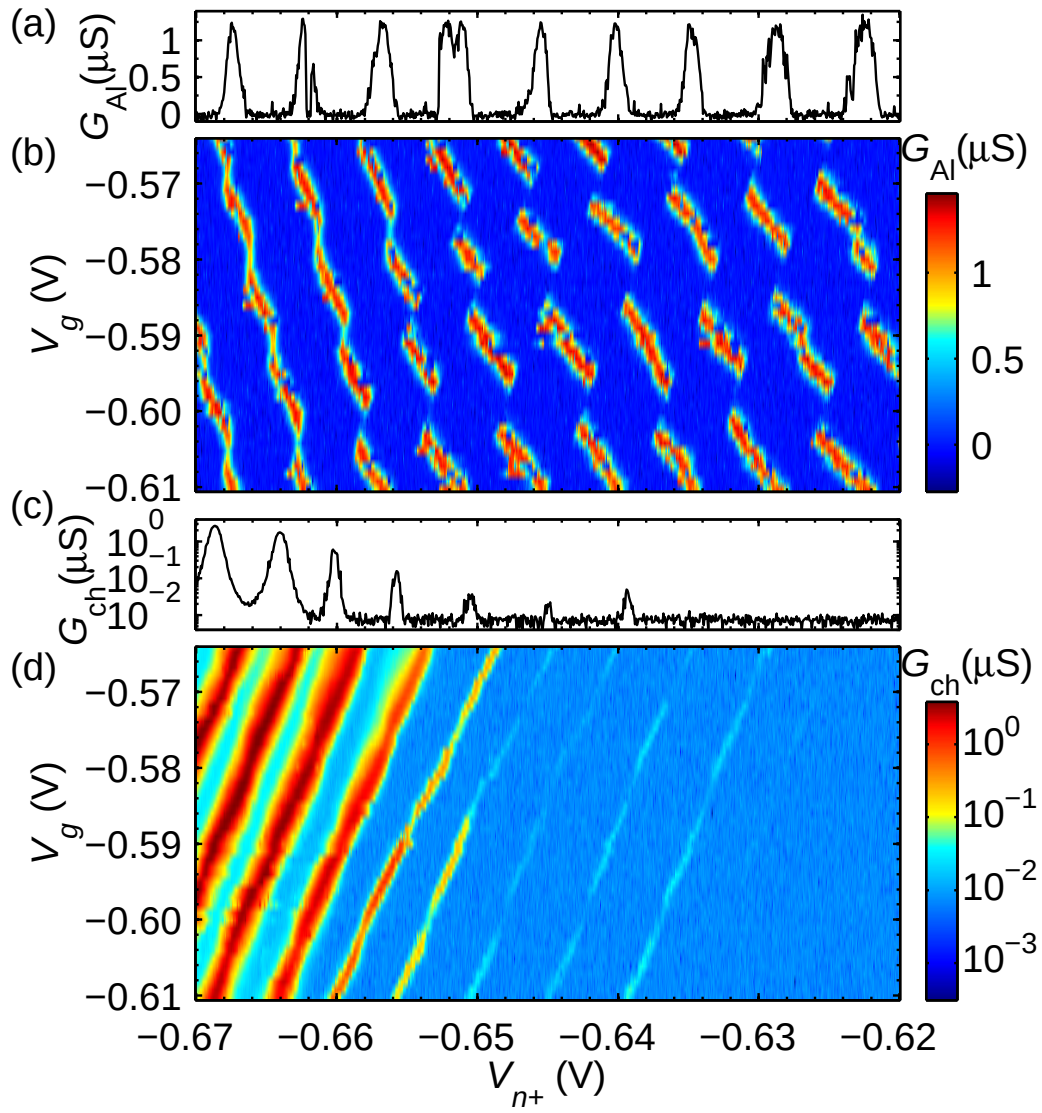


Figure 6.7: Simultaneously measured conductances of both the Al and the Si SETs. (a) and (c) Coulomb blockade oscillations of the Al and the Si SET conductances, respectively, at $V_g = -0.610$ V measured as a function of V_{n+}. (b) and (d) 2D false-color plots of conductances of the Al and the Si SET, respectively, versus V_g and V_{n+}.

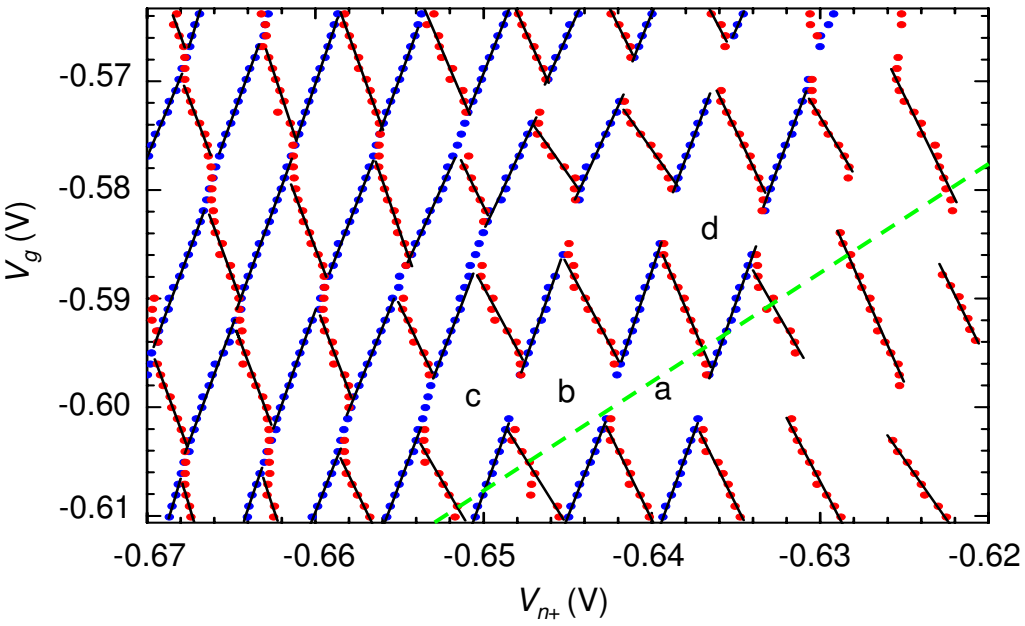


Figure 6.8: Conductance maxima of both SETs versus V_{n+} and V_g. Red dots and blue dots are Gaussian fits to the data in Figs. 6.7(b) and 6.7(d), respectively. Black lines are a linear fit to the points on each edge. The regions labeled a, b, c, d are the four hexagons whose parameters are presented in Table 6.1. Dotted green line is the x-axis of Fig. 6.10 that I used for the charging energy measurement of the Si SET.

6.7(d) are fitted with Gaussians, and the resulting peak centroids are plotted in Fig. 6.8. The two SETs display a clear correlation: whenever an Al SET conductance peak trace meets one from the Si SET, it makes an abrupt step, and vice versa. Because each peak trace corresponds to a unit change in the number of electrons on the corresponding SET island, this correlation proves that single-electron charging events in one SET are coupled to the other.

To more quantitatively explain the above results, I have modeled the device using the circuit depicted in Fig. 6.9(a) which is identical to Fig. 2.3 except for some differences in notation. I use the same matrix form method as in Sec. 2.3.2 to calculate the electrostatics, as follows. Under the assumption that the system will minimize its electrostatic energy automatically by adjusting the number of electrons N_{Si} and N_{Al} on the two SET islands, the total electrostatic energy of this circuit is given in matrix form by:

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, V_g, V_{n+}) = \frac{1}{2}\mathbf{Q}^T \begin{pmatrix} C_{\Sigma\_\mathrm{Al}} & -C_c \\ -C_c & C_{\Sigma\_\mathrm{Si}} \end{pmatrix}^{-1} \mathbf{Q}. \tag{6.3}$$

Here $C_{\Sigma\_\mathrm{Al}} = C_1 + C_3 + C_c + C_{g\_\mathrm{Al}}$ and $C_{\Sigma\_\mathrm{Si}} = C_2 + C_4 + C_c + C_{g\_\mathrm{Si}}$ are the total capacitance of the Al SET and of the Si SET island, respectively. The charge matrix $\mathbf{Q}$ is:

$$\mathbf{Q} = \begin{pmatrix} -eN_{\mathrm{Al}} + C_{g\_\mathrm{Al}}V_g + C_3V_{n+} \\ -eN_{\mathrm{Si}} + C_{g\_\mathrm{Si}}V_g + C_2V_{n+} \end{pmatrix} \tag{6.4}$$

Under energy degenerate conditions, Coulomb blockade is lifted, resulting in the maximal SET conductances. There are in total six such degeneracy conditions associated with adding or subtracting one electron from an SET island, determined

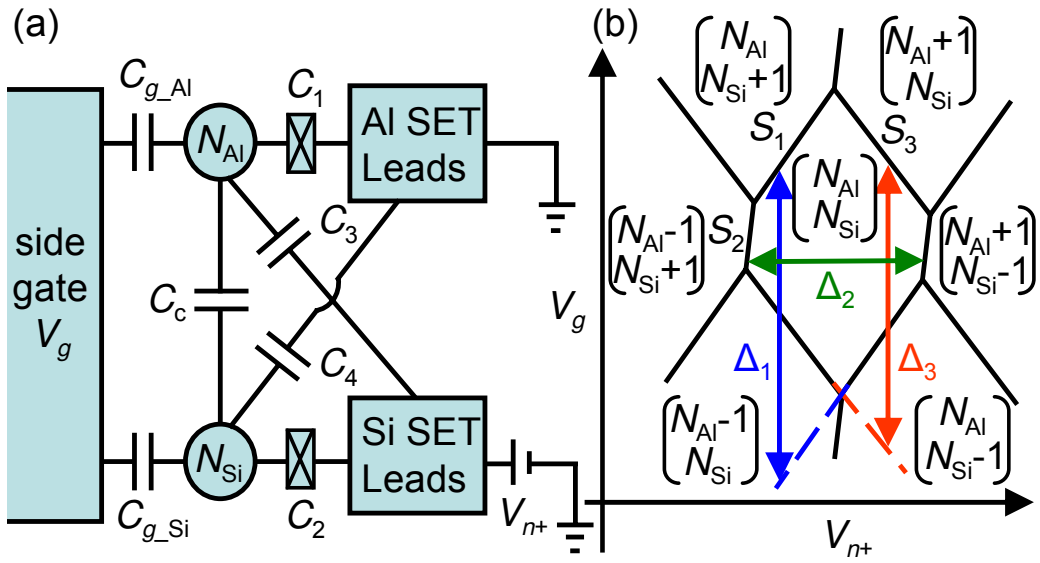


Figure 6.9: (a) Circuit model for the coupled SET system. N_{Al} and N_{Si} are the number of electrons on the Al and Si SET island, respectively. Due to the very small drain-source bias of each SET, I can simplify the two tunnel barrier capacitances for each SET to a single capacitance (C_1 and C_2) as shown. (b) Hexagonal phase diagram based on the model in (a). Each hexagon represents a configuration with a different number of charges on the SET islands. S_1, S_2, and S_3 are the slopes of the hexagon edges. Δ_1, Δ_2, and Δ_3 are the separations between opposite parallel edges of the hexagon.

by:

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, V_g, V_{n+}) = E(N_{\mathrm{Al}} + \delta N_{\mathrm{Al}}, N_{\mathrm{Si}} + \delta N_{\mathrm{Si}}, V_g, V_{n+}) + (\delta N_{\mathrm{Si}}) e V_{n+}. \quad (6.5)$$

Here $\delta N_{\mathrm{Al}} = 0, \pm 1$; $\delta N_{\mathrm{Si}} = 0, \pm 1$; and $|\delta N_{\mathrm{Al}} + \delta N_{\mathrm{Si}}| < 2$, and $(\delta N_{\mathrm{Si}}) e V_{n+}$ is the extra work done by voltage source V_{n+} when one electron tunnels through junction C_2.[46] These equations establish the hexagonal phase diagram depicted in Fig. 6.9(b) with six defined parameters — three slops S_1, S_2, S_3 and three separations Δ_1, Δ_2, Δ_3:

$$S_1 = \frac{C_{\Sigma\_\mathrm{Al}} C_{\Sigma\_\mathrm{Si}} - C_{\Sigma\_\mathrm{Al}} C_2 - C_c C_3 - C_c^2}{C_{\Sigma\_\mathrm{Al}} C_{g\_\mathrm{Si}} + C_c C_{g\_\mathrm{Al}}} \quad (6.6)$$

$$S_2 = \frac{C_{\Sigma\_\mathrm{Al}} C_{\Sigma\_\mathrm{Si}} + C_{\Sigma\_\mathrm{Si}} C_3 + C_c C_2 - C_{\Sigma\_\mathrm{Al}} C_2 - C_c C_3 - C_c^2}{C_{\Sigma\_\mathrm{Al}} C_{g\_\mathrm{Si}} - C_{\Sigma\_\mathrm{Si}} C_{g\_\mathrm{Al}} + C_{g\_\mathrm{Al}} C_c - C_{g\_\mathrm{Si}} C_c} \quad (6.7)$$

$$S_3 = -\frac{C_{\Sigma\_\mathrm{Si}} C_3 + C_c C_2}{C_{\Sigma\_\mathrm{Si}} C_{g\_\mathrm{Al}} + C_c C_{g\_\mathrm{Si}}} \quad (6.8)$$

$$\Delta_1 = \frac{e C_{\Sigma\_\mathrm{Al}}}{C_{\Sigma\_\mathrm{Al}} C_{g\_\mathrm{Si}} + C_c C_{g\_\mathrm{Al}}} \quad (6.9)$$

$$\Delta_2 = \frac{e(C_{\Sigma\_\mathrm{Al}} + C_{\Sigma\_\mathrm{Si}} - 2C_c}{C_{\Sigma\_\mathrm{Al}} C_{\Sigma\_\mathrm{Si}} + C_{\Sigma\_\mathrm{Si}} C_3 + C_c C_2 - C_{\Sigma\_\mathrm{Al}} C_2 - C_c C_3 - C_c^2} \quad (6.10)$$

$$\Delta_3 = \frac{e C_{\Sigma\_\mathrm{Si}}}{C_{\Sigma\_\mathrm{Si}} C_{g\_\mathrm{Al}} + C_c C_{g\_\mathrm{Si}}} \quad (6.11)$$

There is a correspondence evident between this diagram and the data in Fig. 6.8. However, the capacitances associated with the Si SET appear to be bias voltage dependent, resulting in the non-identical hexagons in the data.

There are in total seven capacitance parameters in the circuit model. The total tunnel barrier capacitance of the Al SET $C_1 = 282$ aF has been extracted from diamond chart measurements in Sec. 6.2 with the Si SET in the off state ($V_{n+} = 0$ V). C_1 is dominated by overlap between the Al SET leads and its island, and should be insensitive to the presence or absence of an underlying Si SET channel. The

remaining six parameters can be extracted from the slopes S_1, S_2, S_3 and the separations Δ_1, Δ_2, Δ_3 of each hexagon in Fig. 6.8, as defined in Fig. 6.9(b). However, since the capacitances associated with the Si SET are bias voltage dependent, the assumption that the capacitance values are fixed within one hexagon is not strictly self-consistent. Nevertheless, the edges of the hexagon can still be fitted reasonably well with lines, because each hexagon spans a small voltage interval. Given the complexity of the problem, it is not clear how to determine error bars.

In the end, I extract the three slopes and three separations from the data as follows. First, the boundaries given by $\delta N_{\mathrm{Al}}+\delta N_{\mathrm{Si}} = \pm 1$ (the nominally straight lines traced out by the data in Fig. 6.8) are each fit to a line. Boundaries corresponding to $\delta N_{\mathrm{Al}}+\delta N_{\mathrm{Si}} = 0$ (an effective transfer of an electron from one island to the other) are not clearly visible, so they are determined by neighboring intersections of the visible boundaries. To compensate for gradual changes in the capacitances with bias voltage, averages are made for the slopes and separations from opposite boundaries within each hexagon. Then the six unknown capacitances can be extracted by solving six analytical equations relating S_1, S_2, S_3, Δ_1, Δ_2, and Δ_3.

Discrete background charge motion near the SET islands, which changes the electrostatics of the system, makes systematic study of all the hexagons in Fig. 6.8 difficult. The capacitances for the four typical hexagons labeled in Fig. 6.8 are presented in Table 6.1. For hexagon (a), $C_{\Sigma\_\mathrm{Si}} = 49$ aF, and for hexagon (b), $C_{\Sigma\_\mathrm{Si}} = 60$ aF. To check the validity of the circuit model, I made an independent diamond chart measurement of the Si SET (see Fig. 6.10) along a line depicted in Fig. 6.8. At the bias point near hexagon (a) and (b), the charging energy of the

Table 6.1: Capacitances (in aF) of the four hexagons labeled in Fig. 6.8 for the circuit model in Fig. 6.9. Individually changing C_c by 5%, C_2 by 15%, C_3 by 10%, C_4 by 50%, C_{g_Al} by 5%, or C_{g_Si} by 5% produces qualitatively worse fits to the data.

hexagon	C_c	C_2	C_3	C_4	C_{g_Al}	C_{g_Si}	C_{Σ_Al}	C_{Σ_Si}
a	16	20	14	7	4.1	6.0	316	49
b	21	32	7	1	4.6	6.0	315	60
c	22	32	7	2	4.1	6.7	315	63
d	21	31	10	2	3.9	5.9	317	60

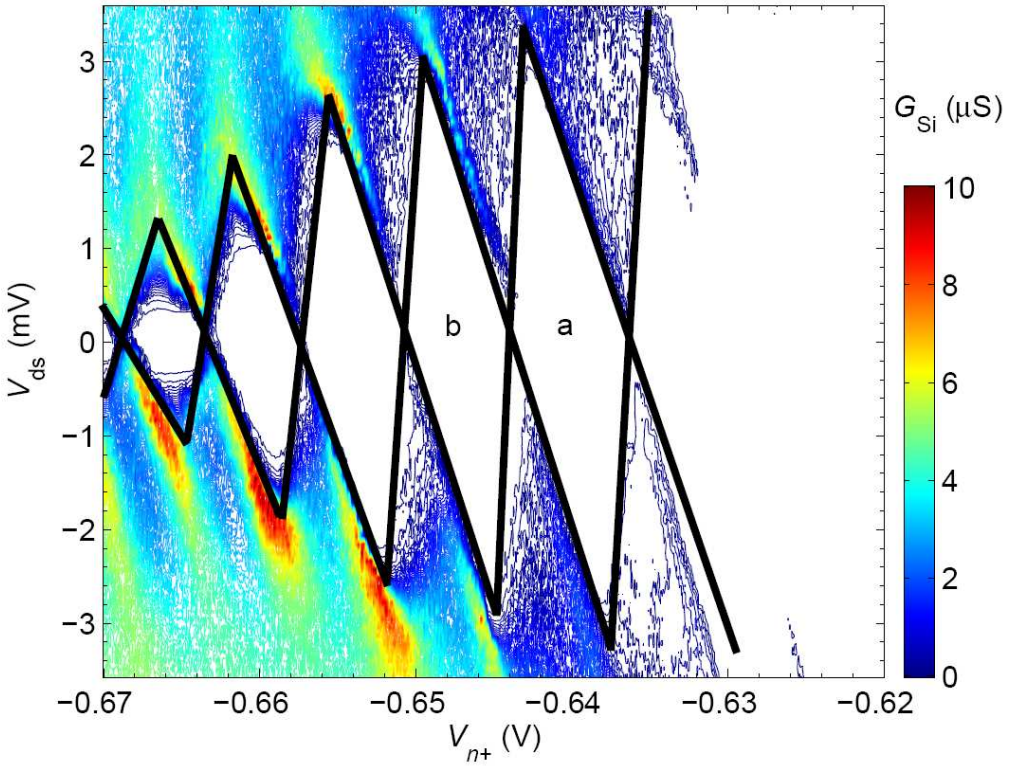


Figure 6.10: Diamond chart of Si SET1 measured along a line depicted in Fig. 6.8. The charging energy of the SET is a few meV, but not constant. It strongly depends on bias voltage or the number of electrons on the SET island. Diamond a and b are near the bias points of hexagon a and b in Fig. 6.8.

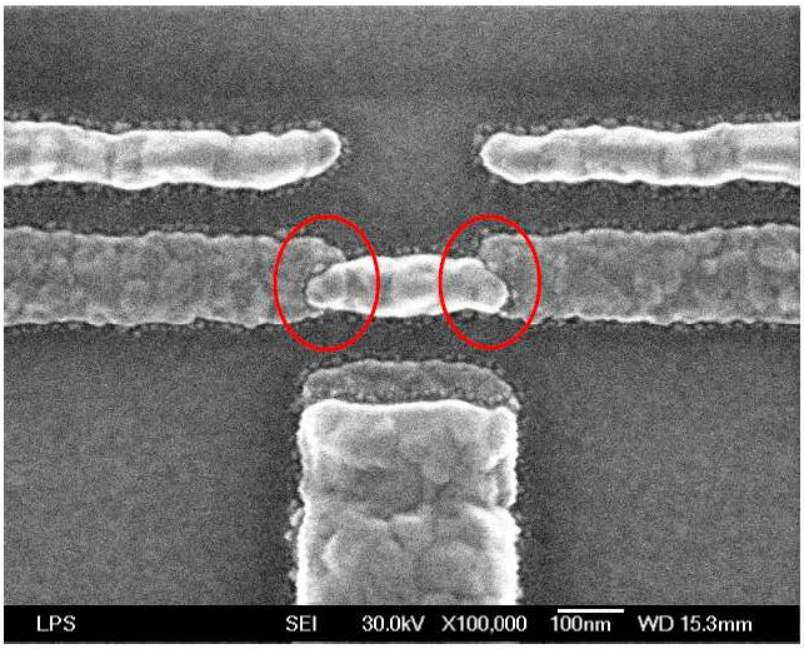
Si SET is $C_{\Sigma\_Si} = 49$ aF and $C_{\Sigma\_Si} = 53$ aF respectively, in good agreement with the calculated values in Table 6.1 and confirming the validity of the circuit model. Significantly, for all the hexagons in Table 6.1, $C_c/C_{\Sigma\_Si} \cong 33 - 35\%$ indicates that the Si SET is strongly coupled to the Al SET, while $C_c/C_{\Sigma\_Al} \cong 5 - 7\%$. The relative small value of C_c/C_{Σ_Al} explains why the discontinuities in Fig. 6.7(d) are less obvious than those in Fig. 6.7(b).

Some additional features in Fig. 6.10 are worth commenting on. The closed diamond structures provide good evidence for transport through a single island and not multiple islands in series in the channel. The charging energy of the Si SET is a few meV, but not constant. It strongly depends on bias voltage or the number of electrons on the Si SET island. The reason could be that this is a few-electron regime, and the single particle level spacings are not constant. Another, more likely possibility, is that the tunnel capacitance of the Si SET depends on the bias voltage. If we assume the tunnel barriers have a triangular shape, when the barrier height is lowered, the width of the barriers will also decrease, resulting in an increase in tunnel capacitances.[98]

6.4 Hypothesis for the alignment of the Al and Si SET islands

If the overlap between the two SET islands were perfect, the value of C_c as calculated from the Al SET island dimensions (Fig. 6.11) and the SiO_2 thickness would be about 30 aF. This is close to the values in Table 6.1 for hexagons (b), (c), and (d). The small values for C_4 in these hexagons mean that there is almost no

(a)



(b)

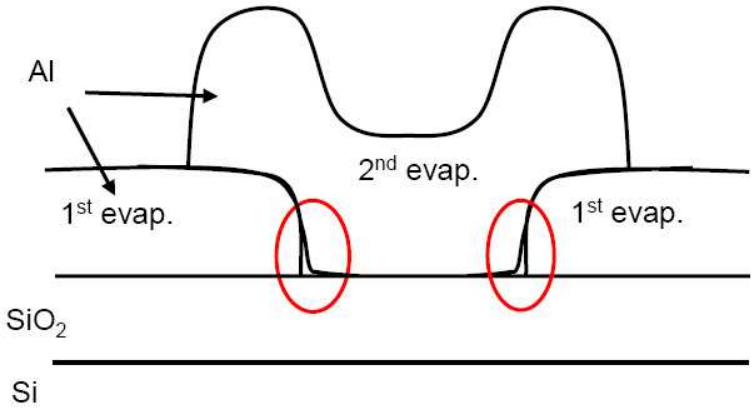


Figure 6.11: (a) SEM image of Al SET1. Red circles emphasize the width difference between the Al SET island and leads which may lead to lateral constriction and create tunnel barriers in the Si channel below. (b) Between the two evaporations there could be a gap at the edges of the Al SET leads with vacuum or AlO_x as the dielectric material, so the effective electric field to bend the Si band will be weaker at those parts, resulting in energy barriers in the channel.

overlap between the Si SET island and the Al SET leads. This strongly suggests that the induced Si SET island is located directly beneath the Al SET island.

I hypothesize the following reasons for the formation of an aligned SET in the channel. Although the width of the SET island and leads in the evaporation shadow mask are the same, the SET island is formed during the second evaporation. A slow pinch-off of features in the mask during the first evaporation therefore makes the island slightly narrower than the leads (see Fig. 6.11(a)). If the angle between evaporations is incorrect, there may also be a lateral offset between island and leads. This island/leads width asymmetry and lateral offset may lead to lateral constrictions in the MOSFET channel below, creating tunnel barriers and therefore an SET in the Si channel aligned with the Al SET above. Another possibility is that between the two evaporations there could be a gap at the edges of the Al SET leads, with vacuum or AlO_x dielectric material in the gap. This would lead to the effective electric field being weaker at those parts, resulting in energy barriers in the channel since the Si band will be bent less [see Fig. 6.11(b)].

6.5 High carrier density regime

In this section, I discuss briefly another regime — when the electric field of the side gate is strong enough to deplete channel electrons, it will pinch off the heavily conducting silicon channel. Near the pinch-off, Coulomb blockade oscillations in the silicon channel are observed as well. From the geometry of the device, the Si SET island should be closest to the side gate and underneath the Al SET island.

Actually, this is exactly what I planned to get when I originally designed this device: to use an Al SET to detect the hopping of electrons at the Si/SiO_2 interface while a nearby side gate is pinching off the channel. Because of this alignment, a similar correlation between the Al and Si SETs is expected.

Figure 6.12 shows such a correlation between the two SETs. Note in this figure the y-axis is V_{n+} and x-axis is V_g. The regular small steps in the Si SET conductance peak traces clearly reflect the single electron charging effect on the Al SET island. The better uniformity and more regular period of the steps in the two left-most peak traces of the Si SET imply that the shape of the Si SET island under those bias conditions is more regular. In addition, these two peak traces correspond to very clear jumps in the Al SET conductance peak traces. However, for reasons that are not clear, the other four are much less obviously correlated with the Al SET peak traces.

Another feature of Fig. 6.12 is that when V_g becomes more negative, but before the channel is completely depleted, the channel conductance becomes non-measurable while the Al SET keeps sensing the depletion of electrons on the Si SET island. This behavior is also observed in the low carrier density regime near the channel threshold, as depicted in Fig. 6.13. Although the Al SET signals are noisier when $V_g > -0.60$ V, it is still clear that about 10 electrons have already accumulated on the Si SET island when the first measurable Si SET conductance peak appears. This behavior is apparently common in other Si SETs. For example, Simmons *et al.* used an integrated QPC to continue the detection of the discharge of electrons on a SiGe quantum dot when the direct current measurement through

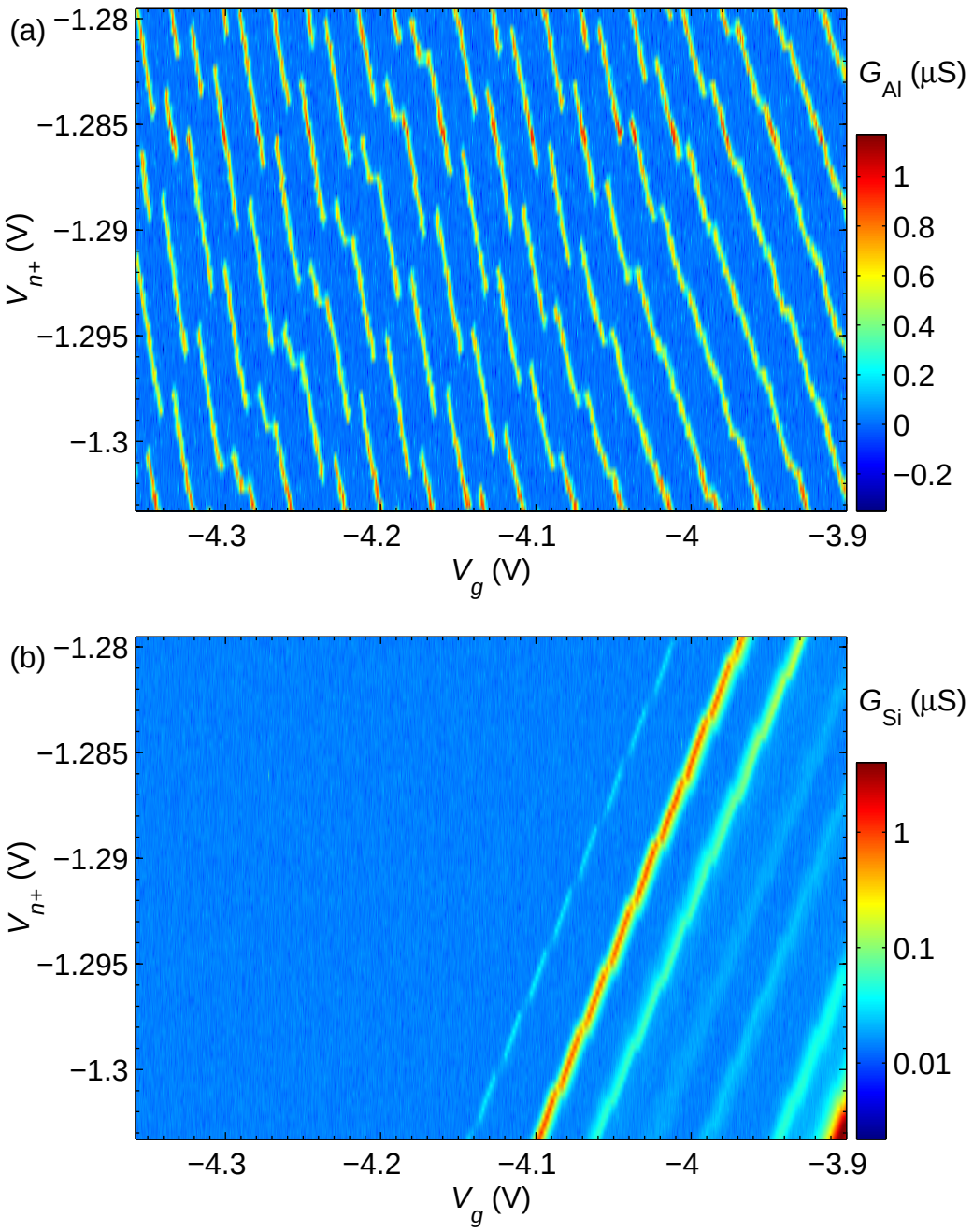


Figure 6.12: Simultaneously measured conductances of both the Al and the Si SETs near the pinch-off by a side gate in the high conducting regime. (a) and (b) Conductances of the Al and the Si SET, respectively, vs V_{n+} and V_g at $V_{p+} = -4.30$ V. Note in this figure the y-axis is V_{n+} and x-axis is V_g.

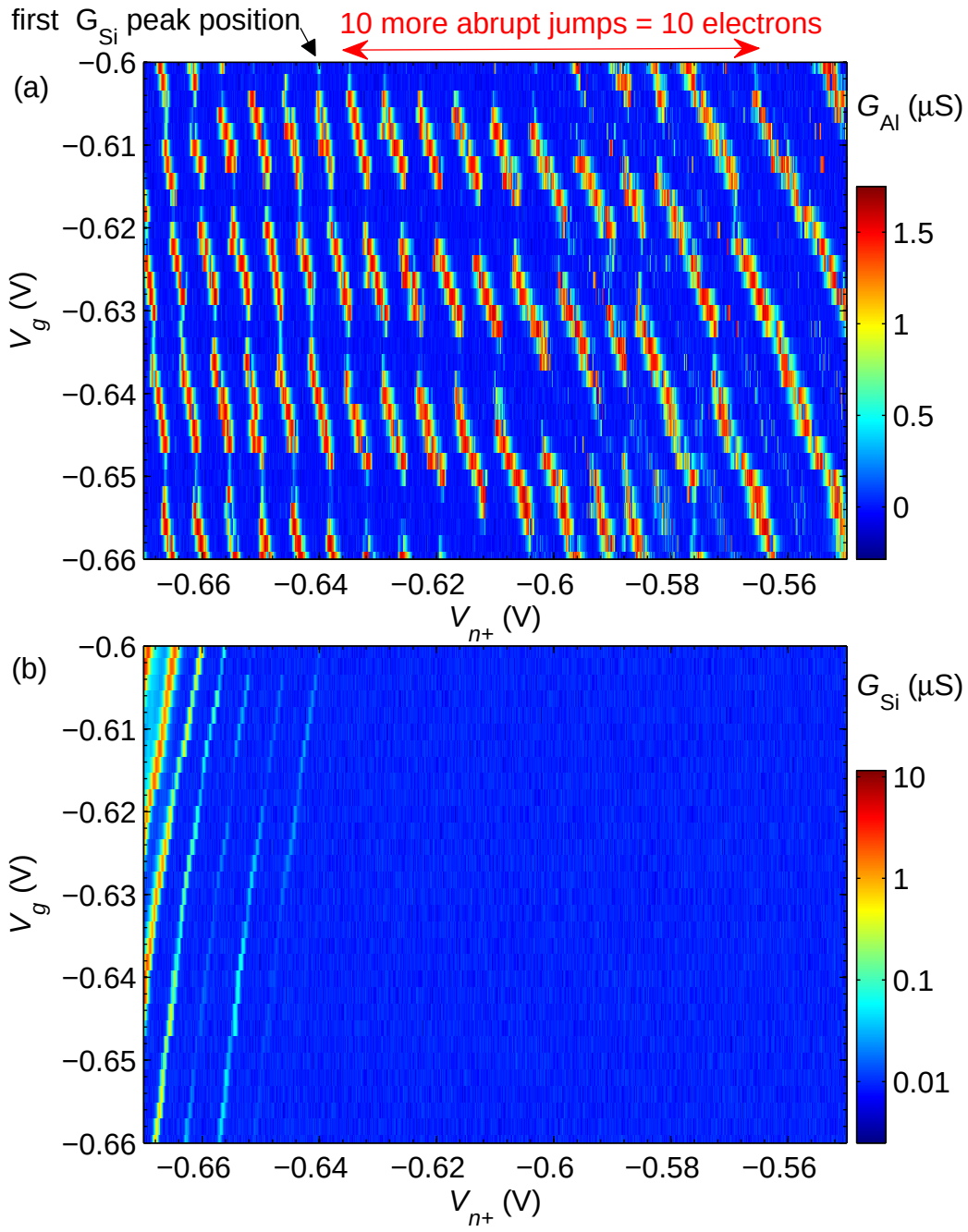


Figure 6.13: Simultaneously measured conductances of both the Al and the Si SETs in the subthreshold regime. (a) and (b) Conductances of the Al and the Si SET, respectively, vs V_g and V_{n+}. The Al SET signals show that about 10 electrons have already accumulated on the Si SET island when the first measurable Si SET conductance peak appears.

the dot was below the noise floor.[99]

From these results we can see that the Al SET acts not only as a gate, but also as an integrated sensor that can in principle tell the number of electrons on the Si SET island. This dual functionality of the Al SET makes this device geometry potentially useful for quantum computation based on Si quantum dots.[50]

6.6 Conclusions

In conclusion, in this chapter I demonstrated that an Al SET can be used as a top gate of a conventional MOSFET to induce a Si SET at the Si/SiO_2 interface near the channel threshold. I also developed a simple electrostatic model to explain the correlated jumps between the two SET conductances and attributed them to single-electron charging effects on the SET islands. The electrostatic model revealed that the two SET islands are closely aligned, with an inter-island capacitance approximately equal to 1/3 of the total capacitance of the Si transistor island, indicating that the Si transistor is strongly coupled to the Al transistor. In the high carrier density regime where a side gate pinches off a heavily conducting Si channel, a similar correlation between the two SETs is also observed.

Since both the Al and Si SETs are sensitive electrometers, this SET sandwich architecture could be used to characterize a MOS structure at low temperature via a cross-correlation measurement between the two SETs.[25, 82] In Chap. 7, I use this architecture to identify sources of unwanted charge motion that may also be sources of decoherence for Si quantum computation.[18, 19] Because the SiO_2 layer could

be made much thinner, future experiments could more fully explore the strongly coupled two-SET regime.

Chapter 7

Characterization of a MOS structure at low temperature using vertically coupled Al and Si SETs

7.1 Overview

In Chap. 6, I showed that an Al SET can be used as a top gate of a narrow n-channel MOSFET and can induce a "mirror" Si SET at the Si/SiO_2 interface. The Coulomb blockade oscillations of the induced Si SET were robust against thermal cycles between base temperature and room temperature. In this chapter, I first discuss two other devices fabricated one year after the device studied in Chap. 6. Both of them display similar behavior – the island of the induced Si SET is aligned with that of the Al SET. Second, I describe the characterization of a MOS structure using such a vertically coupled Al and Si SET system at low temperature. A single charge defect is detected by both SETs. After ruling out the possibility of a TLF, I argue that the defect is tunnel-coupled to the Si SET and is probably either a single charge trap at the Si/SiO_2 interface or a single donor in the Si substrate. The two SET islands and the defect can be modeled as a three-dot system. Due to the negligible charging energy of the Al SET, the three-dot model can be further simplified to a two-dot model, similar to that in Chap. 6. By solving the two-dot model, the capacitances in percentages associated with the defect are extracted.

Based on the ratios of the capacitances, the location of the defect can be estimated. Other properties of the defect such as the coupling strengths to both SETs and the occupancy switching as a function of gate voltage, and the linearity of positions where the defect changes its occupancy in voltage space, are also studied in this chapter.

7.2 Characterization of Al and Si SETs at low temperature

I fabricated Device3 and Device4 (both are n-channel) on the same Si wafer used for Device1 and Device2, using the same fabrication technique as described in Chap. 4. Both devices were measured in the same measurement environment as Device1 studied in Chap. 6: at 20 mK in a dilution refrigerator with 1 T magnetic field to keep the Al SET in normal state.

For Device3, the width of the Al SET island was intentionally fabricated narrower than the leads. In the e-beam lithography pattern, the width of the island was designed to be 80 nm wide, while the leads were 100 nm wide. In Device3, the island and the leads were targeted to be aligned with each other. For Device4, the Al SET island was just slightly narrower that the leads (85 nm vs. 90 nm). But the island and the leads were targeted to have some offset ($\cong$ 35 nm).

Figure 7.1 shows the SEM images of Device3 and Device4 after I finished measuring them. Unfortunately, when I placed Device3 on the SEM sample holder for imaging, SET3 was blown up, as evidenced by the melted tunnel junctions in Fig. 7.1(b). After imaging, SET3 was a short at room temperature. SET4 survived

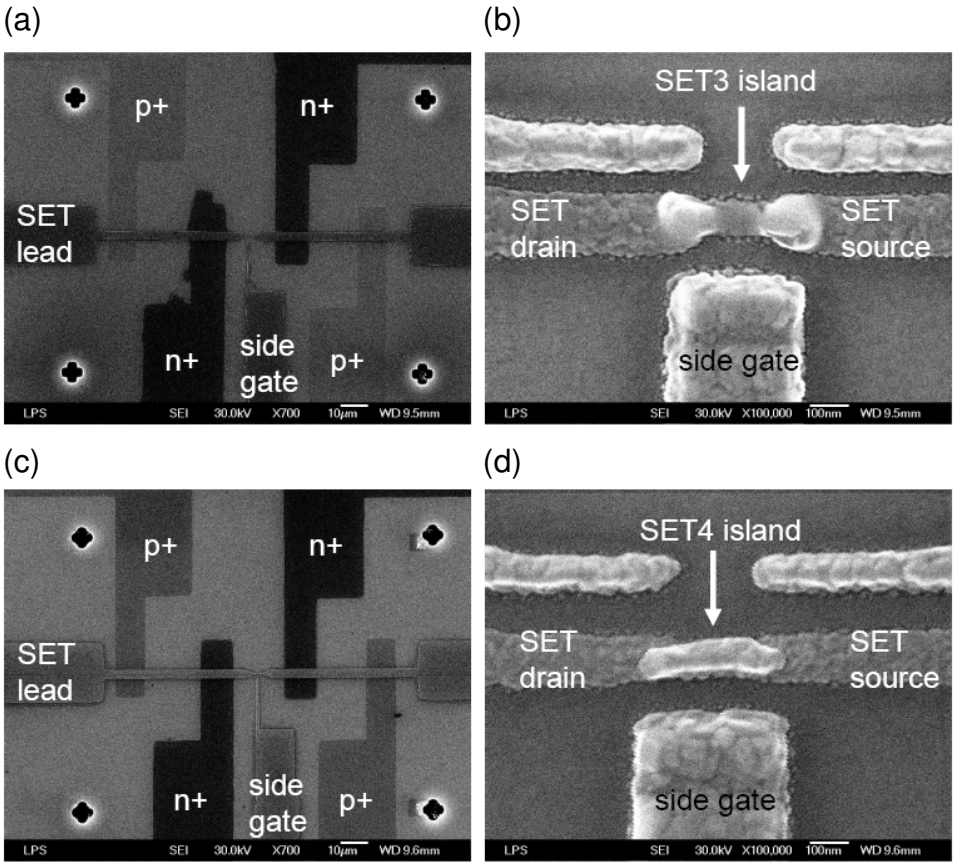


Figure 7.1: (a) and (b) SEM images of Device3, (c) and (d) SEM images of Device4. In (a) and (c), the darkest regions are n+ contacts, the gray regions are p+ contacts, and the four crosses at the four corners are the alignment marks for photo and e-beam lithographies. These images were taken after the devices were measured in a dilution refrigerator. SET3 blew up before imaging, as evidenced by the melted tunnel junctions in (b).

the SEM imaging, however its resistance increased from 86 kΩ to 94 kΩ. This suggests that the electron beam during SEM imaging might have had some effect on the Al SET tunnel junctions.

Diamond chart measurement of both Al SETs

Figure 7.2(a) shows the diamond chart of Al SET3 measured using a DC bias and Fig. 7.2(b) shows the AC differential conductance. Based on the diamond, I find the charging energy is $E_C = 112$ μV, the slopes of the diamond edges are $S_1 = 0.01837$ and $S_2 = -0.02256$, and the period of the diamonds is $\Delta V_g = 22.0$ mV. The total capacitance C_Σ, side gate capacitance C_g, and the two tunnel capacitances C_{11}, C_{12} can then be extracted based on Eqs. 2.4, 2.5, and 2.6 in Sec. 2.1. I find $C_\Sigma = 714$ aF, $C_g = 7.27$ aF, $C_{11} = 388.6$ aF, and $C_{12} = 322.4$ aF.

Figures 7.3(a) and 7.3(b) show the diamond charts for Al SET4. Using the same method, I find $E_C = 92.5$ μV, $C_\Sigma = 865$ aF, $C_g = 9.31$ aF ($\Delta V_g = 17.2$ mV), $C_{11} = 427.9$ aF ($S_1 = 0.02130$), and $C_{12} = 425.1$ aF ($S_2 = -0.02191$).

Coulomb blockade oscillations of both Si SETs and the diamond chart of Si SET3

Using the measurement circuit and technique as depicted in Fig. 6.3, I measure Coulomb blockade oscillations in the Si channel differential conductance near the channel threshold on both Device3 and Device4. Figure 7.4 shows the Coulomb blockade oscillations as a function of the relative bias V_{n+} between the Al SET and

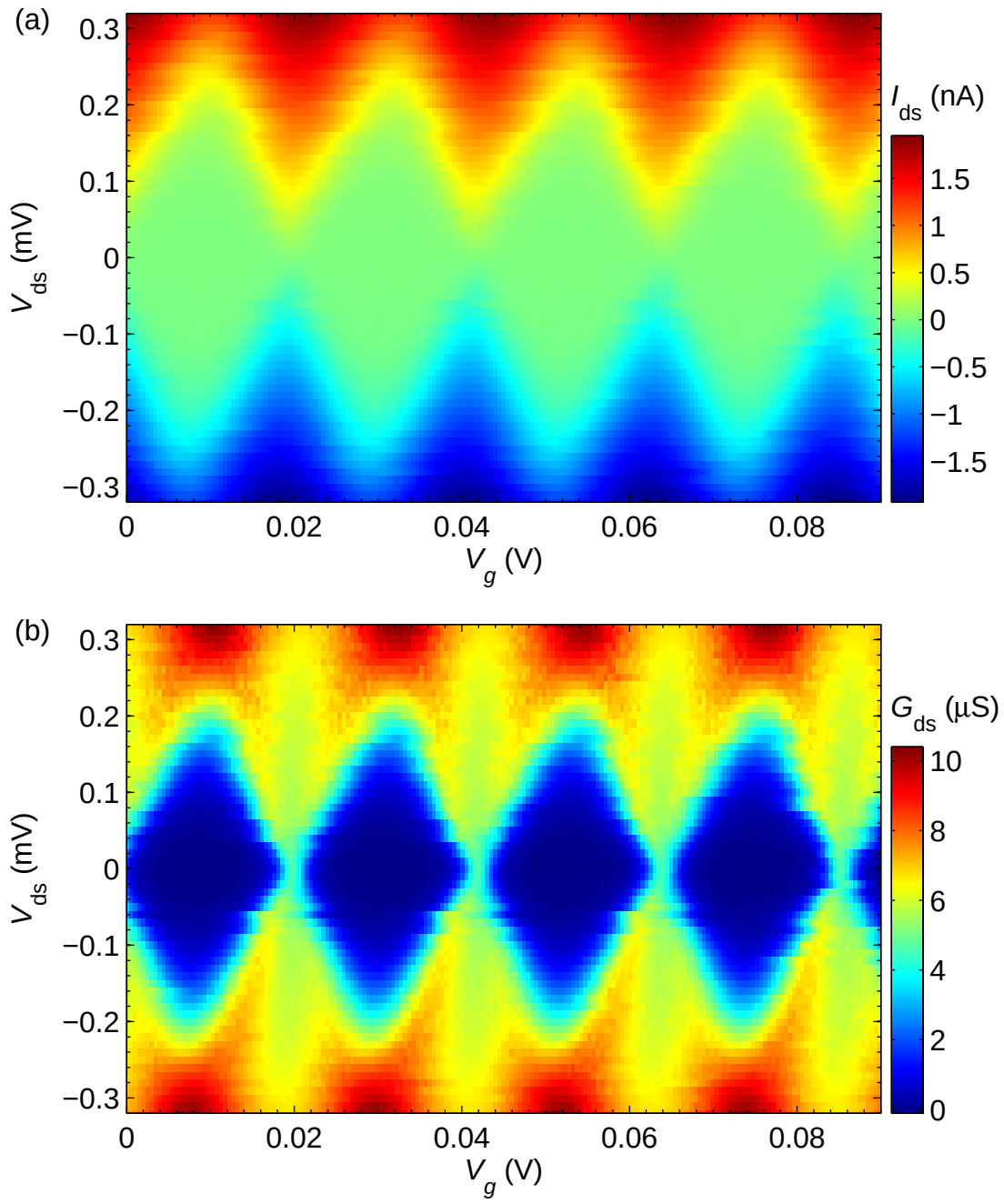


Figure 7.2: Diamond chart of Al SET3 measured at 20 mK. (a) DC current through Al SET3 as a function of V_g and $V_{\rm ds}$. (b) Differential conductance of Al SET3 measured by a lock-in amplifier with an AC excitation voltage of $V_{ac} = 5$ μV at a frequency of $f = 580$ Hz.

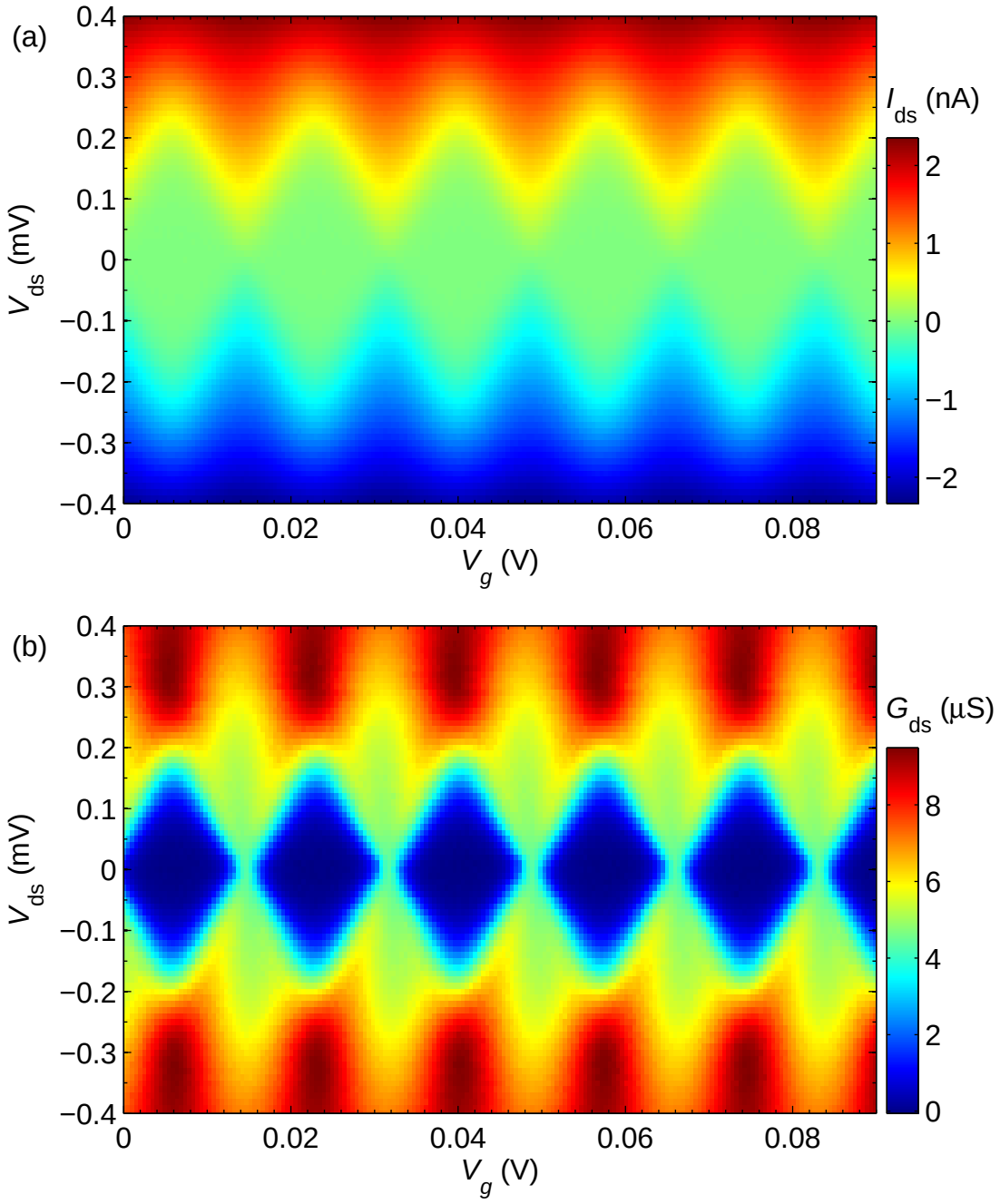


Figure 7.3: Diamond chart of Al SET4 measured at 20 mK. (a) DC current through Al SET4 as a function of V_g and $V_{\rm ds}$. (b) Differential conductance of Al SET4 measured by a lock-in amplifier with an AC excitation voltage of $V_{ac} = 5$ μV at a frequency of $f = 580$ Hz.

the Si SET at $V_g = -0.600$ V for Device3. Figure 7.5 shows the Coulomb blockade oscillations of Si SET4 at $V_g = -0.760$ V. Both samples are stable as evidenced by the excellent overlap between sweeps back and forth. I note that these results mean I am able to observe Coulomb blockade oscillations in all three n-channel devices I fabricated. This suggests that the formation of a Si SET at the Si/SiO_2 interface due to the Al SET is not an accident, but a reliable and repeatable consequence of the device fabrication.

Comparison of Figs. 7.4 and 7.5 reveals that Si SET4 has a much higher threshold than Si SET3 and has much fewer oscillations before the lifting of the Coulomb blockade. Also the oscillations seen in the Si SET4 conductance are less periodic. The variation could be due to a less perfect Si/SiO_2 interface. Since Si SET4 has a non-regular behavior, I will focus on Device3 for the correlation measurements.

Figure 7.6 shows the diamond chart of Si SET3 for the first few peaks. As with Si SET1 discussed in Chap. 6, all the diamond are closed, suggesting the formation of a single island and not multiple islands in series in the channel. The charging energy is a few meV and also strongly depends on bias voltage. As mentioned in Chap. 6, the most likely reason could be the dependence of the tunnel capacitances on bias voltage. However, I do not have a clear explanation at this point why the charging energies are not monotonic.

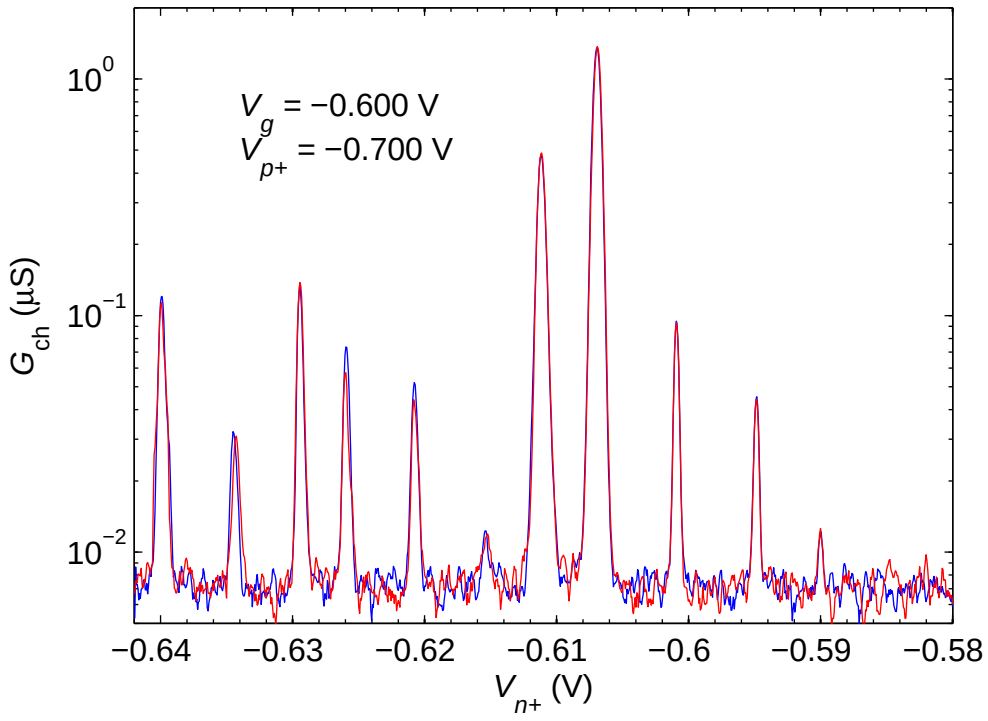


Figure 7.4: Coulomb blockade oscillations in the differential conductance of Si SET3, plotted as a function of the relative bias V_{n+} between the Al SET and the Si SET at $V_g = -0.600$ V and $V_{p+} = -0.700$ V. I used an AC excitation of $V_{ac} = 10$ μV at $f = 47$ Hz. Blue and red curves correspond to sweeps to the left and to the right respectively.

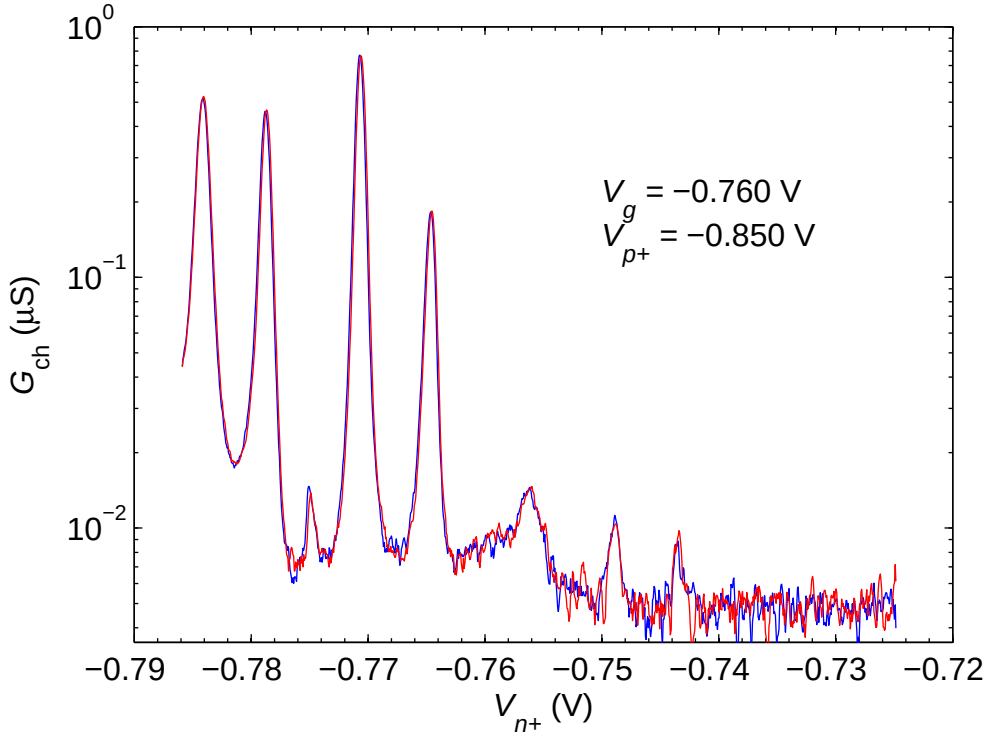


Figure 7.5: Coulomb blockade oscillations in the differential conductance of Si SET4, plotted as a function of the relative bias V_{n+} between the Al SET and the Si SET at $V_g = -0.760$ V and $V_{p+} = -0.850$ V. I used an AC excitation of $V_{ac} = 10$ μV at $f = 47$ Hz. Blue and red curves correspond to sweeps to the left and to the right respectively.

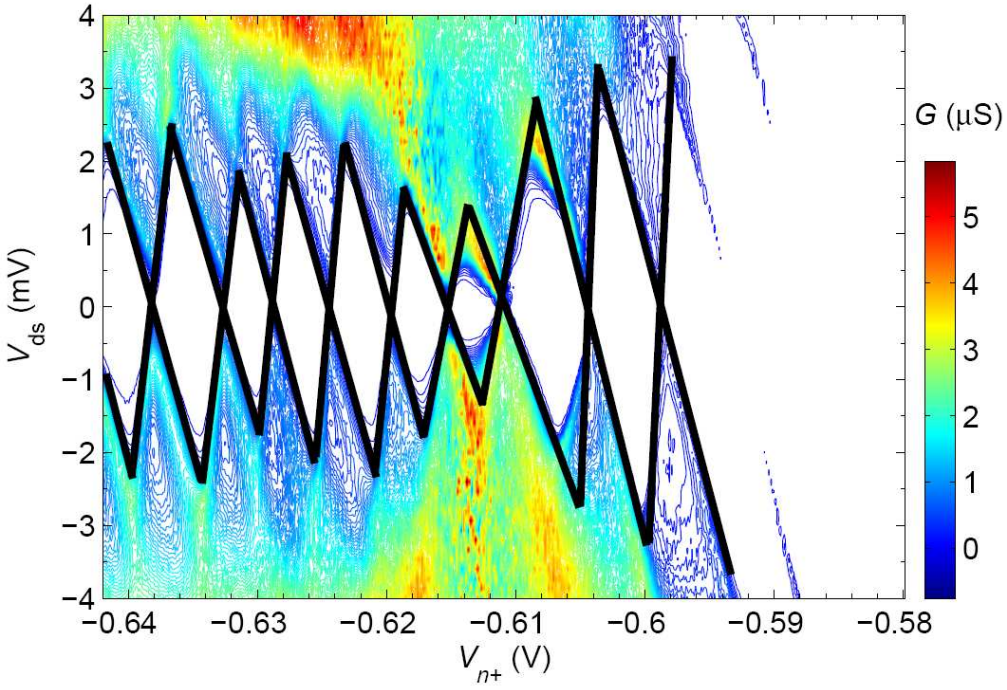


Figure 7.6: Diamond chart of Si SET3. The differential conductance is measured by a lock-in amplifier with an AC excitation voltage of $V_{ac} = 10$ μV at a frequency of $f = 47$ Hz at $V_g = -0.615$ V and $V_{p+} = -0.700$ V. The non-monotonic change in the size of the diamonds with V_{n+} is not understood.

7.3 A single charge defect in Device3

The main experimental goals of this chapter are to confirm the reproducibility of the vertical alignment between the Al and the Si SETs and to use this aligned SET system to study charge defect in a MOS structure. In this section, I discuss my observation of a single charge defect close to both the Al and Si SETs in Device3. If not specified, for the rest of this chapter the Al SET is dc biased at $V_{\rm ds} \cong 100$ μV, and the differential conductance of the Si SET is measured with an ac excitation of $V_{\rm ac} = 10$ μV at $f = 47$ Hz under no dc bias.

Figures 7.7(a) and 7.7(b) show simultaneously measured conductances of the Al SET and the Si SET, respectively, vs V_g and V_{n+}. Clearly the Al and the Si SETs are correlated and the Si SET responds to the Al SET. The discontinuities of the Al SET clearly come from the charging events on the Si SET island. However, the discontinuities of the Si SET are much less obvious, even less obvious than those in Device1 in Chap. 6. The reason is that the charging energy of Al SET3 is so small that the Al SET has almost negligible effect on the Si SET in Device3. The detailed correlation between the two SETs will be discussed in Sec. 7.4.

Figure 7.8 shows the differential conductance of Si SET3 as a function of V_g and V_{n+} at lower V_g than those shown in Fig. 7.7(b). Instead of being continuous lines as in Fig. 7.7(b), the conductance peak traces display a surprising discontinuity (the main splitting is indicated by arrows in Fig. 7.8) apparently caused by some defect charge motion in the system. In order to check if there are any other similar splittings in Si SET3 conductance traces, I sweep V_g in a larger range, below and

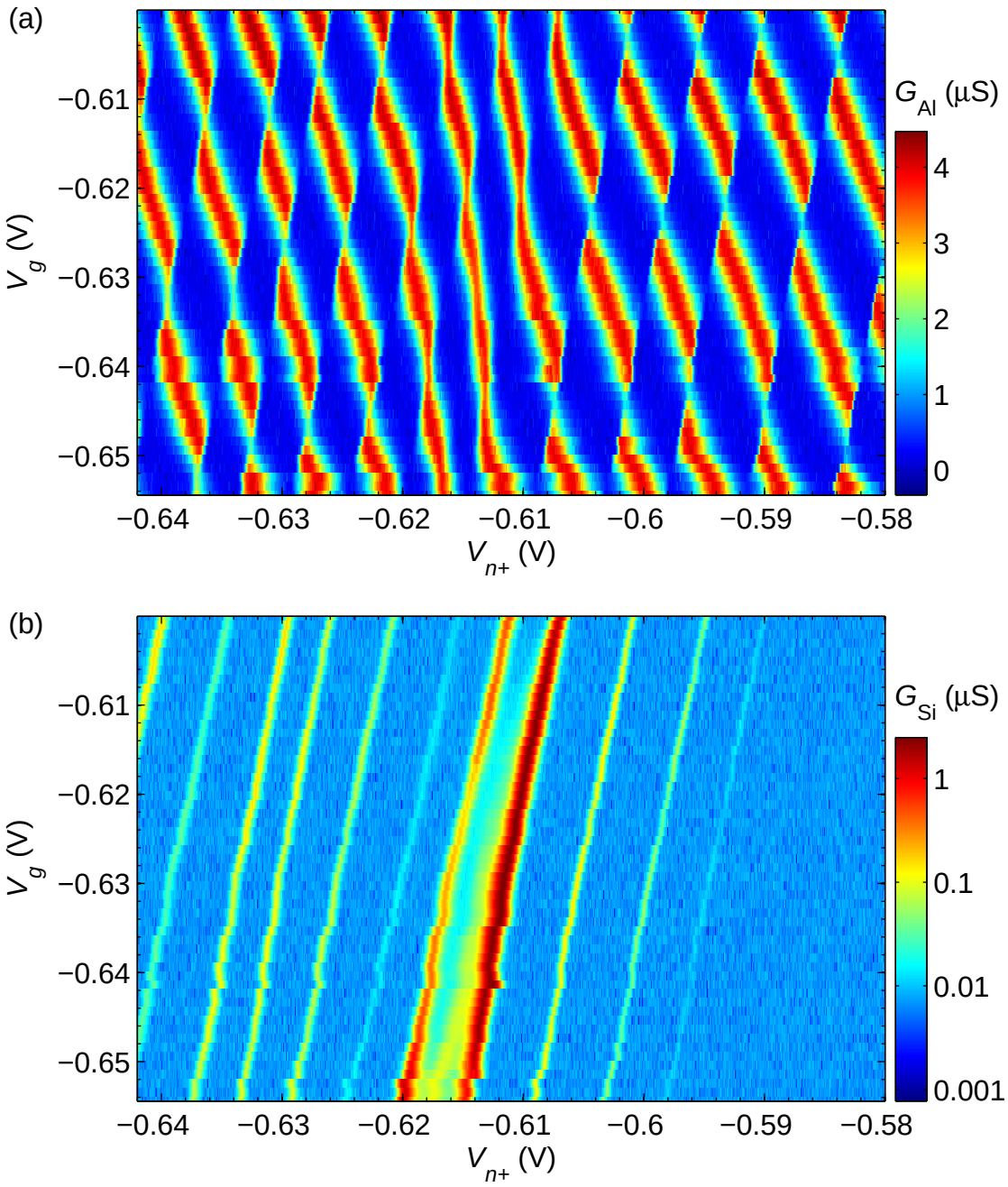


Figure 7.7: Simultaneously measured conductances of both the Al and Si SETs of Device3 vs V_g and V_{n+}. (a) Al SET, dc biased at $V_{\rm ds} \cong 100$ μV. (b) Si SET, ac excitation $V_{\rm ac} = 10$ μV at $f = 47$ Hz.

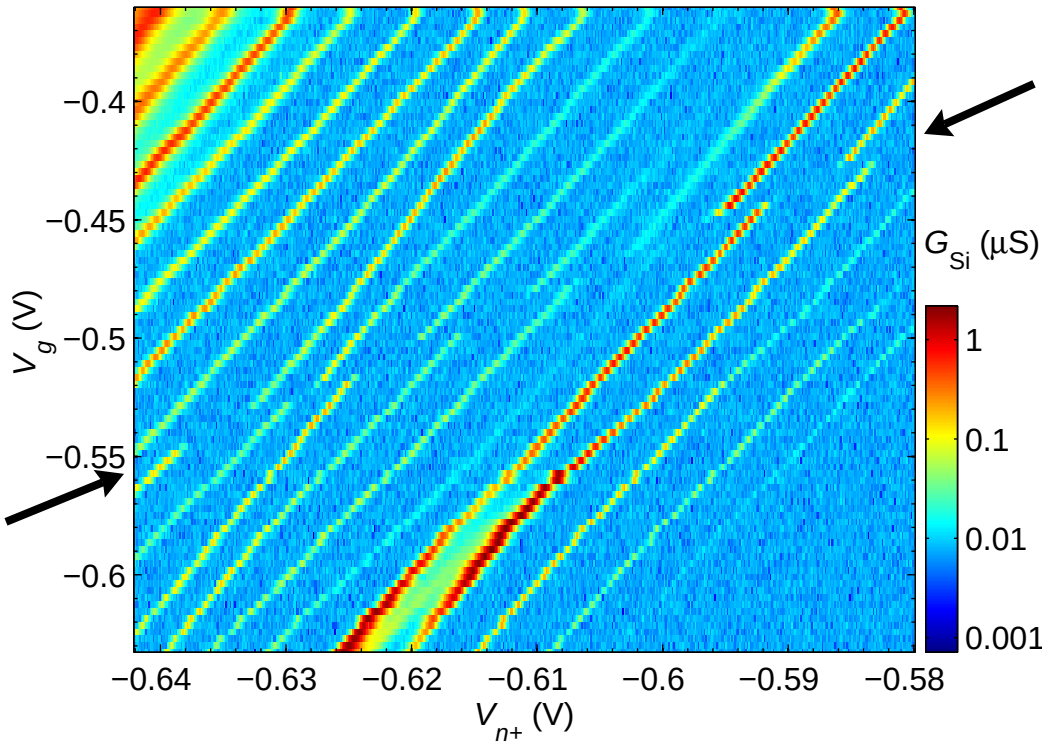


Figure 7.8: Differential conductance of Si SET3 vs V_g and V_{n+}. A single line as indicated by the black arrows shows where the characteristics shift discontinuously.

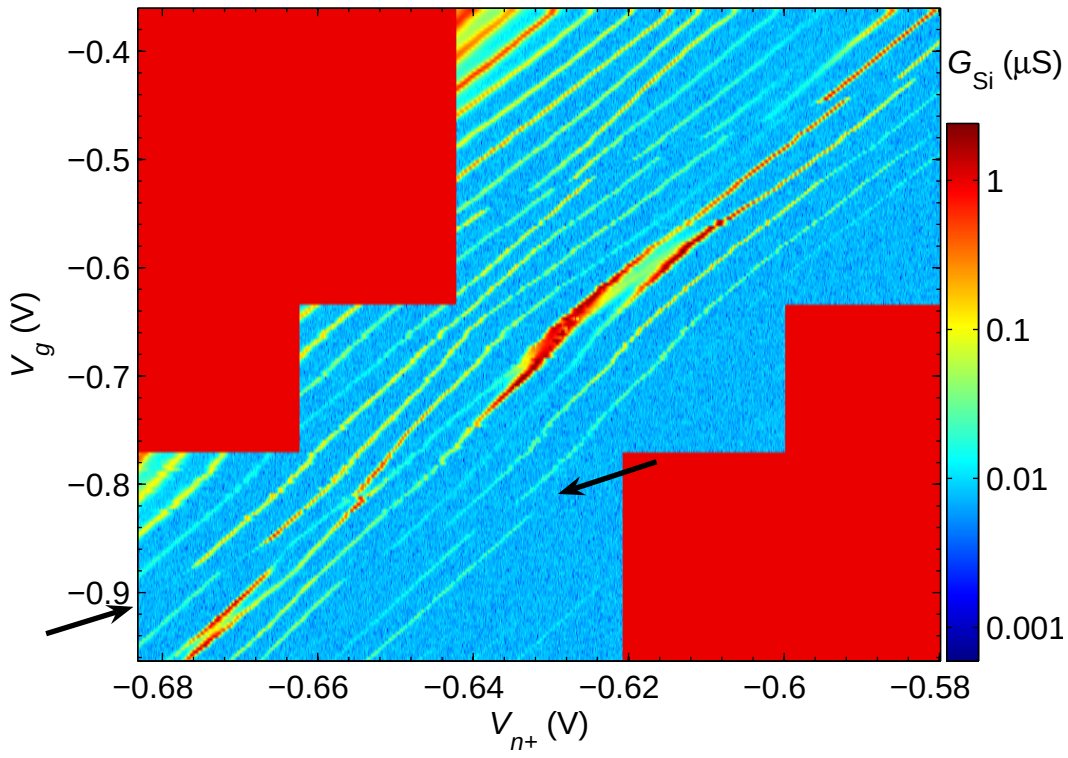


Figure 7.9: Differential conductance of Si SET3 vs V_g and V_{n+} in a larger range than shown in Fig. 7.8 shows a possible second splitting as indicated by the arrows (about 300 mV below the main splitting). The top-left and bottom-right red regions do not correspond to data and should be neglected.

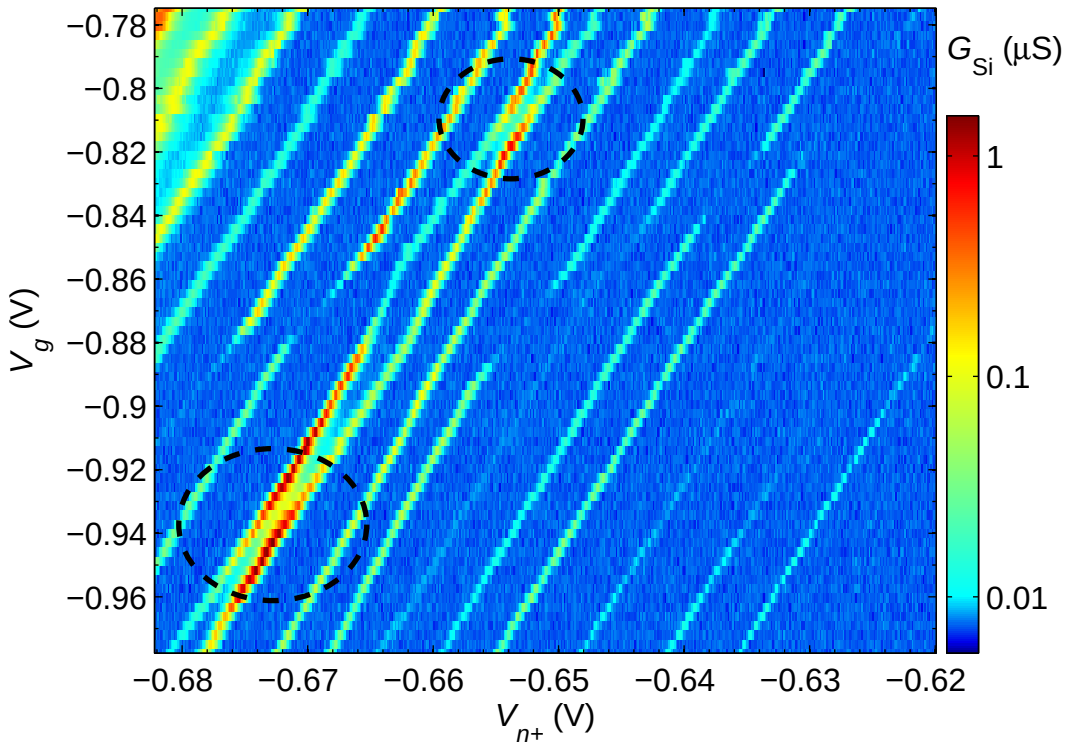


Figure 7.10: Differential conductance of Si SET3 vs V_g and V_{n+} with a five times larger AC excitation voltage ($V_{ac} = 50$ μV). No splitting is evident. Region shown corresponds to the lower part of Fig. 7.9. The two circled parts show anti-crossings of two conductance peak traces.

above the main splitting. Figure 7.9 shows the conductance of Si SET3 over a large range in V_g below the main splitting. Examination of the figure reveals a possible second splitting $\cong$ 300 mV below the main splitting. However, the splitting seems to happen only for some of the conductance peak traces. To double check if it is a real splitting, I resweep the bottom left corner of Fig. 7.9 with a much larger AC excitation voltage, $V_{ac} = 50\ \mu$V (vs $V_{ac} = 10\ \mu$V in all the other figures). Figure 7.10 shows the resulting data. This figure is much less clearly showing a splitting, and in fact I do not think that is a real splitting through all the conductance peak traces. Obviously, at least the middle three traces display no splitting at all. What seems to be happening is that some of the conductance peaks just become too weak to see. One also sees in Fig. 7.10 anti-crossings of two conductance peak traces at $V_{n+} \cong -0.672$ V, $V_g \cong -0.930$ V and $V_{n+} \cong -0.652$ V, $V_g \cong -0.800$ V (the two circled parts).

Figure 7.11 shows conductance data for Si SET3 above the main splitting in Fig. 7.8. There is no obvious splitting in the conductance peak traces, however, there appears to be a second possible splitting $\cong$ 200 mV above the main splitting, but with a much smaller amplitude. I do not sweep V_g to even lower voltages because of the worry that a large positive voltage on the side gate relative to the Si channel may attract channel electrons to flow to the region underneath the side gate. These electrons would be very hard to get rid of and would complicate the system.

Figure 7.12 shows conductance data for the device after it was warmed to room temperature and cooled back down to the base temperature of our dilution refrigerator. This data is interesting from the following three perspectives. First, the main

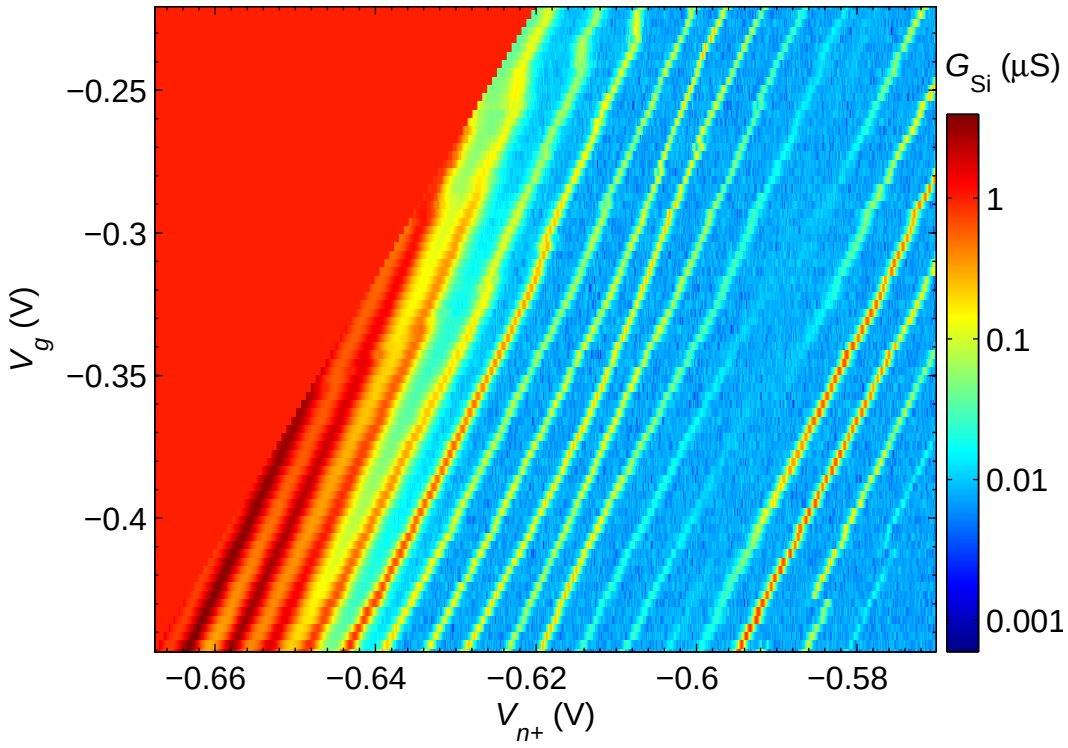


Figure 7.11: Differential conductance of Si SET3 vs V_g and V_{n+}. No other splitting is seen above the main splitting. The left red triangular region does not correspond to data and should be neglected.

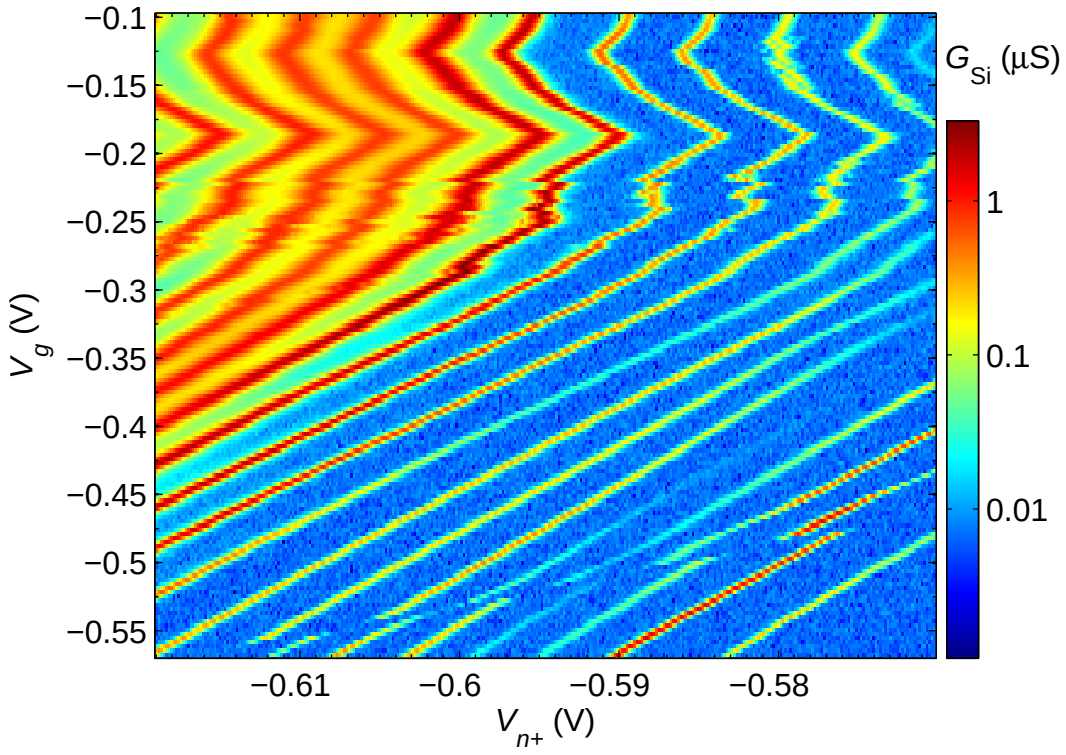


Figure 7.12: Differential conductance of Si SET3 vs V_g and V_{n+} after thermal cycling to room temperature. The main splitting survived. Note that for $V_g > -0.2$V, the Si SET conductance peak traces oscillate rapidly with V_g and then the slope changes sign. This behavior is probably due to channel electrons flowing to the region underneath the side gate when $(V_g - V_{n+})$ is large enough.

splitting in the conductance traces can clearly still be seen. It is not too surprising to have the position of the splitting in V_g-V_{n+} space changed after thermal cycles to room temperature, because the background charge in the MOS system could change, for example, the alkali metal ions in SiO_2 are mobile at room temperature.[53] However, the splitting feature clearly survives thermal cycling to room temperature. Second, the possible second splitting disappears; the much smaller splitting in Fig. 7.11 is not reproducible.

I note that Fig. 7.12 shows another interesting feature. When V_g is more than $\cong$ 300 mV above the main splitting line (measured at $V_{n+} = -0.58$ V), the behavior of Si SET3 conductance peaks changes dramatically. They first oscillate very rapidly with V_g and then the slope changes sign. This behavior is likely because the channel electrons are attracted to the region underneath the side gate when $(V_g - V_{n+})$ is so large.

Based on Figs. 7.9 and 7.11, with reasonable confidence I can claim that no second splitting in Si SET3 conductance peak traces is observed. This means that small grain theory (small Al grains can typically be charged up with multiple electrons) and double donors can be ruled out with reasonable confidence. This suggests the idea that a single charge defect is being observed. This still leaves many possibility. The possible sources and locations of the single charge defect will be discussed in Sec. 7.5.2.

7.4 Confirmation of the vertical alignment and the validity of the electrostatic model in Chapter 6

Before I focus on the main splitting and the study of the characteristics of the single charge defect, I first need to confirm the vertical alignment of the Al and Si SET islands and the validity of the electrostatic model discussed in Chap. 6. I will also extract the capacitances associated with the Al and Si SETs, and I will need these when I quantitatively analyze the single charge defect in Sec. 7.6.

Figures 7.13(a) and 7.13(b) show simultaneously measured conductances of the Al SET and the Si SET, respectively, vs V_g and V_{n+} around the main splitting. The data in Fig. 7.13 is taken by sweeping V_g at different fixed V_{n+}. I note that only the diagonal portions in Fig. 7.13 correspond to data. The upper and lower triangular regions do not correspond to data and should be neglected. Same restrictions apply to Figs. 7.16, 7.17, and 7.18 in Sec. 7.5.1.

Along the main splitting line, the defect charge can change its charge state from one to the other, and vice versa. However, in the regions above and below the main splitting line, the charge defect appears to be in a well-defined stable state. If the charge defect is assumed to be very small, it can be treated as a fixed background charge and should not affect the electrostatic model discussed in Chap. 6. Therefore, I will focus on the regions above and below the main splitting line to confirm the validity of the electrostatic model and the vertical alignment of the two SETs.

As described in Chap. 6, I can again do a Gaussian fit to each conductance peak of both the Al and Si SETs. The resulting peak centroids for both SETs are plotted

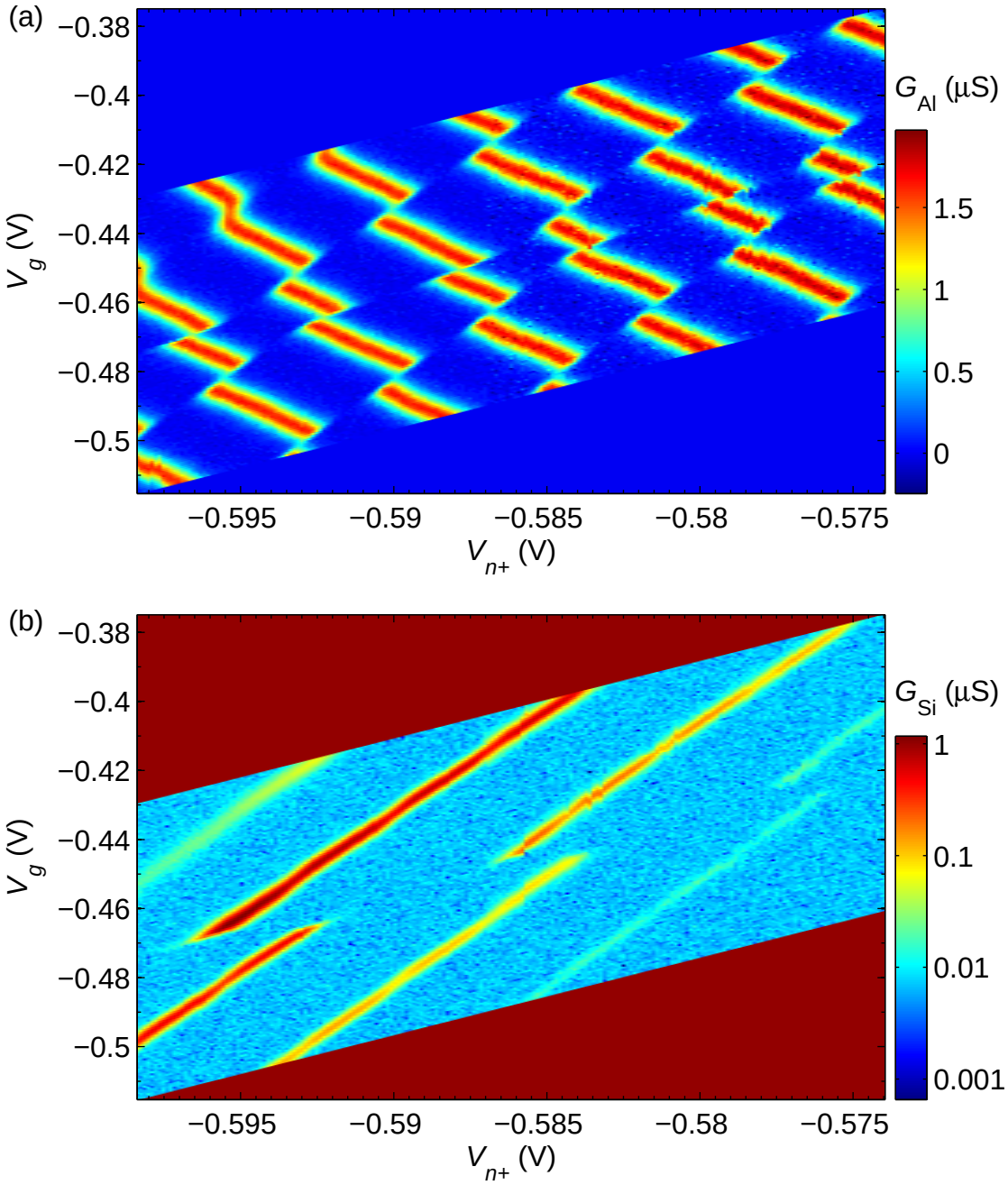


Figure 7.13: Simultaneously measured conductances of both SETs of Device3 around the main splitting. (a) and (b) are conductances of the Al SET and the Si SET, respectively, vs V_g and V_{n+}.

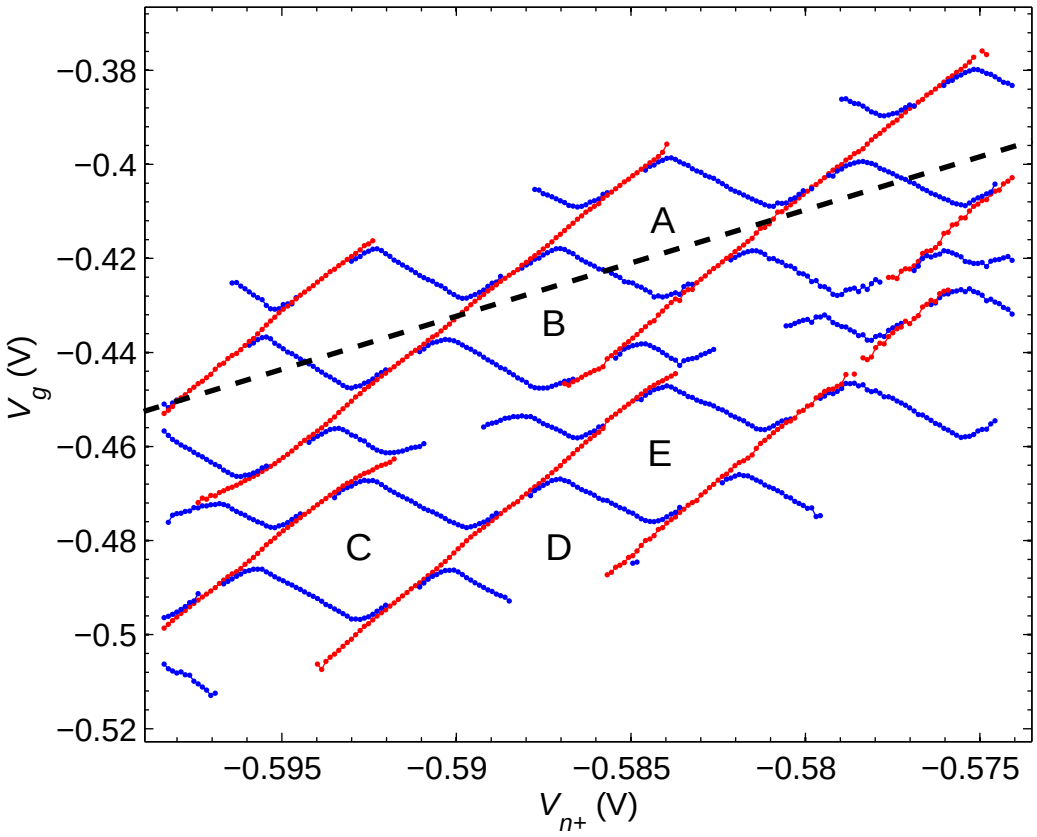


Figure 7.14: Fitted conductance maxima of both the Al and Si SETs in Fig. 7.13 vs V_g and V_{n+}. Blue and red dots are the peaks of the Gaussian fits to the data in Figs. 7.13(a) and 7.13(b), respectively. The regions labeled A, B, C, D, and E are the five parallelograms whose parameters are presented in Table 7.1. The dotted black line is the real x-axis of Fig. 7.15, along which the charging energy of Si SET3 is measured.

in Fig. 7.14. The correlations can be clearly seen: most discontinuities of the Al SET conductance peak traces come from the single-electron charging events on the Si SET island; the others are associated with the main splitting. However, the single-electron charging events on the Al SET island have almost negligible effect on the Si SET conductance, similar to the behavior seen in Fig. 7.7(b). Close examination reveals that some step-like features can be seen in the Si SET conductance peak traces, but the magnitude is very small (only about 3 – 4%). The reason why the steps are so small will be explained shortly.

I can use the same electrostatic model to calculate the capacitances C_2, C_c, C_3, C_4, C_{g_Al}, and C_{g_Si}, which are defined in Fig. 6.9. However, due to the fact that the phase shifts of Si SET3 are so small, the slope of the boundary between $(N_{\mathrm{Al}}, N_{\mathrm{Si}}+1)$ and $(N_{\mathrm{Al}}, N_{\mathrm{Si}})$ is almost the same as that between $(N_{\mathrm{Al}}-1, N_{\mathrm{Si}}+1)$ and $(N_{\mathrm{Al}}, N_{\mathrm{Si}})$ in Fig. 6.9(b). Therefore, the linear fit for those two edges will have very big uncertainties. To overcome this problem, instead of fitting the data with hexagons, I fit the data with a parallelogram. In another words, I treat the two boundaries in Fig. 6.9(b) between $(N_{\mathrm{Al}}, N_{\mathrm{Si}}+1)$ and $(N_{\mathrm{Al}}, N_{\mathrm{Si}})$ and between $(N_{\mathrm{Al}}-1, N_{\mathrm{Si}}+1)$ and $(N_{\mathrm{Al}}, N_{\mathrm{Si}})$ as one. Another simplification I make is to neglect C_4, which is the cross capacitance between the Al SET leads and the Si SET island. This simplification can be justified by the negligible values of C_4's in Device1 (see Table 6.1 in Chap. 6). I have already got the total tunnel capacitance of Al SET3 $C_1 = C_{11} + C_{12} = 711\ aF$, as I discussed in Sec. 7.2 when I characterized the Al SETs. In order to extract the remaining five unknown parameters: C_2, C_c, C_3, C_{g_Al}, C_{g_Si}, I need five independent equations. There are already four such equations—

two slopes S_1 & S_3 and two separations Δ_1 & Δ_3 from the parallelogram [defined in Fig. 6.9(b)]:

$$S_1 = (C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} - C_{\Sigma\_\mathrm{Al}}C_2 - C_cC_3 - C_c^2)/(C_{\Sigma\_\mathrm{Al}}C_{g\_\mathrm{Si}} + C_cC_{g\_\mathrm{Al}}) \tag{7.1}$$

$$S_3 = -(C_{\Sigma\_\mathrm{Si}}C_3 + C_cC_2)/(C_{\Sigma\_\mathrm{Si}}C_{g\_\mathrm{Al}} + C_cC_{g\_\mathrm{Si}}) \tag{7.2}$$

$$\Delta_1 = eC_{\Sigma\_\mathrm{Al}}/(C_{\Sigma\_\mathrm{Al}}C_{g\_\mathrm{Si}} + C_cC_{g\_\mathrm{Al}}) \tag{7.3}$$

$$\Delta_3 = eC_{\Sigma\_\mathrm{Si}}/(C_{\Sigma\_\mathrm{Si}}C_{g\_\mathrm{Al}} + C_cC_{g\_\mathrm{Si}}) \tag{7.4}$$

The fifth equation is the phase shift of the Al SET:

$$\Phi_{\mathrm{Al}} = C_c/C_{\Sigma\_\mathrm{Si}} \tag{7.5}$$

Here, I will only examine five parallelograms: A, B, C, D, and E, as labeled in Fig. 7.14. The results are presented in Table. 7.1. The capacitances of the five parallelograms are very close to each other, indicating that the parallelograms are almost identical to each other. This confirms the assumption that the charge defect is small and plays a negligible role once it is fixed in a stable state. The average C_c is about 26 aF. Based on a parallel-plate capacitor model with 20 nm thick SiO_2, the area of the overlap is 150 nm $\times$ 100 nm which agrees well with the dimension of the Al SET3 island in the SEM image Fig. 7.1. This confirms the vertical alignment of the two SET islands and justifies the assumption that the cross capacitance between the Al SET leads and the Si SET island C_4 can be neglected.

In order to get the charging energy of Si SET3 and to check the above results, I measure the diamond chart of Si SET3 along the dotted black line in Fig. 7.14. The results are shown in Fig. 7.15. Diamond b in Fig. 7.15 corresponds to parallelograms

Table 7.1: Capacitances (in aF) of the five parallelograms labeled in Fig. 7.14 based on the electrostatic model described in Chap. 6.

parallelogram	C_c	C_2	C_3	C_{g_Al}	C_{g_Si}	C_{Σ_Al}	C_{Σ_Si}
A	24.9	46	4.1	3.65	4.60	744	76
B	24.6	48	4.4	3.50	4.40	744	77
C	24.8	50	4.5	3.63	4.58	744	79
D	27.3	54	2.2	3.49	4.82	744	86
E	27.9	48	1.8	3.54	4.80	744	81

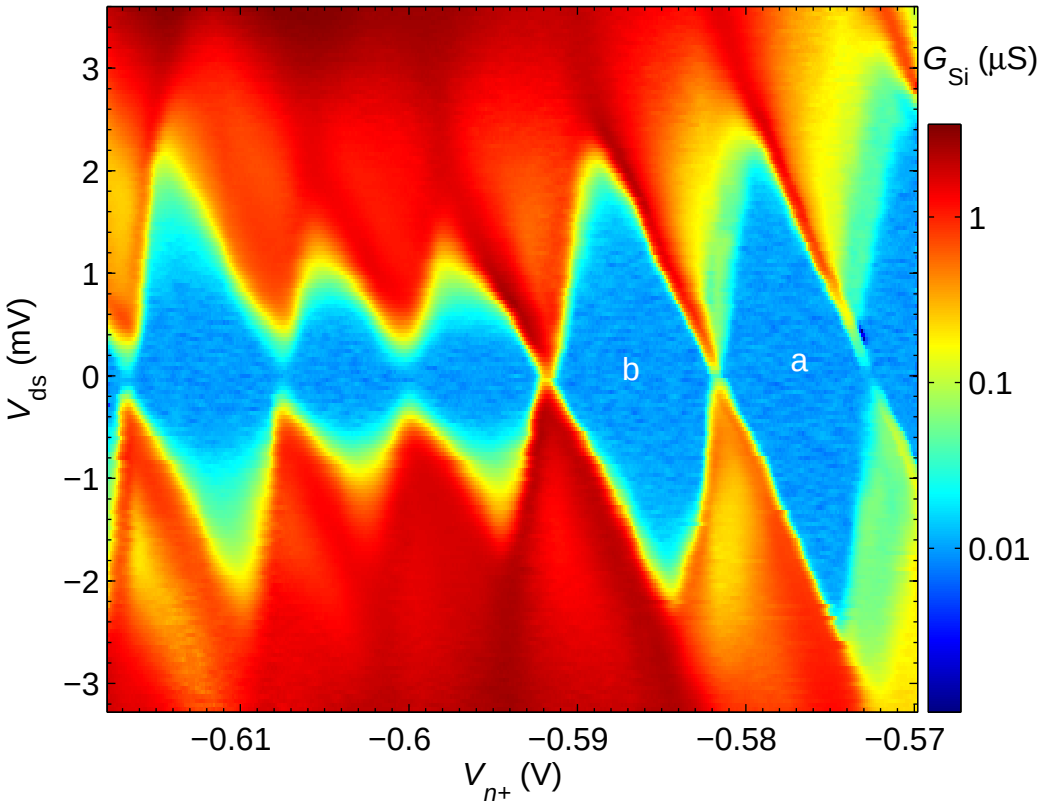


Figure 7.15: Diamond chart of Si SET3 along a line which is parallel to the main splitting line and is indicated in Fig. 7.14.

A and B in Fig. 7.14. Both diamonds a and b have about the same charging energy, $2E_c \cong 2$ mV, corresponding to $C_{\Sigma\_Si} \cong 80$ aF. This number agrees well with the results in Table. 7.1: $C_{\Sigma\_Si} = C_2 + C_c + C_{g\_Si} = 76$ aF, 77 aF, 79 aF, 86 aF, and 81 aF for parallelograms A, B, C, D, and E respectively.

As with Si SET1 discussed in Chap. 6, for all the parallelograms in Table 7.1, $C_c/C_{\Sigma\_Al} \cong 3$ – 4% explains the small magnitude of the discontinuities of the Si SET conductance peak traces in Fig. 7.14, while $C_c/C_{\Sigma\_Si} \cong 32$ – 34% indicates that the Si SET is strongly coupled to the Al SET.

In conclusion, in Device3 I confirmed that the device follows the electrostatic model described in Chap. 6 and that the Al and Si SETs are vertically aligned.

7.5 Characteristics of the single charge defect

7.5.1 Some basic properties of the single charge defect in Device3

Linearity of the main splitting line

Before examining the correlation between the defect and the SETs, I sweep V_g and V_{n+} over a large range to see how the discontinuity in conductance depends on the applied voltage. For example, does the discontinuity merge with the Si channel and disappear as the channel width increases with higher carrier densities? To get a clear picture of how the SET conductances change, many data points are necessary, so intervals of V_g and V_{n+} during sweeps have to be chosen as small as reasonable. However, there is a limited time available for me to take data continuously without

interruption. The main limitation is that I have to transfer liquid helium about every day and half to keep the dilution fridge working properly; during these times mechanical vibrations or thermal gradients in the wire can cause offsets in the data. Therefore, there is a trade-off between sweeping V_g and V_{n+} as finely as possible and finishing the sweep within the allowed time. Figures 7.16, 7.17, and 7.18 show the resulting data over a large range. In the above figures, each pair of Al and Si conductances are taken without any interruption after a single transfer of liquid helium. Enough overlap in voltage space between consecutive sweeps are made so offsets during helium transfer can be corrected.

In Fig. 7.16, when V_{n+} is less negative, the discontinuities in the Al SET conductance remain clear, while the conductance of the Si SET becomes very small because the carrier density in the channel becomes too low. In Fig. 7.18(f), the oscillations of the Si SET conductance are completely washed out when Coulomb blockade in the Si channel is lifted, while the Al SET signal remains robust. From these results, I decide to use the Al SET signal to extract the positions where the defect changes its charge state in V_g and V_{n+} space. Figure 7.19 shows the measured value of V_g as a function of V_{n+} for which the defect charge state changes. The positions are quite linear in V_g and V_{n+} space, a point to which I will come back later.

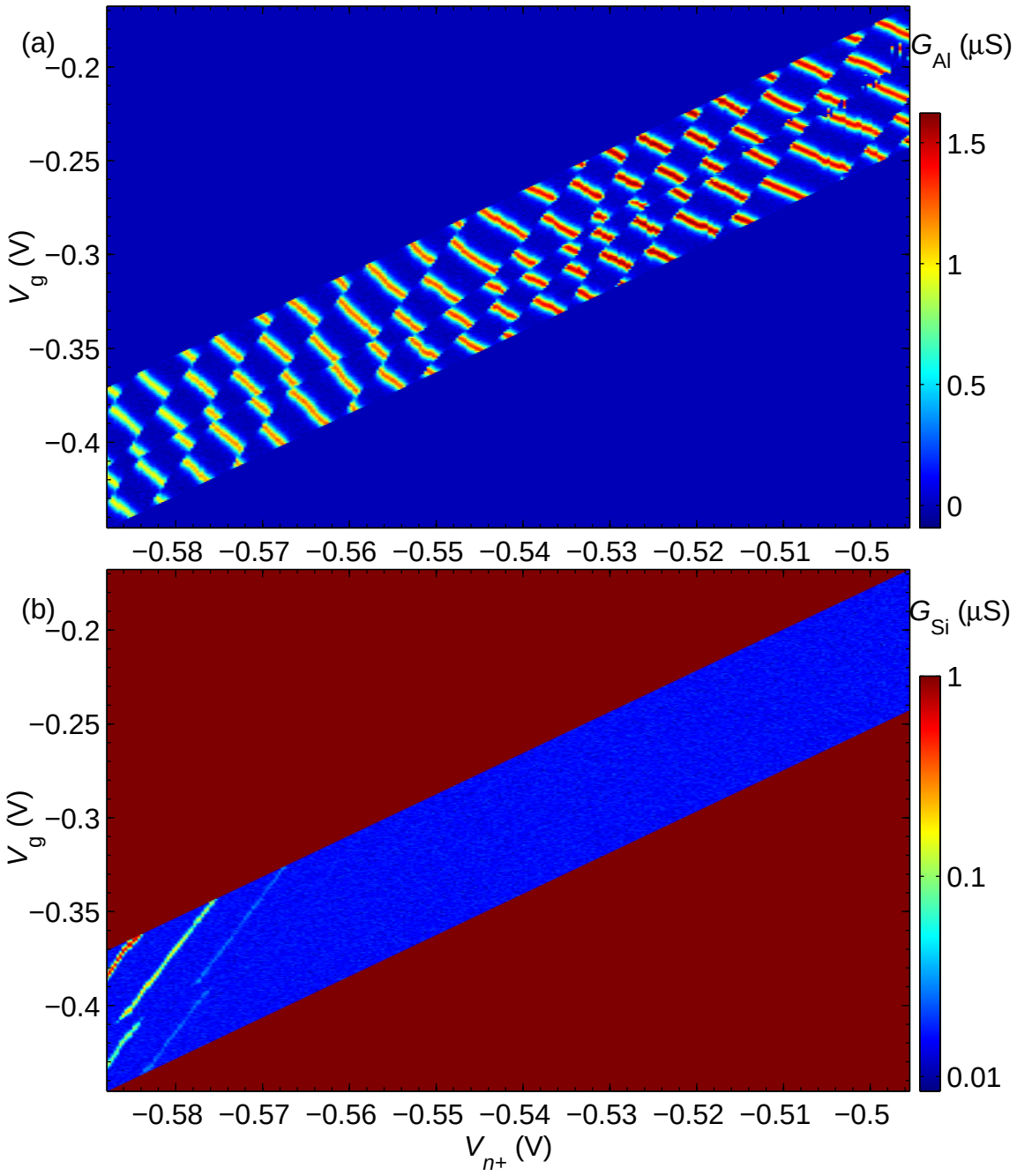


Figure 7.16: Simultaneously measured conductances of both SETs of Device3 around the main splitting. (a) and (b) are conductances of the Al SET and the Si SET, respectively, vs V_g and V_{n+}. No measurable Si SET conductances was found when $V_{n+} > -0.57$V.

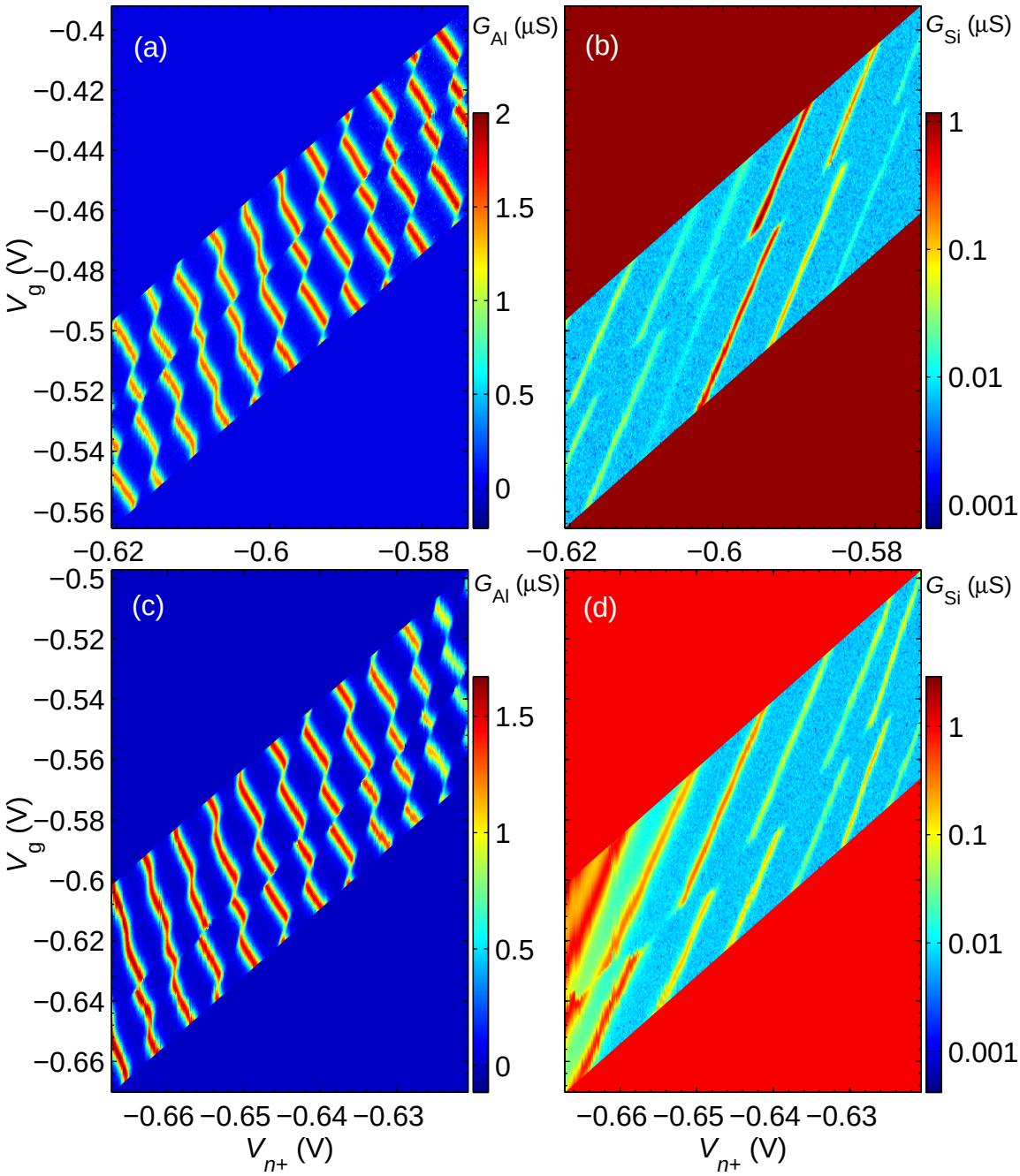


Figure 7.17: Simultaneously measured conductances of both SETs of Device3 around the main splitting. (a) and (c) Conductances of the Al SET, plotted vs V_g and V_{n+}. (b) and (d) Conductances of the Si SET, plotted vs V_g and V_{n+}.

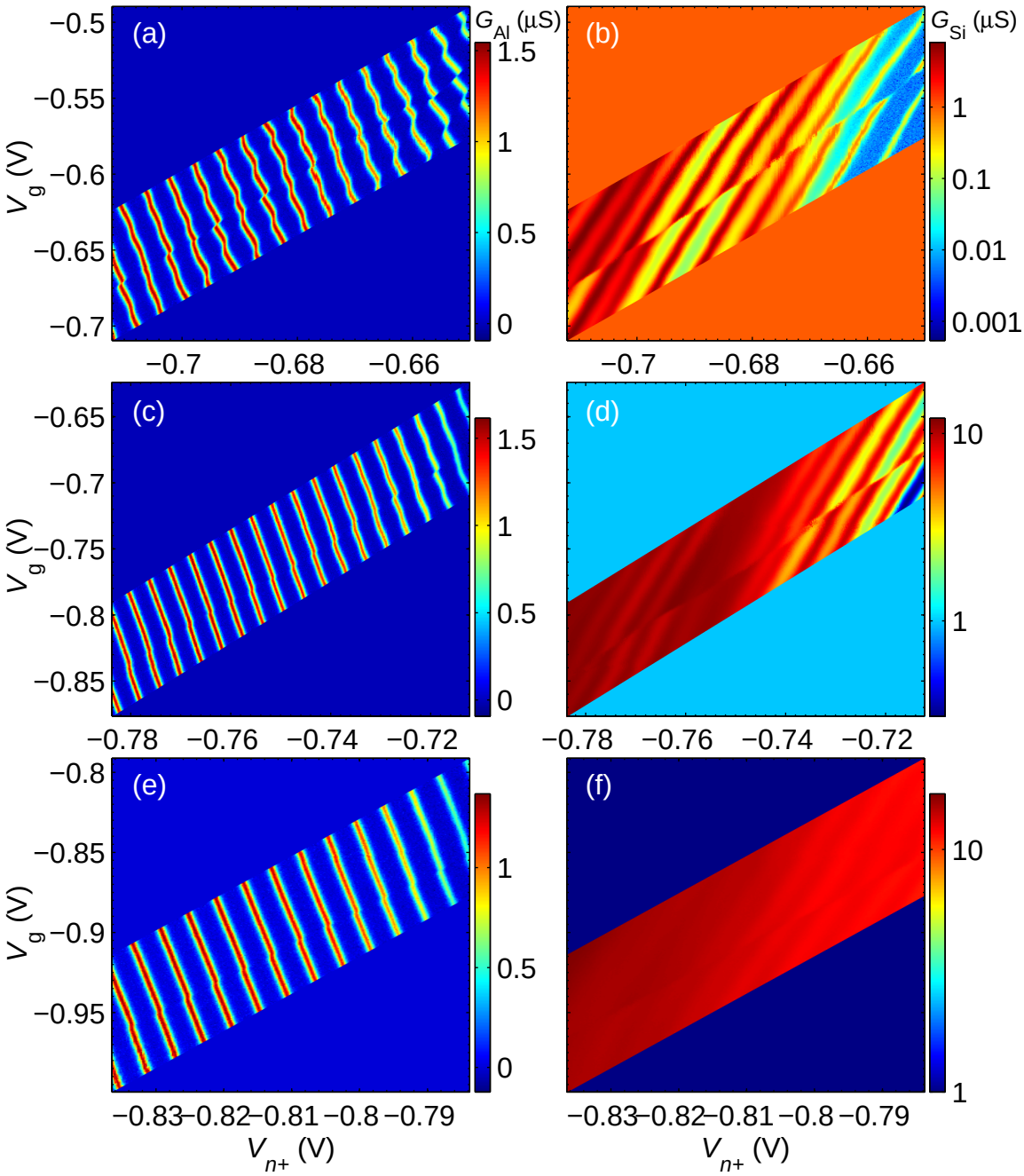


Figure 7.18: Simultaneously measured conductances of both SETs of Device3 around the main splitting. (a), (c), and (e) Conductances of the Al SET, plotted vs V_g and V_{n+}. (b), (d), and (f) Conductances of the Si SET, plotted vs V_g and V_{n+}.

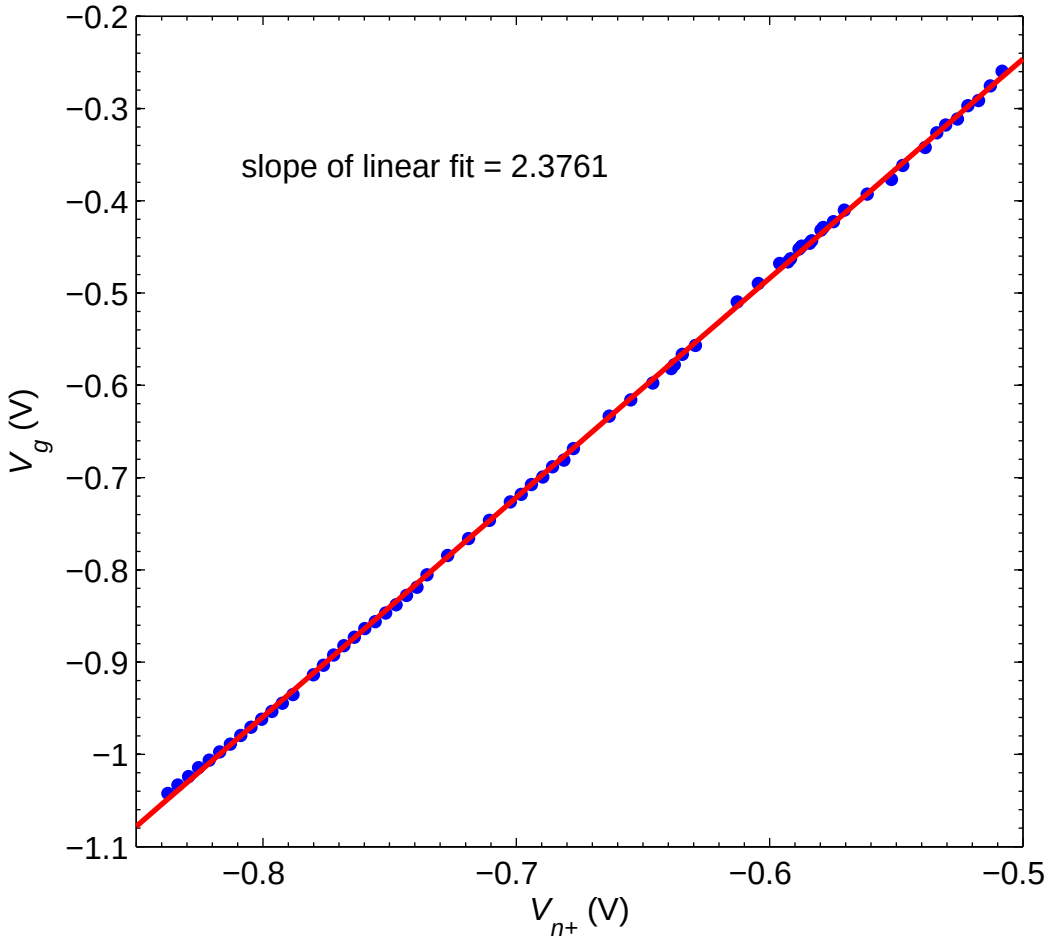


Figure 7.19: Positions where the defect changes its charge states in V_g and V_{n+} space extracted from the Al SET signals in Figs. 7.16, 7.17, and 7.18. The red line is a linear fit with a slope = 2.3761.

Coupling strengths to both SETs

I already mentioned in Sec. 7.4 that some discontinuities in the Al SET conductance peak traces are from the single charge defect when its charge state changes along a "virtually" straight line in the V_g–V_{n+} space. I use the edges of the Al SET3 conductance peak traces in Fig. 7.13(a) to get the straight lines (green lines in Fig. 7.20). In Fig. 7.20, I add these straight lines to the conductance peaks shown in Fig. 7.14. The correspondence of the discontinuities is obvious: both Al and Si SET conductance traces have significant shifts when they meet the green lines (where the defect changes its charge state).

First, I want to determine the signal that is detected by each SET when the defect changes its charge state. This signal is just the phase shift of each SET conductance peak trace. Based on the magnitude of the Si SET3 conductances in Fig. 7.13(b), I can tell how the Si SET conductance peak traces shift: if one follows one of the Si SET3 conductance peak trace from below the main splitting to above, the conductance peak will shift to the left.

Figure 7.21 summarizes how I calculate the phase shift of each SET when it meets the green lines. In this case, $\Phi_{\mathrm{Al}} = \Delta_1/\Delta_2 \cong 0.22\ e$, and $\Phi_{\mathrm{Si}} = \Delta_3/\Delta_4 \cong 0.43\ e$. The easiest way to tell how the Al SET conductance peak trace shifts is as follows. Since $\Phi_{\mathrm{Si}} \cong 0.43\ e$, the Al SET has to shift as depicted in Fig. 7.21. Otherwise, $\Phi_{\mathrm{Al}} = 1 - \Delta_1/\Delta_2 \cong 0.78\ e$ will give $\Phi_{\mathrm{Al}} + \Phi_{\mathrm{Si}} > 1$, which is certainly not true if I assume the defect changes its charge state by only one electron. Explicitly, if one follows one of the Al SET conductance peak trace from below to above the

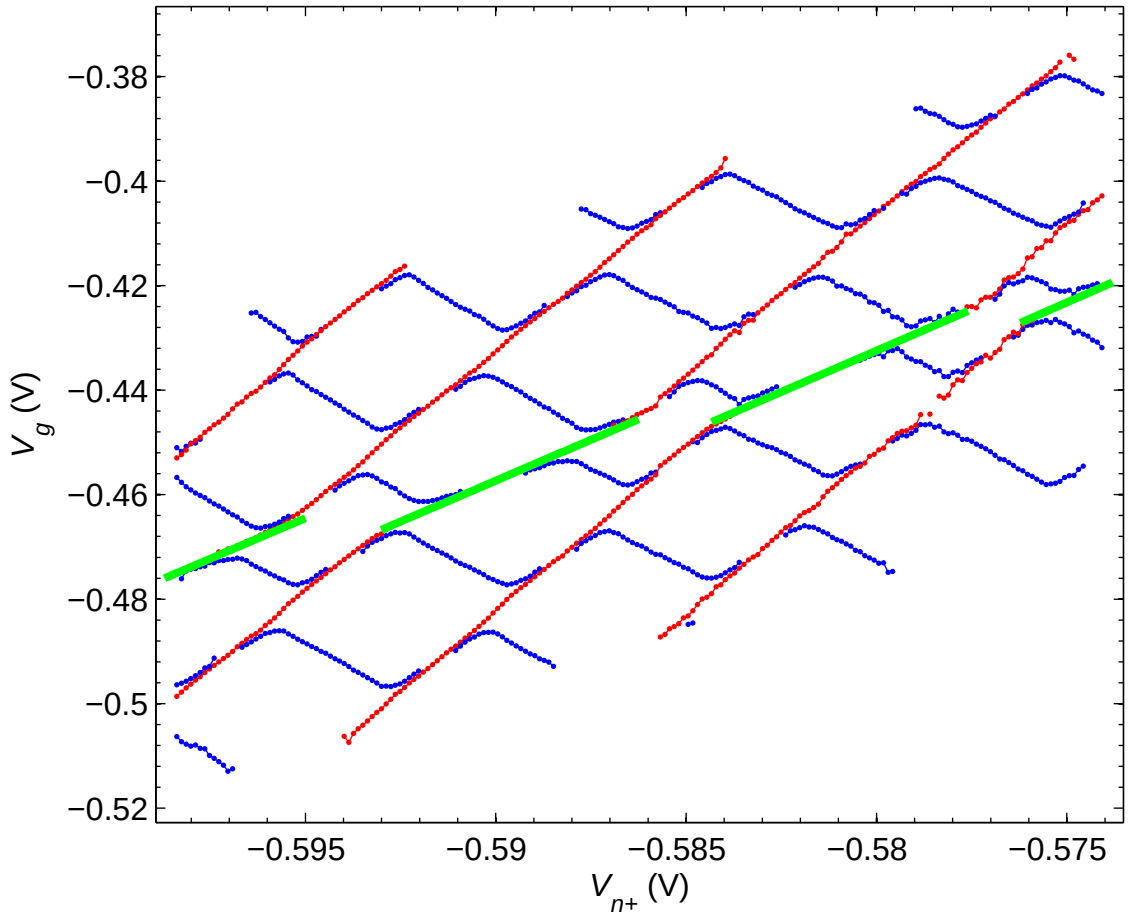


Figure 7.20: Same fitted data as in Fig. 7.14. Green lines define boundaries where the defect charge changes its charge state based on the edges of the Al SET conductance peak traces in Fig. 7.13(a).

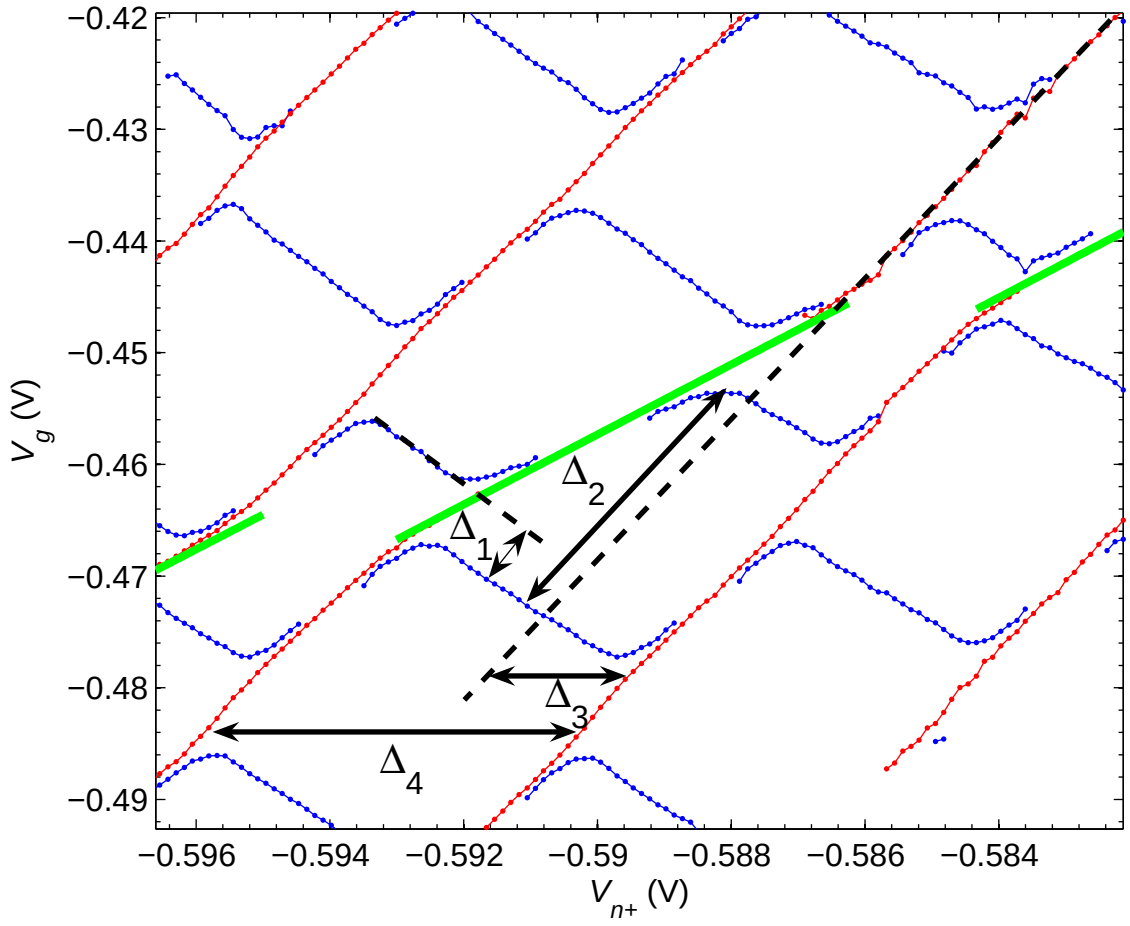


Figure 7.21: Calculation of charge signal measured by the Al and Si SETs when the defect charge changes its charge state. This figure is a detailed view of Fig. 7.20. The signal detected by each SET is just the phase shift Φ of the conductance peak trace. For the Al SET, $\Phi_{\mathrm{Al}} = \Delta_1/\Delta_2$; for the Si SET, $\Phi_{\mathrm{Si}} = \Delta_3/\Delta_4$.

main splitting, the conductance trace will shift to the right. I will come back to this point later.

7.5.2 Possible sources and locations of the single charge defect

First, Fig. 7.20 reveals some information about the location of the defect. For example, the slope dV_g/dV_{n+} of the green lines is bigger than 1, but smaller than that of the red dotted lines (the Si SET conductance peak traces). This implies that the side gate has a more significant effect on the defect than on the Si SET island. Therefore the defect should be between the Si channel and the side gate. Note: I have assumed that along the green lines in Fig. 7.20, the slope dV_g/dV_{n+} is determined by a constant defect potential E_{D}.

Second, I can rule out that the defect and the defect charge motion are on the sample surface, because $\Phi_{\mathrm{Si}} > \Phi_{\mathrm{Al}}$, meaning the defect is closer to the Si SET. Also if the defect can tunnel-couple to the Al SET, it is expected to have $dV_g/dV_{n+} < 0$, which also disagrees with the data, assuming that the resonant tunneling happens when the potential of the defect E_{D} equals to the Fermi level of the Al electrodes E_{Al}.

Third, the defect could not be in the SiO_2 because both Φ_{Al} and Φ_{Si} are significant fractions of one electron. To get such big signals, let's consider the most effective way for the defect motion to couple to each SET: the defect charge moves between the two SET islands. Based on a parallel plate model and the image charge method ($Q_i = -x \cdot Q/d$, d is the distance between the two plates, x is distance from

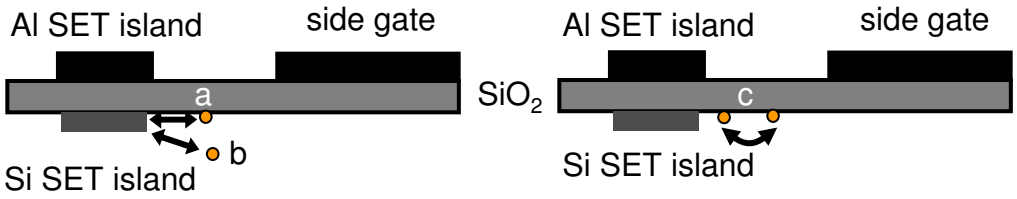


Figure 7.22: Possible defect locations (schematic cross-section view of the Al SET coupled to the Si SET). (a) A single charge trap at the Si/SiO_2 interface, tunnel-coupled to the Si SET. (b) A single donor in the Si substrate, tunnel-coupled to the Si SET. (c) A TLF between two interface states or between two donor sites in the Si substrate.

the other plate, Q is the point charge),[100] the defect charge has to move up to $\cong$ 9 nm (0.43×20 nm) in the oxide. I think this is implausibly far.

The remaining possible locations and charge motions of the defect (see Fig. 7.22) could be: a) a single charge trap at the Si/SiO_2 interface, b) a single charge defect (most likely a single donor) in the Si substrate, or c) a two-level fluctuator (TLF) between two interface states or between two donor sites in the Si substrate. For cases a) and b), the single charge charge defect has to be tunnel-coupled to the Si SET (one electron can be exchanged between them) to create significant signals in both SETs.

7.5.3 Why the charge motion could not be a TLF?

In this section, I will try to rule out the case of a TLF. First, the chance to have two interface states or two single donor sites in the Si substrate between which an

electron can tunnel back and forth is small compared to have just a single interface trap or a single donor which is tunnel-coupled to the Si SET. Second, for a TLF, if the Si SET conductance peak traces are assumed to shift in the way described in Sec. 7.5.1 (the conductance peak trace shifts to the right when it meets the green lines in Fig. 7.20 from above), which is a "screening" effect to the Si SET (V_g has to be more negative to recover the conductance peaks), then the fluctuator must be closer to the Si SET island when it is above the main splitting line and further away from the Si SET island when V_g is more negative. Figure 7.23 summarizes this situation. Note: I have assumed the TLF is an electron, but the same argument can be valid for a hole. Given that the TLF is driven by electric fields, this is contrary to the direction of the electric field, because a more negative side gate voltage tends to push the electron towards the SET islands.

Figure 7.24 shows another possibility. The fluctuator is beyond the side gate edges and tunnels in the region between the side gate edge and the SET lead. In Fig. 7.24, I only plot the electric field lines created by the side gate while keeping all other electrodes grounded, since I only consider the effect from the side gate while keeping all the other electrodes at constant potentials.

To have a signal of about 0.40 e detected by the Si SET, the TLF has to tunnel between two sites which are well separated and have a significant coupling difference to the Si SET island. However, based on Fig. 7.24, and due to the geometry of my device, couplings of the TLF to the side gate or the Si SET lead will dominate, and neither site could have a significant coupling to the Si SET island. This line of argument naturally raises the question of how could it be possible to have a

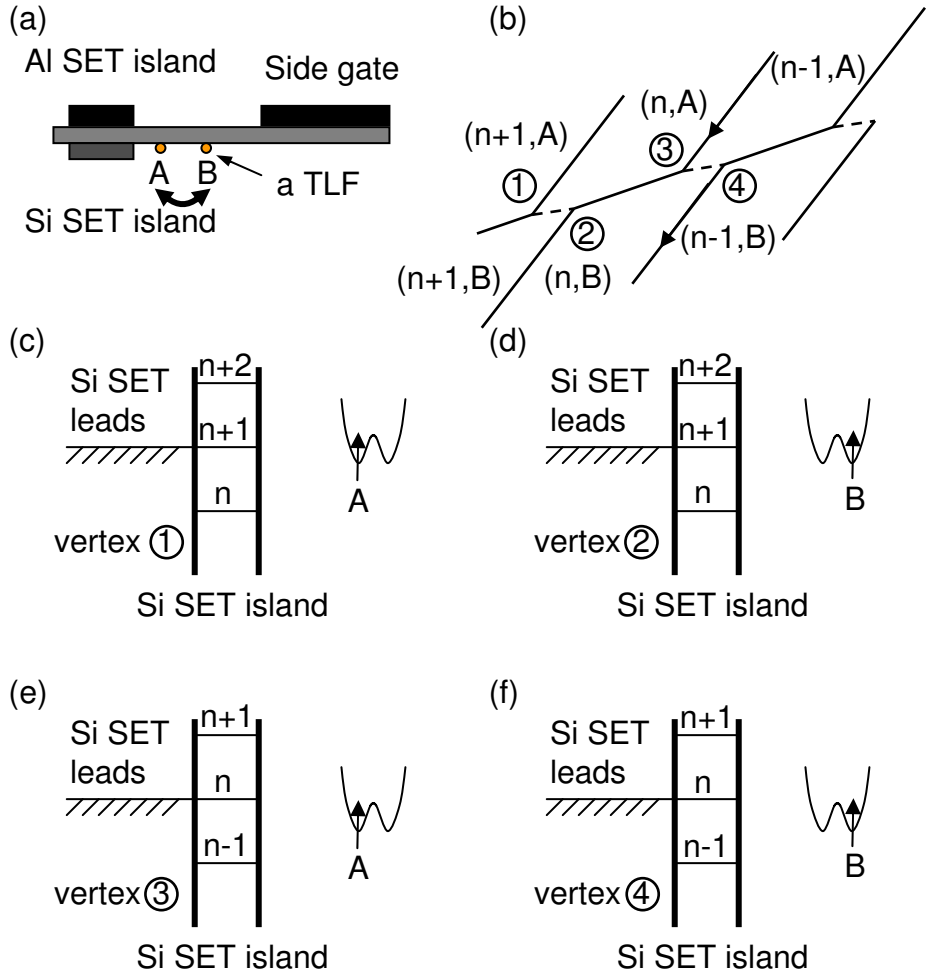


Figure 7.23: (a) Schematic cross-section view of the Al SET coupled to the Si SET. A and B are two possible sites (see Fig. 7.24) between which the TLF can tunnel back and forth. (b) Schematic of the correlated conductances of the Al and Si SETs. Arrows show how the Si SET conductance peak traces shift. (c) – (f) Schematics of the energy diagram of the system at the four vertexes labeled 1, 2, 3, and 4 in (b) respectively. The up arrows represent the occupancy of one electron.

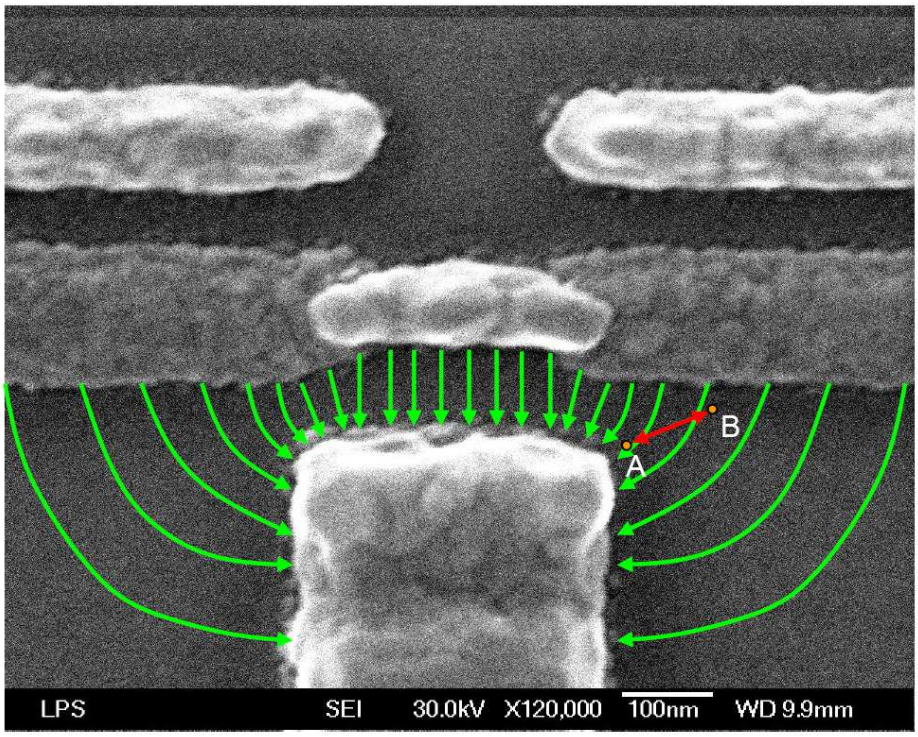


Figure 7.24: SEM image of a device that was fabricated simultaneously with Device3 using the same fabrication parameters. The green lines represent the electric field lines between the side gate and the Al SET. Since the Si SET is close to the Al SET, the electric field between the side gate and the Si SET should not be too different. A and B are two possible sites between which a TLF can tunnel back and forth at the Si/SiO_2 interface or in the Si substrate. Under more negative side gate voltages, the TLF tends to stay at site B which is further away from the SET islands than site A.

significant coupling difference between the defect and the Si SET island?

If there is really a TLF between the Si SET island and side gate, then what behavior do we expect? First, for a more negative gate voltage, the TLF will be pushed closer to the Si SET island, which will further increase the Si SET island potential energy. Therefore, the effect of the TLF on the Si SET should be an "enhancement": to recover the Si SET conductance, V_g has to be less negative to compensate the effect of the TLF. Therefore, the Si SET conductance peak traces have to shift in the opposite way from the previous discussions, as depicted in Fig. 7.25. Of course, this shift will be contrary to the measured intensity of the Si SET conductance.

The Al SET phase shift, however, could remain in the same direction when it crosses the boundary 2-3 in Fig. 7.25, which can be explained as follows. From above to below boundary 2-3, the TLF becomes closer to the Al SET island, but the number of electrons on the Si SET island drops by one. Because the Si SET island has a much stronger coupling to the Al SET island than the TLF does, the combined effect will be to induce more electrons on the Al SET island, that is, the Al SET conductance peak trace will shift downwards, the same as discussed before.

In this case, it is possible for the coupling between the TLF and the Si SET island to be dominant. However, because the side gate is so close to the Si SET island, it seems impossible to have a significant coupling difference to the Si SET island between the two sites of the TLF. The phase shift of the Si SET conductance should be much smaller.

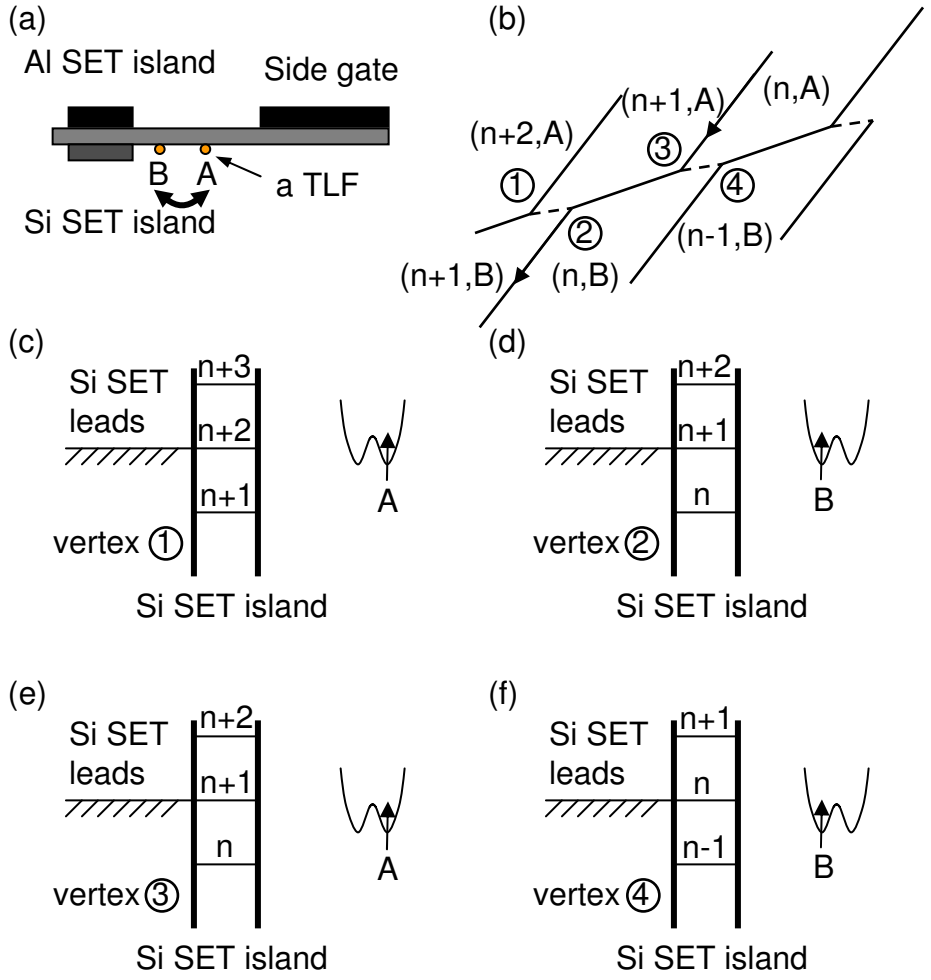


Figure 7.25: (a) Schematic cross-section view of the device. (b) Schematic of the correlated conductances of the Al and Si SETs. Arrows show how the Si SET conductance peak traces shift. (c) – (f) Schematics of the energy diagram of the system at the four vertexes labeled 1, 2, 3, and 4 in (b) respectively. The up arrows represent the occupancy of one electron.

7.6 Electrostatic model to explain the experimental data

After ruling out the possibility of a TLF, I now consider the possibility that the defect is tunnel-coupled to the Si SET island. Figure 7.26 shows the charge configurations. Along the boundary B-C, the number of electrons on the Si SET island does not change while the defect changes its occupancy. Therefore there is no current measured in the Si SET. At the boundary C-D, an electron is exchanged between the Si SET island and the defect. This is a second order process and the electrostatic interaction between the defect and the Si SET prevents continuous electron tunneling through the Si SET island. Therefore, no conductance of the Si SET is measured either.

7.6.1 Electrostatic model and qualitative explanation of the data

For the tunnel-coupled situation, the couplings can be modeled as capacitors as depicted in Fig. 7.27. For the Al and Si SETs, because the DC biases are very small, < 100 μV, I will not distinguish between drain and source. This leaves five electrodes in the system: the Al SET leads (both drain and source), the Al SET island, the Si SET leads (both drain and source), the Si SET island, and the side gate. I will define the coupling capacitances of the defect to the above five electrodes as C_h, C_e, C_f, C_d, and C_{g_D}, respectively. The couplings between the Si SET and the Al SET are the same as in Chap. 6, except without C_4, the coupling between the Si SET island and the Al SET leads, which is negligible. Again due to the negligible charging energy of the Al SET, the charging events on the Al SET island

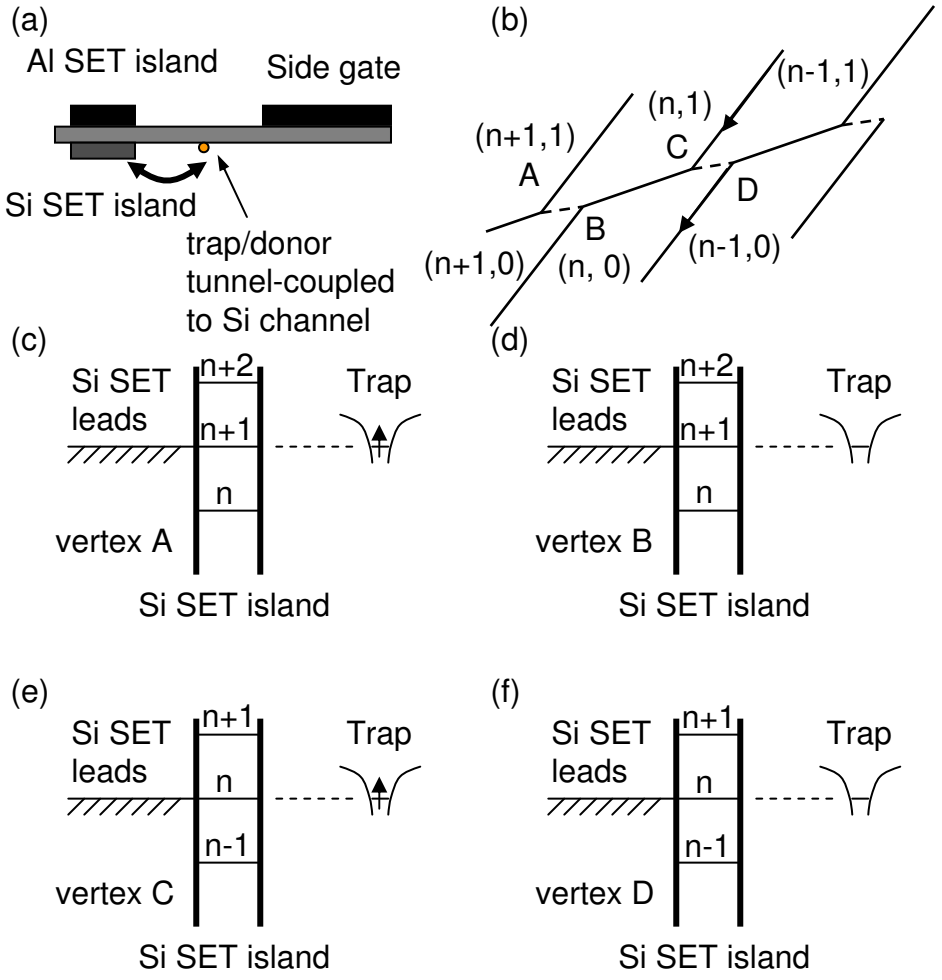


Figure 7.26: (a) Schematic cross-section view of the device when the defect is tunnel-coupled to the Si SET island. (b) Schematic of the correlated conductances of the Al and Si SETs. Arrows show how the Si SET conductance peak traces shift. (c) – (f) Schematics of the energy diagram of the system at the four vertexes labeled as A, B, C, and D in (b) respectively. The up arrows represent the occupancy of one electron.

have almost negligible effect on the defect and the Si SET. The electrostatic model in Fig. 7.27(a) can thus be simplified to the model shown in Fig. 7.27(b). The resulting phase diagram is shown in Fig. 7.28. This is similar to Fig. 7.26(b), except with details of the parameters.

If there is no coupling between the defect and the Si SET island, the defect site will get occupied whenever the defect energy is aligned with the Fermi energy of the Si channel; the defect site will be empty whenever its potential energy is higher than the Fermi energy. The Fermi level can be well controlled by the external voltage source V_{n+}. However, due to the coupling between the defect and the Si SET island, the charging and discharging of the defect site will be more complicated. A change in the number of electrons on the Si SET island changes the potential of the defect as well. Similarly, a change in the occupancy of the defect site will act as an offset charge, that is, as an effective change in gate voltage. For example, when an electron tunnels away from the Si SET island, the potential of the defect will be lowered. Therefore when line B-C (the boundary between defect is empty and occupied) in Fig. 7.28 passes through vertex C (in B $\rightarrow$ C direction), the defect will get occupied. To restore the defect potential to align with the Fermi energy, V_g has to be more negative, resulting in a downward vertical shift Δ in V_g.

On the other hand, when line F-C in Fig. 7.28 passes through vertex C (in F $\rightarrow$ C direction), the disappearance of the defect electron will lower the potential of the Si SET island, therefore the Si SET island will tend to have more electrons than it would have otherwise. The effect is to shift line F-C to the right. The same argument holds for the phase shift of the Al SET: there tends to be more

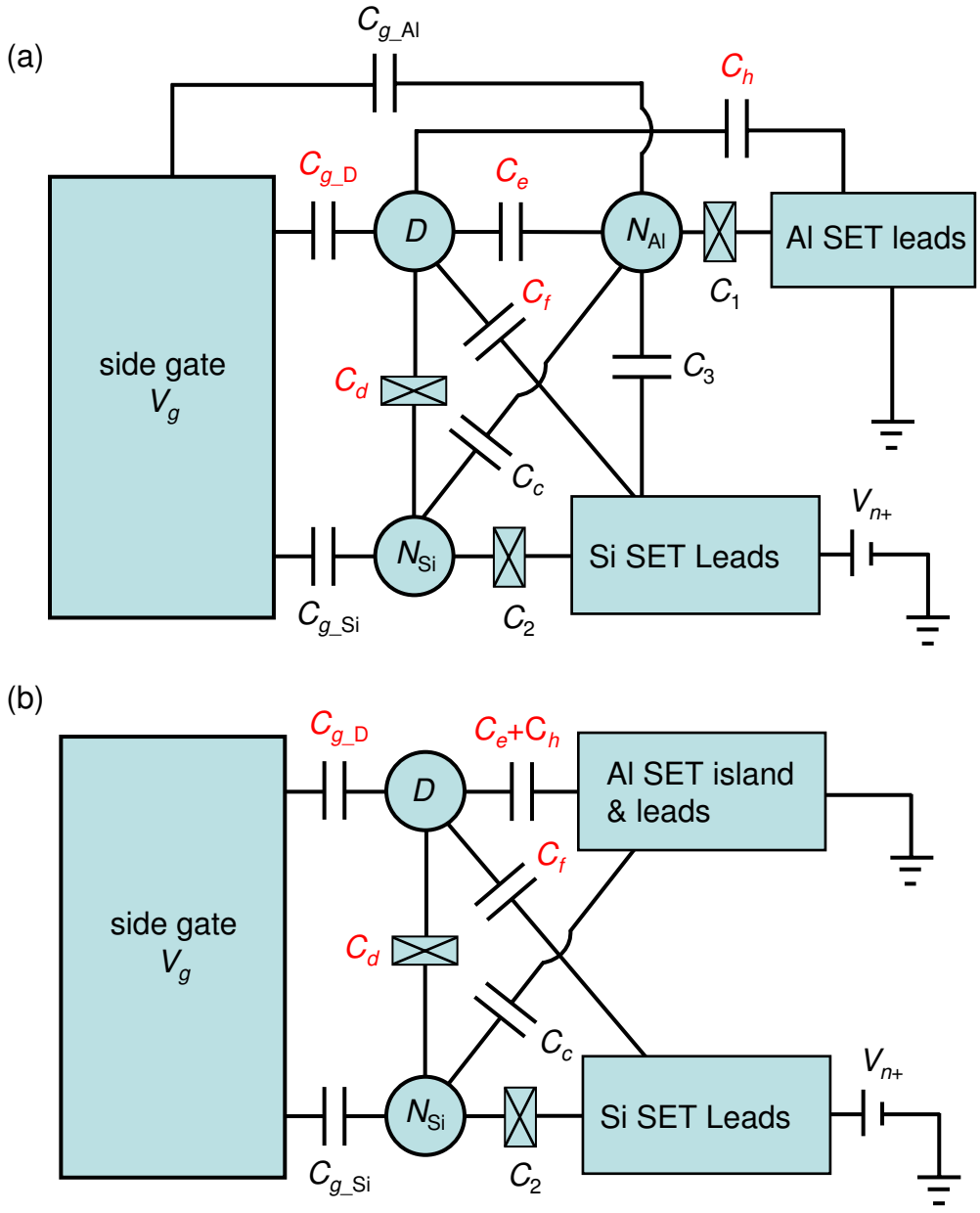


Figure 7.27: (a) Three-dot model. (b) Two-dot model. All the capacitances are defined as labeled. The small green boxes represent tunnel-couplings and D represents the defect.

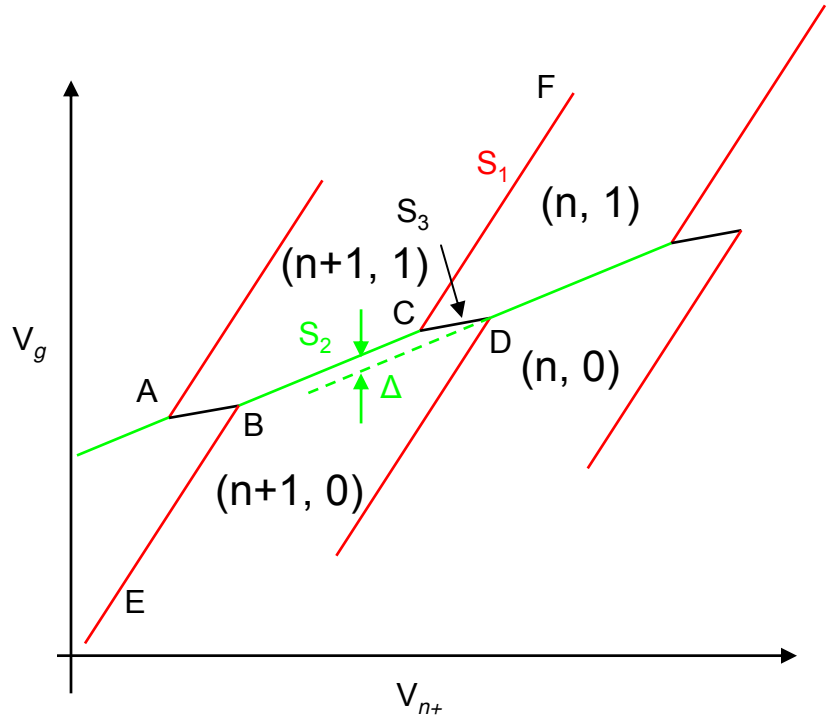


Figure 7.28: Phase diagram based on the model in Fig. 7.27. This phase diagram is also a schematic of the data in Fig. 7.20. The single-electron charging events on the Al SET island are neglected because of its small charging energy. Each pair of numbers in parenthesis represents a stable charge configuration. n is the number of electrons on the Si SET island. The y-component being 0 represents that the defect is unoccupied while 1 represents that the defect is occupied. S_1 is the slope of the Si SET conductance peak traces. S_2 is the slope of the green lines along which the defect changes its occupancy. S_3 is the slope of the boundary between (n,1) and (n+1,0). Δ is the vertical spacing between the neighboring green lines.

electrons on the Al SET island, therefore the Al SET conductance peak traces will shift downwards just as what it does when an electron leaves the Si SET island. All these features have been reflected in the data (Fig. 7.21) and Fig. 7.28.

In the above electrostatic model, the single charge defect is tunnel-coupled to the Si SET island. However, it could be tunnel-coupled to the Si SET leads as well. The following two cases would lead to the same observable behavior: (i) an electron tunnels directly from the defect site to the Si SET leads; (ii) an electron tunnels from the defect to the Si SET island while another electron simultaneously tunnels from the Si SET island to the leads, a process called cotunneling.[101] Two other cases could also occur: (i) an electron tunnels directly from the defect site to the Si SET island; (ii) an electron tunnels from the defect to the Si SET leads while another electron simultaneously tunnels from the Si SET leads to the island.

The tunneling rate between the defect and the Si SET island or the cotunneling rate is fast enough that in Figs. 7.16, 7.17, and 7.18, when V_{n+} < -0.51 V, no hysteresis of the Si SET conductances is observed as the gate voltage is swept back and forth. This case is shown in Figs. 7.29(a) and 7.29(b) for the Si and Al SET conductance traces at $V_{n+} = -0.585$V respectively. This implies that the tunneling rate or cotunneling rate is faster than 1 Hz, the bandwidth of the measurement. However when V_{n+} > -0.51 V, a hysteresis is observed, suggesting a slower tunneling rate or cotunneling rate than the measurement bandwidth. Figure 7.29(c) shows the Al SET conductance traces at $V_{n+} = -0.496$V in both directions with a clear hysteresis as indicated by the blue and red arrows where the defect changes its occupancy. No Si SET conductance is measurable at such a low V_{n+} bias. Note:

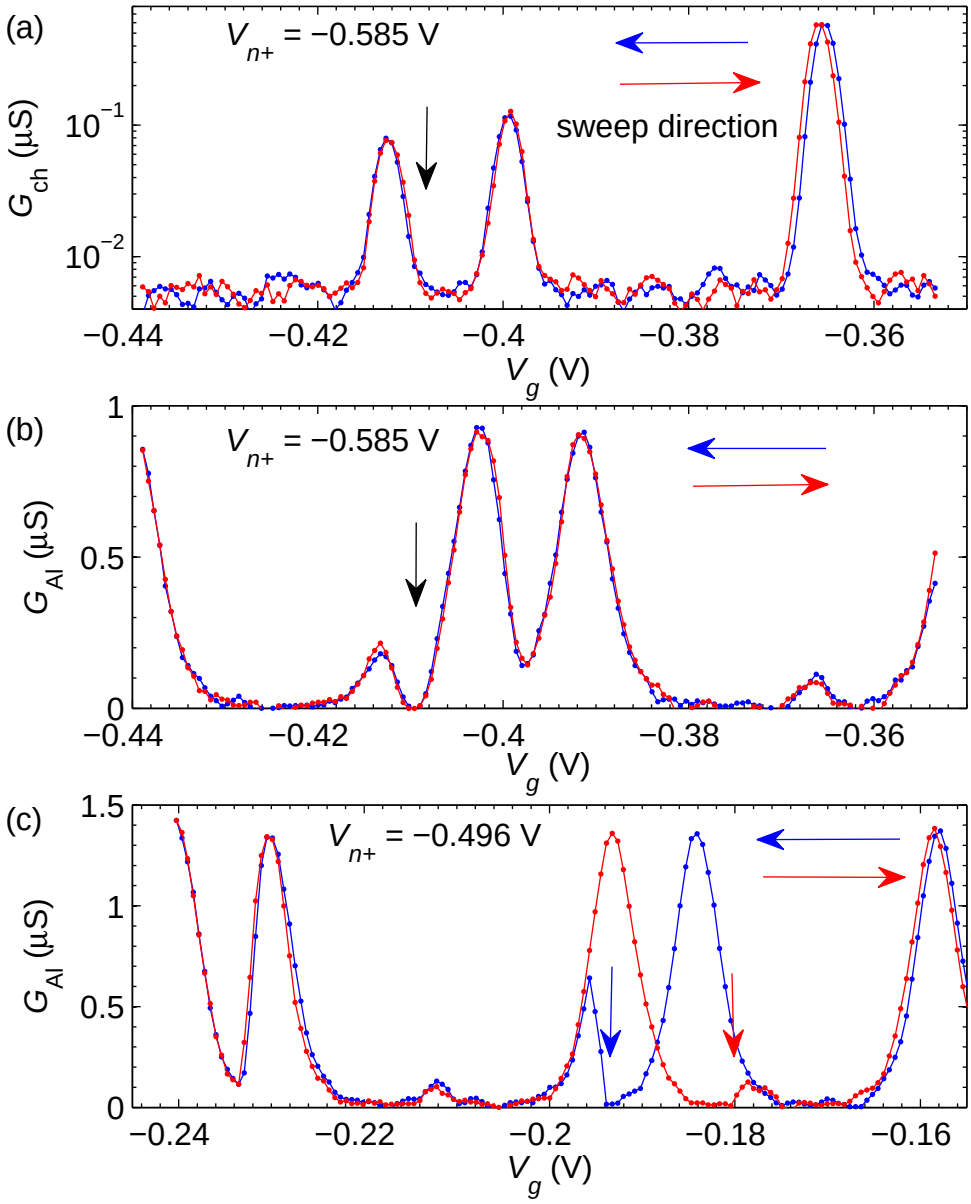


Figure 7.29: (a) and (b) show the the Si and Al SET conductance traces, respectively, as a function of V_g at $V_{n+} = -0.585V$. No hysteresis is observed. (c) shows the Al SET conductance traces as a function of V_g at $V_{n+} = -0.496V$. Hysteresis can be seen. The black arrows in (a) and (b) show where the defect changes its occupancy. The blue and red arrows in (c) show where the defect changes its occupancy in the corresponding sweep direction.

Our measurement limit is about 10 fA, corresponding to a tunneling rate of the Si SET about 100 kHz.

The fact that only one electron is involved makes the absolute values of the defect capacitances almost irrelevant to the problem. The absolute values of V_g and V_{n+} at which the single electron starts to move are totally irrelevant also, since an arbitrary offset in V_g and V_{n+} will not change the physics. Actually the random fixed background charges and the work function differences have already shifted V_g and V_{n+} in an uncontrolled way. The absolute values of the defect capacitances will only slightly modify the capacitance matrix associated with the Al and Si SET islands. In the limit of a small defect, it will be totally irrelevant. The similarity of the five parallelograms in Fig. 7.14 and the linearity of the position where the defect changes its occupancy in voltage space in Fig. 7.19 are also consistent with the defect being very small.

7.6.2 Mathematics of the three-dot and two-dot electrostatic models

The electrostatic model can quantitatively be compared to the data. Based on the model, Fig. 7.27(a), the capacitance matrix can be written as discussed in Sec. 2.3.2 as:

$$\mathbf{C} = \begin{pmatrix} C_{\Sigma\_\mathrm{Al}} & -C_c & -C_e \\ -C_c & C_{\Sigma\_\mathrm{Si}} & -C_d \\ -C_e & -C_d & C_{\Sigma\_\mathrm{D}} \end{pmatrix} \tag{7.6}$$

The charge matrix can be written as:

$$\mathbf{Q} = \begin{pmatrix} -eN_{\mathrm{Al}} + C_{g\_\mathrm{Al}}V_g + C_3V_{n+} \\ -eN_{\mathrm{Si}} + C_{g\_\mathrm{Si}}V_g + C_2V_{n+} \\ -eN_{\mathrm{D}} + C_{g\_\mathrm{D}}V_g + C_fV_{n+} \end{pmatrix} \tag{7.7}$$

Then the total electrostatic energy can be expressed in matrix form as:

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, N_{\mathrm{D}}, V_g, V_{n+}) = \frac{1}{2}\mathbf{Q}^T\mathbf{C}^{-1}\mathbf{Q}. \tag{7.8}$$

where the total capacitances $C_{\Sigma\_\mathrm{Al}} = C_1 + C_e + C_{g\_\mathrm{Al}} + C_c + C_3$, $C_{\Sigma\_\mathrm{Si}} = C_c + C_2 + C_d + C_{g\_\mathrm{Si}}$, and $C_{\Sigma\_\mathrm{D}} = C_e + C_h + C_d + C_f + C_{g\_\mathrm{D}}$.

The energy degenerate conditions that set the boundaries B-E, B-C and C-D in Fig. 7.28 respectively are:

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Al}}, N_{\mathrm{Si}} \pm 1, 0, V_g, V_{n+}) \pm eV_{n+} \tag{7.9}$$

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, 1, V_g, V_{n+}) + eV_{n+} \tag{7.10}$$

$$E(N_{\mathrm{Al}}, N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Al}}, N_{\mathrm{Si}} - 1, 1, V_g, V_{n+}) \tag{7.11}$$

where eV_{n+} is the extra work done by voltage source V_{n+}, when one electron tunnels to the Si SET island or the defect from the Si SET leads. Since the charging effect of the Al SET is negligible, δN_{Al} has been neglected in the above energy degenerate conditions.

I can solve Eqs. 7.9, 7.10, 7.11 to get the slopes S_{3D_1}, S_{3D_2}, S_{3D_3} and the vertical spacing Δ_{3D} (due to the single electron charging effect on the Si SET island) as defined in Fig. 7.28 (the subscripts "3D" and later "2D" represent the results in

the 3D model and the 2D model respectively):

$$\begin{aligned} S_{3D\_1} &= (C_2C_e^2 - C_3C_cC_{\Sigma\_\mathrm{D}} - C_3C_eC_d - C_2C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{D}} - C_fC_{\Sigma\_\mathrm{Al}}C_d \\ &\quad -C_fC_cC_e - C_{\Sigma\_\mathrm{Al}}C_d^2 - C_c^2C_{\Sigma\_\mathrm{D}} - C_e^2C_{\Sigma\_\mathrm{Si}} + C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}}C_{\Sigma\_\mathrm{D}} \\ &\quad -2C_cC_eC_d)/(-C_{g\_\mathrm{Si}}C_e^2 + C_{g\_\mathrm{Al}}C_cC_{\Sigma\_\mathrm{D}} + C_{g\_\mathrm{Al}}C_eC_d + C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{D}} \\ &\quad +C_{g\_\mathrm{D}}C_{\Sigma\_\mathrm{Al}}C_d + C_{g\_\mathrm{D}}C_cC_e) \end{aligned} \tag{7.12}$$

$$\begin{aligned} S_{3D\_2} &= (-C_fC_c^2 + C_2C_cC_e + C_2C_{\Sigma\_\mathrm{Al}}C_d + C_3C_cC_d + C_3C_eC_{\Sigma\_\mathrm{Si}} \\ &\quad +C_fC_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} - C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}}C_{\Sigma\_\mathrm{D}} + 2C_cC_eC_d + C_{\Sigma\_\mathrm{Al}}C_d^2 + C_c^2C_{\Sigma\_\mathrm{D}} \\ &\quad +C_e^2C_{\Sigma\_\mathrm{Si}})/(-C_{g\_\mathrm{Al}}C_cC_d - C_{g\_\mathrm{Al}}C_eC_{\Sigma\_\mathrm{Si}} - C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}C_d - C_{g\_\mathrm{Si}}C_cC_e \\ &\quad -C_{g\_\mathrm{D}}C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} + C_{g\_\mathrm{D}}C_c^2) \end{aligned} \tag{7.13}$$

$$\begin{aligned} S_{3D\_3} &= (C_2C_e^2 - C_fC_c^2 + C_2C_cC_e + C_2C_{\Sigma\_\mathrm{Al}}C_d + C_3C_cC_d + C_3C_eC_{\Sigma\_\mathrm{Si}} \\ &\quad +C_fC_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} - C_3C_cC_{\Sigma\_\mathrm{D}} - C_3C_eC_d - C_2C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{D}} - C_fC_{\Sigma\_\mathrm{Al}}C_d \\ &\quad -C_fC_cC_e)/(-C_{g\_\mathrm{Si}}C_e^2 + C_{g\_\mathrm{D}}C_{\Sigma\_\mathrm{Al}}C_d + C_{g\_\mathrm{D}}C_c^2 + C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{D}} \\ &\quad +C_{g\_\mathrm{Al}}C_cC_{\Sigma\_\mathrm{D}} + C_{g\_\mathrm{Al}}C_eC_d + C_{g\_\mathrm{D}}C_cC_e - C_{g\_\mathrm{D}}C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} \\ &\quad -C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}C_d - C_{g\_\mathrm{Si}}C_cC_e - C_{g\_\mathrm{Al}}C_cC_d - C_{g\_\mathrm{Al}}C_eC_{\Sigma\_\mathrm{Si}}) \end{aligned} \tag{7.14}$$

$$\begin{aligned} \Delta_{3D} &= e(C_{\Sigma\_\mathrm{Al}}C_d + C_cC_e)/(C_{g\_\mathrm{Al}}C_cC_d + C_{g\_\mathrm{Al}}C_eC_{\Sigma\_\mathrm{Si}} + C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}C_d \\ &\quad +C_{g\_\mathrm{Si}}C_cC_e + C_{g\_\mathrm{D}}C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}} - C_{g\_\mathrm{D}}C_c^2) \end{aligned} \tag{7.15}$$

Needless to say, these solutions are complicated; each one has more than ten terms.

I can also try using the simplified model shown in Fig. 7.27(b) to do the calculation, assuming a negligible charging energy of the Al SET, that is, no discreteness

of N_{Al}. In this case, the capacitance matrix and the charge matrix can be written as:

$$\mathbf{C} = \begin{pmatrix} C_{\Sigma\_\mathrm{Si}} & -C_d \\ -C_d & C_{\Sigma\_\mathrm{D}} \end{pmatrix} \tag{7.16}$$

$$\mathbf{Q} = \begin{pmatrix} -eN_{\mathrm{Si}} + C_{g\_\mathrm{Si}}V_g + C_2V_{n+} \\ -eN_{\mathrm{D}} + C_{g\_\mathrm{D}}V_g + C_fV_{n+} \end{pmatrix} \tag{7.17}$$

Now conditions that set the boundaries will be:

$$E(N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Si}} \pm 1, 0, V_g, V_{n+}) \pm eV_{n+} \tag{7.18}$$

$$E(N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Si}}, 1, V_g, V_{n+}) + eV_{n+} \tag{7.19}$$

$$E(N_{\mathrm{Si}}, 0, V_g, V_{n+}) = E(N_{\mathrm{Si}} - 1, 1, V_g, V_{n+}) \tag{7.20}$$

By solving the above equations, I can get the solutions of the slopes and Δ:

$$S_{2D\_1} = \frac{C_{\Sigma\_\mathrm{Si}}C_{\Sigma\_\mathrm{D}} - C_d^2 - C_{\Sigma\_\mathrm{D}}C_2 - C_dC_f}{C_{\Sigma\_\mathrm{D}}C_{g\_\mathrm{Si}} + C_dC_{g\_\mathrm{D}}} \tag{7.21}$$

$$S_{2D\_2} = \frac{C_{\Sigma\_\mathrm{Si}}C_{\Sigma\_\mathrm{D}} - C_d^2 - C_dC_2 - C_{\Sigma\_\mathrm{Si}}C_f}{C_{\Sigma\_\mathrm{Si}}C_{g\_\mathrm{D}} + C_dC_{g\_\mathrm{Si}}} \tag{7.22}$$

$$S_{2D\_3} = \frac{C_{\Sigma\_\mathrm{D}}C_2 - C_dC_2 + C_dC_f - C_{\Sigma\_\mathrm{Si}}C_f}{C_{\Sigma\_\mathrm{Si}}C_{g\_\mathrm{D}} - C_{\Sigma\_\mathrm{D}}C_{g\_\mathrm{Si}} + C_dC_{g\_\mathrm{Si}} - C_dC_{g\_\mathrm{D}}} \tag{7.23}$$

$$\Delta_{2D} = \frac{eC_d}{C_{\Sigma\_\mathrm{Si}}C_{g\_\mathrm{D}} + C_dC_{g\_\mathrm{Si}}} \tag{7.24}$$

If I let C_{Σ_Al} go to infinity in the 3-dot model, then only the terms with C_{Σ_Al} will be significant. Then the solutions of the 3-dot model, Eqs. 7.12 – 7.15, will be reduced back to Eqs. 7.21 – 7.24 in the 2-dot model. In the limit of very small C_e, C_d, and C_{Σ_D}, S_{3D_1} can be reduced to:

$$S_{3D\_1} = \frac{-C_3C_c - C_2C_{\Sigma\_\mathrm{Al}} - C_c^2 + C_{\Sigma\_\mathrm{Al}}C_{\Sigma\_\mathrm{Si}}}{C_{g\_\mathrm{Al}}C_c + C_{g\_\mathrm{Si}}C_{\Sigma\_\mathrm{Al}}} \tag{7.25}$$

which is exactly Eq. 7.1. Therefore, both 3-dot and 2-dot models make good sense.

There is another way to deduce Eqs. 7.22, 7.23 and 7.24, which would be very helpful in understanding the electrostatics associated with the defect. S_{2D_3} is the slope of the boundary at which the defect can exchange one electron with the Si SET island. Therefore the change of V_g and V_{n+} have to maintain a ratio to keep both the defect potential change ΔE_D and the Si SET island potential change ΔE_{Si} the same. Based on the 2-dot electrostatic model Fig. 7.27(b), ΔV_g change on side gate will change the defect potential and the Si SET island potential by:

$$\Delta E_{D\_V_g} = \frac{e}{C_{\Sigma\_\mathrm{D}}} \Delta V_g (C_{g\_\mathrm{D}} + \frac{C_{g\_\mathrm{Si}}}{C_{\Sigma\_\mathrm{Si}}} C_d) \tag{7.26}$$

$$\Delta E_{Si\_V_g} = \frac{e}{C_{\Sigma\_\mathrm{Si}}} \Delta V_g (C_{g\_\mathrm{Si}} + \frac{C_{g\_\mathrm{D}}}{C_{\Sigma\_\mathrm{D}}} C_d) \tag{7.27}$$

The first terms in Eqs. 7.26 and 7.27 are from the direct coupling of the side gate to the defect and the Si SET island respectively, while the second terms are from the indirect coupling mediated by the Si SET island and the defect respectively. Similarly, ΔV_{n+} on the Si channel will change the defect potential and the Si SET island potential by:

$$\Delta E_{D\_V_{n+}} = \frac{e}{C_{\Sigma\_\mathrm{D}}} \Delta V_{n+} (C_f + \frac{C_2}{C_{\Sigma\_\mathrm{Si}}} C_d) \tag{7.28}$$

$$\Delta E_{Si\_V_{n+}} = \frac{e}{C_{\Sigma\_\mathrm{D}}} \Delta V_{n+} (C_2 + \frac{C_f}{C_{\Sigma\_\mathrm{D}}} C_d) \tag{7.29}$$

Then Eq. 7.26 + Eq. 7.28 = Eq. 7.27 + Eq. 7.29 will lead to Eq. 7.23.

S_{2D_2} is the slope of the boundary at which the defect changes its occupancy, therefore the defect potential will maintain aligned with the Fermi energy of the Si channel. However, since this process involves one electron tunneling from/to the Si

SET leads which is held at a non-zero voltage, a simple calculation as above will not hold. To simplify the calculation, I convert the bias condition from biasing the Si SET to biasing the Al SET. In the latter case, although an electron is still involved to tunnel between the Si channel and the defect, because the Si channel is grounded, no extra term will be included in the calculation.

To calculate S_{2D_2} in V_g-V_{Al} space, I have to know how the slope in the voltage space changes between the two different bias conditions. It turns out that the two slopes will satisfy the following formula:

$$S + S' = 1 \tag{7.30}$$

where S and S' are the slopes of lines in voltage space V_g-V_{n+} and V_g-V_{Al} respectively. The justification will be argued as follows. Let's assume that there are two points in V_g-V_{n+} voltage space: (V_{n+_1}, V_{g_1}), and (V_{n+_2}, V_{g_2}), which determine a slope $S = \frac{V_{g\_1} - V_{g\_2}}{V_{n+\_1} - V_{n+\_2}}$. If we change the voltage space from V_g-V_{n+} to V_g-V_{Al}, the two points will change accordingly: (V_{n+_1}, V_{g_1}) $\rightarrow$ (-V_{n+_1}, $V_{g\_1} - V_{n+\_1}$) and (V_{n+_2}, V_{g_2}) $\rightarrow$ (-V_{n+_2}, $V_{g\_2} - V_{n+\_2}$). Then the slope of the line determined by the new two points will be: $S' = \frac{V'_{g\_1} - V'_{g\_2}}{V'_{n+\_1} - V'_{n+\_2}} = \frac{(V_{g\_1} - V_{n+\_1}) - (V_{g\_2} - V_{n+\_2})}{-V_{n+\_1} + V_{n+\_2}} = -S + 1$. Equation 7.30 will be very helpful to convert slopes if a switch to a different voltage space is necessary or makes problems easier to understand.

Now I can calculate ΔE_D from ΔV_{Al} in V_g-V_{Al} space as follows:

$$\Delta E_{D\_V_{Al}} = \frac{e}{C_{\Sigma\_\mathrm{D}}} \Delta V_{Al} (C_e + C_h + \frac{C_c}{C_{\Sigma\_\mathrm{Si}}} C_d) \tag{7.31}$$

ΔE_D from ΔV_g will be the same as Eq. 7.26. Finally, we have $\Delta E_{D\_V_{Al}} + \Delta E_{D\_V_g} = 0$,

which gives:

$$S'_{2D\_2} = \frac{V_g}{V_{Al}} = -(C_e + C_h + \frac{C_c}{C_{\Sigma\_\mathrm{Si}}} C_d)/(C_{g\_\mathrm{D}} + \frac{C_{g\_\mathrm{Si}}}{C_{\Sigma\_\mathrm{Si}}} C_d) \tag{7.32}$$

We can easily confirm that $S_{2D\_2} + S'_{2D\_2} = 1$, that is, Eq. 7.22 + Eq. 7.32 = 1. Because the simple relationship between S'_{2D_2} and S_{2D_2}, and the fact that S'_{2D_2} is simpler than S_{2D_2}, I will try to use S'_{2D_2} instead of S_{2D_2} as one parameter for the calculation.

Δ can be calculated in the same way. One electron change on the Si SET island will change the defect potential by:

$$E_{D\_Si} = \frac{e^2 C_d}{C_{\Sigma\_\mathrm{Si}} C_{\Sigma\_\mathrm{D}}} \tag{7.33}$$

ΔV_g will have the same effect on ΔE_D as in Eq. 7.26. From Eqs. 7.33 and 7.26, Eq. 7.24 can be recovered.

I introduced in Sec. 7.5.1 two very important parameters for the final calculation: the phase shift of the Al and Si SETs due to the occupancy change of the defect. These parameters need a more careful justification. For a three-dot system, the effect on one dot due to a unit change of the number of electrons on another dot consists of two parts: the direct coupling between the first two dots and the indirect coupling mediated by the third dot. The phase shift of the Al SET due to the defect in Fig. 7.27(a) can be calculated as:

$$\Phi_{Al\_D} = \frac{C_e}{C_{\Sigma\_\mathrm{D}}} + \frac{C_c C_d}{C_{\Sigma\_\mathrm{D}} C_{\Sigma\_\mathrm{Si}}}. \tag{7.34}$$

The first and the second terms are the direct and indirect couplings respectively. A more careful and complicated calculation using the three model, gives an extra term

C_d^2 in the denominator. However, it is more than two orders of magnitude smaller than $C_{\Sigma\_\mathrm{D}}C_{\Sigma\_\mathrm{Si}}$ and can be neglected. Note the indirect coupling is comparable to the direct coupling and can not be neglected, since $C_c/C_{\Sigma\_\mathrm{Si}}$ is big, $\cong 0.31$. To calculate the phase shift of the Si SET due to the defect, the indirect coupling mediated by the Al SET can be safely neglected, because in this case the mediated interaction by the Al SET will always include one factor $C_c/C_{\Sigma\_\mathrm{Al}}$, which is only a couple of percent. Therefore, the phase shift of the Si SET due to the defect will be:

$$\Phi_{Si\_D} \cong \frac{C_d}{C_{\Sigma\_\mathrm{D}}}. \tag{7.35}$$

7.6.3 Results and discussions

There are in total five unknown capacitances (C_h, C_e, C_f, C_d, and C_{g_D}) associated with the defect in the electrostatic model in Fig. 7.27. However, I have six parameters which can be extracted from the data: S_{2D_1} (Eq. 7.21), S_{2D_2} (Eq. 7.22), S_{2D_3} (Eq. 7.23), Δ_{2D} (Eq. 7.24), Φ_{Al_D} (Eq. 7.34), and Φ_{Si_D} (Eq. 7.35). Among them, S_{2D_1} is more related to the Al/Si SET system (for very small C_{Σ_D}, $S_{2D\_1} \rightarrow (C_c + C_{g\_\mathrm{Si}})/C_{g\_\mathrm{Si}}$ containing no information of the defect), but it can be used to check the validity of the model. In Eqs. 7.32, 7.24, and 7.34, the absolute value of C_{Σ_D} enters the problem only by slightly changing C_{Σ_Si} with one extra term C_d. Equation 7.35 is totally independent of the absolute value of C_{Σ_D}. Equation 7.23 slightly depends on the absolute value of C_{Σ_D}, because some of its terms involve multiplications of two capacitances associated with the defect. Therefore, what

really matter are the ratios of the capacitances associated with the defect. This agrees with the previous arguments in Sec. 7.6.1.

In the ideal case, all the Al SET conductance peak traces, as well as the Si SET peak traces, would be straight lines and parallel to each other. The occupancy change of defect charge will shift both the Al and Si SET peak traces uniformly, resulting in the main splitting line. In reality, however, the conductance peak traces are not really parallel to each other and their shifts due to the defect are not uniform in the whole voltage space. The reason is the change of the electrostatic couplings among the three dots and other electrodes under different bias conditions, which could come from slow background charge motions or changes in the shape of the Si SET island or the defect under different biases. The change in the Si SET island can be clearly seen in the non-uniform charging energies in Fig. 7.15. These effects make systematic study of the splitting over a large voltage space difficult, if not impossible.

To simplify things, I just analyze the behavior in a restricted voltage range. Diamonds a) and b) in Fig. 7.15 are about the same, meaning there is no big change of the Si SET island at these specific bias conditions. This will make it much easier to understand the main splitting. Also the electrostatics of the Al and Si SET system has been well understood in this region with all the couplings shown in Table 7.1. Therefore, I will focus on the splitting near ($V_{n+} = -0.585\ V$, $V_g = -0.45\ V$) in Fig. 7.21. The mean values of the capacitances associated with the Si SET in Table 7.1 are used. Averages are made for S_{2D_2}, Δ_{2D}, Φ_{Al_D} to compensate for the gradual changes in capacitances with bias voltage. However, S_{2D_3} and Φ_{Si_D} are

not possible to be averaged, because only one value of each can be extracted in this region.

Table 7.2 shows the solutions for the capacitances associated with the defect in terms of C_{Σ_D}. To get Table 7.2, only four measured parameters S_{2D_2}, Δ_{2D}, Φ_{Al_D}, and Φ_{Si_D} are used under different values of C_{Σ_D} (see column 1 of Table 7.2). S_{2D_3} is not used due to its presumably big uncertainty (it is determined by two intersections of two pairs of lines with a small slope difference).

Note that as C_{Σ_D} changes in the calculation by two orders of magnitude, the defect capacitances (ratios) do not change significantly (C_h/C_{Σ_D} changes the biggest, about 20%, because it has the smallest amplitude; all others change by a few percent). Table 7.3 shows the resulting slopes and Δ's in the 2D and 3D models based on the calculated capacitances in Table 7.2. The resulting S_{2D_1} changes by only about 5% for a change of C_{Σ_D} by two orders of magnitude, however, S_{2D_3} seems to change a lot, due to its stronger dependence on the absolute value of C_{Σ_D}. There is no big difference of the results between the 2D and 3D models. Again, difference between S_{2D_3} and S_{3D_3} is the biggest, about 10%, while Δ_{2D} and Δ_{3D} have a difference by less than 1%. The other two parameters have a few percent difference. This justifies the simplification from the 3D model to the 2D model.

The measured number $S_{2D\_3} = 0.368$. If S_{2D_3} is included as the fifth parameter, all the absolute values of the capacitances associated with the defect can be extracted as the following: $C_{\Sigma\_D} = 0.79$ aF, $\frac{C_d}{C_{\Sigma\_D}} = 0.429$, $\frac{C_e}{C_{\Sigma\_D}} = 0.082$, $\frac{C_f}{C_{\Sigma\_D}} = 0.326$, $\frac{C_h}{C_{\Sigma\_D}} = 0.058$, $\frac{C_{g\_D}}{C_{\Sigma\_D}} = 0.105$.

The above calculated values contain some additional information about the

Table 7.2: Capacitances associated with the defect in terms of fractions in C_{Σ_D}. All the solutions are calculated based on only four parameters $S_{2D\_2} = 3.1461$, $\Delta_{2D} = 6.594\ mV$, $\Phi_{Al\_D} = 0.2208$, and $\Phi_{Si\_D} = 0.4287$, assuming the different C_{Σ_D} values shown in column 1. The mean value of the capacitances associated with Si SET in Table Table 7.1 are used: $C_{\Sigma\_\mathrm{Si}} = 79.7$ aF, $C_2 = 49.2$ aF, $C_e = 25.9$ aF, and $C_{g\_\mathrm{Si}} = 4.64$ aF.

$C_{\Sigma\_\mathrm{D}}(aF)$	$\frac{C_d}{C_{\Sigma\_\mathrm{D}}}$	$\frac{C_e}{C_{\Sigma\_\mathrm{D}}}$	$\frac{C_f}{C_{\Sigma\_\mathrm{D}}}$	$\frac{C_h}{C_{\Sigma\_\mathrm{D}}}$	$\frac{C_{g\_\mathrm{D}}}{C_{\Sigma\_\mathrm{D}}}$
0.1	0.429	0.082	0.325	0.059	0.105
1	0.429	0.082	0.326	0.058	0.105
5	0.429	0.085	0.332	0.052	0.103
10	0.429	0.089	0.338	0.045	0.100

Table 7.3: Slopes and Δ's in the 2D and 3D models based on the calculated capacitances in Table 7.2.

$C_{\Sigma\_\mathrm{D}}(aF)$	S_{2D_1}	S_{2D_2}	S_{2D_3}	$\Delta_{2D}\ (mV)$	S_{3D_1}	S_{3D_2}	S_{3D_3}	$\Delta_{3D}\ (mV)$
0.1	6.578	3.146	0.378	6.594	6.170	3.060	0.424	6.638
1	6.541	3.146	0.364	6.594	6.136	3.059	0.410	6.637
5	6.389	3.146	0.302	6.594	5.997	3.057	0.348	6.636
10	6.222	3.146	0.222	6.594	5.843	3.053	0.268	6.635

defect's location. First, the total defect capacitance C_{Σ_D} is quite small, which confirms that the defect is indeed very small and justifies my previous assumption. The self-capacitance of a conducting sphere in bulk silicon is $4\pi\epsilon R$, where R is the radius. $C_{\Sigma\_D} = 0.79$ aF gives R $\cong$ 0.6 nm, which is much smaller than the Bohr radius of phosphorus ($\cong$ 1.6 nm) and arsenic ($\cong$ 2.5 nm) in bulk silicon. Of course, C_{Σ_D} is not well known; a 10% change of S_{2D_3} around $S_{2D\_3} = 0.368$ could cause C_{Σ_D} to change by a factor of about 3 to 5. Therefore, we can not take too seriously the precise value of C_{Σ_D}.

However, the ratios between the capacitances associated with the defect are robust, as seen in Table 7.2. First, C_d is bigger than C_f, so the defect is closer to the Si SET island than to the Si SET leads. However, I do not know which lead the defect is close to. I tried experiments with different DC biases between the Si SET leads to check which lead has more effect on the defect. But these experiments were not successful, because non-zero V_{ds} will broaden the conductance peaks dramatically, and I could not get a precise peak position for a comparison. Second, $C_d + C_f$ has the biggest contribution to C_{Σ_D}, about 76%. This means the defect is much closer to the Si SET channel than to the other electrodes. Based on the SEM image shown in Fig. 7.1(b), the lateral distance between the Al SET edge (presumably also the Si SET edge) and the side gate is about 100 nm. $(C_d + C_f)/C_{g\_D} \cong 7.2$ implies that the defect is about 1/8 of the distance between the Si channel and the side gate, or about 13 nm away from the Si channel. If I include the smaller dielectric constant of the thin SiO_2 layer (20 nm) beneath the side gate, the defect will be a little bit further away from the Si channel, about 20 nm. Third, even though the defect is

much closer to the Si channel than to the side gate, the coupling from the defect to the Al SET $C_e + C_h$ is very small, only $\cong 0.14 C_{\Sigma\_D}$, and comparable to C_{g_D}, $\cong 0.105 C_{\Sigma\_D}$. This means that the screening from the Si SET is pretty big, which is not too surprising because the Si SET is right beneath the Al SET.

Now I can try to explain the linearity in Fig. 7.19. It would be easier to consider it in V_g-V_{Al} space instead of V_g-V_{n+}. In the extreme limit, the Si SET tunnel barriers are so transparent (C_{Σ_Si} can be considered as infinity) that the number of electrons on Si SET island is not quantized and the Si channel behaves like one electrode. In this case, the defect will be capacitively coupled to the Al SET (quantization has already been neglected), the Si channel, and the side gate. To keep the the defect in resonance with the Si channel, we have V_g/V_{Al} = -$(C_e + C_h)/C_{g\_D}$, that is $-(0.082 + 0.058)/0.105 = -1.333$. To convert this slope back to V_g-V_{n+} space according to Formula 7.30, we have $V_g/V_{n+} = 2.333$, in good agreement with the measured $V_g/V_{n+} = 2.376$. This linearity simply means that $(C_e + C_h)/C_{g\_D}$ is constant over a large voltage range, which is only true for a small defect whose electron wave function does not change significantly under different biases. This is consistent with the defect being small.

Evolution of Φ_{Al_D} and Φ_{Si_D}

Another property of the defect I has studied is the evolution of the signal amplitude Φ_{Al_D} and Φ_{Si_D} from the defect detected by the Al and Si SETs. Figure 7.30 shows Φ along the straight line in Fig. 7.19. Both Φ_{Al_D} and Φ_{Si_D} are calculated

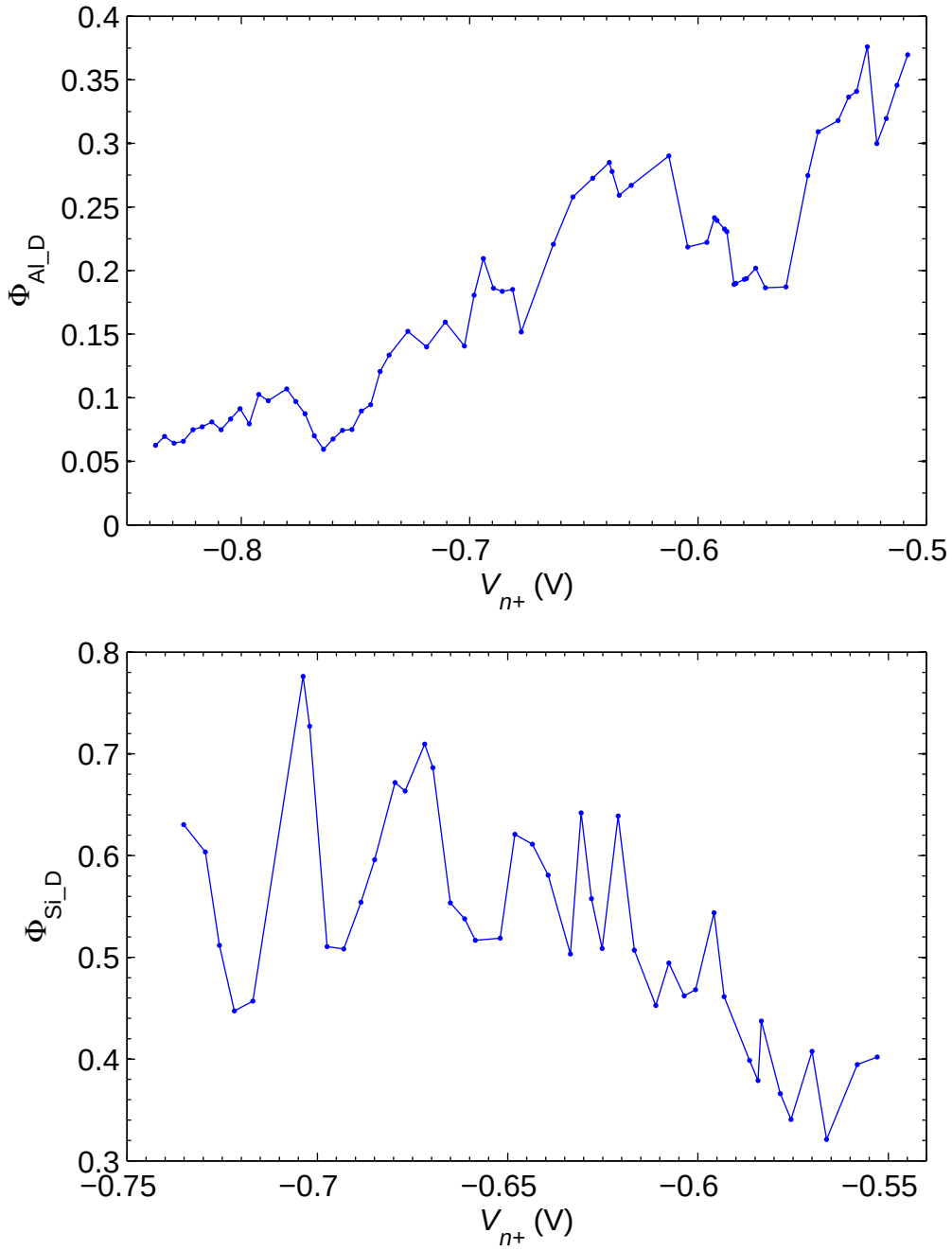


Figure 7.30: (a) The signal amplitude Φ_{Al_D} detected by the Al SET. (b) The signal amplitude Φ_{Si_D} detected by the Si SET. For both figures, the real x-axis is the along the straight line in Fig. 7.19. Note: the x-axes are different.

as shown in Fig. 7.21 based on eyeball fit. The x-axis in Fig. 7.30(a) covers a larger range. Note that the Al SET can sense the defect over the entire range. On the other hand, as V_{n+} approaches -0.5 V there is no measurable Si SET conductance and at very negative V_{n+} the Coulomb blockade oscillations disappear in the Si SET. The behavior of Φ_{Al_D} in Fig. 7.30(a) is obvious: a smaller signal is detected when there are more carriers in the silicon channel. In contrast, due to the irregularity of Coulomb blockade oscillations in the Si SET conductances, Φ_{Si_D} fluctuates a lot. Nevertheless Φ_{Si_D} is larger when V_{n+} is more negative.

Both trends can be understood as follows. I have shown that $(C_e + C_h)/C_{g\_D}$ is nearly constant based on the linearity in Fig. 7.19. C_{g_D} appears to be the same under different biases, therefore we might also expect $(C_e + C_h)$ to be nearly bias independent. In Eq. 7.34,

$$\Phi_{Al\_D} = \frac{C_e}{C_{\Sigma\_\mathrm{D}}} + \frac{C_c C_d}{C_{\Sigma\_\mathrm{D}} C_{\Sigma\_\mathrm{Si}}}.$$

the second term will go to zero as C_{Σ_Si} goes to infinity at very negative V_{n+}. In this limit, Φ_{Al_D} will reduce to $\frac{C_e}{C_{\Sigma\_\mathrm{D}}}$. Figure 7.30(a) shows $\Phi_{Al\_D} \cong 0.06$ in this limit. If C_e does not change, the change of Φ_{Al_D} from $\cong 0.082$ to $\cong 0.06$ means that C_{Σ_D} becomes about 37% bigger. Simple arithmetic shows that the increase of C_{Σ_D} mainly comes from the increase of C_d only, because Φ_{Si_D} changes from $\cong$ 0.43 to $\cong$ 0.60 at very negative V_{n+}, as shown in Fig. 7.30(b) and $\Phi_{Si\_D} = \frac{C_d}{C_{\Sigma\_\mathrm{D}}} = (0.43 + 0.37)/(1 + 0.37) \cong 0.6$. Therefore, when V_{n+} becomes more negative, more electrons are induced on the Si SET island and its dimensions increase, resulting in a larger coupling between the defect and the Si SET island.

7.7 Switching of the defect occupancy

7.7.1 Gate voltage dependence

Another thing I want to discuss is the switching of the defect occupancy as a function of gate voltage. To simplify things, all the experiments in this section have the Al SET drain and source tied together. I do not extract the conductance information of the Al SET. The relative bias to induce the Si conducting channel is applied to the Al SET while the Si SET is grounded except for a small ac drive ($V_{ac} = 10\ \mu$V, $f = 42$ Hz). This ac drive is used to find the differential conductance of the Si SET. In another words, I am in the V_g-V_{Al} voltage space.

Figure 7.31(a) shows the differential conductance of the Si SET as a function of V_g and $V_{\rm Al}$, and Fig. 7.31(b) shows data from a fine sweep near one of the conductance splittings in Fig. 7.31(a). The white lines and the two Si SET conductance peak traces can be recognized as the boundaries for different charge configurations (n, 0), (n-1, 1), (n-1, 0), and (n, 1), similar to Fig. 7.28 except that the x-axis here is $V_{\rm Al} = -V_{n+}$.

Along one of the Si SET conductance peak trace, line B in Fig. 7.31(b), the Si SET island potential is kept constant by a combination of V_g and $V_{\rm Al}$ such that $\Delta V_g/\Delta V_{\rm Al} = -4$. However, the conductance changes its magnitude once it passes the boundary between (n, 0) and (n-1, 1) as shown in Fig. 7.32. The change is simply because the defect changes its occupancy from empty to occupied: Level 1 = G corresponds to the condition when the defect is empty and Level 0 = 0 corresponds to the condition when the defect is occupied; the intermediate Si SET conductance

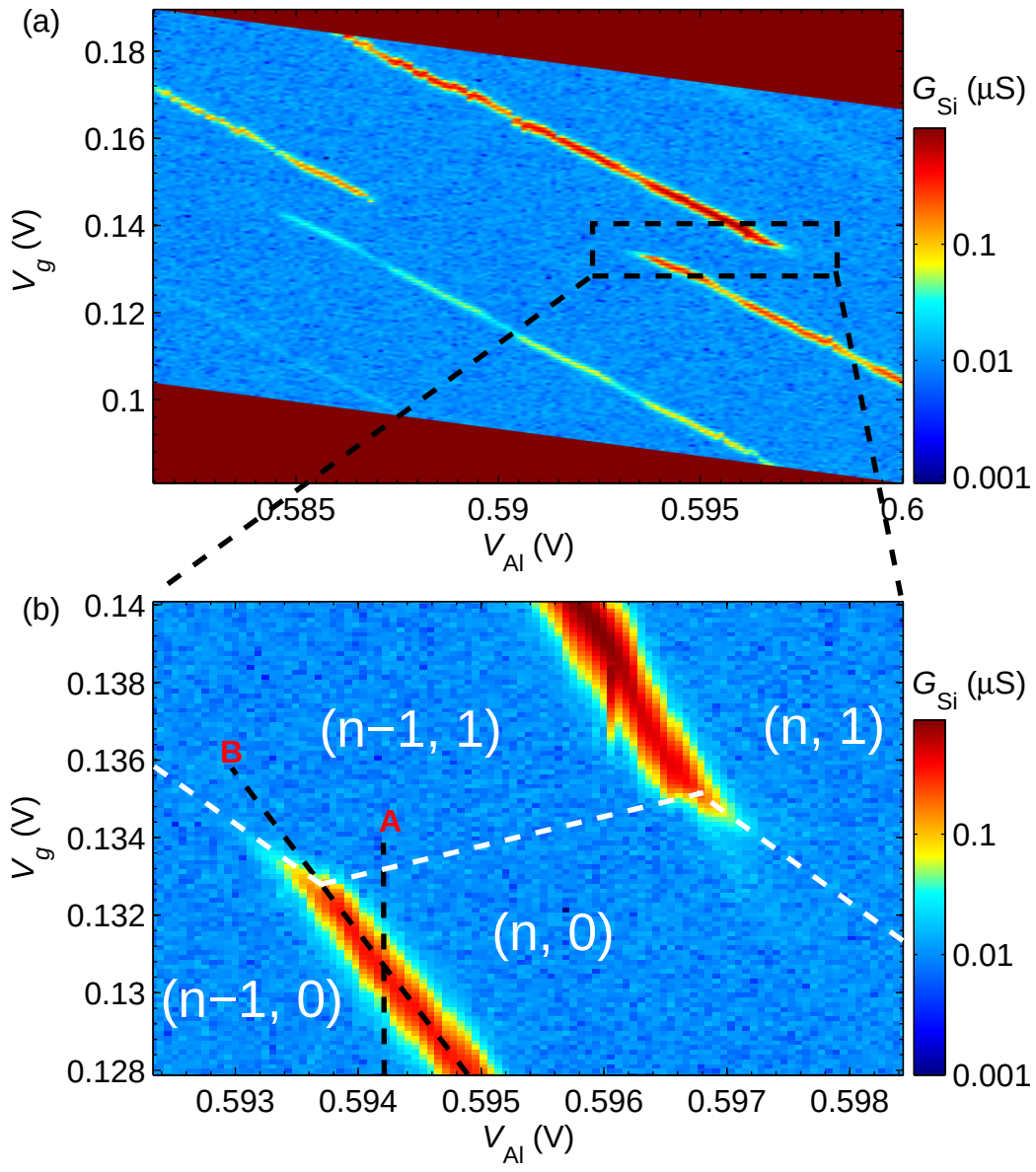


Figure 7.31: (a) Si SET conductance vs V_g and V_{Al}. The relative bias between the Al and Si SETs is applied to the Al SET in this case. (b) A fine sweep of the boxed region in (a). The white lines and the two Si SET conductance peak traces can be recognized as the boundaries for different charge configurations (n, 0), (n-1, 1), (n-1, 0), and (n, 1). Lines B and A are two sweep lines with data shown in Figs. 7.32 and 7.33 respectively.

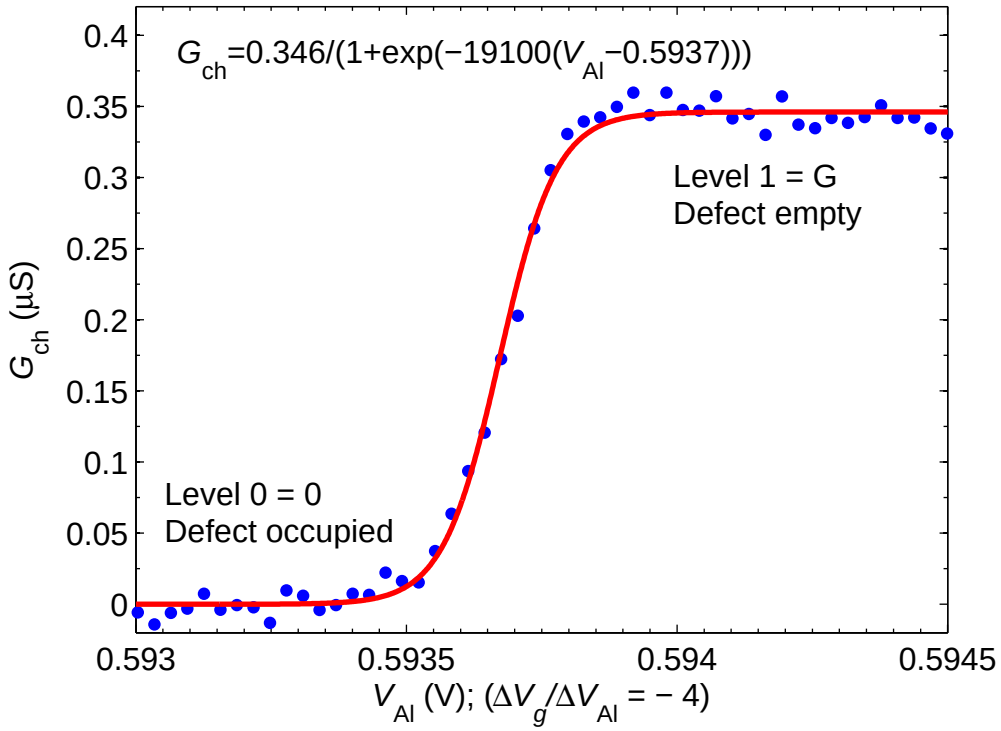


Figure 7.32: Si SET conductance change along line B in Fig. 7.31(b) along which $\Delta V_g/\Delta V_{\rm Al} = -4$. The magnitude of the conductance changes continuously from Level 1 = G (corresponding to an empty defect) to Level 0 = 0 (corresponding to an occupied defect). The red curve is a fit to Eq. 7.38 with the degeneracy factor $g = 1$.

corresponds to a defect state which is sometimes occupied and empty the rest of the time. No RTS near the Si SET conductance transition point is observed, which means that only the time averaged value is measured and the switching rate of the defect is much faster than the measurement bandwidth ($T_{constant}$ = 10 ms on the lock-in amplifier).

The probability of having an empty defect is:[66]

$$P_{empty} = 1/(1 + \frac{1}{g}\, e^{-(E_T - E_F)/k_B T}) \tag{7.36}$$

where E_T is the energy of the occupied defect site, E_F is the Fermi level, k_B is the Boltzmann constant, T is temperature, and g is the degeneracy factor. Because the coefficient in the exponential part is very big, as will be seen, g does not play a big role, so it will be set to 1 as a crude approximation. E_T can be tuned by V_g and V_{Al} through voltage conversion factors α and β respectively. Since only the change of E_T around E_F is important, Eq. 7.36 can be rewritten as:

$$\begin{aligned} P_{empty} &= 1/(1 + e^{(\alpha \Delta V_g + \beta \Delta V_{\mathrm{Al}})e/k_B T}) \\ &= 1/(1 + e^{(-4\alpha + \beta)\Delta V_{\mathrm{Al}} e/k_B T}) \end{aligned} \tag{7.37}$$

In the above equation, $\Delta V_g = -4\Delta V_{\mathrm{Al}}$ has been used, and ΔV_g and ΔV_{Al} are relative changes around Fermi level. So the time averaged Si SET conductance is:

$$G_{ch} = \mathrm{G}/(1 + e^{(-4\alpha + \beta)\Delta V_{\mathrm{Al}} e/k_B T}) \tag{7.38}$$

The red curve in Fig. 7.32 is a fit to Eq. 7.38, resulting in:

$$(-4\alpha + \beta)e/k_B T = -19100 \tag{7.39}$$

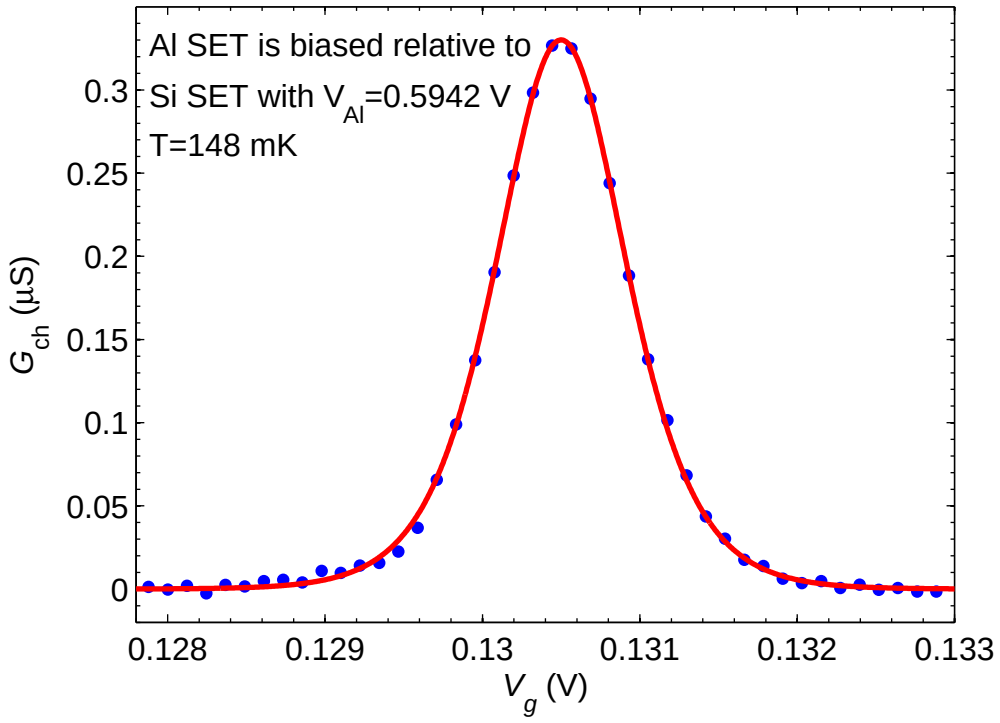


Figure 7.33: One of the Si SET conductance peaks as a function of V_g, measured along the vertical line A in Fig. 7.31(b) with $V_{\rm Al} = 0.5942$ V. The red curve is a fit to Eq. 7.40 with a channel electron temperature $T = 0.148$ K.

The temperature can be extracted as follows. Figure 7.33 shows one of the Si SET conductance peaks as a function of side gate voltage V_g along the vertical line A in Fig. 7.31(b). The red line is a fit according to the following equation:[102]

$$G = A/cosh^2(e\gamma(V_g - V_{g0})/2.5k_BT) \tag{7.40}$$

where V_{g0} is the peak center voltage; γ is the gate voltage conversion factor, $\gamma = C_{g\_\mathrm{Si}}/C_{\Sigma\_\mathrm{Si}} = 0.058$ based on Table 7.1. The extracted electron temperature is $T = 148$ mK, which is high compared to the base temperature, but remarkably low considering the difficulty of extracting heat from electron systems at mK temperature. One of many reasons could be noise on the twisted pairs which are used to bias the Si SET and are not very well filtered.

With the temperature known, I can use Eq. 7.39 to get $(-4\alpha + \beta) = -0.244$. Based on the electrostatic model and the results in Table 7.2, $\alpha = C_{g\_\mathrm{D}}/C_{\Sigma\_\mathrm{D}} = 0.105$ and $\beta = (C_e + C_h)/C_{\Sigma\_\mathrm{D}} = 0.141$, so $(-4\alpha + \beta) = -0.279$ which is in reasonable agreement.

7.7.2 Tunneling rate

In Fig. 7.29, I showed that when the relative bias V_{n+} is large (more negative with more carriers in the channel), there is no hysteresis in the switching of the defect occupancy within our measurement bandwidth (about 1 Hz). In contrast, when V_{n+} is small (less negative) there is hysteresis based on the Al SET response. Consequently the tunneling rate depends on the conductance of the channel. In Sec. 7.7.1, I showed that within our bandwidth (about 16 Hz) only the time averaged

occupancy is observed. Without exact knowledge of the defect and its location, it would be very difficult to calculate the tunneling rate. In reference [103], Calderón *et al*. studied a phosphorus electron tunneling from the donor site in the Si substrate to the Si/SiO_2 interface. In that case, the tunnel barrier height was the bonding energy of the phosphorus atom (about 46 meV) and their calculation showed that the tunneling time was nearly an exponential function of the distance d between the donor site and the interface. At $d = 20$ nm, the tunneling time was a few tens of picoseconds, while for $d = 30$ nm the tunneling time was about 1 ns. For my case, the defect is about 20 nm away from the Si channel, a comparable fast tunneling rate is expected.

7.8 Conclusions

In this chapter, I first argued for the self-alignment of the Al/Si SET system based on comparing my measured results to the electrostatic model I described in Chap. 6. I studied a single charge defect using this vertically coupled Al/Si SET system. After ruling out the possibility of a TLF, I argued that the defect has to be tunnel-coupled to the Si SET. Using a simplified two-dot model that neglected the quantization of charge on the Al SET island, I extracted the capacitances in percentages associated with the defect. However, it was difficult to get a precise value of the absolute capacitance of the defect because only one electron was involved and the model behavior depended weakly on the absolute capacitance of the defect. The results nevertheless revealed that the defect size is small, corresponding to a

sphere with a radius on the order of 1 nm. Based on the big difference between the defect coupling capacitance to the Si SET and to the side gate, I estimated the defect is about 20 nm away from the Si channel, much closer than to the side gate. Without exact knowledge of the defect, it is impossible to calculate the tunneling rate. However a reasonably fast rate is expected based on the 20 nm tunneling distance. The defect occupancy was studied as a function of voltage and it showed linearity, which means the coupling capacitances of the defect to the Al SET and to the side gate are nearly bias independent. Based on the evolution of the charge signal amplitude in both the Al and Si SETs, the coupling capacitance between the defect and the Si SET island increases dramatically with more carriers on the Si SET island. Finally, a study of the switching of the defect occupancy by the Si SET showed good agreement with the coupling capacitance results in Table 7.2.

Chapter 8

Design of a metallic SET gated by lateral Schottky gates for measurement of the field ionization of single donors in Si

8.1 Overview

As mentioned in Chap. 1, my main motivation in this work was to detect the charge motion of single donor electrons between donor sites and the Si/SiO_2 interface. Although these early experiments were not successful, they led me to examine the channel devices discussed in previous chapters. In this chapter, I discuss one of these early experiments in which I used an Al SET gated by lateral PtSi Schottky gates to measure field ionization of single donors in silicon.

8.2 Introduction

Detection and control of charge motion at the level of individual dopant atoms is attractive not only for future atomic scale devices,[104] but also for Si-based quantum computers.[104] For example, in Kane's architecture [10] quantum information is encoded into the nuclear spin state of individual P^{31} impurities. Both single- and two-qubit operations would require the precise manipulation and measurement of the positions of the donor electrons. Therefore the dynamics of donor electrons must be well understood before any quantum logic operation could be performed.

Of particular importance is the motion of a single electron between a donor site and a nearby Si/SiO_2 interface under an applied electric field (see Fig. 8.1). In principle, a highly sensitive electrometer such as an SET (charge sensitivity $\sim 10^{-5}$ e/$\sqrt{Hz}$) should make the detection of such charge motion possible, provided that the dopant is located close enough to the SET island.

Detection of single charges is also of particular importance for single spin measurement. Many proposals [7, 9, 10, 16, 22, 23, 24] for spin qubits in semiconductors incorporate spin-charge conversion to measure the final spin states, because detection of charges is in general much easier and faster than direct detection of spins. For example, there has been tremendous experimental progress,[105, 106] for single-shot read-out of a single electron spin in a GaAs/AlGaAs quantum dot by detecting spin-dependent electron tunneling. One proposed method [16] for making a spin measurement in Si incorporates electric-field-dependent ionization of two-electron systems to distinguish between singlet and triplet spin states. Provided that one of the two electrons was in a known spin state, the spin of the other electron could then be determined.

It has been shown theoretically for a system as depicted in Fig. 8.1 that there exists a critical field above which a donor electron will ionize and move to a nearby Si/SiO_2 interface.[103] This critical field is approximately inversely proportional to the depth d of the donor below the interface, and for d $\cong$ 30 nm the field is $\cong$ 15 kV/cm.[103] One experimental challenge facing the measurement of this field ionization is the realization of a gate capable of applying such a large electric field with as little uncertainty as possible and without leakage.

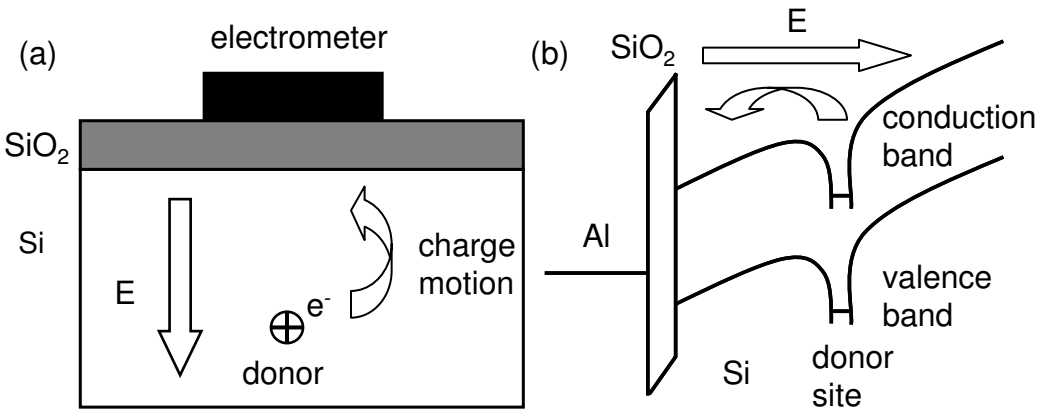


Figure 8.1: (a) Schematic showing a single donor in Si with a highly sensitive electrometer, such as an SET, aligned directly above. The electron can shuttle between the donor site and the Si/SiO_2 interface under an applied electric field E as shown by the arrow. The charge motion can be detected by the highly sensitive electrometer. (b) Band diagram of the situation in (a). The dips in conduction band and valence band of Si represent the Coulomb potential at the donor site.

Such an electric field could in principle be applied by a heavily doped back gate created via ion implantation or by molecular beam epitaxial (MBE) growth. A back gate is appealing because its electric field is relatively uniform in the lateral direction, making the electrostatics of the device easier to model and understand. However, sharp density profiles are difficult to obtain using either of these fabrication techniques. In order to obtain a metallic layer which conducts at low temperature, the peak dopant density must be larger than the metal-insulator transition ($3.45 \times 10^{18}/\mathrm{cm}^3$). High density ion implantation into a pure Si substrate can create such a conducting layer about 1 μm below the surface.[77] However, straggle during the ion implantation introduces extra impurities near the Si/SiO_2 interface with a non-negligible density. Implantation also introduces lattice damage that may not be thoroughly repaired even in a subsequent high temperature anneal. This problem could perhaps be overcome by growing a layer of intrinsic Si expitaxially on a heavily doped substrate. However, dopant migration toward the surface during the epitaxial growth, as well as diffusion during the subsequent high temperature thermal oxidation, both make the transition from a conducting layer to an intrinsic layer far from ideal. For both of these back gate possibilities, extra impurities between the heavily doped region and the Si/SiO_2 interface introduce a large uncertainty into the applied electric field in the substrate.

In this chapter I describe a different approach, the use of lateral Schottky gates to apply the electric field required to ionize donor electrons close to a nearby Si/SiO_2 interface. This situation is depicted in Fig. 8.2. Compared with a metallic gate on top of SiO_2 which gives a 3.2 eV barrier height, a PtSi Schottky gate has a 0.85 eV

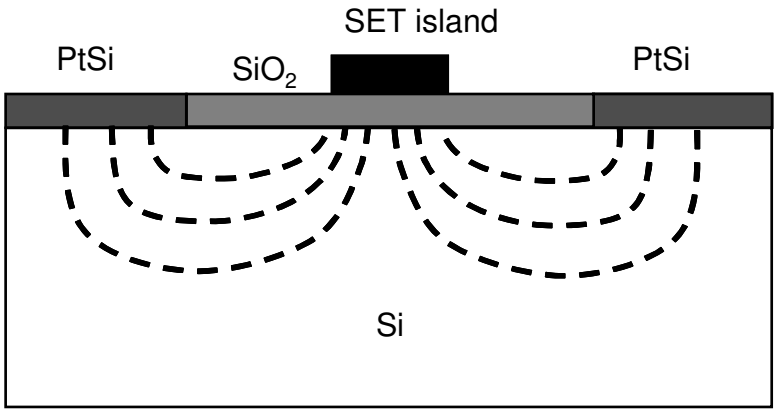


Figure 8.2: Schematic of an Al/AlO_x/Al SET on an oxidized Si substrate that is gated by lateral PtSi Schottky gates. Dashed lines represent the electric field lines.

barrier for electrons and a 0.27 eV barrier for holes . This suggests that either electrons or holes can be injected under appropriate bias and made to accumulate at the Si/SiO_2 interface. Such a technique would be valuable because it could be used to populate or depopulate dilute donors in the substrate. Because PtSi is grown at much lower temperature (just above 300°C) [107] than typical for MBE growth, a Schottky gate should make the transition from conducting layer to intrinsic Si far more abrupt than would a heavily doped back gate, minimizing unwanted impurities. Here I measure and characterize the electric field applied via a Schottky gate using an SET on a nominally undoped Si substrate. I also demonstrate the injection of electrons and holes from the gate.

8.3 Fabrication

Device fabrication starts from a nearly intrinsic Si (100) wafer with nominal resistivity $\rho > 10,000\ \Omega$ cm. It is oxidized in a tube furnace at 950°C for 30 minutes to a thickness of about 25 nm. Photolithography and RIE are used to define alignment marks that are used in subsequent photolithography steps. A second photolithography step is then used to pattern Schottky gates. The sample is dipped in HF to expose the Si, followed immediately by deposition of 25 nm of Pt in an electron-beam evaporator. I choose this thickness of Pt to be the same as that of the SiO_2 to make the overall surface flat for subsequent resist coating.

Following the Pt deposition, e-beam lithography and self-aligned double-angle evaporation are used to make the SET.[64] The SET island is aligned $\cong 4.5\ \mu$m away from the edge of the gate and contacts the substrate with an area $\cong$ (70 nm $\times$ 80 nm). A recipe is used that combines the photolithography for the leads and bond pads and the e-beam lithography for the SET itself into a single Al evaporation step. This is essential to avoid eutectic formation between different metals during subsequent annealing steps.

The final step is a 425°C forming gas anneal that serves three purposes: creating the PtSi, passivating dangling bonds at the Si/SiO_2 interface, and repairing any remaining damage.

8.4 Schematic and model of the measurement

The experiments are performed in an Oxford dilution refrigerator with base temperature around 20 mK. This temperature is well below the approximate 2 K charging energy of the SET, so the device operates within the Coulomb blockade regime. A 1 T magnetic field is applied to keep the SET in the normal state.

The SET is dc biased with a fixed drain-source voltage $V_{\rm ds}$, and the drain-source current $I_{\rm ds}$ is recorded using a room temperature trans-impedance amplifier while the potential V_g on the Schottky gate is swept slowly.

Gate bias voltages V_g can be divided into three regimes (see Fig. 8.3). First, if V_g is not large enough for carriers to tunnel across the Schottky barrier, the Schottky gate will only weakly modulate the SET from the electrostatics. In this case the Coulomb blockade period should be large, about 1.2 V/e based on finite element analysis of the sample geometry using the FEMLAB physics modeling package. Second, if V_g is negative enough, electrons on the gate will tunnel across the Schottky barrier and accumulate at the Si/SiO_2 interface. Conversely, for positive enough V_g, holes will tunnel and accumulate at the interface. For these last two cases, the modulation of the SET is dominated by the capacitance between the SET island and the Si/SiO_2 interface which gives a much stronger coupling than in the first case, and the Coulomb blockade period should be corresponding smaller, $\cong$ 20 mV/e.

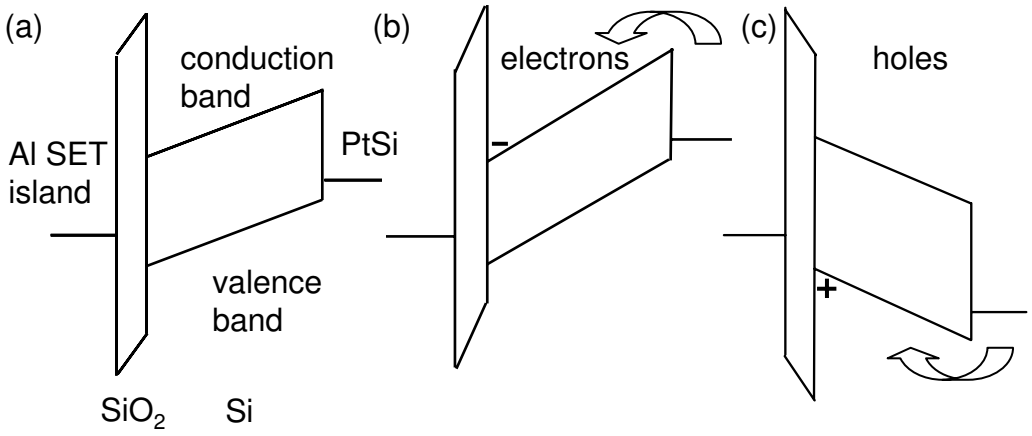


Figure 8.3: Band diagrams relevant for a PtSi Schottky gate near an Aluminum conductor on an oxidized Si substrate. (a) No carriers leak into the substrate for small V_g. (b) For large negative V_g, electrons are injected from the Schottky gate and accumulate at the Si/SiO_2 interface. (c) For large positive V_g, holes are injected from the Schottky gate and accumulate at the Si/SiO_2 interface. In cases (b) and (c), the electrostatic coupling to the SET island is much stronger than in case (a), which will be reflected in measurements of the corresponding Coulomb blockade period.

8.5 Data and discussion

Figure 8.4 shows a typical I_{ds}–V_g curve with V_g swept in opposite directions. The Coulomb blockade peaks are almost uniform over a 12 V range with a period $\cong$ 1.2 V/e, agreeing well with our simulations. More importantly, the sweeps back and forth almost track each other, with the biggest offset only 18% of 1 e period.

Counting Coulomb blockade oscillations can be considered a measure of the change of the electric field right beneath the SET island, because the electric field depends on the charge density on the island, and every period means one more electron is added to or removed from the island. Based on the FEMLAB simulations of our SET geometry, every period corresponds to a change of electric field 2 kV/cm underneath the island. Therefore, 18% of 1 e corresponds to an absolute electric field difference $\cong$ 0.36 kV/cm, or an uncertainty of about 2% at a field of 15 kV/cm. This means that the electric field under the SET island depends almost entirely on V_g, with minimal hysteresis.

Figure 8.5 shows that as V_g is decreased even further to -16 V, there is a sudden change in the Coulomb blockade period corresponding to accumulation of electrons at the interface. Figure 8.5(b) is a subset of the data in Fig. 8.5(a) with a Coulomb blockade period $\cong$ 20 mV/e. The period is small because the gate capacitance becomes large when electrons accumulate at the Si/SiO_2 interface.

At positive V_g there is similar behavior for holes, but at a much lower voltage magnitude (1.935 V) because of the lower Schottky barrier height for holes. Figure 8.6 shows data for the accumulation of holes.

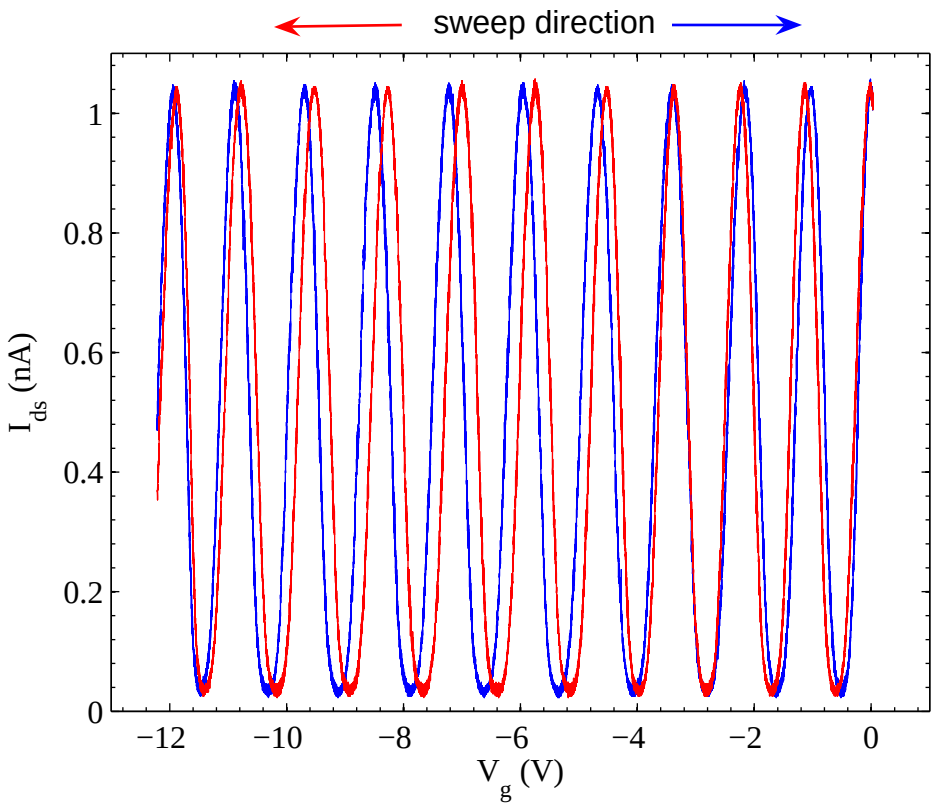


Figure 8.4: Typical $I_{\rm ds}$–V_g curve with Schottky gate V_g swept back and forth over a wide range. The almost uniform Coulomb blockade period $\cong$ 1.2 V/e agrees well with our simulations. Back and forth sweeps have at most an offset 18% of 1 e period, corresponding to an electric field difference $\cong$ 0.36 kV/cm. For a 15 kV/cm field, this offset gives only about 2% uncertainty.

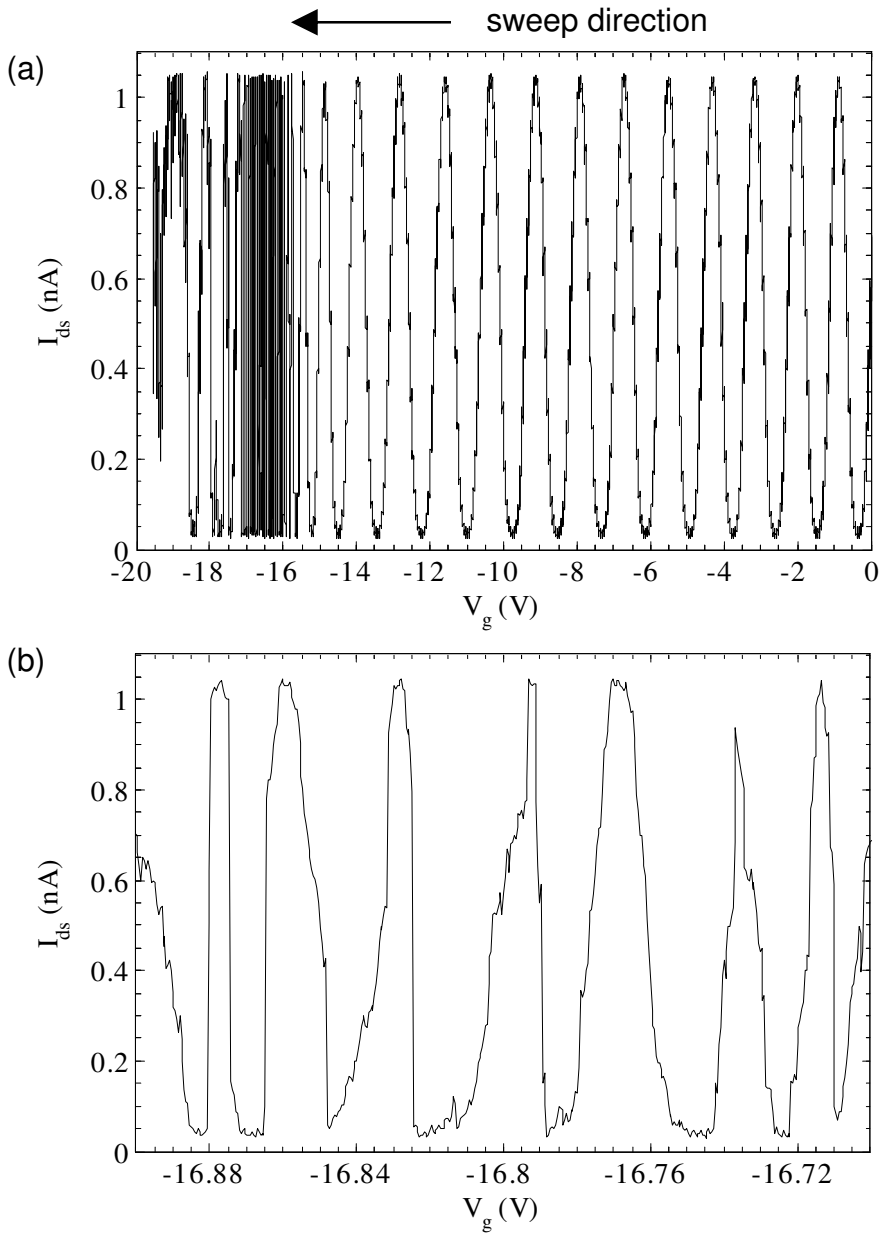


Figure 8.5: (a) $I_{\rm ds}$ versus V_g. There is a sudden change in the Coulomb blockade period at V_g = -16 V that corresponds to accumulation of electrons at the interface. (b) Subset of the data in (a) near $V_g = -16.8$ V showing a Coulomb blockade period $\cong$ 20 mV/e because of the large gate capacitance in the case of accumulation.

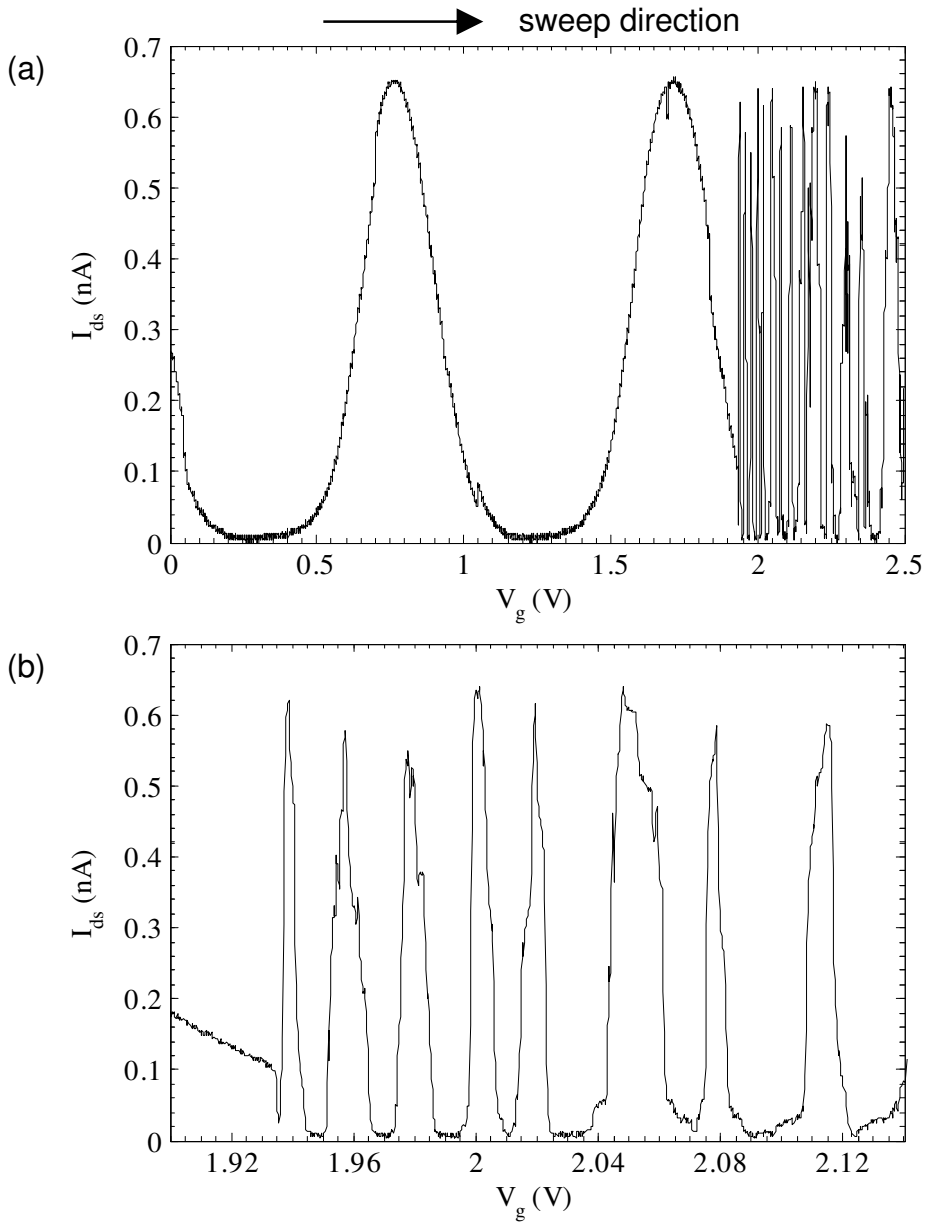


Figure 8.6: (a) $I_{\rm ds}$ versus V_g. There is a sudden change in the Coulomb blockade period at $V_g = 1.935$ V that corresponds to accumulation of holes at the interface. (b) Subset of the data in (a) near $V_g = 2.0$ V showing a Coulomb blockade period $\cong 20$ mV/e because of the large gate capacitance in the case of accumulation.

Counting Coulomb blockade peaks can only tell us about changes in electric field from one gate voltage to the next. To determine the absolute value of the electric field requires that its value be known for at least one reference value of V_g. The flat band voltage (the voltage at which there is no electric field in the substrate) can be used as a reference point for determination of the absolute electric field strength. However, due to work function differences between Si and the metal gate, interface states at the Si/SiO_2 interface, fixed oxide charges, oxide trapped charges, *etc.*, the flat band will in general be shifted away from $V_g = 0$.

To determine the flat band voltage, I first flood the Si/SiO_2 interface with holes by applying $V_g = 4.0$ V; this voltage is higher than that required for holes to tunnel. Then I lower V_g to remove the holes from the interface. The voltage when the last hole leaves the interface corresponds to the flat band voltage and can be determined by a sudden change in the Coulomb blockade period. Figure 8.7 shows my data for the determination of the flat band voltage, which occurs near $V_g =$ 0.5 V for this device. The change of the Coulomb blockade period in Fig. 8.7 is not as dramatic as seen in Figs. 8.5 and 8.6, for reasons that are not yet understood. One possibility for the discrepancy is interface states.

I note that a field of $\cong$ 15 kV/cm corresponds to $\cong$ 10 V below the flat band voltage. In Fig. 8.5(a) at V_g = -9.5 V, there is no injection of electrons from the Schottky gate. Therefore, there is at least $\cong$ 6.5 V or $\cong$ 11 kV/cm electric field margin before electrons leak from the gate.

One problem with this device is the lateral leakage of carriers along the SET leads all the way out to the bond pads where the oxide layer was broken during

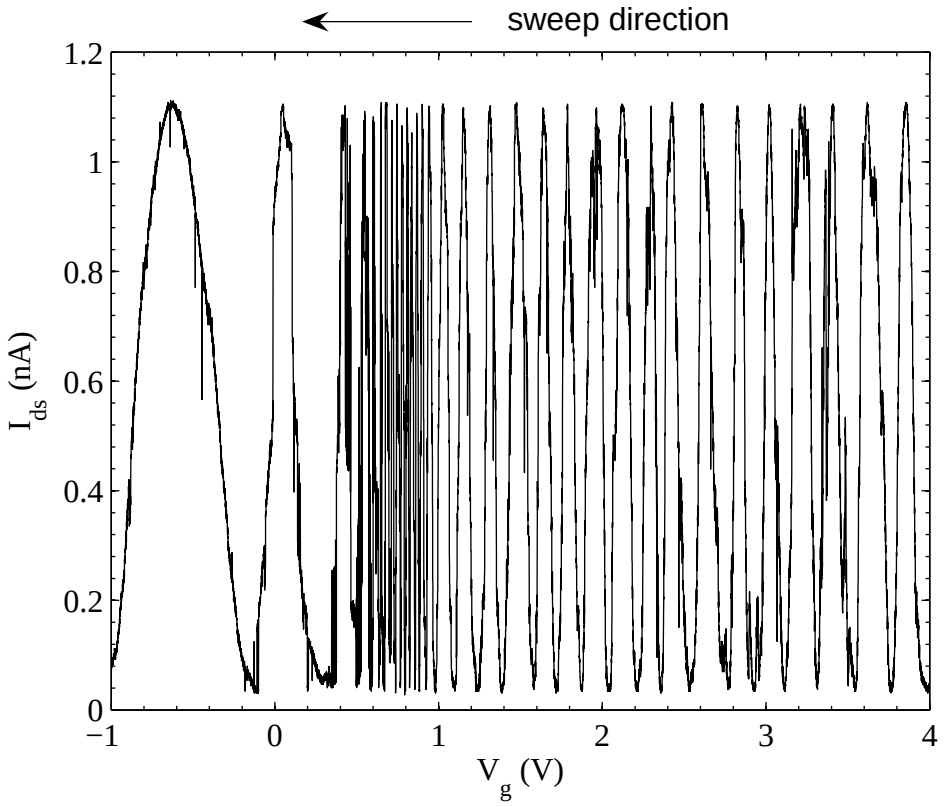


Figure 8.7: Determination of the flat band voltage, corresponding to the voltage when the last hole leaves the interface as V_g is decreased. This can be determined by the sudden change of Coulomb blockade period occurring near $V_g = 0.5$ V.

wire bonding. This is reflected in the Coulomb blockade period. For $V_g < -17$ V in Fig. 8.5, $V_g > 2.5$ V in Fig. 8.6, and $V_g > 1.0$ V in Fig. 8.7, the Coulomb blockade period is between the large ($\cong$ 1.2 V/e) and the small ($\cong$ 20 mV/e) ones. This can be explained by the effective voltage divider from the lateral leakage resistance in series with the Schottky gate resistance. Additional effort would be required to eliminate this leakage path such that a controllable number of carriers accumulate under the SET.

8.6 Conclusions

I fabricated an Al SET that is gated by a lateral PtSi Schottky gate. By studying the Coulomb blockade period while sweeping the gate, I identified the flat band voltage and the accumulation of carriers, both electrons and holes, at the Si/SiO_2 interface under the SET island. I also demonstrated that the Schottky gate can create a well defined electric field in the substrate. PtSi Schottky gates provide a large enough barrier to apply the electric field required to ionize single donors $\cong$ 30 nm below the Si/SiO_2 interface without leaking. These results are promising for measurement of the field ionization of single donors in Si, a cornerstone of Si-based quantum computation and single spin measurement.

Chapter 9

Future work and summary

9.1 Future work

Although I have been able to understand some properties of the defect, its exact nature is still unclear at this point. To fully understand the defect, more experiments would need to be done. I will now list a few experiments that I think would be very interesting to carry out.

If the system is carefully biased such that the defect is at the transition point of occupied/unoccupied, RTS on both SET conductances should be observed, provided that both SETs are measured with high enough bandwidth. The lifetime of the defect at occupied or unoccupied states ($\tau_{occupied}/\tau_{unoccupied}$) as a function of gate voltage or temperature would be very helpful to understand the nature of the defect. For example, the temperature dependence of $\tau_{occupied}/\tau_{unoccupied}$ can provide an energy scale of the defect.

Another knob that I can turn is the magnetic field. With a magnetic field, the Zeeman splitting will shift the defect transition point in voltage space. The shift to a higher or lower gate voltage can give us information about the defect transition: whether it is between $1e^-$ and $2e^-$ or between $0e^-$ and $1e^-$,[62, 80, 81] because for a single electron, the lower Zeeman level will decrease as magnetic field increases, in contrast to a two-electron system. As suggested by reference [81], a

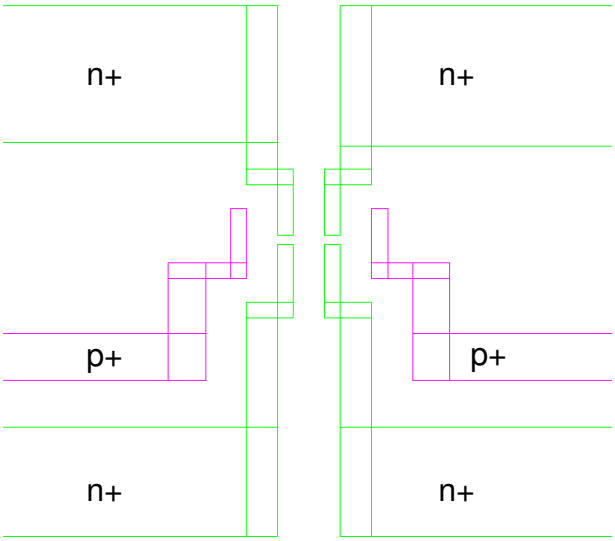


Figure 9.1: Implantation pattern for four-terminal measurement.

more complicated ESR experiment could possibly be performed to obtain the energy spectrum.

Possible improvements

All my conductance measurements on the Si SET were based on a two-terminal measurement. The sensitivity could be improved by doing a four-terminal measurement. This can be easily realized by redesigning the phosphorus implantation pattern to add another pair of n+ contact leads in parallel with the current one, as depicted in Fig. 9.1 [compare to Fig. 4.2(b)].

Other possible experiments: Donors & Kondo effect

It is likely that I was observing a single charge trap at the Si/SiO_2 interface, not a donor in the substrate. But I can intentionally implant phosphorus donors in this system, say under the SET island or between the side gate and the SET island. In that case, under an external electric field I should be able to observe the tunneling of donor electrons to the Si SET. This experiment requires relatively precise alignment between the implanted donor sites and the SET, but can be done within a few tens of nanometers by careful alignment between e-beam lithographies.

The Kondo effect, a well-studied phenomena in condensed-matter physics, initially described a spin-flip process of a magnetic impurity interacting with conduction electrons.[108] This idea has been generalized to a single quantum dot [109] and electrostatically coupled double quantum dots.[84, 85] For a single quantum dot, the system resembles a magnetic impurity if there are an odd number of electrons on the dot (total spin is up or down). In electrostatically coupled quantum dots under certain bias conditions as seen in Fig. 6.9, an electron will be energetically favorable on either the first or the second SET island, representing the pseudo-spin states.[84, 85] The Kondo effect has already been observed on electrostatically coupled double quantum dots in reference [85]. My system is similar to theirs and similar effects may be visible. If the coupling between the two SET islands needs to be stronger, the SiO_2 layer (currently 20 nm) can be thinned to a few nanometers such that both SETs are strongly coupled to each other.

9.2 Summary

One of the key issues that I want to address in our group is to determine the SETs utility for single charge and spin measurement in silicon, a necessary first step toward a future Si-based quantum computer. However from my early results, it is apparent that our charge detection scheme is limited by intrinsic background charge noise associated with the Si/SiO_2 system. This noise mechanism may also cause decoherence in qubits and gate errors for a Si-based quantum computer, as discussed in Chap. 3. In Chap. 8, I discussed one of the approaches that I have tried for detection of single donor ionization. I demonstrated that a lateral PtSi Schottky gate can create a well defined and large enough electric field in the substrate to ionize single donors without leaking.

To better understand these background charges, I designed a MOSFET incorporating an Al SET as the top gate to monitor charging of a Si channel during relative biasing. Near the channel conductance threshold, I observed Coulomb blockade oscillations, indicating the formation of a Si SET at the Si/SiO_2 interface. The tunnel barriers of the Si SET were due to potential fluctuations in the Si conducting channel, presumably lateral constrictions or potential bumps associated with the Al SET, because the same behavior has been observed in all three devices I fabricated. In Chap. 6, I showed that the Si SET was vertically aligned with the Al SET by comparing my data to results from a simple electrostatic model based on two capacitively coupled quantum dots. The inter-island capacitance was found to be about 1/3 of the total capacitance of the Si SET island, indicating that the Si SET was

strongly coupled to the Al SET.

This SET sandwich architecture was then used to characterize a MOS structure at low temperature via a cross-correlation measurement between the two SETs, as discussed in Chap. 7. I observed a defect, which I attributed to a single charge due to the fact that charge motion associated with only one charge transfer was detected by both SETs over a large range of applied voltage. After ruling out the possibility of a TLF in the system based on the responses of the two SETs, I demonstrated that the defect appeared to be tunnel-coupled to the Si SET. Based on a simplified electrostatic model of two dots, I extracted the defect capacitances in the model in terms of percentages of the total capacitance of the defect. However, it was difficult to get precise values of the absolute capacitances, because only one electron transfer was involved. Some other properties of the defect were also found, *e.g.* the transition position when the defect changed its occupancy and the evolution of the coupling strengths of the defect to both SETs.

The main properties of the defect are as follows:

1) A single charge defect.

2) Tunnel-coupled to the Si SET.

3) Size is small: on the order of 1 nm.

4) About 20 nm away from the channel, much closer than to the side gate.

5) A single donor in the Si substrate or a single charge trap at the Si/SiO_2 interface.

If the defect were a single donor in silicon, it could bind a second electron to form a D^- state, as discussed in Chap. 3. However, the binding energy is very small

(about 2 mV). In my experiment, I did not see charging associated with this second electron. This probably can help me rule out the case of a single donor in the Si substrate.

Appendix A

Error propagation

Error propagation is well developed. For example, detailed discussion of Secs. A.1 and A.2 can be found in references [110] and [111] respectively. Here, I summarize the key results.

A.1 General error propagation

If q is a function of x_1, x_2, $\cdots$, x_i, q=$q(x_1, x_2, \cdots, x_i)$ and each x_i has its own uncertainty σ_i. Then the uncertainty in q is:

$$\sigma_q = \sqrt{(\frac{\partial q}{\partial x_1}\sigma_1)^2 + (\frac{\partial q}{\partial x_2}\sigma_2)^2 + \cdots + (\frac{\partial q}{\partial x_i}\sigma_i)^2} \tag{A.1}$$

if all the x's are independent variables and their uncertainties are random. However, if the x's are not independent, but **interdependent** variables, the above error equation does not hold. In this case, the covariance between x's must be included in the error propagation. For the simplest case, $q_i = q(x_i, y_i)$ is only a function of x and y, which are **interdependent**. Let (x_i, y_i) be N pairs of measured data. Then the uncertainty in q is:

$$\sigma_q = \sqrt{(\frac{\partial q}{\partial x}\sigma_x)^2 + (\frac{\partial q}{\partial y}\sigma_y)^2 + 2\frac{\partial q}{\partial x}\frac{\partial q}{\partial y}\sigma_{xy}} \tag{A.2}$$

where σ_{xy} is the covariance of x and y, and is defined as:

$$\sigma_{xy} = \frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})(y_i - \bar{y}) \tag{A.3}$$

If x and y are independent, σ_{xy} will be zero, and Eq. A.2 will be reduced to Eq. A.1. Equation A.2 can be written in matrix form:

$$\sigma_q^2 = \begin{pmatrix} \frac{\partial q}{\partial x} & \frac{\partial q}{\partial y} \end{pmatrix} \begin{pmatrix} \sigma_x^2 & \sigma_{xy} \\ \sigma_{xy} & \sigma_y^2 \end{pmatrix} \begin{pmatrix} \frac{\partial q}{\partial x} \\ \frac{\partial q}{\partial y} \end{pmatrix} \tag{A.4}$$

The general form for the uncertainty of q=$q(x_1, x_2, \cdots, x_i)$ would be:

$$\sigma_q^2 = \sum_i (\frac{\partial q}{\partial x_i}\sigma_i)^2 + 2\sum_i \sum_{j \neq i} \frac{\partial q}{\partial x_i}\frac{\partial q}{\partial x_j}\sigma_{ij} \tag{A.5}$$

A.2 Uncertainty of the intersection of two fitted lines

Suppose that there are two sets of data (x_{1i}, y_{1i})(N points) and (x_{2i}, y_{2i})(M points), which are linearly fitted with two lines $y = a + bx$, and $y = c + dx$. Note, a and b are **interdependent** variables, and so are c and d. Also, a and b are totally independent of c and d. The coordinate of the intersection can be calculated easily:

$$x_0 = (c - a)/(b - d) \tag{A.6}$$

$$y_0 = (bc - ad)/(b - d) \tag{A.7}$$

The values and variances of a and b can be calculated from the original data set (x_{1i}, y_{1i}). The results can be found in any textbooks on linear regression.[110, 111] The explicit results are:

$$a = ((\sum_i x_{1i}^2)(\sum_i y_{1i}) - (\sum_i x_{1i}) \sum_i (x_{1i}y_{1i}))/D_1 \tag{A.8}$$

$$b = (N(\sum_i x_{1i}y_{1i}) - (\sum_i x_{1i})(\sum_i y_{1i}))/D_1 \tag{A.9}$$

where

$$D_1 = N(\sum_i x_{1i}^2) - (\sum_i x_{1i})^2 = N\sum_i (x_{1i} - \bar{x_1})^2 \tag{A.10}$$

If (x_{1i}, y_{1i}) can be described by a linear function in theory, $y = a + bx$ is the best fit to that function, and all the y_{1i}'s have the same uncertainty, then the uncertainty in y_1 should be equal to:

$$\sigma_{y1}^2 = \sum_i (y_{1i} - a - bx_{1i})^2/(N-2) \tag{A.11}$$

Based on Eqs. A.8 and A.9 and the general error propagation formula Eq. A.1 (because all $(x_{1i},\ y_{1i})$ are independent to each other), it is easy to calculate the variances of a and b assuming all y_{1i} have the same uncertainty σ_{y1} as defined in Eq. A.11:

$$\sigma_a^2 = \sigma_{y1}^2(\sum_i x_{1i}^2)/D_1 \tag{A.12}$$

$$\sigma_b^2 = \sigma_{y1}^2 N/D_1 \tag{A.13}$$

Similarly, c and d and their uncertainties for data set (x_{2i}, y_{2i}) can be calculated as:

$$c = ((\sum_i x_{2i}^2)(\sum_i y_{2i}) - (\sum_i x_{2i})(\sum_i x_{2i}y_{2i}))/D_2 \tag{A.14}$$

$$d = (M(\sum_i x_{2i}y_{2i}) - (\sum_i x_{2i})(\sum_i y_{2i}))/D_2 \tag{A.15}$$

$$\sigma_c^2 = \sigma_{y2}^2 \sum_i x_{2i}^2/D_2 \tag{A.16}$$

$$\sigma_d^2 = \sigma_{y2}^2 M/D_2 \tag{A.17}$$

where

$$D_2 = M(\sum_i x_{2i}^2) - (\sum_i x_{2i})^2 = M\sum_i (x_{2i} - \bar{x_2})^2 \tag{A.18}$$

In general, in linear regression the slope and intercept are not independent but **interdependent**. However, the calculation of the covariance between a and b, or c and d is not that trivial to me and needs ensemble theory. I will deduce how to calculate it in Sec. A.3. Here I just write down the explicit forms which look very simple:

$$\sigma_{ab} = \sigma_{ba} = -\sigma_a^2(\sum_i x_{1i})/(\sum_i x_{1i}^2) = -\sigma_b^2(\sum_i x_{1i})/N \tag{A.19}$$

$$\sigma_{cd} = \sigma_{dc} = -\sigma_c^2(\sum_i x_{2i})/(\sum_i x_{2i}^2) = -\sigma_d^2(\sum_i x_{2i})/M \tag{A.20}$$

Because a and b are independent of c and d, the covariances σ_{ac}, σ_{ad}, σ_{bc} and σ_{bd} are all zero.

Finally, we can calculate the uncertainty of the intersection (x_0, y_0) based on Eq. A.5:

$$\sigma_{x0}^2 = \begin{pmatrix} \frac{\partial x_0}{\partial a} & \frac{\partial x_0}{\partial b} & \frac{\partial x_0}{\partial c} & \frac{\partial x_0}{\partial d} \end{pmatrix} \begin{pmatrix} \sigma_a^2 & \sigma_{ab} & 0 & 0 \\ \sigma_{ba} & \sigma_b^2 & 0 & 0 \\ 0 & 0 & \sigma_c^2 & \sigma_{cd} \\ 0 & 0 & \sigma_{dc} & \sigma_d^2 \end{pmatrix} \begin{pmatrix} \frac{\partial x_0}{\partial a} \\ \frac{\partial x_0}{\partial b} \\ \frac{\partial x_0}{\partial c} \\ \frac{\partial x_0}{\partial d} \end{pmatrix} \tag{A.21}$$

$$\sigma_{y0}^2 = \begin{pmatrix} \frac{\partial y_0}{\partial a} & \frac{\partial y_0}{\partial b} & \frac{\partial y_0}{\partial c} & \frac{\partial y_0}{\partial d} \end{pmatrix} \begin{pmatrix} \sigma_a^2 & \sigma_{ab} & 0 & 0 \\ \sigma_{ba} & \sigma_b^2 & 0 & 0 \\ 0 & 0 & \sigma_c^2 & \sigma_{cd} \\ 0 & 0 & \sigma_{dc} & \sigma_d^2 \end{pmatrix} \begin{pmatrix} \frac{\partial y_0}{\partial a} \\ \frac{\partial y_0}{\partial b} \\ \frac{\partial y_0}{\partial c} \\ \frac{\partial y_0}{\partial d} \end{pmatrix} \tag{A.22}$$

A.3 Deduction of covariance between intercept and slope

Equations A.19 and A.20 in Sec. A.2 look very simple, but I do not think the derivation is trivial. Perhaps there is an easy and direct way to get them, but I am not aware of a simple way to reach the same results.

The definition of covariance between the intercept a and the slope b is defined as in Eq. A.3:

$$\sigma_{ab} = \frac{1}{K}\sum_k (a^k - \bar{a})((b^k - \bar{b}) \tag{A.23}$$

where $\bar{a}$ and $\bar{b}$ are the least square results as defined in Eq. A.8 and A.9. Note in this section I will neglect the subscript 1 in all equations in the previous sections.

For each y_i, it can change by σ_y, which is the standard deviation of y. For N of y_i's, there can be many combinations of $y_i \pm \sigma_y$: $(y_1 \pm \sigma_y, y_2 \pm \sigma_y, \cdots, y_N \pm \sigma_y)$. Let k be one of the combination, for example $(y_1 + \sigma_y, y_2 - \sigma_y, \cdots, y_N + \sigma_y)$. For each combination, we can have a pair of a^k and b^k.

Since σ_y is small, a^k and b^k can be expanded to:

$$a^k = \bar{a} + \sum_i \frac{\partial \bar{a}}{\partial y_i}\delta y_i^k \tag{A.24}$$

$$b^k = \bar{b} + \sum_i \frac{\partial \bar{b}}{\partial y_i}\delta y_i^k \tag{A.25}$$

where $\delta y_i^k = \pm\sigma_y$ is for the k^{th} combination. Then:

$$\begin{aligned}
\sigma_{ab} &= \frac{1}{K}\sum_k(\sum_i \frac{\partial \bar{a}}{\partial y_i}\delta y_i^k)(\sum_j \frac{\partial \bar{b}}{\partial y_i}\delta y_i^k) \\
&= \frac{1}{KD^2}\sum_k\sum_i((\Sigma x^2) - x_i(\Sigma x))\sum_j(Nx_j - (\Sigma x))\delta y_i^k \delta y_j^k \\
&= \frac{1}{KD^2}\sum_k\sum_i\sum_j((\Sigma x^2) - x_i(\Sigma x))(Nx_j - (\Sigma x))\delta y_i^k \delta y_j^k \\
&= \frac{1}{KD^2}\sum_k\sum_i\sum_{j=i}((\Sigma x^2) - x_i(\Sigma x))(Nx_i - (\Sigma x))\delta y_i^k \delta y_i^k \\
&+ \frac{1}{KD^2}\sum_k\sum_i\sum_{j\neq i}((\Sigma x^2) - x_i(\Sigma x))(Nx_j - (\Sigma x))\delta y_i^k \delta y_j^k \qquad \text{(A.26)}
\end{aligned}$$

Since δy_i^k and δy_j^k are totally un-correlated, if we sum k first, the 2^{nd} term should be zero. Then Eq. A.26 becomes:

$$\begin{aligned}
\sigma_{ab} &= \frac{1}{KD^2}\sum_k\sum_i\sum_{j=i}((\Sigma x^2) - x_i(\Sigma x))(Nx_i - (\Sigma x))(\delta y_i^k)^2 \\
&= \frac{(\sigma_y)^2}{KD^2}\sum_k\sum_i((\Sigma x^2)Nx_i - (\Sigma x^2)(\Sigma x) - N(\Sigma x)x_i^2 + (\Sigma x)^2 x_i) \\
&= \frac{(\sigma_y)^2}{KD^2}\sum_k((\Sigma x^2)N(\Sigma x) - N(\Sigma x^2)(\Sigma x) - N(\Sigma x)(\Sigma x^2) + (\Sigma x)^2(\Sigma x)) \\
&= \frac{(\sigma_y)^2}{KD^2}\sum_k((\Sigma x)^2(\Sigma x) - N(\Sigma x)(\Sigma x^2)) \\
&= \frac{(\sigma_y)^2}{D^2}(\Sigma x)((\Sigma x)^2 - N(\Sigma x^2)) \\
&= -\frac{(\sigma_y)^2}{D}\Sigma x = -\frac{\sigma_b^2}{N}\Sigma x = -\sigma_a^2\frac{\Sigma x}{\Sigma x^2} \qquad \text{(A.27)}
\end{aligned}$$

which is exactly Eq. A.19. So σ_{ab} depends on Σx. If $\Sigma x = 0$, $\sigma_{ab} = 0$. This implies another simple way to calculate σ_{ab} – to center data such that $\Sigma x = 0$, in which case a and b will be independent, and Eq. A.1 should be used to calculate error propagation.

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