ABSTRACT

Title of dissertation: CMOS N-DIMENSIONAL M-LEVEL HYSTERESIS CIRCUITS AND POSSIBLE APPLICATIONS

Yu Jiang, Doctor of Philosophy, 2007

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Computer Engineering

Hysteresis is a natural phenomenon existing in many systems. Binary hysteresis is the simplest yet important model to study electronically generated hysteresis. Binary hysteresis circuits, the Schmitt trigger being an example, are widely used in reducing noise sensitivity, designing oscillators, generating chaotic signals, etc. A new concept, n-dimensional m-level multi-cell hysteresis is presented. A group of CMOS binary hysteresis circuits with full control which operate in all four quadrants is introduced. CMOS circuits, that give various one-dimensional multi-level hysteresis, in both current mode and voltage mode, are presented. Various combinations of adding forward and reverse binary hysteresis are demonstrated. CMOS circuits, in both current mode and voltage mode, that give two-dimensional multi-level multi-cell hysteresis, are designed. Further discussion is given on how to extend the results to more dimensions. Two-dimensional hysteresis is used to generate chaotic signals. A couple of areas where multi-cell hysteresis can be useful are suggested.

CMOS N-DIMENSIONAL M-LEVEL HYSTERESIS CIRCUITS AND POSSIBLE APPLICATIONS

by

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DEDICATION

To my family

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

According to wikipedia [67], the name of hysteresis has the meaning of "deficiency", or "lagging behind", which was used by Sir James Alfred Ewing, a Scottish physicist and engineer, to described the characteristic hysteresis curve of magnets. The output at one moment of a deterministic system with no hysteresis can be predicted with only the input to the system at that moment and the initial state. Yet for a system with hysteresis characteristics, the output of the system does not only depend on the input to the system at the moment, but also the history of the system. A system with hysteresis is a system with memory. Another important characteristic of hysteresis phenomenon is branching; the definition of hysteresis is given by I. D. Mayergoyz [32] as following: "Consider a transducer that can be characterized by an input $u(t)$ and an output $f(t)$. This transducer is called a hysteresis transducer if its input-output relationship is a multi-branch nonlinearity for which branch-to-branch transitions occur after input extrema." A hysteresis system must be multistable for branching to happen, meaning the system must have multiple equilibrium points for a constant input value. The output while the input is increasing may be different than the output while the input is decreasing [3].

Hysteresis phenomenon was first discovered in magnetics, then later discovered in mechanical hysteresis, ferroelectric hysteresis, and superconductor hysteresis.

Hysteresis phenomena not only exist in physics but many disciplines of science: economic systems show signs of hysteresis; cells undergoing cell division have hysteresis behavior in changing states; some neurons do not return to the original state after the removal of stimulus. Hysteresis has been widely studied and mathematical tools and models have been developed to study real life hysteresis systems [10] [32].

In I. Mayergoyz's book [32], hysteresis was categorized into two groups, the rate-independent and rate-dependent. For rate-independent hysteresis output depends on the past value of the input but not the speed of the input. Then rate-independent hysteresis was further divided into two groups, hysteresis with local memories and hysteresis with non local memories. The future output of hysteresis with local memory is uniquely determined by the current output and input. Yet, for hysteresis with non-local memories, the future output not only relies on the current input and output, but also the past extremum values of the input. In I. Mayergoyz's book, extensive studies on the mathematical models of hysteresis and their application are given.

A new concept, n-dimensional m-level multi-cell hysteresis is presented here. This new concept which is the main contribution of this dissertation has not been found in the survey of literatures. Additionally, a significant part of the research work is the CMOS implementation of the n-dimensional m-level multi-celled hysteresis. There are five chapters in the dissertation: Chapter one: Introduction. Chapter two: Binary Hysteresis Circuits, which gives a review on the past job trying to have some control on the binary hysteresis. Chapter three: CMOS Binary Hysteresis Circuits with Full Control. Chapter four: Circuits for Handling Sweeping Signals,

that include analogue adders, multipliers, current voltage converters, and voltage current converters. Chapter five: CMOS Multi-Cell Hysteresis Circuit, explains the construction of multi-cell hysteresis.

1.1 Multi-Celled Hysteresis

In this section, the new concept of multi-celled hysteresis is explained. We start with the more familiar concept of binary hysteresis, then proceed to construct multi-level hysteresis using binary hysteresis, and finally reach the construction of multi-celled hysteresis.

1.1.1 Binary Hysteresis

A system is said to exhibit binary hysteresis if it has different switching levels in its input-output transfer characteristics, which make the output signal snap alternately between two stable states (logic low and high). This is illustrated in the hysteresis curves shown in Figure 3.1. For different switching characteristics, binary hysteresis is categorized in two groups, forward binary hysteresis and its reverse, as shown in Figure 3.1, with u as the input and y as the output.

The mathematical description of forward binary hysteresis is contained in Equation (3.1). Here H_+, H_-, u_{H2L}, and u_{L2H} are real parameters characterizing the hysteresis, where $H_- < H_+$ and $u_{H2L} < u_{L2H}$ are assumed, and y_0 is the previous value of y. The presence of y_0 in Equation (3.1) ensures that the hysteresis is not multi-valued.

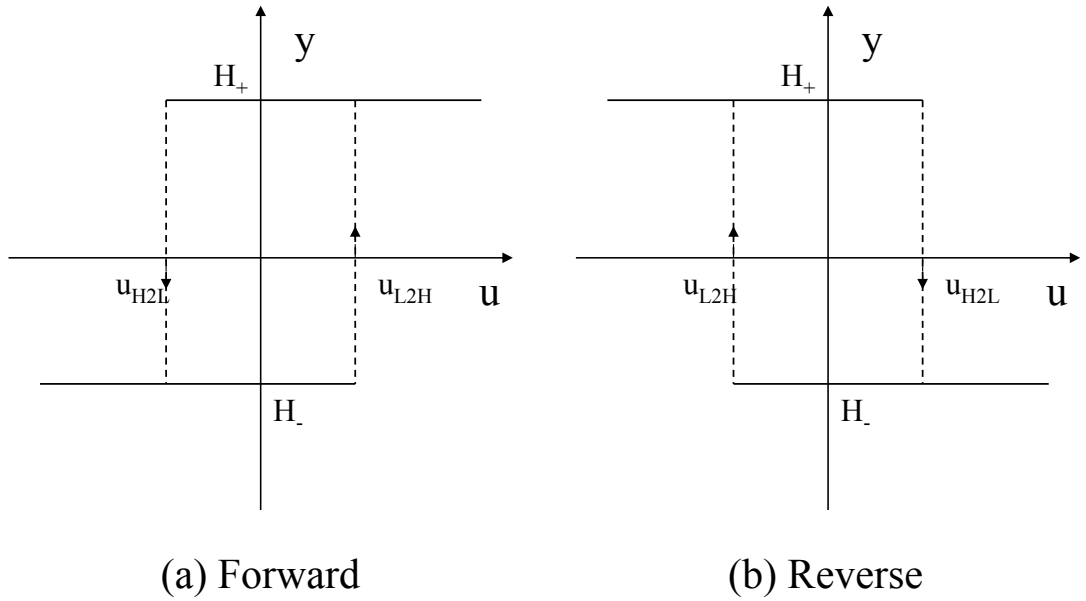

Figure 1.1: Binary hysteresis, (a) forward and (b) reverse.

$$y(u, y_0) = \begin{cases} H_+ & u > u_{L2H}, \text{ for any } y_0 \\ H_+ & u_{H2L} \leq u \leq u_{L2H}, \text{ if } y_0 = H_+ \\ H_- & u_{H2L} \leq u \leq u_{L2H}, \text{ if } y_0 = H_- \\ H_- & u < u_{H2L}, \text{ for any } y_0 \end{cases} \tag{1.1}$$

Reverse hysteresis can be described in a very similar way in Equation (3.2), where $H_- < H_+$ still holds as in the forward hysteresis case, yet $u_{L2H} < u_{H2L}$.

$$y(u, y_0) = \begin{cases} H_+ & u < u_{L2H}, \text{ for any } y_0 \\ H_+ & u_{L2H} \leq u \leq u_{H2L}, \text{ if } y_0 = H_+ \\ H_- & u_{L2H} \leq u \leq u_{H2L}, \text{ if } y_0 = H_- \\ H_- & u > u_{L2H} \end{cases} \tag{1.2}$$

Alternate to using H_-, H_+, u_{H2L}, and u_{L2H}, both forward and reverse hysteresis can be characterized by their height H_H, width u_W, center position vertically

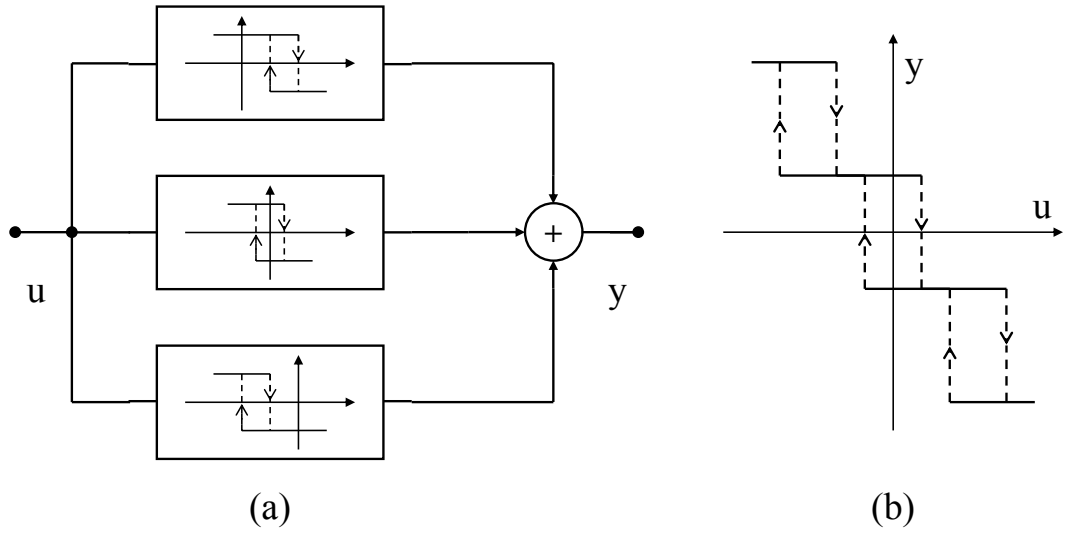

Figure 1.2: Generation of 4-level hysteresis by adding 3 binary hysteresis. (a) Schematic. (b) 4-level hysteresis

with H_C, and horizontally with u_C, as shown in Equations (3.3).

$$\begin{aligned} H_H &= H_+ - H_- \\ u_W &= |u_{H2L} - u_{L2H}| \\ H_C &= (H_+ + H_-)/2 \\ u_C &= (u_{H2L} + u_{L2H})/2 \end{aligned} \tag{1.3}$$

1.1.2 Multi-Level Hysteresis

Multi-level hysteresis can be achieved by adding several binary hysteresis curves centered at different positions. In the case where three reverse binary hysteresis curves are added together, they generate 4-level hysteresis, as shown in Figure 1.2, where there are six switching points. The output can take four values, which is why it is referred to as 4-level hysteresis. In the general case, adding $(m-1)$ binary

hysteresis generates m-level hysteresis.

1.1.3 Multi-Celled Hysteresis

Before embarking on a discussion of the more complicated cases, we start by generating two-dimensional three-level hysteresis cubes. A circuit to generate two-dimensional three-level hysteresis cubes takes two of the three-level hysteresis circuits, as shown in Figure 5.12. The two inputs to the multiplier, H_X and H_Y, are both three-level hysteresis signals. The output Z is the product of H_X and H_Y. A three-dimensional plot of the two-dimensional three-level hysteresis cells is shown in Figure 5.12 (b). A total of four hysteresis cells are generated in the two input case. This can be generalized in two different ways, both by adding more levels of hysteresis or by increasing the dimensions of the hysteresis. If n 3-level hysteresis signals are used as inputs, then 2^n hysteresis cubes can be generated. It is not difficult to see that $(m-1)^n$ hysteresis cubes can be generated by multiplying n m-level hysteresis signals.

1.2 Contributions of the dissertation

The main contributions of the dissertation are in the following areas.

- First, the new concept of multi-dimensional multi-level hysteresis is introduced.

- Second, a group of CMOS binary hysteresis circuits with full control which operate in all four quadrants is introduced. These CMOS binary hysteresis cir-

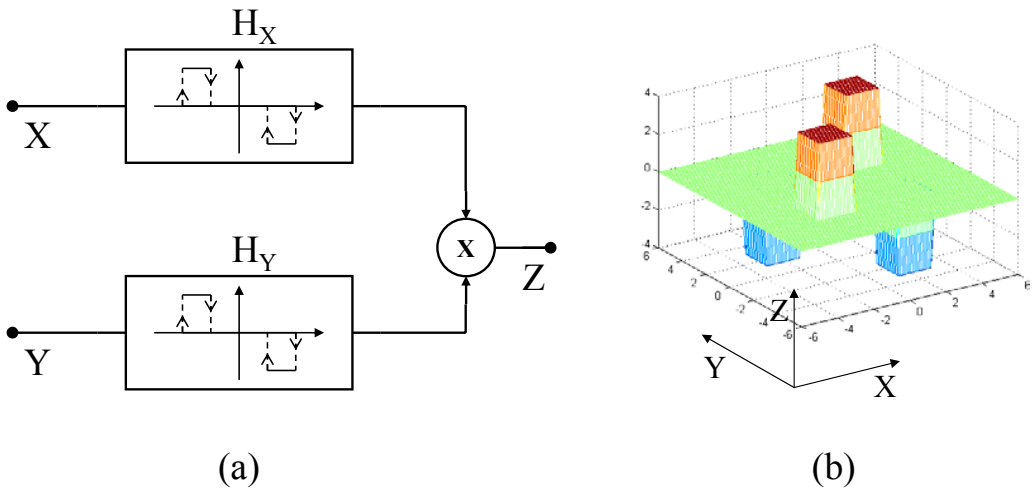

Figure 1.3: Generation of 2-dimensional 3-level hysteresis cubes. (a) Schematic. (b) 3-D plot of the hysteresis cubes

cuits include the following four kinds: current-input current-output, voltage-input voltage-output, current-input voltage out, and voltage-input current-output. For each kind of binary hysteresis circuit, both forward and reverse hysteresis can be achieved. The position (u_C, H_C), the width u_W, and the height H_H of each hysteresis can be adjusted independently by external current sources and/or voltage sources. Also, the hysteresis can be put in any of the four quadrants. The detailed discussions on these CMOS binary hysteresis circuits are given in Chapter three. Before that, the historical review of the past means of designing and controlling hysteresis externally are given in Chapter two.

- Thirdly, CMOS circuits, to be combined with the CMOS binary hysteresis circuits, that are also building blocks for multi-dimensional multi-level hysteresis

are designed. These circuits include analogue four-quadrant adders, analogue four-quadrant multipliers, in both current and voltage mode, current voltage converters, and voltage current converters. The detailed discussions on the above circuits are given in Chapter four.

- Fourthly, CMOS circuits are designed to give various one-dimensional multi-level hysteresis, in both current mode and voltage mode. Various combinations of adding forward and reverse binary hysteresis are demonstrated. Furthermore, CMOS circuits, in both current mode and voltage mode, that give two-dimensional multi-level multi-cell hysteresis are designed. Further discussion on how to extend the results to more dimensions, n-D, is given. These are covered in Chapter five.

- Finally, multi-cell hysteresis is suggested to be used in chaotic signal generation, as is covered in section 5.6 of Chapter five. We suggest a couple of areas that multi-cell hysteresis can be useful in Chapter six which gives summaries.

Chapter 2

Binary Hysteresis Circuits

To construct multi-cell hysteresis, binary hysteresis circuits are the most important building blocks. In order to place hysteresis cubes at any location in the input-output space, we would like binary hysteresis circuits to possess fully controllable width, height, horizontal and vertical position of the hysteresis. In this chapter, a review of the known binary hysteresis are given.

Binary hysteresis circuits have the feature that the output transfer characteristics have different input thresholds for positive-going and negative-going input signals. The circuits also respond to a slowly changing input waveform with a fast transition time at the output. Former work on binary hysteresis circuits is presented in this Chapter in four Sections: voltage-input voltage-output, current-input voltage-output, voltage-input current-output, and current-input current-output.

If CMOS schematics of the circuits are available in any of the former works in the discussion, similar results are generated by running PSpice simulations with the schematic. MOSIS 1.2 μm transistor models (BSIM1, Level 4, and Run n7ab) [37] are used in all the simulations. Also, since some of the names and symbols appear many times in many places, I would like to clarify the definitions and expressions of these names before further discussion. The common names and symbols used often are listed in Table 2.1.

Table 2.1: The definitions and expressions of the common names and symbols.

* Fabrication process dependant, only valid for BSIM1, Level 4, and Run n7ab.

Symbol	Definition	Expression/Value
ε_{OX}	Dielectric constant of silicon dioxide	$35.1 \times 10^{-18} F/\mu m$
T_{OX}	Gate-oxide Thickness	$30.6nm$ *
C_{OX}	Gate capacitance per unit area	$C_{OX} = \varepsilon_{OX}/T_{OX}$
μ_n	Electron mobility	688.4 cm^2/Vs *
μ_p	Hole mobility	167.4 cm^2/Vs *
K_N	NMOS transconductance parameter	$K_N = \mu_n C_{OX}$
K_P	PMOS transconductance parameter	$K_P = \mu_p C_{OX}$
W_N & W_P	NMOS & PMOS channel widths	
L_N & L_P	NMOS & PMOS channel lengths	
$\beta_{N,P}$		$\beta_{N,P} = \frac{K_{N,P}}{2}\frac{W_{N,P}}{L_{N,P}}$
V_{THN} & V_{THP}	NMOS & PMOS threshold voltages	$0.5666V$ &$-0.7996V$

Since the only large signal current that can run through MOS transistors is either from drain to source for NMOS transistor, or source to drain for PMOS transistors, instead of using either I_{DS} or I_{SD}, the symbol I will be used, with substrate normally referring to the name of the transistor that the current is flowing through. For a NMOS transistor, the current can be expressed in Equation (2.1), with $\beta_N = (K_N W_N/2L_N)$. The source to drain current of a PMOS transistor can be described in very similar way, in Equation (2.2), $\beta_P = (K_P W_P/2L_P)$.

$$I = \begin{cases} \beta_N[2(V_{GS} - V_{THN})V_{DS} - V_{DS}^2] & \text{if } V_{GS} \geq V_{THN} \text{ and } 0 \leq V_{DS} < V_{GS} - V_{THN} \\ \beta_N(V_{GS} - V_{THN})^2 & \text{if } V_{GS} \geq V_{THN} \text{ and } V_{DS} \geq V_{GS} - V_{THN} \\ 0 & V_{GS} < V_{THN} \end{cases} \tag{2.1}$$

$$I = \begin{cases} \beta_P[2(V_{SG} + V_{THP})V_{SD} - V_{SD}^2] & \text{if } V_{SG} \geq -V_{THP} \text{ and } 0 \leq V_{SD} < V_{SG} + V_{THP} \\ \beta_P(V_{SG} + V_{THP})^2 & \text{if } V_{SG} \geq -V_{THP} \text{ and } V_{SD} \geq V_{SG} - V_{THP} \\ 0 & V_{SG} < -V_{THP} \end{cases} \tag{2.2}$$

2.1 Voltage-Input Voltage-Output Hysteresis Circuits

2.1.1 CMOS Schmitt Trigger

The most well known voltage-input voltage-output hysteresis circuit is probably the Schmitt trigger. The Schmitt trigger was invented in the early 20th century by O. H. Schmitt [49] using vacuum tubes for modeling neurons. The basic schematic and the transfer characteristics of a CMOS Schmitt trigger [21] are shown in Figure 2.1.

As the input increases from low to high, the output switches from high to low when the input exceeds V_{H2L}. As the input decreases, the output can switch back to high again only when the input goes below V_{L2H}. The circuit can be divided into two parts, depending on whether the output is high or low. If the output is low, then MP3 is on while MN3 is off. At this time, only the p-channel portions are

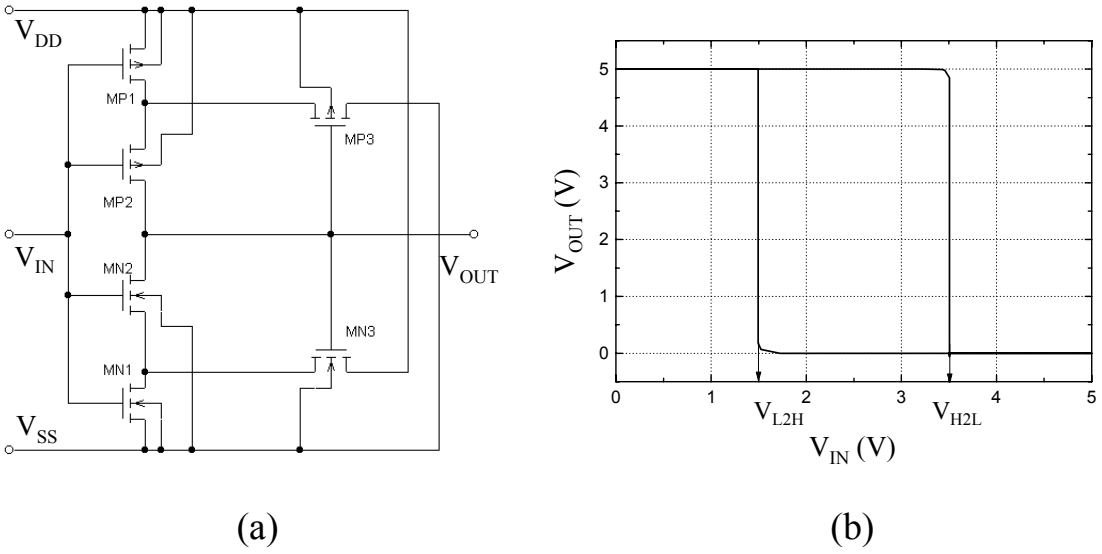

Figure 2.1: CMOS Schmitt trigger, a voltage-input voltage-output hysteresis circuit. (a) Schematic used in PSpice simulation. (b) Simulated transfer characteristics, reverse hysteresis. $V_{DD} = 5V$ and $V_{SS} = 0V$.

considered in calculating the switching point voltage. If the output is high, then MN3 is on and MP3 is off and only the n-channel portions are considered. With the given V_{H2L} and V_{L2H}, the transistor sizes of MN1, MN3, MP1 and MP3 can be decided by Equations (2.3) and (2.4), if V_{SS} is grounded [2].

$$\frac{\beta_{MN1}}{\beta_{MN2}} = \left[\frac{V_{DD} - V_{H2L}}{V_{H2L} - V_{THN}}\right]^2 \tag{2.3}$$

$$\frac{\beta_{MP1}}{\beta_{MP2}} = \left[\frac{V_{L2H}}{V_{DD} - V_{L2H} - V_{THP}}\right]^2 \tag{2.4}$$

Therefore, we can rearrange Equations (2.3) and (2.4) to solve for switching voltage V_{H2L} and V_{L2H} in term of the transistor parameters, as shown in Equations (2.5) and (2.6).

$$V_{H2L} = \frac{V_{DD} + \sqrt{\frac{\beta_{MN1}}{\beta_{MN2}}} \cdot V_{THN}}{1 + \sqrt{\frac{\beta_{MN1}}{\beta_{MN2}}}} = \frac{V_{DD} - V_{THN}}{1 + \sqrt{\frac{\beta_{MN1}}{\beta_{MN2}}}} + V_{THN} \tag{2.5}$$

$$V_{L2H} = \frac{V_{DD} - V_{THP}}{1 + \sqrt{\frac{\beta_{MP1}}{\beta_{MP2}}}} \tag{2.6}$$

Equations (2.5) and (2.6) describe the instantaneous switching points of the Schmitt trigger. Detailed study of the transient behavior from one stable state to another can be found in I. M. Filanovsky and H. Baltes's discussions on Schmitt trigger design [14]. For the Schmitt trigger circuit shown in Figure 2.1, the switching voltages and the 2-level output voltages are decided by the transistor parameters and the bias voltages V_{DD} and V_{SS}. In other words, the parameters of the hysteresis can not be adjusted externally, except by power supply adjustment, after the design of the circuit is finished.

2.1.2 Pfister's Schmitt Trigger

There is a slight variation of the Schmitt trigger, due to A. Pfister [41], shown in Figure 2.2. With an additional pair of transistors, MN4 and MP4, at the output stage, the switching voltages of the hysteresis can be adjusted externally by the control voltage,V_{CT}, although the variation is not over a very wide range. One can also notice that the switching from low to high and high to low can not be adjusted independently. There is no control on the output high and output low. The simulation results of Pfister's Schmitt trigger are shown in Figure 2.3.

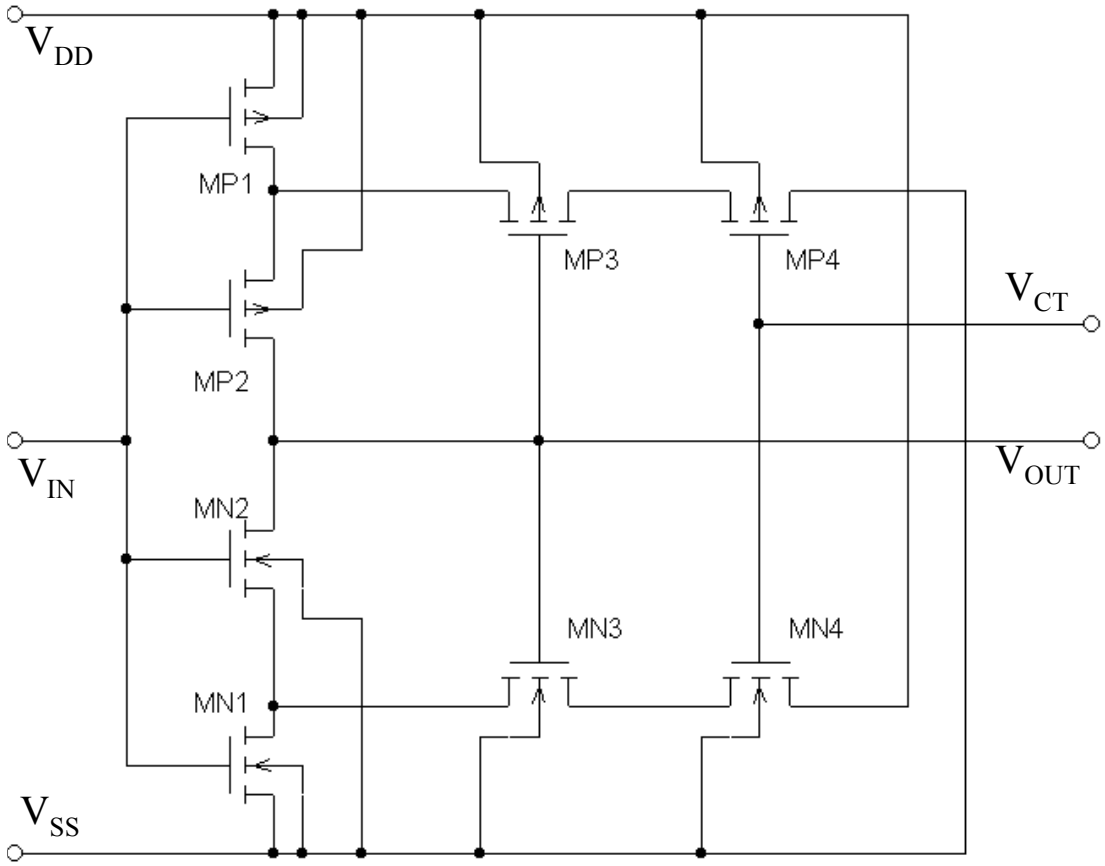

Figure 2.2: Pfister's CMOS adjustable Schmitt trigger [41], with external voltage control.

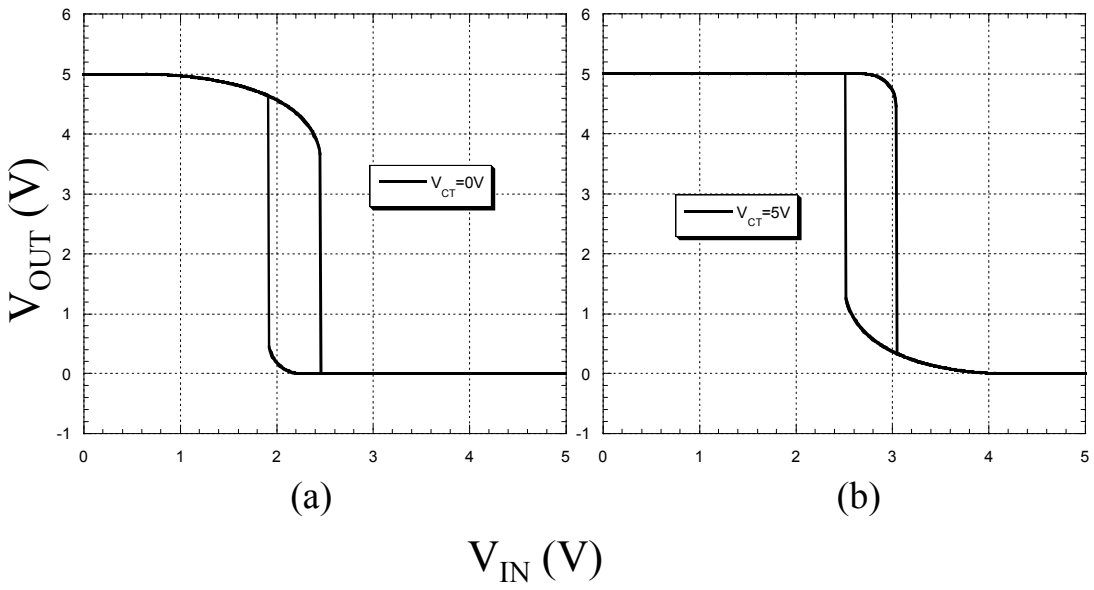

Figure 2.3: Pfister's CMOS adjustable Schmitt trigger [41], with external voltage control simulation results. $V_{DD} = 5V$ and $V_{SS} = 0V$. (a)$V_{CT} = 0V$. (b)$V_{CT} = 5V$.

2.1.3 Kim's Adjustable Hysteresis Using Operational Transconductance Amplifier

A Schmitt trigger claimed to have fully adjustable hysteresis was implemented using an operational transconductance amplifier (OTA) by K. Kim [23] to give reversed hysteresis. The circuit configuration and the transfer characteristics of Kim's Schmitt trigger are shown in Figure 2.4. The transfer characteristics are directly grabbed from Kim's paper. The two-level output voltages V_+ and V_- are linearly controlled by the bias current I_{B1} simultaneously. The switching threshold voltages V_{H2L} and V_{L2H} are linearly controlled by a different bias current, I_{B2}, also simultaneously. For this hysteresis circuit, the height and width of the hysteresis can be adjusted but the position of the hysteresis is fixed, to be symmetric about

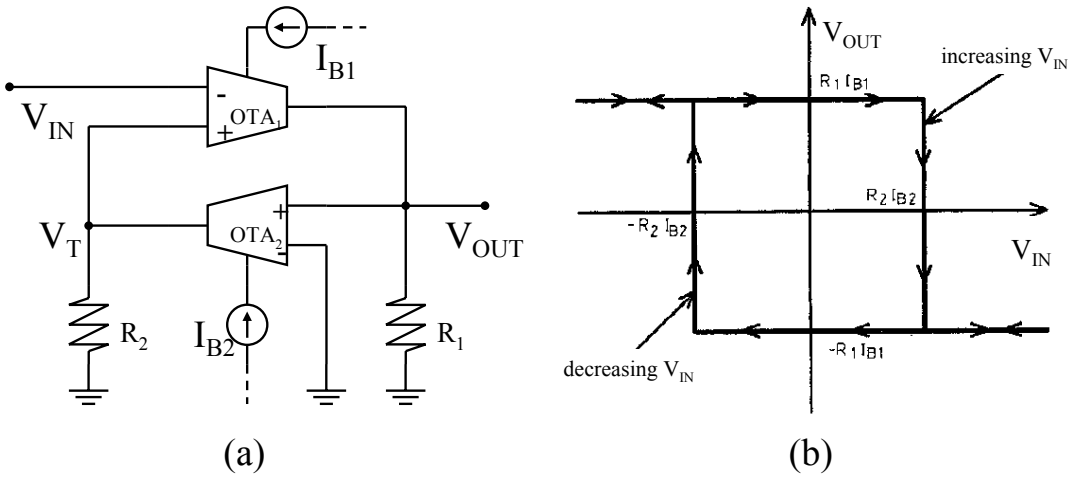

Figure 2.4: Kim's adjustable hysteresis using operational transconductance amplifier [23]. (a)Circuit configuration. (b)Transfer characteristic.

the origin. Therefore, Kim's Schmitt trigger is not really fully adjustable.

2.1.4 Adjustable Hysteresis Using Operational Amplifier

Semistate design theory has been used in the design of hysteresis by R. W. Newcomb [36] to achieve swept binary hysteresis by using operational amplifiers, as shown in Figure 2.5. The hysteresis parameter can be adjusted by the bias voltages V_S and V_B. One example of Newcomb's experimental swept hysteresis results are shown in Figure 2.6.

Newcomb's hysteresis has partial tunability, but it is not in CMOS VLSI design.

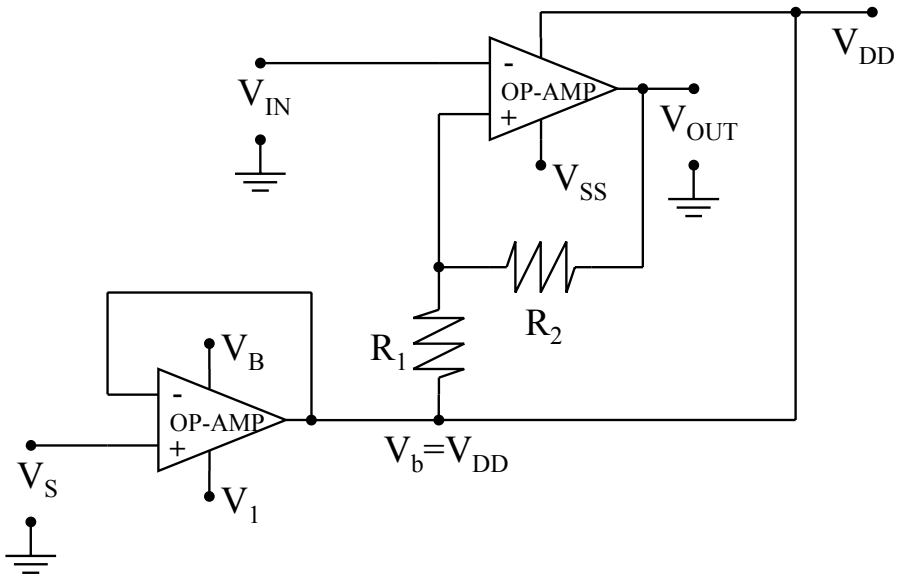

Figure 2.5: Newcomb's swept hysteresis hysteresis realization circuits [36].

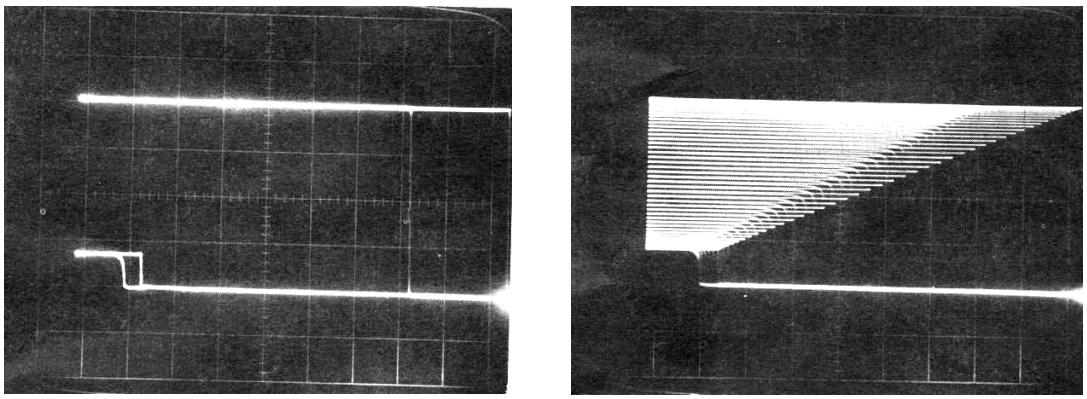

Figure 2.6: Newcomb's experimental swept hysteresis results [36]. (a) V_S is a square wave. (b) V_S is a sine wave.

2.1.5 Summary

A comparison of the above voltage-input voltage-output hysteresis circuits is given in Table 2.2. None of the listed circuits give complete control of the hysteresis height, width, and position.

Table 2.2: Comparison of the voltage-input voltage-output binary hysteresis circuits.

	Hysteresis	Horizontal	Vertical
CMOS Schmitt [21]	Reverse	None	None
Pfister's [41]	Reverse	Limited	None
Kim's OTA-R [23]	Reverse	Limited	Limited
Newcomb Swept [36]	Reverse	Limited	Limited

2.2 Current-Input Voltage-Output Hysteresis Circuits

Current-input voltage-output hysteresis circuits take currents as inputs and produce voltage as outputs. Often current-input voltage-output hysteresis circuits are referred to as current Schmitt triggers in the literature ([29], [59], and [60]), although they do not operate completely in the current domain. Current-input Schmitt triggers are particularly useful in photodetectors, barcode readers, and optical remote controls.

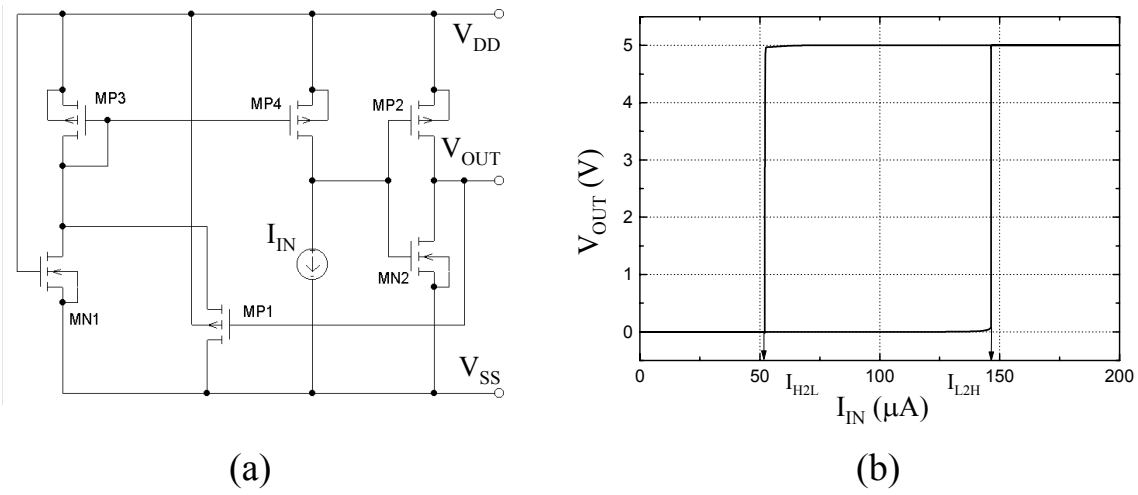

Figure 2.7: Liao's CMOS current-input voltage-output hysteresis circuit. [29]. (a) Schematic used in PSpice simulation. (b) Simulated transfer characteristic, forward hysteresis. $V_{DD} = 5V$ and $V_{SS} = 0V$.

2.2.1 Liao's CMOS Current-Input Voltage-Output Hysteresis Circuit

Liao [29] has achieved a current-input voltage-output Schmitt trigger using only 6 transistors. The schematic and the transfer characteristics of this 6-transistor current-mode Schmitt trigger are shown in Figure 2.7. The feedback is established through MP1 by comparing I_{IN} and the current flowing through MP4.

For this circuit, the switching current I_{H2L} is determined by the parameters of transistor MN1. The width of the hysteresis $I_W = I_{L2H} - I_{H2L}$ is decided by the parameters of transistor MP1. This is an impressive circuit made up of only 6 transistors but it has the disadvantage that the hysteresis parameters cannot be controlled externally. However, some minor variations could be made to this circuit to achieve certain external control. For example, the transistor MN1 could

be replaced by a current source in which one of the threshold currents I_{H2L} could be controlled by this current source. If $\beta_{P3} \gg \beta_{N1}, \beta_{P1}$ and $V_{THN} \cong V_{THP}$, the two switching points I_{H2L} and I_{L2H} are given in Equations (2.7).

$$\begin{aligned} I_{H2L} &= \beta_{N1}(V_{DD} - V_{SS} - V_{THN})^2 \\ I_{L2H} &= \beta_{N1}(V_{DD} - V_{SS} - V_{THN})^2 + \beta_{P1}(V_{DD} - V_{SS} - 2V_{THP})^2 \end{aligned} \tag{2.7}$$

2.2.2 Z. Wang's CMOS Current-Input Voltage-Output Hysteresis Circuit with One Control

A current-input voltage-output Schmitt trigger with one controllable threshold current was achieved by using only 7 transistors by Z. Wang and W. Guggenbuhl [59]. The schematic of the circuit is shown in Figure 2.8 (a), and the simulations results are shown in Figure 2.8 (b). The transistor pair MN2 and MP1 compares I_0 and the current though MP1. The comparison result switches the feedback transistor MP4 on or off. This Schmitt trigger generates a reverse hysteresis. The only controllable threshold current I_{L2H} is given by I_0. The hysteresis width $I_W = I_{H2L} - I_{L2H}$ is decided by the dimensions of transistor MP4. With fixed voltage supply, the hysteresis generated by the circuit in Figure 2.8 has fixed width and height but externally controllable position along the horizontal axis. The two switching points I_{L2H} and I_{H2L} are given by Equations (2.8).

$$\begin{aligned} I_{L2H} &= I_0 \\ I_{H2L} &= I_0 + \beta_{P4}\left[2\left(V_{DD} - V_{SS} - \sqrt{\tfrac{I_0}{\beta_{N2}}} - V_{THP}\right)\left(\sqrt{\tfrac{I_0}{\beta_{P1}}} + V_{THP}\right) - \left(\sqrt{\tfrac{I_0}{\beta_{P1}}} + V_{THP}\right)^2\right] \end{aligned} \tag{2.8}$$

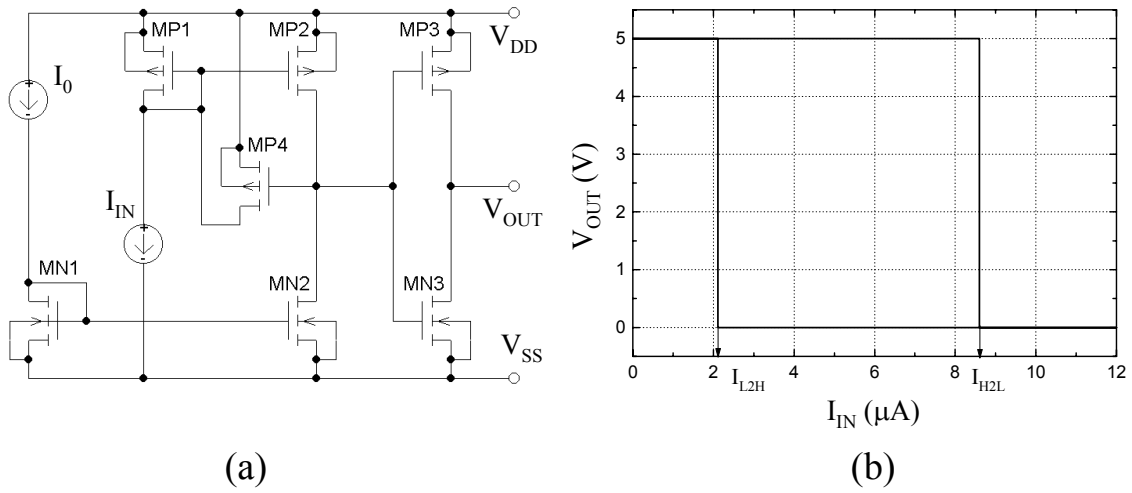

Figure 2.8: Z. Wang's CMOS 7-transistor current-input voltage-output hysteresis circuit [59]. (a) Schematic used in PSpice simulation. (b) Simulated transfer characteristic, reverse hysteresis. $V_{DD} = 5V$, $V_{SS} = 0V$ and $I_0 = 2\mu A$.

2.2.3 Z. Wang's CMOS Current-Input Voltage-Output Hysteresis Circuit with Full Control Horizontally

Z. Wang and W. Guggenbuhl [60] furthered their study and achieved an 8 transistor CMOS current-input voltage-output hysteresis circuit with adjustable hysteresis, as shown in Figure 2.9. MP1 and MP2, MN3 and MN4 are matching pairs that compare the currents I_{SD} of MP1 and I_{IN}. The output of the comparator controls the switching of MN1 and MN2, which creates a regenerative feedback. The threshold currents are exclusively determined by the current I_{SD} of MP1. The current I_{SD} of MP1 is controlled by V_{OUT} through switching MN1 on or off. It is not difficult to see that the lower switching current I_{H2L} has the same value as I_1 and the hysteresis width $I_W = I_{L2H} - I_{H2L}$ is I_0. The two switching currents I_{H2L} and I_{L2H}

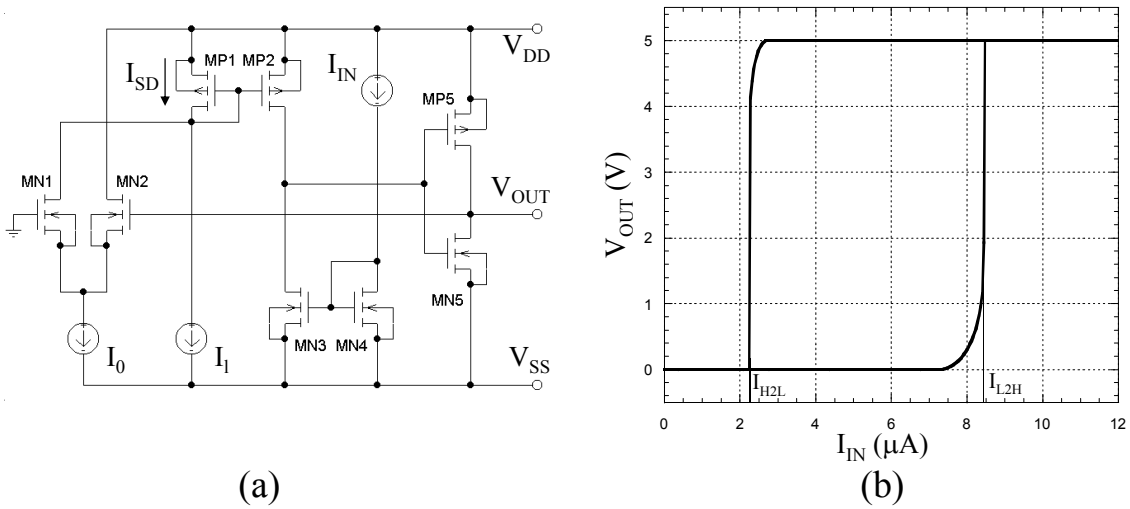

Figure 2.9: Z. Wang's CMOS 8-transistor current-input voltage-output hysteresis circuit [60]. (a) Schematic used in PSpice simulation. (b) Simulated transfer characteristic, forward hysteresis. $V_{DD} = 5V$, $V_{SS} = 0V$, $I_0 = 6\mu A$, and $I_1 = 2\mu A$.

are given by Equations (2.9). The simulation results are given in Figure 2.9 (b). The horizontal position and the width of the hysteresis are completely externally adjustable by two current sources I_1 and I_0, but the output high and low are fixed by V_{DD} and V_{SS}.

$$\begin{aligned} I_{H2L} &= I_1 \\ I_{L2H} &= I_1 + I_0 \end{aligned} \tag{2.9}$$

2.2.4 Z. Wang's CMOS Two Input Current-Input Voltage-Output Hysteresis Circuit with Full Control Horizontally

The circuit in Figure 2.9 was further extended to a two-input current comparator with variable hysteresis, as shown in Figure 2.10. The current comparing

pair MN5 and MP5 switches MN1 on or off as MN6 and MP6 control MN2. At any moment except the transition time, one and only one of MN1 and MN2 is on, which leads the current to feed back to either MP1 or MP2. This ensures the hysteresis characteristic of the circuit. It is obvious that the hysteresis width I_W is twice the value of the bias current I_{HY}. Since the circuit is symmetric with respect to I_1 and I_2, it can be used to generate either forward or reverse hysteresis. If I_1 is the input and I_2 is the control, forward hysteresis is obtained. If I_2 is the input and I_1 is the control, reverse hysteresis is obtained. For the reverse hysteresis, the two switching currents I_{H2L} and I_{L2H} are shown in Equations (2.10). A simulation example is shown in Figure 2.10 (b).

$$\begin{aligned} I_{H2L} &= I_1 + I_{HY} \\ I_{L2H} &= I_1 - I_{HY} \end{aligned} \tag{2.10}$$

2.2.5 Summary

In Table 2.3, a comparison is given of the four CMOS current-input voltage-output hysteresis circuits discussed here. For all four of the current-input voltage-output binary hysteresis circuits discussed in this section, the output voltage switches between V_{DD} and V_{SS} and can not be adjusted externally.

One can notice that for all the listed circuits in Table 2.3, passing the output through an inverter can change the forward hysteresis to reverse hysteresis, or vice versa.

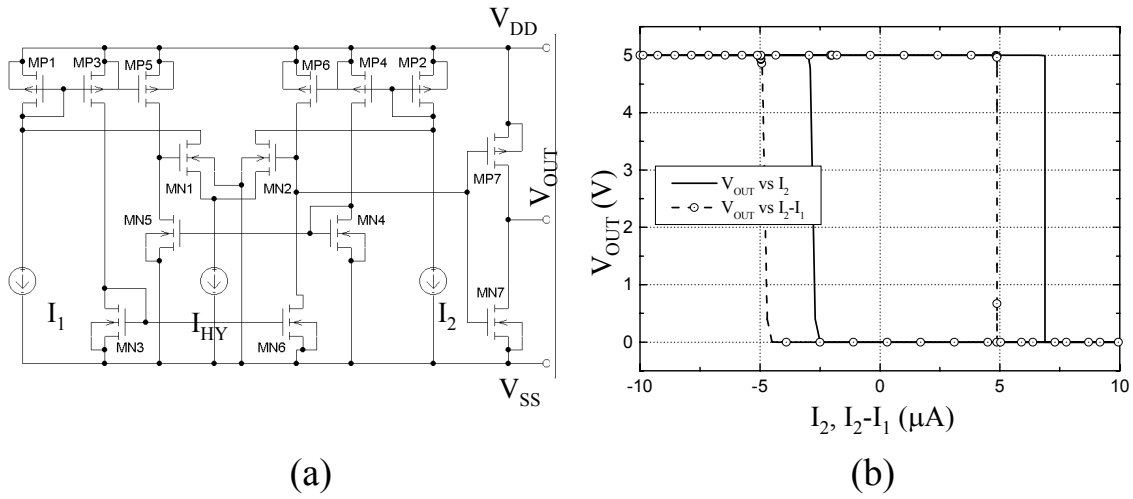

Figure 2.10: CMOS two-input current comparator with hysteresis [60]. (a) Schematic used in PSpice simulation. (b)Simulated transfer characteristic, reverse hysteresis. This circuit gives reverse hysteresis; I_2 is the input and I_1 is the control. $V_{DD} = 5V$, $V_{SS} = 0V$, and $I_1 = 2\mu A$.

Table 2.3: Comparison of the current-input voltage-output binary hysteresis circuits.

	Hysteresis	Horizontal	Vertical
Liao's 6 MOSs [29]	Forward	None	None
Z. Wang's 7 MOSs [59]	Reverse	Limited	None
Z. Wang's 8 MOSs [60]	Forward	Complete	None
Z. Wang's Two Input [60]	Forward & reverse	Complete	None

2.3 Voltage-Input Current-Output Hysteresis Circuits

2.3.1 Linares-Barronco's CMOS Transconductance Hysteresis Circuit

A Transconductance-mode (T-mode) hysteresis amplifier has been achieved to give voltage-input current-output reverse hysteresis characteristic [31]. The schematic of the T-mode hysteresis is shown in Figure 2.11. In this T-mode hysteresis amplifier, the threshold voltages, V_{L2H} and V_{H2L}, can be adjusted externally and independently by V_{E+} and V_{E-}. The simulation results are shown in Figure 2.12. Figure 2.12(a) shows the simulation results of adjusting V_{L2H} by varying V_{E+} with fixed V_{E-}. Figure 18 (b) shows the simulation results of adjusting V_{H2L} by varying V_{E-} with fixed V_{E+}. This CMOS circuit has full external control horizontally but no control in the vertical direction. Also, The horizontal control has limited range, as shown in Figure 2.12, since the two control voltages V_{E+} and V_{E-} are limited by $V_{SS} \leq V_{E-} < V_{E+} \leq V_{DD}$

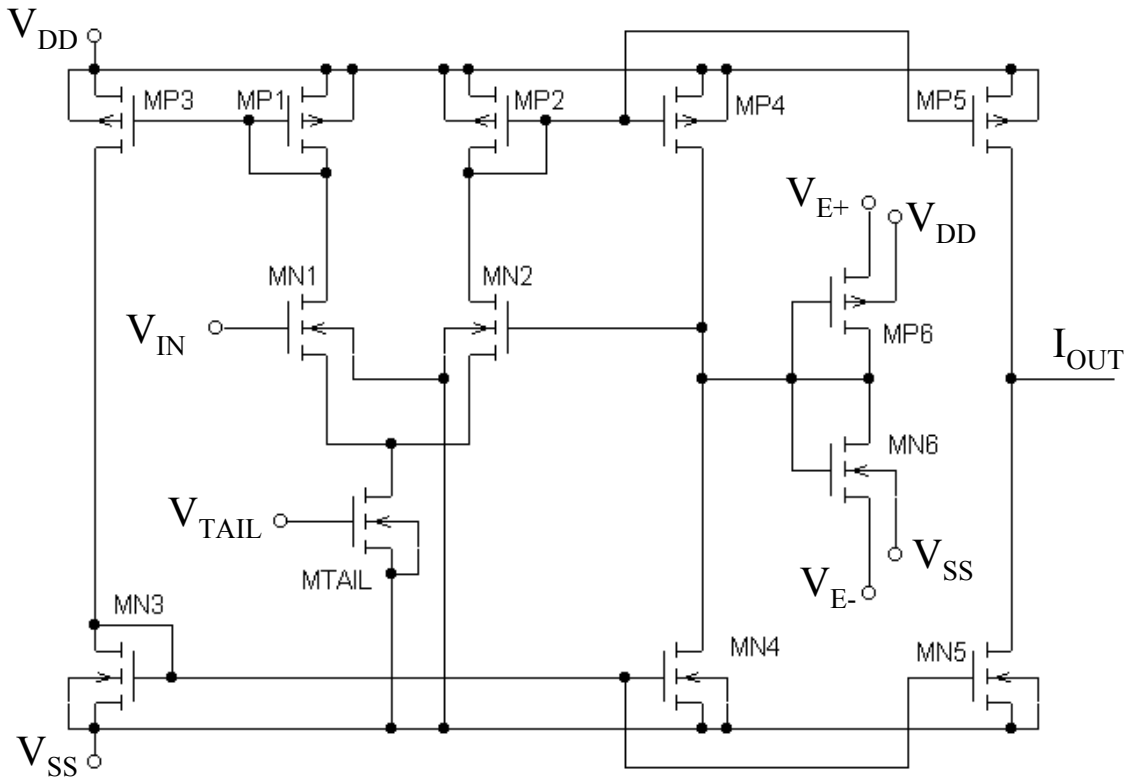

Figure 2.11: Schematic of the T-mode hysteresis amplifier [31].

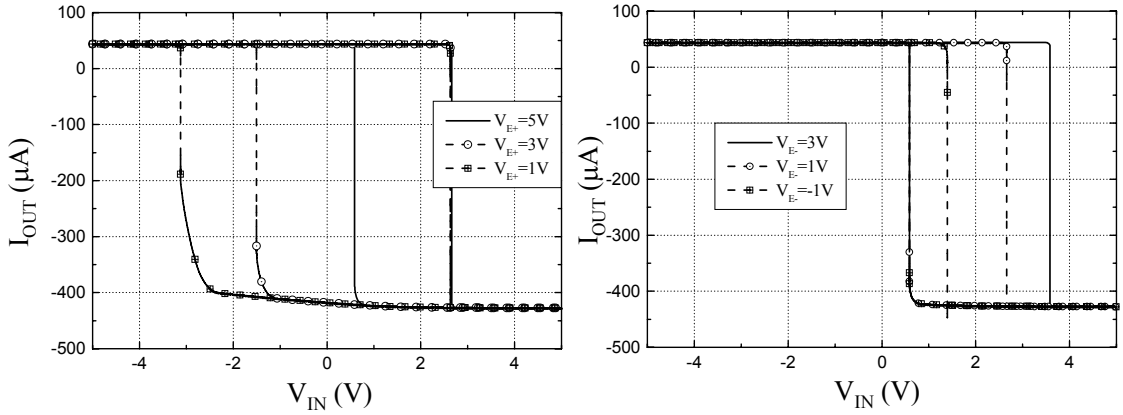

Figure 2.12: Simulated transfer characteristics for T-mode hysteresis amplifier. $V_{DD} = 5V$ and $V_{SS} = -5V$. (a) For $V_{E-} = 1V$, the solid line, dashed line with centered circles, and dashed line with crossed squares are the output curve when $V_{E+} = 5V$, $3V$, and $1V$, respectively. (b) For $V_{E+} = 5V$, the solid line, dashed line with centered circles, and dashed line with crossed squares are the output curve when $V_{E-} = 3V$, $1V$, and $-1V$, respectively.

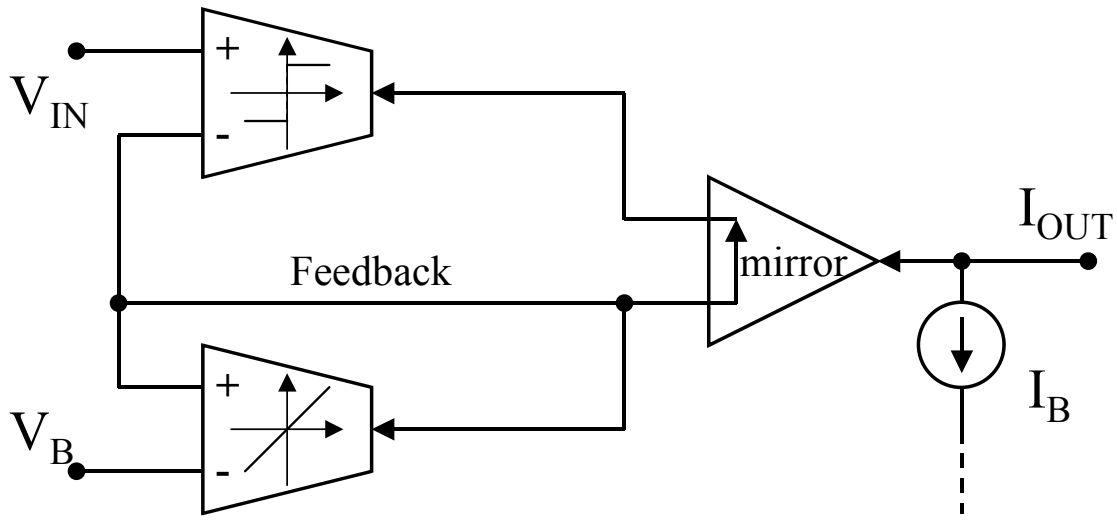

Figure 2.13: Schematic of the step-linear voltage-input current-output hysteresis circuit [61].

2.3.2 L. Wang's Voltage-Input Current-Output Hysteresis Circuit

Another approach to realize voltage-input current-output hysteresis is the step-linear hysteresis circuit [61], as suggested by M. Kataoka and T. Saito [22]. Semistate design theory for binary and swept hysteresis [36] was applied in the design of the voltage-input current-output hysteresis circuit, as shown in Figure 2.13. Differential pairs have been chosen to realize both linear and step functions.

After finishing the design of the differential pairs, the hysteresis output has a fixed height and width. The vertical position of the hysteresis is controlled by the bias current I_B. The horizontal position of the hysteresis is controlled by the bias voltage V_B, which is used to bias one input of the linear differential pair. Simulation results of the CMOS realization of Figure 2.13 are shown in Figure 2.14. The hysteresis output curves are obtained with different bias current I_B and voltage V_B.

2.3.3 Summary

In Table 2.4, a comparison of the two CMOS voltage-input current-output hysteresis circuits discussed here is given.

Table 2.4: Comparison of the voltage-input current-output binary hysteresis circuits.

	Hysteresis	Horizontal	Vertical
Linares-Barronco's [31]	Reverse	Limited Range	None
L. Wang's [61]	Forward	Limited	Limited

2.4 Current-Input Current-Output Hysteresis Circuits

The least amount of study has been done in this category. There are not many current-input current-output hysteresis circuits in the literature search. One is the winner-take-all (WTA) circuit, which has the function of choosing a winner from a group of signals. Based on Starzyk and Fang's current-mode winner-take-all (WTA) circuit [53], hysteresis was added by adding local feedback to the winning node of the array [13]. One element of DeWeerth's WTA circuit with distributed hysteresis is shown in Figure 2.15 (a). The experimental results of S. P. DeWeerth and T. G. Moris [13], as shown in Figure 2.15 (b), did show hysteresis characteristics, but the operation of the circuit was not well explained. Further investigation is needed for generating current-input, current-output binary hysteresis with full control.

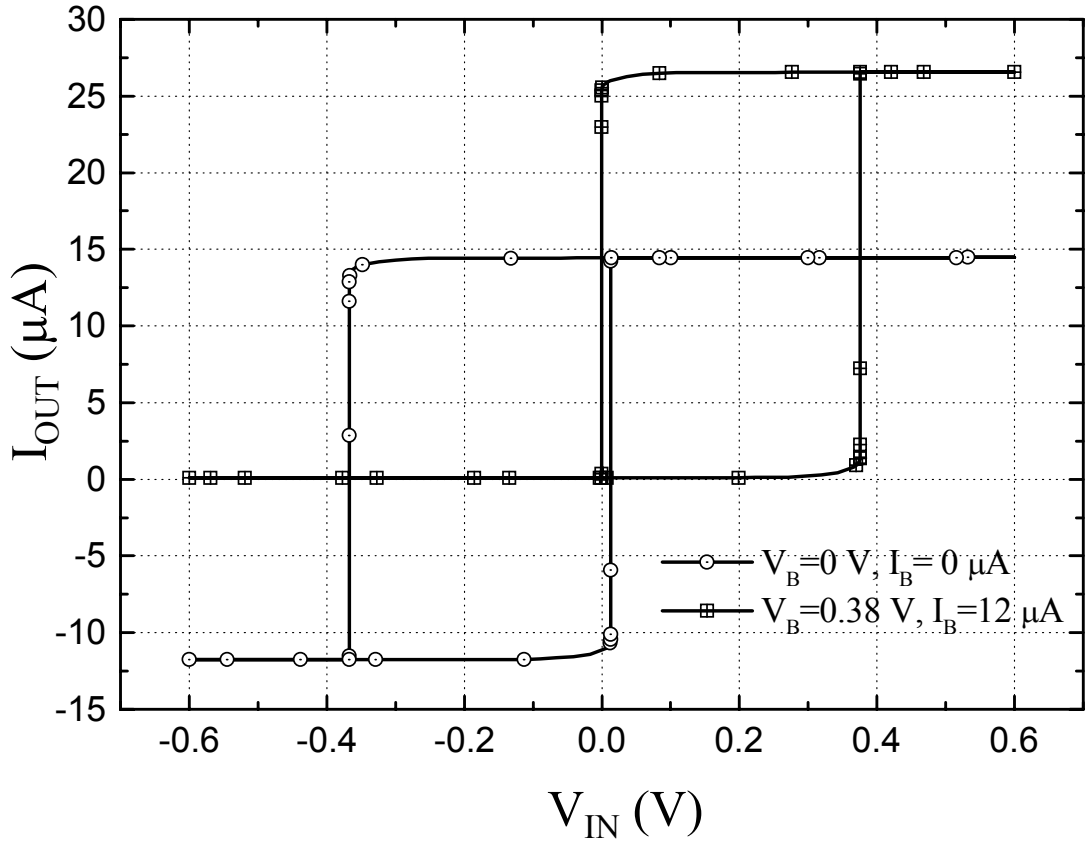

Figure 2.14: One simulation example of the voltage-input current-output Hysteresis for the circuit in Figure 2.13. The solid line with circles is the output when $V_B = 0V$ and $I_B = 0\mu A$. The solid line with squares is the output when $V_B = 0.38V$ and $I_B = 12\mu A$

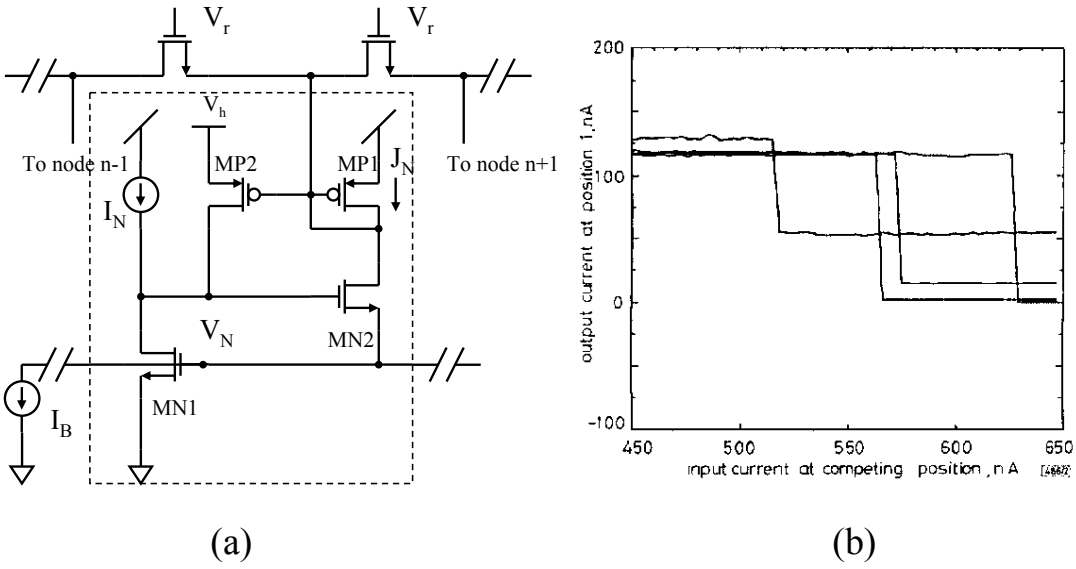

Figure 2.15: DeWeerth's winner-take-all(WTA) circuit with distributed hysteresis [13]. (a)Schematic of one element in WTA circuit. (b)Experimental data showing variable hysteretic circuit behavior.

2.5 Summary of Known Binary Hysteresis Circuits

For all the previous studies on binary hysteresis circuits, none of them has full external control of the hysteresis width, height, horizontal and vertical position. Some of them are not CMOS circuits. Therefore, our study is focused on building CMOS binary hysteresis circuits with full external control. We would also like to extend the operating range of the binary hysteresis circuits into all four quadrants.

Chapter 3

CMOS Binary Hysteresis Circuits with Full Control

3.1 Overview

In order to put hysteresis cubes in any place in the input-output space, we need to have binary hysteresis circuits with full control and with operating range in all four quadrants; such circuits will be discussed in this chapter.

Binary hysteresis can be categorized in two groups, forward and reverse, based on the switching characteristics, as shown in Figure 3.1.

The mathematical description of forward binary hysteresis is contained in Equation (3.1), with u the input and y the output. H_+, H_-, u_{H2L}, and u_{L2H} are real parameters characterizing the hysteresis, where $H_- < H_+$ and $u_{H2L} < u_{L2H}$ are assumed, and y_0 is the previous value of y. The presence of y_0 in Equation (3.1) ensures that the hysteresis is not multi-valued.

$$y(u, y_0) = \begin{cases} H_+ & u > u_{L2H}, \text{ for any } y_0 \\ H_+ & u_{H2L} \leq u \leq u_{L2H}, \text{ if } y_0 = H_+ \\ H_- & u_{H2L} \leq u \leq u_{L2H}, \text{ if } y_0 = H_- \\ H_- & u < u_{H2L}, \text{ for any } y_0 \end{cases} \tag{3.1}$$

Reverse hysteresis can be described in a very similar way in Equation (3.2),

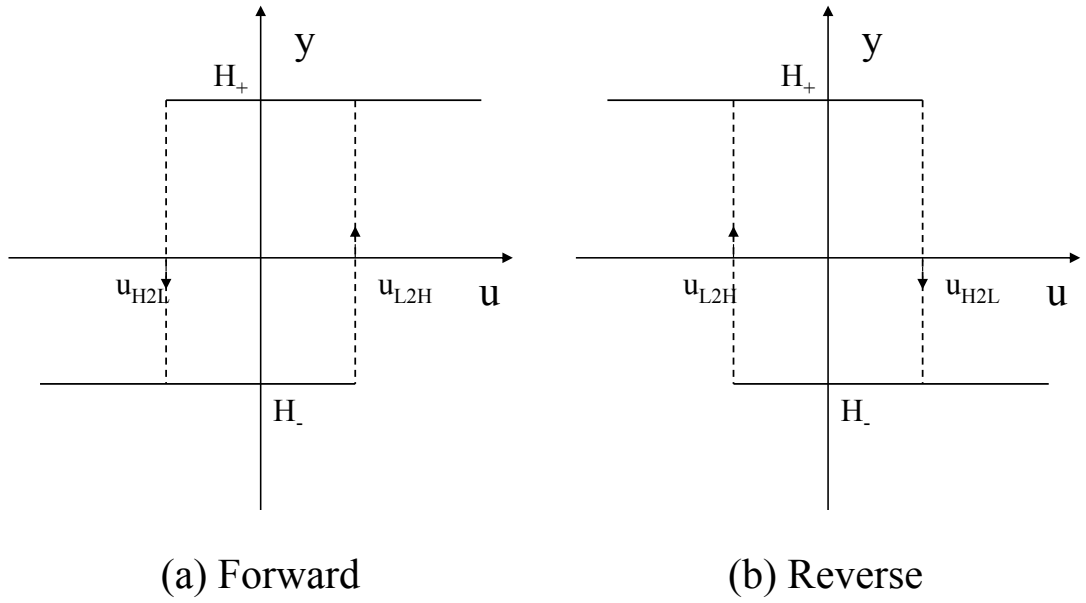

Figure 3.1: Binary hysteresis (a) Forward and (b) Reverse [36].

where $H_- < H_+$ still holds as in the forward hysteresis case, yet $u_{L2H} < u_{H2L}$.

$$y(u, y_0) = \begin{cases} H_+ & u < u_{L2H}, \text{ for any } y_0 \\ H_+ & u_{L2H} \leq u \leq u_{H2L}, \text{ if } y_0 = H_+ \\ H_- & u_{L2H} \leq u \leq u_{H2L}, \text{ if } y_0 = H_- \\ H_- & u > u_{L2H} \end{cases} \tag{3.2}$$

Alternate to using H_-, H_+, u_{H2L}, and u_{L2H}, both forward and reverse hysteresis can be characterized by there height H_H, width u_W, center position vertically with H_C, and horizontally with u_C, as shown in Equations (3.3).

$$\begin{aligned} H_H &= H_+ - H_- \\ u_W &= |u_{H2L} - u_{L2H}| \\ H_C &= (H_+ + H_-)/2 \\ u_C &= (u_{H2L} + u_{L2H})/2 \end{aligned} \tag{3.3}$$

In this chapter, binary hysteresis circuits with full control in four input-output variable categories are discussed in the following four sections. The four categories are current-input current-output, voltage-input voltage-output, current-input voltage-output, current-output voltage-output. Full control means that each of the four parameters of the hysteresis H_+, H_-, u_{H2L}, and u_{L2H} can be adjusted independently, subject to $H_+ > H_-$, $u_{H2L} < u_{L2H}$ for forward hysteresis, and $u_{L2H} < u_{H2L}$ for reverse hysteresis. In each of the sections, the schematics of the circuit, the operation principle, and the control on the switching characteristics are presented. Simulation results demonstrate the switching characteristics.

For all the simulations in this chapter, MOSIS 1.2 μm transistor models (BSIM1, Level 4, and Run n7ab) are used [37].

3.2 CMOS Current-Input Current-Output Binary Hysteresis Circuits with Full Control

Based on the current mirror and current comparator schematic in Z. Wang and W. Guggenbhl's circuit [60], a new current-input current-output binary hysteresis circuit with full adjustment is designed. The first edition shown in Figure 3.2 only works in the fourth quadrant of I_{OUT} vs I_{IN}. By using the bidirectional current mirrors, the operating range of the binary hysteresis circuit is extended to all four quadrants, as shown in Figure 3.5.

3.2.1 CMOS Current-Input Current-Output Binary Hysteresis Circuit in the Fourth Quadrant

The schematic of the current-input current-output binary hysteresis circuit is shown in Figure 3.2. I_{IL}, I_{IW}, I_{OH}, and I_{OW} are the four bias currents, seen at the bottom of the circuit schematic. While in the top of the middle, I_{IN} is the input current. Transistor pairs MP1 and MP2, MN3 and MN4 form current mirrors. Transistors MP2 and MN3 form a current comparator. The current comparison result is fed back to the gate of transistor MN1, at the very left, to control MN1 to be on or off. Inversion of the comparison vs MN7 and MP7 is fed back to the gate of transistor MN2 to control MN2 to be off or on. It is important to point out that one and only one of MN1 and MN2 is switched on through the feedback mechanism. Therefore, the current flowing through MP1 is either I_{IL} (the current controlling for I_{H2L}) or the sum of I_{IL} and I_{IW} (the width control current). The two current sources I_{IL} and I_{IW} control the two switching currents I_{L2H} and I_{H2L}. Transistors MP3 and MP4, MN5 and MN6, with two current sources I_{OH} and I_{OW}, form the output end of this circuit. These four transistors work in a similar way as MP1 and MP2, MN1 and MN2. Therefore, the output (vertical height and width) is controlled by the two current sources I_{OH} and I_{OW}.

When the input current $I_{IN} = 0$, the gate voltage of transistor MP7 and MN7 is high, the transistors MN1 and MN6 are on, and the transistors MN2 and MN5 are off. Therefore the current in MP1 is $I_{IL} + I_{IW}$, which is compared with the input current I_{IN}. At the same time the output current $I_{OUT} = -(I_{OH} + I_{OW})$. When

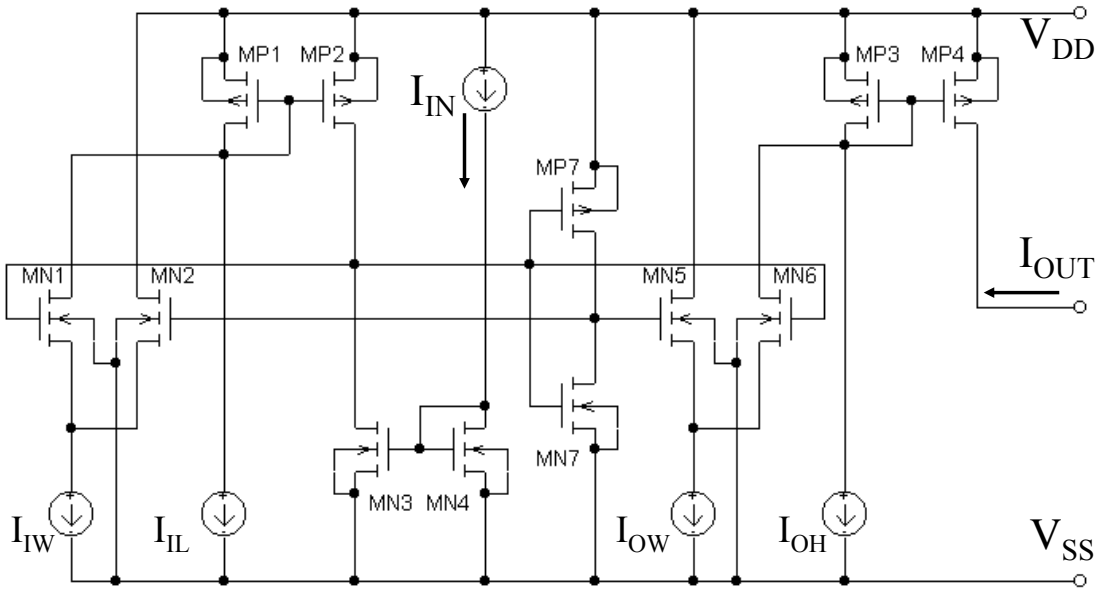

Figure 3.2: Schematic of the CMOS current-input current-output hysteresis circuit in fourth quadrant.

I_{IN} sweeps from 0 to high, the switching occurs at $I_{IN} = I_{IL} + I_{IW}$, MN2 and MN5 are turned on and MN1 and MN6 are turned off. The output current jumps from $-(I_{OH} + I_{OW})$ to $-I_{OH}$ and the current through MP1 switches from $I_{IL} + I_{IW}$ to I_{IL}. When I_{IN} sweeps from high to zero, the switching occurs at $I_{IN} = I_{IL}$, and the output I_{OUT} jumps from $-I_{OH}$ to $-(I_{OH} + I_{OW})$.

The assumed positive directions of the input and output currents are shown by the arrows in Figure 3.2; note that $I_{OUT} < 0$. The switching currents, I_{H2L} and I_{L2H} are given in terms of current source values by Equations (3.4). Similarly the output high and output low, I_+ and I_-, are given in Equations (3.5). The center location of the hysteresis ($I_{IC},\ I_{OC}$) is given in Equations (3.6), and the width I_W

and height I_H are given in Equations (3.7).

$$\begin{aligned} I_{H2L} &= I_{IL} \\ I_{L2H} &= I_{IL} + I_{IW} \end{aligned} \tag{3.4}$$

$$\begin{aligned} I_{+} &= -I_{OH} \\ I_{-} &= -\left(I_{OH} + I_{OW}\right) \end{aligned} \tag{3.5}$$

$$\begin{aligned} I_{IC} &= (I_{L2H} + I_{H2L})/2 = (2I_{IL} + I_{IW})/2 \\ I_{OC} &= (I_{+} + I_{-})/2 = -(2I_{OH} + I_{OW})/2 \end{aligned} \tag{3.6}$$

$$\begin{aligned} I_W &= I_{L2H} - I_{H2L} = I_{IW} \\ I_H &= I_{+} - I_{-} = I_{OW} \end{aligned} \tag{3.7}$$

PSpice simulation results are shown in Figure 3.3. For all PMOS transistors, the width to length ratio is $(W/L) = (4\mu m/12\mu m)$. And for all NMOS transistors, $(W/L) = (4\mu m/12\mu m)$. $V_{DD} = 3V$ and $V_{SS} = -3V$. The top plot of Figure 3.3 is I_{OUT} vs I_{IN} when I_{IN} sweeps from low to high, the middle one is I_{OUT} vs I_{IN} when I_{IN} sweeps from high to low, and the bottom plot is overlaying the above two on top of each other.

PSpice simulation results with different biasing currents are shown in Figure 3.4. For each set of biasing currents, the plot is I_{OUT} vs I_{IN} with the input current I_{IN} sweeping in both directions.

We have achieved complete control on the hysteresis, position, width and height, but there are limitations to the circuit shown in Figure 3.2. Although it has full adjustment of the four binary hysteresis parameters, the adjustment range is limited. It is clear that the bias currents I_{IL} and I_{OH} can not be negative numbers.

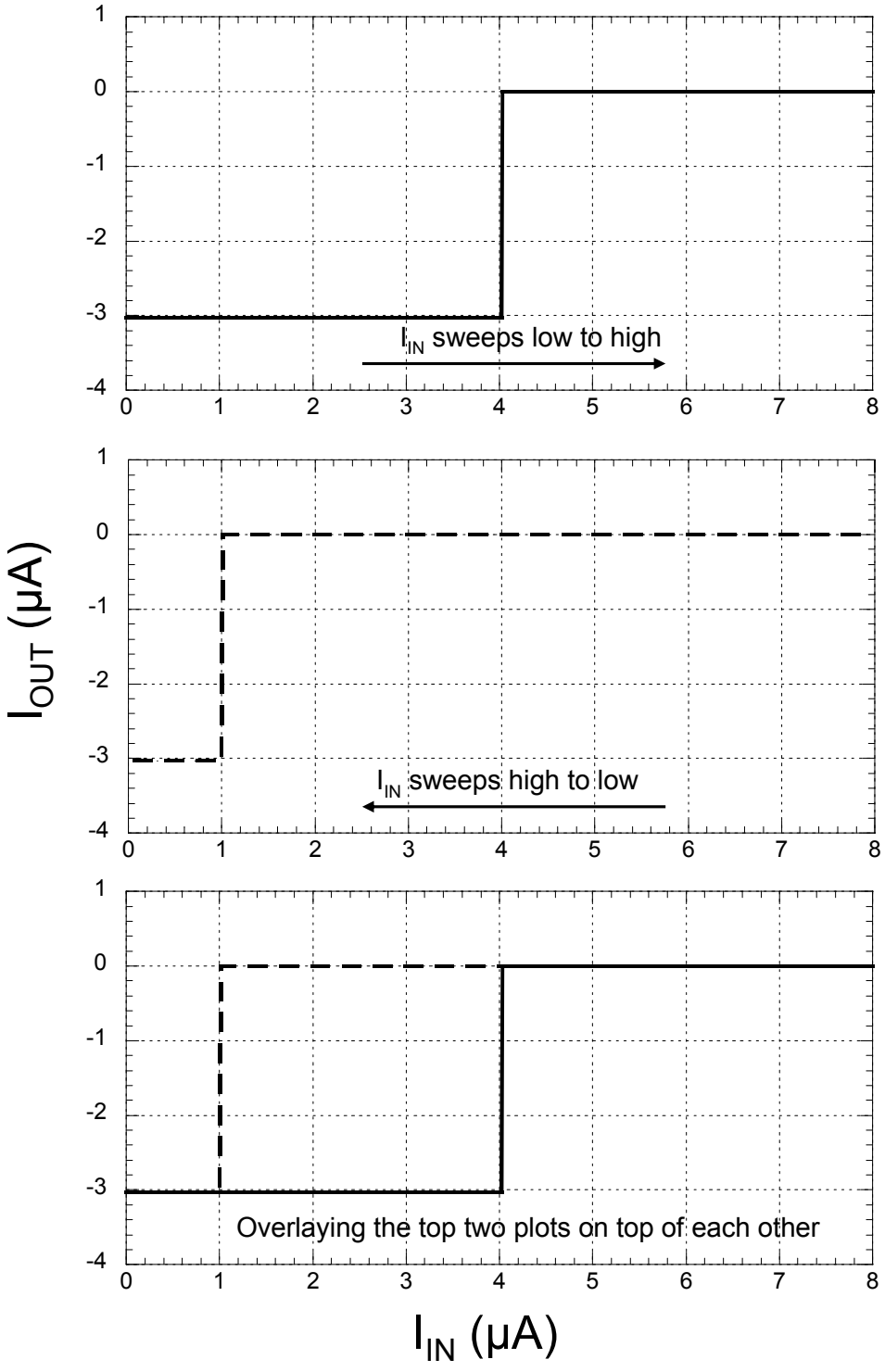

Figure 3.3: PSpice simulation results for the current-input current-output hysteresis circuit in the 4th quadrant, shown in Figure 3.2.

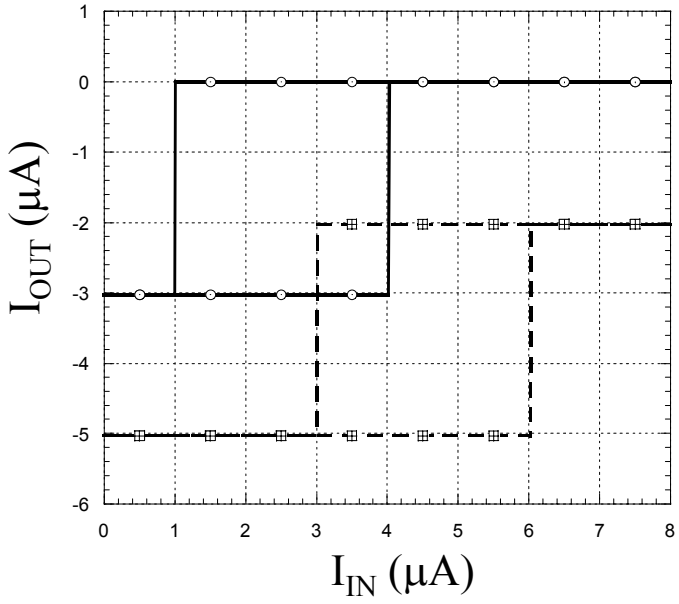

Figure 3.4: PSpice simulation results for the current-input current-output hysteresis circuit in the 4th quadrant, shown in Figure 3.2. The solid line with circles is I_{OUT} vs I_{IN} when $I_{IL} = 1\mu A$, $I_{IW} = 3\mu A$, $I_{OH} = 0\mu A$, and $I_{OW} = 3\mu A$. The dashed line with squares is I_{OUT} vs I_{IN} when $I_{IL} = 3\mu A$, $I_{IW} = 3\mu A$, $I_{OH} = 2\mu A$, and $I_{OW} = 3\mu A$.

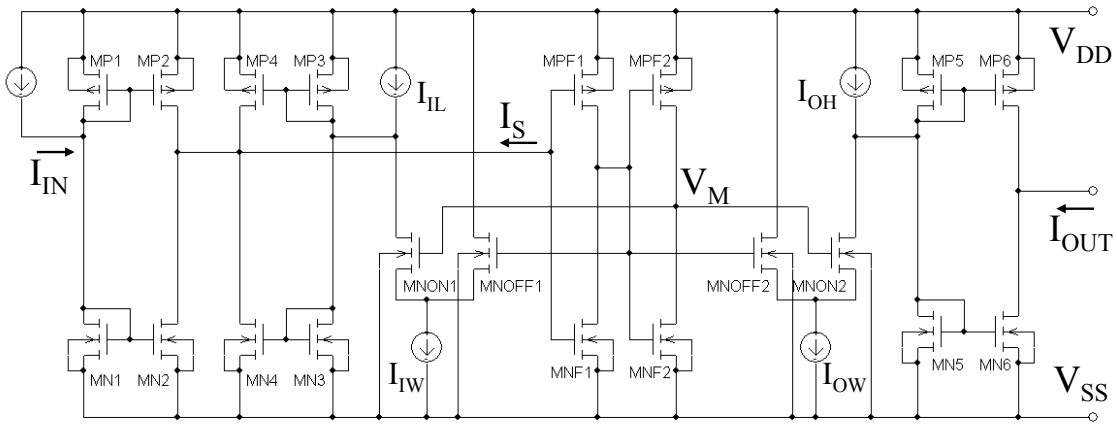

Figure 3.5: Schematic of the current-input current-output forward binary hysteresis circuit working in the full input and output range, all four quadrants.

Therefore, since $I_{OUT} < 0$, the operational range of this current-input current-output hysteresis circuit lies in the 4th quadrant of the input-output plane.

3.2.2 CMOS Current-Input Current-Output Binary Hysteresis Circuit in All Four Quadrants

3.2.2.1 Schematic and Operation Principle

To overcome the quadrant shortcoming of the circuit in Figure 3.2, bi-directional current mirrors are used to replace all the current mirrors and current sinks. The current-input current-output binary hysteresis circuit working with both positive and negative values is achieved by the schematic shown in Figure 3.5.

The arrows in Figure 3.5 show the assumed positive directions of the input and output currents. When the input current I_{IN} is negative and very low and is

overpowering the effects of both I_{IL} and I_{IW}, I_S is negative in the direction defined in Figure 3.5 and consequently charges up the gates of transistor MPF1 and MNF1 to be high, and V_M is high. On the input end, transistor MNON1 is on and MNOFF1 is off, therefore, $I_S = I_{IN} + (I_{IL} - I_{IW}) = I_{IN} - (-I_{IL} + I_{IW})$. On the output end, transistor MNON2 is on and MNOFF2 is off, and the output current $I_{OUT} = I_{OH} - IOW$. In the case of I_{IN} sweeping from low to high, negative to positive, the switching happens when $I_{IN} = (-I_{IL} + I_{IW})$, then I_S becomes positive and discharges the gates of transistors MPF1 and MNF1, turning MNON1 and MNON2 off, and turning MNOFF1 and MNOFF2 on, I_S becomes $I_{IN} - (-I_{IL})$ and I_{OUT} jumps to I_{OH}. When the input current I_{IN} is positive and very high, I_S is positive, the gates of transistor MPF1 and MNF1 are low, and V_M is low. At the input end, transistor MNON1 is off and MNOFF1 is on, $I_S = I_{IN} + I_{IL} = I_{IN} - (-I_{IL})$. At the output end, transistor MNON2 is on and MNOFF2 is off, and the output current $I_{OUT} = I_{OH}$. In the case of I_{IN} sweeping from high to low, the switching happens when $I_{IN} = (-I_{IL})$, then I_S becomes negative and charges the gates of transistors MPF1 and MNF1, turning MNON1 and MNON2 on, and turning MNOFF1 and MNOFF2 off, I_S switches to $I_{IN} - (-I_{IL} + I_{IW})$ and I_{OUT} switches to $I_{OH} - I_{OW}$. The hysteresis curve is a forward one, with $I_{H2L} < I_{L2H}$.

The switching currents, I_{H2L} and I_{L2H} are given in terms of current source values by Equations (3.8). The output high and output low, I_+ and I_-, are given in Equations (3.9). The center (I_{IC}, I_{OC}), the width I_W, and the height I_H of the

forward hysteresis are given in Equations (3.10) and Equations (3.11).

$$\begin{aligned} I_{H2L} &= -I_{IL} \\ I_{L2H} &= -I_{IL} + I_{IW} \end{aligned} \tag{3.8}$$

$$\begin{aligned} I_{+} &= I_{OH} \\ I_{-} &= I_{OH} - I_{OW} \end{aligned} \tag{3.9}$$

$$\begin{aligned} I_{IC} &= (I_{L2H} + I_{H2L})/2 = (-2I_{IL} + I_{IW})/2 \\ I_{OC} &= (I_{+} + I_{-})/2 = (2I_{OH} - I_{OW})/2 \end{aligned} \tag{3.10}$$

$$\begin{aligned} I_{W} &= I_{H2L} - I_{L2H} = I_{IW} \\ I_{H} &= I_{+} - I_{-} = I_{OW} \end{aligned} \tag{3.11}$$

3.2.2.2 PSpice Simulations

The simulation results are shown in Figure 3.6. For all PMOS transistors, the width to length ratio is $(W/L) = (12\mu m/8\mu m)$. And for all NMOS transistors, $(W/L) = (4\mu m/8\mu m)$. $V_{DD} = 3.0V$ and $V_{SS} = -3.0V$. For all the plots, I_{IN} is the x-axis and I_{OUT} is the y-axis in the units of μA.

The operational range of the binary current-input current-output circuit in Figure 3.5 is determined by the operational range of the bi-directional current mirrors and the maximum currents that can be carried by MNON1, MNOFF1, MNON2, and MNOFF2. For the bi-directional current mirrors to work properly, for example, the one formed by transistors MN1, MN2, MP1, and MP2, all the transistors are in saturation. The maximum currents through transistors MNON1, MN1, and MP1 are given by Equations (3.12). For the chosen transistor width to length ratio,

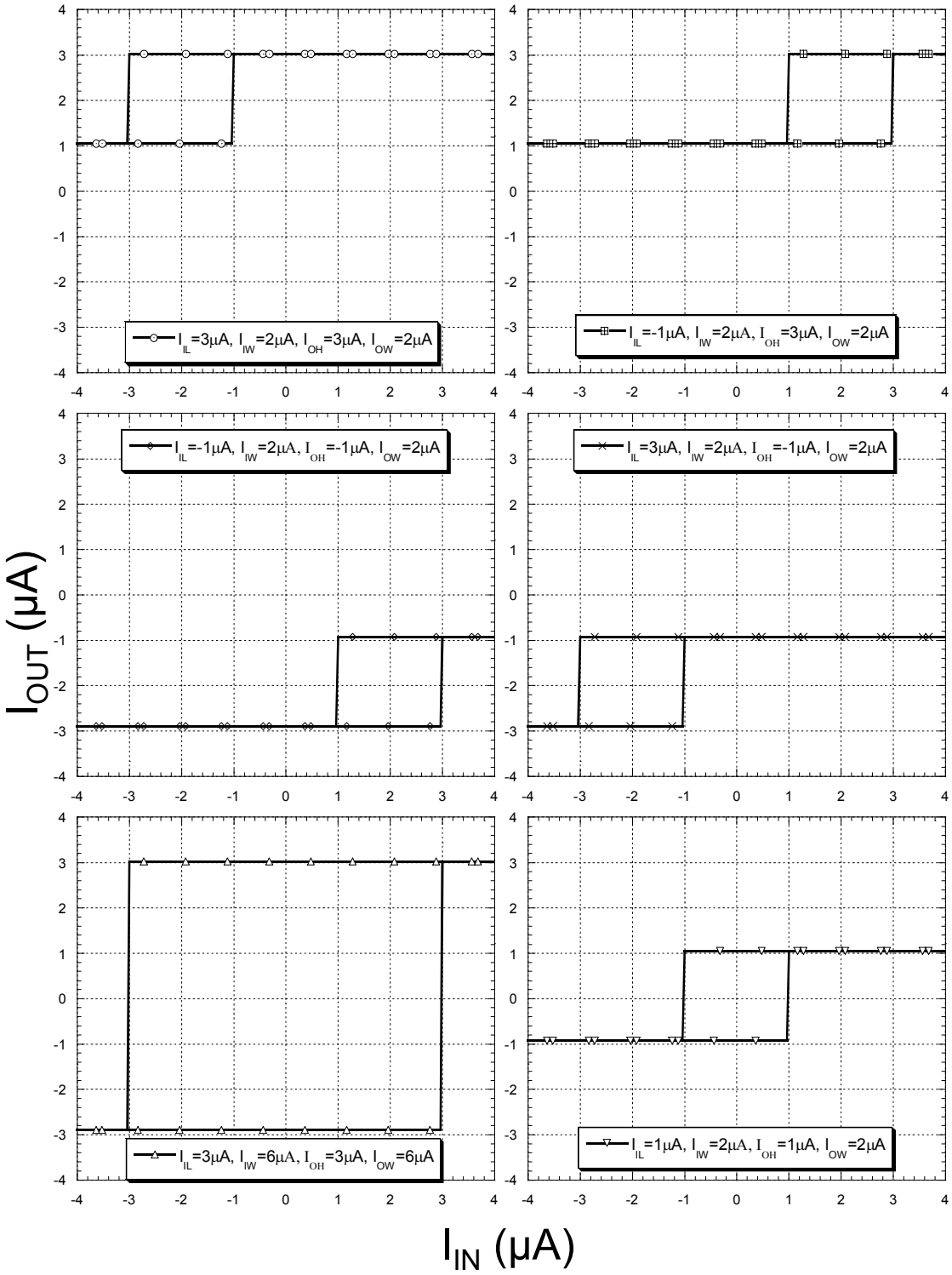

Figure 3.6: PSpice simulation results for the current-input current-output forward hysteresis circuit with full operating range, shown in Figure 3.5.

the bidirectional current mirror works in the range of about $-200\mu A$ to $+200\mu A$, and the maximum current that can flow through MNON1 (or MNOFF1, MNON2, MNOFF2) is $200\mu A$. Therefore, the operational range of the hysteresis is given by Equations (3.13).

$$\begin{aligned} I_{NMON1}(MAX) &= \beta_{MNON1}\left(V_{DD} - V_{SS} - V_{THN}\right)^2 \\ I_{MN1}(MAX) &= \beta_{MN1}\left(V_{DD} - V_{SS} - V_{THN} - V_{THP}\right)^2 \\ I_{MP1}(MAX) &= \beta_{MP1}\left(V_{DD} - V_{SS} - V_{THN} - V_{THP}\right)^2 \end{aligned} \tag{3.12}$$

$$\begin{aligned} &-200\mu A < I_{H2L} < I_{L2H} < 200\mu A \\ &I_{L2H} - I_{H2L} < 200\mu A \\ &-200\mu A < I_{-} < I_{+} < 200\mu A \\ &I_{+} - I_{-} < 200\mu A \end{aligned} \tag{3.13}$$

Simulation results of the frequency response of the current-input current-output binary hysteresis circuit, shown in Figure 3.5, are shown in Figure 3.7. The input current source I_{IN} is a triangular wave with the magnitude of $80\mu A$, and the frequencies of $10KHz$, $100KHz$, $1MHz$, and $2MHz$. The hysteresis has sharp transition when frequency is up to $100KHz$. With the increasing of frequency, the hysteresis starts to lose the sharp shape and becomes wider due to the parasitic capacitance effects.

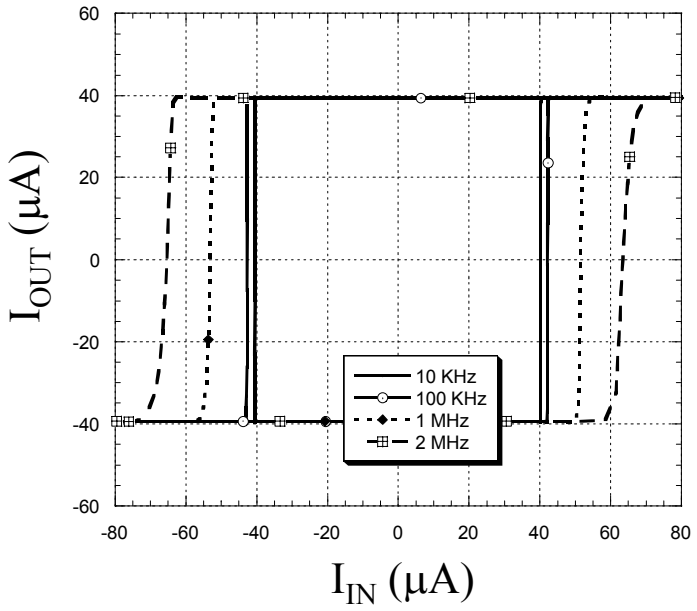

Figure 3.7: Frequency response of the current-input current-output forward binary hysteresis circuit shown in Figure 3.5. $I_{IL} = 40\mu A$, $I_{IW} = 80\mu A$, $I_{OH} = 40\mu A$, and $I_{OW} = 80\mu A$.

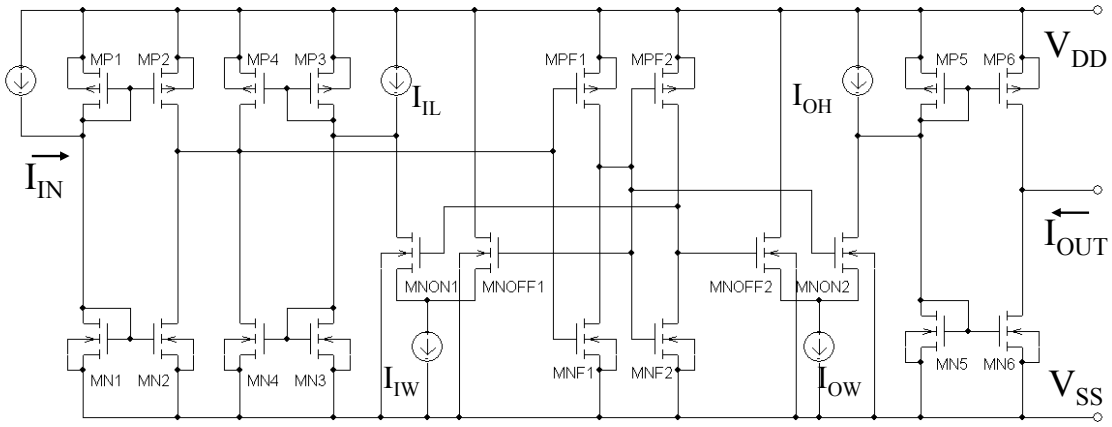

Figure 3.8: Schematic of the current-input current-output reverse binary hysteresis circuit working in the full input and output range, all four quadrants.

3.2.2.3 CMOS Current-Input Current-Output Reverse Binary Hysteresis Circuit

The current-input current-output hysteresis circuit, shown in Figure 3.5, only gives forward binary hysteresis. A little variation on the circuit design can yield reverse binary hysteresis. The gate of transistor MNOFF2 is connected to the drains of MNF2 and MPF2, instead of the gates of MNF2 and MNF2, as in Figure 3.5, and the gate of transistor MNON2 is connected to the gates of MNF2 and MPF2, instead of the drains of MNF2 and MPF2, as in Figure 3.5. The schematic of the binary hysteresis circuit that gives reverse binary hysteresis is shown in Figure 3.8. The simulation results are shown in Figure 3.9.

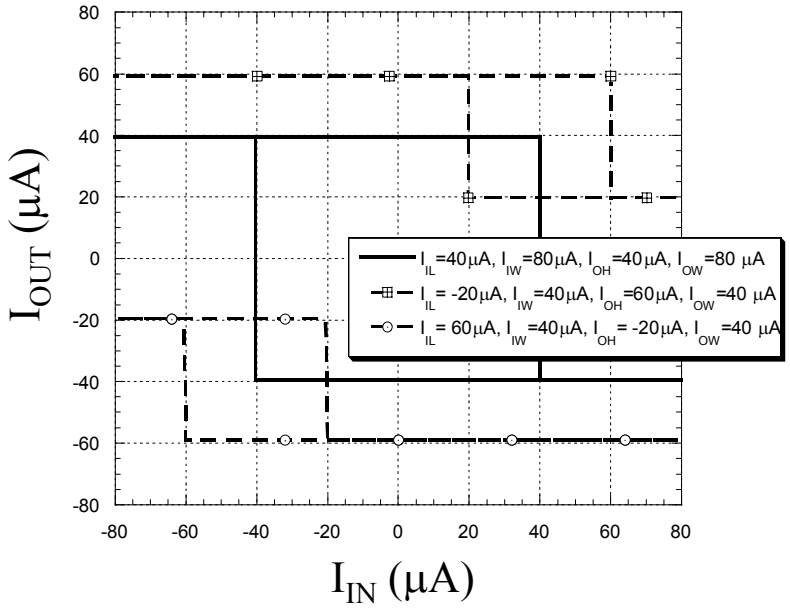

Figure 3.9: PSpice simulation results for the current-input current-output reverse binary hysteresis circuit with full operating range, shown in Figure 3.8.

3.2.3 Summary

CMOS current-input current-output forward and reverse binary circuits with full level and jump point adjustment via external current sources have been achieved. The operating range of the binary hysteresis is extended to all four quadrants. The PSpice simulation results demonstrate its full adjustment function.

3.3 CMOS Voltage-Input Voltage-Output Binary Hysteresis Circuits with Full Control in All Four Quadrants

3.3.1 Schematic and Operation Principle

The schematic of the voltage-input voltage-output reverse binary hysteresis circuit is shown in Figure 3.10. Notice that all the bodies of PMOS transistors are biased to V_{DD} and all the bodies of NMOS transistors are biased to V_{SS}, as were automatically the cases for Figure 3.5 and Figure 3.8. A differential amplifier was used as a voltage comparator. Transistor pairs MP1 and MP3, MP2 and MP4, and MN3 and MN4 are matching pairs that form current mirrors. If the gate voltage of transistor MN1 is higher than the gate voltage of MN2, the current I_S is positive with the direction indicated in Figure 3.10, therefore, the gate voltages of the inverter formed by transistor pair MPF and MNF are discharged and V_M will reach V_{DD}. Similarly, if the gate voltage of MN1 is lower than the gate voltage of MN2, I_S is negative and the gate voltages of MPF and MNF are charged and V_M will reach V_{SS}. The feedback is set up by using the inverter formed by transistor pair MPI and MNI, with the source of PMOS MPI biased to a voltage source V_{IH} and the source of MNOS MNI biased to a voltage source V_{IL}. With V_M being V_{DD} or V_{SS}, the gate voltage of MN2 is biased to V_{IL} or V_{IH}. The output end is formed by the inverter MPO and MNO, with the source of PMOS MPO biased to V_{OH} and the source of NMOS MNO biased to V_{OL}, therefore, the output voltage will be either V_{OH} or V_{OL}.

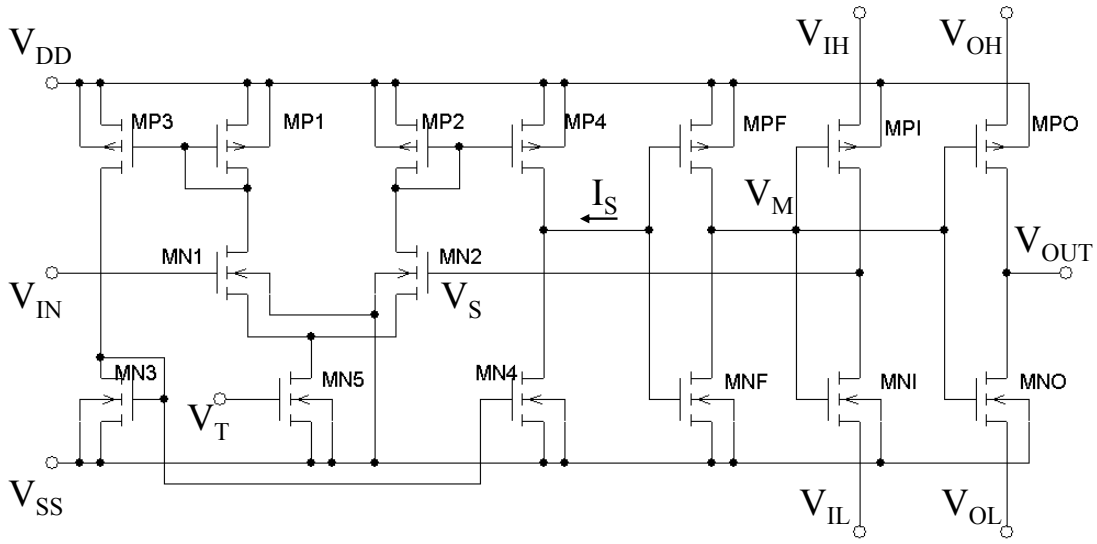

Figure 3.10: Schematic of the voltage-input voltage-output reverse binary hysteresis circuit working in all four quadrants, with full control.

In the case of V_{IN} sweeping from V_{SS} to V_{DD}, initially, V_{IN} is low, I_S is negative, $V_M = V_{SS}$, $V_S = V_{IH}$, and $V_{OUT} = V_{OH}$. The switching occurs when V_{IN} is higher than $V_S = V_{IH}$, then I_S becomes positive, V_M switches from V_{SS} to V_{DD}, and V_{OUT} from V_{OH} to V_{OL}. Also, at the same time, V_S switches from V_{IH} to V_{IL}.

In the case of V_{IN} sweeping from V_{DD} to V_{SS}, initially, V_{IN} is high, I_S is positive, $V_M = V_{DD}$, $V_S = V_{IL}$, and $V_{OUT} = V_{OL}$. The switching occurs when V_{IN} is lower than $V_S = V_{IL}$, then I_S becomes negative, V_M switches from V_{DD} to V_{SS}, and V_{OUT} from V_{OL} to V_{OH}, and V_S switches from V_{IL} to V_{IH}.

The voltage-input and voltage-output hysteresis circuit, shown in Figure 3.10, gives reverse hysteresis curve, with $V_{L2H} < V_{H2L}$. The switching voltages, V_{H2L} and V_{L2H} are given in terms of bias voltage source values by Equations (3.14). The output high and output low, V_+ and V_-, are given in Equations (3.15). The center

position ($V_{IC},\ V_{OC}$), width V_W and height V_H of the hysteresis are given in Equations (3.16) and Equations (3.17).

$$\begin{aligned} V_{H2L} &= V_{IH} \\ V_{L2H} &= V_{IL} \end{aligned} \tag{3.14}$$

$$\begin{aligned} V_{+} &= V_{OH} \\ V_{-} &= V_{OL} \end{aligned} \tag{3.15}$$

$$\begin{aligned} V_{IC} &= (V_{IH} + V_{IL})/2 \\ V_{OC} &= (V_{OH} + V_{OL})/2 \end{aligned} \tag{3.16}$$

$$\begin{aligned} V_W &= V_{IH} - V_{IL} \\ V_H &= V_{OH} - V_{OL} \end{aligned} \tag{3.17}$$

3.3.2 PSpice Simulations

PSpice simulation results for the circuit in Figure 3.10 are shown in Figure 3.11. V_{IN} is the x-axis and V_{OUT} is the y-axis in the units of Volts for all the plots. $V_{DD} = 3.0V$, $V_{SS} = -3.0V$, and the tail voltage $V_T = -2.0V$. For NMOS transistors MN1 and MN2, $(W/L) = (8\mu m/4\mu m)$, for all the other NMOS transistors, $(W/L) = (4\mu m/4\mu m)$, for all the PMOS transistors, $(W/L) = (12\mu m/4\mu m)$.

The operational range of the binary voltage-input voltage-output circuit in Figure 3.10 is given by Equation (3.18).

$$\begin{aligned} -3V \leq V_{L2H} < V_{H2L} \leq 3V \\ -3V \leq V_{-} < V_{+} \leq 3V \end{aligned} \tag{3.18}$$

Simulation results of the frequency response of the binary voltage-input voltage-output, shown in Figure 3.10, are shown in Figure 3.12. The input voltage source

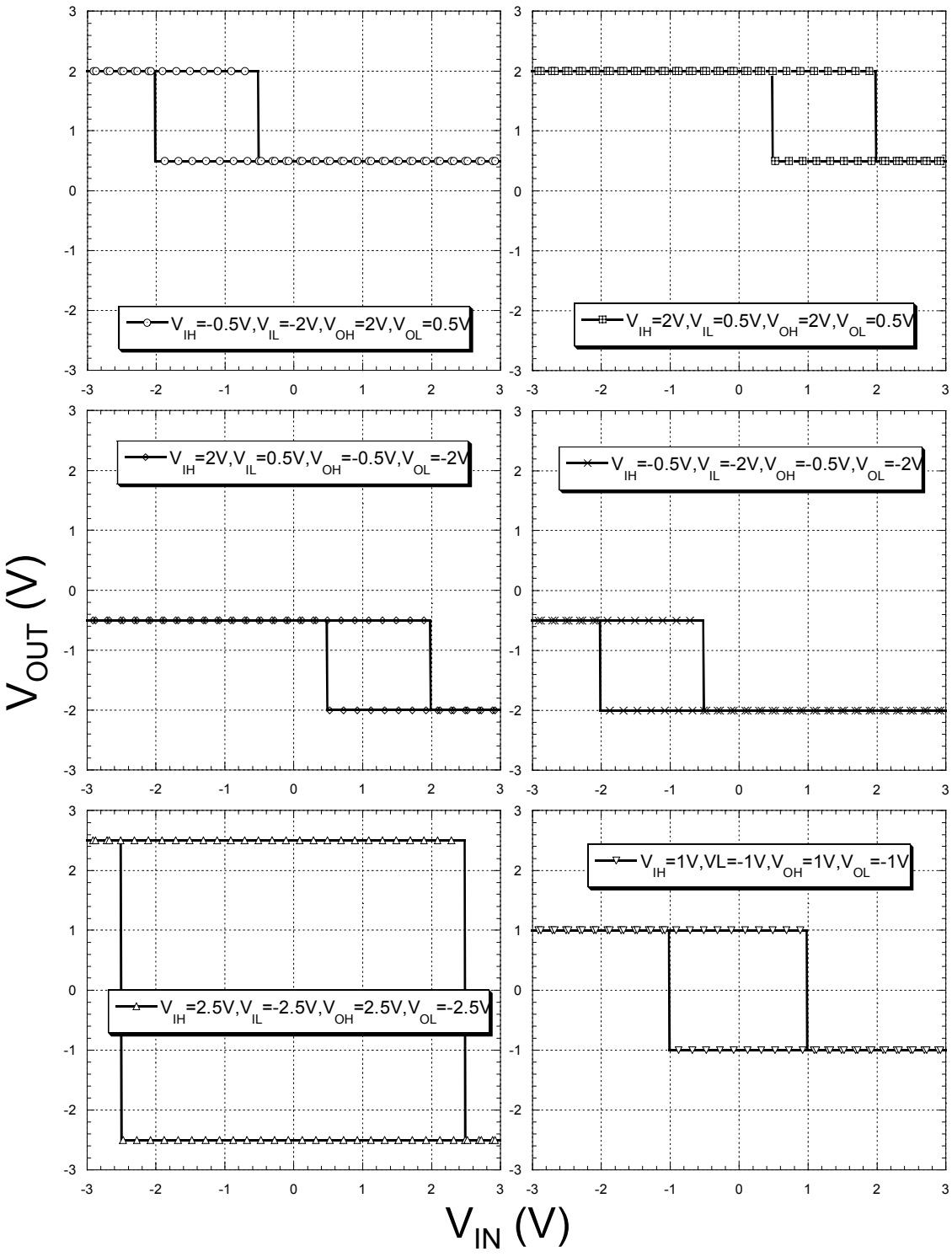

Figure 3.11: PSpice simulation results for the voltage-input voltage-output reverse binary hysteresis circuit with full control, shown in Figure 3.10.

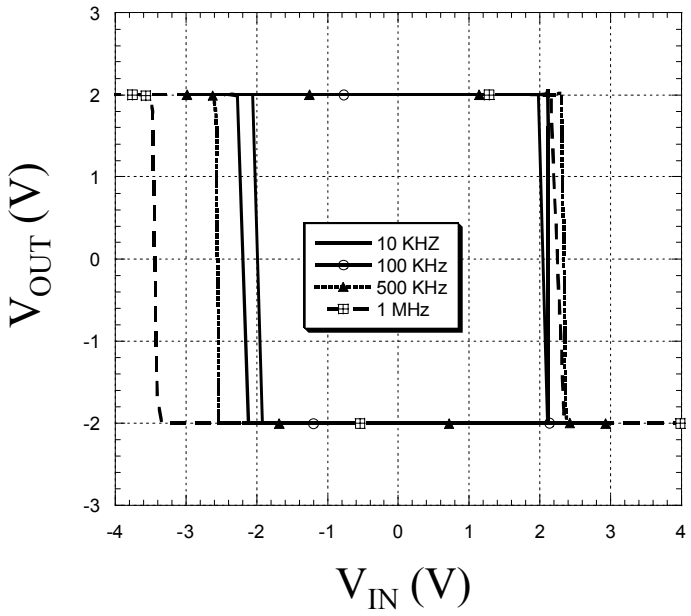

Figure 3.12: Frequency response of the voltage-input voltage-output reverse binary hysteresis circuit shown in Figure 3.10. $V_{IH} = 2V$, $V_{IL} = -2V$, $V_{OH} = 2V$, and $V_{OL} = -2V$.

V_{IN} is a triangular wave with the magnitude of $4V$, and the frequencies of $10KHz$, $100KHz$, $500KHz$, and $1MHz$. The hysteresis has sharp transition when frequency is up to $100KHz$. With the increasing of frequency, the hysteresis starts to lose the sharp shape and becomes wider.

3.3.3 CMOS Voltage-Input Voltage-Output Forward Binary Hysteresis Circuit

The voltage-input voltage-output hysteresis circuit, shown in Figure 3.10, only gives reverse binary hysteresis. A little variation on the circuit design can yield

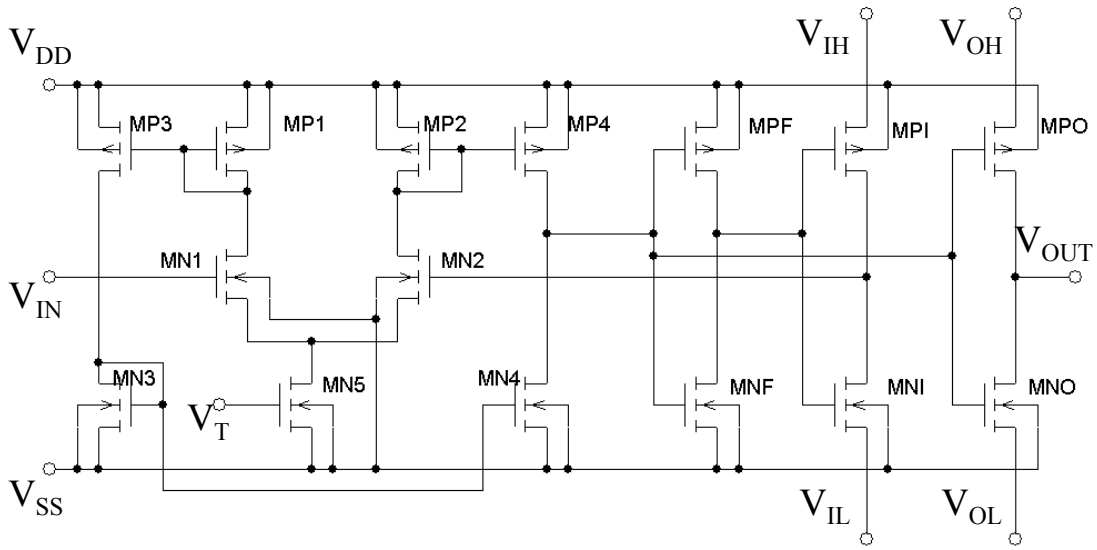

Figure 3.13: Schematic of the voltage-input voltage-output forward binary hysteresis circuit working in the full input and output range, all four quadrants.

forward binary hysteresis. The gates of transistors MNO and MPO are connected to the gates of MNF and MPF, instead of the drains of MNF and MPF, as in Figure 3.10. The schematic of the binary hysteresis circuit that gives forward binary hysteresis is shown in Figure 3.13. The simulation results are shown in Figure 3.14.

3.3.4 Summary

The simulation results demonstrate that both reverse and forward binary hysteresis can be achieved by the CMOS voltage-input voltage-output binary hysteresis circuits, in Figure 3.10 and Figure 3.13. There is full control on the output levels and the jump points via external voltage sources. Both circuits operate in all four quadrants.

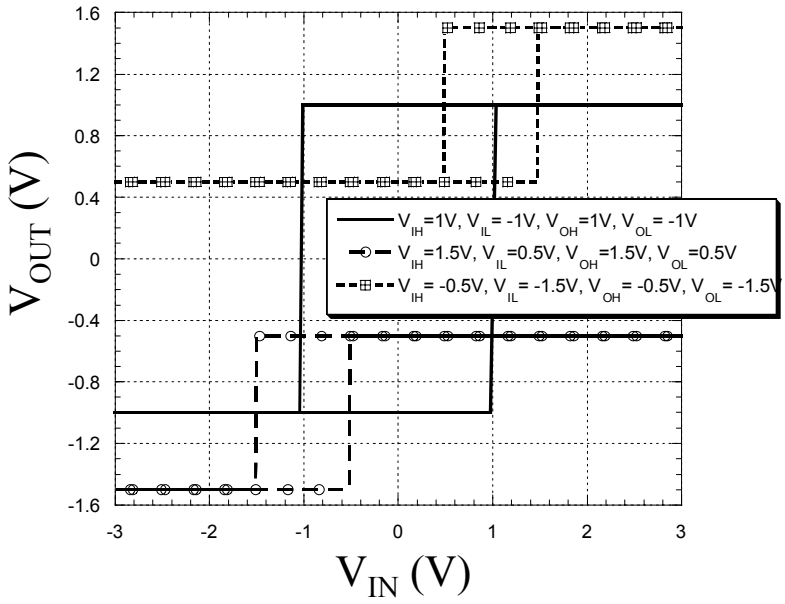

Figure 3.14: PSpice simulation results for the voltage-input voltage-output forward binary hysteresis circuit with full operating range, shown in Figure 3.13.

3.4 CMOS Voltage-Input Current-Output Binary Hysteresis Circuits with Full Control in All Four Quadrants

By combining the design and switching techniques used in the current-input current-output hysteresis circuit, shown in Figure 3.2, and the voltage-input voltage-output hysteresis circuit, shown in Figure 3.10, a voltage-input current-output hysteresis circuit, as well as a current-input voltage-output hysteresis circuit can be achieved. The discussion on the voltage-input current-output hysteresis circuit is given in this section and the current-input voltage-input hysteresis circuit will be discussed in the following Section.

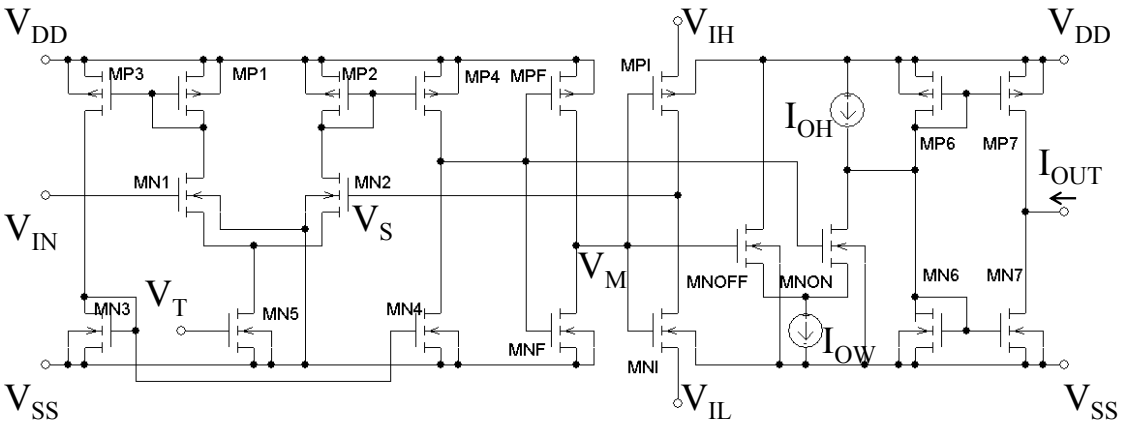

Figure 3.15: Schematic of the voltage-input current-output forward binary hysteresis circuit working in all four quadrants, with full control.

3.4.1 Schematic and Operation Principle

We can take the input part of the voltage-input voltage-output hysteresis circuit, shown in Figure 3.10, and the output part of the current-input current-output hysteresis circuit, shown in Figure 3.5, and combine them to achieve a voltage-input current-output binary hysteresis circuit with full control. The schematic is shown in Figure 3.15.

When V_{IN} is low, $V_M = V_{SS}$, $V_S = V_{IH}$, transistor MNOFF is off and MNON is on, and the output current $I_{OUT} = I_{OH} - I_{OW}$. While V_{IN} is sweeping from V_{SS} to V_{DD}, the switching occurs when V_{IN} is higher than $V_S = V_{IH}$, V_M switches from V_{SS} to V_{DD}, V_S switches from V_{IH} to V_{IL}, transistor MNOFF is turned on and transistor MNON is turned off and I_{OUT} switches from $I_{OH} - I_{OW}$ to I_{OH}. Also, at the same time, V_S switches from V_{IH} to V_{IL}. Similarly, while V_{IN} is sweeping from V_{DD} to V_{SS}, the switching voltage is at $V_{IN} = V_S = V_{IL}$, the output I_{OUT} switches from

I_{OH} to $I_{OH} - I_{OW}$. The switching curve is a forward hysteresis, with $V_{H2L} < V_{L2H}$.

The switching voltages and the output currents are given in Equations (3.19) and Equations (3.20). The center ($V_{IC},\ I_{OC}$), the width V_W and the height I_H of the hysteresis are given in Equations (3.21) and Equations (3.22).

$$\begin{aligned} V_{L2H} &= V_{IH} \\ V_{H2L} &= V_{IL} \end{aligned} \tag{3.19}$$

$$\begin{aligned} I_+ &= I_{OH} \\ I_- &= I_{OH} - I_{OW} \end{aligned} \tag{3.20}$$

$$\begin{aligned} V_{IC} &= (V_{IH} + V_{IL})/2 \\ I_{OC} &= (2I_{OH} - I_{OW})/2 \end{aligned} \tag{3.21}$$

$$\begin{aligned} V_W &= V_{IH} - V_{IL} \\ I_H &= I_{OW} \end{aligned} \tag{3.22}$$

The operational range of the forward hysteresis generated by the voltage-input current-output circuit in Figure 3.15 is given by Equations (3.23).

$$\begin{aligned} -3V \leq V_{H2L} < V_{L2H} \leq 3V \\ -200\mu A < I_- < I_+ < 200\mu A \\ I_+ - I_- < 200\mu A \end{aligned} \tag{3.23}$$

3.4.2 PSpice Simulations

PSpice simulation results for the circuit in Figure 3.15 are shown in Figure 3.16. V_{IN} is the x-axis with the unit of Volts and I_{OUT} is the y-axis in the units of μA for all the plots. $V_{DD} = 3.0V$, $V_{SS} = -3.0V$ and $V_T = -2.0V$. For NMOS transistors

MN1 and MN2, $(W/L) = (8\mu m/4\mu m)$, for all the other NMOS transistors, $(W/L) = (4\mu m/4\mu m)$, for all the PMOS transistors, $(W/L) = (12\mu m/4\mu m)$.

3.4.3 CMOS Voltage-Input Current-Output Reverse Binary Hysteresis Circuit

The voltage-input current-output hysteresis circuit, shown in Figure 3.15, only gives forward binary hysteresis. A little change on the circuit design can yield reverse binary hysteresis. The gate of transistor MNOFF is connected to the gates of MNF and MPF, instead of the drains of MNF and MPF, as in Figure 3.15, and the gate of transistor MNON is connected to the drains of MNF and MPF, instead of the gates of MNF and MPF, as in Figure 3.15. The schematic of the binary hysteresis circuit that gives forward binary hysteresis is shown in Figure 3.17. The simulation results are shown in Figure 3.18.

3.4.4 Summary

The simulation results, shown in Figure 3.16 and Figure 3.18, demonstrate that the CMOS voltage-input voltage-output binary hysteresis circuits, in Figure 3.15 and Figure 3.17 achieve full control on output levels and jump points, via external current and voltage sources. They give both forward and reverse hysteresis in all four quadrants.

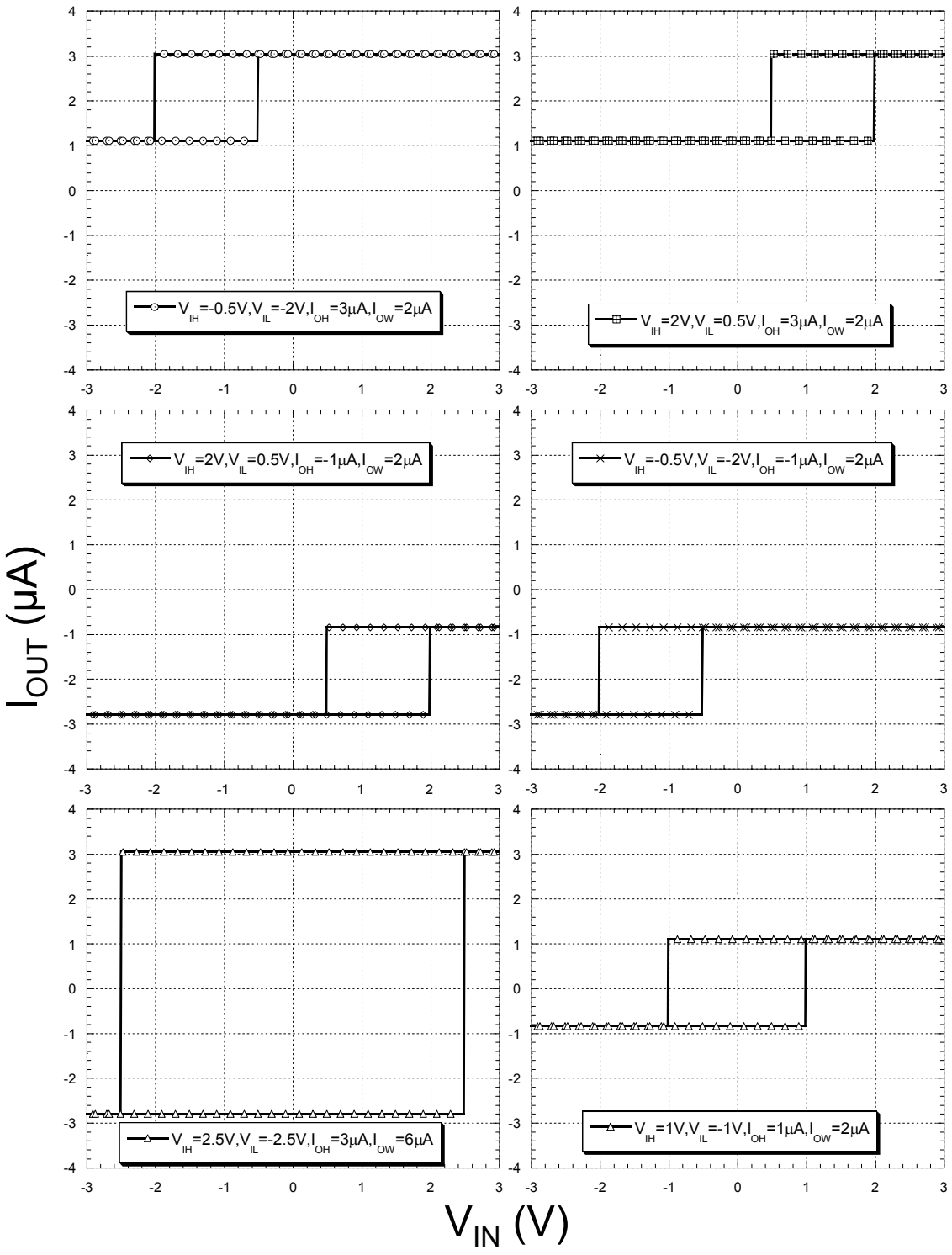

Figure 3.16: PSpice simulation results for the voltage-input current-output forward binary hysteresis circuit with full control, shown in Figure 3.15.

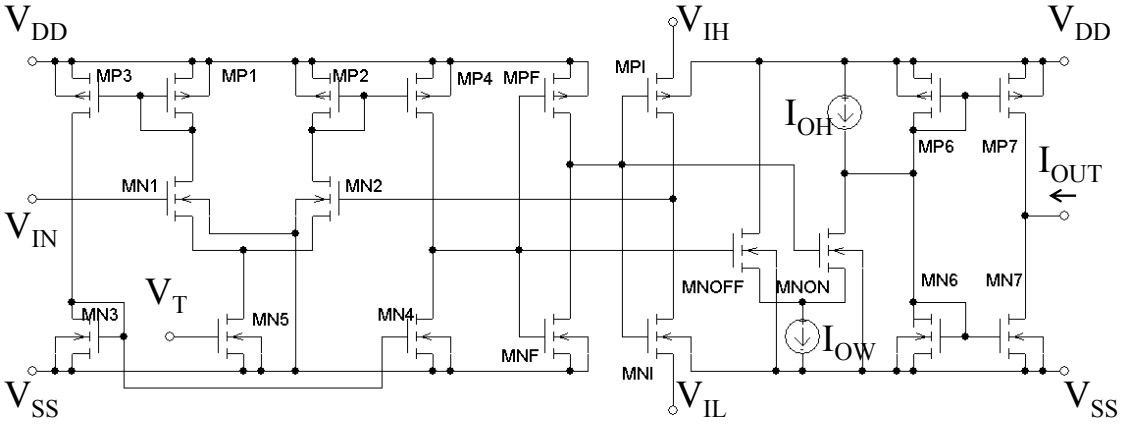

Figure 3.17: Schematic of the voltage-input current-output reverse binary hysteresis circuit working in the full input and output range, all four quadrants.

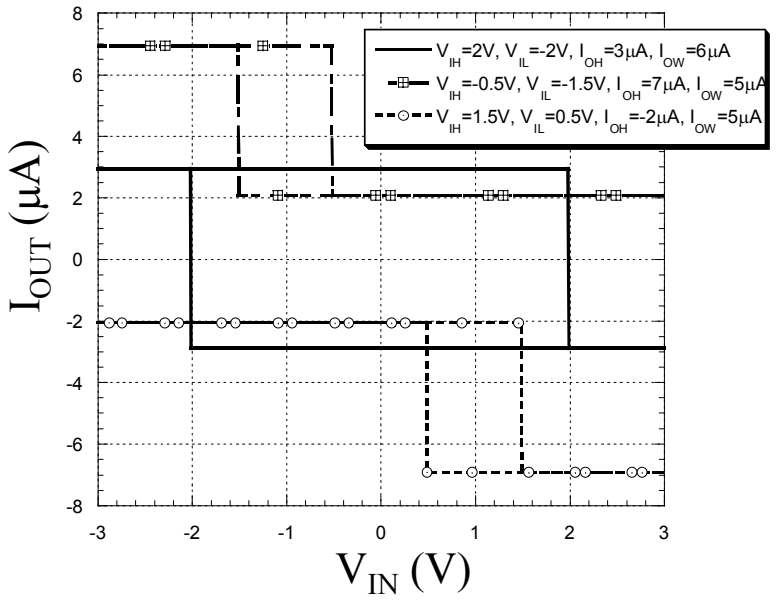

Figure 3.18: PSpice simulation results for the voltage-input current-output reverse binary hysteresis circuit with full operating range, shown in Figure 3.17.

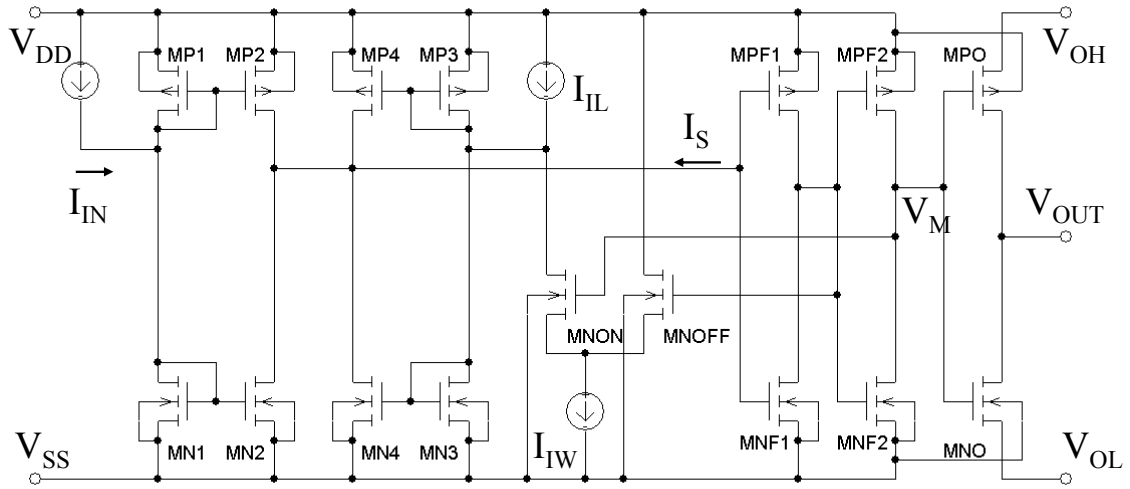

Figure 3.19: Schematic of the current-input voltage-output forward binary hysteresis circuit working in all four quadrants, with full control.

3.5 CMOS Current-Input Voltage-Output Binary Hysteresis Circuits with Full Control in All Four Quadrants

3.5.1 Schematic and Operation Principle

We can take the input part of the current-input current-output hysteresis circuit, shown in Figure 3.5, and the output part of the voltage-input voltage-output hysteresis circuit, shown in Figure 3.10 and combine them to achieve a current-input voltage-output forward binary hysteresis circuit with full control. The schematic is shown in Figure 3.19.

The arrows in Figure 3.19 show the assumed positive directions of the I_{IN} and I_S. When the input current I_{IN} is negative and very low and is overpowering the effects of both I_{IL} and I_{IW}, I_S is negative, which charges up the gates of transistors

MPF1 and MNF1 to be high, and V_M is high, transistor MNON is on and MNOFF is off. Therefore $I_S = I_{IN} + (I_{IL} - I_{IW}) = I_{IN} - (-I_{IL} + I_{IW})$, and the output voltage $V_{OUT} = V_{OL}$. In the case of I_{IN} sweeping from low to high, the switching happens when $I_{IN} = (-I_{IL} + I_{IW})$. Then I_S becomes positive and discharges the gates of transistors MPF1 and MNF1, turning MNON off, and MNOFF on, I_S switches to $I_{IN} - (-I_{IL})$ and V_{OUT} switches to V_{OH}. When the input current I_{IN} is positive and very high, I_S is positive, the gates of transistor MPF1 and MNF1 are low, V_M is low, transistor MNON is off, and MNOFF is on, $I_S = I_{IN} + I_{IL} = I_{IN} - (-I_{IL})$, and the output voltage $V_{OUT} = V_{OH}$. In the case of I_{IN} sweeping from high to low, the switching happens when $I_{IN} = (-I_{IL})$. Then I_S becomes negative and charges the gates of transistors MPF1 and MNF1, turning MNON on, and MNOFF off, I_S switches to $I_{IN} - (-I_{IL} + I_{IW})$ and V_{OUT} switches to V_{OL}. The hysteresis curve is a forward one, with $I_{H2L} < I_{L2H}$.

The switching currents and the output voltages are given in Equations 3.24 and 3.25. The center $(I_{IC},\ V_{OC})$, the width I_W and the height V_H of the forward hysteresis are given in Equations (3.26) and (3.27).

$$\begin{aligned} I_{L2H} &= -I_{IL} + I_{IW} \\ I_{H2L} &= -I_{IL} \end{aligned} \tag{3.24}$$

$$\begin{aligned} V_+ &= V_{OH} \\ V_- &= V_{OL} \end{aligned} \tag{3.25}$$

$$I_{IC} = (-2I_{IL} + I_{IW})/2$$
$$V_{OC} = (V_{OH} + V_{OL})/2 \tag{3.26}$$

$$I_W = I_{IW}$$
$$V_H = V_{OH} - V_{OL} \tag{3.27}$$

The operational range of the forward hysteresis generated by the current-input voltage output circuit in Figure 3.19 is given by Equations (3.28).

$$-200\mu A < I_{H2L} < I_{L2H} < 200\mu A$$
$$I_{L2H} - I_{H2L} < 200\mu A \tag{3.28}$$
$$-3V < V_- < V_+ < 3V$$

3.5.2 PSpice Simulation

PSpice simulation results for the circuit in Figure 3.19 are shown in Figure 3.20. I_{IN} is the x-axis with the unit of μA and V_{OUT} is the y-axis in the units of Volts for all the plots. $V_{DD} = 3.0V$ and $V_{SS} = -3.0V$. For NMOS transistors MN1$\sim$MN4, MNON, and MNOFF $(W/L) = (4\mu m/8\mu m)$, for NMOS transistors, MNF1, MNF2 ,and MNO, $(W/L) = (4\mu m/4\mu m)$. For PMOS transistors MP1$\sim$MP4, $(W/L) = (12\mu m/8\mu m)$, for PMOS transistors, MPF1, MPF2 ,and MPO, $(W/L) = (12\mu m/4\mu m)$.

3.5.3 CMOS Current-Input Voltage-Output Reverse Binary Hysteresis Circuit

The current-input voltage-output hysteresis circuit, shown in Figure 3.19, only gives forward binary hysteresis. A little change in the circuit design can yield reverse

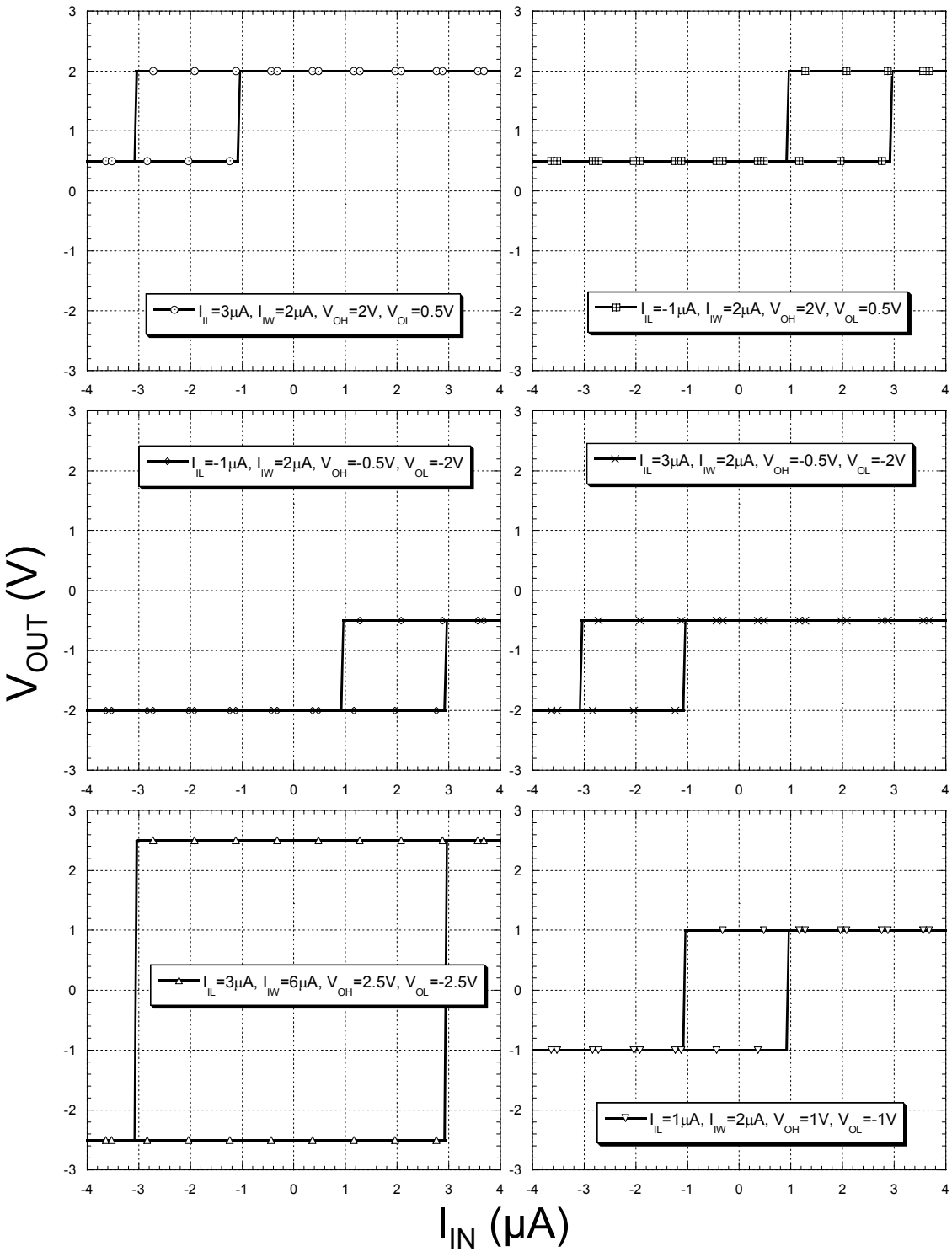

Figure 3.20: PSpice simulation results for the current-input voltage-output forward binary hysteresis circuit with full control, shown in Figure 3.19.

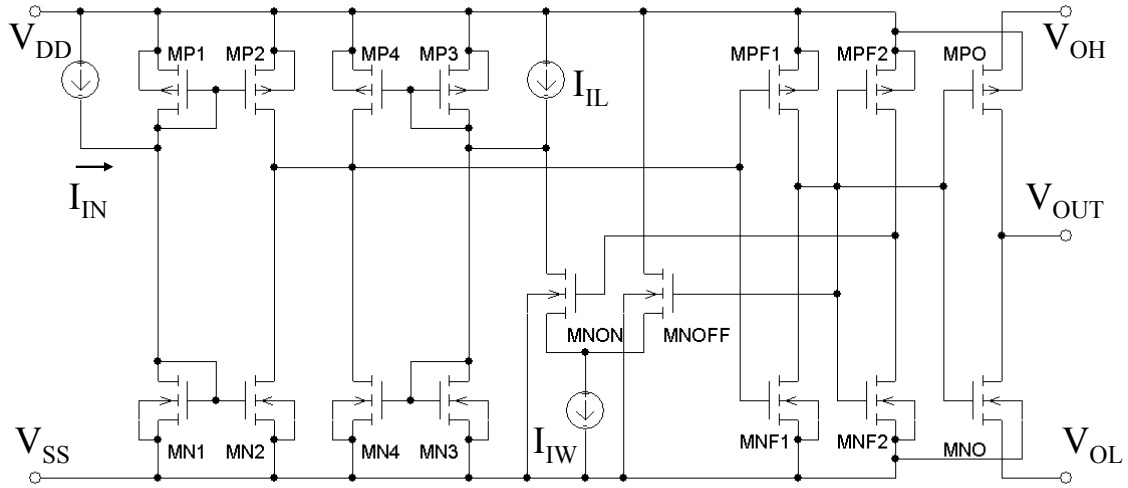

Figure 3.21: Schematic of the current-input voltage-output reverse binary hysteresis circuit working in the full input and output range, all four quadrants.

binary hysteresis. The gates of transistor MPO and MNO are connected to the gates of MNF2 and MPF2, instead of the drains of MNF2 and MPF2, as in Figure 3.19. The schematic of the binary hysteresis circuit that gives forward binary hysteresis is shown in Figure 3.21. The simulation results are shown in Figure 3.22.

3.5.4 Summary

The simulation results demonstrate that the CMOS current-input voltage-output binary hysteresis circuits, in Figure 3.19 and Figure 3.21 achieve full control on the output levels and jump points, via external current and voltage sources. Both circuits operate in all four quadrants.

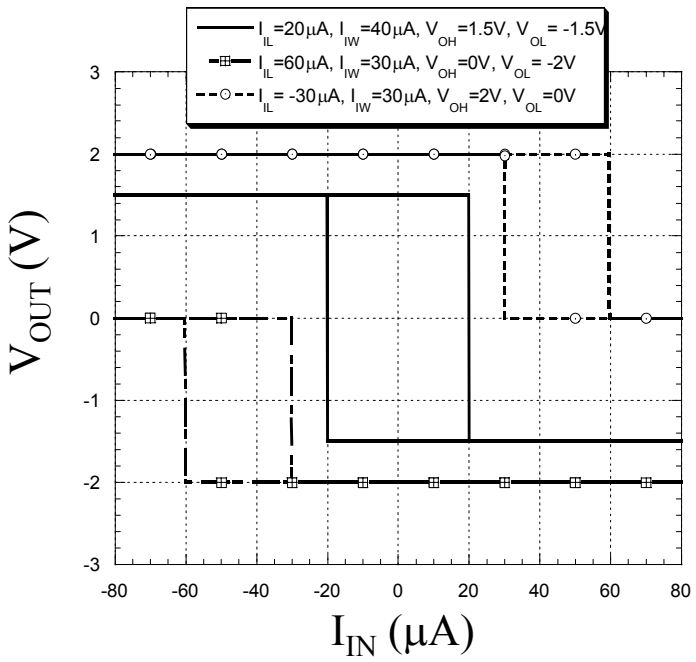

Figure 3.22: PSpice simulation results for the current-input voltage-output reverse binary hysteresis circuit with full operating range, shown in Figure 3.21.

3.6 Summary

CMOS binary forward and reverse hysteresis circuits, with current or voltage input, and current or voltage output have been achieved. Each of the eight hysteresis circuits has full control on the hysteresis and operates in all four quadrants.

Chapter 4

Circuits for Handling Sweeping Signals

4.1 Overview

We have simulated binary hysteresis circuits with full control in all four quadrants, as discussed in Chapter three. To build multi-level and multi-dimensional hysteresis, analogue adders and multipliers that operate in all four quadrants are needed. Also, we would like to have the freedom to convert voltage signals to current signals and current signals to voltage signals linearly. Therefore, in this chapter, analogue adders, multipliers, a linear current voltage converter, and a voltage current converter that can handle sweeping signals are discussed.

For all the simulations in this chapter, MOSIS 1.2 μm transistor models (BSIM1, Level 4, and Run n7ab) are used [37].

4.2 Analogue Adders

4.2.1 Overview

A voltage adder/subtractor is an important element not only in the construction of multi-level and multi-dimensional hysteresis, but also in the construction of multipliers. Adding current signals could be just as simple as tying the nodes together; adding voltage signals is not so trivial. In the past literature, search

shows that there were not many CMOS voltage adders and subtractors. R. Fried and C. C. Enz [15] proposed an accurate voltage adder/subtractor which used the exponential characteristic of MOS transistors biased in weak inversion. Fried's adder/subtractor has low power consumption but limited input range. H. Chaoui [9] proposed an adder that used the characteristic of MOS transistors biased in the triode region, which again, has limited operational range. With $\pm 5V$ voltage supply, Chaoui's adder gave only a positive output range. A. Monpapassorn [34] proposed a wide range voltage adder/subtractor, which used three current conveyors and three current-voltage convertors, with all the transistors biased in saturation region. Monpapassorn's adder had wide positive and negative, input and output ranges, but to serve the programmable purpose, it had many transistors, 13 transistors for each current conveyor. M. Al-Nsour and H. S. Abdel-Aty-Zohdy [1] proposed a MOS voltage adder which had balanced differential inputs and also gave differential output. S. W. Tsay and R. W. Newcomb [55] proposed an adder/subtractor/sign inverter circuit. Although Tsay's adder has both positive and negative voltage supply, it only gave a positive output range.

In this Section, a new voltage adder with single end input and single end output is presented with wide voltage operation range that covers both positive and negative values.

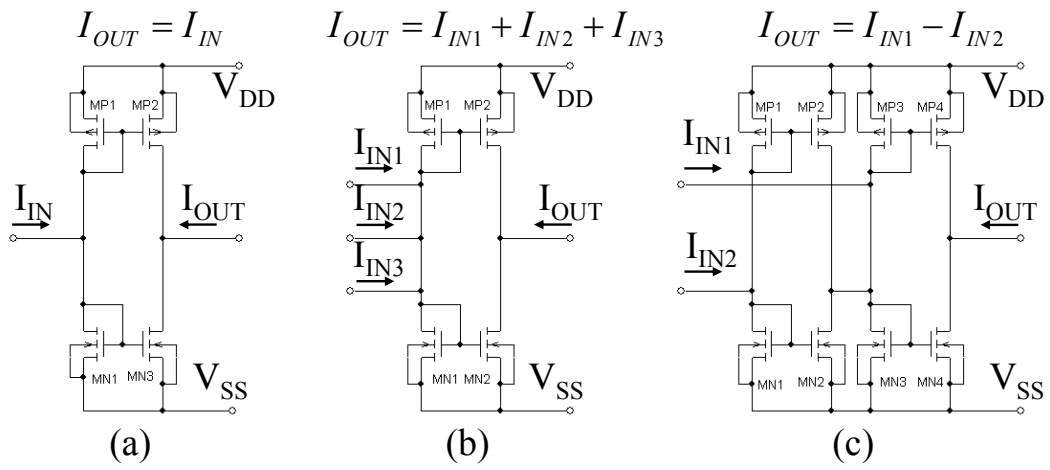

Figure 4.1: Schematics of a current sign inverter, a current adder, and a current subtractor. (a) Sign inverter. (b) Adder. (c) Subtractor.

4.2.2 Analogue Current Adder/Subtractor/Sign Inverter Schematics and Simulation Results

Current domain sign inverting, addition, subtraction are really straight forward; bi-directional current mirrors are used to achieve four quadrant operations of the above calculation. The schematics of a current sign inverter, an adder and a subtractor are shown in Figure 4.1. Using the sign invert, adder, and subtractor circuit shown in Figure 4.1, a two port current mode adder/subtractor is designed. The schematic is shown in Figure 4.2.

Simulation results are shown in Figure 4.3, with $V_{DD} = 3.0V$ and $V_{SS} = -3.0V$. For all PMOS transistors, the width to length ratio is $(W/L) = (4\mu m/5.6\mu m)$. And for all NMOS transistors, $(W/L) = (4.8\mu m/4\mu m)$. The adder works well in the range of $-20\mu A$ to $+20\mu A$ for the two inputs I_X and I_Y.

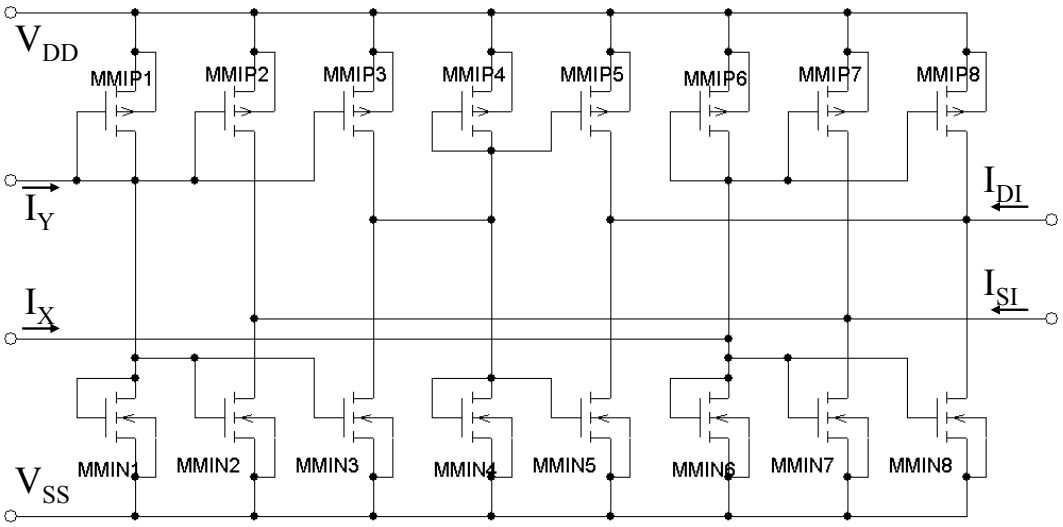

Figure 4.2: Schematics of a current a current adder/subtractor with $I_{SI} = I_X + I_Y$ and $I_{DI} = I_X - I_Y$.

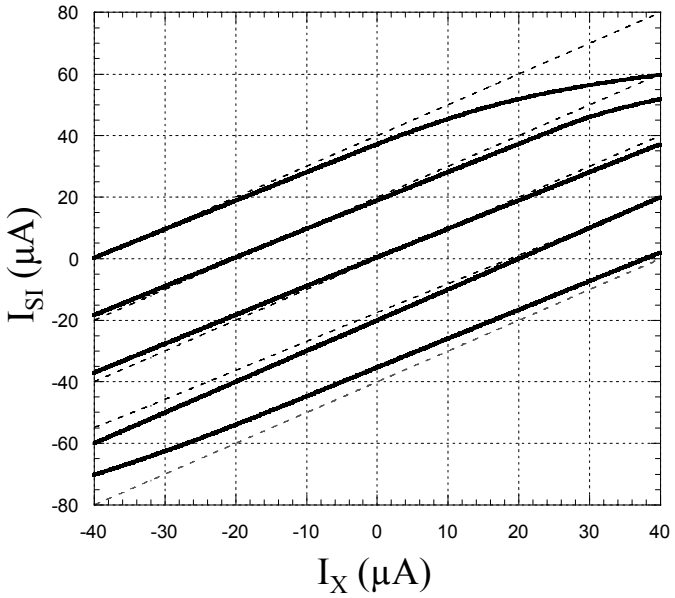

Figure 4.3: Simulation results for the CMOS current adder/subtractor shown in Figure 4.2. I_X sweeps from $-40\mu A$ to $40\mu A$, and I_Y steps from $-40\mu A$ to $40\mu A$ with $20\mu A$ step. The solid line is I_{SI}, and the dashed line is $I_X + I_Y$.

4.2.3 Analysis of Tsay's Voltage Adder/Subtractor/Sign Inverter and Torrance's Common Mode Rejector

The new voltage adder presented in this section is based on two previous works, S. W. Tsay's [55] adder and R. R. Torrance's common mode rejection circuit [54].

The schematic of Tsay's adder/subtractor/sign inverter is shown in Figure 4.4. Two identical differential pairs' output ends are tied together, which forces $I_1 = I_2$. Tsay argued that since $I_1 = K(V_A - V_B)$ and $I_2 = -K(V_C - V_D)$, therefore $V_A - V_B = -(V_C - V_D)$. For an adder, V_D is grounded, and then $V_B = V_A + V_C$. For a subtractor, V_C is grounded, and then $V_B = V_A - V_D$. For a sign inverter, both V_A and V_C are grounded, and then $V_B = -V_D$. The key idea in Tsay's circuit is to force $I_1 = I_2$, which actually is $I_{MN1} - I_{MN2} = -(I_{MN3} - I_{MN4})$. The same result could be achieved by forcing $I_{MN1} = I_{MN4}$ and $I_{MN2} = I_{MN3}$, which leads to a simpler circuit.

R. R. Torrance, T. R. Viswanathan, and J. V. Hanson [54] proposed a common mode rejection circuit, as shown in Figure 4.5, which also used two differential pairs, as in Tsay's adder [55]. Through the current mirror formed by transistor pair MP1 and MP2, $I_{MN1} = I_{MN4}$. Transistors MN1$\sim$MN4 are identical and biased in saturation. To eliminate the body effect on the threshold voltage, all four transistors' bodies are tied to their sources, not the lowest voltage V_{SS}. The sources of MN1 and MN2 are tied together and biased with a current source I, and the sources of MN3 and MN4 are tied together and biased with the same value of current I. Since $I_{MN1} = I_{MN4}$ and $I_{MN1} + I_{MN2} = I_{MN3} + I_{MN4} = I$, $I_{MN2} = I_{MN3}$ is also true.

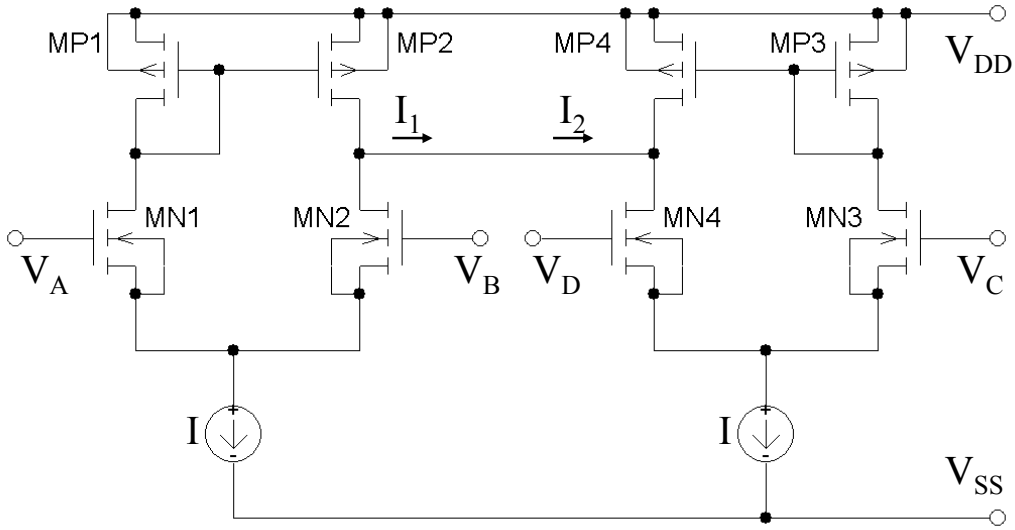

Figure 4.4: Schematic of S. W. Tsay and R. W. Newcomb's [55] adder/subtractor/sign invertor.

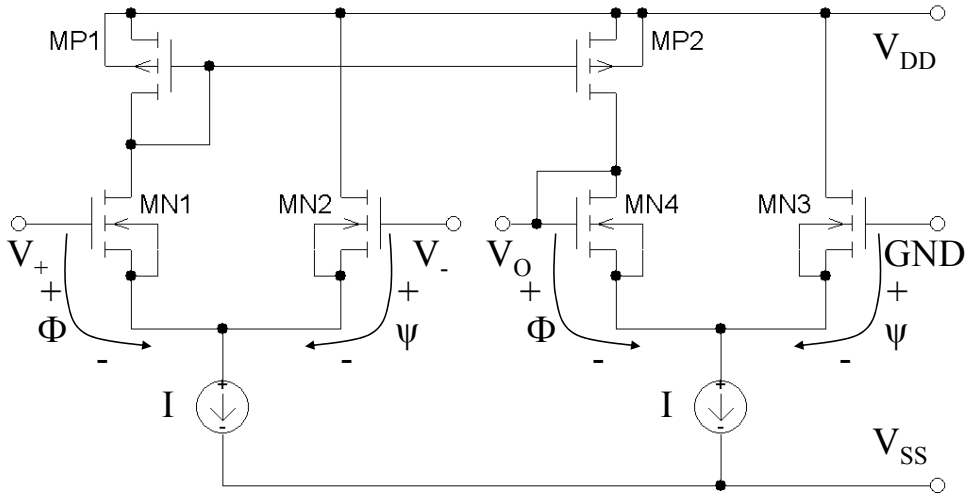

Figure 4.5: Schematic of R. R. Torrance's [54] common mode rejection circuit.

For a transistor in saturation, the drain to source current is given by Equation (4.1), with V_{TH} the threshold voltage. K_N is the transconductance parameter, the same name used in Baker [2], and $\beta = \frac{K_N}{2}\frac{W}{L}$. Since $I_{MN1} = I_{MN4}$, the gate to source voltage drops V_{GS} are the same for MN1 and MN4, which are labeled as Φ in Figure 4.5. Similarly, the gate to source voltage of MN2 and MN3 are the same, Ψ. Apply Kirchhoff voltage law, $V_+ - V_- = \Phi - \Psi$ and $V_{OUT} = \Phi - \Psi$, therefore the output $V_{OUT} = V_+ - V_-$. The voltage difference $\Phi - \Psi$ is given by Equation (4.2), which does not need to be linear for this scheme to work. Similar analysis can be applied on Tsay's adder [55].

$$I = \beta \left(V_{GS} - V_{TH}\right)^2 \tag{4.1}$$

$$\Phi - \Psi = \sqrt{\frac{1}{\beta}}\left(\sqrt{I_{MN1}} - \sqrt{I_{MN2}}\right) = \sqrt{\frac{1}{\beta}}\left(\sqrt{I_{MN4}} - \sqrt{I_{MN3}}\right) \tag{4.2}$$

4.2.4 Analogue Voltage Adder/Subtractor/Sign Inverter Schematic and Operation Principles

By using the ideas presented in S. W. Tsay's [55] adder and R. R. Torrance's common mode rejection circuit [54], a new voltage adder/subtractor/inverter circuit is designed with wide positive and negative, input and output ranges. The schematic of the adder/subtractor/inverter circuit is shown in Figure 4.6. Since the linearity of the circuit is extremely sensitive to the precision of the current source I, transistors MNT1∼MNT4 are used to form cascade mirrors to improve linearity. The bodies of transistors MN1∼MN4 are tied to their sources, not V_{SS}, to eliminate the body effect on the threshold voltage V_{TH}. Therefore, a Pwell is needed in the fabrication,

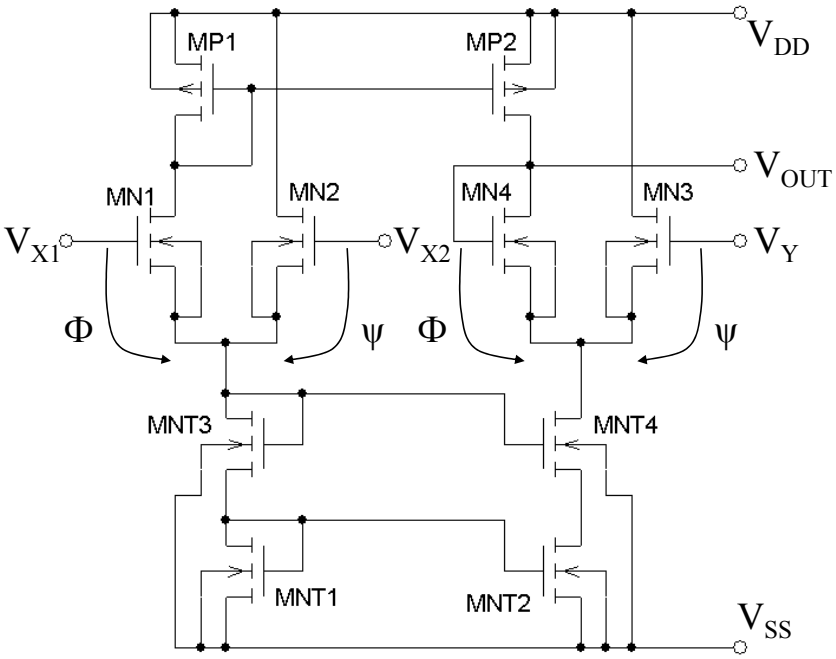

Figure 4.6: Schematic of a new CMOS voltage adder/subtractor/sign invertor.

which requires larger fabrication area than the ones without Pwell.

The voltage difference $\Phi - \Psi$, in Figure 4.6 is given by Equation (4.3), and the output voltage V_{OUT} is given by Equation (4.4). The circuit in Figure 4.6 is an adder if V_{X2} is grounded, a subtractor if V_{X1} is grounded, and a sign inverter if both V_{X1} and V_Y are grounded. The output voltage V_{OUT} is given by Equation (4.4).

$$\Phi - \Psi = V_{X1} - V_{X2} = V_{OUT} - V_Y \tag{4.3}$$

$$V_{OUT} = V_Y + V_{X1} - V_{X2} \tag{4.4}$$

4.2.5 Analogue Voltage Adder/Subtractor/Sign Inverter Simulation Results

For all the simulations, $V_{DD} = 3.0V$ and $V_{SS} = -3.0V$. Transistor sizes used in the simulations are listed in Table 4.1. When V_{X2} is grounded, the circuit in

Table 4.1: Transistor sizes used in the simulations of the CMOS analogue voltage adder/subtractor/sign inverter in Figure 4.6.

		W/L
NMOS	MNT1∼MNT4	$32\mu m/4\mu m$
	MN1∼MN4	$4\mu m/8\mu m$
PMOS	MP1 & MP2	$12\mu m/8\mu m$

Figure 4.6 is an adder, with $V_{OUT} = V_{X1} + V_Y$. The simulation results are shown in Figure 4.7 and Figure 4.8. In Figure 4.7, V_{X1} sweeps from $-1.5V$ to $1.5V$, and V_Y steps from $-1.5V$ to $1.5V$ with $0.5V$ step. The solid line is the output V_{OUT} and the dashed line is the theoretical result of $V_{X1} + V_Y$.

In Figure 4.8, V_Y sweeps from $-1.5V$ to $1.5V$, and V_{X1} steps from $-1.5V$ to $1.5V$ with $0.5V$ step. The solid line is the output V_{OUT} and the dashed line is the theoretical result of $V_{X1} + V_Y$.

The simulation results in Figures 4.7 and 4.8 have shown that the voltage adder works well in the range of $-1V$ to $1V$ for both V_{X1} and V_Y.

When V_{X1} is grounded, the circuit in Figure 4.6 is a subtracter, with $V_{OUT} =$

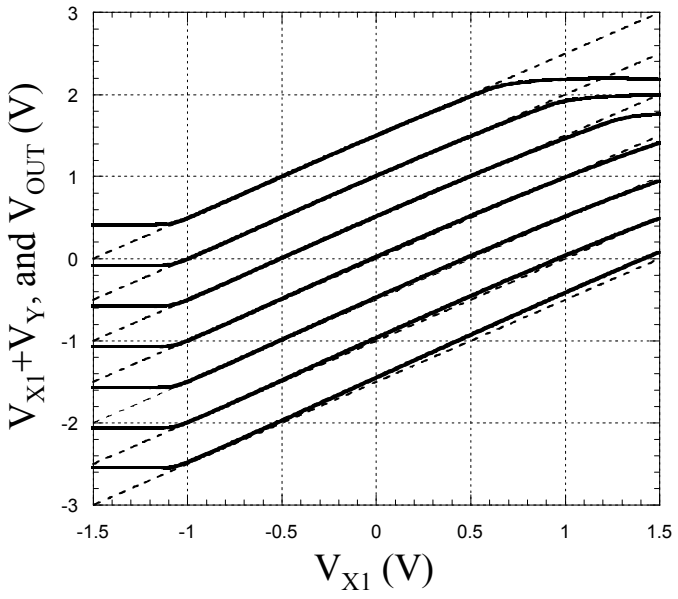

Figure 4.7: Simulation results for the voltage adder/subtractor/sign inverter, shown in Figure 4.6, used as a voltage adder, with $V_{OUT} = V_{X1} + V_Y$. V_{X1} sweeps from $-1.5V$ to $1.5V$ and V_Y steps from $-1.5V$ to $1.5V$ with $0.5V$ step.

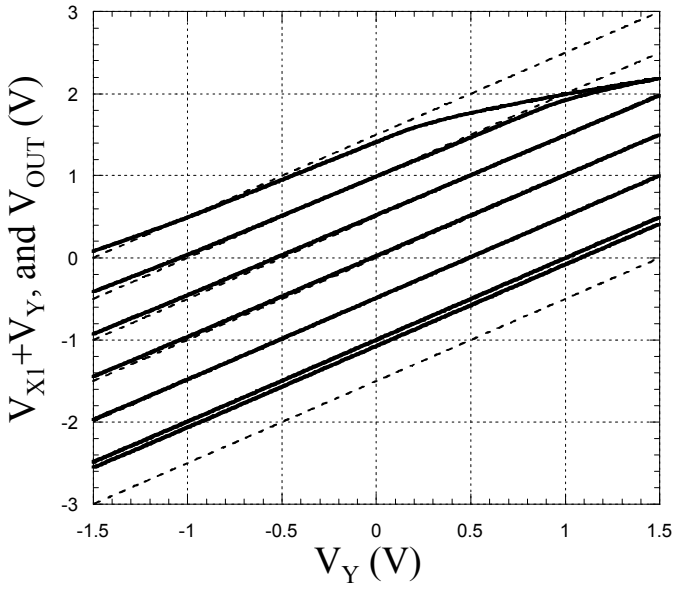

Figure 4.8: Simulation results for the voltage adder/subtractor/sign inverter, shown in Figure 4.6, used as a voltage adder, with $V_{OUT} = V_{X1} + V_Y$. V_Y sweeps from $-1.5V$ to $1.5V$, and V_{X1} steps from $-1.5V$ to $1.5V$ with $0.5V$ step.

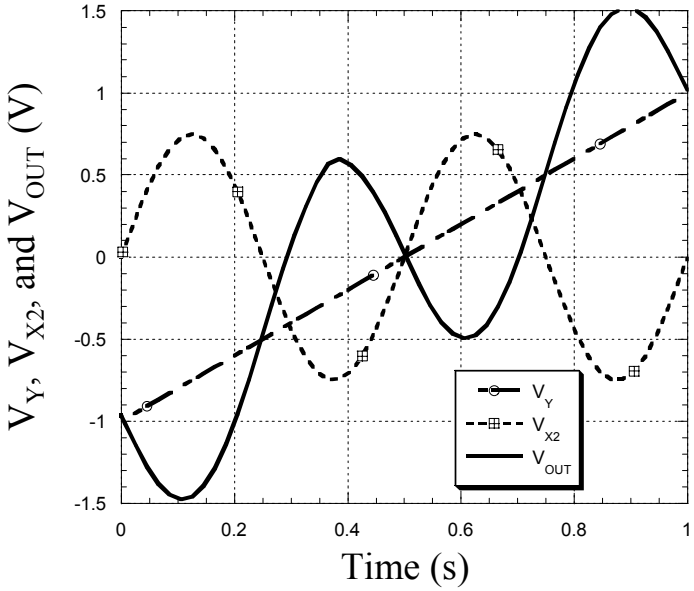

Figure 4.9: Simulation results for the voltage adder/subtractor/sign inverter, shown in Figure 4.6, used as a voltage subtracter, with $V_{OUT} = V_Y - V_{X2}$.

$V_Y - V_{X2}$. The simulation results are shown in Figure 4.9. V_Y is a linear function, which sweeps from $-1V$ to $1V$, a dot-dash line with circles, V_{X2} is a sinusoidal function, a dashed line with crossed squares, and the output V_{OUT} is the solid line.

When both V_{X1} and V_Y are grounded, the circuit in Figure 4.6 is a sign inverter, with $V_{OUT} = -V_{X2}$. The simulation results are shown in Figure 4.10. V_{X2} is a sinusoidal function sweeps from $-1V$ to $1V$, a dot-dash line, and the output V_{OUT} is the solid line.

4.2.6 Summary

A CMOS analogue voltage adder/subtracter/sign inverter is presented. The simulation results demonstrate that the voltage adder/subtracter/sign inverter works

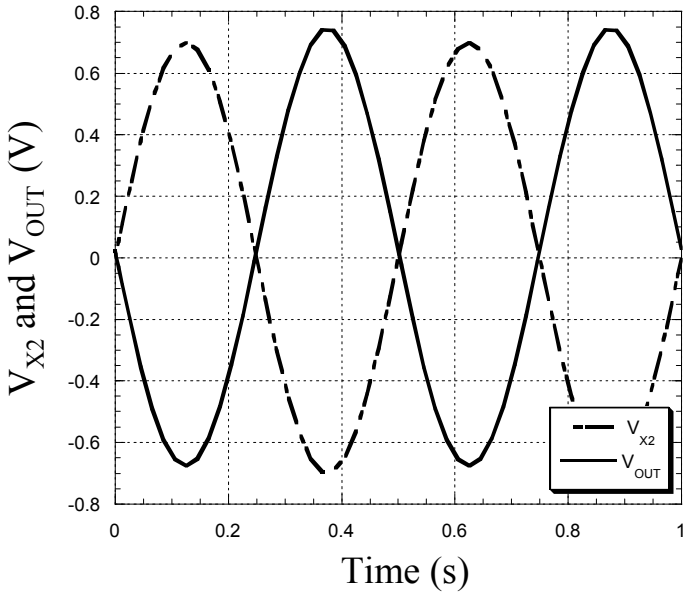

Figure 4.10: Simulation results for the voltage adder/subtractor/sign inverter, shown in Figure 4.6, used as a voltage sign inverter, with $V_{OUT} = -V_{X2}$.

in wide ranges of inputs, $-1V$ to $+1V$.

4.3 Analogue Four-Quadrant Multipliers

4.3.1 Literature Review on Four-Quadrant Multipliers

Analog multiplication of two signals is one of the most important operations in analog signal processing, as it is used not only for computation purposes but also in filters, mixers, modulators, and in neural networks. An ideal analog multiplier yields a linear production $z = Mxy$ of two inputs x and y, with M being the multiplication constant. There are single-quadrant (x and y both unipolar), double-quadrant (one of x and y being bipolar), and four-quadrant multipliers (x and y both bipolar). For

the purpose of building multi-celled hysteresis, and being able to put hysteresis in any place in the input-output space, four-quadrant multipliers are required.

There are a number of analog multipliers available from previous studies, with both voltage and current as the input and output. In this subsection, multipliers using the Gilbert-cell, quarter square technique, and quadritail categories are discussed.

4.3.1.1 Gilbert-Cell Based Four Quadrant Multipliers

In 1968, B. Gilbert proposed a four-quadrant multiplier using BJTs (bipolar junction transistors) [17]. The basic scheme of the multiplication core of a Gilbert cell is shown in Figure 4.11 (a), (In Gilbert's original paper, Q3 and Q4 were PNP type BJTs [17]), that has two doubly balanced, cross-coupled differential amplifiers. A differential voltage to current converter is needed to linearly convert the input voltage V_Y to current I_Y for voltage input V_Y if the BJT Gilbert cell is used. A Gilbert cell can also be realized by MOS technology, as shown in Figure 4.11 (b), first reported by D. C. Soo [52].

The analysis of the operation of a MOS version of the Gilbert cell is given as follows: $K_N = \mu_o C_{ox}$ is the transconductance parameter with the effective mobility μ_o and unit gate capacitance C_{ox}, and $\beta = \frac{K_N}{2}\frac{W}{L}$. All transistors are biased in saturation. The drain to source currents of the four transistors M1$\sim$M4 are given in Equations 4.5. Since I_{OUT} can be written as Equation (4.6), the output current I_{OUT} is given by Equation (4.7), to achieve multiplication of V_X and V_Y, notice that

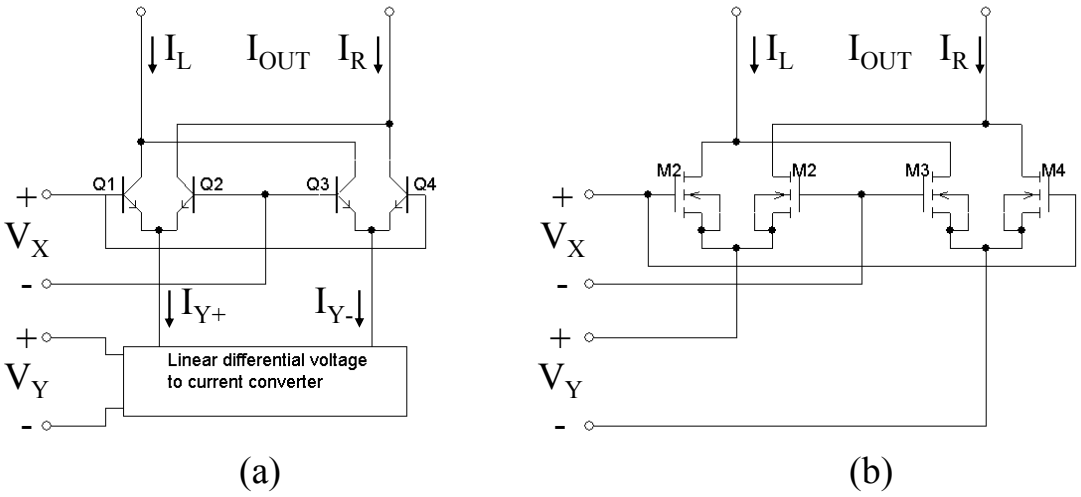

Figure 4.11: Quadritail-Gilbert Cell like Multipliers. (a) BJT Gilbert Cell. (b) CMOS Gilbert cell.

the bodies of the four transistors M1∼M4 are tied to their sources to eliminate the body effect on the threshold voltage V_{TH}.

$$\begin{aligned} I_1 &= \beta\left(V_{X+} - V_{Y+} - V_{TH}\right)^2 \\ I_2 &= \beta\left(V_{X-} - V_{Y+} - V_{TH}\right)^2 \\ I_3 &= \beta\left(V_{X-} - V_{Y-} - V_{TH}\right)^2 \\ I_4 &= \beta\left(V_{X+} - V_{Y-} - V_{TH}\right)^2 \end{aligned} \tag{4.5}$$

$$I_{OUT} = I_R - I_L = (I_2 + I_4) - (I_1 + I_3) = (I_4 - I_1) - (I_2 - I_3) \tag{4.6}$$

$$\begin{aligned} I_{OUT} &= \beta\left(V_{Y+} - V_{Y-}\right)\left[2V_{X+} - (V_{Y+} + V_{Y-}) - 2V_{TH}\right] \\ &\quad -\beta\left(V_{Y+} - V_{Y-}\right)\left[2V_{X-} - (V_{Y+} + V_{Y-}) - 2V_{TH}\right] \\ &= 2\beta\left(V_{X+} - V_{X-}\right)\left(V_{Y+} - V_{Y-}\right) \\ &= 2\beta V_X V_Y \end{aligned} \tag{4.7}$$

The Gilbert-cell scheme has been widely used in composing analog multipliers. The BJT based Gilbert-cell was used by C. F. Chan , H. -S. Ling, and O. Choy [8]

in their current-input and current-output analog multiplier. By adding another pair of BJTs, the differential input current I_X was converted into differential voltages applied to the basis of the Gilbert-cell BJTs, Q1, Q2, Q3, and Q4. The output current I_{OUT} is given by $I_{OUT} = (I_X I_Y)/I_S$, with I_S as a bias current in Chan's multiplier [8]. Differential input of I_X and I_Y were used in Chan's multiplier [8] to give four quadrant performance.

D. C. Soo [52] and Z. Wang [63] used MOS based Gilbert-cell in their voltage-input current-output multipliers. The core of the multiplier is exactly as in Figure 4.11 (b). By adding a pair of load resistors on top of the drain end of the 4 MOSs of the Gilbert-cell to get the difference of the voltage at the drain end, Z. Wang [63] constructed his 4-transistor multiplier, which is the same technique D. C. Soo [52] used in his test circuit to take the voltage reading. Notice that Soo's circuit [52] and Wang's circuit [63] used differential inputs.

4.3.1.2 Four Quadrant Multipliers Using Quarter Square Technique

Another four-quadrant multiplier scheme is known as quarter-square technique; the multiplication is achieved by Equation (4.8).

$$\frac{1}{4}\left\{(X+Y)^2-(X-Y)^2\right\}=XY \tag{4.8}$$

In general, the multiplication is achieved in three steps: the first is to find the sum and difference of the two input signals, then these results are squared, the last is to get the difference of the squares [40], [5], [28], [66], and [25]. Sometimes, the first two steps are combined into one, as in Song [51]. When biased in saturation,

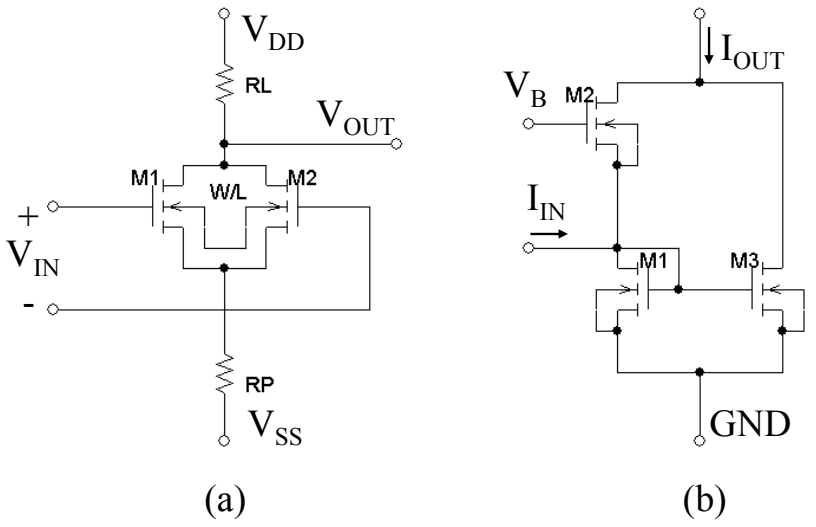

Figure 4.12: Squaring circuits. (a)Voltage input [40]. (b) Current input [6], which was further discussed by D. M. W. Leenaerts [28].

the drain to source current I can be expressed by Equation (4.1). For MOS-based square circuits, the property that the drain to source current is proportional to the square of the gate to source voltage when biased in saturation was used in many of the design of multipliers, as in Song's [51] (further discussed in [24]), in Bult's [5], and in Wiegerink's [66]. Other schemes had more than one transistor to calculate the square. The core squaring circuits of J. S. Pena-Ñinol [40] and K. Bult [6] are shown in Figure 4.12. The output voltage V_{OUT} of J. S. Pena-Ñinol's and output current I_{OUT} of K. Bult's squaring circuits are given in Equations 4.9 and 4.10, with $\beta_n = \frac{K_N}{2}\frac{W}{L}$ and V_{DCSQ} a common constant which could be canceled in the last step of taking the difference of the squares. The Bult's squaring core [5] of Figure 4.12 (b)was also used in Leenaerts's [28] multiplier.

$$V_{OUT} = -\frac{1}{4}K_N\left(\frac{W}{L}\right)R_L V_I^2 + V_{DCSQ} \tag{4.9}$$

$$I_{OUT} = \frac{1}{2}\beta\left(V_B - 2V_{THN}\right)^2 + \frac{I_{IN}^2}{2\beta\left(V_B - 2V_{TH}\right)^2} \tag{4.10}$$

The above two circuits in Figure 4.12 used MOS transistors as the core for squaring. K. Kimura [25] proposed a BJT four-quadrant quarter-square multiplier that operates on low supply voltage. It used unbalanced emitter coupled pairs, Q_1-Q_3 and Q_2-Q_4 which have emitter area ratios of K. To the third order approximation for small input V_{IN}, the differential output current I_{OUT} can be expressed in terms of the square of V_{IN} plus a common term, which cancels in the last step of taking the difference of the squares. This circuit was further discussed in [27], although the summing and differential circuits were not mentioned in either [25] or [27].

For all the above circuits, the inputs were always differential inputs, and the outputs were always currents for the core squaring circuits, load resistor or resistors were added to take the voltage outputs (see Figure 4.12). The circuits of J. S. Pena-Ñinol's [40], H.-J. Song's [51], K. Bult's voltage-input multiplier [5] and K. Kimura's [25] have voltage inputs. Both K. Bult's multiplier [6] and R. J. Wiegerink's [66] multiplier have current inputs.

Class AB multipliers [39] [65] also used the quarter-squared technique. Current mode class AB cell was used to square the input current. The problem of a class AB type of cell is that it has both PMOS and NMOS transistors in the squaring circuit and the parameters β_P and β_N of the PMOS and NMOS are assumed to be equal, which is more difficult to achieve than matching two NMOS transistors.

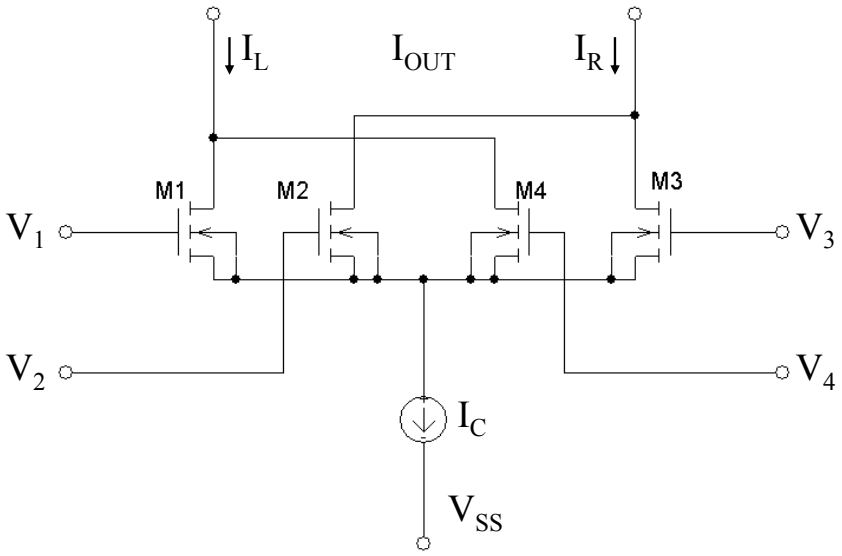

Figure 4.13: Schematic of quadritail multiplication core.

4.3.1.3 Quadritail Four Quadrant Multipliers

There also are four-quadrant analog multipliers based on the mixed configuration of Gilbert-cell and the quarter-squared technique, which includes K. Bult's [7], Z. Wang's [62], and K. Kimura's [26]. K. Kimura used quadritail to describe the multiplication core [26]. A quadritail circuit is shown in Figure 4.13. Notice that the sources of all four transistors are tied together and biased by a current source. For all four transistors M1∼M4, although the source voltages may vary during the operation, the body effect (the effect of V_{BS} on the threshold Voltage V_{TH}) has the same influence on the threshold voltage V_{TH}. Therefore, the bodies of the four transistors M1∼M4 can go to V_{SS} as they need not be tied to their sources.

There are various combinations of biasing the four gate voltages of V_1∼V_4. The gate voltages in Wang's multiplier [62] are given by Equation (4.11), and the gate

voltages in Kimura's [26] are given by Equation (4.12), with V_R being a DC reference voltage. The differential output current $I_{OUT} = I_L - I_R$ is given by Equation (4.13) for both sets of biasing voltages, with $\beta = \frac{K_N}{2}\frac{W}{L}$.

$$\begin{aligned} V_1 &= V_{X+} \\ V_2 &= V_{X+} - V_Y \\ V_3 &= V_{X-} \\ V_4 &= V_{X-} - V_Y \end{aligned} \tag{4.11}$$

$$\begin{aligned} V_1 &= V_X + V_Y + V_R \\ V_2 &= V_Y + V_R \\ V_3 &= V_X + V_R \\ V_4 &= V_R \end{aligned} \tag{4.12}$$

$$I_{OUT} = I_L - I_R = 2\beta V_X V_Y \tag{4.13}$$

For the quadritail multipliers, additional summing and subtracting circuits are needed.

There are also various other techniques to make four-quadrant analog multipliers, including four terminal devices [33], [57], and [12], BiCMOS multiplier [30] (with both BJT and MOS), and multiplication in digital domain with A/D and D/A converters [42].

We stay in CMOS technology in designing four-quadrant analog multipliers, with non differential current-input and voltage-input, and single end output. Bult's squaring circuit [6] for current-input multiplier and quadritail for voltage-input multiplier are in our main considerations.

4.3.2 Current-Input Four-Quadrant Multiplier

Since the summation and subtraction of currents are fairly easy to realize, the well known quarter-squared principle is used in designing the current-input four-quadrant multiplier. The principle is given in current form in Equation (4.14).

$$(I_X + I_Y)^2 - (I_X - I_Y)^2 = 4I_X I_Y \tag{4.14}$$

4.3.2.1 Current-Input Four-Quadrant Multiplier Schematics and Operation Principles

In order to calculate the multiplication of two input currents I_X and I_Y, by Equation (4.14), the squares of the sum and difference of I_X and I_Y are calculated, and then the difference of the two squares are taken. Only three NMOS transistors were used in Bult's squaring circuit[6], which is shown in Figure 4.14.

All three NMOS transistors, M1, M2, and M3 are biased in saturation. To eliminate body effect on threshold voltage V_{TH}, the bodies of all three transistors are tied to their sources. Also, the three transistors have the same sizes W and L, with $\beta = \frac{K_N}{2}\frac{W}{L}$; the drain to source currents I_1, I_2, and I_3 of M1, M2, and M3 are given by Equations (4.15).

$$\begin{aligned} I_1 &= \beta\,(V_B - V_{SS} - V_{TH})^2 \\ I_2 &= \beta\,(V_A - V_B - V_{TH})^2 = \beta\,[(V_A - V_{SS} - 2V_{TH}) - (V_B - V_{SS} - V_{TH})]^2 \\ I_3 &= \beta\,(V_B - V_{SS} - V_{TH})^2 \end{aligned} \tag{4.15}$$

From Kirchhoff current law, Equations (4.16) and (4.17) can be obtained.

$$I_{IN} = I_1 - I_2 \tag{4.16}$$

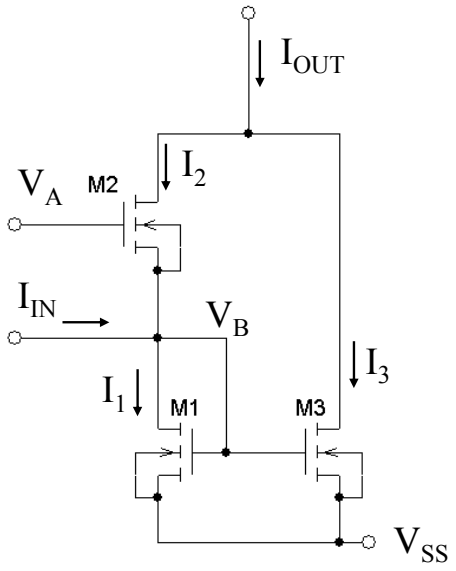

Figure 4.14: The schematic of Bult's current squaring circuit [6].

$$I_{OUT} = I_2 + I_3 = I_1 + I_2 \tag{4.17}$$

Therefore, the input current I_{IN} can be expressed in the form of V_A and V_B by Equation (4.18). Solving $V_B - V_{SS} - V_{TH}$ in terms of I_{IN} and V_A gives Equation (4.19).

$$I_{IN} = \beta \left[2(V_A - V_{SS} - 2V_{TH})(V_B - V_{SS} - V_{TH}) - (V_A - V_{SS} - 2V_{TH})^2 \right] \tag{4.18}$$

$$V_B - V_{SS} - V_{TH} = \frac{I_{IN}}{2\beta(V_A - V_{SS} - V_{TH})} + \frac{(V_A - V_{SS} - V_{TH})}{2} \tag{4.19}$$

Plug $V_B - V_{SS} - V_{TH}$, represented in Equation (4.19), into Equation (4.15) and use Equation (4.17) to get I_{OUT} expressed in terms of I_{IN} and V_A by Equation (4.20).

$$I_{OUT} = \frac{I_{IN}^2}{2\beta \left(V_A - V_{SS} - 2V_{TH}\right)^2} + \frac{\beta \left(V_A - V_{SS} - 2V_{TH}\right)^2}{2} \tag{4.20}$$

The core part of the four-quadrant current-input multiplier is shown in Figure 4.15. Transistors MPS2 and MPD2 are mirrors of of MPS1 and MPD2, and MNO2

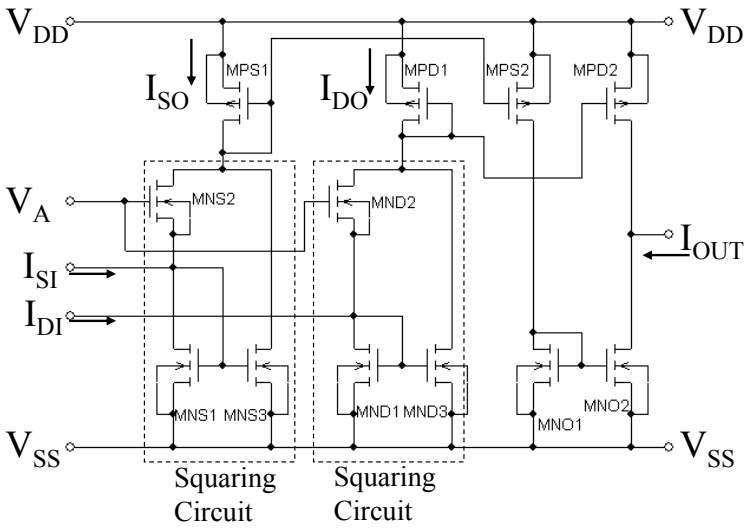

Figure 4.15: The schematic of the multiplication core of the current-input multiplier.

is a mirror for MNO1. Therefore, the output current is the difference of I_{SO} and I_{DO}, and is given in Equation (4.21). When $I_{SI} = I_X + I_Y$ and $I_{DI} = I_X - I_Y$, the output current I_{OUT} is given in Equation (4.22).

$$I_{OUT} = \frac{I_{SI}^2 - I_{DI}^2}{2\beta \left(V_A - V_{SS} - 2V_{TH}\right)^2} \tag{4.21}$$

$$I_{OUT} = \frac{2}{\beta \left(V_A - V_{SS} - 2V_{TH}\right)^2} I_X I_Y \tag{4.22}$$

The complete CMOS four-quadrant current-input current-output multiplier is constructed with two parts, the current adder/subtractor, shown in Figure 4.2, and the multiplication core, shown in Figure 4.15. The schematic of the complete circuit is shown in Figure 4.16.

4.3.2.2 Current-Input Four-Quadrant Multiplier Simulation Results

PSpice simulation results are shown in Figure 4.17 and Figure 4.18. I_X is the x-axis and I_{OUT} the y-axis with the unit of μA. The circuit is biased at $V_{DD} = 3.0V$,

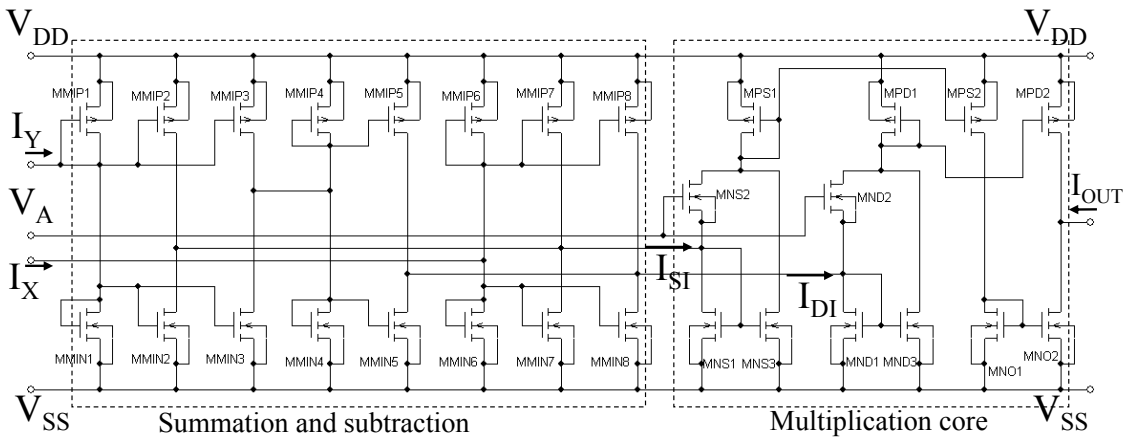

Figure 4.16: The schematic of the CMOS complete four-quadrant current-input multiplier.

$V_{SS} = -3.0V$, and $V_A = 1.0V$. The transistor sizes used in the simulations are listed in Table 4.2

As shown in Figure 4.17, the CMOS current-input current-output multiplier losses its linearity when I_X and I_Y are outside of the ranges of $-20\mu A \sim +20\mu A$. The simulation results for I_X and I_Y in the ranges of $-20\mu A \sim +20\mu A$ are shown in Figure 4.18. The multiplication factor M in $I_{OUT} = MI_XI_Y$ is $1.88 \times 10^{-2}/\mu A/$ in the simulation results. Using transistor parameters, we find the theoretical value for $M = 2/\beta(V_A - V_{SS} - 2V_{TH})^2$ is $2.38 \times 10^{-2}/\mu A$. This CMOS current-input four-quadrant multiplier has the input range of $-20\mu A$ to $+20\mu A$.

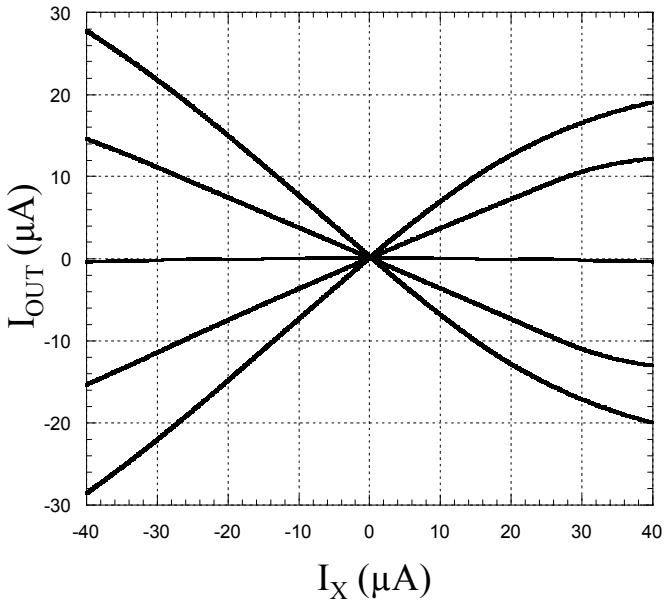

Figure 4.17: Simulation results for the CMOS four quadrant current-input current-output multiplier in Figure 4.16. I_X sweeps from $-40\mu A$ to $+40\mu A$, and I_Y steps from $-40\mu A$ to $+40\mu A$ with $+20\mu A$ step.

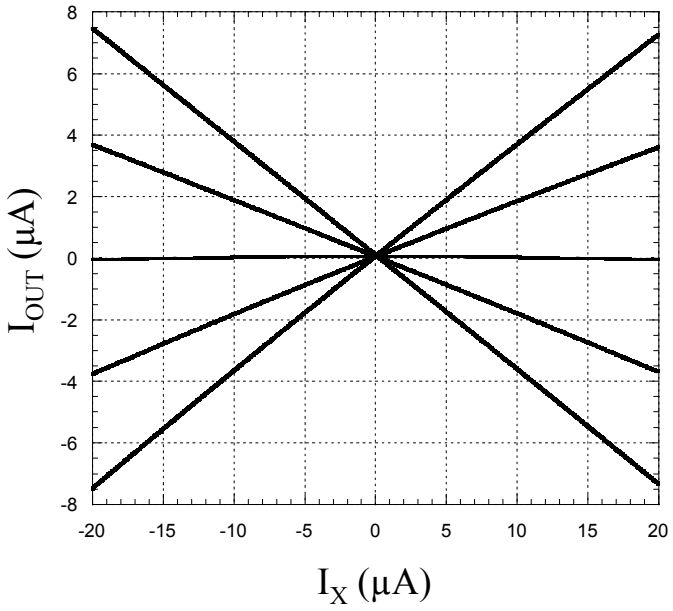

Figure 4.18: Simulation results for the CMOS four quadrant current-input current-output multiplier in Figure 4.16. I_X sweeps from $-20\mu A$ to $+20\mu A$, and I_Y steps from $-20\mu A$ to $+20\mu A$ with $+10\mu A$ step.

Table 4.2: Transistor sizes used in the simulations of the CMOS four-quadrant current-input multiplier in Figure 4.16.

		W/L
NMOS	MMNI1∼MMNI8	$4.8\mu m/4\mu m$
	MNS1∼MNS3 & MND1∼MND3	$4\mu m/8\mu m$
	MNO1 & MNO2	$4\mu m/10.4\mu m$
PMOS	MPNI1∼MPNI8	$4\mu m/5.6\mu m$
	MPD1, MPD2, MPS1, & MPS2	$12\mu m/4\mu m$

4.3.3 Voltage-Input Four-Quadrant Multiplier

4.3.3.1 Voltage-Input Four-Quadrant Multiplier Schematics and Operation Principles

We used the quadritail cell named by K. Kimura [26] as the multiplication core of the voltage input multiplier. One big advantage of this quadritail is that there is no need for a separated Pwell for the four transistors and all the bodies are biased with the lowest voltage V_{SS}, since the sources of all four transistors are tied together so the body effect would have the same influence on their threshold voltages V_{TH}. The schematic of the multiplication core is shown in Figure 4.19, which is Figure 4.13 with the gate voltages of M1∼M4 biased to V_X, $V_X + V_Y$, GND, and V_Y.

All four transistors M1∼M4 are biased in saturation, therefore, the drain to source currents of each transistor are given in Equations (4.23), with V_C the common

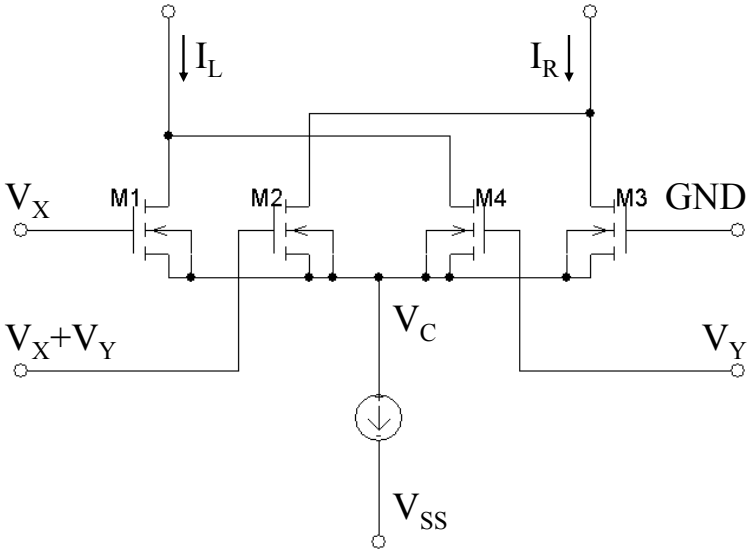

Figure 4.19: The schematic of the multiplication core of the voltage-input multiplier–quadritail.

source voltage and $\beta = \frac{K_N}{2}\frac{W}{L}$. The two currents I_L and I_R are given by Equations (4.24). If we take the difference between I_R and I_L, Equation (4.25) can be obtained, and the multiplication of V_X and V_Y is achieved.

$$\begin{aligned} I_1 &= \beta\left(V_X - V_C - V_{TH}\right)^2 \\ I_2 &= \beta\left(V_X + V_Y - V_C - V_{TH}\right)^2 \\ I_3 &= \beta\left(0 - V_C - V_{TH}\right)^2 \\ I_4 &= \beta\left(V_Y - V_C - V_{TH}\right)^2 \end{aligned} \tag{4.23}$$

$$\begin{aligned} I_L &= I_1 + I_4 \\ I_R &= I_2 + I_3 \end{aligned} \tag{4.24}$$

$$I_R - I_L = 2\beta V_X V_Y \tag{4.25}$$

The complete schematic of the voltage-input multiplier is shown in Figure 4.20, where an adder is used to calculate the sum of V_X and V_Y to bias the gate

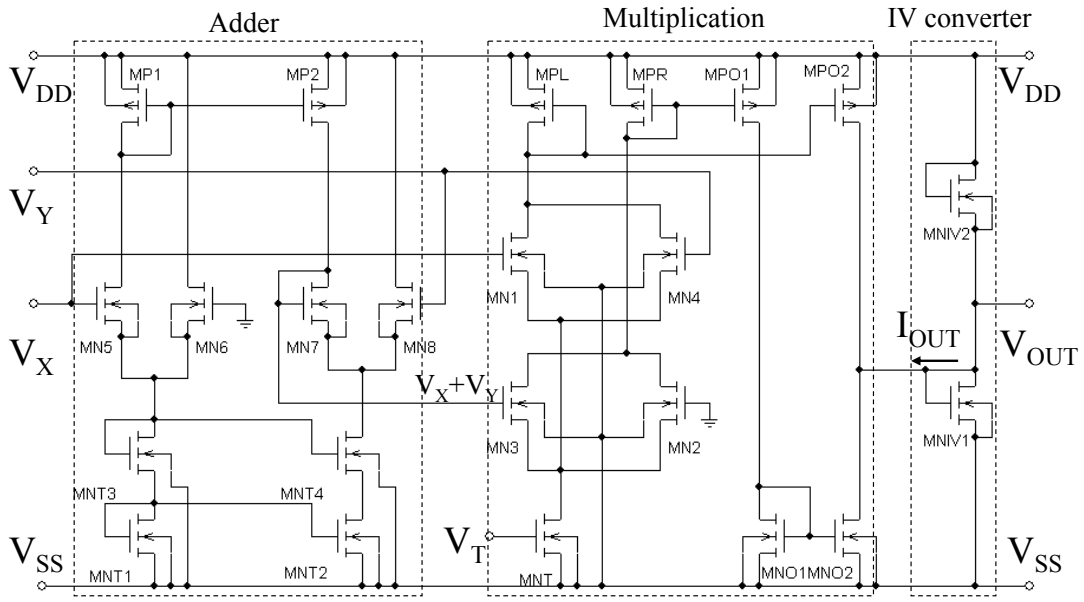

Figure 4.20: The schematic of the complete CMOS four quadrant voltage-input multiplier.

of transistor MN2. A linear current voltage converter is used to convert I_{OUT} into V_{OUT} if a voltage output is desired.

4.3.3.2 Voltage-Input Four-Quadrant Multiplier Simulation Results

PSpice simulation results of I_{OUT} are shown in Figure 4.21 and Figure 4.22. For both plots, V_X is the x-axis with the unit of Volts, and I_{OUT} is the y-axis with the unit of μA. The circuit is biased at $V_{DD} = 3.0V$, $V_{SS} = -3.0V$, and $V_T = -2.0V$. The transistor sizes used in the simulations are listed in Table 4.3.

As shown in Figure 4.21, the CMOS voltage-input multiplier losses its linearity when V_X and V_Y are outside of the ranges of $-0.75V \sim 0.75V$. The simulation results for V_X and V_Y in the ranges of $-0.75V \sim 0.75V$ are shown in Figure 4.22.

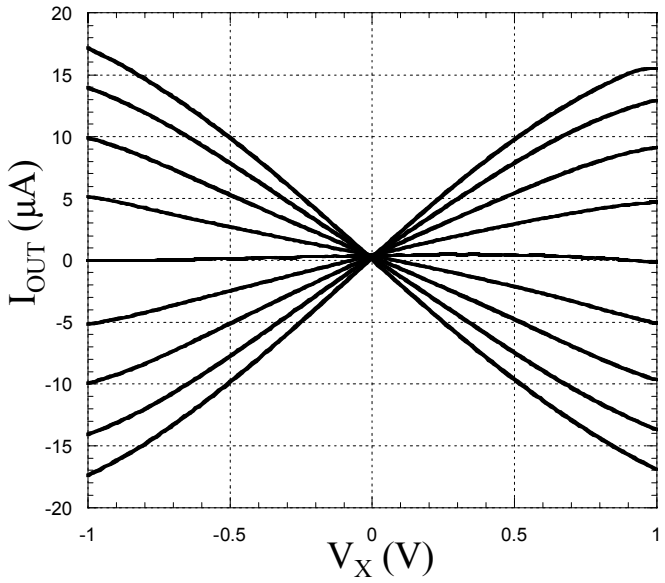

Figure 4.21: Simulation results for the CMOS four-quadrant voltage-input multiplier in Figure4.20, with the current output I_{OUT}. V_X sweeps from $-1V$ to $+1V$, and V_Y steps from $-1V$ to $+1V$ with $+0.25V$ step.

Table 4.3: Transistor sizes used in the simulations of the CMOS four-quadrant voltage-input multiplier in Figure 4.20.

		W/L
NMOS	MNT1∼MNT4	$32\mu m/4\mu m$
	MN5∼MN8	$4\mu m/8\mu m$
	MN1∼MN4	$4\mu m/8\mu m$
	MNT	$16\mu m/4\mu m$
	MNO1 & MNO2	$16\mu m/8\mu m$
	MNIV1 & MNIV2	$4\mu m/24\mu m$
PMOS	MP1 & MP2	$12\mu m/8\mu m$
	MPL, MPR, MPO1, & MPO2	$12\mu m/8\mu m$

The multiplication factor M in $V_{OUT} = MI_XI_Y$ is $19.9\mu A/V^2$ in the simulation results. For the chosen transistor parameters, the theoretical value for $M = 2\beta$ is $18.6\mu A/V^2$.

If voltage output is desired, a linear current voltage converter is added to the right end of the circuit, as shown in Figure 4.20. The simulation results of the voltage output V_{OUT} are shown in Figure 4.23. The multiplication factor M in $V_{OUT} = MV_XV_Y$ is $0.676/V$ in the simulation results. For the chosen transistor parameters, the theoretical value is $0.597/V$.

This voltage-input multiplier has the input range of $-0.75V$ to $+0.75V$.

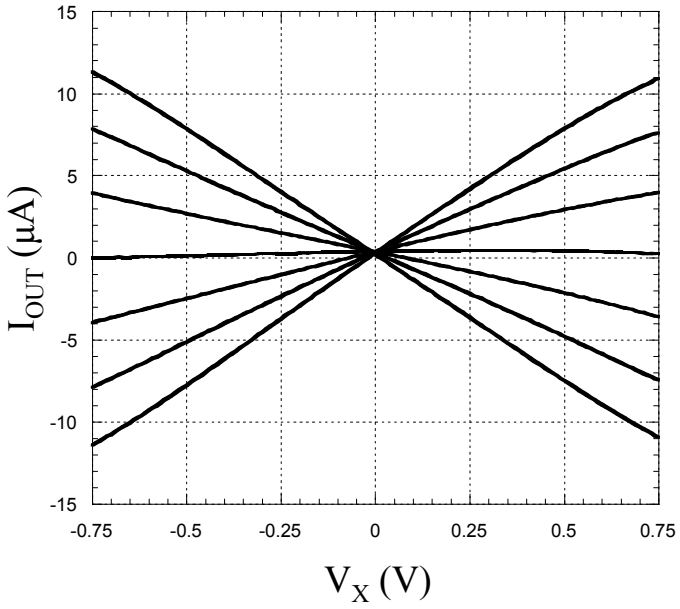

Figure 4.22: Simulation results for the CMOS four-quadrant voltage-input multiplier in Figure4.20, with the current output I_{OUT}. V_X sweeps from $-0.75V$ to $+0.75V$, and V_Y steps from $-0.75V$ to $+0.75V$ with $+0.25V$ step.

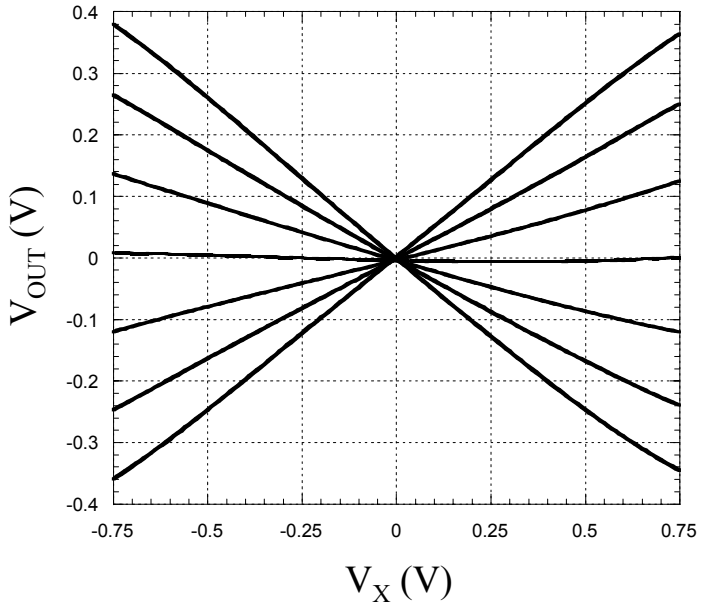

Figure 4.23: Simulation results for the CMOS four quadrant voltage-input multiplier in Figure4.20, with the voltage output V_{OUT}. V_X sweeps from $-0.75V$ to $+0.75V$, and V_Y steps from $-0.75V$ to $+0.75V$ with $+0.25V$ step.

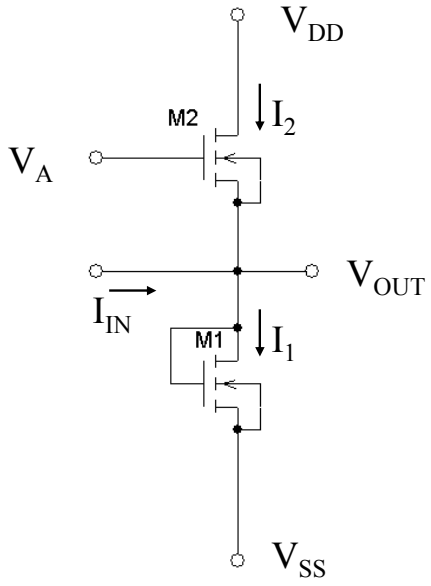

Figure 4.24: Schematic of the linear current-voltage converter [6].

4.4 Linear Voltage-Current Converter and Current-Voltage Converter

4.4.1 Linear Current-Voltage Converter

K. Bult and H. Wallinga [6] proposed an linear current-voltage converter, which had only two transistors, as shown in Figure 4.24. Both NMOS transistors, M1 and M2 are biased in saturation. To eliminate body effect on threshold voltage V_{TH}, the bodies of both three transistors are tied to their sources. Also,they have the same sizes W and L, with $\beta = \frac{K_N}{2}\frac{W}{L}$, the drain to source currents I_1 and I_2 of M1 and M2 are given by Equations (4.26).

$$\begin{aligned} I_1 &= \beta \left(V_{OUT} - V_{SS} - V_{TH}\right)^2 \\ I_2 &= \beta \left(V_A - V_{OUT} - V_{TH}\right)^2 \end{aligned} \tag{4.26}$$

From Kirchhoff's current law, we know that $I_{IN} = I_1 - I_2$, therefore I_{IN} can

be written as in Equation (4.27). By choosing $V_A = V_{DD} = -V_{SS}$, V_{OUT} is given in Equation (4.28).

$$I_{IN} = \beta \left(V_A - V_{SS} - 2V_{TH}\right)\left(2V_{OUT} - V_{SS} - V_A\right) \tag{4.27}$$

$$V_{OUT} = \frac{I_{IN}}{2\beta \left(V_{DD} - V_{SS} - 2V_{TH}\right)} \tag{4.28}$$

PSpice simulation results are shown in Figure 4.25. I_{IN} is the x-axis with the unit of μA and V_{OUT} the y-axis with the unit of Volts. I_{IN} sweeps from$-200\mu A$ to $+200\mu A$. The circuit is biased at $V_A = V_{DD} = 3.0V$, and $V_{SS} = -3.0V$. The four curves are for four different transistor width to length ratios $(W/L) = (4\mu m/4\mu m)$–solid line with circles, $= (4\mu m/8\mu m)$–dashed line with crossed squares, $= (4\mu m/12\mu m)$–dashed line with circles, and $(W/L) = (4\mu m/24\mu m)$–solid line with squares. The ratios of V_{OUT}/I_{IN} in the simulation results and theoretical calculation of $V_{OUT}/I_{IN} = 1/[2\beta \left(V_{DD} - V_{SS} - 2V_{TH}\right)]$ are listed in Table 4.4.

Table 4.4: V_{OUT}/I_{IN} in the unit of $K\Omega$ for different (W/L) ratios used in CMOS linear current voltage converter, shown in Figure 4.24.

W/L	$4\mu/4\mu$	$4\mu/8\mu$	$4\mu/12\mu$	$4\mu/24\mu$
Simulation	5.86	11.48	17.36	34.29
Theoretical	5.49	10.75	16.07	32.09

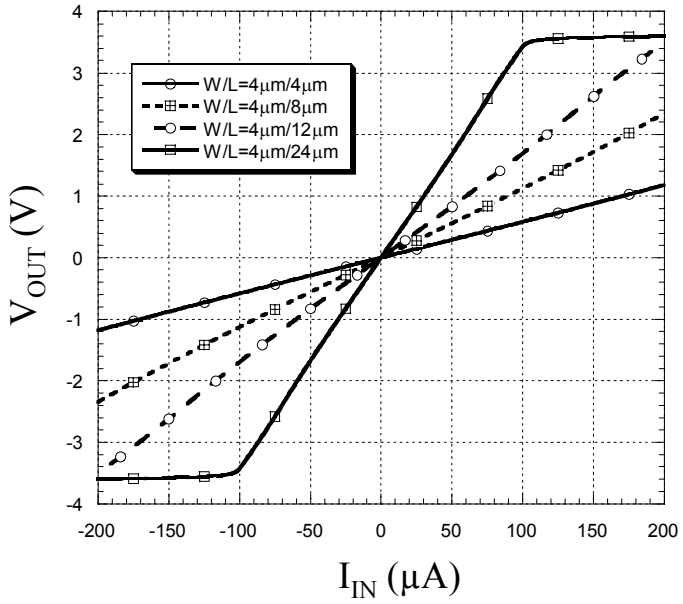

Figure 4.25: Simulation results for the linear current voltage converter in Figure 4.24.

4.4.2 Linear Differential Voltage-Current Converter

Linear differential voltage-current converter can be achieved by using differential amplifiers, as shown in Figure 4.26. Transistors MN1 and MN2 form the differential pair, with the sources tied together and biased with a current source formed by transistor MN5. MP1∼MP4 and MN3 and MN4 form the current mirrors to give the output current $I_{OUT} = I_1 - I_2$. All transistors are biased in saturation. With $\beta = \frac{K_N}{2}\frac{W}{L}$, the drain to source currents I_1 and I_2 of MN1 and MN2 are given by Equations (4.29). For $V_{IN} = V_{IN1} - V_{IN2}$, the input voltage V_{IN} can be expressed via I_1 and I_2 by Equation (4.30).

$$\begin{aligned} I_1 &= \beta \left(V_{IN1} - V_C - V_{TH}\right)^2 \\ I_2 &= \beta \left(V_{IN2} - V_C - V_{TH}\right)^2 \end{aligned} \tag{4.29}$$

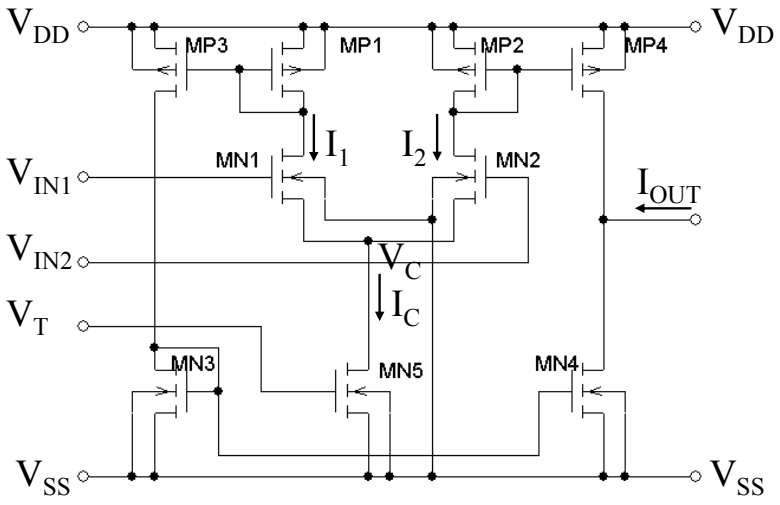

Figure 4.26: Schematic of the CMOS linear differential voltage-current converter–differential pair.

$$V_{IN} = \sqrt{\frac{I_1}{\beta}} - \sqrt{\frac{I_2}{\beta}} \tag{4.30}$$

Also notice that $I_C = I_1 + I_2$, with $I_{OUT} = I_1 - I_2$, we can have $I_1 = (I_C + I_{OUT})/2$ and $I_2 = (I_C - I_{OUT})/2$, therefore, V_{IN} can be rewritten in terms of I_C and I_{OUT}, in Equation (4.31). If $I_{OUT} << I_C$, since $\sqrt{1+t} = 1 + \frac{1}{2}t - \frac{1}{8}t^2 + \frac{1}{16}t^3....$ for small t, the second degree approximation of V_{IN} can be expressed in Equation (4.32). The output current I_{OUT} is linearly proportional to input differential voltage V_{IN}, as shown in Equation (4.33).

$$V_{IN} = \sqrt{\frac{I_C}{2\beta}} \left(\sqrt{1 + \frac{I_{OUT}}{I_C}} - \sqrt{1 - \frac{I_{OUT}}{I_C}} \right) \tag{4.31}$$

$$V_{IN} = \sqrt{\frac{I_C}{2\beta}} \left(\frac{I_{OUT}}{I_C} \right) \tag{4.32}$$

$$I_{OUT} = \sqrt{2\beta I_C} V_{IN} \tag{4.33}$$

PSpice simulation results are shown in Figure 4.27. V_{IN} is the x-axis with the

unit of volt and I_{OUT} the y-axis with the unit of μA. V_{IN} sweeps from$-1V$ to $+1V$. The circuit is biased at $V_{DD} = 3.0V$, $V_{SS} = -3.0V$ and $V_T = -2.0V$. Transistor sizes except MN1 and MN2 are listed in Table 4.5. The four curves are for three different transistor width to length ratios of MN1 and MN2: $(W/L) = (4\mu m/8\mu m)$–solid line with circle, $= (4\mu m/4\mu m)$–dash line with crossed squares, and $(W/L) = (8\mu m/4\mu m)$–dashed line with diamonds. The ratios of I_{OUT}/V_{IN} in the simulation results and theoretical calculations of $I_{OUT}/V_{IN} = \sqrt{2\beta I_C}$, with $I_C = 25\mu A$, are listed in Table 4.6.

Table 4.5: Transistor sizes used in the simulations of the CMOS linear voltage-current converter in Figure 4.26.

		W/L
NMOS	MN3 & MN4	$4\mu m/4\mu m$
	MN5	$16\mu m/4\mu m$
PMOS	MP1∼MP4	$12\mu m/4\mu m$

Table 4.6: I_{OUT}/V_{IN} in the unit of $\mu A/V$ for different (W/L) ratios used in CMOS linear differential voltage-current converter, shown in Figure 4.26.

W/L	$4\mu/8\mu$	$4\mu/4\mu$	$8\mu/4\mu$
Simulation	22.92	32.42	45.66
Theoretical	21.56	29.76	43.93

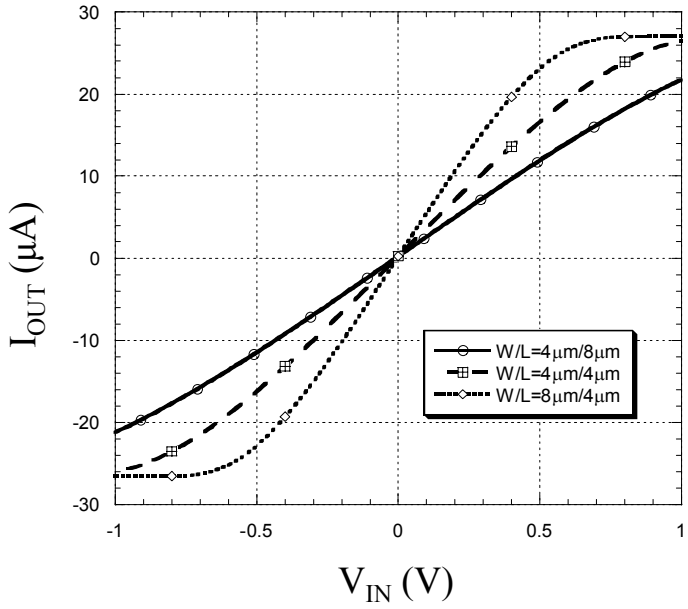

Figure 4.27: Simulation results for the CMOS linear differential voltage-current converter in Figure 4.26.

4.5 Summary

In this chapter, various circuits needed in building multi-level and multi-dimensional hysteresis are covered. These circuits include: voltage adder, current-input multiplier, voltage-input multiplier, linear current to voltage converter, and voltage to current converter. With these circuits and binary hysteresis circuits, multi-level and multi-dimensional hysteresis can be built, as will be seen in Chapter five.

Chapter 5

CMOS Multi-Cell Hysteresis Circuit and Possible Application on Chaos Generation

5.1 Introduction

In the previous chapters, CMOS binary hysteresis circuits with full control and operating in all four quadrants, analogue adders, four-quadrant analogue multipliers, linear current voltage converters, and linear voltage current converts have been discussed in detail. In this chapter, construction of multi-level hysteresis and multi-dimensional hysteresis is discussed. First, a brief review of the CMOS circuits as the building blocks for the multi-cell hysteresis is given. Then the discussion moves on to the construction of multi-level hysteresis using CMOS circuits, then the construction of multi-cell hysteresis. Finally, we suggest possible application of multi-cell hysteresis on chaos generation.

For all the simulations in this chapter, the same MOSIS 1.2 μm transistor models (BSIM1, Level 4, and Run n7ab) are used [37], as in the previous chapters. Since all the circuits discussed in this chapter are constructed with binary hysteresis circuits in Chapter three, and adders and multipliers in Chapter four, all the transistor parameters, and biasing voltages V_{DD} and V_{SS} are the same as in the previous chapters.

(a) Forward (b) Reverse

Figure 5.1: Block diagrams of binary hysteresis circuits. (a)Forward binary hysteresis. (b) Reverse binary hysteresis.

5.2 CMOS Circuits as Building Blocks of Multi-Level Hysteresis and Multi-Cell Hysteresis

There are four types of binary hysteresis circuits with full control in all four quadrants, current-input current-output, voltage-input voltage-output, current-input voltage-output, and voltage-input current output. With slight alternations on circuits, each of them can give both forward and reverse binary hysteresis curves. For all the binary hysteresis circuits, complete control has been achieved on the hysteresis position, height, and width, in all four quadrants. All CMOS binary hysteresis circuits are represented by the block diagrams, shown in Figure 5.1.

For the construction of multi-level hysteresis and multi-cell hysteresis, we also need analogue adders and multipliers. The detailed discussions of adders and multipliers are given in Chapter four. All the adders and multipliers work in all four quadrants. For current-input adder, it is easy to add another input port by tying an extra node. The CMOS adders and multipliers are represented by the block diagrams, shown in Figure 5.2.

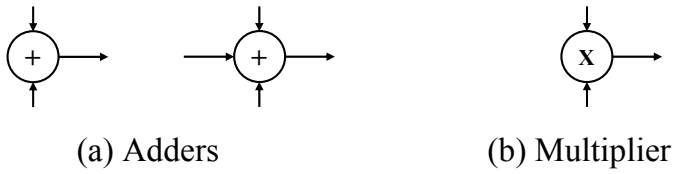

Figure 5.2: Block diagrams of adders and multiplier. (a)Two input port adder and three input port adder. (b) Two input port multiplier.

5.3 CMOS Multi-Level Hysteresis Circuits

Multi-level hysteresis can be achieved by adding several binary hysteresis curves. When three forward hystereses are added, a 4-level forward hysteresis can be generated, as shown in Figure 5.3. This particular case can be generalized to make m-level forward hysteresis by adding $(m-1)$ forward binary hysteresis, or m-level reverse hysteresis by adding $(m-1)$ reverse binary hysteresis. This particular type of multi-level hysteresis was used in building high dimension chaotic oscillators, first proposed by J. E. Varrientos and E. Sánchez-Sinencio [56], later extend to 9-scrolls using 9-level hysteresis by F. Han [20].

5.3.1 CMOS Voltage Mode Multi-Level Hysteresis

With the available CMOS voltage mode binary hysteresis circuits and analogue adders, CMOS voltage mode multi-level hysteresis can be achieved. Two CMOS voltage-input voltage-output binary hysteresis and one two port voltage adder are used to construct the CMOS voltage mode multi-level hysteresis circuits, as shown in Figure 5.4.

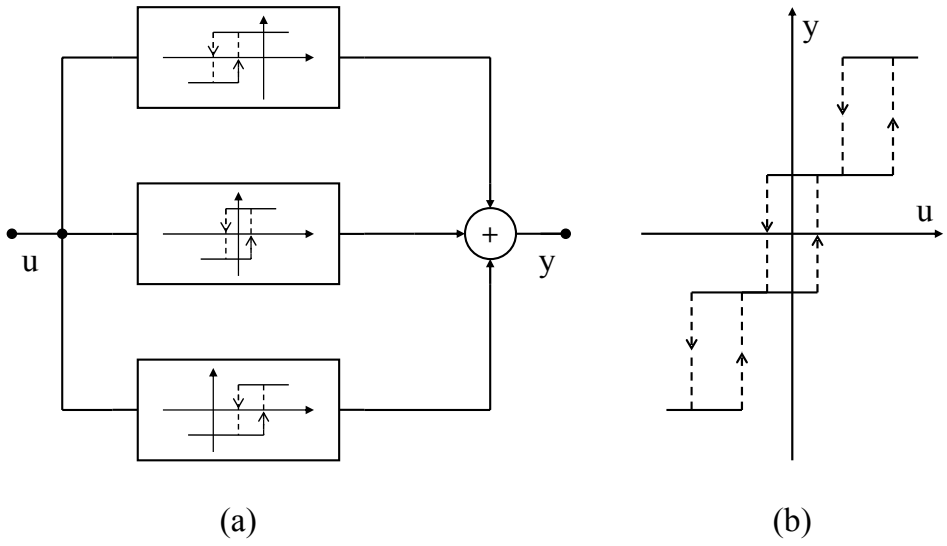

Figure 5.3: Generation of 4-level hysteresis by adding 3 forward binary hysteresis. (a) Schematic. (b) 4-level hysteresis.

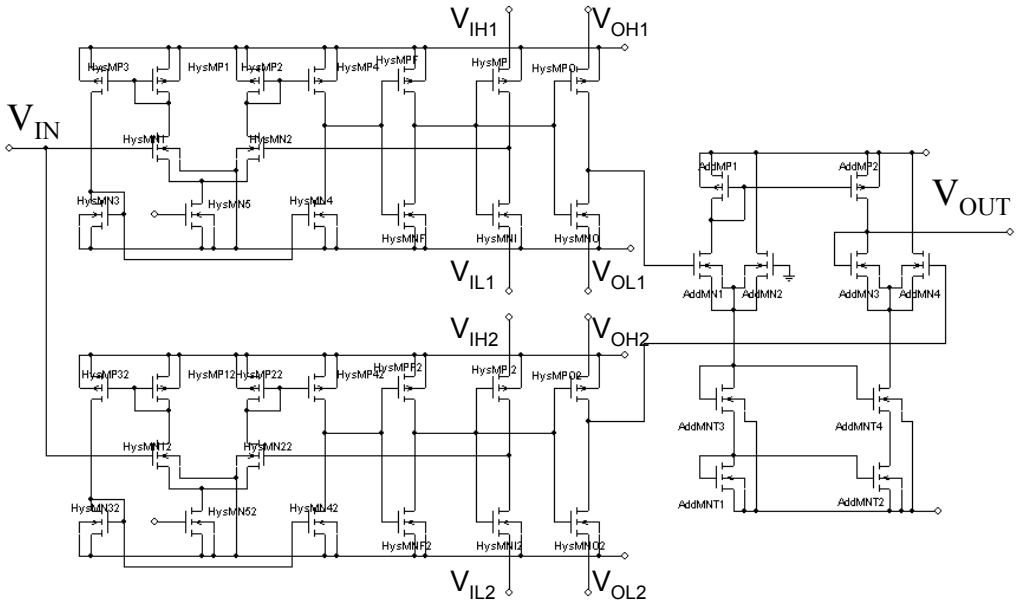

Figure 5.4: Schematic of a CMOS voltage mode multi-level hysteresis circuits, with two voltage-input voltage-output binary hysteresis circuits on the left and one analogue voltage adder on the right.

One example of PSpice simulation results is shown in Figure 5.5. The output voltage V_{OUT} has two sections of hysteresis. There is complete control on the horizontal position, width, and the height of each section of the hysteresis by the eight external voltage sources V_{IL1}, V_{IH1}, V_{OL1}, V_{OH1}, V_{IL2}, V_{IH2}, V_{OL2}, and V_{OH2}.

We can also add forward hysteresis with the reverse one. One example is shown in Figure 5.6. The reverse binary hysteresis has $V_{L2H} = -2V$ and $V_{H2L} = -0.4V$, and the forward binary hysteresis has $V_{H2L} = 0.4V$ and $V_{L2H} = 2V$. While the input voltage V_{IN} is increasing, the output voltage V_{OUT} jumps from $-0.5V$ to $-1.5V$ when V_{IN} passes $-0.4V$, and then to $0V$ when V_{IN} passes $2V$. While the input voltage V_{IN} is decreasing, the output voltage V_{OUT} jumps from $0V$ to $-1.5V$ when V_{IN} passes $0.4V$, and then to $-0.5V$ when V_{IN} passes $-2V$.

5.3.2 CMOS Current Mode Multi-Level Hysteresis

Multi-level hysteresis can also be achieved in current mode. Three CMOS current-input current-output binary hystereses are used to construct the CMOS current mode multi-level hysteresis circuits. The output nodes of the three binary hysteresis are tied together to give the sum.

PSpice simulation results to generate 4-level hysteresis is shown in Figure 5.8. The three binary hysteresis are centered at $(-5\mu A,\ 0\mu A)$, $(0\mu A,\ 0\mu A)$, and $(5\mu A,\ 0\mu A)$, with the same height $4\mu A$, and the same width $4\mu A$. The output current I_{OUT} has three sections of hysteresis. Since complete control on the horizontal position, width, and the height of the each of the binary hysteresis has been

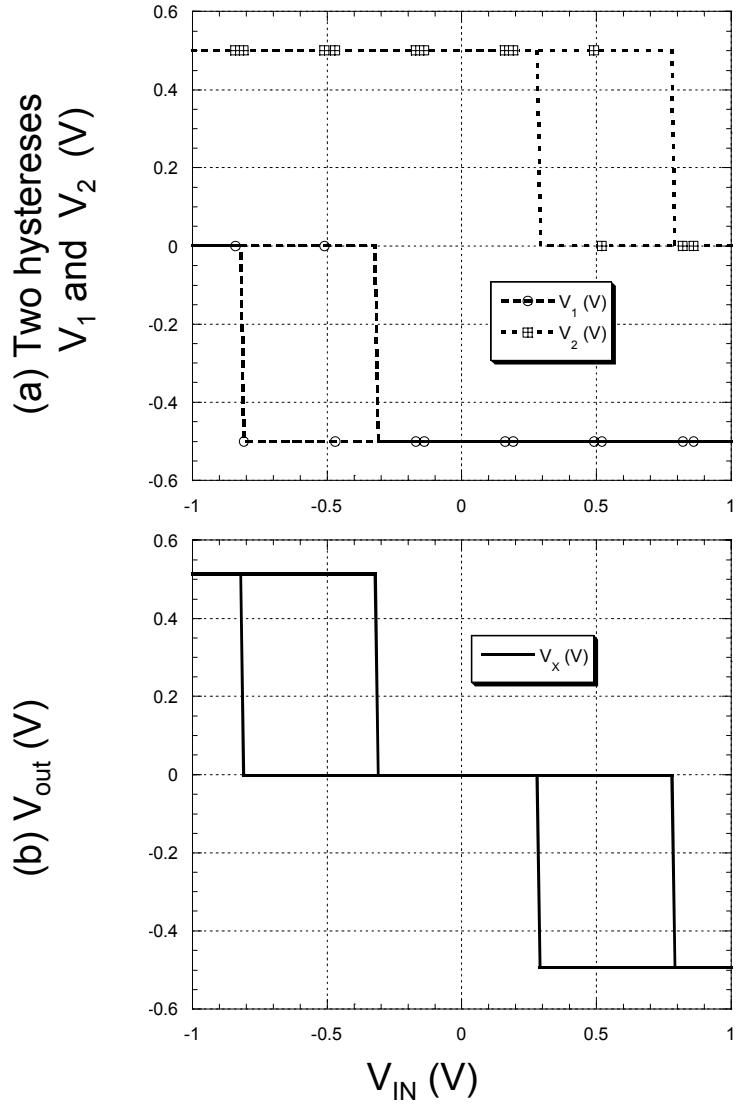

Figure 5.5: PSpice simulation results for the generation of a voltage mode 3-level hysteresis. (a) Two reverse binary hysteresis centered $(-0.25V,\ -0.55V)$ and $(0.25V,\ 0.55V)$, with the same height of $0.5V$ and width of $0.5V$. (b) Output voltage V_{OUT} in the unit of Volts. Both plots have V_{IN} in the unit of Volts as x-axis.

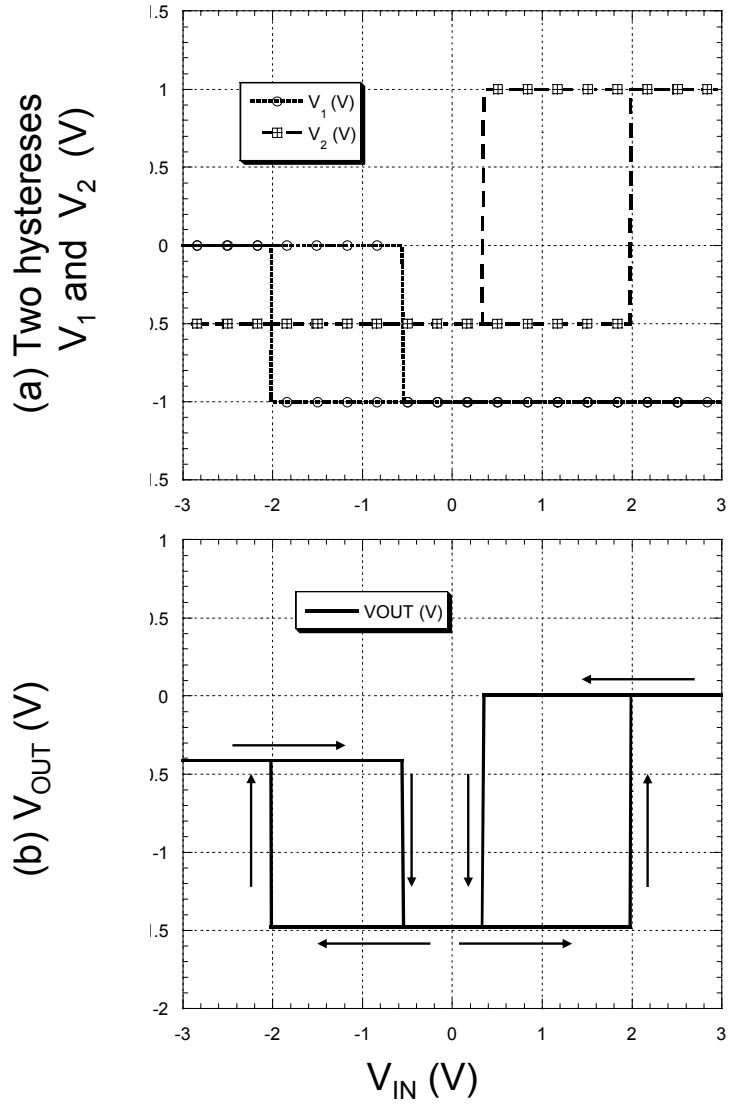

Figure 5.6: PSpice simulation results for the generation of a voltage mode 3-level hysteresis. (a) One forward hysteresis centered at $(1.2V,\ 0.25V)$ with height of $1.5V$ and width of $1.6V$, and one reverse binary hysteresis centered $(-1.2V,\ -0)$ with the height of $1V$ and width of $1.6V$. (b) Output voltage V_{OUT} in the unit of Volts. Both plots have V_{IN} in the unit of Volt as x-axis.

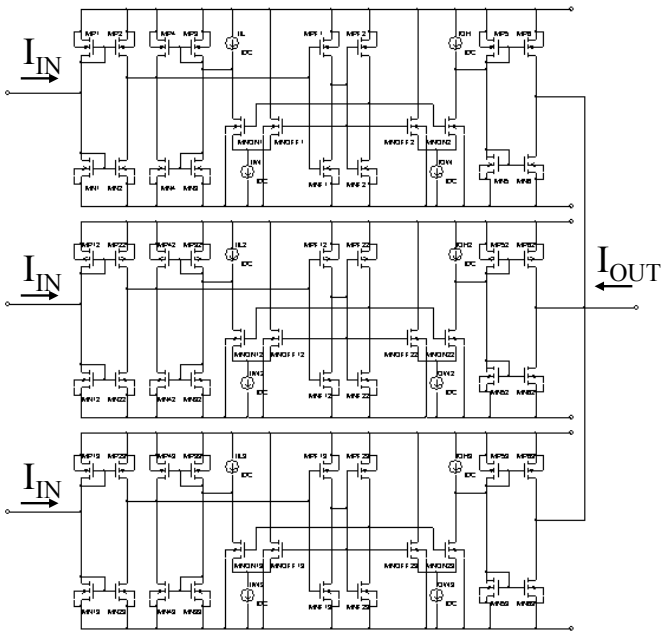

Figure 5.7: Schematic of a CMOS current mode multi-level hysteresis circuit, with three current-input current-output binary hysteresis circuits.

achieved by external current sources, there is complete control on the horizontal position, width, and the height each section of the hysteresis.

Another example is to add binary hysteresis with different height and width and centered at the same horizontal location. Pspice simulations results are shown in Figure 5.9. The three binary hysteresis are centered at $0\mu A$ horizontally. They are have the width of $2\mu A$, $4\mu A$, and $8\mu A$, and the height of $2\mu A$, $4\mu A$, and $8\mu A$. This type of multi-level hysteresis was used by M. J. Smith and C. L. Portmann in their neural optimization circuit as an A/D converter [50]. For this hysteresis in Figure 5.9 (b), if the input current I_{IN} does not sweep all the way past $\pm 4\mu A$, the hysteresis would have various paths, shown as the dart lines.

Figure 5.10 is one Pspice simulation example of adding one forward hysteresis with one reverse hysteresis. Two hystereses with the same height of $8\mu A$ and width of $8\mu A$, centered at different positions are added. The output current I_{OUT} is shown in Figure 5.10 (b). While the input current I_{IN} is sweeping from low to high, the output current I_{OUT} jumps from $0\mu A$ to $8\mu A$ when input current I_{IN} passes $-2\mu A$ and then jumps back to $0\mu A$ when I_{IN} passes $6\mu A$. While the input current I_{IN} is sweeping from high to low, the output current I_{OUT} jumps from $0\mu A$ to $8\mu A$ when input current I_{IN} passes $2\mu A$ and then jumps back to $0\mu A$ when I_{IN} passes $-6\mu A$. Depending on the sweeping direction of the input current, the rectangular waveform is positioned at different locations. There is no overlapping of the switching points of the two binary hysteresis, yet the two rectangular waveforms for the two input sweeping directions overlap.

In order to separate the two rectangular waveforms for the two input sweeping

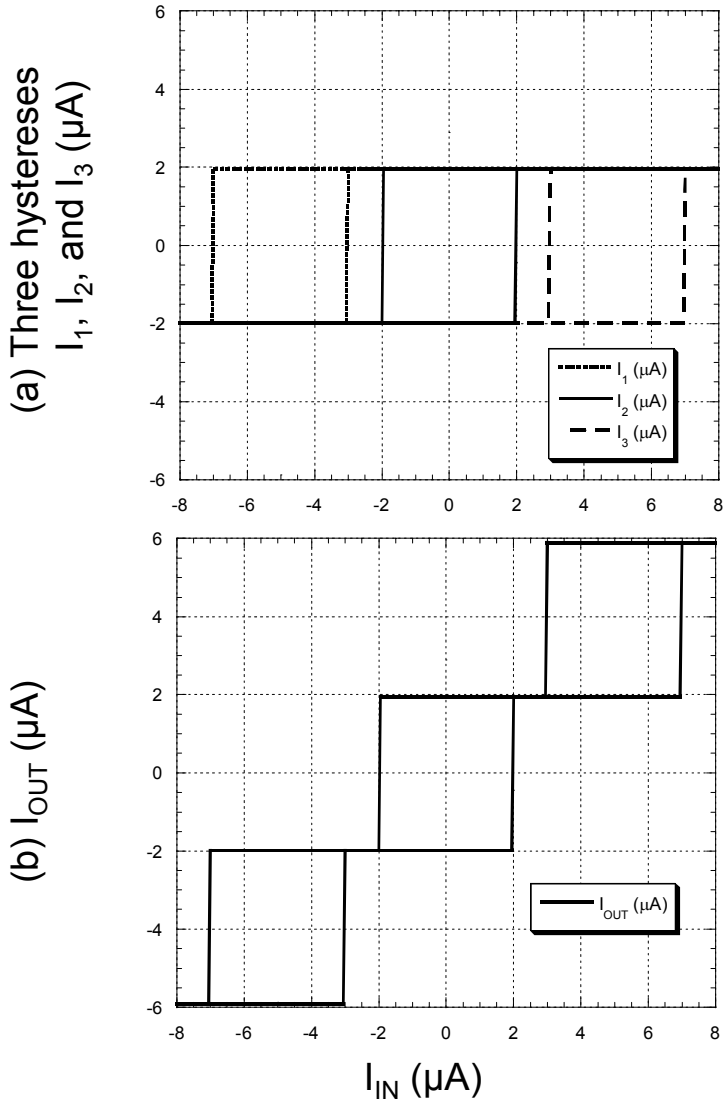

Figure 5.8: PSpice simulation results for the generation of a current mode 4-level hysteresis by adding 3 forward binary hystereses. (a) Three binary hystereses are positioned at different locations horizontally without overlapping of the switching points, in the unit of μA. (b) Output current I_{OUT} in the unit of μA. Both plots have I_{IN} in the unit of μA as x-axis.

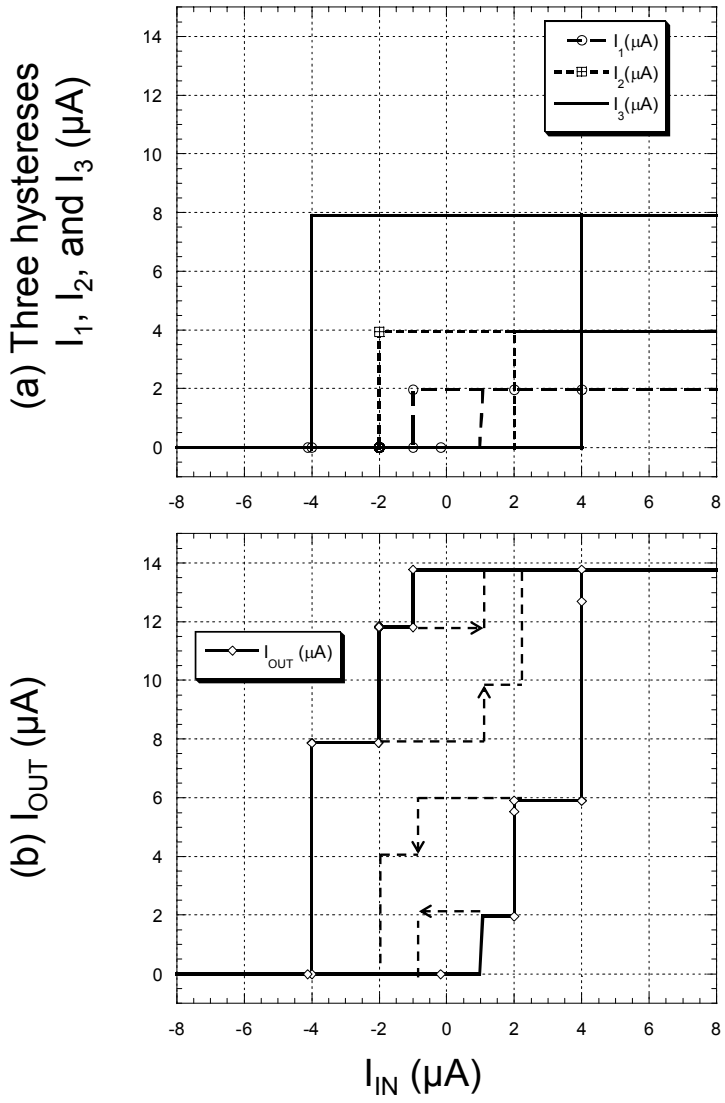

Figure 5.9: PSpice simulation results for the generation of a current mode 8-level hysteresis by adding 3 forward binary hysteresis. (a) Three binary hysteresis positioned at same horizontal position with different height and width, in the unit of μA. (b) Output current I_{OUT} in the unit of μA. Both plots have I_{IN} in the unit of μA as x-axis.

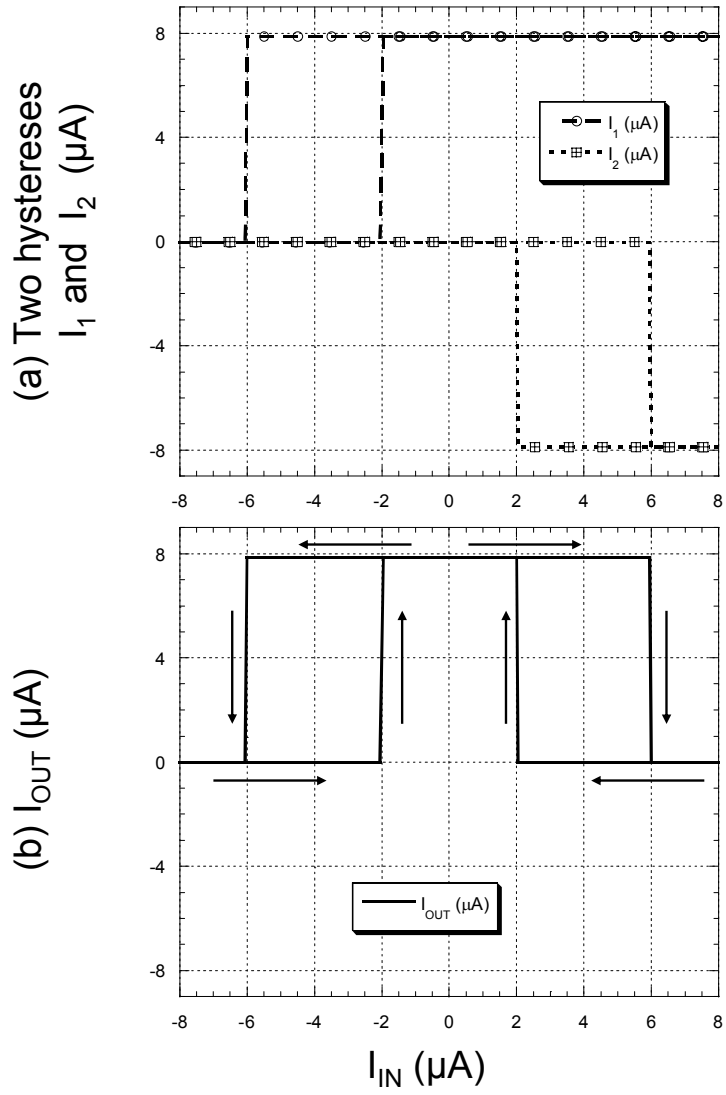

Figure 5.10: PSpice simulation results for the generation of a current mode 2-level hysteresis by adding one forward and one reverse binary hysteresis. (a) Two binary hysteresis, one forward, centered at $(-4\mu A,\ 4\mu A)$, and one reverse, centered at $(4\mu A,\ -4\mu A)$. (b) Output current I_{OUT} in the unit of μA. Both plots have I_{IN} in the unit of μA as x-axis.

directions, we need to make the switching current $I_{L2H}(F)$ of the forward hysteresis higher than the switching current $I_{L2H}(R)$ of the reverse one. One example is shown in Figure 5.11. In this case, the output current I_{OUT} jumps up when input current I_{IN} passes $2\mu A$, and down when I_{IN} passes $6\mu A$, while I_{IN} is increasing. the output current I_{OUT} jumps up when input current I_{IN} passes $-2\mu A$, and down when I_{IN} passes $-6\mu A$, while I_{IN} is decreasing.

5.3.3 Summary

We have demonstrated with PSpice simulations that with the binary hysteresis with full control and analogue adders, various multi-level hystereses can be constructed, with both current mode and voltage mode operation. When n number of binary hysteresis are added, the switching points of each binary hysteresis u^i_{H2L} and u^i_{L2H} (for $i = 1, 2....n$) are preserved in the output of multi-level hysteresis. The height $H^i_H = H^i_+ - H^i_-$ of each binary hysteresis is also preserved in the output, as the difference between hysteresis levels. Also notice that adding current signals is much simpler than adding voltage signals. Therefore, current mode operation is more suitable for addition than voltage mode.

5.4 CMOS Multi-Cell Hysteresis Circuits

After the construction of the multi-level hysteresis, we are moving on to build multi-cell hysteresis. The idea of how to construct a multi-cell hysteresis is shown in Figure 5.12, by multiplying two multi-level hysteresis H_X and H_Y to generate the

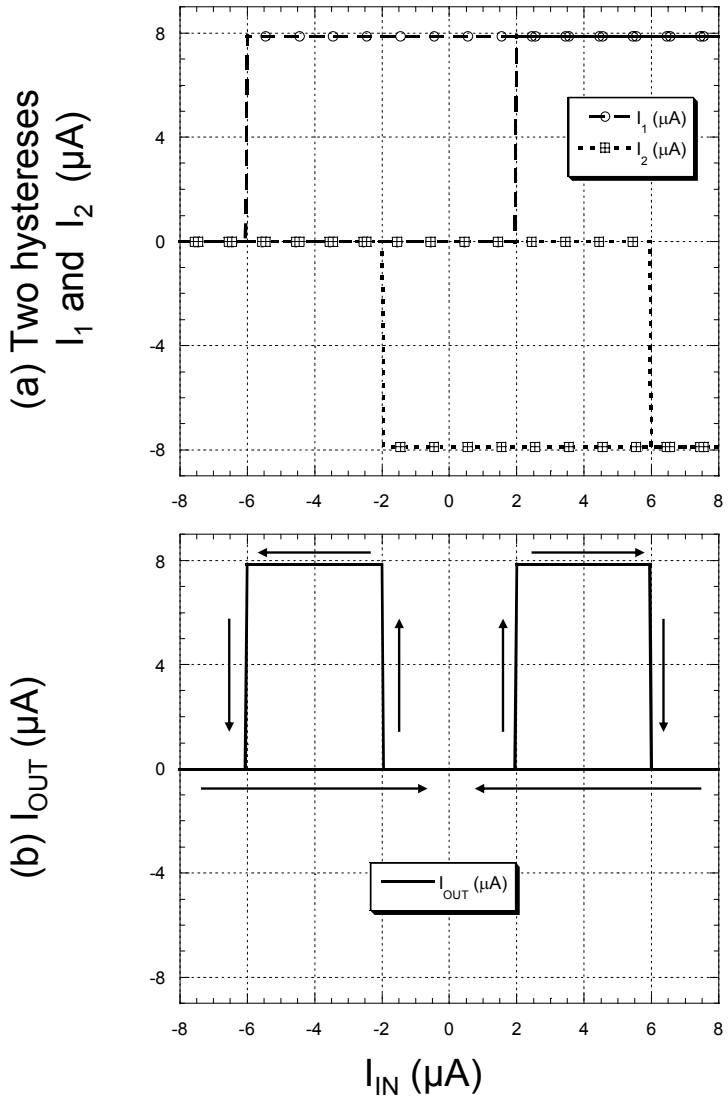

Figure 5.11: PSpice simulation results for the generation of a current mode 2-level hysteresis by adding one forward and one reverse binary hysteresis. (a) Two binary hysteresis, one forward, centered at $(-2\mu A,\ 4\mu A)$, and one reverse, centered at $(2\mu A,\ -4\mu A)$. (b) Output current I_{OUT} in the unit of μA. Both plots have I_{IN} in the unit of μA as x-axis.

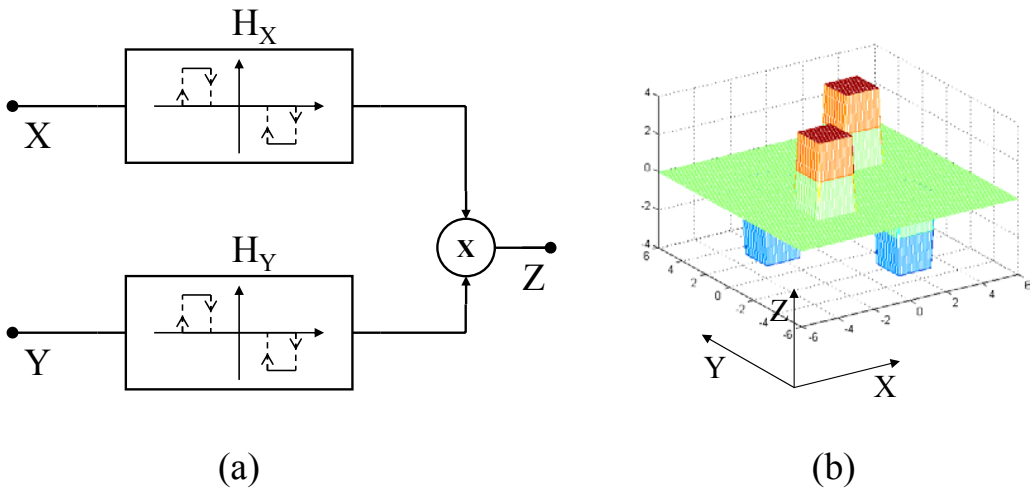

Figure 5.12: Generation of 2-dimensional 3-level hysteresis cubes. (a) Schematic. (b) 3-D plot of the hysteresis cubes

output Z. A 3-dimensional plot of 2-dimensional 3-level hysteresis cubes is shown in Figure 5.12 (b). A total of four hysteresis cubes are generated in this case.

5.4.1 CMOS Voltage Mode Multi-Cell Hysteresis

The schematic of a CMOS voltage mode circuit to generate multi-cell hysteresis is shown in Figure 5.13, with four binary voltage-input voltage-output hysteresis circuits, two analogue voltage adders and one analogue voltage multiplier. The top two binary hysteresis circuits and the top voltage adder form one multi-level voltage mode multi-level hysteresis, which is tuned to generate the three-level hysteresis signal as shown in Figure 5.5 (b). The left bottom part of the circuit are identical to the left top part, that gives the same three-level hysteresis.

Figure 5.14 shows the PSpice simulation results of the CMOS voltage mode multi-cell circuit, as shown in Figure 5.13. Input V_{INX} is triangular wave with the

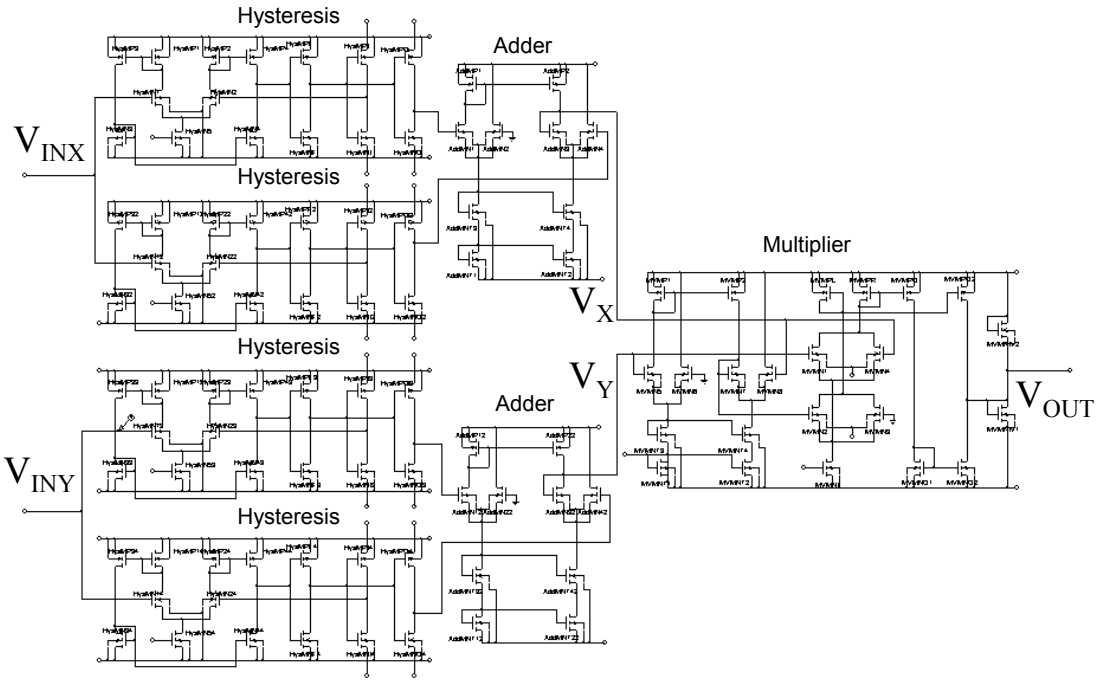

Figure 5.13: Schematic of a CMOS voltage mode multi-cell hysteresis circuit, with 4 binary voltage-input voltage-output hysteresis circuits on the left, 2 analogue voltage adders in the middle, and one analogue voltage multiplier on the right.

period of $2S$, and V_{INY} is a slower triangular wave with the period of $80S$. The multi-level hysteresis signals V_X and V_Y are shown in Figure 5.14 (b). Notice that there are some spikes on the signal V_X. Those spikes are due to the simulation error, not the real circuit response, since the time scales of V_{INX} and V_{INY} are very different. The output voltage V_{OUT} is shown in Figure 5.14 (c).

To get a better look at the response of the output signal V_{OUT} to the two inputs V_{INX} and V_{INY}, the two multi-level hysteresis signal V_X and V_Y are fed to the multiplier. Then a MATLAB program is used to sample the output V_{OUT} and to give three dimensional plots. The three dimensional plots of V_{OUT}, as the z-axis, with respect to V_{INX} and V_{INY} are shown in Figure 5.15.

All four plots in Figure 5.15 can be overlaid on top of each other, as shown in Figure 5.16. Clearly, there are 4 hysteresis cells in this case.

5.4.2 CMOS Current Mode Multi-Cell Hysteresis

The schematic of a CMOS current mode circuit to generate multi-cell hysteresis is shown in Figure 5.17, with four binary current-input current-output hysteresis circuits and one analogue voltage multiplier. The top left two binary hysteresis circuits form one multi-level current mode multi-level hysteresis. The top right part of the circuit are identical to the top left part, that gives the same multi-level hysteresis.

Two identical multi-level hysteresis signals I_X and I_Y are fed to a current multiplier to give the output I_{OUT}. Then a MATLAB program is used to sample

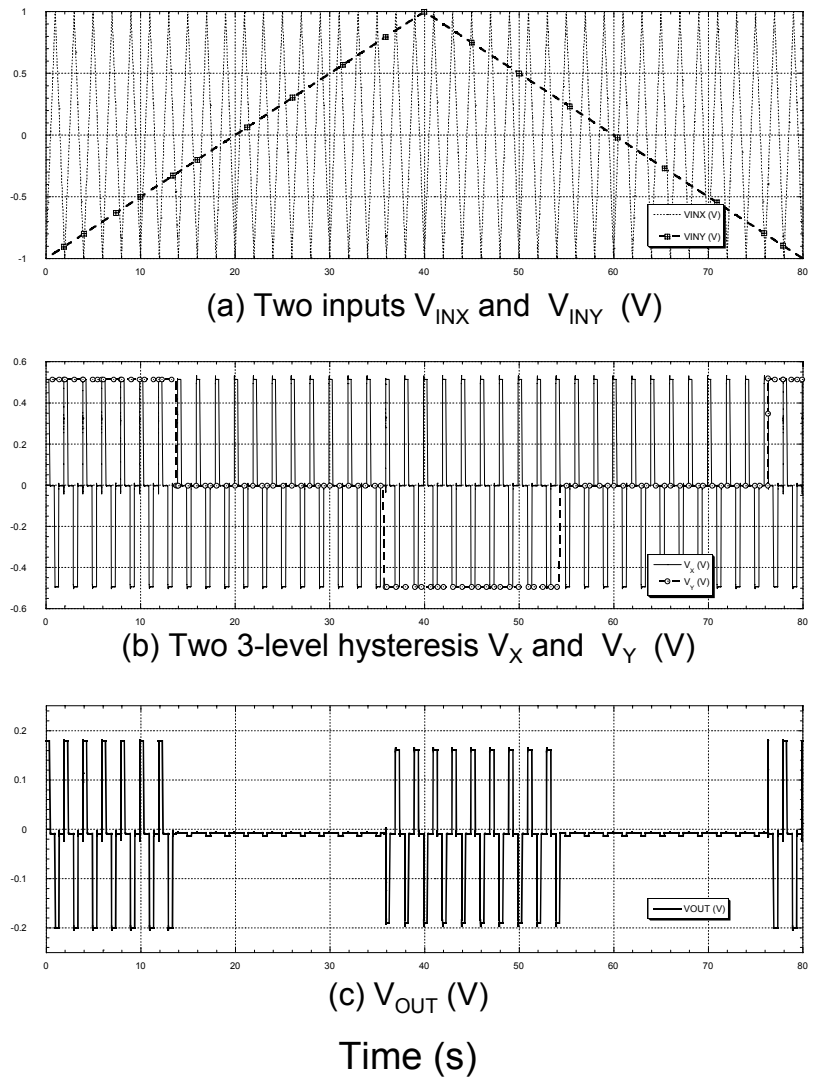

Figure 5.14: PSpice simulation results for the CMOS voltage mode multi-cell hysteresis circuits in Figure 5.13. (a) Two triangular wave inputs: V_{INX} with period of $2S$, and V_{INY} with period of $80S$. (b) Two 3-level hysteresis, V_X the thin solid line, and V_Y the thick dart line with circles. (c) Output voltage V_{OUT}. All three plots have time as the x-axis with the unit of second.

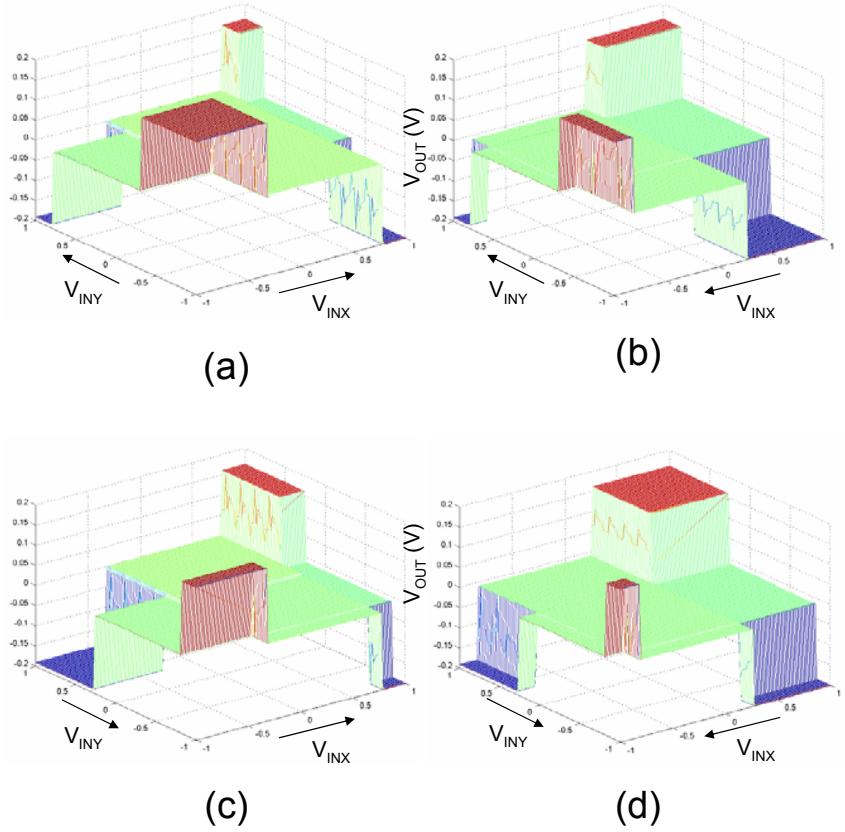

Figure 5.15: Voltage mode multi-cell hysteresis, three dimensional plot of V_{OUT} with respect to V_{INX} and V_{INY}. (a) Both V_{INX} and V_{INY} sweep from low to high. (b) V_{INX} sweeps from high to low, and V_{INY} sweeps from low to high. (c) V_{INX} sweeps from low to high, and V_{INY} sweeps from high to low. (d) Both V_{INX} and V_{INY} sweep from high to low.

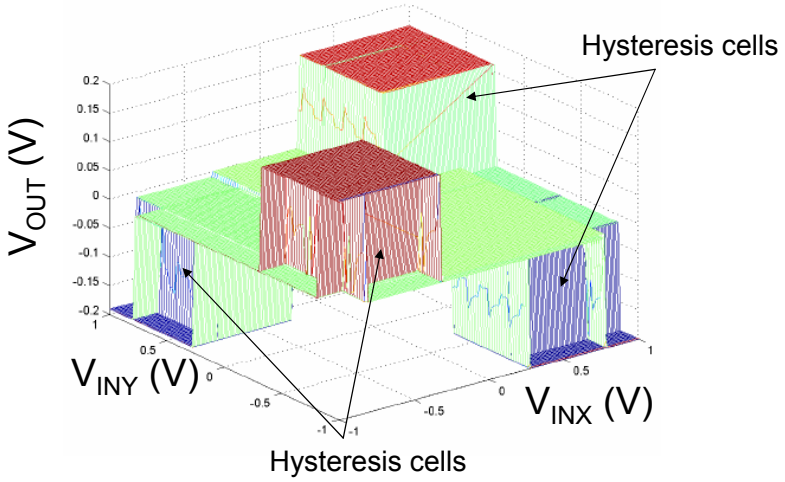

Figure 5.16: Voltage mode multi-cell hysteresis, with 4 cells.

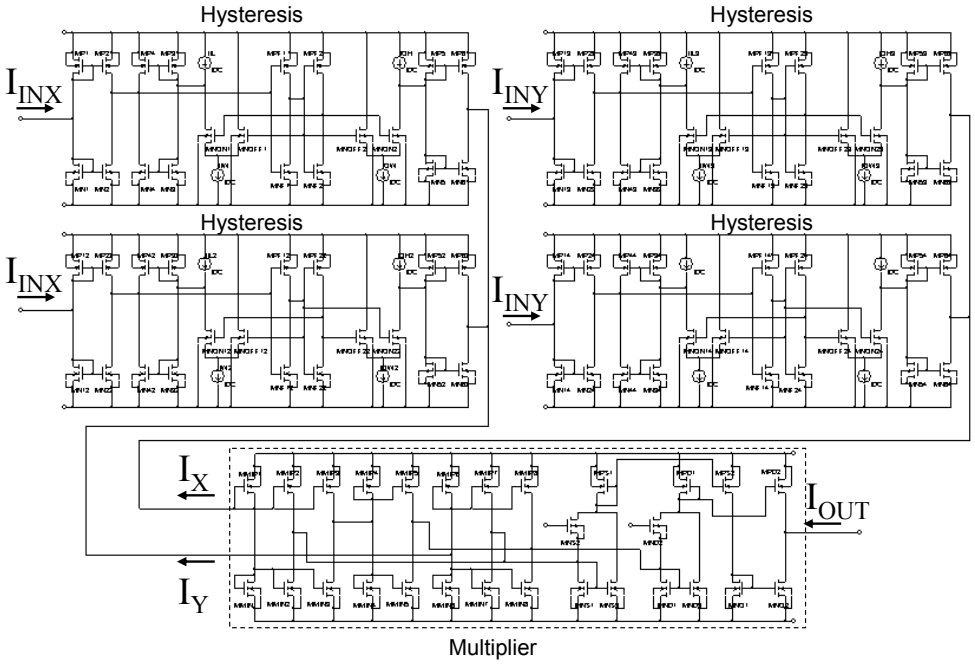

Figure 5.17: Schematic of a CMOS current mode multi-cell hysteresis circuit, with 4 binary current-input current-output hysteresis circuits on the top, and one analogue current multiplier on the bottom.

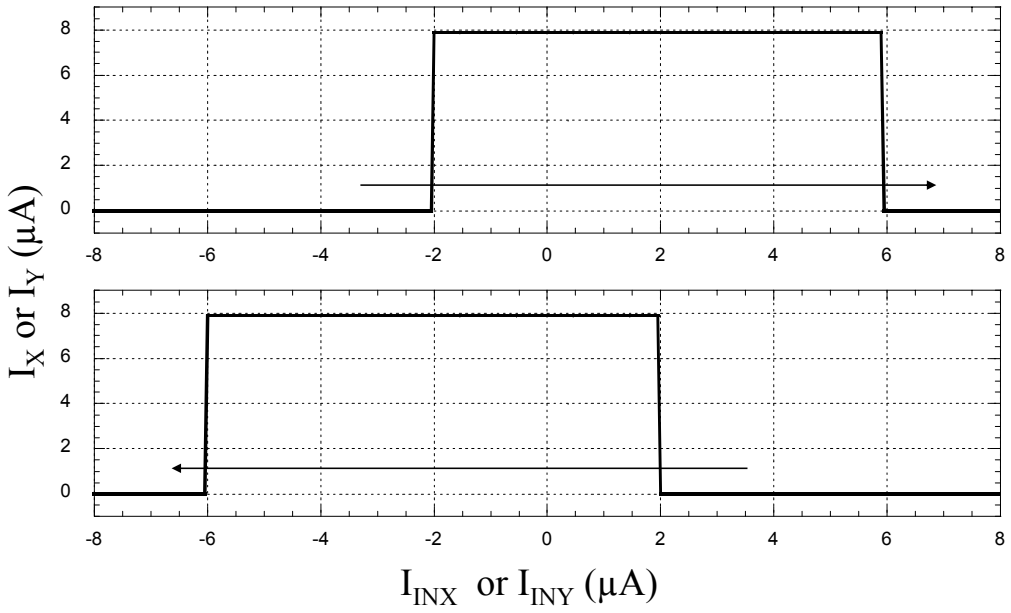

Figure 5.18: Multi-level hysteresis signals V_X and V_Y, that is fed to current multiplier to generate current mode multi-cell hysteresis.

the output I_{OUT} and give three dimensional plots. I_X and I_Y are shown in Figure 5.18. The arrows in the plots indicate the sweeping directions of the input current I_{INX} and I_{INY}, increasing on the top plot and decreasing on the bottom plot.

The three dimensional plots of I_{OUT}, as the z-axis, with respect to I_{INX} and I_{INY} are shown in Figure 5.19.

Another example is shown in Figure 5.20, where all four plots are overlaid for I_{INX} and I_{INY} sweeping both directions. I_X and I_Y are fed to a current multiplier. I_X and I_Y are shown in Figure 5.20 (a), only the right rectangular wave can be seen when I_{INX} or I_{INY} increases, and only the left rectangular wave can be seen when I_{INX} or I_{INY} decreases.

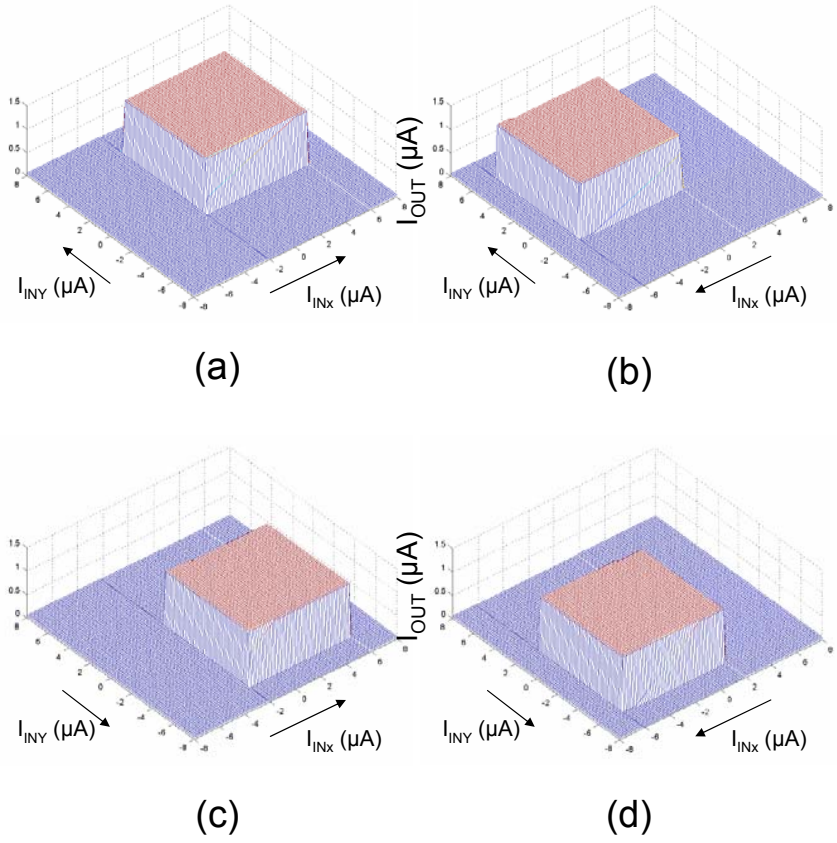

Figure 5.19: Current mode multi-cell hysteresis, three dimensional plot of I_{OUT} with respect to I_{INX} and I_{INY}. (a) Both I_{INX} and I_{INY} sweep from low to high. (b) I_{INX} sweeps from high to low, and I_{INY} sweeps from low to high. (c) I_{INX} sweeps from low to high, and I_{INY} sweeps from high to low. (d) Both I_{INX} and I_{INY} sweep from high to low.

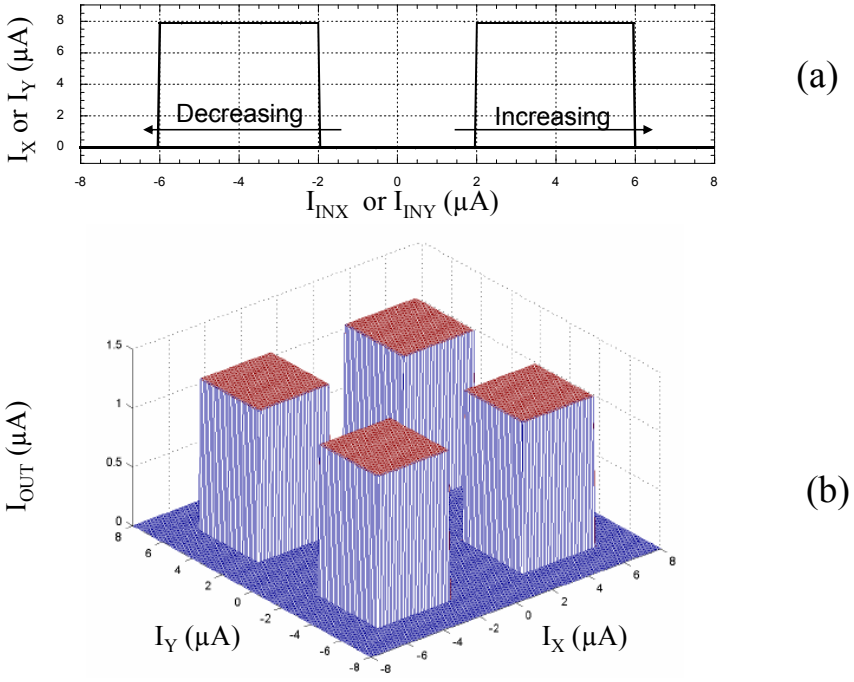

Figure 5.20: Current mode multi-cell hysteresis. (a) I_X or I_Y, with the right rectangular waveform when I_{INX} or I_{INY} sweeping from low to high, and the left rectangular wave when I_{INX} or I_{INY} sweeping from high to low. (b)I_{OUT}, top most lobe for both I_{INX} and I_{INY} increasing, right most lobe for I_{INX} increasing and I_{INY} decreasing, left most lobe for I_{INX} decreasing and I_{INY} increasing, and bottom most lobe for both I_{INX} and I_{INY} decreasing.

5.4.3 Summary

With the binary hysteresis circuits, analogue adders and multipliers, we are able to build CMOS circuits to generate multi-cell hysteresis in both voltage and current mode. In this section, we have demonstrated how to generate various hysteresis cubes the two-dimensional domain.

5.5 More Discussions on Multi-Cell Hysteresis

We have generated hysteresis cubes in the two dimensional domain. In this section, we are suggesting two ways of generalizing the results into higher dimensions.

Multiplying several arbitrary multi-level hystereses could get really complicated. Let us take one of the simplest cases as an example, that of multiplying two binary hysteresis. Two binary hysteresis H_X and H_Y, as shown in Figure 5.21 (a), both have H_- not zero but the value of 1. The two signals, H_X and H_Y, do not have the same value of H_+, for signal H_X, $H_+ = 2$, and for H_Y, $H_+ = 3$. H_X is a forward binary hysteresis with $X_{L2H} = 0.5$ and $X_{H2L} = -0.5$. H_Y is a forward binary hysteresis with $Y_{L2H} = 0.4$ and $Y_{H2L} = -0.4$. The three dimensional plots of the product of H_X and H_Y with different sweeping direction of input signal X and Y are shown in Figure 5.21 (b1)$\sim$(b4). Notice that the output $Z = H_X H_Y$ has 4 values in the region of $-0.5 < X < 0.5$ and $-0.4 < Y < 0.4$. By setting H_- or H_+ to zero can simplify the situation.

One method for achieving multi-cell hysteresis is using a certain type of multi-level hysteresis. As an example the hysteresis shown in the simulation results in

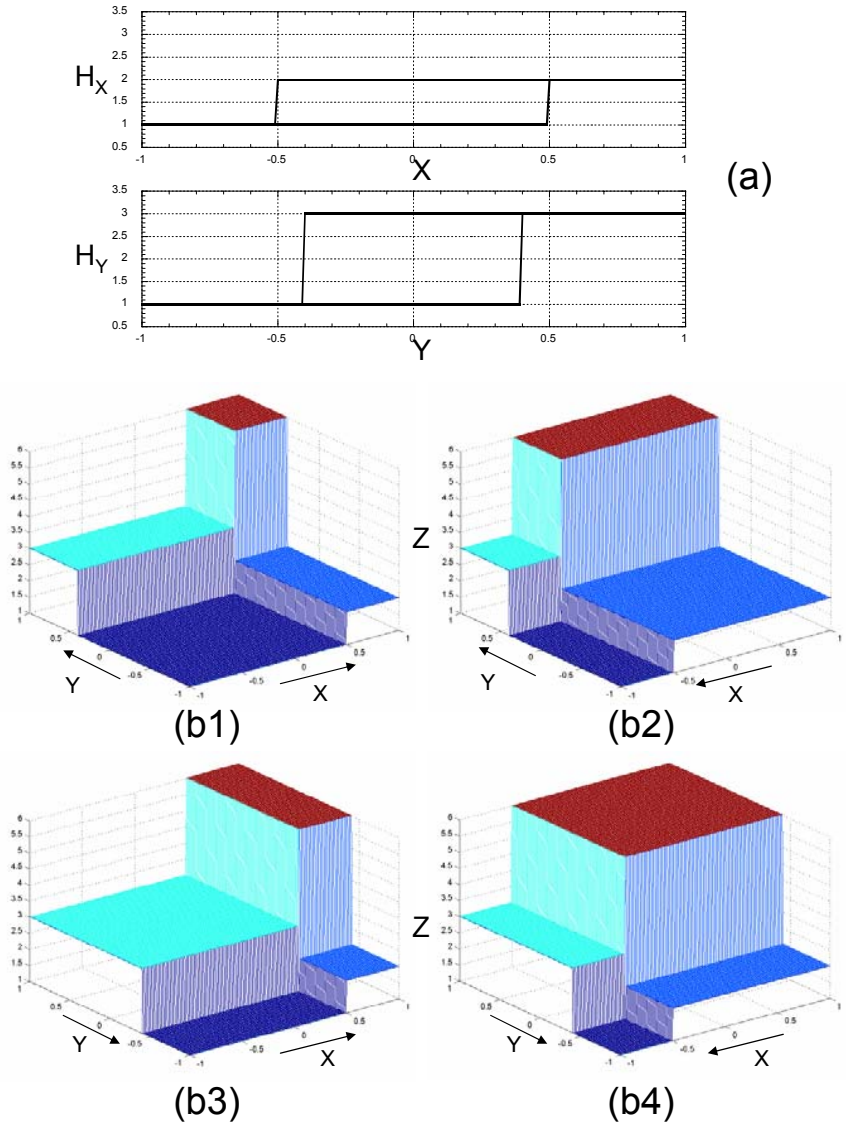

Figure 5.21: Multiplication of two binary hysteresis H_X and H_Y. (a)H_X and H_Y with respect to X and Y. (b1)$\sim$(b2) $Z = H_X H_Y$ with respect to X and Y.

Figure 5.10 (b), and in Figure 5.11 (b), the hysteresis has limited width and its value is always zero outside the width. For this kind of hysteresis, more hysteresis can be added to form a chain. Each hysteresis section on the chain has adjustable input location, width, and output height. Then various numbers of such hysteresis chains can be multiplied to give multi-dimensional hysteresis cells. Figure 5.22 illustrate such a case in two dimension. Two chains of hysteresis are shown in Figure 5.22 (a), the output Z is shown in Figure 5.22 (b). With three hysteresis sections in H_X and two hysteresis sections in H_Y, the output $Z = H_X H_Y$ has six hysteresis cells.

It is not difficult to picture this kind of multi-cell hysteresis, for which, we can increase the number of hysteresis sections on each chain, and we can also increase the number of chains. If there are n chains of hysteresis, and each chain has m_i (for $i = 1, 2, ..., n$) hysteresis sections, the total number of cells N can be generated is given by Equation (5.1).

$$N = \prod_{i=1}^{n} m_i \tag{5.1}$$

Another way of making multi-cell hysteresis is to make a single multi-dimensional hysteresis cell then add which together. For example, we can take n forward binary hysteresis, each described by Equation (5.2), with $i = 1, 2, ..., n$. All H_-^i are tuned to be zero. All H_+^i are tuned to be one except $H_+^1 = H_+$. Then the output Z of the multiplication is given by Equation (5.3), where $U = [u^1, u^2, u^3, ...u^n]$ is the n-dimensional input. This single multi-dimensional hysteresis cell has tunable input widths, position, and output height H_+. Changing any or all of the forward binary hystereses would give similar results. If number m of such n-dimensional single cell

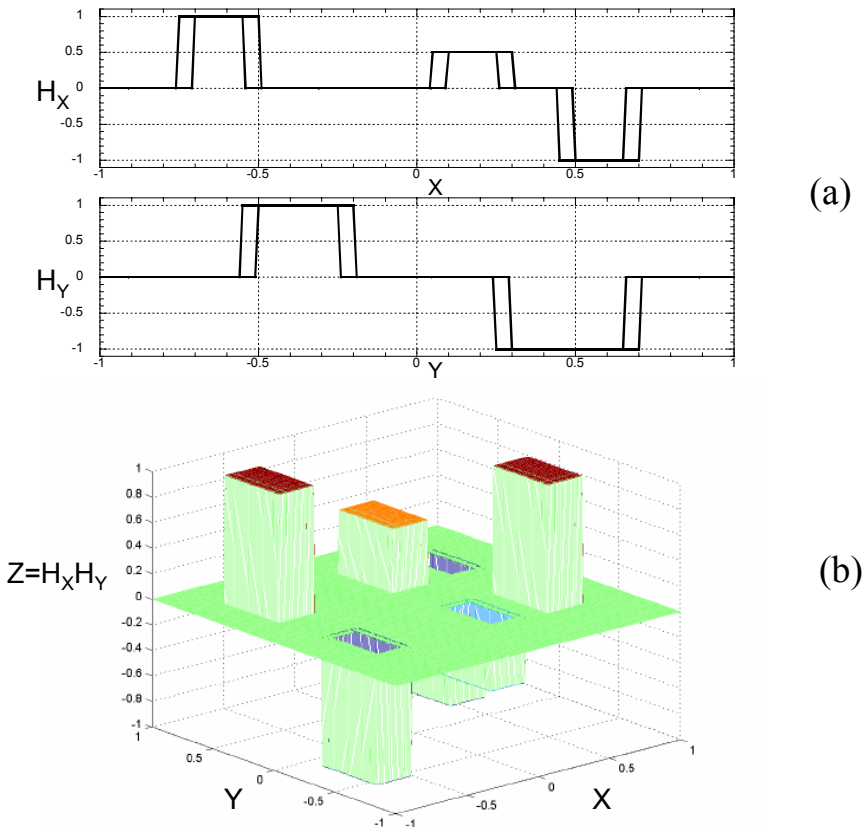

Figure 5.22: Generalized case for generating hysteresis cells. (a) Multi-level hysteresis that are the inputs for a multiplier. H_X has three hysteresis sections and H_Y has two hysteresis sections. (b) Multi-cell hysteresis, with six hysteresis cells.

hystereses are added together, n-dimensional n-level hysteresis can be generated. For example, the multi-cell hysteresis shown in Figure 5.16 can be generated this way.

$$y^i(u^i, y_0^i) = \begin{cases} H_+^i & u^i > u_{L2H}^i \\ H_+^i & u_{H2L}^i \le u^i \le u_{L2H}^i \quad \text{if} \quad y_0^i = H_+^i \\ H_-^i & u_{H2L}^i \le u^i \le u_{L2H}^i \quad \text{if} \quad y_0^i = H_-^i \\ H_-^i & u^i < u_{H2L}^i \end{cases} \tag{5.2}$$

$$Z(u^i, y_0^i) = \prod_{i=1}^{n} y^i(u^i, y_0^i) \tag{5.3}$$

The above two methods are certainly not the only two ways of making multi-level multi-dimensional hysteresis. One can multiply any number of multi-level hysteresis to get multi-cell hysteresis, but describing such multi-cell hysteresis might be complicated.

5.6 Possible Application of Multi-Dimensional Hysteresis Cell on Chaos Generation

Due to the interest of studying nonlinear phenomena, simple chaotic oscillators have been studied extensively, the idea of using hysteresis as the nonlinear element for generating chaotic signals was suggested by O. E. Rössler [45]. Then many of the hysteresis chaos generators have been published [35] [61] [22]. Following later, different approaches for higher orders of chaotic systems were proposed, that includes adding additional story elements by T. Saito [46], and using multi-level hysteresis

by J. E. Varrientos and E. Sánchez-Sinencio [56]. Recently, F. Han [20] extended the result into 9-scrolls by using 9-level hysteresis.

A general continuous time second-order linear system can be described by the state equation shown in Equation (5.4), with x_1 and x_2 the two state variables. The general solution of the state equation is a set of spirals, given in Equation (5.5), with $\omega = \sqrt{1-\sigma^2}$ and θ = angle of $(-\sigma + j\omega)$. When binary hysteresis is introduced in the system, then the input space is separated in two half planes, for each half plane, the two sets of spirals have different equilibrium points. The system starts with staying on one plane and evolves along one spiral and when it hits the boundary, it jumps to the other plane. Then it evolves along the spiral with a different equilibrium point until it hits the boundary and jumps again, and so on so forth. When multi-level hysteresis is adding to the system, the input space is separated in many strip planes, on each one of the planes, each set of spirals has a different center. That system similarly evolves along the spiral until it hits the boundary and jumps to a different plane and evolves along a different spiral. Multi-level hysteresis introduces more planes and boundaries into the system and thus, increases the complexity of the system. Since both binary hysteresis and multi-level hysteresis have one dimensional input functions, the boundaries are only along one of the input.

$$\begin{aligned} \frac{dx_1}{dt} &= x_2 \\ \frac{dx_2}{dt} &= -x_1 - 2\sigma x_2 \end{aligned} \tag{5.4}$$

$$x_1(t) = Ke^{-\sigma t}cos(\omega t + \phi)$$
$$x_2(t) = Ke^{-\sigma t}cos(\omega t + \phi + \theta) \tag{5.5}$$

Our effort is to introduce more planes and boundaries by using two-dimensional hysteresis cell. When a two-dimensional hysteresis cell is brought into the system, the second-order system can be described by semistate equations, as Equations (5.6), with a_1 and a_2 as constants. $h_1(x_1)$ and $h_2(x_2)$ are both binary hysteresis. The multiplication of $h_1(x_1)$ and $h_2(x_2)$ gives two-dimensional multi-level hysteresis cell(s).

$$\frac{dx_1}{dt} = x_2 + a_1 h_1(x_1)h_2(x_2)$$
$$\frac{dx_2}{dt} = -x_1 - 2\sigma x_2 + a_2 h_1(x_1)h_2(x_2) \tag{5.6}$$

Equations (5.6) are suitable for electronic realization. The schematic of the electronic circuits using mainly voltage control current sources as building parts is shown in Figure 5.23. The binary hysteresis parts of the circuit for both h_1 and h_2 are outlined by dot-dash lines and marked with 'Hysteresis'. The multiplier gives the product of h_1 and h_2, which is a two-dimensional multi-level hysteresis.

One example of PSpice simulation results for Equations (5.6) is shown in Figure 5.25 and Figure 5.26. h_1 is a reverse hysteresis with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 1$, and $u_{L2L} = 0$, and h_2 is also a reverse one with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 0$, and $u_{L2H} = -1$. Therefore, the product of h_1 and h_2 creates two values 1 and 0, and four boundaries, $x_1 = 0$, $x_1 = 1$, $x_2 = -1$, and $x_2 = 0$. The three-dimensional plot of $h_1(x_1)h_2(x_2)$ vs x_1 and x_2 is shown in Figure 5.24. Figure 5.25 is the time evolution of V_1 and V_2. Figure 5.26 gives the phase trajectory. Since there are two planes, there are two sets of spirals, centered $(0,\ 0)$ and $(-1,\ 0.3)$. When the spiral

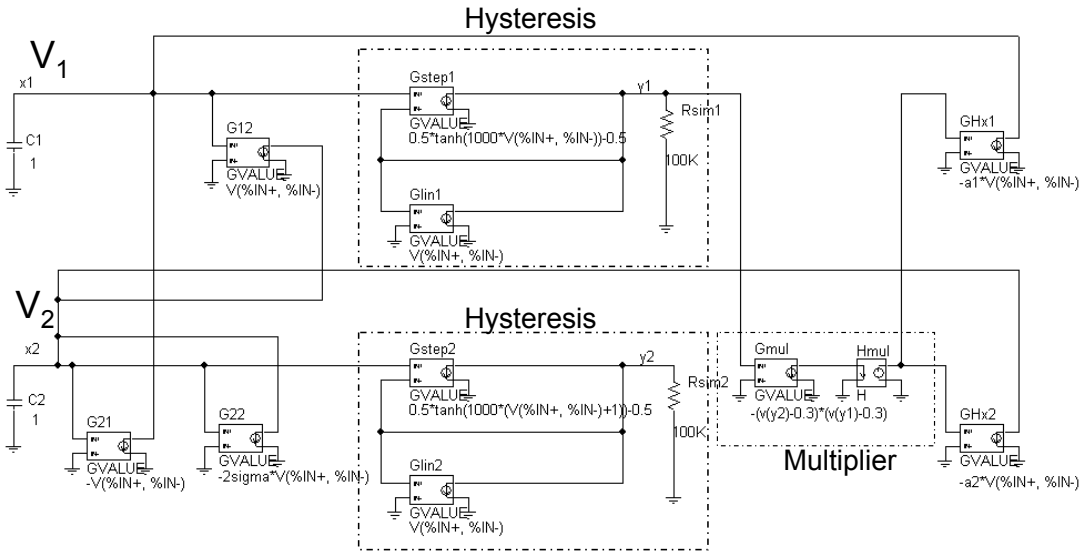

Figure 5.23: Schematic for generating chaotic signal using two dimensional hysteresis cell.

hit one of the four boundaries in the right direction, (the h_1h_2 value changes), the system jumps to a different spiral. For this simulation, there is only one jump at $x_2 = -1$ which is bit hard to see, yet the jumps happening at $x_1 = 0$, $x_1 = 1$, and $x_2 = 0$ are quite obvious.

Another example of the same hysteresis cell but different constants a_1, a_2 and σ is shown in Figure 5.27 for time evolution, and in Figure 5.28 for the phase trajectory. For this one, there is no jumping at $x_1 = 1$ but the jumps at $x_1 = 0$, $x_2 = -1$, and $x_2 = 0$ are obvious.

To make it more interesting, we change the value of h_+ and h_- to 0.7 and -0.3 for both h_1 and h_2. The product of h_1 and h_2 has three values 0.49, 0.09 and -0.21, therefore, we should have three sets of spirals with three centers. The three-dimensional plot of $h_1(x_1)h_2(x_2)$ vs x_1 and x_2 is shown in Figure 5.29. The

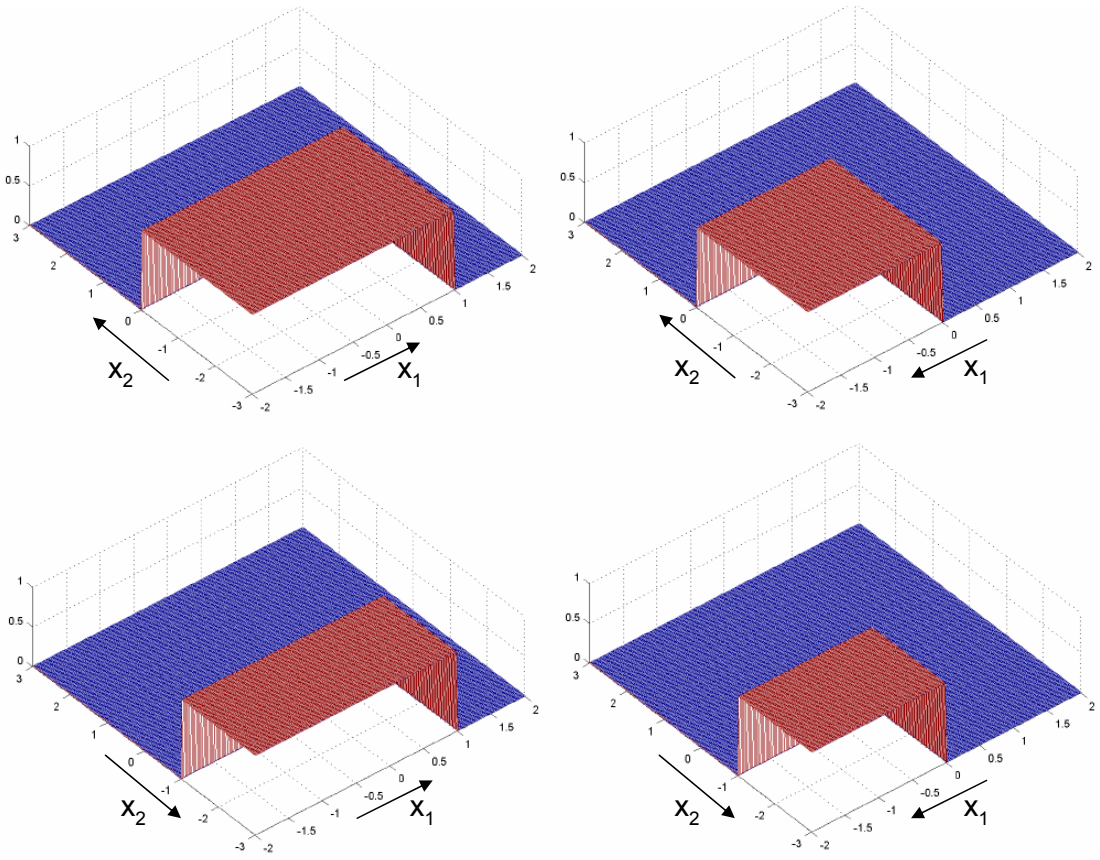

Figure 5.24: Two-dimensional hysteresis $h_1(x_1)h_2(x_2)$ vs x_1 and x_2. With different sweeping directions of x_1 and x_2, the boundaries are at different locations.

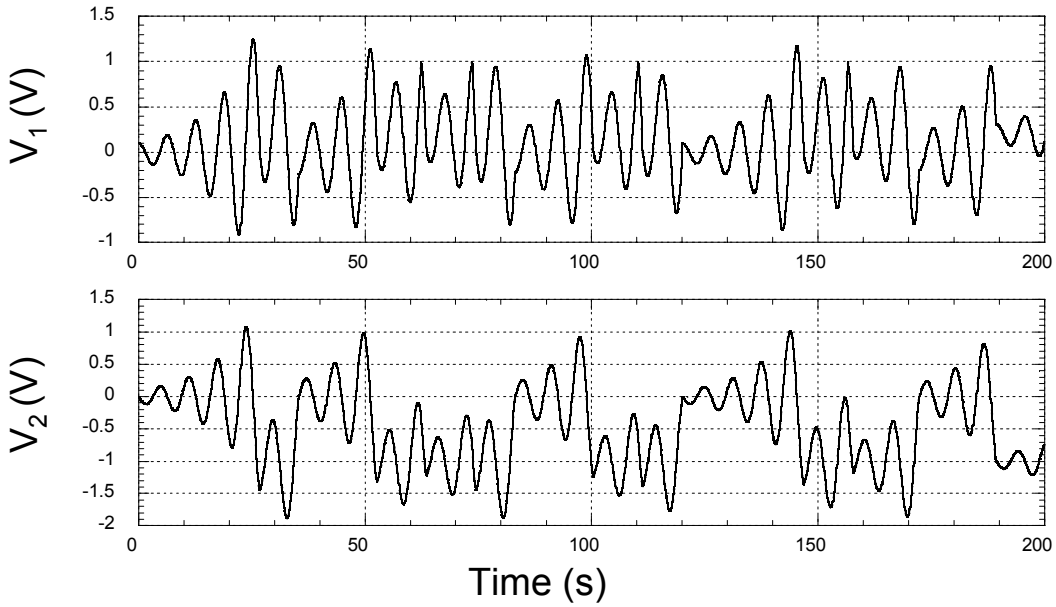

Figure 5.25: Time evolution of V_1 and V_2, for $a1 = 1$, $a2 = 0.41$, $\sigma = -0.1$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 1$, and $u_{L2H} = 0$, and h_2 is also a reverse one with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

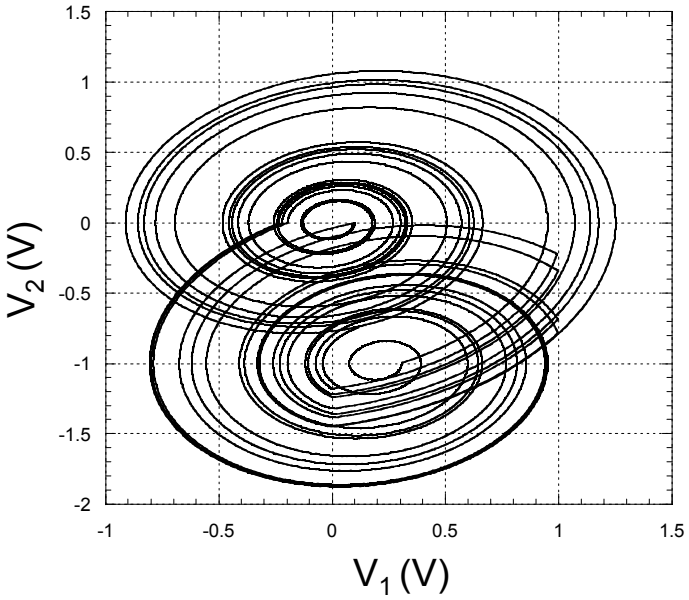

Figure 5.26: Phase trajectories of V_1 and V_2, for $a1 = 1$, $a2 = 0.41$, $\sigma = -0.1$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 1$, and $u_{L2H} = 0$, and h_2 is also a reverse one with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

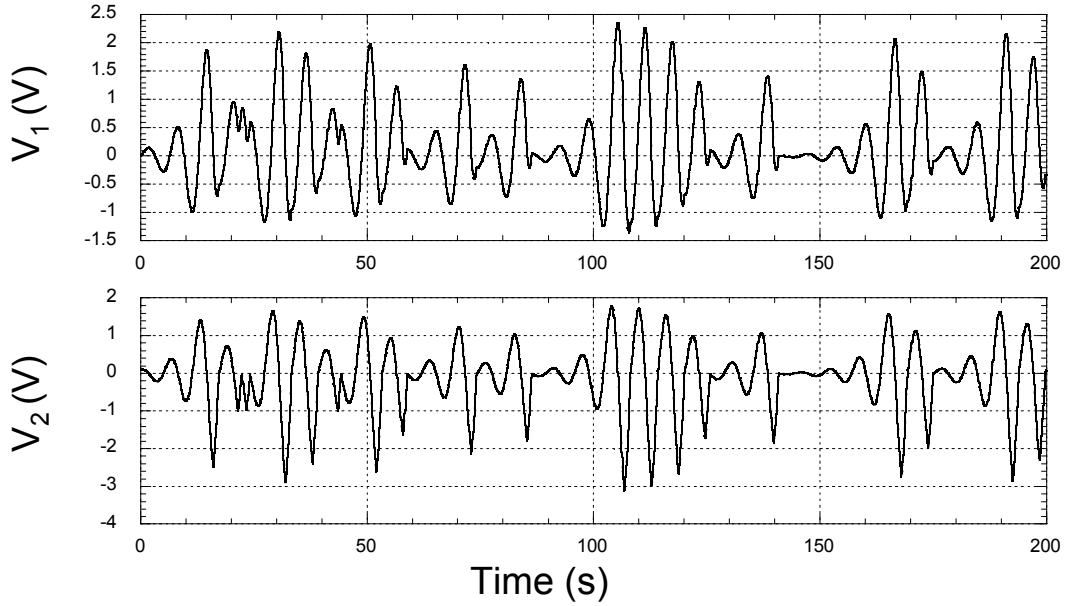

Figure 5.27: Time evolution of V_1 and V_2, for $a1 = 1$, $a2 = 2$, $\sigma = -0.2$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 1$, and $u_{L2L} = 0$, and h_2 is also a reverse one with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

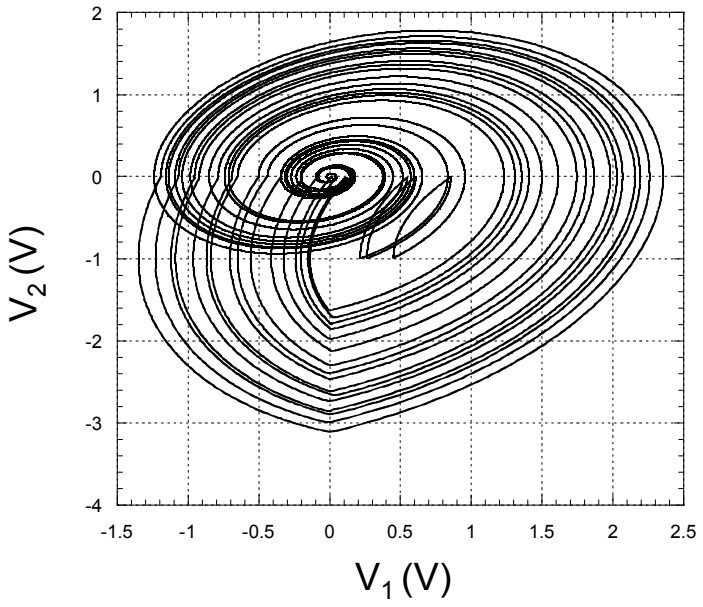

Figure 5.28: Phase trajectory of V_1 and V_2, for $a1 = 1$, $a2 = 2$, $\sigma = -0.2$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 1$, and $u_{L2L} = 0$, and h_2 is also a reverse one with $h_+ = 1$, $h_- = 0$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

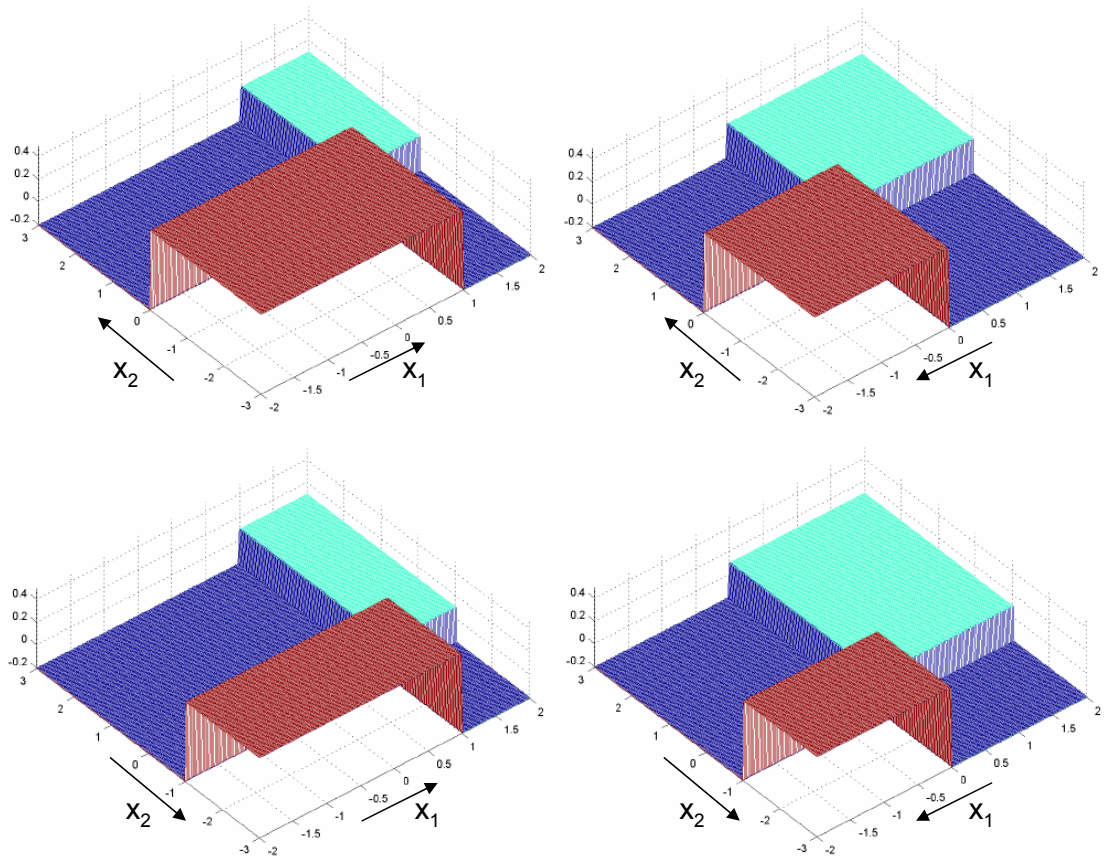

Figure 5.29: Two-dimensional hysteresis $h_1(x_1)h_2(x_2)$ vs x_1 and x_2. With different sweeping directions of x_1 and x_2, the boundaries are at different locations.

simulation results are shown in Figure 5.30 for time evolution, and in Figure 5.31 for the phase trajectory. The jumps on the four boundaries are obvious and clearly, there are three sets of spirals with three centers.

The above are just very primitive demonstrations that it is quite possible to use multi-cell hysteresis to generate chaotic signals.

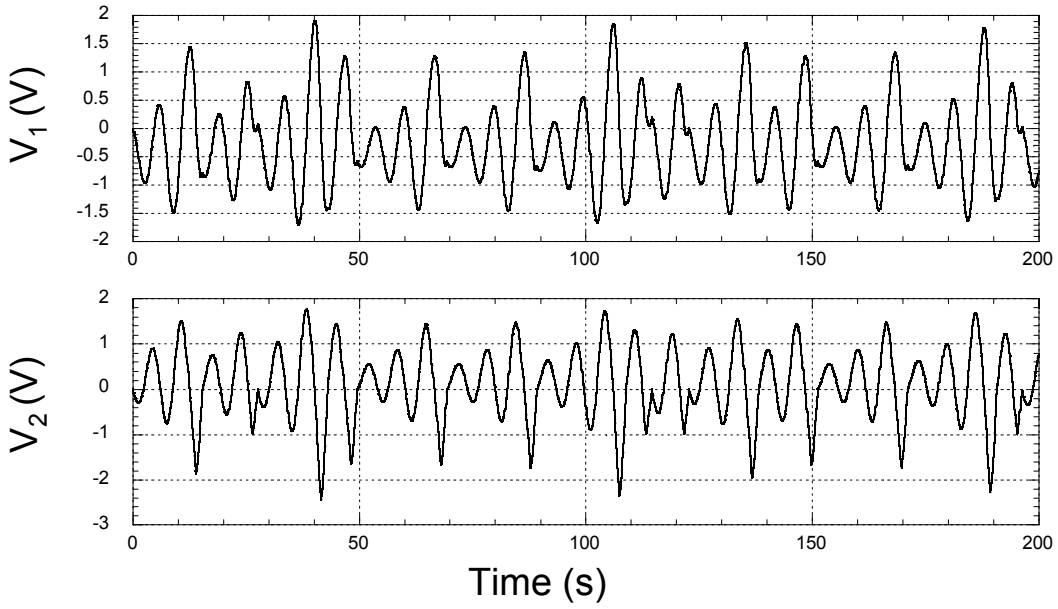

Figure 5.30: Time evolution of V_1 and V_2, for $a1 = 1$, $a2 = 2$, $\sigma = -0.1$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 0.7$, $h_- = -0.3$, $u_{H2L} = 1$, and $u_{L2L} = 0$, and h_2 is also a reverse one with $h_+ = 0.7$, $h_- = 0.3$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

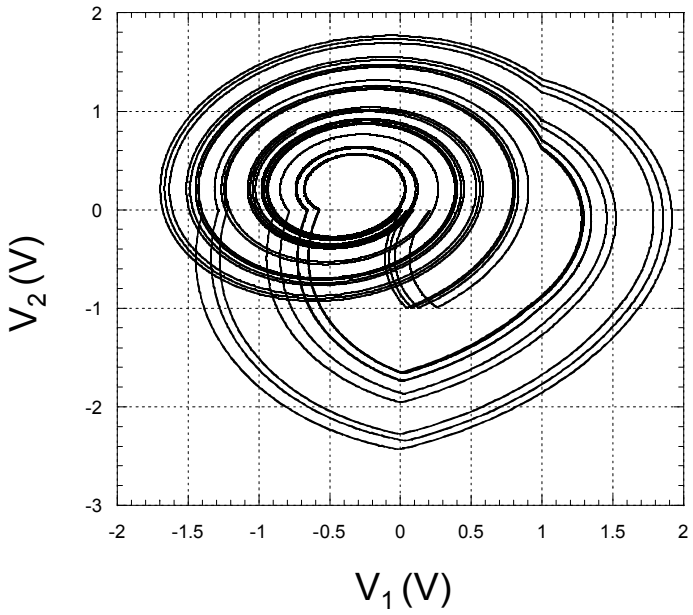

Figure 5.31: Phase trajectory of V_1 and V_2, for $a1 = 1$, $a2 = 2$, $\sigma = -0.1$ with initial condition $V_1 = 0.1$ and $V_2 = 0$. h_1 is a reverse hysteresis with $h_+ = 0.7$, $h_- = -0.3$, $u_{H2L} = 1$, and $u_{L2L} = 0$, and h_2 is also a reverse one with $h_+ = 0.7$, $h_- = 0.3$, $u_{H2L} = 0$, and $u_{L2H} = -1$.

5.7 Summary

In this chapter, we have demonstrated how to generate various multi-level hystereses using CMOS circuits. We have also achieved two-dimensional multi-level hysteresis with CMOS circuit realizations. We pointed out two methods to generalize the results into multi-dimensional, multi-level hysteresis cells. In the end, we suggested the possible application of multi-cell hysteresis on the generation of chaotic signals.

Chapter 6

Summary and Open Values

6.1 Summary

Here is the summary of what has been achieved in this dissertation:

First, the new concept of multi-cell hysteresis is introduced the first time in Chapter one.

Second, in Chapter three, a group of CMOS binary hysteresis circuits with full control which operate in all four quadrants have been achieved in simulations. These CMOS binary hysteresis circuits include the following four kinds: current-input current-output in section 3.2, voltage-input voltage-output in section 3.3, current-input voltage out in section 3.4, and voltage-input current-output in section 3.5. For each kind of binary hysteresis circuit, both forward and reverse hysteresis have been achieved. The complete independant control on the position (u_C, H_C), the width u_W, and the height H_H of each hysteresis was realized by either external current sources or external voltage sources. All eight CMOS binary hysteresis circuit operate in all four quadrants. The detailed discussions on these CMOS binary hysteresis circuits are given in Chapter three.

Thirdly, in Chapter four, CMOS circuits, to be combined with the CMOS binary hysteresis circuits, that are also building blocks for multi-cell hysteresis are designed. These circuits include analogue four-quadrant adders in section 4.2, ana-

logue four-quadrant multipliers in section 4.3, in both current and voltage mode, current-voltage converters in section 4.4, and voltage-current converters in section 4.4. The detailed discussions on the above circuits are given in Chapter four.

Fourthly, in Chapter five, CMOS circuits to give various multi-level hysteresis, in both current mode and voltage mode, have been achieved in section 5.3. Furthermore, CMOS circuits to give multi-level multi-cell hysteresis, in both current mode and voltage mode, have been achieved, in section 5.4. Further discussion on how to extend the results to higher dimensions was also given in section 5.5.

Finally, multi-cell hysteresis was suggested to be used in chaotic signal generation, as is covered in section 5.6 of Chapter five.

6.2 Open Problems

6.2.1 More on Binary Hysteresis

Looking back at binary hysteresis, in all the early discussions, we categorized them in two groups, based on the switching characteristics, as shown in Figure 6.1 (a) and Figure 6.1 (b), notice that here we rename the forward hysteresis described in the previous chapters to forward DU (down up) with $u_{H2L} < u_{L2H}$, and reverse one to reverse UD (up down) with $u_{L2H} < u_{H2L}$. Mathematically speaking, the limits on u_{H2L} and u_{L2H} need not be there. The other cases, as shown in Figure 6.1 (c) and Figure 6.1 (d), are also mathematically valid. The question is can we build CMOS circuits to realize them? This would also be for the future interest.

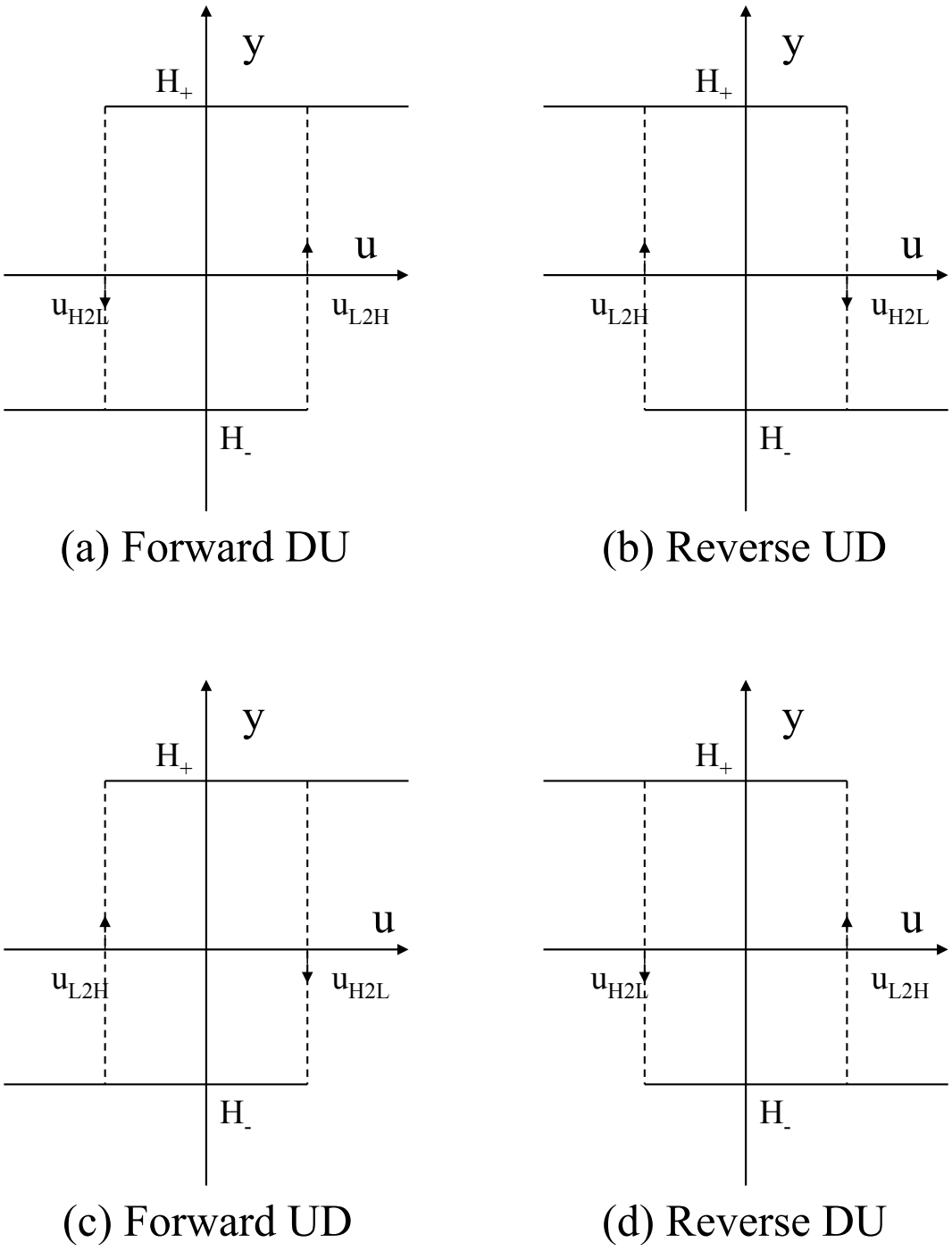

Figure 6.1: Binary hysteresis (a) Forward DU (down up). (b) Reverse UD (up down). (c) Forward UD (up down). (d) Reverse DU (down up).

6.2.2 Multi-Cell Hysteresis In Neural Networks

The key features of neural networks, that include asynchronous parallel processing, continuous-time dynamics and global interaction of network elements excite great interest and lead to a number of open problems.

6.2.2.1 CNN: Cellular Neural Network

A new circuit architecture for a type of neural network was proposed by L. O. Chua and L. Yang [11]. The new architecture was given the name of cellular neural network (CNN). The basic unit of a cellular network, a cell, contains some linear and nonlinear circuit elements. In a cellular neural network, a cell is only connected with its neighbors. A two-dimensional cellular neural network is shown in Figure 6.2.

The state equation for a typical $M \times N$ cellular network is given in Equation (6.1), for $1 \leq i \leq M,\ 1 \leq j \leq N$. x_{ij} is the state, u_{ij} is the input, $A(i,j,k,l)$ is the feedback operator taking output from nearby cells, $B(i,j,k,l)$ the input control operator, and I the threshold value, all with the defining neighbors, $N_r(i,j)$. The output $y_{ij}(t)$ is given by Equation (6.2), with $f(x)$ normally a single input single output nonlinear function. Multi-level hysteresis was proposed to be the nonlinear function $f(x)$ in gray scale image-processing for its robustness to noise [68].

$$\frac{dx_{ij}(t)}{dt} = -\tau_{ij}x_{ij}(t) + \sum_{C(k,l)\in N_r(i,j)} A(i,j,k,l)y_{kl}(t) + \sum_{C(k,l)\in N_r(i,j)} B(i,j,k,l)u_{kl} + I \tag{6.1}$$

$$y_{ij}(t) = f\left(x_{ij}(t)\right) \tag{6.2}$$

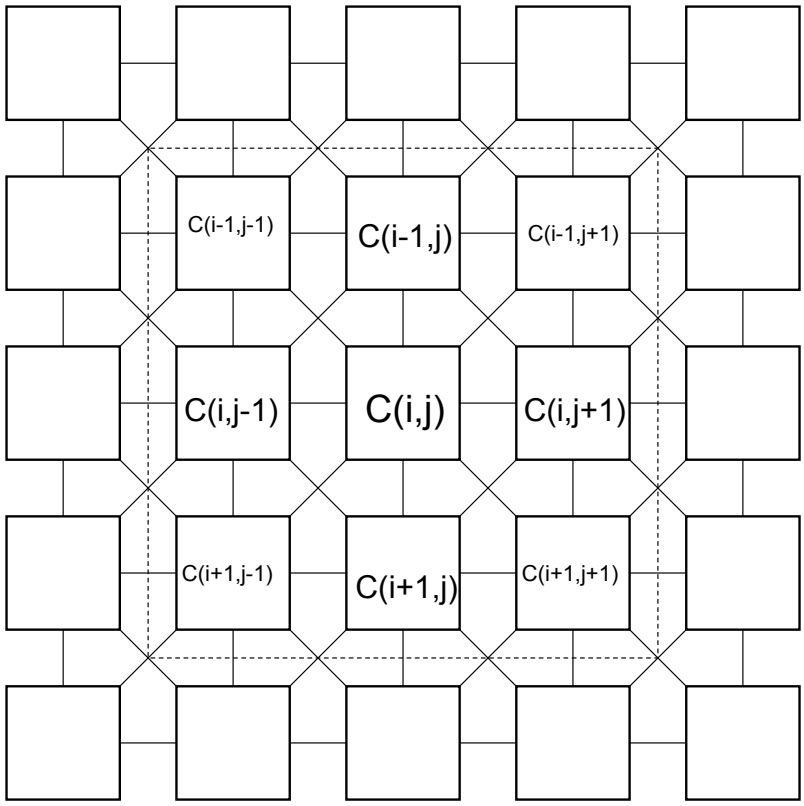

Figure 6.2: A two-dimensional cellular neural network. The links between cells represent the interaction between cells. The links are different in each case of definition of neighbors.

Since a cellular neural network is a multi-dimensional neural network, it is natural to consider using vectors as state variables to each cell, instead of a scalar $x_{ij}(t)$. Using the $M \times N$ two-dimensional cellular neural network as an example, the state variable for cell $C(i,j)$ can be defined as $[x^1_{ij}(t), x^2_{ij}(t)]$ and the state equations of such a neural network are given by Equations (6.3) and (6.4), for $1 \leq i \leq M,\ 1 \leq j \leq N$. The output of cell $C(i,j)$, y_{ij}, is given by Equation (6.5), with $H\left(x^1_{ij}(t), x^2_{ij}(t)\right)$ being the two-dimensional hysteresis function.

$$\frac{dx^1_{ij}(t)}{dt} = -\tau_{ij}x^1_{ij}(t) + \sum_{C(k,l)\in N_r(i,j)} A(i,j,k,l)y_{kl}(t) + \sum_{C(k,l)\in N_r(i,j)} B(i,j,k,l)u_{kl} + I \tag{6.3}$$

$$\frac{dx^2_{ij}(t)}{dt} = -\tau_{ij}x^2_{ij}(t) + \sum_{C(k,l)\in N_r(i,j)} A(i,j,k,l)y_{kl}(t) + \sum_{C(k,l)\in N_r(i,j)} B(i,j,k,l)u_{kl} + I \tag{6.4}$$

$$y_{ij}(t) = H\left(x^1_{ij}(t), x^2_{ij}(t)\right) \tag{6.5}$$

Another way to apply multi-cell hysteresis is that instead of using a one-dimensional nonlinear function $f(x)$, in Equation (6.2), multi-dimensional multi-level hysteresis is used here, as shown in Equation (6.6). H is a multi-dimensional hysteresis function with the states of cell $C(i,j)$ and its neighboring cells as the multi-dimensional input. This new cellular neural network can be described by state equation, as shown in Equation (6.7).

$$y_{ij}(t) = H(x_{kl}(t)), \text{ with } x(k,l) \text{ the states of } C(i,j) \text{ and its neighbors} \tag{6.6}$$

$$\frac{dx_{ij}(t)}{dt} = -\tau_{ij}x_{ij}(t) + y_{ij}(t) + \sum_{C(k,l)\in N_r(i,j)} B(i,j,k,l)u_{kl} + I \tag{6.7}$$

This is still in the very early stage of consideration of applying multi-dimensional hysteresis to cellular neural networks and is a topic worthy of future consideration.

6.2.2.2 Radial Basis Function Neural Network

Radial basis function (RBF) neural networks also have our eyes for applying multi-dimensional hysteresis cells also. RBF neural networks were developed by D. S. Broomhead and D. Lowe [4] and T. Poggio and G. Girosi [43]. A radial basis function (RBF) neural network can be described by Equation (6.8), with N as the number of neurons. $S_i(X_i)$ is a radial based function.

$$f_{nn}(X) = \sum_{i=1}^{N} w_i S_i(X_i) \tag{6.8}$$

Radial basis functions have their origins in the study of multivariable approximation theory. It was proven [44] [47] that a RBF neural network, with sufficiently large number of nodes and appropriately placed node center and variances, can approximate any continuous function. A Gaussian radial basis function is expressed by Equation (6.9), with $X = [x_1, x_2, ..., x_Q]$ the Q-dimensional input, $\xi = [\xi_1, \xi_2, ..., \xi_Q]$ the center, and η the width.

$$S(X) = exp\left(\frac{-\|X - \xi\|}{\eta^2}\right) \tag{6.9}$$

Three dimensional plots of two-dimensional input radial basis functions are shown in Figure 6.9.

Gaussian radial basis functions are localized basis function, meaning that each function can only affect the network output locally. This property, with the function approximation ability, was used in localized representation, storage and learning [58].

The question is that "can we replace the radial basis function in RBF neural network by multi-dimensional hysteresis function to approximate any multi-

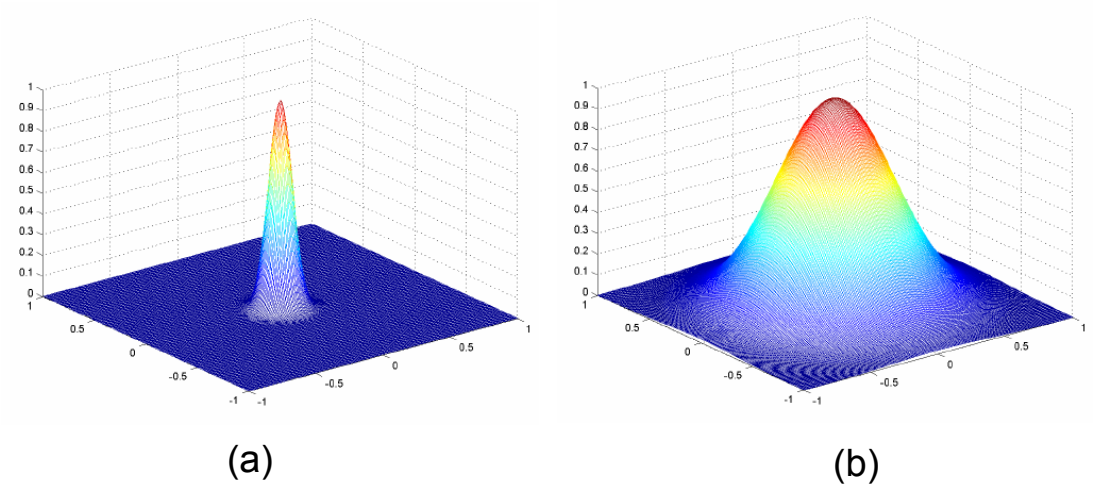

Figure 6.3: Radial basis functions with different width η. (a) $\eta = 0.1$. (b) $\eta = 0.5$.

dimensional hysteresis function? " How can we do it? This is also worthy of consideration of future work.

Since multi-dimensional multi-level hysteresis is a new concept, applying it to neural networks is in the early stage of consideration. Further investigation on applying multi-cell hysteresis is encouraged.

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