ABSTRACT

Title of Dissertation: EFFECT OF DYNAMIC FLEXURAL LOADING ON THE DURABILITY AND FAILURE SITE OF SOLDER INTECONNECTS IN PRINTED WIRING ASSEMBLIES

Joseph Varghese, Doctor of Philosophy, 2007

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This dissertation investigates the durability of solder interconnects of area array packages mounted on Printed Wiring Assemblies (PWAs) subjected to dynamic flexural loads, using a combination of testing, empirical curve fitting and mechanistic modeling.

Dynamic 4-point bend tests are conducted on a drop tower and with an impact pendulum. Failure data is collected and an empirical rate-dependent durability model, based on mechanistic considerations, is developed to estimate the fatigue failure envelopes of the solder, as a function of solder strain and strain-rate. The solder plastic strain histories are obtained from the PWA flexural strain and strain rate, using transfer

functions developed from 3D transient Finite Element Analysis (FEA) with rate-dependent solder material properties. The test data also shows the existence of multiple competing failure sites: solder, copper trace, PWB under solder pads, and layers of intermetallic compound (IMC) between the solder and solder pads. The failures in the IMC layers are found to be either in the bulk of the IMC layers or at the interface between different species of IMC layers. The dominant failure site is found to be strongly dependent on the loading conditions. The empirical model is demonstrated for solder failures as well as Cu trace failures, and the transition between their competing failure envelopes is identified.

This dissertation then focuses in detail on two of these competing failure sites: (i) the solder and (ii) the interface between two IMC layers. A strain-range fatigue damage model, based on strain-rate hardening and exhaustion of ductility, is used to quantify the durability and estimate the fatigue constants of the solder for high strain rates of loading. Interfacial fracture mechanics is used to estimate the damage accumulation rates at the IMC interface.

The IMC failure model and the solder failure model provide a mechanistic perspective on the failure site transitions. Durability metrics, based on the mechanics of these two failure mechanisms, are used to quantify the competing damage accumulation rates at the two failure sites for a given loading condition. The results not only identify which failure site dominates but also provide estimate of the durability of the solder interconnect. The test data shows good correlation with the model predictions.

The test vehicles used in this study consist of PWAs with Sn37Pb solder interconnects. But the proposed test methodologies and mechanistic models are generic

enough to be easily extended to other emerging lead free solder materials. Wherever possible, suggestions are provided for the development of test techniques or phenomenological models which can be used for engineering applications.

A methodology is proposed in the appendix to implement the findings of this thesis in real-world applications. Damage in the solder interconnect is quantified in terms of generic empirical metrics, PWA flexural strain and strain rate. It is shown that the proposed metrics (PWA strain and strain rate) can quantify the durability of the solder interconnect, irrespective of the loading orientation or the PWA boundary conditions.

EFFECT OF DYNAMIC FLEXURAL LOADING ON THE DURABILITY AND FAILURE SITE OF SOLDER INTECONNECTS OF PRINTED WIRING ASSEMBLIES

by

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When I first came to College Park, I did not want to do a PhD. The plan was to get out with a Masters, find a good job, and buy a BMW. I have been here a long time, and the last few years have been the most intellectually rewarding period of my life.

No one deserves more credit for shaping my years in UMD other than Prof. Abhijit Dasgupta, a scholar and a gentleman. The more I sink into the real world, the more I realize the importance of his actions.

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Chapter 1: Introduction

Dynamic loading plays a crucial role in the performance and reliability of electronic devices. Portable electronic devices are often subjected to transient loads and vibration loading due to drop events during mechanical handling, accidental misuse, or shipping (transportation). Hence, they need to be rugged and sufficiently shock resistant. Furthermore, these products are typically densely packed with electrical and electromechanical components, have complex displays, heavy batteries, and are housed in thin-walled plastic cases. Many of the design features to reduce their weight and size, makes them susceptible to shock induced failure. Examples of such products include cell phones, laptops, Portable Digital Assistants (PDA), pagers, hand-held gaming products and portable audio-video entertainment devices.

A common cause of failure in portable electronics is accidental drop by the user. Military applications often generate repetitive shocks (artillery fire), sudden high G loading (launching or maneuvering), or ballistic impact. The final product has to be designed and tested for drop/shock loading in these environments. The main reliability challenges are usually mechanical failures like dislodging of the batteries, disengaging of the snap fits, contact damage in the casing, cracking of the Liquid Crystal Display (LCD), and fatigue of the electrical connections in the Printed Wiring Assembly (PWA), to name a few. Of all the potential failure sites in the product, this dissertation focuses on PWA failure, specifically in the solder interconnect between the component and the board.

The PWA is connected to the housing of the product by using fasteners like screws, spring clips, etc. When the product is dropped, the PWA acts like a plate subjected to an acceleration pulse at the base. As expected, the structural response of the PWA depends

on the distribution of components on the board, the boundary conditions imposed by the fasteners that connect the board to the product casing, and the drop orientation. The durability of solder interconnects of the components mounted on the PWA depends on this structural response.

Area-array components, like Ball Grid Arrays (BGAs), are increasingly being used in portable devices because of their ability to accommodate a large number of I/Os for a given footprint. A substrate is used to redistribute the very fine pitch (as small as 0.075 mm) peripheral pads on the chip to much larger pitch (1mm, 0.75mm and 0.5mm) area-array pads on the board [1]. As shown in the figure below, the die is attached with an adhesive to this substrate. The demand for increased device functionality has led to BGA designs with interconnects of finer pitch, which thereby shrinks the package dimensions. Hence the size of the solder interconnects is getting smaller, which can make it more sensitive to stresses induced by dynamic flexure of the PWA. One of the most common failure sites due to dynamic loading of electronic products is in the surface mount solder interconnect between the board and the substrate of the component, commonly referred to as the second level interconnects. Researchers are trying to develop techniques to characterize, quantify, and predict the durability of the solder interconnect at high strain rates of loading.

What complicates the process of developing a generic test technique to quantify solder interconnect durability is the presence of competing failure sites. Researchers have reported multiple failure sites in the solder interconnect, depending on the solder type, plating material, specimen geometry and loading conditions [2-4]. For example: it was shown that interconnects with Electroless Nickel Immersion Gold (ENIG) finish have a

tendency to fail either in the solder or the intermetallic layer at the solder – copper pad interface during drop test conditions, while those with Organic Solderability Preservative (OSP) finish tend to fail either in the solder or in the PWB/ copper trace (). Thermal aging, which changes the microstructure of Sn37Pb solders and the morphology of the intermetallic layer, was also found to affect the location of the failure site. Each failure site has a characteristic failure mechanism, and hence, a different influence on interconnect durability. The complex interactions between the competing failure mechanisms, especially under different conditions of high strain-rate mechanical loading and thermal aging, have not yet been fully understood by the microelectronics reliability community.

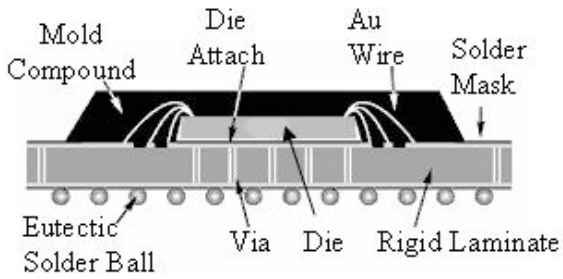

Figure 1-1: Schematic of a typical Ball Grid Array. Source: www.practicalcomponents.com

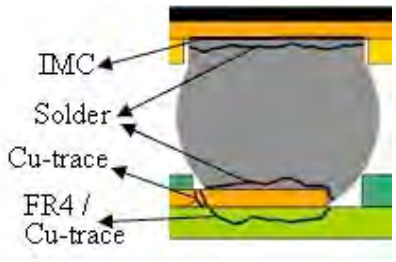

Figure 1-2: Competing failure sites in the solder interconnect[5]

In summary, there is tremendous interest in extending the current state-of-art to quantify the durability and understand failure site transitions in the PWAs under drop testing conditions, for three reasons:

1. Existing testing methodologies do not provide adequate insight into the physics of the failure of the interconnect; and although useful from a statistical comparative perspective, have limited validity because they are conducted at the system level and they treat the test specimen as a "black-box". For example, durability is generally quantified in terms of number of drops to failure, without conducting any analysis of the modal response of the board, location of component on the PWA, post-impact vibration, location of failure site, stresses at the failure site, etc.
2. There is a need for a systematic methodology, either empirical or mechanistic, to characterize the observed failure site transition from the solder to other parts of the PWA.
3. Conducting drop tests on full products is a very costly and time-consuming process, and the results are very difficult to post-process. There is a need for a quicker, cheaper technique to replicate the loading experienced by the PWA during assembly and field conditions.

This dissertation presents a detailed study to characterize the drop durability of the solder interconnects in the PWA. The durability and failure site are characterized as a function of the load amplitude and loading rate (individually or combined). This study also shows that PWA flexural strain and strain rate can be used as empirical durability metrics for any drop orientation and PWA boundary condition. An empirical Failure Site Transition Zone (FSTZ) is characterized on the basis of the proposed durability metrics, to identify the transitions between competing failure mechanisms like solder fatigue and copper trace fatigue. Furthermore, detailed mechanistic analysis is conducted to provide insights into the failure site transition from the ductile solder to the brittle interface

between two IMC layers. Insights are developed to explain the complex interactions between the solder and the intermetallic layer. Durability and the failure site of the solder interconnect is characterized in terms of both the empirical and mechanistic parameters.

1.1. Problem Statement

The problem statement of this study is to understand the interactions between the solder and the intermetallic layer, in order to predict the durability and the failure site in surface mount interconnects during drop testing of the PWA. The focus of this study is limited to two common failure sites: the bulk of the solder joint and the interface between the two IMC layers at the interface between the solder and the bond pad. To conduct this analysis, the two competing failure modes in the interconnect and their respective root causes must be quantified. This raises a range of issues, listed below, that must be resolved before the stated problem statement can be addressed.

1. The prevalent metric used to characterize drop durability is number of drops from a given height. Unfortunately, this metric is specific to the geometry of the PWA, orientation of drop, and boundary conditions of the PWA; and cannot be easily extrapolated or generalized to other architectures and loading configurations. *Generic damage metrics* that can quantify the durability, without being influenced strongly by the test setup or the specimen configuration, need to be identified. Furthermore, these metrics should serve as assessing parameters to capture the transition of failure sites during different loading conditions.

2. A test setup has to be developed to help researchers understand the individual and combined effects of loading amplitude and loading rate on the interconnect. The design, fabrication, and instrumentation of an experimental setup for repeatable and

accurate testing at high loading rates can be quite challenging. Failure monitoring is an additional challenge because the interconnect fracture during drop testing may last only for a few microseconds before the crack closes up again.

3. Limited work has been done to characterize the failure site transitions or to understand the complex interactions between the solder and the intermetallic layer. Mechanistic parameters that can capture the physics of the problem, and are independent of loading condition and specimen geometry must be identified.

4. A model must be developed using numerical and/or analytical techniques, to quantitatively explain the experimental results published in this thesis and other related experimental results published in the literature.

1.2. Background and Motivation

In general, drop testing is expensive and time-consuming, requiring much manpower in measurement and failure analysis. At present, manufacturers of electronic devices use the JESD22-B104-B standard for mechanical shock [6] to quantify reliability of the portable electronic product by the number of drops to failure. The electronic product is held in the desired orientation and attached to a drop carriage that is allowed to fall. The product is released just before it hits the ground to allow it to execute its natural rigid body motion and structural dynamics. But even a single drop event of an electronic product can produce a complex load history [7]. The structural response of the PWA is strongly dependent on the mass distribution of the internal electronics and the orientation of drop [8]. Hence, characterizing the drop durability of the interconnect by running tests or simulations at the product level is a very complex task. Drop testing the PWA is an

easier solution to the same problem.

Board level tests are usually conducted on a Sub-assembly Drop Testing Machine based on the JEDEC JESD22-B111 Standards [9]. The PWA is screwed on to a drop carriage in the horizontal position at four or six points and dropped from different drop heights. Instrumentation includes accelerometers on the drop carriage, strain gages on the PWA and a high speed failure monitoring system. The drop durability is quantified in terms of the number of drops to failure. There are some issues with the existing technique that necessitate the development of an alternate test technique. These are briefly discussed below. A detailed description of these limitations is presented in the next chapter (Chapter 2)

The durability of the solder interconnects is dependent on a variety of parameters: mass distribution in the PWA, drop height, dynamic material properties of the structure, boundary conditions, etc. The failed interconnect is usually in the outermost row of the ball grid array, implying that failure is driven by flexure of the PWA [10]. So far, researchers have developed an understanding damage accumulation in the interconnect, while focusing on a *single* failure mechanism. Researchers have also begun to explore the individual contributions of loading amplitude and rate on interconnect durability. The current state-of-art can be extended by characterizing and analyzing the effect of competing failure modes, under various dynamic loading conditions.

For a given interconnect, the potential failure mechanisms are bond pad lift-off, copper trace failure, fracture of the brittle intermetallic and fatigue failure of the ductile solder. Tests indicate that the failure site within the interconnect changes from solder ball to intermetallic or bond pad as the drop height increases [11]. Limited work has been

done to understand the strain rate dependent transitions between these failure sites.

Existing durability estimation models for drop testing are not generic in nature and are specific to the package mass, package design, and orientation. The parameters used to quantify durability (plastic strain or peeling stress) are based on bulk solder material properties, even though test data indicates that the failure site is not the solder ball [12]. This is primarily due to the fact that the damage constants are unknown for the other failure sites.

Another factor that is getting increased attention is the transition to lead free solders. The behavior of lead free interconnects under vibration/shock loading conditions is largely unknown. The dynamic properties of many lead free solders are still being determined. Limited drop test results are available to compare the drop durability of leaded solders and Pb-free solders. The empirical design rules for leaded solders may be no longer suitable for those with lead-free solders. As a consequence, establishing new design rules for Pb-free packages for drop durability has become an important topic in the electronic packaging industry.

With this motivation, this dissertation aims at addressing the above issues by providing generic empirical metrics to quantify durability and failure site, irrespective of boundary conditions, and drop orientation, but dependent on the PWA geometry. The proposed empirical metrics have further been applied to Pb-free and SnPb solder systems, in the as-reflowed and aged conditions, to provide a quantitative comparison of the durability under dynamic loading conditions, which are still not well-documented in literature. 3D transient Finite Element Analysis (FEA) has been used to extract empirical fatigue constants of the solders from high strain-rate tests. Furthermore, interfacial

fracture mechanics has also been used to provide a mechanistic insight into two competing failure sites: solder and the interface between the two IMC layers

1.3. Approach

Accelerated reliability tests are used for conducting this study and correlating the laboratory and field loading conditions. A high-speed four point bend tester, built in-house, is used to characterize the durability and the failure site transitions. A high speed data acquisition and resistance monitoring system is used to monitor failure in the solder interconnect. The test coupons used in this dissertation have very simple designs to allow in-depth analysis with minimum complexity. All test coupons used for in-depth analysis have Sn37Pb BGA components mounted on the board. *Eutectic Sn37Pb has been chosen as the solder material because its dynamic properties have been well characterized and documented in literature.* Interfacial fracture mechanics, using linear elastic material properties, is used to develop a qualitative understanding of the failure site transitions within the solder interconnect. 3D transient finite element analysis, with rate-dependent solder material properties are combined with the interfacial fracture mechanics model to estimate the strain energy release rate of the non-planar interface within the IMC layer. The results of the analysis are used to provide insights into the failure site transition and the durability of the interconnect. This is compared with experimental results to verify the hypothesis made in the analysis.

1.4. Overview of the Thesis

This thesis includes manuscripts that have been either published in, or accepted by, or submitted to scholarly journals. An exhaustive literature review about durability

assessment and failure site transitions in the solder interconnects of PWAs is presented in Chapter 2. The test setup, instrumentation and failure monitoring schemes are discussed in detail in Chapter 3. PWA flexural strain and strain rate are used as empirical durability metrics to quantify the durability of the solder interconnects of a PWA supported in the four point bend configuration and subjected to out-of-plane bending. A "Failure Map" is developed, in terms of PWA strain and strain rate, to plot the dynamic fatigue failure envelopes of the solder and identify the FSTZ. 3D transient FEA is used to understand the behavior of the solder at different loading conditions, and to determine the empirical fatigue constants for cyclic loading of the solder at high strain rates. Chapter 4 introduces a mechanistic model to understand individual and combined effects of load and loading rate on the failure of the solder. A new damage metric is proposed to quantify rate-dependent durability of the solder. Chapter 5 characterizes failure in the interface between the IMC layers of the solder interconnect. FEA is used to conduct stress analysis at the macroscopic level and interfacial fracture mechanics is used at the microscopic level. Chapter 6 introduces a technique to predict the durability and failure site of solder interconnects of PWAs subjected to dynamic flexural loading. The proposed technique draws on the mechanistic models developed in Chapters 4 and 5. The predicted durability and failure site show good correlation with experimental data.

Chapter 2: Literature Review

This chapter starts by reviewing existing techniques to estimate the durability of portable electronic products subjected to drop tests. This is followed by a discussion of the drawbacks of these test methods specific to quantifying solder interconnect durability. Board level drop testing is then reviewed extensively, with a focus on the test technique and failure site transitions induced by loading rate and thermal aging. FEA simulation of board level drops and proposed durability models are also reviewed. Since this dissertation studies failure site transition from the solder to the interface between the IMC layers, a literature review of dynamic testing of individual solder interconnects is also conducted. The test techniques and failure envelopes used to characterize failure in the intermetallic layer of the solder interconnect are reviewed. The drawbacks of the existing state-of-art and the need for a new study to characterize durability and failure site transitions are then presented.

The problem of understanding the response of a structure to shock/vibration loading is not completely unknown. Much work has been done to understand the structural response during missile launch/gun fire [13, 14], occupant safety during vehicle collisions [15, 16], durability of casks under drop test conditions [17], random vibration induced fatigue of aircraft parts [18], dynamic response of human beings during road/rail transportation [19], etc. As described later on in this thesis, some of the tools used for analysis in the situations mentioned above have been implemented or modified in this study.

2.1. Product Level Drop Testing

At present, the trend among electronics manufacturers is to use the JEDEC JESD22-B104-B standard [6] to quantify reliability of the portable electronic product by the number of drops to failure. The electronic product is held in the desired orientation and attached to a drop carriage that is allowed to fall. The product is released from the drop carriage just before it hits the impact surface. This allows control of drop orientation before impact and also allows the electronic product to undergo its natural dynamic response after impact. Goyal, et al. [7, 20] used strings to control the orientation, while Lim, et al. [8] and Seah, et al. [21] used a gripper style mechanism. A load cell is used to determine the impact force. The drop carriage and the electronic product usually have accelerometers and/or strain gages on them. The drop event is usually recorded with a high speed camera to verify repeatability of orientation of impact. Published literature shows that a variety of failure sites and modes are possible for a given product level drop test. This includes cracking of the LCD screen, detachment of the battery case, damage in the plastic housing, etc. This study, and hence the literature review, focuses on solder interconnect failure in the area array components mounted on the PWA, inside the product.

A single drop event of an electronic device can produce a complex load history due to “clattering”. Goyal, et al. [7, 22] used high-speed photography to show that during a single drop, one corner of the electronic product usually touches down first and there is “clattering” as other corners strike repeatedly due to rebounds. During “clattering”, the product can experience extremely high net velocity changes at each impact, thus inducing velocity shocks. Clattering of the product can also lead to alternating shocks that could

cause resonance in suspended fragile components. Goyal, et al. [23, 24] also showed that the shock response of the electronic product is dependent on its mass distribution. Shock Response Spectrum (SRS) was used to correlate product response to the incident shock pulse and the natural frequency of the internal electronics and to define damage conditions in the suspended sub-assemblies by checking if the peak acceleration or peak displacement exceeded some critical value.

Work has also been done to characterize the drop durability of electronic products and sub-assemblies using dynamic 3D FEA. Low [25] simulated the drop an electronic product surrounded by a cushion buffer and showed that the cushion reduces the magnitude of the impact load. Hua, et al. [26] simulated the drop of a spindle fixation subassembly of an electronic product at various impact velocities and orientations to determine the G levels at which the spindle will fail. Similar work has been done to characterize the impact force and drop response of 2 way radios [26], cell phones [26, 27] and audio systems [28]. Thus, it is very common to use FEA to identify the failure-prone zones in a portable product, or to identify critical values of the loading conditions under which the product may fail.

Characterizing the drop durability of the interconnects by running tests or simulations at the product level is a very complex task. When a portable electronic device is dropped, part of the kinetic energy goes into the rigid body motion during rebound, part goes into the strain energy of deformation of the internal electronics and external housing, and the rest is lost to damping and friction. Only a portion of the energy absorbed by the internal electronics ends up causing damage to the interconnects. The amount of energy responsible for deformation of the interconnect depends on the loading

conditions, boundary conditions, component architecture, housing structure, and materials. This was verified during drop tests conducted by Lim, et al. [8, 29] and Seah, et al. [21] that showed that the strains and accelerations in the PWA varied with the electronic device for the same orientation of drop, and varied with orientation for each device of the PWA. Even if the test condition is kept constant, the contact damage in the outer surface of the product will change the dynamics of the PWA inside the housing. No study has been conducted so far to quantify the effect of contact damage in the housing on the internal behavior of the durability of the product.

It is therefore not possible to create a *generic* test specification for drop durability of surface mount interconnects, which is based on the incident kinetic energy of drop or shock response spectrum damage estimation criteria. Instead, it is better to relate the damage in the interconnects to the local response close to the failure site. This relationship is less dependent on the incident kinetic energy, boundary conditions, mass distribution and orientation of drop.

Board level testing can be used to develop the failure envelopes for the characteristic damage causing mechanisms in the surface mount interconnects. From an industry perspective, testing the drop durability of the interconnect at the board level is easier and can be done by the OEM. However, this does not mean that product level drop testing can be neglected. Experimental work [30] indicates that constraining a sub-assembly to behave as a single system and not allowing natural motion of the product during drop testing can lead to underestimating the damage potential of the drop and may even miss important failure mechanisms. This is explained in detail in the following sections.

2.2. Board Level Drop Testing

JEDEC standards are generally used by the portable electronics industry to quantify PWA durability. While following the existing standard has its own advantages, it is also a black box technique which offers no insight into the physics of the drop event. This has motivated many researchers to develop alternate techniques to quantify drop durability and understand the phenomenon. This section begins with a review of all the test setups developed to understand the behavior of solder interconnects at high loading rates, including the JEDEC board level drop tester. The experimental data and FEA simulations are then discussed to show the effect of material properties, loading rate and other parameters on the durability and the failure site of the interconnect. The section ends with a review of damage metrics that have been proposed by various researchers.

2.2.1 Test Methods

Board level tests are usually conducted on a Sub-assembly Drop Testing Machine based on the JEDEC Standards [9]. The PWA is mounted on to the drop carriage in the horizontal position at four or six points. The drop carriage falls along two guide rods on to stationary stops, and induces out of plane displacement in the PWA on impact. The impact surface can be changed to vary the profile of the impact force. On impact, the PWA responds to the transient impact force applied to the base and then vibrates at its natural frequency. Instrumentation includes accelerometers on the drop carriage, strain gages on the PWA and a high speed failure monitoring system. The metric for characterizing durability is the number of drops to failure.

The amplitude of the shock pulse depends on the height of the drop, but the

duration of the pulse is strongly influenced by the material properties of the impact surface and the fixture. As explained by Wong, et al [31], the duration of the shock pulse during the drop test depends on the time it takes for the stress waves to bounce from the free end and come back as tensile waves. Part of the compressive wave goes into the standoffs and gets converted from longitudinal waves to flexural waves in the PWA. The maximum acceleration is at the clamped ends of the PWA because that is directly connected to the drop fixture that experiences extremely high acceleration as it is stopped during drop. The highest acceleration is at time of impact and the other acceleration spikes are after a certain time gap depending on how much time it takes for the flexural wave to reach the center of the board. The wave at the center has lower amplitude and higher time period due to the damping of the wave.

The dynamic response of the PWA to drop tests conducted according to the JESD22-B104-B standards can vary depending on the robustness of the test setup. Jing-en, et al. [32] conducted JEDEC board level drop tests on PWAs populated with TFPBGA packages facing downwards. Accelerometers were attached on the fixture and the center of the PWA to measure the impact acceleration and the board response, respectively. Strain gages were also attached to the PWA, on the opposite side of the component. Fourier transforms of the data obtained from strain gages showed that the fundamental frequency of vibration varied with the tightness of the screw holding the PWA to the fixture. As the number of drops increases, the screw tends to loosen, leading to a phase lag in the PWA response. Wearing out of the impact surface after repeated drops can change the coefficient of restitution, thus changing the nature of the input acceleration pulse. Similar drop tests were also conducted by Wang, et al. [33] on PWAs

clamped at both edges, mounted with flip-chips of different sizes, with and without underfill. The drop height was maintained as 1 meter to obtain an input acceleration of about 1000 Gs. The PWA was instrumented with an accelerometer and strain gages and a high speed camera was used to measure the board displacement. These tests too, showed that the dynamic response of the PWA was strongly dependent on the impact surface. Thus, the same drop height may induce different levels of damage in the PWA. A source of testing variability that has not been studied so far is the change in the boundary condition due to damage in the PWA, near the mounting screws on the JEDEC fixture.

Alternate techniques have also been proposed to quantify the durability of PWAs under dynamic loading conditions. This study used a pendulum style test setup [10] to impact a constrained PWA in the in-plane and out-of-plane orientations. The kinetic energy of impact was varied by changing the mass of the steel sphere and/or the impact velocity. The impact velocity was varied by changing the pendulum release height. For out-of-plane impact, the specimen was oriented vertically and clamped at its four corners. For in-plane impact, the specimen was oriented horizontally and the two edges orthogonal to the impact axis are guided with leaf springs to remain in the impact plane. Horizontal motion of the impacted edge led to bending of the specimen. The PWA was instrumented with strain gages mounted near the edge of the component and a high speed failure monitoring system. Durability was quantified in terms of PWA strain obtained from the strain gage under the assumption that the effect of the boundary conditions is negligible.

The assumption made in this study about the boundary conditions may not be valid all the time. Fong Kuan, et al. [34] placed strain gages on one side of a JEDEC standard

PWA to correlate local PWA strains to solder joint durability. For a given loading condition and location on the PWA, the strain gages showed higher strains for the 6 screw configuration than for the 4 screw configuration. This is because the strains measured on one side of the board are affected by the in-plane strains induced by the clamped boundary condition of the board and by the flexural strains due to the curvature of the board. Solder durability is a function of PWA flexure, and due care must be taken to eliminate the effect of boundary conditions from the strain gage data. This can be remedied by using strain gages on both sides of the PWA at the same location to eliminate the effect of the boundary conditions, or by using simply supported boundary conditions.

Lall, et al [35] also developed an in-plane drop test method for PWAs. A glass tube with a diameter that is equal to the board edge length was used to guide the drop. High speed imaging was used to track the post-impact deflections of the PWA. Repeatability was measured by tracking the angle of the PWA before and after impact. Durability was quantified in terms of number of drops to failure.

In spite of the work done by the researchers mentioned above, there was a growing need to develop a new technique due to two reasons:

1. To understand the factors that affect drop durability, one needs to be able to closely control the input loading conditions. This includes the amplitude and rate of loading. This is not possible with the test setups mentioned above.
2. A variety of Pb-free solders are available that can replace SnPb solders. A variety of material combinations in terms of solder alloys and pad finishes are possible. The reliability of each material combination will be different and the test setups

mentioned above are very time and labor intensive.

For most plastic encapsulated microelectronic systems, the mass of the component is very small. Dynamic flexural tests to replace conventional drop/impact tests were developed after Wong, et al. [36] proved experimentally that damage to the solder due to component inertia is negligible when compared that due to PWA curvature. They conducted drop tests on PWAs that were constrained from flexing so that the only failure driver was component inertia. The acceleration pulse due to drop was as high as 3000 Gs with a time period of 0.5 milliseconds. An additional mass was attached to the component to increase its inertia. The PWA did not show any failure, even with such high component inertia, thus leading to the conclusion that PWA flexure is the dominant parameter that drives solder interconnect failure. Hence, the effect of component inertia on solder durability can be neglected.

Motivated by the work done above, this study used high-speed four point bend testing to quantify drop durability [37]. A commercially available servo-hydraulic test machine was used at low loading rates. High loading rates were achieved by using a modified drop tower to drop steel spheres on a fixture holding the specimen in a four-point configuration. The PWA was instrumented with strain gages and a high speed failure monitoring system. The PWA was simply supported and not clamped so that the strain gage measured only the flexural strain. This allowed a direct correlation between the sensor data and durability, without any post-processing to remove the effect of clamped boundary conditions from the strain gage data. Durability was quantified in terms of PWA flexural strain and strain rate.

The post-impact strain response of a PWA experienced the first mode of vibration

resembles a damped sinusoidal wave. A conventional four point bend can induce cycling loading on a PWA, but can not capture the dynamic response of the PWA. Seah, et al. [38] developed a high-speed displacement-controlled bending machine where a cam was used to enforce a PWA strain profile that was similar to that seen during a JEDEC drop test. The PWA with a component at the center is clamped at four corners and attached to an anvil at the center, such that it resembles a four point bend setup. This leads to uniform bending moment around the component and a single rotation of the cam moves the anvil such that the PWA experiences a sinusoidal strain profile. Durability was quantified in terms of PWA strain, at different values of loading frequency. Reiff and Bradley [39] induced a similar type of damped sinusoid PWA response by conducting indirect impact tests. The PWA was clamped at the corners and loaded with an anvil in the region of interest. The anvil had had two knife edges that induced a four point bend condition. The mass was dropped from different heights on to the anvil. On impact, the PWA vibrated in its natural frequency and PWA strain was used as a metric to quantify durability.

Marjämaki, et al. [40] used vibration to understand drop behavior of PWAs. They compared the failure sites observed in PWA vibration and drop tests. Specimens with Cu/OSP and Ni/Au assemblies tested with 10 replications. Solder cracking was observed at low amplitude vibration. Failure site transition from solder to the intermetallic layer and FR4/Cu trace was observed with increase in vibration amplitude. Similar failure sites observed for both drop and large amplitude vibration.

2.2.2 Experimental Data

Tan, et al. [41] explored the effect of loading rate on the overstress failures of

solder interconnects. They conducted bend tests on PWAs mounted with Multi Chip Modules (MCMs) at displacement rates ranging from 0.1 mm/sec to 10 mm/sec and then drop tests from heights of 1 meter and 1.5 meters. As ramp rate increases, the deflection and load required for failure decreases. But at higher ramp rates, load and deflection don't follow the same trends. Graph of PWA strain vs time tapers off as deflection is increased due to the yielding of the solder ball, which reduces the board curvature. Visual inspection also showed that solder ball deformation decreases with increasing loading rates. The failure site during bend was in the solder, while the dominant failure modes in drop testing were bond-pad lift off and intermetallic fracture. Similar studies were also conducted by Geng, et al [42] on PWAs mounted with eutectic Sn-Pb solders. Three point bend tests were used to show that the solder failed at lesser board deflections as the displacement rates increased.

Yu, et al. [2] explored the effect of vibration mode shapes on the drop durability of PWAs. The test coupons were PWAs mounted with a single SnAgCu BGA component. The tests were conducted using a JEDEC style drop tester with a mass attached to the PWA, on the opposite side of the component. The location of the mass was varied to induce different mode shapes during the post-impact vibration of the PWA. As expected, drop tests conducted with the component and mass at the center of the board showed a decrease in durability with increasing drop height. For the same drop height, tests done with the mass and component at different locations showed a relative increase in durability when the chip is not at the location of the primary mode shape. They also noticed a change in the failure site from the bulk solder to the intermetallic layer with increasing drop height.

Jing-en, et al. [43] used JEDEC board drop tests to conduct a Design of Experiments (DOE) study on durability of Systems in Package (SiP) components. The test coupon had 12 BGA components: 6 on each side of the center line. The BGA components had different package sizes, ball layouts, package layouts and die thicknesses. The boards were supported at 4 points and failure site was found to be in the intermetallic layer of the outer most solder ball on the component side. The test data showed that durability decreases with increased solder ball height. Increase in diameter decreases durability because smaller solder balls are more compliant which reduces stress. However, when solder ball diameter is smaller than solder mask opening, the stress increases and durability is reduced. SnAgCu components were shown to have lower impact life than eutectic Sn-Pb components. This is because SnAgCu has a larger elastic modulus (46GPa) as compared to eutectic Sn-Pb (31.6GPa), so the stresses are higher. For the same distance of the outer perimeter from the neutral point, drop durability was shown to increase with increase in the number of solder ball perimeter rows. Similar DOE studies using JEDEC drop standards were conducted by Yu and Jin [44] to reduce the interfacial peeling stresses in Radio Frequency (RF) packages with Land Grid Array (LGA) solder interconnects. LS-Dyna was used to relate the loading conditions to the solder stresses.

Lee, et al [45] conducted board level drop tests to investigate the effect of different solder materials and peak reflow temperatures on the durability and failure site of the solder interconnects. The test coupon, a Plastic Ball Grid Array (PBGA) component mounted on a 6 layer FR4 board with ENIG surface finish, was allowed to fall on to a stainless steel plate in the in-plane direction. It was found that eutectic Sn-Pb solder joints

performed better than Pb-free solder joints. Three failure sites were observed: within the bulk solder, the interface of the solder joint and copper pad, and fracture of the copper trace near the pad-trace junction. Heaslip, et al. [46, 47] also compared the drop durability of Sn37Pb and Sn95.5Ag3.8Cu0.7 solders on JEDEC drop testers and showed that the failure sites and failure mechanisms change with drop height and solder type. Similarly, JEDEC level drop tests have been used to compare the durability of Pb-free solders with different compositions [48], different underfill materials [49], different solder finishes [50], etc.

The experimental work discussed above showed that both durability and failure site depends on a variety of parameters, including material properties and loading conditions. During the thesis work, Varghese and Dasgupta [4, 37] decoupled the effect of load amplitude and rate on the durability and the failure site by conducting high-speed bend tests on a PWA with a single SnPb/OSP BGA on it. They showed that there exists a FSTZ that can be characterized in terms of PWA strain and strain rate beyond which the failure site changed from solder to the FR4/Cu-pad. The developed technique was used in this study [11] to characterize the durability and failure site transitions for PWAs with SnPb/ENIG interconnects, where the failure site changed from the solder to the intermetallic layer. Resistance monitoring showed that crack propagation in the solder failure takes longer, while brittle failure in the intermetallic is instantaneous. Similar conclusions have been made by Seah, et al. [51] and Heaslip, et al. [47].

The sudden decrease in the durability due to the failure site transition prompted a study of how various solder and plating material combinations behave under dynamic loading conditions. Chong, et al. [52, 53] compared the drop durability of leaded and

lead free BGA components with OSP, immersion tin and ENIG surface finishes by conducted JEDEC drop tests of PWAs supported at its corners. SnPb solders were found to have better drop durability than Pb-free solders, irrespective of surface finish. For a given solder material, OSP finish provided better drop durability than the other pad finishes. The solder interconnect strength was ranked as SnPb/OSP > SnPb/ENIG > Pb-free/OSP > Pb-free/ENIG > Pb-free/Immersion tin. The failure site for ENIG-based components was the intermetallic layer and that for OSP-based components was FR4/copper trace. Chai, et al. [54] studied the effect of board design, failure mechanism and durability of Quad Flat Package (QFP) and Chip Scale Package (CSP) components subjected to JESD22-B111 drop tests. Components with ENIG surface finish showed less durability than OSP surface finish, especially when used with SnAgCu solder interconnects. Failure analysis showed copper trace failure for all OSP specimens and intermetallic failure between the Ni_3Sn_4 and Ni-P layers for all ENIG specimens.

The authoritative work on the effect of isothermal and thermal cycling aging on intermetallic and kirkendall void growth was published in 2006 by Luhua and Pang [55]. They conducted JEDEC drop tests on thermally aged PWAs mounted with SnAgCu BGA components with different plating materials to study the effect of intermetallic morphology and kirdendall void growth on board level durability. The PWAs were subjected to thermal cycling aging of 500, 1000 and 1500 cycles, with a profile of -40^0C to 125^0C. The microstructure near the Intermetallic Compound (IMC) layer compared for isothermal and cyclic aging. The average grain size in the solder, near the intermetallic layer, was 20 microns before aging, 13 microns after 500 thermal cycles, and 5.8 microns after 1500 thermal cycles. The decrease in grain size means more number of grains,

which leads to more grain boundaries. The authors suggested that the reduction in grain size at the solder/IMC interface was due to dynamic re-crystallization caused by the thermal stresses induced by Coefficient of Thermal Expansion (CTE) mismatch. Some PWAs were also subjected to isothermal aging at 150^0C for 120 hours, 240 hours and 390 hours. The grain size at solder/IMC interface increased to 30 microns after 260 hours of aging, and some even reached 50 microns. In some PWAs, the grain boundaries disappeared and grains were combined together.

The authors observed a significant decrease of drop durability was observed for both SnAgCu/ENIG and SnAgCu/Cu-OSP packages after thermal aging. SnAgCu/ENIG showed better durability after aging than SnAgCu/Cu-OSP. Most of the interconnects failed at the intermetallic layer, though some also failed in the copper trace and the FR4/Cu-pad. In the as-reflowed SnAgCu/cu-OSP specimen, the intermetallic failure was either near the Cu_6Sn_5/Cu_3Sn interface or near the $SnAgCu/Cu_6Sn_5$ interface or within the Cu_6Sn_5 layer. After 500 cycles of thermal aging, dominant cracks were seen within the Cu_6Sn_5. After 1000 hours, the crack was near the IMC/Cu pad, where a new layer of Cu_3Sn had formed. The crack was found to be flatter than the ones in less aged specimens. After 1500 hours of aging, the crack propagated through the bottom interface. For the SnAgCu/ENIG specimens, the crack was at the IMC/Ni(p) interface for all conditions of thermal cycling. At 1500 cycles, the Ni(P) layer was found to be very thin in some locations and voids could be seen in some spots. In some cases, a non-planar NiCuSn ternary layer was found to grow at the intermetallic layer. .

The authors discussed the formation of Kirkendall voids in the SnAgCu/OSP solder joints that were subject to isothermal aging. Unbalanced Cu-Sn interdiffusion through

interface creates atomic-level vacancies because the migrating Cu atoms on the bare Cu side are not filled by Sn atoms. These vacancies coalesce into the so-called Kirkendall voids. No voids were observed for the as-reflowed specimens, but quite a lot voids formed at the Cu-IMC interface after 500 thermal cycles. The density of the voids area increased with number of thermal cycles. The voids finally coalesced and generated micro-cracks at the interface. The authors noted that the voiding process due to thermal cycling was faster than that in isothermal aging. This could be due to the dynamic recrystallization at the Solder/Cu_6Sn_5 interface which could accelerate the interdiffusion of Cu atoms. The interdiffusion rate in the Cu_6Sn_5/Cu_3Sn/Cu interfaces kept the original rate, causing the unbalanced Cu-Sn interdiffusion through interface to become even more significant. The growth of kirkendall voids could explain the effect of thermal cycling on drop durability of SAC/Cu-OSP samples. As the sub-micron level voids formed near the Cu/IMC interface and coalesced during thermal cycling and these cracks propagated much easier at the interface than in the IMC layer.

Dewen, et al. [56] examined the evolution of the interfacial microstructure of SnAgCu solders bonded to Au/Ni/Cu pads for as-reflowed and aged conditions. One intermetallic compound with rough morphology and with needles penetrating into the solder was observed in the as-reflowed state. After aging, the authors observed that the solder/copper pad interface had two intermetallic compounds with a flat interface between them. Some parts of the IMC spalled into the bulk solder. Drop tests were conducted on the as-reflowed and aged PWAs. The as-reflowed PWA had cracks going through the solder and the intermetallic layer. The aged PWA failed completely in the intermetallic layer. Failure analysis showed that the crack weaved through the

intermetallics and the interface between the two intermetallics. Analysis of the fracture surface showed that the crack was brittle and no plastic deformation was found at the fracture surface. Thus, thermal aging influences the durability by providing alternate paths for crack propagation.

Irrespective of the test method used, the failure site dictates the failure mechanism and hence the damage model that is needed to predict durability. Appropriate damage metrics have to be chosen to quantify durability and develop failure envelopes. Researchers have used finite element simulations to gain an insight into the problem.

2.2.3 Simulation

Drop testing simulations have been conducted by modeling the solder as a rate independent elastic material [33], a rate dependent elastic material [2, 57, 58] and a rate dependent bilinear material [59]. The maximum strain rate in the solder ball during drop testing, calculated from FEA, varies from 200/sec [33] in Sn-Pb solders to 20/sec [2] in SAC solders.

Yu, et al [2] conducted simulations of tests conducted on a JEDEC drop testing machine using rate-dependent elastic material properties to understand the effect of PWA orientation on drop durability. It was shown that a 2 degree and 10 degree drop orientation with respect to the horizontal can decrease maximum out-of-plane displacement of the PWA by 30%, when compared to that of a JEDEC style drop test. By using simple energy principles, an equivalent drop height was proposed to accommodate the effect of PWA orientation on the drop durability.

Simulation of board level drop testing was also used to conduct parametric

analyses. Wong, et al. [31] conducted a parametric study of board level drop test using FEA simulations and proposed that peeling stress in solder is the primary damage causing mechanism. It increases linearly with increasing impact velocity, increases monotonically (almost logarithmically) with decreasing bump height, decreases monotonically (asymptotically) with increasing solder bumps, and increases with increasing board length. The peeling stress in the solder is due to the curvature of the board and the inertial force of the component. For the same component, the peeling stress decreases with increasing PWA thickness because the differential stiffness decreases. But after a certain thickness value, the PWA stiffness is so high that it does not flatten under the component and increases the peeling stress. Similar parametric studies were done by other researchers [60, 61] for JEDEC drop tests of PWAs.

Irrespective of whether strain-based or stress-based metrics are used to quantify durability, it is very clear that rate-dependent elastic-plastic solder material properties have to be used to realistically simulate the drop event. This necessitates the use of explicit finite element codes that are very time-consuming. Researchers have tried to develop techniques to reduce the simulation run time by first starting with implicit codes. Jie, et al. [62] created approximate models of the test specimens and compared that to the results obtained from an accurate FEA model. Different techniques were used to replace the solder joints, including equivalent beams and equivalent solder joint. One of the drawbacks of using beams to replace solders was the fact that only one node was used to represent the interface between the solder and the board. This affected the curvature at the solder/board interface, leading to erroneous results. In the equivalent solder joint model, one equivalent solder joint is used to represent a cluster of solder joints that are

not critical to the analysis instead of using one beam per solder joint. The material properties of the equivalent solder joint was the same, but the dimensions were different. For example: the height of real solder joints was maintained, but the radius of the columns was increased to four times, such that mass of the solder column layer remained the same. FEA simulations were run on single component PWA with 10,000 interconnects using linear elastic material properties. The stresses at critical solder joint for the equivalent solder joint model and actual model were found to be in good correlation. Significant reductions in model size and computational time were observed. Gu, et al. [63] also explored the feasibility of using an equivalent continuous layer of solder to replace the solder balls. Equivalent elastic modulus, poisson's ratio and shear modulus were used in the approximate FEA model. Different techniques were explored, including a fully smeared model and a partially smeared model with solders at critical locations. The optimization of accuracy and computation time was done by comparing the simulation run time, total number of elements, size of critical element area, etc.

Lall, et al. [35, 64] used explicit FEA code to model the in-plane drop of two PWAs to study the reliability of CSP and BGA packages, with eutectic Sn-Pb and Pb-free solders. Two modelling approaches were used: reduced integration solid elements and continuum solid elements. Node to surface contact algorithm was used with rigid elements to model the floor. Smeared properties are used for the components. FEA results and test data were correlated using mode shapes captured by camera.

Liping and Marcinkiewicz [59] used FEA to explore the feasibility of using von mises strain and plastic strain in the solder as the failure criterion. They conducted board level drop tests on PWAs mounted with Sn-Pb components using a JEDEC style drop

tester and then simulated the tests using 3D explicit FEA. The solder was modeled as a rate-dependent bilinear material with strain rates up to 1E2 sec^{-1}. An accelerometer attached to the fixture and two strain gages on the PWA were used to correlate the experiment and numerical model. The FEA used the shock pulse as input and tracked the von mises and plastic strains in the solder with respect to time. Both types of strains showed sinusoidal fluctuation that corresponded to the post-impact board vibrations, but the von mises strain showed elastic recovery and the plastic strains showed a logarithmic increase as the vibrations continued. They showed that test conditions that induced higher plastic strain in the solder (as calculated by FEA) also led to lower interconnect durability. Hence, plastic strain was proposed as a failure criterion. It was also shown that simulations using rate-independent solder material properties overestimate the solder plastic strain by as much as 50%, when compared to those using rate-dependent properties. This study underlined the necessity of using rate-dependent material properties for the simulation of PWA drop tests.

Tee, et al [65] explored the use of stress in the solder as the parameter to quantify drop durability when the failure site is the intermetallic layer. JEDEC style drop tests were conducted on PWAs instrumented with strain gages. The FEA model used 3D quarter symmetry of the component with linear elastic material properties. The shock pulse was used as input to the FEA model and the calculated PWA strains showed good correlation with the strain gage data. The shear, peeling, and principal stresses in the solder were plotted with respect to time. They showed that shear stresses in the solder were negligible compared to the peeling and principal stresses and the magnitude of the peeling stress was more than that of the principal stress. The authors concluded that

peeling stress was the primary criterion to quantify durability. Luan, et al. [66] used peeling stress as the damage parameter to quantify the drop durability of system in package components. JEDEC drop tests were conducted and the measured impact pulse was used as input to a 3D FEA model with linear elastic material properties. Detailed package geometry, solder balls and pad design were included in the model. FEA shows high stress concentration at the failure site, which was the intermetallic layer on the component side of the outer most solder ball. As proposed by Tee, et al [65], maximum peeling stress was considered to be the root cause of the brittle failure. Power law fit was used to correlate average drops to failure from the test to maximum peeling stress of critical solder, obtained from the FEA. The authors noted that the value of the peeling stress is depends on element size, material models, etc., while the number of drops to failure depends on the test setup, failure criteria and other variables. Hence, the correlation constants are dependent on the failure model and drop tester. Tee, et al. [67] also used peeling stress to characterize the drop durability of Thin and Fine-pitch Ball Grid Array (TFBGA) packages with SnAgCu interconnects subjected to JEDEC drop tests. 3D FEA with linear elastic material properties was used and the stress concentration at the intermetallic layer in the outermost solder ball matched the failure site. The durability shows a power law relationship with peeling stress at the failure site. Pang and Che [68] used von-mises stress as the damage metric to understand the damage in the interconnects of SnAgCu PBGA components. The PWA was clamped at both edges and subjected to drop tests. FEA with rate-dependent elastic-plastic properties was used to compute the von-mises stress.

Shah and Mello [69] proposed the use normal and shear forces in the solder to

develop overstress failure envelopes for the solder interconnects. Mathematically, $Z(F_{normal}, F_{shear}) = 0$ is used to characterize failure, such that $Z>0$ implies failure. F_{normal} and F_{shear} are the normal and shear forces in the failure site, respectively. $Z(F_{normal}, F_{shear})$ can be defined as a linear function (Mohr-Coulomb) or non-linear function (Drucker-Pager), depending on the physics of the loading and failure site. This technique, commonly used to characterize crack propagation in brittle rocks, was applied to three-point bend tests of a PWA at different displacement rates. The component of interest was a single BGA chipset at the center of the PWA and the observed failure site was the intermetallic layer. The load-displacement curves obtained at different displacement rates show that the critical load to failure decreases with increasing loading rate. A detailed 3D FEA model, with elastic material properties, was used to determine the force state of the failure site by summing the internal forces in a layer of elements in the ball at different values of board curvature. Comparison with experiments showed that the ball with the force state closest to the failure envelope was the first to actually fail. A case study, using a computer motherboard, was used to successfully demonstrate the applicability of the proposed approach.

2.2.4 Durability Models

Durability models have been proposed over the last few years to quantify interconnect durability under board level impact testing conditions. In Feb 2003, Varghese and Dasgupta [70] introduced a test methodology (included in this thesis) to predict impact durability of surface mount interconnects. PWA flexural strain was used as the damage metric and the damage model was based on brittle crack propagation because the failure site was in the brittle intermetallic layer. A damage quantification

algorithm was proposed, which used wavelet decomposition to decompose the PWA strain history into its constituent modal contributions, and rainflow cycle-counting to assess the damage at each frequency level. The test methodology was demonstrated for a PWA with a single Sn-Pb PBGA component, subjected to in-plane and out-of-plane impact on fixtures with different boundary conditions. Although the damage constants were verified to be independent of impact orientation, loading conditions and boundary conditions, the model constants were specific to the architecture of the PWA being tested. In Nov 2003 [10] the test methodology was modified to change the damage metric from PWA strain to solder strain by using FEA. This made the test methodology more generic, within the approximations of the analysis, because the model constants were a function of the material properties alone. Tee, et al. [71] proposed a durability model in May 2003 for out-of-plane drop testing of PWAs. Maximum peeling stress in the solder was used as the damage metric and the durability model was formulated using a power law relationship. The technique was demonstrated for boards mounted with TFBGA and Very Thin Profile Fine Pitch Ball Grid Array (VTFBGA) components and subjected to drops on a JEDEC board level drop tester. In 2004, Liping and Marcinkiewicz [59] proposed the use of effective plastic strain in the solder ball as the damage metric and compared the component reliability at different loading conditions. Although a damage model was not developed, components with higher effective plastic strain were shown to fail earlier than those with lower values of plastic strain in the solder ball. In 2005, Lall, et al. [72] demonstrated the use of a damage quantification technique very similar to the one proposed in this study, on test vehicles mounted with BGAs and CSPs, subjected to in-plane drop. Wavelets and cycle counting techniques were used to quantify the complex

load history. PWA flexural strain was used as the damage metric and the damage model was based on the Coffin-Manson relationship because the failure site was in the solder. In 2006, Varghese and Dasgupta [73] proposed an empirical rate-dependent durability model based on mechanistic considerations. The derivation and explanation are provided in this thesis. PWA strain and strain rate were used as metrics to quantify durability and identify a critical zone where the failure site changed from the solder to other parts of the PWA. The model was successfully used quantify the behavior of PWAs with SnPb/OSP single chip BGAs and SnPb/ENIG stacked die BGAs.

2.3. Correlation Between Board and Product Level Drop Testing

It is generally difficult to correlate the board level drop test results to product level drop test results. The PWA is clamped to the fixture during board level drop testing and is allowed to vibrate after a single drop event. Product level drop testing usually involves multiple impacts and rotations after the first impact, termed as clattering. High-speed photography by Goyal and Buratynski [74] indicates that during a single product level drop event, one corner of the electronic product touches down first and there is "clattering" as other corners strike repeatedly. The product then bounces or comes to rest after undergoing these multiple impacts at its ends. It has been shown that during clattering, the product can experience velocity shocks that are several times higher than those experienced in a single drop event. The details of the clattering motion, and the various impact parameters of interest to the designer (change in velocities and impulses, the duration of the clatter, et cetera) depend significantly on the mass distribution of the product and its effective coefficient of restitution at impact [23]. The mass distribution and boundary conditions of the PWAs used in the JEDEC board level drop tests is

different from the PWAs mounted in an actual portable electronic device.

One of the factors that make correlation of board level and product level JEDEC drop test data difficult is the use of damage metrics that are very structure-specific, for example: incident force, incident kinetic energy, incident velocity. This makes the damage constants strongly dependent of drop orientation and boundary conditions. Goyal, et al. [24] showed that the impulses associated with individual clatter impacts are very significant because it could lead to resonances in the internal components. This may not be captured by the board level drop tests. Experimental work by Goyal, et al. [30] also indicates that constraining the internal assembly to behave as a single system, as is done in board level drop tests, may even miss important failure mechanisms.

2.4. Interconnect Level Testing

During board level drop testing, the stresses and strains in the solder and the intermetallic layer are influenced by the geometry and material properties of the board, die, overmold, etc. Motivated by the failure site transitions observed during drop, vibration and high-speed bend testing described in the earlier section, researchers developed techniques to characterize the fracture strength and failure site of the solder interconnect at different loading rates. Before reviewing the published literature in this field, it is important to discuss what intermetallics are used in the microelectronics industry and what role they play in a solder interconnect.

Today's predominant PWA surface finishes include Hot Air Solder Level (HASL), OSP, ENIG, Immersion Silver (ImmAg), Immersion Tin (ImmSn), Reflowed Tin/Lead, Electrolytic Nickel Gold, and Electroless Palladium. The solder surface finish techniques

mentioned above fall into two categories based on the composition of the intermetallic layer between the solder and the copper pad: Those with copper-tin intermetallics and those with nickel-tin intermetallics. The intermetallic compound bonds the solder to the copper pad and is a potential failure site. Techniques like HASL and OSP create the Cu_3Sn and Cu_6Sn_5 intermetallic layers between the solder and the copper pad. Solder interconnects with copper-tin intermetallics have shown good durability under thermal cycling, vibration and drop testing conditions. Techniques like ENIG and Electrolytic Nickel Gold provide very good bonding between the solder and the copper trace by forming nickel-tin intermetallics. But the corrosion of nickel by gold results in the formation of a thin black line that can not withstand dynamic loading. Gold embrittlement, when the gold content is more than 0.3%, can also lower the reliability of the joint. Hence, manufacturers of portable electronic devices prefer to use OSP, HASL, or other techniques in their assembly processes. Keeping in mind the cost benefits of OSP, many mobile phone parts are finished with OSP on soldered areas, and with ENIG on touchpad surfaces. Hence, the fracture toughness of the intermetallic layer strongly depends on plating material and the manufacturing process.

Darveaux, et al. [3] used a conventional tensile testing machine to characterize the strength and toughness of a solder joint. The specimen was prepared by soldering together two substrates to form an area array, like a BGA or a flip-chip. The sample was pulled in tension at different displacement rates till the joint failed. Stress in solder was calculated as the ratio of the applied force to the cross-sectional area of all solder balls in the area array package. The strain rate was approximately calculated as the product of the applied displacement rate and the height of solder. The authors acknowledged that the

actual strain rate in the solder joint was less than that given by the calculated value of strain rate because some of the displacement was taken up by the elastic response of the grips and the load train. The biggest advantage of this testing technique was that it took lesser time to obtain statistically relevant data compared to ball shear or ball pull, which could only measure one interface at a time. In their first published paper itself, the authors had tested 990 samples with 566,251 solder balls.

The authors studied the effect of pad metallization, solder alloy, reflow conditions and thermal aging on interfacial fracture of interconnects at high strain rates by subjecting BGA components to pull tests at high displacement rates. During the test, the whole BGA is lifted off the PWA and the solder strain rate is defined as the ratio of the displacement rate of tester to the height of solder ball. The authors reported three failure modes: ductile solder fatigue, brittle fracture of intermetallic layer and pad lift-off. They proposed the use of the Ductile to Brittle Transition Strain Rate (DTBTSR) as a metric to quantify the performance of a package relative to interfacial failure. It was found that the failure site transition generally occurred between strain rates of 0.1 sec^{-1} and 1 sec^{-1}, with solder failure at the low strain rates and intermetallic failure at the high strain rates. In solder failure, failure site was observed to have a cone-cone or taffy pull type of failure. During intermetallic failure, the solder showed little plastic deformation and the fracture surfaces were flat. The authors also showed experimentally that the interfacial strength of the intermetallic layer decreases with increasing loading rate. This trend was observed for all solder alloys and for all aging conditions. Similar to the idea proposed in this thesis [4, 37], the authors characterized the failure site transitions in terms of rate-dependent increase in the tensile strength of the ductile solder and decrease in the tensile strength of

the brittle intermetallic.

Yeh and Lai [75] modified a drop tower to develop a Ball Impact Tester (BIT) that conducted high-speed shear tests on the solder interconnects of BGAs. A fixture was used to hold the component in a vertical position and a hammer was released from a specific height to fall along a guide rail. The hammer struck a pin which was in contact with the solder interconnect and the impact force was measured. The force-time plot was used to quantify certain parameters of the solder interconnect: Peak force was used as a measure of strength, which was a mix of normal and shear loading because the pin actually caused mixed mode loading in the interconnect. The time taken to go from zero force to peak force was used as a measure of the ductility of the solder joint. The loading part of force-time plot was used to measure joint toughness by calculating area under the curve. Impact energy was calculated as a product of the toughness and the impact velocity. The ratio of the slope of the force-time curve to the impact velocity was used to represent the stiffness of the joint. Tests showed that different fracture toughness values and failure sites could be obtained by varying the impact force magnitude and rate.

Yi-Shao, et al. [48] and Chang-Lin, et al. [76, 77] characterized transitions in the failure site on the basis of applied force and solder dynamic yield stress. Three failure modes were observed: solder failure, fracture through solder and intermetallic, and intermetallic fracture. It as observed that at low force amplitudes and rates, the failure was in the solder. As the loading amplitude increases, the yield stress of the solder increases due to strain-rate hardening. For the same load amplitude, the failure site transitioned from pure solder to mixed solder and intermetallic and finally purely intermetallic as the loading rate increased. The failure site was said to transition when the

yield stress of the solder exceeded a certain value.

Yeh and Lai [78] used a force based failure envelope similar to that developed by Shah and Mello [69] to characterize intermetallic failure during ball impact tests. The interfacial failure was characterized by $\left(\frac{|f_n|}{S_n}\right)^{C_n} + \left(\frac{|f_s|}{S_s}\right)^{C_s} \geq 1$, where subscripts f_n and f_s are the applied normal and shear forces, respectively, and S_n and S_s are the normal and shear force strengths of the intermetallic layer, respectively. A case study was presented using a single solder interconnect subjected to ball impact tests. A 3D FEA model with quarter symmetry was used with tetrahedral solid elements to eliminate hourglassing effects due to the localized stresses at point of impact. Intermetallic fracture at the solder/Cu-pad interface was modeled using tiebreak nodes-to-surface contact which links adjacent meshes and confines the movements of nodes until the bond breaks. As a zeroth order approximation, the values of C_s and C_n were assumed to be 2, thus making the failure envelope elliptical in nature. The normal force strength (S_n) was calculated as the product of the tensile strength and contact area, and the shear force strength (S_s) was assumed to be twice the value of S_n. The area under the ascending part of the force-time curve obtained from the impact tests was used to determine the impact energy. It was shown that the plot of (f_n-f_s) with respect to applied force shows the same slope, irrespective of solder composition.

2.5. Summary

The literature review presented above can be summarized as follows

• Many test setups have been proposed to quantify drop durability of PWAs. It has been

demonstrated that component inertia has a negligible effect on the durability of PWAs mounted with low mass components (for example: PBGAs). Hence, board level drop tests can be replaced by high speed bending of the PWA, as discussed in Chapter 3.

- There are many metrics to quantify durability of the PWA under dynamic flexural loading conditions. Some metrics, like PWA strain, make the results specific to the specimen tested, while others, like plastic strain in the solder at the failure site make the results much more generic. All the prior durability models were rate-independent, even though the failure sites experience rate-dependent behavior.
- Numerous studies report that under certain conditions of applied loading and thermal aging, the failure site changes from the solder to the intermetallic. Some researchers have used empirical models to characterize the failure site transition. However, no study provides a qualitative or quantitative mechanistic explanation of the observed phenomenon.

This dissertation extends the state-of-art in the following manner

- In Chapter 3, Failure Maps are developed in terms of PWA strain and strain rate to characterize failure site transitions from the solder to other parts of the PWA. A rate-dependent empirical durability model based on mechanistic considerations is developed to quantify fatigue failure envelopes for the solder. The fatigue constants of the empirical model are used to identify the individual effect of loading amplitude and rate on the behavior of the solder interconnect.
- In Chapter 4, mechanistic insights are provided into the strong dependence of the solder failure on load magnitude, and weak dependence on loading rate. A durability metric is

introduced to quantify rate-dependent durability of the solder, in the strain rates observed during dynamic flexural loading of the PWA.

- In Chapter 5, mechanistic insights are provided into the failure in the interfacial IMC layer of the solder interconnect. The effect of thermal aging on the morphology, and hence the durability of the interfacial IMC layer are understood and quantified.
- In Chapter 6, interfacial fracture mechanics and exhaustion of ductility principles are used to characterize the durability and failure site transition in the solder interconnect in terms of mechanistic parameters, rather than empirical ones.

Chapter 3: Empirical Rate-dependent Failure Envelopes[+]

This chapter presents an experimental study to characterize the durability and failure site transitions in the solder interconnects of PWAs subjected to dynamic flexural loading. Depending on the loading conditions, the failure is found to be either in the solder joint or in the Cu trace on the PWB. PWA strain and strain rate are measured and used to develop a rate-dependent empirical durability model for the solder. It is observed that for the test conditions of this study, the durability of the solder is strongly dependent on loading amplitude and weakly dependent on loading rate. The transition to Cu-trace failures is charactierized in terms of competing failure envelopes and failure maps. The original draft of this chapter is a journal paper that is currently accepted for publication in Microelectronics Reliability. The next chapter (Chapter 4) will focus on developing mechanistic fatigue curves for the solder.

An Experimental Approach to Characterize Rate-dependent Failure Envelopes and Failure Site Transitions in Surface Mount Assemblies.

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This paper presents an experimental approach to identify the fatigue failure envelopes for solder damage in Printed Wiring Assemblies (PWAs) subjected to dynamic

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loading. An empirical, rate-dependent, power-law durability model, motivated by mechanistic considerations, is proposed to characterize the failure envelopes in terms of PWA flexural strain and strain rate, as damage metrics. It is further shown that there are critical combinations of these damage parameters, beyond which the failure site changes from the solder to other locations on the PWA. A case study, using a simple PWA specimen containing a single area array component, is presented to demonstrate the proposed approach. Under certain loading conditions, the failure site changes from the bulk solder to the Cu-trace/FR4 interface. The proposed durability model is shown to successfully describe the solder damage failure envelopes. The concept of a "Failure Map" is shown to provide a suitable framework to quantify the durability of the solder interconnect, determine its failure envelope, and identify the failure transition zone of the specimen. The applicability of the proposed technique for comparing the durability of different packaging styles and for developing design guidelines for PWAs subjected to dynamic loading (for example: drop) is discussed.

Keywords: drop test, four-point bend, failure site transition, strain rate, dynamic, durability model.

Nomenclature

a, b : Coffin-Manson constants for solder (-)

c, d, a_1, b_1, c_1, d_1: Damage model constants (-)

A, B, C : Damage model constants (-)

$\Delta\varepsilon_p$: Plastic strain in the solder interconnect (-)

ε_f : Failure strain of the solder (-)

ε_{PWA} : PWA flexural strain (-)

$\varepsilon_{PWA}^{failure}$: PWA strain for overstress failure at quasi-static loading conditions (-)

$\dot{\varepsilon}_{PWA}$: PWA flexural strain rate (sec^{-1})

$\dot{\varepsilon}_0$: Quasi-static PWA strain rate (sec^{-1})

N_f : Average number of cycles to failure (-)

3.1. Introduction and Problem Statement

Dynamic loading plays a crucial role in the durability of solder interconnects in Printed Wiring Assemblies (PWAs). The trend toward decreasing solder ball diameter, pad diameter and I/O pitch makes the interconnect more susceptible to failure. This is often true for PWAs in portable electronic devices that are frequently subjected to dynamic loading during mechanical handling, accidental misuse and/or shipping (transportation). Examples include cell phones, laptops, and PDAs. PWAs used in military applications are often subjected to severe vibration, repetitive impacts and/or high G loading. Dynamic loading of the PWA during product assembly can also severely shorten the durability of the solder interconnect. Hence board level solder joint reliability under dynamic loading conditions is of critical concern to the microelectronics industry.

Board level tests are usually conducted on a sub-assembly drop testing machine based on a JEDEC Standard [9]. The PWA is screwed on to a drop carriage in the horizontal position at four or six points. The drop carriage falls along two guide rods and

induces out-of-plane displacement in the PWA on impact. On impact, the PWA responds to the transient impact force applied to the base and then vibrates at its natural frequencies. Instrumentation typically consists of accelerometers mounted on the drop carriage and strain gages on the PWA. Recent work by Seah, et al. [38] proves that solder ball damage due to PWA flexure is much greater than that caused by inertial loading, thus making PWA flexural strain and strain rate the primary mechanisms which cause damage. Hence, bend tests can be used to focus the study on PWA flexural strain and strain rate and on its effect on interconnect durability.

Much work has been done to develop durability models and failure envelopes for solder interconnects under dynamic loading conditions. Empirical models have been developed to quantify durability as a function of PWA strain [9]-[70] and PWA displacement [110]. In some cases, Finite Element Analysis (FEA) with rate-independent material properties has been used to quantify durability in terms of solder stress [35] [12][113] or solder strain [12][27] and to develop failure envelopes based on normal and shear forces in the solder [69].

However, the existing durability models and failure envelopes are rate-independent, even though tests show that the durability of the PWA varies with the loading rate [58][42]. There is a need to understand the combined effect of load amplitude and loading rate on the durability of the solder interconnects. Appropriate damage metrics have to be chosen to quantify durability and develop failure envelopes.

This work is vital because load amplitude and loading rate can change the failure site from the solder to other locations on the PWA. The failure site dictates the failure mechanism and hence the damage model that is needed to predict durability. Yu, et al. [2]

were the first to report a transition in the failure site from solder to the intermetallic with increasing drop height during drop testing of PWAs. Heaslip, et al. [47] compared the drop durability of Sn37Pb and Sn95.5Ag3.8Cu0.7 solders and showed that the failure sites and failure mechanisms change with drop height and solder type; while Varghese, et al. conducted high-speed bend tests and showed that the failure site transitions from the solder to the copper trace for specimens with Organic Solderability Preservative (OSP) finish [114][4]; and from the solder to the intermetallic compound (IMC) layer for specimens with Electroless Nickel/Immersion Gold (ENIG) finish [11]. Wong, et al. [36] showed that the failure sites and failure mechanisms change with solder and plating type. Despite the previous work described above, the transition of the failure site due to dynamic loading remains poorly quantified and understood.

An experimental approach is presented to characterize the failure site transitions, develop failure envelopes for each component architecture and quantify the durability of the solder interconnects for PWAs subjected to dynamic loading. PWA flexural strain and PWA flexural strain rate are used as damage metrics. The proposed technique is demonstrated on a PWA with a single Plastic Ball Grid Array (PBGA) mounted on it. The results of this study can be used by engineers as the basis of design guidelines for different surface mount component architectures and by researchers to develop damage models for surface mount interconnects.

This paper is part of an ongoing effort to develop a generic test methodology for drop testing of PWAs. Earlier work by the authors [113] focused on the effect of loading amplitude, loading orientation and boundary conditions on the durability of the solder interconnects. The work presented in this paper adds the effect of loading rate on the

durability and the failure site of the PWA, with an emphasis on solder failure.

The experimental details are first explained, followed by the test results. The subsequent sections discuss the failure envelope and the damage model. The applications of this technique and future work are discussed at the end of the paper.

3.2. Approach

A test matrix, as shown in Figure 3-1, is developed to characterize the durability in terms of PWA flexural strain and strain rate. The test matrix spans four orders of magnitude of PWA flexural strain rate. Dynamic four-point bend tests are conducted to induce a nominally uniform bending moment in the region of interest around the component. The tests are replicated once to verify the consistency of the data. A commercially-available servo-hydraulic bend test machine is used for the low strain rate tests, and a drop tower is used for the high strain rate tests. A high-speed data acquisition system is used to obtain the strain history and durability of the specimen for each test condition. Failure analysis is performed after each test to identify the failure sites. A damage law and failure envelope are developed to quantify the durability of the solder interconnects.

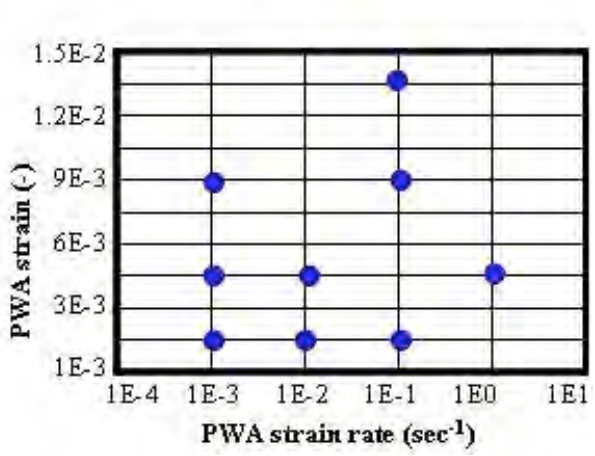

Figure 3-1: Test matrix. The circles represent the test conditions.

The following simplifying approximations have been made in the development of the proposed technique. Interconnect damage due to inertial mass of the component and stress wave propagation in the solder ball is assumed to be negligible when compared to the rate-dependent damage due to PWA dynamic flexure. The solder balls are approximated as isotropic, homogenous and defect free. The effect of initial defects and initial residual stresses on drop durability is neglected. Damage accumulation is assumed to follow Miner's rule.

3.3. Test Setup

A commercially available servo-hydraulic test machine is used for four-point bend tests at PWA flexural strain rates below 0.1 sec^{-1}, (Figure 3-2) and a drop tower is used for strain rates above 0.1 sec^{-1} and up to 2 sec^{-1} (Figure 3-3). The displacement of the LVDT in the servo-hydraulic machine can be varied from 0 to 100 mm and displacement rate can be varied from 0 to 12.5 mm/sec. The drop tower is used to drop steel spheres on the fixture holding the specimen in a four-point bend configuration to conduct high-speed bending tests (Figure 3-3). The fixtures holding the specimen are made of Delrin to damp

out the high frequency ringing due to the impact of a steel sphere. These fixtures slide on hardened steel guide rods with linear bearings. The rigid base and the crossbar are made of aluminum. The guide rods are carefully aligned parallel to each other and perpendicular to the base. Both guide rods are torqued to increase their natural frequencies and thus decrease vibration during testing. The mass of the sphere can be varied from 65 g to 450 g and the impact velocity can be varied from 0 to 6 m/sec by changing the sphere drop height.

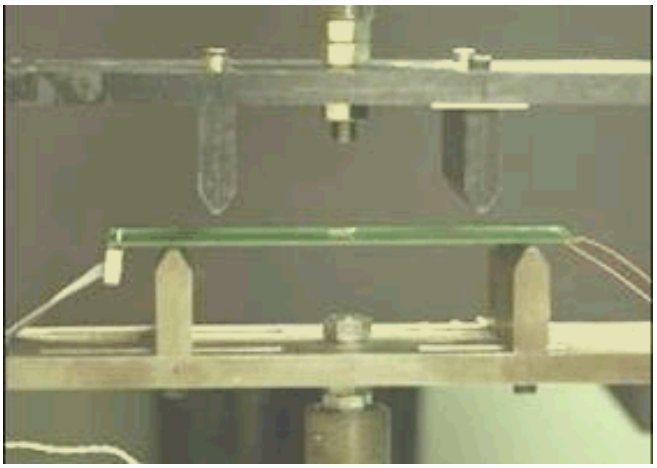

Figure 3-2: Four-point bend test fixture on servo-hydraulic mechanical tester.

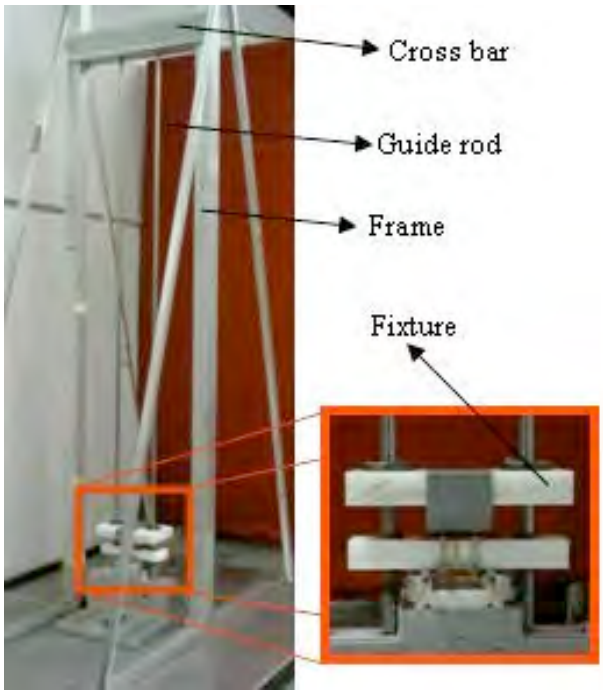

Figure 3-3: Drop tower with four-point bend fixture.

A high-speed 4-channel data acquisition system, with a maximum sampling rate of 5 MHz per channel, is used to track the PWA response and the solder ball failure in real time (Figure 3-4). As the curvature of the board increases, the cracked surfaces of the failed interconnects are mechanically separated, thus causing an increase in the daisy chain resistance. Failure is defined as an increase in the electrical resistance of the interconnect by 1000 Ω. As the curvature decreases, the fractured ends on the interconnect contact each other again, thus closing the electrical circuit. Due to this transient nature of the test, the opening of the circuit lasts for as little as five milliseconds. As a consequence, an in-situ high-speed resistance measurement system, developed in an earlier study [9], is used for continuous failure monitoring during the test. The resistance monitoring system consists of a Wheatstone bridge, with the daisy chain resistance forming the quarter bridge. The bridge can be balanced and its sensitivity varied, by

changing the values of the resistance of the other three arms of the bridge.

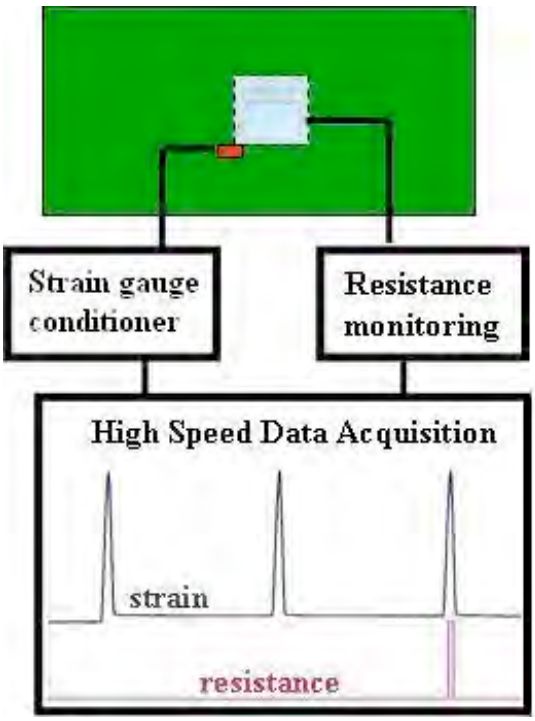

Figure 3-4: Schematic diagram of the instrumentation.

3.4. Specimen Design

The specimen (Figure 3-5) is a 256 I/O, full grid PBGA with 0.5 mm diameter solder balls on a 1 mm pitch. This component is daisy chained for in-situ electrical continuity checks and is mounted at the center of a 140 mm X 101.6 mm X 1.6 mm FR-4 board. The board has one layer of copper traces on its surface at the component side to connect the daisy-chained component to the terminals. The solder balls are made of Sn37Pb eutectic solder. The pad finishes on the board and component side consists of an organic solderability preservative (OSP) and Sn15Pb, respectively. A 350 Ω strain gage with 3.18 mm gage length and 2.54 mm grid width is attached to the board near the corner of the component (the site of maximum PWA curvature) to measure the flexural

strain and the flexural strain rate. An electrical continuity tests is performed on each daisy-chained component to detect any opens or shorts. The purpose of choosing this simple specimen design is to allow an in-depth study of the drop event, without making the analysis too complex. The specimens are tested in as-soldered condition without any additional aging. The influence of aging on failures due to dynamic loading is discussed in an earlier paper [11]. The changes in the microstructure due to thermal aging can provide a low-energy path for crack propagation through the intermetallic layer which leads to a drastic reduction in the durability of the interconnect.

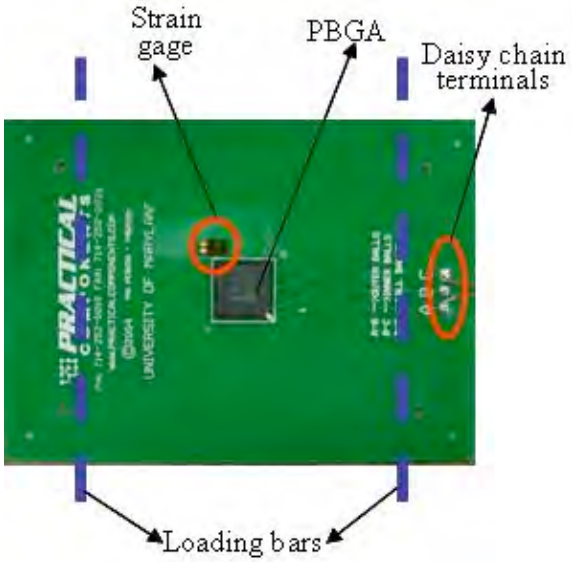

Figure 3-5: Specimen configuration.

3.5. Damage Model

As explained earlier, existing damage models in literature [10][12][27][35][70] [110]-[113] do not address the rate-dependence of durability, for dynamic loading of PWAs. We propose a new mechanistic, rate-dependent durability estimation model in this paper that focuses on solder failure. The model constants are architecture-dependent

and are empirically determined from dynamic testing.

During low-cycle fatigue, failure in the solder is dominated by plastic strain. The durability model, as proposed by Coffin and Manson [115] is:

$$N_f = a * \left(\Delta\varepsilon_p\right)^{-b} \tag{3-1}$$

For overstress failure, $N_f = 1, \Delta\varepsilon_p = \varepsilon_f$. Therefore,

$$\frac{N_f}{1} = \frac{a\left(\Delta\varepsilon_p\right)^{-b}}{a\left(\varepsilon_f\right)^{-b}} \tag{3-2}$$

Solder is a rate-dependent ductile material [116]. For a given loading condition, the plastic strain and the failure strain (ductility) of a ductile material decrease with increasing strain rate due to a phenomenon called strain-rate hardening. For a given PWA architecture, the solder plastic strain increases monotonically with PWA strain. Therefore,

$$\Delta\varepsilon_p = f\left(\dot{\varepsilon}_{PWA}, \varepsilon_{PWA}\right) = a_1 * \left(\varepsilon_{PWA}\right)^{b_1} \tag{3-3}$$

where, $a_1 = c * \left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-c_1}$

Similarly:

$$\varepsilon_f = f\left(\dot{\varepsilon}_{PWA}, \varepsilon_{PWA}^{failure}\right) = k_1 * \varepsilon_{PWA}^{failure} \tag{3-4}$$

where, $k_1 = d * \left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-d_1}$

Substituting Eq. 3-3 and Eq. 3-4 into Eq. 3-2,

$$N_f = \left(\frac{c}{d*(\varepsilon_{PWA}^{failure})^{-b}}\right)*(\varepsilon_{PWA})^{-b*b_1}*\left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-b*(d_1-c_1)} \quad (3\text{-}5)$$

Failure strain in the solder decreases with increasing strain rate [83]. Assuming that the failure strain is more rate-dependent than the plastic strain (ie. $d_1>c_1$), the equation takes the form

$$N_f = A*\left(\frac{\varepsilon_{PWA}}{\varepsilon_{PWA}^{failure}}\right)^{-B}*\left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-C} \quad (3\text{-}6)$$

The suitability of this model will be tested in Section 5 on experimental data.

3.6. Results

Cyclic four-point bend tests are conducted for different combinations of PWA flexural strain and strain rate, as shown in the test matrix (Figure 3-1). The testing is stopped as soon as a failure is detected and the specimen is cross-sectioned to determine the failure site. For all specimens, the failure is found to be in the outer rows of the component, parallel to the loading bars of the test fixture. Figure 3-6 shows the variation of durability and failure site with respect to PWA flexural strain and strain rate. A *failure site transition zone* exists for some critical combinations of PWA flexural strain and strain rate, below which the failure is in the bulk solder (Figure 3-7) and beyond which the failure site is in the FR4/copper trace (Figure 3-8, Figure 3-9).

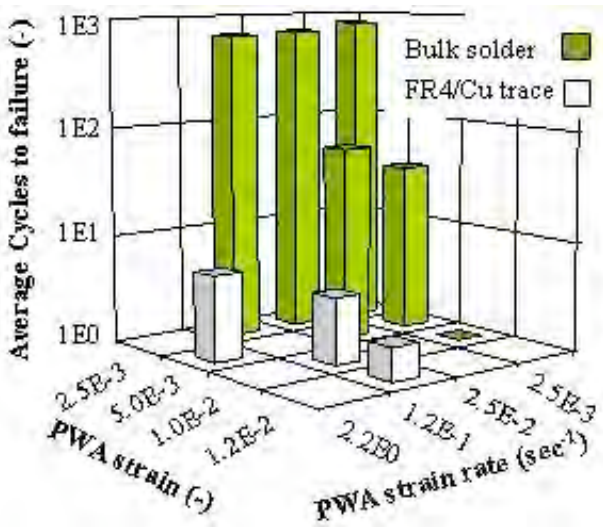

Figure 3-6: Durability and failure site in terms of the damage metrics: PWA strain and strain rate.

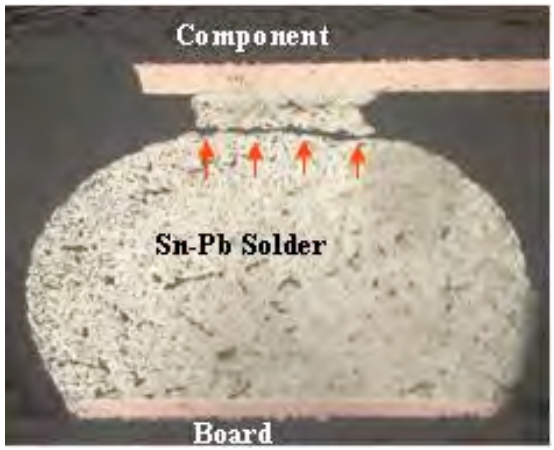

Figure 3-7: Failure in bulk solder.

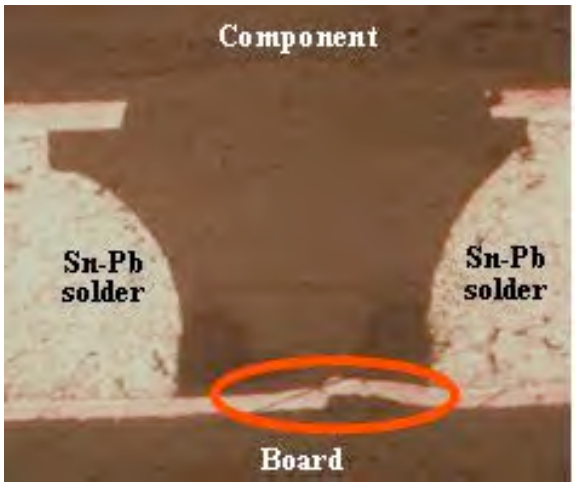

Figure 3-8: Failure in Copper trace.

Figure 3-9: Crack in FR4 under the solder ball.

A brief summary of the test results is presented in Table 3-1. Figure 3-10 shows the variation of durability with respect to PWA strain and strain rate. For a given loading condition, solid trend lines are used for similar failure sites and dashed trend lines are used whenever there is a failure site transition. Irrespective of the failure site, the durability has a power law relationship with PWA flexural strain (Figure 3-10).

Table 3-1: Experimental results.

Test num	PWA strain (-)	PWA strain rate (sec^{-1})	Cycles to failure		Failure Site
			Test 1	Test 2	
1	2.5E-3	2.5E-3	639	1000	Solder
2	5.0E-3	4.9E-3	31	39	Solder
3	9.4E-3	2.5E-3	1	1	Solder
4	2.5E-3	1.2E-1	691	651	Solder
5	2.5E-3	2.5E-2	608	804	Solder
6	4.9E-3	3.8E-2	71	50	Solder
7	5.6E-3	2.2E0	7	5	FR4/ Cu-trace
8	9.4E-3	9.5E-2	5	3	FR4/ Cu-trace
9	1.2E-2	1.2E-1	2	2	FR4/ Cu-trace

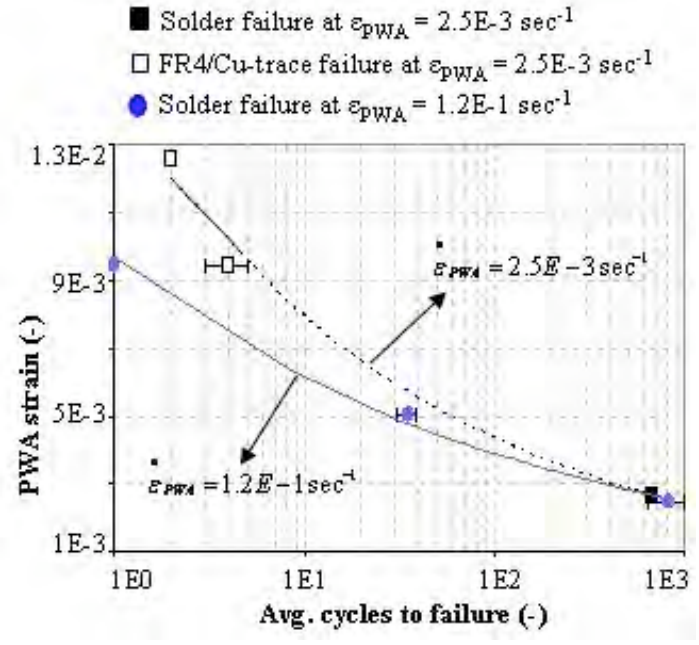

Figure 3-10: Variation of durability with PWA flexural strain for different PWA strain rates.

The test data corresponding to failure in bulk solder are used to obtain the model constants. The values of overstress PWA strain ($\varepsilon_{PWA}^{failure}$) and static PWA strain rate ($\dot{\varepsilon}_0$) are 9.4E-3 and 2.5E-3 sec^{-1}, respectively. The values of the model constants, obtained from this test program, are listed in Table 3-2. A contour plot of the model (Figure 3-11) demonstrates its capability to quantify the durability of the solder within reasonable error limits (Figure 3-12). The overstress failure envelope for the solder corresponds to those combinations of PWA strain and strain rate for which average cycles to failure is one. The solder failure envelopes are seen to have a strong dependence on strain level and a weak dependence on strain rate. In the limit, when rate sensitivity is negligible (eg in intermetallic failures), this durability model simplifies to the strain-based power-law model proposed by Varghese and Dasgupta [12].

Table 3-2: Empirical damage constants.

A(-)	B(-)	C(-)
2.28	-4.43	-0.05

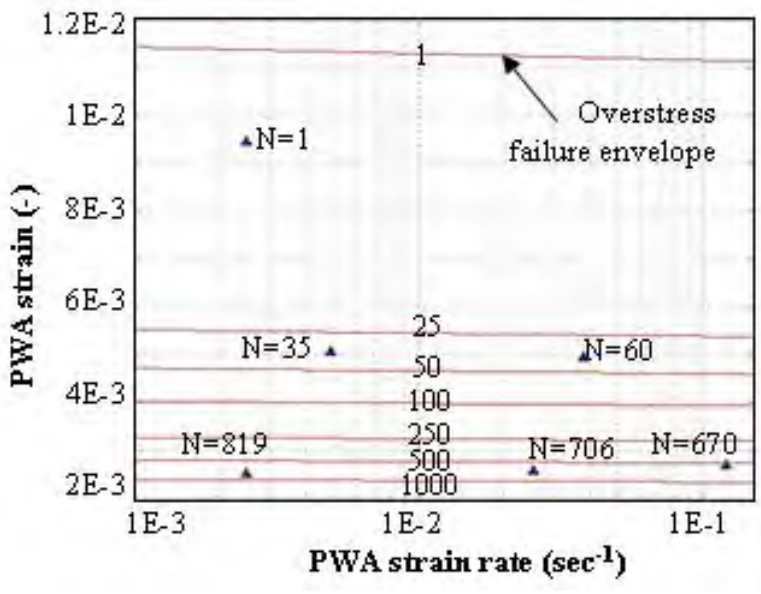

Figure 3-11: Contour plot of the average durability of the solder. The dots represent the test data.

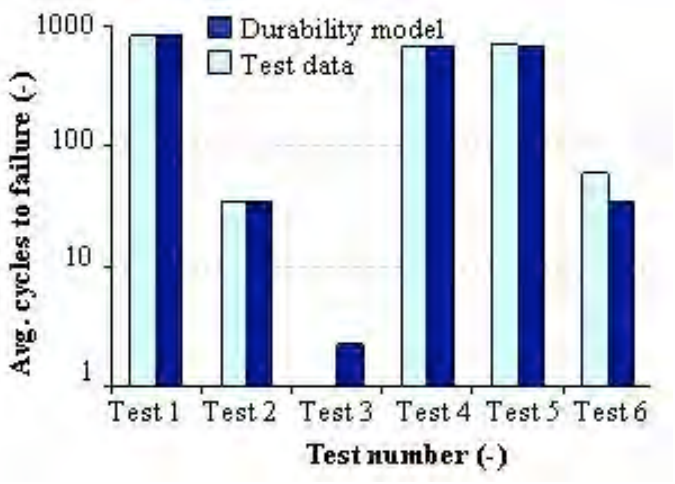

Figure 3-12: Comparison of durability model fit: model vs test data.

The simple mechanistic durability model proposed in Equation 5, is thus seen to describe the failure envelopes with reasonable accuracy. The empirically obtained damage constants in Table 2 are valid only for the tested specimen architecture, because the damage metrics are structure-specific. Future work will use non-linear explicit finite element analysis (FEA) to deduce solder stress from the PWA strain and strain rate. The

corresponding model constants will be reasonably independent of the specimen geometry and predominantly dependent on the dynamic material properties of the solder. The values in Table 2 are presented for illustrative purposes. Additional data points are needed to achieve reasonable confidence in the damage constants.

3.7. Discussion

The phenomenon of transitions in the failure site during dynamic loading of PWAs, especially during drop testing, has not received sufficient attention in the literature. As discussed earlier, the loading conditions can change the failure site from the solder to the intermetallic layer [2][11], copper trace [4], bond pad [36], etc. The strain energy of deformation is divided among competing failure sites, for example: solder, FR4/Cu-trace and intermetallic layer. Ductile materials, like eutectic Sn37Pb solder, have rate-dependent material properties and show an increase in yield stress with strain rate [116]. For the same load amplitude, this phenomenon, called strain-rate hardening, leads to a decrease in the plastic deformation of the solder ball at high strain rates, as confirmed by Tan, et al. [41]. This hardening of the solder interconnect increases the stress in the solder joint and in selected parts of the interconnect system. Thus at high flexure rates, there exist certain loading conditions at which the stress is high enough to reach the cyclic failure limit in the FR4/Cu-trace or in the intermetallic layer, before the strain reaches the cyclic ductility limit in the ductile solder. This leads to a transition in the failure site from the solder to one of the other sites. This concept was schematically in an earlier publication [4].

A schematic 3D plot of the competing failure envelopes is shown in Figure 3-13, to illustrate the notion of failure map and transition zone that marks the transition between

the interconnect failure modes. Figure 3-14 presents the same data in the form of a contour plot. In the example presented in this study, we consider two competing failure sites: solder and FR4/Cu-trace. Each failure site has a fatigue failure envelope, which is quantified in terms of PWA strain and PWA strain rate. The material with the lowest durability for a given loading condition defines both the durability and the dominant failure site for that condition. The fatigue failure envelopes of the competing failure sites intersect along the *failure site transition zone* (defined by the PWA strain and strain rate), as shown in Figure 3-13 and Figure 3-14. At low values of strain and strain rate, the failure site is in the solder and the durability of the interconnect is defined by the solder failure envelope. Beyond the failure site transition zone, the failure site is in the FR4/Cu-trace, and the interconnect durability is defined by the FR4/Cu-trace failure envelope.

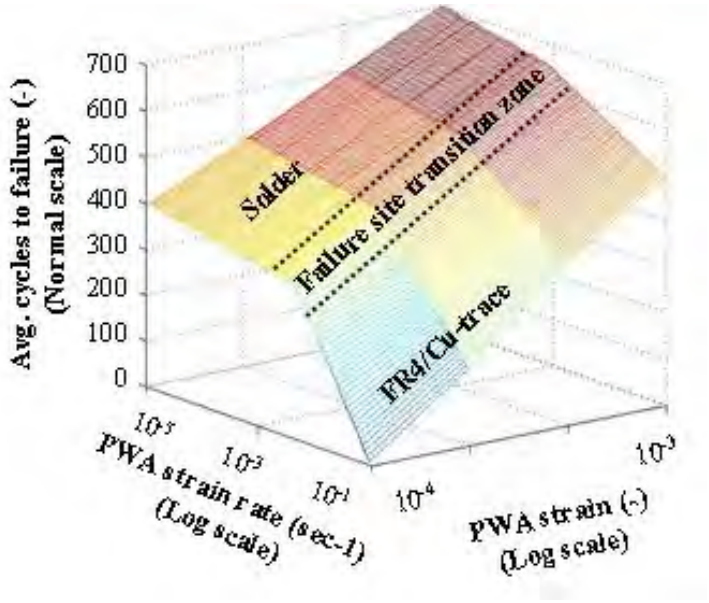

Figure 3-13: Schematic plot of competing failure envelopes for solder and FR4/Cu-trace.

In this study, the failure in the FR4/Cu-trace is either bond-pad liftoff or a fracture of the trace between the two solder balls. In bond pad liftoff, the cracks start from the

surface of the PWA on the solder side, grow through FR4 epoxy and finally fracture the copper trace. No trends have been observed as to when one kind of FR4/Cu trace failure dominates over the other.

The competition between the failure modes is strongly dependent on the PWA flexural strain and strain rate. The technique proposed in this paper allows the engineer or researcher to develop a *failure map* for a given PWA architecture, which defines the failure envelope for each failure mechanism and identifies the *failure site transition zones*, as shown in Figure 3-13 and Figure 3-14. This type of failure map is specific to the component geometry and dynamic properties of the materials used in this assembly. This makes the failure map an ideal experimental method to compare the durability of different PWA systems subjected to dynamic loading conditions.

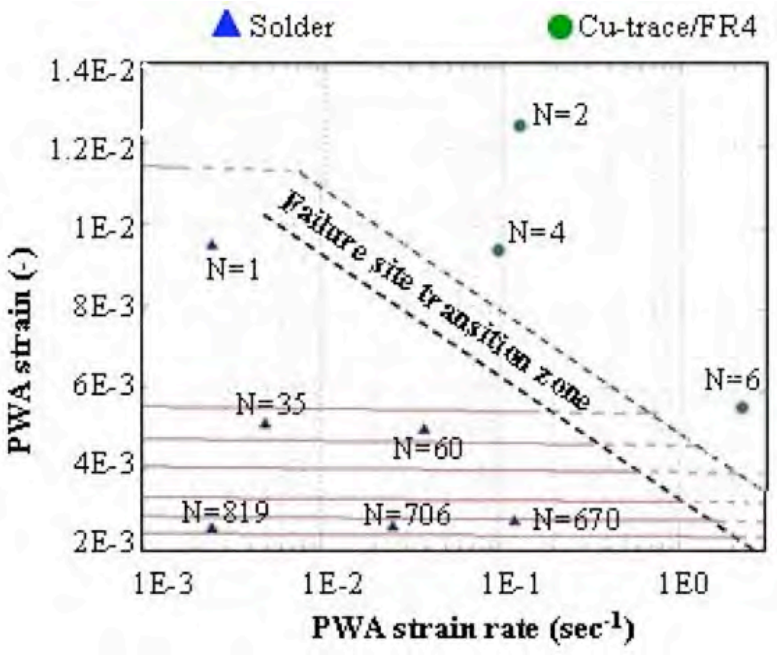

Figure 3-14: Failure map for the solder interconnect.

3.8. Conclusions and Future Work

When a PWA is subjected to dynamic loading, there are competing failure mechanisms in action, each corresponding to a different failure site. The failure site depends on the loading conditions, the assembly architecture and the dynamic properties of the materials used in the PWA. This paper focuses on failure envelopes for dynamic failures in the solder. PWA flexural strain and strain rate are used as damage metrics to quantify the solder durability and to develop the fatigue failure envelopes. Failure maps are shown to be a convenient method for identifying these competing failure envelopes and their transition zones. This *failure map* is an ideal tool for comparing the performance of different surface mount packages under dynamic loading conditions. Future work will concentrate on demonstrating the use of the proposed technique as a tool to rank the durability of different material systems. PWA flexural strain and strain rate will be used to compare the durability of Sn-Pb PWAs with Sn-Ag-Cu PWAs. Similarly, the proposed technique will be used to compare the durability of unaged PWAs with that of aged PWAs, under dynamic loading conditions. Dynamic FEA will be used to make the damage model constants independent of specimen geometry, and dependent only on the dynamic material properties of the solder. Additional data points will be presented to increase the confidence in the damage constants.

Acknowledgements

This work is sponsored by members of the CALCE Electronics Products and Systems Consortium at the University of Maryland. Discussions with Ed Tinsley of Dell, Inc. and Simon Prakash of Apple Computer, Inc., are also gratefully acknowledged.

Chapter 4: Solder Fatigue Model*

In this chapter, the test specimens are analyzed with 3D finite element analysis and rate-dependent solder properties, to quantify the fatigue failure envelopes of the solder. This provides failure envelopes in terms of mechanistic parameters, rather than empirical ones (as was done in Chapter 3). As observed in Chapter 3, for the test conditions of this study, the solder durability is strongly dependent on PWA strain and weakly dependent on PWA strain rate. It is hypothesized that the weak rate-dependence of solder durability is due to the competing effects of strain-rate hardening and exhaustion of ductility. The ratio of plastic strain to the failure strain is proposed as a non-empirical, mechanistic metric to quantify the solder durability and fatigue curves. The original draft of this chapter is a journal paper that is currently submitted for peer-review to IEEE Components and Packaging Technologies.

Mechanistic Insights Into The Rate-Dependent Failure Envelopes of Solder Interconnects in Surface Mount Assemblies.

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This paper characterizes the fatigue failure envelopes for solder damage in Printed Wiring Assemblies (PWAs) subjected to dynamic flexural loading. For a given PWA flexural strain, an increase in the PWA flexural strain rate decreases the plastic strain due

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to strain rate hardening. The solder failure strain also decreases due to exhaustion of ductility. This study explores the effects of these two competing mechanisms on the rate-dependent durability of the solder interconnect. The ratio of solder plastic strain to its failure strain is proposed as a metric to quantify the rate-dependent durability of the solder interconnect. Explicit transient non-linear finite element analysis (FEA) is used to derive damage constants that are independent of the specimen geometry and dependent only on solder material properties. A case study, using a simple PWA specimen containing a single area array Sn37Pb Ball Grid Array (BGA) component, is presented to demonstrate the proposed approach.

Keywords: drop test, four point bend, BGA, solder failure, strain rate dependence, durability model

Nomenclature

a, b : Mechanistic durability constants for solder (-)

p, q : Failure strain constants for solder (-)

c, b_1, c_1 : Empirical durability model constants (-)

ε_p : Plastic strain in the solder (-)

ε_f : Failure strain of the solder (-)

ε_{PWA} : PWA flexural strain (-)

$\dot{\varepsilon}_p$: Solder plastic strain rate (sec^{-1})

$\dot{\varepsilon}_0$: Quasi-static PWA strain rate (sec^{-1})

$\dot{\varepsilon}_{PWA}$: PWA flexural strain rate (sec^{-1})

N_f : Average number of cycles to failure (-)

4.1. Introduction

Dynamic loading plays a crucial role in the durability of solder interconnects in Printed Wiring Assemblies (PWAs). The trend toward decreasing solder ball diameter, pad diameter and I/O pitch makes the interconnect more susceptible to failure. This is often true for PWAs in portable electronic devices that are often subjected to dynamic loading during mechanical handling, accidental misuse and/or shipping (transportation). Hence board level solder joint reliability under dynamic loading conditions is of critical concern to the microelectronics industry.

Board level tests are usually conducted on a sub-assembly drop testing machine based on a JEDEC Standard [9]. Recent work by Seah, et al. [109] proved that in surface mount assemblies on compliant organic PWBs, solder ball damage due to PWA flexure is much greater than that caused by inertial loading or by stress wave propagation. Thus, PWA flexural strain and strain rate can be used as the primary metrics to quantify damage accumulation rates. Hence, bend tests can be used in lieu of drop tests to focus the study on PWA flexural strain and strain rate and on its effect on interconnect durability [73].

Much work has been done to develop durability models for solder interconnects under dynamic loading conditions. Empirical models have been developed to quantify durability as a function of PWA strain [110][117], PWA displacement [111], and PWA strain rate [10]. All of the above mentioned damage metrics are structure-specific. Hence,

the damage constants are unique to the tested PWA geometry. FEA can be used to make the damage metrics relatively independent of PWA geometry, and solely dependent on the material properties at the failure site.

FEA with rate-independent material properties has been used to quantify durability in terms of solder stress [118] or solder strain [113]. Many researchers have also used rate-dependent material properties to quantify durability. Zhu and Marcinkiewicz [119] explored the possibility of using von-Mises strain and plastic strain as the damage metric for solders in PWAs subjected to drop tests. The von-Mises strain showed recoverable deformation, while the plastic strain showed steady accumulation during the post-impact vibration. Chong, et al. [120] used plastic strain as the damage metric and showed that plastic strain increases with time as the PWA vibrates. Chea and Pang [121] used plastic strain in the solder to quantify damage in PWAs subjected to four point bend and drop tests. Gu and Jin [63] used peeling stress in the solder as the damage criterion while optimizing the design of RF land grid array packages. Shah and Mello [69] developed failure envelopes based on normal and shear forces on the solder ball to quantify the durability of the interconnects.

This paper seeks to extend the excellent work done by the researchers mentioned above. The ratio of solder plastic strain to its failure strain is proposed as a metric to quantify the rate-dependent durability of the solder interconnect. The proposed damage metric is motivated by mechanistic considerations. For a given load amplitude, an increase in the loading rate decreases the plastic strain and failure strain in the solder due to strain-rate hardening and exhaustion of ductility, respectively. The hypothesis of the proposed approach is that solder durability depends on the competing effects of these two mechanisms.

This paper is part of an ongoing effort to understand and quantify the damage experienced by solder interconnects during drop testing of PWAs. Earlier work [10][113] by the authors focused on the effect of load amplitude, impact orientation and PWA boundary conditions on interconnect durability. Later publications [73][118] added the effect of loading rate and thermal aging on the durability and failure site of the interconnect. The current study characterizes the rate-dependent durability of the solder in terms of the ratio of the plastic strain to the failure strain.

The paper is arranged in the following format: The details of the FEA are first presented, followed by the FEA transfer functions that relate the plastic strain in the Sn37Pb solder to the PWA flexural strain at different loading rates. The variation of solder failure strain with PWA flexural strain is obtained and the fatigue failure envelope is presented.

4.2. Approach

This paper uses experimental data from a previous study [73] in which a PWA of a simple design was subjected to high-speed four-point bend tests at different loading amplitudes and rates. The specimen design and test results are presented in this paper for the sake of completion. A 3D transient FEA model of the PWA is used to relate the PWA strain to the plastic strain in the solder, for different PWA strain rates. Data available in literature [5] is extrapolated to quantify the decrease in solder failure strain with increasing strain rate. The power law relation is established between the proposed durability metrics ($\varepsilon_p/\varepsilon_f$) obtained from the FEA and cycles to failure, obtained from the experiments. A flow chart of the approach is shown in Figure 4-1. The left hand and right hand sides of the flowchart explain the quantification of strain-rate hardening and exhaustion of ductility, respectively.

The following simplifying approximations have been made in the FEA model: The solder ball is assumed to be isotropic and homogenous, with no internal or external defects. It is assumed that the dynamic constitutive equations of the solder obtained from Split Hopkinson's tests of macroscopic solder specimens can be used to represent the material behavior of the solder balls. In other words, the length scale effects on the material properties of the solder due to its microstructure are ignored. All the materials in the PWA are modeled as isotropic homogenous.

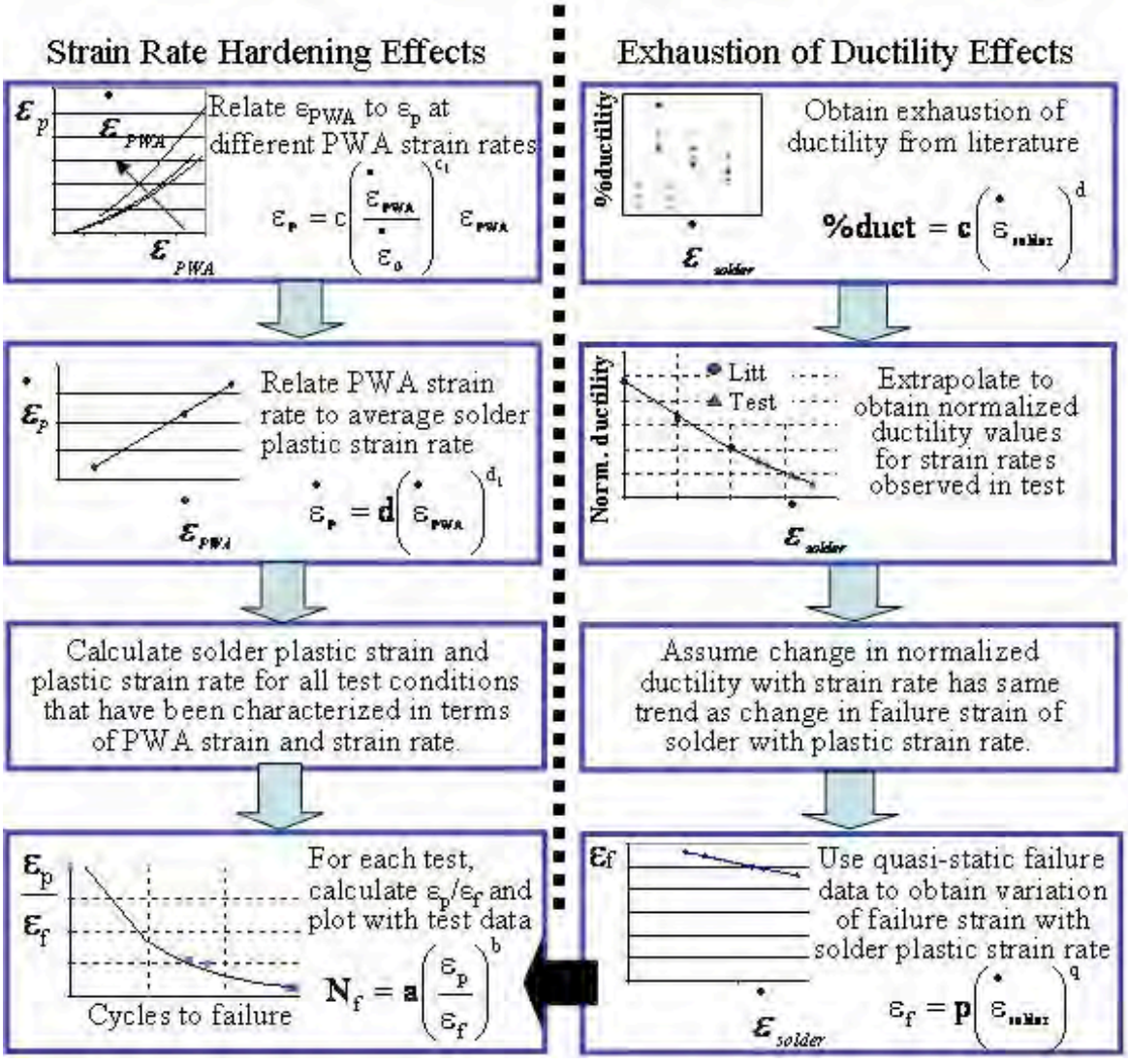

Figure 4-1: Flowchart of the approach

4.3. Specimen design

The specimen (Figure 4-2) is a 256 I/O, full grid PBGA with 0.5mm diameter solder balls on a 1mm pitch. This component is daisy chained for in-situ electrical continuity checks and is mounted at the center of a 140 mm X 101.6 mm X 1.6 mm FR-4 board. The board has one layer of copper (Cu) trace on its surface at the component side to connect the daisy-chained component to the terminals. The percentage coverage of copper on the board surface is negligible. Therefore, the material properties of the board are predominantly those of the FR4. The solder balls are made of Sn37Pb eutectic solder, which is solder mask defined on the component side, and non-solder mask defined on the board side. The pad finishes on the board and component side consists of an Organic Solderability Preservative (OSP) and Sn15Pb, respectively. A strain gage is attached to the board near the corner of the component (the site of maximum curvature) to measure the flexural strain and the flexural strain rate. An electrical continuity tests is performed on each daisy-chained component to detect any opens or shorts. The purpose of choosing this simple specimen design is to allow an in-depth study of the drop event, without making the analysis too complex. Sn37Pb solder also makes a better baseline sample because it is a well-studied material with numerous publications [5][116]about its behavior under high strain rate loading conditions. The specimens are tested in as-soldered condition without any additional aging. Details of the test matrix, test setup, and the specimen can be found in an earlier publication [73].

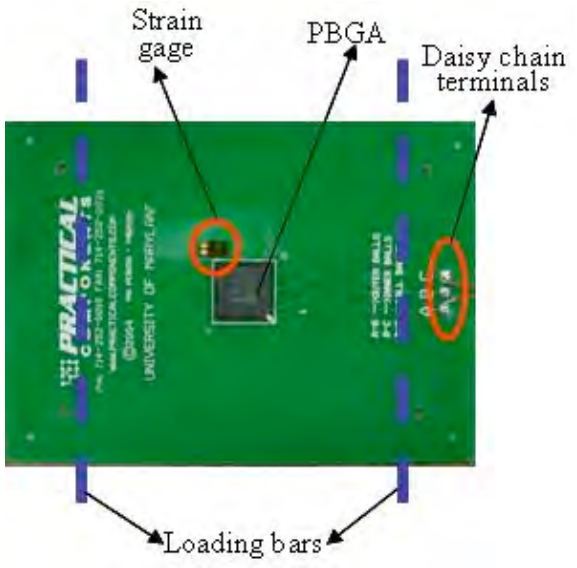

Figure 4-2: Specimen configuration

4.4. Test results

A brief summary of the test results is presented in Table 4-1. Since the focus of this study is on solder durability, failures in the FR4/Cu-trace are not addressed here. PWA flexural strain and PWA flexural strain rate are used as the empirical durability metrics. Non-linear transient finite element analysis (FEA) with an explicit solver is used to deduce the solder plastic strain for each test condition.

Table 4-1: Experimental results

#	PWA strain (-)	PWA strain rate (sec^{-1})	Cycles to failure		Failure Site
			Test 1	Test 2	
1	2.5E-3	2.5E-3	639	1000	Solder
2	5.0E-3	4.9E-3	31	39	Solder
3	9.4E-3	2.5E-3	1	1	Solder
4	2.5E-3	1.2E-1	691	651	Solder
5	2.5E-3	2.5E-2	608	804	Solder
6	4.9E-3	3.8E-2	71	50	Solder
7	5.6E-3	2.2E0	7	5	FR4/ Cu-trace
8	9.4E-3	9.5E-2	5	3	FR4/ Cu-trace
9	1.2E-2	1.2E-1	2	2	FR4/ Cu-trace

4.5. FEA Model

An explicit transient non-linear finite element model is generated using a commercially available software to obtain the transfer function at different values of PWA strain rate. A 3-D strip model of the PWA is created, with a thickness of one pitch. 8-noded hexahedral elements are used to model the specimen. As shown in Figure 4-3, only one half length of the PWA is modeled because the test coupon is symmetric and the four point loading restricts its structural response to the first mode [73]. Symmetry boundary conditions are applied to the vertical axis in the center of the component. The copper trace connections between the solder balls and the copper trace that connects the daisy-chained component to the terminals are ignored in the FEA model (Figure 4-4).

The intermetallic compound (IMC) layer between the solder and the copper pad is also ignored. All materials are modeled with isotropic homogenous properties.

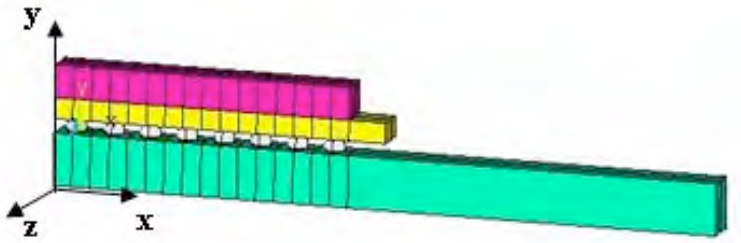

Figure 4-3: FEA model with symmetric boundary conditions on the vertical axis at center of model

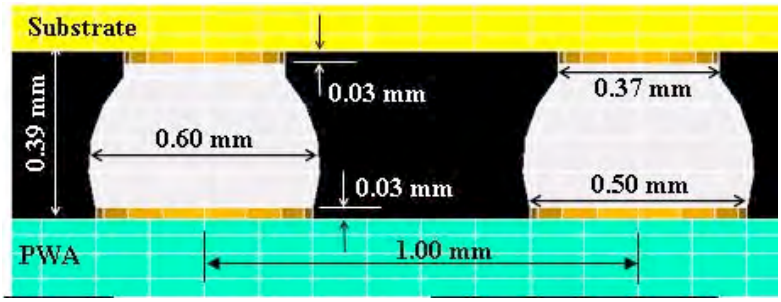

Figure 4-4: FEA model of the solder interconnect

The mesh has 34992 elements and 40962 nodes, and is scaled to provide maximum mesh density at regions of high stress gradients, for example at the solder/Cu pad interface, and at the Cu pad/PWA interface. The solder and the copper pad are modeled with elastic-plastic properties, while all the other materials are modeled as linear elastic. The linear elastic properties of all the materials in the PWA are listed first (Table 4-2), followed by the rate-independent inelastic properties of copper (Table 4-3) and solder (Table 4-4). Since the tests were conducted over a large range of strain-rates, the solder has been modeled with rate-dependent properties obtained from literature [116]. The variation of solder yield stress with strain rate is listed in Table 4-5. Figure 4-5 shows the rate-dependent stress-strain curves of the Sn37Pb solder.

Table 4-2: Linear elastic material properties of the PWA

Material	**Elastic modulus (GPa)**	**Poisson's ratio (-)**	**Density (kg/m^3)**
FR4	17.2	0.39	1000
Overmold	15.8	0.25	1900
Substrate	22	0.3	1000
Copper	120	0.34	8930
Solder	29.9	0.35	8400

Table 4-3: Bilinear material properties of copper

Yield Stress (MPa)	**Post-yield Modulus (GPa)**
24	12

Table 4-4: Quasi-static inelastic material properties of solder

Stress (MPa)	**Strain (-)**
0.00	0.0
15.10	4.8E-4
15.59	5.0E-4
17.32	5.9E-4
19.05	7.2E-4
20.78	8.8E-4
22.52	1.0E-3
24.25	1.4E-3
25.98	1.7E-3
31.18	3.6E-3
34.64	5.9E-3
43.30	1.8E-2
51.96	4.85E-2
60.62	1.12E-1
69.28	2.36E-1
77.94	4.54E-1
86.60	8.16E-1

Table 4-5: Dynamic material properties of solder

Yield Stress (MPa)	29.9	35.8	41.8	50.8	62.8	74.7
Strain rate (-)	1E-3	1E-2	1E-1	1E0	1E1	1E2

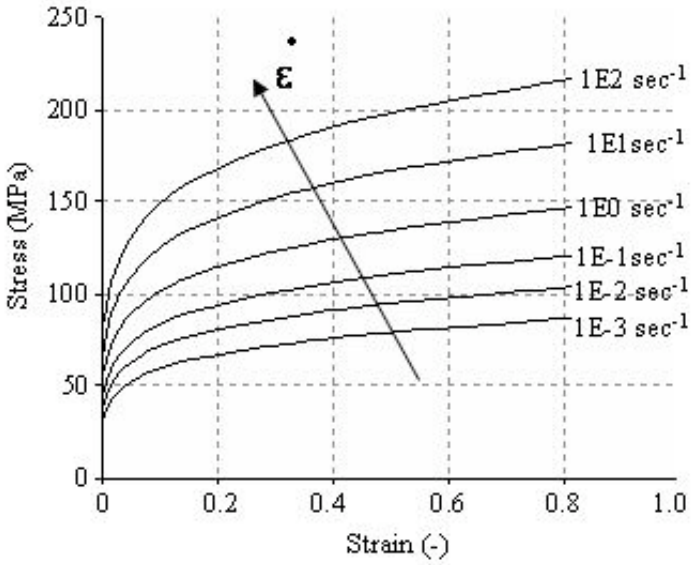

Figure 4-5: Rate-dependent properties of the Sn37Pb solder

FEA simulation at different loading rates shows that the region of maximum plastic strain is in the solder neck on the component side of the outermost solder ball. Figure 4-6 shows a plot of the distribution of plastic strains in the outer most solder ball. This is in very good agreement with the test data, where the failure is in the neck of the outermost joint, on the component side (Figure 4-7). Hence, the results of the FEA can be viewed with a high degree of confidence.

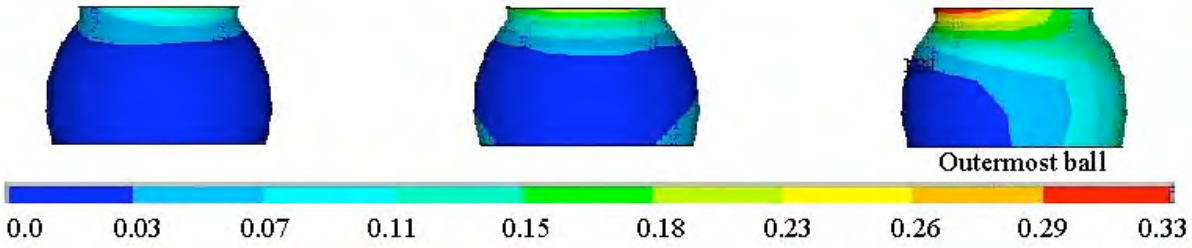

Figure 4-6: Distribution of plastic strain in the solder balls at PWA strain and strain rate of 8E-3 and 1E-2 sec-1, respectively.

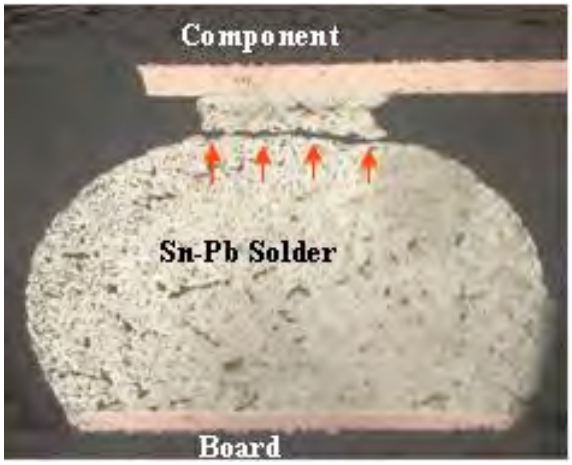

Figure 4-7: Cross-sectioning image of the outer most solder joint shows failure in the solder neck [73]

The FEA transfer function is obtained by plotting the average equivalent plastic strain in the solder with respect to the PWA flexural strain averaged over the region of the strain gage. The averaging of the solder equivalent plastic strain decreases the dependence of the results on meshing approximation. The average technique is used extensively in the field of solder durability, but there are no standard averaging schemes. The averaging requires a trade-off between losing data resolution across a large region versus numerical errors in a very small region. The authors have chosen *a single row* of elements, spread over 5% of the solder cross-sectional area in the region of maximum plastic strain, to provide a quantitative estimate of strains in the region. Figure 4-8 and Figure 4-9 show the cross-sectional area (which comprises of two elements) over which the plastic strains are averaged. The results of this study must be viewed within the context of this averaging scheme.

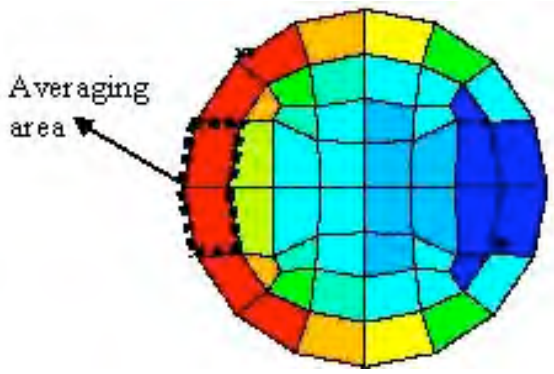

Figure 4-8: Top view of the solder neck. The averaging area is about 5% of the total cross-sectional area.

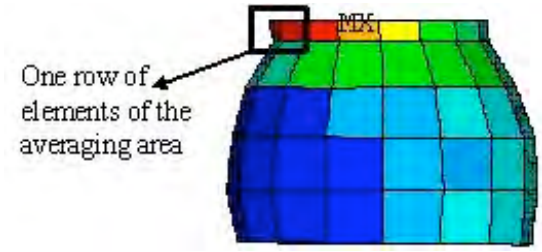

Figure 4-9: Front view of the solder neck. The averaging area comprises of a single row of two elements.

4.6. Effect of Strain Rate Hardening

The solder plastic strain increases monotonically with PWA flexural strain for all cases. For the same PWA flexure, the plastic strain in the solder decreases with increasing PWA strain rate. This is because the solder undergoes strain-rate hardening, which increases its yield stress and hence, delays the onset of plastic strain. Figure 4-10 shows the plot of average solder plastic strain rate with respect to average PWA strain rate. The average strain rate is obtained by dividing the strain amplitude by the loading time.

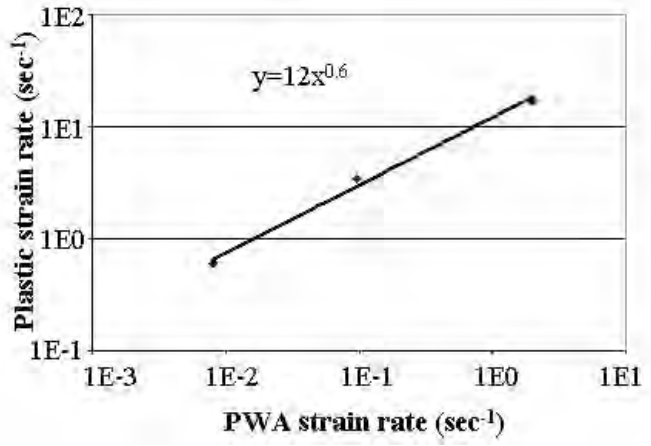

Figure 4-10: Log-log plot of average solder strain rate to the average PWA flexural strain rate

The curves shown in Figure 4-11 are the transfer functions needed to correlate PWA flexural strain to the average plastic strain at the failure site, for different values of PWA strain rates and corresponding solder plastic strain rates.

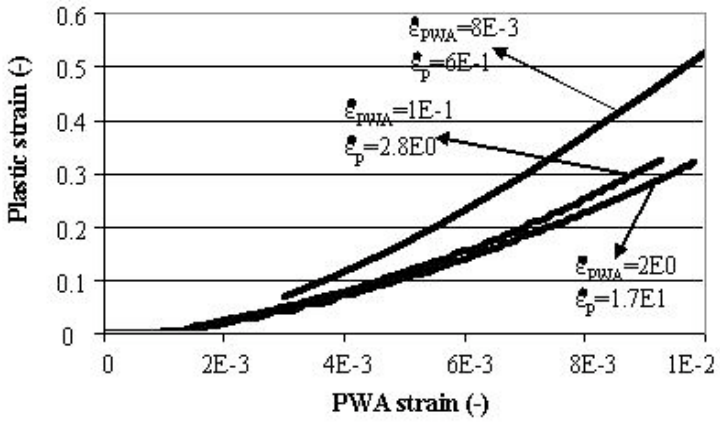

Figure 4-11: FEA transfer function for different PWA strain rates and solder plastic strain rates.

As proposed by the authors in an earlier study [73], the transfer function in Figure 4-11 can be approximated as a power law relationship (Eq. 4-1). The values of the constants are listed in Table 4-6.

$$\varepsilon_p = f\left(\dot{\varepsilon}_{PWA}, \varepsilon_{PWA}\right) = C\left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-c_1} \left(\varepsilon_{PWA}\right)^{b_1} \quad (4\text{-}1)$$

Table 4-6: FEA transfer function constants

C	c_1	b_1
7928	0.09	2.05

Thus, the test data, obtained in terms of PWA strain and strain rate (Table 4-1) can be represented in terms of solder plastic strain and solder plastic strain rate Table 4-7.

4.7. Effect of Ductility Exhaustion

The failure strain of the solder is rate-dependent due to the exhaustion of ductility. Plumbridge and Gagg [5] conducted tensile tests at 20 ºC on Sn37Pb solders at strain rates ranging from 1E-3 to 1E-1 sec^{-1} and showed that the failure strain of the solder decreases monotonically with increasing strain rate. Here, we make a simplifying approximation that the failure strain follows the same slope at higher strain rates. On the basis of this approximation, the data published by Plumbridge and Gagg [5] is extrapolated to a strain rate of 1E1 sec^{-1} and normalized with respect to the quasi-static solder strain rate obtained from this study. For the solder strain rates of interest, the plot of normalized failure strain with solder strain rate follows a power law equation, as shown in Figure 4-12.

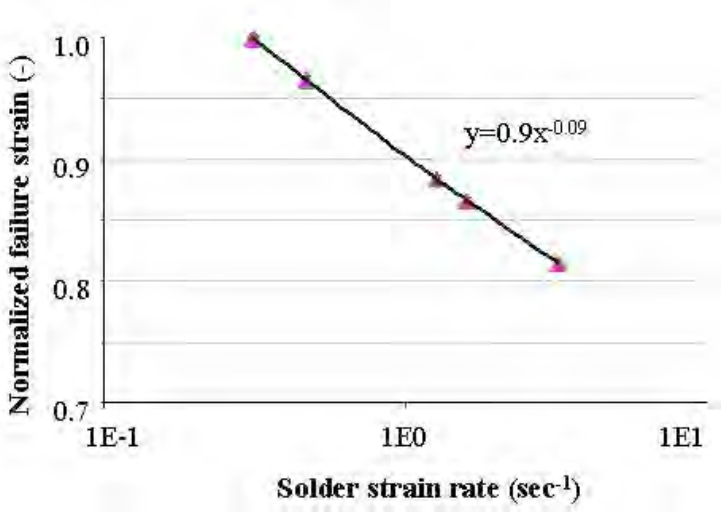

Figure 4-12: Log-normal plot of normalized failure strain versus solder strain rate. Estimated from [5].

The failure strain obtained from the macro-scale samples [5] may not be directly applicable for solder interconnects due to a variety of reasons, including length scale effects and microstructure. For the purpose of this study, we make a simplifying approximation that the failure strain of the micron-scale solder used in this study follows the trend reported in Figure 4-12. Further testing is needed to characterize the variation of failure strain with strain rate at the microscale. From the numerical simulations of the test specimens used in this study, the solder undergoes overstress failure at a plastic strain value of 5.93E-1 under quasi-static loading conditions. Using this data and the figure shown above, we can now estimate the solder failure strain for the strain rates of interest in this study. As expected, failure strain decreases monotonically with increasing solder plastic strain rate. As shown in Figure 4-13, the relationship can be approximated as a power law (Eq. 4-2).

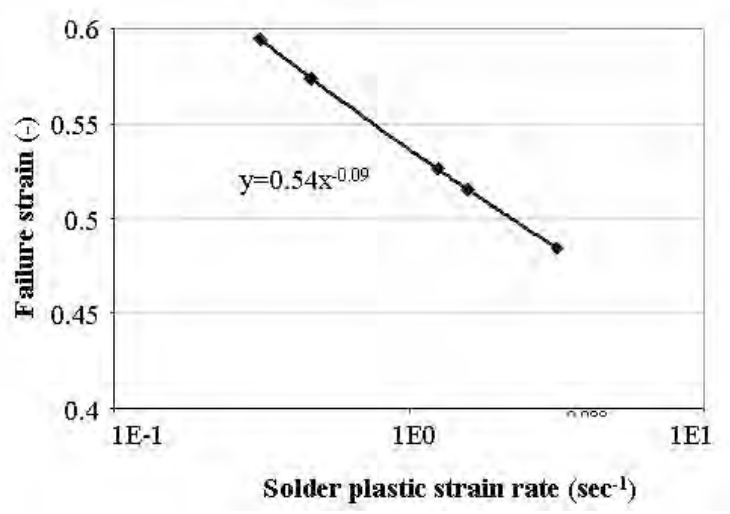

Figure 4-13: Log-normal plot of variation of failure strain versus solder plastic strain rate

$$\varepsilon_f = p\left(\dot{\varepsilon}_p\right)^{-q} \qquad (4\text{-}2)$$

where p = 0.5 and q = 0.09, from the data presented in Figure 4-13.

4.8. Solder Fatigue Curves

The *rate-dependent* durability of the solder is presented in terms of the ratio of the plastic strain to the failure strain. In other words,

$$\frac{\varepsilon_p}{\varepsilon_f} = a\left(N_f\right)^{-b} \qquad (4\text{-}3)$$

So, for a given PWA flexural strain, the solder plastic strain and the failure strain, both decrease with increasing loading rate. The decrease in the plastic strain due to strain-rate hardening decreases the damage in the solder, thus increasing its durability. But the decrease in the failure strain due to ductility exhaustion in the solder has the effect of decreasing its durability. To fully understand the competing effects of these two phenomena, let us look at the available data in its entirety. Table 4-7 lists the durability of the solder in terms of the test parameters (PWA strain and strain rate), and mechanistic

parameters (plastic strain and failure strain). Let us consider the solder response to a constant PWA strain of 2.5E-3 and different PWA strain rates (Test numbers 3, 4, and 6 from Table 4-7). It can be seen that as the PWA strain rate increases, the solder plastic strain and the failure strain decrease monotonically, but the ratio of the plastic strain to the failure strain shows a monotonic increase (Figure 4-14). This leads to a decrease in the durability of the solder

Table 4-7: Durability in terms of empirical [73] and mechanistic parameters

Test num	PWA strain (-)	PWA strain rate (sec^{-1})	Solder plastic strain (-)	Solder plastic strain rate (sec^{-1})	Solder failure strain (-)	Cycles to failure	
						A	B
1	5.0E-3	4.9E-3	1.56E-1	4.66E-1	5.72E-1	31	39
2	4.9E-3	3.8E-2	1.22E-1	1.59E0	5.13E-1	50	71
3	2.5E-3	2.5E-2	3.30E-2	1.25E0	5.24E-1	608	804
4	2.5E-3	2.5E-3	3.58E-2	3.15E-1	5.92E-1	639	1000
5	9.4E-3	2.5E-3	5.93E-1	3.10E-1	5.93E-1	1	1
6	2.5E-3	1.2E-1	3.14E-2	3.19E0	4.83E-1	651	691

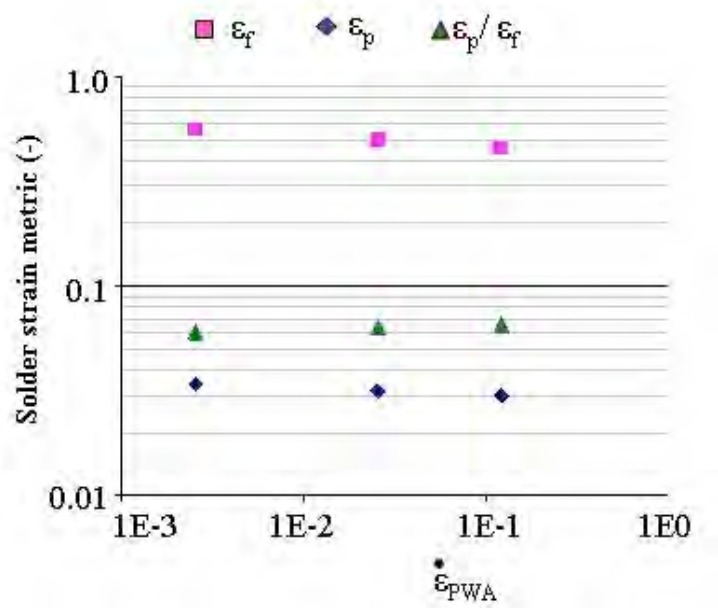

Figure 4-14: Effect of loading rate on solder plastic strain, failure strain, and ratio of the two.

For the loading rates observed in this study, the failure strain is more rate-dependent than the plastic strain. In other words, exhaustion of ductility dominates, and the durability decreases with increasing PWA strain rate. Combining the results of the FEA with test data, we can now plot a fatigue curve for the solder (Figure 4-15). The solder durability is seen to follow a power law relation with the ratio of plastic strain to failure strain. The values of the *rate-dependent* constants of the durability model (Eq. 4-3) are listed in Table 4-8.

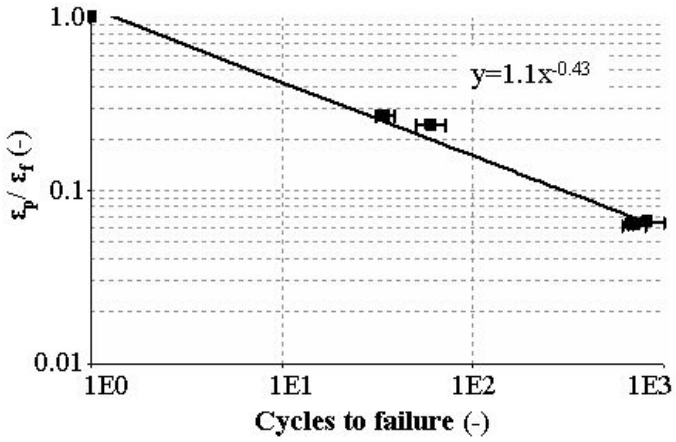

Figure 4-15: Fatigue curve for dynamic loading of solder

Table 4-8: Rate-dependent durability constants for solder

a	b
1.13	0.43

4.9. Discussion

It has been shown in earlier studies [58][42][47]that the durability of the interconnect decreases with increasing loading rate during drop testing and high speed bending of PWAs. This study provides a mechanistic perspective into solder durability at plastic strain rates ranging from 1E-1 to 1E1 sec^{-1}. These strain rates are too high for creep dominated deformation and too low for damage due to adiabatic heating. It is proposed that the variation of durability with strain rate depends on the competing effects of strain rate hardening and ductility exhaustion. The ratio of plastic strain to failure strain is proposed as a metric to quantify durability of the solder for the strain rates observed in this study.

The proposed durability model is a modification of the Coffin-Manson relationship. Another modified Coffin-Manson model, proposed by Eckel [104], can be used to relate

the durability of the solder to loading frequency. Several studies, including the ones by Shi, et al. [105] and Kanchanomai, et al. [106] have used Eckels model to describe solder durability at various loading frequencies. One of the limitations of Eckel's model is that the value of the exponent is dependent on the strain amplitude. The effect of frequency is higher when the strain range is higher and when the elastic modulus is lower. In comparison, the durability model proposed in this study is based on mechanistic concepts. Further work is needed to collect additional data to increase the robustness of the model constants, and make it applicable to a wider range of strain rates.

For the strain rates observed in this study, the durability of the solder varies strongly with solder plastic strain, and very weakly with solder plastic strain rate. This can be better understood by substituting Eq. 4-2 into Eq. 4-3, and re-presenting the master-curve shown in Figure 4-15 by a family of Coffin-Manson curves, each corresponding to a different solder plastic strain rate (Figure 4-16). The values of the Coffin-Manson durability constants for each level of plastic strain rate are listed in Table 4-9. For a solder plastic strain rate of 1E0 sec^{-1}, a 100% increase in the solder plastic strain from 0.1 to 0.2 decreases the durability by almost 83%. On the other hand, at a solder plastic strain of 0.1, an increase in the plastic strain rate by one order of magnitude from 1E0 $sec^{-1}$to 1E1 sec^{-1} changes the durability by approximately 40%.

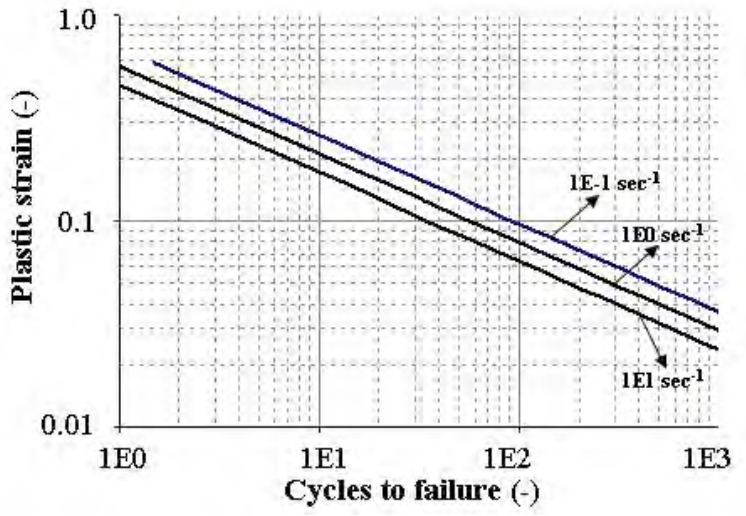

Figure 4-16: Family of Coffin-Manson curves for Sn37Pb solder at different plastic strain rates.

Table 4-9: Coffin-Manson Model constants for solder

Plastic strain rate (sec^{-1})	a	b
1E-1	0.7	0.43
1E0	0.57	0.43
1E1	0.46	0.43

The rate-dependence of the solder is negligible at the PWA strain rates (1E-3 to 1E-1) and solder strain rates (1E-1 to 1E1 sec^{-1}) observed in this study, which is could be why the durability shows a weak dependence on strain rate. This could be attributed to changes in the deformation mechanisms at the microstructural level at these strain rates that can affect the rate-dependent material properties of the solder. For example: below a transitional strain rate of 1E-3 sec^{-1}, Sn37Pb solder deforms due to wedge cracking induced by grain boundary sliding. The solder deforms due to cavitation on the colony boundaries when the strain rate is above the transitional strain rate [100]. Other studies have also reported that plastic deformation is dominated by dislocation motion at quasi-

static loading rates, and by twinning at high strain rates [101][102]. This change in the deformation mechanism has been attributed to the strain rate hardening of the solder because it takes a higher value of the flow stress for nucleation of twins than dislocation motion [103]. Analysis at the microstructural level, which is beyond the scope of this study, can provide further insight into the behavior of the solder at the strain rates of interest.

Depending on the geometry and material properties of the PWA, solder interconnects subjected to JEDEC board level drop tests [9] can experience strain rates close to those presented in this study and higher. Researchers have reported that solder interconnects can experience strain rates as high as 1E3 sec^{-1} during product level drop tests [122]. Hence, further work also needs to be done to increase the range of strain rates to include 1E3 sec^{-1}.

4.10. Conclusions and Future Work

A mechanistic insight is offered to explain the dependence of solder durability on loading rate. For the test coupons used in this study, solder plastic strain varies strongly with the PWA flexural strain, and weakly with the PWA flexural strain rate. Solder failure strain is found to decrease exponentially with increasing solder strain rate. In the range of strain rates observed in this study, the effect of strain rate hardening was weaker than that of ductility exhaustion. Hence, the damage metric, the ratio of solder plastic strain to solder failure strain, increased with increasing PWA flexural strain rate. Durability was shown to decrease exponentially with increasing values of the damage metric. For the loading conditions used in this study, solder durability was strongly dependent on solder plastic strain, and weakly dependent on solder plastic strain rate.

Future work needs to focus on characterizing the variation of failure strain with

strain rate for micron-scale solders. Work also needs to be done to increase the robustness of the model constants, and make it applicable to a wider range of strain rates.

Acknowledgements

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Chapter 5: Intermetallic Fracture Model[#]

This chapter presents mechanistic insights into the failure at the interface between the two IMC layers ($Au0_{.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4) of a Sn37Pb/ENIG interconnect subjected to dynamic flexural loading. The original draft of this chapter is a journal paper that is currently submitted for peer-review in Engineering Fracture Mechanics. The ratio of the interfacial strain energy release rate to the interfacial fracture toughness is proposed as a mechanistic parameter to characterize the failure envelopes, instead of empirical metrics like PWA strain and strain rate, or drop height. For the test samples and test conditions used in this study, the non-planarity of the interface between the two IMC layers has a significant effect on the stress field at the crack tip. For a given PWA geometry and loading condition, the strain energy release rate at the interface is shown to increase with decreasing interfacial roughness, thus increasing the chances of interfacial fracture. The proposed mechanistic durability metrics provide a suitable framework to quantify the durability of the interface, and have a power law relationship to the average cycles to failure obtained from the test data

Failures in Intermetallic Layers of Solder Interconnects with ENIG Plating

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This study presents mechanistic insights into the interfacial failure between two

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intermetallic layers ($Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4) of a Sn37Pb solder interconnect on a ENIG PWA, when subjected to dynamic flexural loading. Instead of empirical metrics (for example: PWA strain, drop height), the magnitude of the interfacial strain energy release rate (G^t) normalized with respect to the interfacial fracture toughness (G_c) is used as a mechanistic parameter to characterize the failure envelopes. The effect of non-planarity of the interface between the two intermetallic layers on the stress field at the crack tip is also quantified. The applicability of the proposed failure metrics for quantifying durability under dynamic loading (for example: drop testing) is discussed.

5.1. Introduction

Fracture at the interface of the intermetallic compound (IMC) of solder interconnects can have a significant effect on the durability of Printed Wiring Assemblies (PWAs). This is often true for PWAs with Electroless Nickel Immersion Gold (ENIG) plating and/or PWAs subjected to thermal aging for prolonged periods of time. This failure mechanism is especially relevant under dynamic flexural loading of the PWAs due to vibration and/or repetitive impacts during mechanical handling, accidental misuse and shipping (transportation). Hence, understanding of interfacial fracture at the IMC layer under flexural loading conditions is of critical concern to the microelectronics industry.

Tests conducted by Luhua and Pang [5] showed that even within the IMC layer, the failure site can change with thermal aging (from the interface between the solder and the IMC, to the interface between the two IMC layers, to the interface between the IMC and the copper pad). In solder interconnects with Electroless Nickel Immersion gold (ENIG) finish, the most commonly reported failure site is in the thin black Ni(p) layer between the nickel plating and the Ni_3Sn_4 IMC [5]. Other failure sites observed in interconnects

with ENIG finish include the interface between the $Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4 IMC layers [86][87][88].

Failure in the intermetallic layer has been characterized in terms of empirical metrics, like drop height of a JEDEC board-level drop-tester [5][43][54], or PWA flexural strain and strain rate [86]. In all these studies, durability shows a monotonic decrease with increasing values of the drop severity, as measured by the empirical metric(s). The fracture toughness of the IMC layer has been shown to decrease with loading rate [3] and with thermal aging [5].

FEA has been used by several authors to make the damage metrics less sensitive to PWA geometry, and more strongly dependent on the properties of the material(s) at the failure site. As an example, durability of the IMC layer has been characterized in terms of the peeling stress at the intermetallic layer [65][66][113] using FEA with *rate-independent* material properties. The stress in the IMC layer is calculated by averaging the stresses in the elements at the solder-copper interface. The morphology of the intermetallic layers was not explicitly considered in this study. Pang and Che [68] used FEA with *rate-dependent* elastic-plastic material properties to characterize IMC durability during JEDEC board level drop tests in terms of von Mises stress at the interface. However, von Mises stress is usually not the best metric for brittle failure mechanisms such as IMC fracture. Yeh and Lai [75] characterized intermetallic failure during high speed ball shear tests in terms of normal and shear forces in the IMC layer. The forces in the IMC layers were estimated with FEA by using 'tiebreak' nodes-to-surface contact at the solder – copper interface. This technique links adjacent meshes and confines the movements of nodes until the bond breaks. Again, these authors did not

explicitly consider the morphology of the IMC layer(s).

In all of these studies, FEA did not provide any insight into the effect of the interfacial morphology on the stress distribution in the IMC layer because the solder – copper interface was assumed to be planar. However, studies by several researchers have shown that the interface between the two IMC layers is jagged and wavy [5][128][129][130]. The severity of waviness of the interfacial morphology depends on the manufacturing processes and solder/plating material systems. The interfacial morphology varies constantly with time, even at room temperature, due to diffusion between the plating material, copper trace and solder [130]. Figure 5-1 shows the variation in the morphology of Cu_6Sn_5/Cu_3Sn interface of a SnAgCu interconnect with Organic Solderability Preservative (OSP) finish, at various conditions of thermal cycling [5]. The non-planar interface increases the effective fracture technique by crack-blunting and crack-shielding mechanisms at the crack tip. Closed-form analytical models, based on interfacial fracture mechanics, can be used to fill this gap.

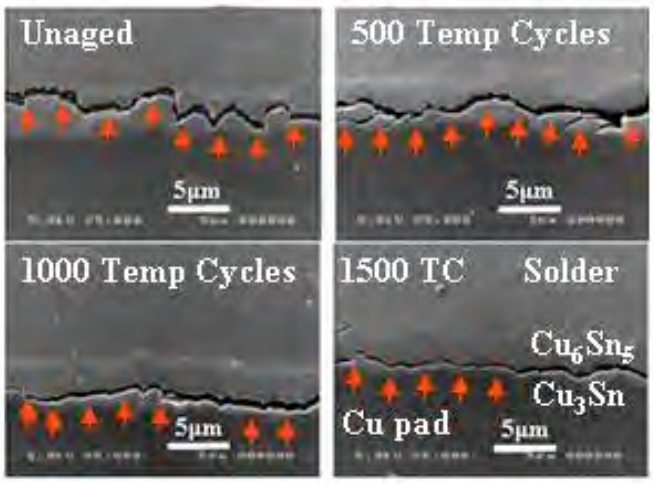

Figure 5-1: Interface of two IMC layers at different thermal aging conditions [5]

This paper seeks to extend the excellent work done by the researchers mentioned

above, by using a simple analytical model based on interfacial fracture mechanics, to develop an understanding of the failure in the interface between the two IMC layers. As a mechanistic interfacial fracture parameter, the energy release rate G^t (normalized by the fracture toughness, G_c), is used to characterize the failure envelopes. This technique is less sensitive to specimen geometry, than empirical metrics like PWA strain and drop height. The proposed durability model is demonstrated on a Sn37Pb/ENIG component subjected to four point bend tests [85][86].

This paper is part of an ongoing effort to understand and quantify the damage experienced by solder interconnects during quasi-static as well as dynamic flexural loading of PWAs. Earlier work by the authors focused on identifying empirical metrics to quantify interconnects durability [113] and to characterize failure site transitions from the solder to other parts of the PWA [73][123]. Recent work [124] established mechanistic, non-empirical, metrics to quantify the rate-dependent durability of the solder. The current study extends the previous work by proposing similar non-empirical metrics for interfacial fracture between the two IMC layers of solder-ENIG interfaces.

The experimental details are first explained in brief, followed by the macroscopic and microscopic analysis of the test data. The subsequent sections discuss the failure envelope and the durability model. Finally, the applications of this technique and future work are discussed.

5.2. Approach

The durability metrics and model proposed in this paper are based on experimental data from a previous study [85][86]in which a PWA of simple design was subjected to

four-point bend tests at different loading amplitudes and rates. The specimen design and test results are summarized in this paper for the sake of completeness. Details can be found in [85][86]. A macroscale to microscale approach is used to develop a mechanistic understanding of the observed failure. The macroscale model uses FEA to relate the PWA flexural strain to the peeling and shear stress in the IMC layer. The microscale model estimates the interfacial strain energy release rate (G^t) and mode mixity (ψ) at the interface between the two IMC layers, based on the stresses obtained from the macroscopic model. This analysis takes into account the non-planar (wavy) morphology of the IMC layer, and provides transfer functions between PWA strain and G^t, for different magnitudes of interfacial waviness. The interfacial fracture toughness (G_c) is evaluated from the test data corresponding to overstress failure (N_f=1) and failure is predicted to occur when the calculated value of G^t reaches G_c. Durability is characterized in terms of the ratio of the interfacial strain energy release rate to the interfacial fracture toughness (G^t/G_c).

The following simplifying approximations have been made: The PWA is assumed to be isotropic and homogenous, with no internal or external defects. The solder and the copper trace are modeled as elastic-plastic materials. All other materials in the PWA, including the IMCs, have linear elastic properties. The wavy interface between the two IMC layers is idealized with a saw-tooth profile. This simplifying assumption can be justified on the basis of the jagged interfacial morphology observed by numerous researchers [5][126][28] .

5.3. Experiment Details

The component is a stacked die Ball Grid Array (BGA) with 160 I/O, 0.44 mm

diameter, 0.8 mm pitch Sn37Pb eutectic solder balls. The pad finishes on the component and board side consist of electrolytic gold over nickel and ENIG, respectively. The PWAs are subjected to isothermal aging at 135ºC for 168 hours. The IMC layer consists of Ni_3Sn_4 on the copper side and $Au_{0.5}Ni_{0.5}Sn_4$, on the solder side. The thickness of the IMC layer is in the range of 2 to 3 microns.

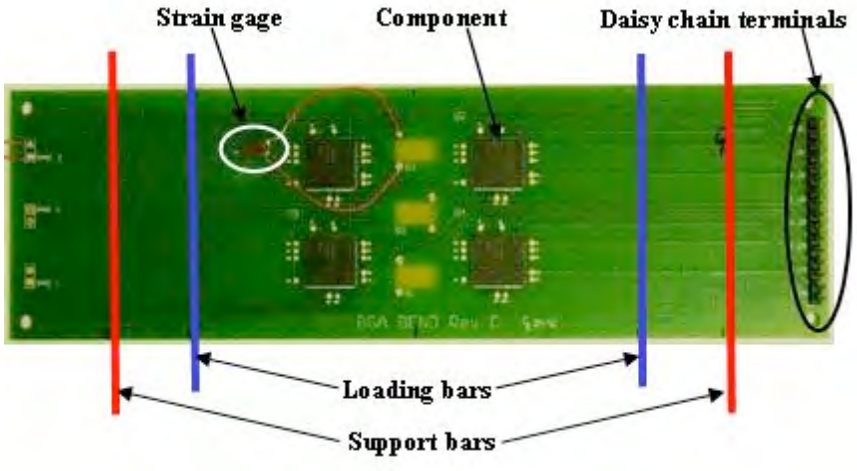

Figure 5-2: PWA specimen, showing location of components and strain gage.

A 350 Ω strain gage with 3.18 mm gage length and 2.54 mm grid width is attached to the board near the corner of the component (Figure 5-2) to measure the flexural strain and the flexural strain rate. The PWA is subjected to 4 point bend tests. The failure site is found to be the interface between the Ni_3Sn_4 and the $Au_{0.5}Ni_{0.5}Sn_4$ IMC layers, and is in agreement with other works in the literature [87][88]. Figure 5-3 shows the location of the crack. Details of the test matrix, test setup, specimen design and test results can be found in an earlier publication [86].

Figure 5-3: Fracture in the IMC layer on the package side of the solder [86][85]

5.4. Macroscale model

A commercially available software is used to generate a 2-D finite element model of the specimen with 4-noded plane stress elements. The elements are given an appropriate out-of-plane thickness to reflect the geometry of the PWA. As shown in Figure 5-4, only one half length of the PWA is modeled because the the specimen is symmetric and its structural response is limited to the symmetric first mode [85][86]. Symmetry boundary conditions are applied about x=0, at the center of the model The copper trace connections are ignored in the FEA model. The IMC layer between the solder and the copper pad is also ignored in the FEA model, but it is addressed later in the microscale model. As mentioned earlier, all materials are modeled with isotropic homogenous properties.

Figure 5-4: 2D model of PWA with symmetric boundary conditions

The mesh has 4126 elements and 4435 nodes, and is scaled to provide maximum mesh density at regions of high stress gradients, for example at the solder/Cu pad

interface, and at the Cu pad/PWA interface (Figure 5-5). The outermost solder ball has a higher mesh density than the inner solder balls because it is the location of the failure site. The solder and copper are modeled as *rate-independent* elastic-plastic materials. All other materials are modeled as linear elastic. The material properties are listed in the section 4.5.

The FEA results show that the maximum stresses are in the outermost interconnect, at the solder neck near the component termination. This is in very good agreement with the test data, where the failure is at the interface of the two IMC layers between the component copper-pad and the solder ball. Hence, the results of the FEA macroscale model can be treated with a reasonable degree of confidence.

The average stress in the intermetallic layer is obtained by dividing the local interconnect force by a local effective load-bearing area. The averaging decreases the dependence of the results on meshing approximation, and requires a trade-off between losing data resolution across a large region versus FEA discretization errors in a very small region. Because of the lack of industry standards for averaging, a logical scheme is chosen in this study. The averaging zone consists of a sufficient number of elements in a single row on each side of the solder-copper interface, near the critical location (in the neck of the solder joint), such that averaging zone is approximately 5% of the solder joint cross-sectional area. Figure 5-5 shows the area (which comprises of four elements: two each from the solder and copper) over which the stresses are averaged. The results of this study must be viewed within the context of this averaging scheme.

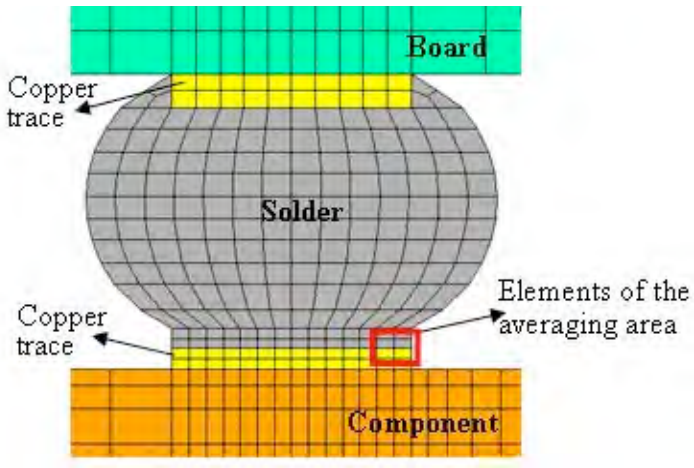

Figure 5-5: The averaging area comprises of two elements each in the solder and the copper trace in the finely meshed outer solder ball.

Figure 5-6 is the FEA transfer function that relates the PWA strain to the peeling and shear stress in the intermetallic layer. The PWA strain is obtained by averaging the longitudinal strains (along the x-axis) over the elements on the board surface located under the foot-print of the strain gage. *However, this macroscale transfer function does not include the the effect of the morphology at the interface between the two IMC layers.* This necessitates the use of the microscale model. The next section describes how the output of the macroscale (FEA) model is used to quantify the stress distribution in the interface.

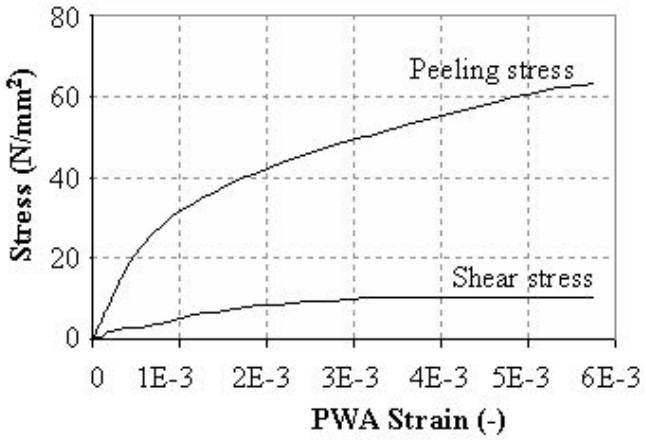

Figure 5-6: Variation of peeling and shear stress in the IMC layer with PWA strain

5.5. Microscale model

The micro-scale model, based on interfacial fracture mechanics, uses the data in Figure 5-6 to assess the durability of the IMC interface. Let us assume the existence of a small crack that initiates at the interface of the $Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4 layers. For purposes of illustration, we assume a crack length of 1% of the diameter of the solder ball at the neck. However, the theory is equally applicable for other assumptions of crack length. The material at this location in the interconnect structure undergoes mixed mode loading. Using simple approximations, the stress distribution is first used to define the stress intensity factors (K) for bulk materials, K_I and K_{II}. Details of this technique are available in the literature [90].

$$K_I = \sigma_p \sqrt{2\pi a} \tag{5-1}$$

$$K_{II} = \tau \sqrt{2\pi a} \tag{5-2}$$

Where,

^{a} is the crack length (assumed here to be 1% of the solder ball diameter at the neck)

σ_p is the peeling stress (mode I) obtained from the FEA macro-model

τ is the shear stress (mode II) obtained from the FEA macro-model

$\Phi = \tan^{-1}\left(\frac{K_{II}}{K_I}\right)$ is the phase angle, indicating the mode mixity in the bulk material

In a homogeneous material, the crack propagates along a trajectory at which K_{II} is zero [91]. However, at a bi-material interface, the trajectory of the crack depends both on the fracture energy and the phase angle [92]. The differences in the material properties of the two IMC layers change the value of the effective mode I and mode II stress intensity factors at the interface. As proposed by Suo and Hutchinson [93], we can now relate the bulk stress intensity factors (K_I and K_{II}) to the interfacial stress intensity factors (K_1 and K_2).

$$K_1 + iK_2 = \left(\frac{1-\alpha}{1-\beta^2}\right)^{\frac{1}{2}} (K_I + iK_{II}) L^{i\varepsilon} e^{i\varpi} \tag{5-3}$$

Where

α and β are the non-dimensional Dundurs parameters [94] that relate the properties of the two materials at the interface.

L is the characteristic length of the stress field, whose value in this study is the thickness of the IMC layer: 3μm

ε is a non-dimensional parameter that represents the oscillatory nature of the stress field at the tip of the interfacial crack [125]

ω is the phase shift in the mode mixity due to the mismatch in the material properties at the interface, whose values are provided in [92]

The stress intensity factor exhibits an oscillatory behavior near the crack tip due to the complex eigen-values obtained as part of the solution of the above equation [98]. The oscillatory field implies that the material in the small zone behind the crack tip interpenetrate even when the crack is subjected to far-field tensile loads. They also imply that K_1 and K_2 are coupled and do not have the same meaning (or units) as the stress intensity factor for homogenous materials [95].

Studies [95][97][99] have indicated that β makes a negligible contribution to the solution of the above equation and to the value of ω. Hence it is a justifiable approximation to take the value of $\beta = 0$. In addition to simplifying the solution, it also decouples interfacial stress intensity factors, K_1 and K_2, thus making them as representative of the stress field as the bulk stress intensity factors, K_I and K_{II}. As shown in Figure 5-1, the material properties of the intermetallic compounds (obtained from literature [96]) can be used to estimate the Dundurs parameters and the phase angle of the interfacial crack.

Table 5-1: Material properties [96] of the IMCs and calculated values of the interfacial parameters

$Au_{0.5}Ni_{0.5}Sn_4$		Ni_3Sn_4		α	$\omega(\alpha, 0)$
E (GPa)	ν (-)	E (GPa)	ν (-)	(-)	(^{o})
133.3	0.33	48	-0.47	-0.47	3.25^0

Figure 5-7 and Figure 5-8 show the variation of the stress intensity factors and the corresponding phase angles with PWA strain, respectively. While the interfacial and bulk stress intensity factors increase monotonically and non-linearly with PWA strain, the mode mixity is almost independent of PWA strain.

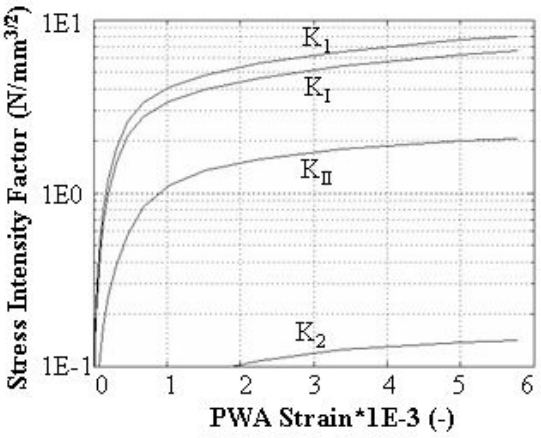

Figure 5-7: Variation of bulk and interfacial Stress Intensity Factor with PWA strain

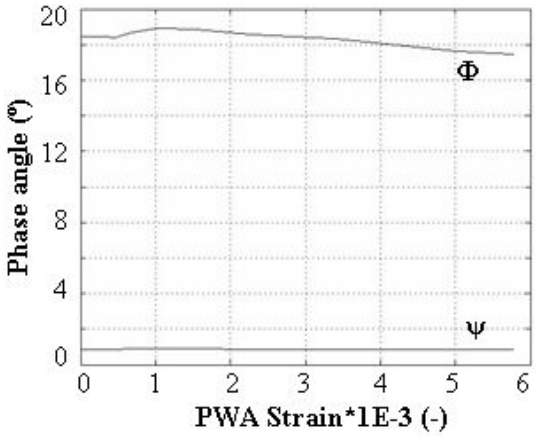

Figure 5-8: Plot of bulk and interfacial phase angle with PWA strain shows almost no variation. Hence the mode mixity can be assumed to be constant

Assuming β=0, the strain energy release rate for the interfacial crack can be calculated using the following equation [97].

$$G = \frac{E_{Au-Ni-Sn} + E_{Ni-Sn}}{2E_{Au-Ni-Sn}E_{NiSn}}\left(K_1^2 + K_2^2\right) \tag{5-4}$$

The above equation assumes a flat interface between the two IMC layers. Let us introduce the effect of non-planarity at the interface. As mentioned in the literature review, the jagged interface between the two IMC layers acts as a crack tip blunting mechanism. In this study, we approximate the waviness of the interface between the IMC

layers with a triangular wave-form. The facet angle (θ) in a wavy IMC interface can be expressed in terms of the pitch (λ) and height (h) of the triangular profile. As proposed by Evans and Hutchinson [91], the effective stress intensity factors for non-planar interfaces is given by

$$K_2^t + iK_1^t = K_2 + iK_1 - f(\xi)e^{i\omega}(K_1 Sin\theta + K_2 Cos\theta) \tag{5-5}$$

where

ξ is the size of the characteristic length on the crack surface, whose value in this study is 1% of the crack length.

f(ξ) is a non-dimensional scaling factor for the stress intensity factors whose value, as obtained from [91], is 0.2

$\theta = -\tan^{-1}\left(\frac{h}{\lambda}\right)$ is the facet angle of the non-planar interface.

K_i^t is the stress intensity factor of the non-planar interface at the i^{th} mode.

The variation in the interfacial strain energy release rate due to the non-planarity of the interface, when compared to a planar interface, is given by the following equation [91].

$$\frac{G^t}{G} = 1 + \frac{(f^2 - 2f)(Sin(\theta) + \tan(\Psi)Cos(\theta))^2}{1 + \tan^2(\Psi)} \tag{5-6}$$

Where

G^t is the strain energy release rate due to crack propagation along a wavy interface and G is the baseline for a smooth, flat interface

$\Psi = \tan^{-1}\left(\frac{K_2^t}{K_1^t}\right)$ is the effective mode mixity at the non-planar interface

Figure 5-9 is a 3D plot of the above equation and shows that G^t/G decreases monotonically with increasing interfacial waviness and phase angle. The changes in the value of h/λ reflect the changes in the interfacial morphology from rough (h/λ = 5) to smooth (h/λ =0). The rough interface clearly provides better resistance to crack propagation, and hence has a lower energy release rate for a given loading condition. For a given level of mode mixity at the interface, the value of the interfacial strain energy release rate decreases with increasing non-planarity. For the same ψ, G^t/G decreases with increasing h/λ, and for a given h/λ, G^t/G decreases with increasing ψ.

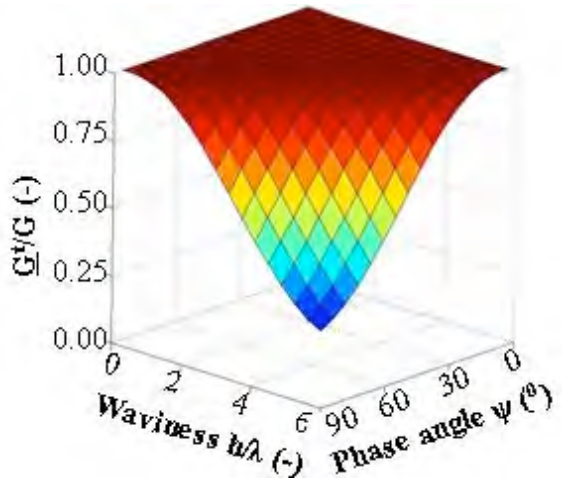

Figure 5-9: 3D plot of the variation of G^t/G with waviness and phase angle

Figure 5-9 can be combined with the equations discussed above to obtain the FEA transfer functions between the interfacial strain energy release rate and PWA strain for different facet angles. The FEA transfer function for different amounts of interfacial waviness is shown in Figure 5-10.

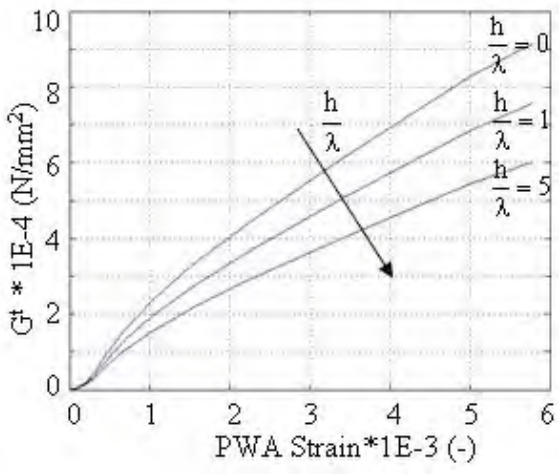

Figure 5-10: FEA transfer function for different interfacial morphologies.

Environmental Scanning Electron Microscopy (ESEM) is used to obtain images of the failure site. (Figure 5-11) and quantify the waviness of the crack (Table 5-2). The average value of h/λ is approximately 0.5, with a variance of 0.13. This corresponds to a θ of approximately 168^0. The waviness often reduces with thermal aging due to diffusion, thus reducing the effective interfacial fracture toughness.

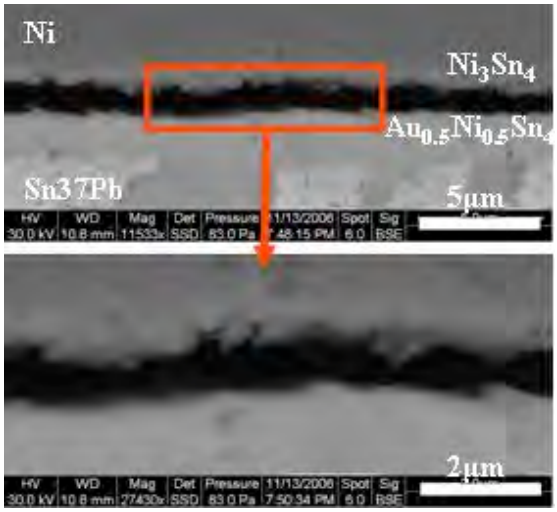

Figure 5-11: Typical ESEM picture of failure site

Table 5-2: Typical values of the interfacial waviness

h (μm)	1.2	0.9	0.8	1.1	1.0	0.8	1.0
λ (μm)	3.1	1.7	1.9	3.0	2.9	1.2	1.6
h/λ (-)	0.39	0.53	0.42	0.37	0.35	0.67	0.63

Failure occurs when G^t reaches a critical value (G_c), which is a material property. The value of G_c may also change with strain rate and with aging, but that is beyond scope of this study. For quasi-static loading, test data shows that the overstress failure of the intermetallic layer occurs at a PWA strain value of 4E-3. The FEA transfer function developed in Figure 5-10 can be used to estimate the G_c value of the interface at that mode mixity. Hence, by combining the FEA plot and the test data, we can obtain the variation of the normalized G^t/G_c as a function of PWA strain, for the facet angle calculated from the fracture site (Figure 5-12).

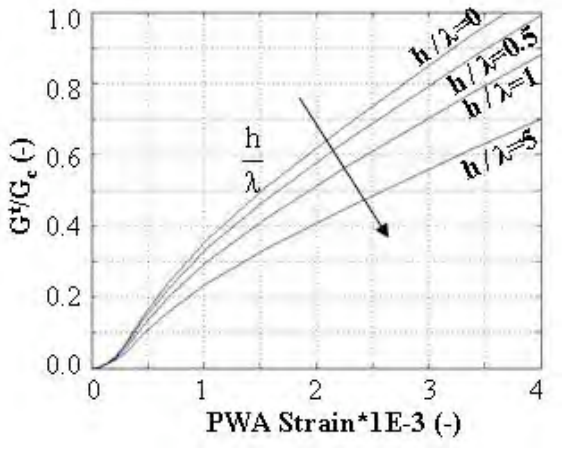

Figure 5-12: Normalized interfacial strain energy release rate as a function of PWA strain, for different morphologies between the IMC layers.

5.6. Durability model

The test results presented in an earlier publication [86] quantified the durability of the IMC interface in terms of the empirical metrics: PWA strain and strain rate. In view of the weak rate-sensitivity revealed in [86], the rate effects are ignored in the present study. In other words, durability is considered to be a function only of the PWA strain, and not of the PWA strain rate. Using the analysis conducted above, we can represent the durability data in terms of the mechanistic parameter: G^t/G_c (Table 5-3)

Table 5-3: Durability in terms of empirical [86] and mechanistic parameters

Board Num	PWA strain (-)	G^t/G_c (-)	Avg cycles to failure (-)
1	3.04E-6	0.82	15.75
2	2.06E-6	0.58	133
3	2.01E-6	0.56	204.25
4	1.06E-6	0.3	1735

The durability of the IMC interface can be related to Gt/Gc with a power law relationship as given below.

$$\frac{G^t}{G} = p(N_f)^q \tag{5-7}$$

where p = 1.64 and q = -0.18 are the durability constants. Figure 5-13 shows the fatigue curve for this IMC interface, in terms of the normalized durability parameter (G^t/G_c).

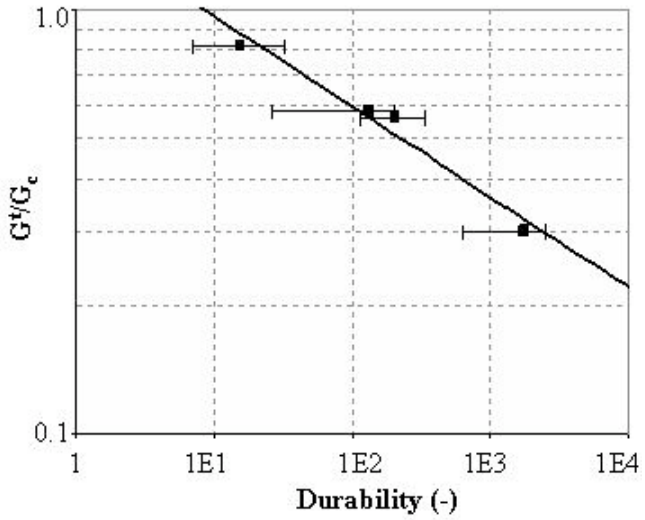

Figure 5-13: Plot of interfacial fatigue curve between the two examined IMCs.

Failure analysis of the tested specimens revealed that the crack path was limited to the interface between the two IMC layers [86]. Normalizing the diameter of the solder neck with the durability for a given loading condition gives us the average crack propagation rate for each loading condition. As shown in the equation below and in Figure 5-14, Gt/Gc follows a power law relation with the average crack propagation rate.

$$\left\langle \frac{da}{dN} \right\rangle = m\left(\frac{G_t}{G}\right)^n \tag{5-8}$$

where m=0.05 and n=4.5 are the constants of the equation for this intermetallic system.

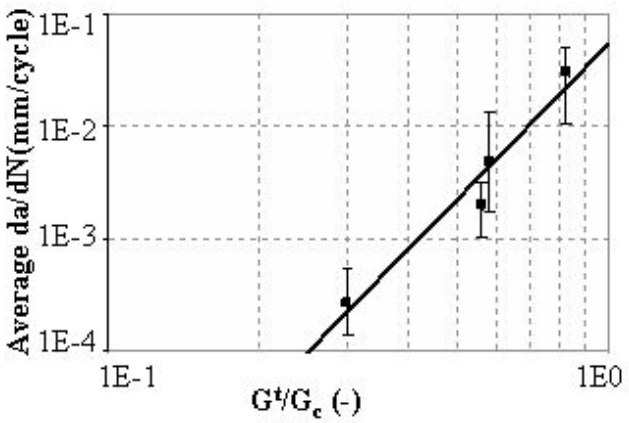

Figure 5-14: Variation of average crack propagation rate with G^t/G_c.

In the above figure, the calculated values of the abscissa (Gt/Gc) are based on the existence of a crack at the IMC interface, and does not take crack propagation into account. Also, the ordinate represents the crack propagation rate averaged over the solder ball neck. The values of m and n must be viewed within the context of this approximation.

5.7. Discussion

The effective strain energy release rate (G^t) has been used in many studies to understand crack propagation in interfaces. Examples include de-cohesion of thin film on substrates [91], delamination of underfill/solder mask interface in electronic packages [107], delamination of epoxy/silicon interfaces[108], among others.

In this study, the crack path was completely through the interface. However, this need not be the case all the time. Mixed-path cracks, where the propagation is through the IMC layers and the solder, have been observed during ball impact tests [75] and uniaxial vibration of solder interconnects [126]. Similar mixed-path cracks have also been observed during decohesion of thin film on brittle substrates [127]. The tendency of the

crack to either remain at the interfaces or deviate away into the bulk material depends on the sign and magnitude of the phase angle [91]. This is specially true for ductile/brittle interfaces. As shown in Figure 5-8, the phase angle at the crack tip depends on the geometry and material properties of the PWA. *Hence, it is possible to design the PWA in a manner in which the crack follows a pre-planned trajectory.*

In general, adhesion between two IMC layers is due to a combination of mechanical interlocking at the interface (analyzed in this study) and interatomic forces across the interface, which is in a state of constant evolution even at room temperature. The diffusion of Sn and Ni leads to a steady change in the thickness and morphology of the two IMC layers. Studies have also shown that the residual stress in the IMC layer, caused by negative volume changes, increases with aging time. The residual stress can change the value of the mode I and mode II stress intensity factors at the site of the micro-crack, and hence the value of the phase angle at the crack tip [91]. This will not only affect the durability of the joint, but also the path of the crack as it could be diverted away or toward the interface.

5.8. Summary and Conclusions

To the best knowledge of the authors, this is the first study that provides a mechanistic perspective on the effect of interfacial morphology on interfacial fracture between the two IMC layers of a solder-ENIG interconnect system.

The durability of the joint has a power law dependence on the normalized energy release rate (Gt/Gc). For a given mixed mode loading condition, Gt/Gc decreases with increasing slope of the facet. This provides a mechanistic explanation as to why a jagged

interface (associated with unaged PWAs or certain reflow profiles) rarely sees failure in the IMC layer during flexural testing, while a relatively smoother interface (associated with aged PWAs) is more prone to interfacial failure.

For the test coupon used in this study, the mode-mixity did not vary with the applied load. Hence, the results of the overstress failure (Nf=1) were used to determine the fracture toughness of the interface, $G_c(\psi)$, at that phase angle. Characterizing the fracture toughness of the interface by using a brazil-nut or a double cantilever beam specimen could greatly enhance the accuracy of the proposed approach.

The average crack propagation rate is found to have a power-law dependence on the normalized crack energy release rate (G_t/G_c). The technique and insight developed in this study can be used to quantify the effect of thermal aging on the fracture in the interfacial intermetallic layer. This study can also be used to understand the widely reported [5][86][3][75][123] failure site transitions observed during flexural loading of unaged and aged PWAs, from the solder and the interface between the IMC layers. This will be the focus of future studies.

Chapter 6: Examples: Competing Failure Mechanisms in PWAs During Dynamic Flexural Loading[%]

This chapter presents a technique to assess the competition between competing failure mechanisms in the solder interconnect, and to assess the resulting durability. The failure mechanisms of interest are cyclic fatigue in the solder material and interfacial fracture between IMC layers. Mechanistic metrics, developed in Chapters 4 and 5, are used to quantify damage in the solder and IMC interface, respectively. The applicability and the limitations of the proposed metrics are also discussed. The original draft of this chapter is a journal paper that is currently submitted for peer-review to ASME Journal of Electronic Packaging.

A Technique to Predict the Failure Site and Durability in the Solder Interconnect During Flexural Loading of the Printed Wiring Assembly

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A methodology is presented to predict the durability and the dominant failure site in the interconnects of a Printed Wiring Assembly (PWA) subjected to flexural loading, in the presence of competing failure mechanisms. This study focuses on two widely reported failure sites: solder balls and interfacial intermetallic layers. The failure

[%] Submitted for review to ASME Journal of Electronic Packaging

envelope for each of these sites is examined in terms of mechanistic metrics (based on interfacial strain energy release rate and plastic strain), instead of empirical metrics (such as drop height, PWA acceleration, or PWA flexural strain). Three examples are presented to demonstrate the technique. The predicted failure site and durability are found to agree with experimental data.

Keywords: Interfacial fracture, solder, intermetallic compound, thermal aging, competing failure envelopes, damage

6.1. Introduction

The importance of dynamic loading to the durability of SMT solder interconnects in modern portable electronic products has received much attention in the recent literature [9][105][116][129][131]. Up until a few years ago, it was common to group all failure mechanisms in the interconnect system under a common category. However, recent research [3][54][73] has documented the major competing failure sites to be in the solder, copper trace, intermetallic layer, and the interface between the copper pad and the PWB.

Failures in the intermetallic compound (IMC) can be further sub-divided into the bulk IMC, the interface between IMC species, and the interface between solder and IMC. However, very few researchers [55][86] have made such detailed distinctions between failure mechanisms, and instead provided more qualitative comparisons of drop durability of emerging technologies. Further research on this topic is warranted because load amplitude and loading rate can change the failure site from the solder to other competing failure sites in the interconnect. *The failure site and the associated failure mechanism govern the proper choice of damage model for predicting durability.*

In recent years, researchers have reported on the change in failure site within the solder interconnect under different loading conditions. Yu, et al. [2] were the first to report a transition in the failure site from solder to the IMC layer with increasing drop height during JEDEC level drop testing of PWAs. Heaslip, et al. [47] compared the drop durability of Sn37Pb and Sn95.5Ag3.8Cu0.7 solders and showed that the failure sites and failure mechanisms change with drop height and solder type. Barry, et al [126] conducted mode I cyclic loading on single solder interconnects and observed a change in the failure site from the solder to the IMC layer, as the crack progressed through the cross-section. Song, et al. [86] conducted high-speed four point bend tests and reported on failure site transitions from the solder to the interface between the IMC layers for specimens with Electroless Nickel/Immersion Gold (ENIG) finish. A Failure Site Transition Zone (FSTZ), in terms of PWA strain and strain rate, was proposed to characterize the failure site transitions. Chai, et al. [54] and Darveaux [3] characterized the fracture strength and failure site of solder interconnects with different combinations of solder alloy and plating material. In general, solders with ENIG finish showed failure site transition from solder to the IMC layer with increasing loading rate and thermal aging. Yeh and Lai [132] ran charpy style impact tests on single solder interconnect assemblies. Depending on the loading rate, the failure was found to be in the solder, IMC layer, or mixed mode (crack traveling through the solder and the IMC layer). The failure site transitions were characterized in terms of the normal and shear forces in the solder.

This paper seeks to extend the excellent work done by the researchers mentioned above by providing a mechanistic insight into the failure site transitions. Despite the previous work described above, the transition of the failure site in the solder interconnect

due to flexural loading of the PWA remains poorly quantified and understood. Most metrics used to characterize the failure site transitions are empirical in nature, and are specific to the tested PWA. Studies that have used numerical simulation do not consider the effect of the interfacial morphology on the stress distribution in the IMC layer because the solder – copper interface was assumed to be planar.

However, studies by several researchers have shown that the interface between the two IMC layers is jagged and wavy [55][87][88][130]. The severity of waviness of the interfacial morphology depends on the manufacturing processes and solder/plating material systems. The interfacial morphology varies constantly with time, even at room temperature, due to diffusion between the plating material, copper trace and solder [130]. Figure 6-1 shows the variation in the morphology of Cu_6Sn_5/Cu_3Sn interface of a SnAgCu interconnect with Organic Solderability Preservative (OSP) finish, at various conditions of thermal cycling [9]. The non-planar interface increases the effective fracture toughness by crack-blunting and crack-shielding mechanisms at the crack tip.

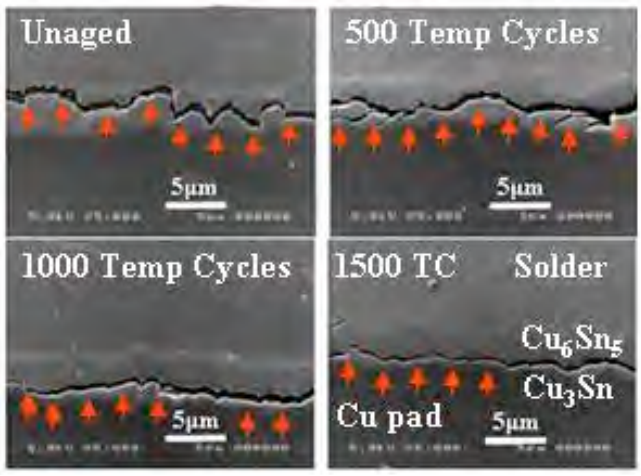

Figure 6-1: Interface of two IMC layers at different thermal aging conditions [55]

This study aims to provide a mechanistic perspective on the failure site transitions

from the solder to the interface between the IMC layers. Fatigue curves using mechanistic durability metrics for both competing failure sites are used to predict the durability and the failure site of the solder interconnect. The proposed technique is demonstrated on a Sn37Pb/ENIG component subjected to four point bend tests.

This paper is part of an ongoing effort to understand and quantify the damage experienced by solder interconnects during quasi-static as well as dynamic flexural loading of PWAs. Earlier work by the authors focused on identifying empirical metrics to quantify interconnects durability [113] and to characterize failure site transitions from the solder to other parts of the PWA [73][118]. Recent work established mechanistic, non-empirical, metrics to quantify the rate-dependent durability of the solder [124] and the rate-independent durability of the interface between the intermetallic layers [133]. The current study extends the previous work by proposing a technique to combine models of these two competing failure modes, to predict which one will dominate under different stress conditions.

The paper is arranged as follows: the experimental data taken from earlier work [85][86], to validate the proposed assessment of competing failure modes, are first summarized. The mechanistic failure models, presented earlier by the authors for relating the applied load to damage in the solder [124] and in the interfacial IMC layers [133] are also summarized for completeness. The subsequent section demonstrates how the dominant failure mode is picked from these competing candidates. Finally, the technique is demonstrated using three examples.

6.2. Approach

The durability metrics and model proposed in this paper are based on experimental data from a previous study [85][86] in which a PWA of simple design was subjected to four-point bend tests at different loading amplitudes and rates. The specimen design and test results are summarized in this paper for the sake of completeness. An FEA model of the PWA is developed to relate the input loading conditions to the plastic strain in the solder and the stresses in the IMC layer. Interfacial fracture mechanics is used to estimate the interfacial strain energy release rate (G^t) and mode mixity (ψ) at the interface between the two IMC layers, based on the stresses obtained from the FEA model. Damage in the solder is characterized in terms of the ratio of plastic strain to the failure strain ($\varepsilon_p/\varepsilon_f$) of the solder material. Damage in the IMC layer is characterized in terms of the ratio of the interfacial strain energy release rate to the interfacial fracture toughness (G^t/G_c) for the IMC interface. Of these two possible failure sites, the one with the highest accumulated damage is predicted to dominate for a given loading condition. Three examples of this approach are presented in this paper.

The following simplifying approximations have been made in the damage modeling effort: The PWA is assumed to be isotropic and homogenous, with no internal or external defects. The solder and the copper trace are modeled as elastic-plastic materials. All other materials in the PWA, including the IMCs, have linear elastic properties. It is assumed that the constitutive equations of bulk solder obtained from literature can be used to represent the behavior of the solder balls. In other words, the length scale effects on the material properties of the solder due to its microstructure are ignored. The wavy interface between the two IMC layers is idealized with a saw-tooth

profile. This simplifying assumption can be justified on the basis of the jagged interfacial morphology observed by numerous researchers [55][86][130].

6.3. Experimental Data

Four stacked-die Ball Grid Array (BGA) packages with 160 Sn37Pb eutectic solder balls each, are mounted on each FR-4 board, as shown in Figure 2. The pad finishes on the component and PWB consist of electrolytic and electroless gold over nickel, respectively. The PWA is subjected to 4 point bend tests at different load amplitudes and loading rates. The flexural strain and strain rate are monitored with suitably placed strain gages. The purpose of choosing this simple specimen design is to allow an in-depth study of the failure site transition, without making the analysis too complex. Sn37Pb solder also makes a better baseline sample because it is a well-studied material with well documented [5][82][83] behavior under high strain-rate loading conditions. Details of the test matrix, test setup, and the specimen can be found in earlier publications [73][86].

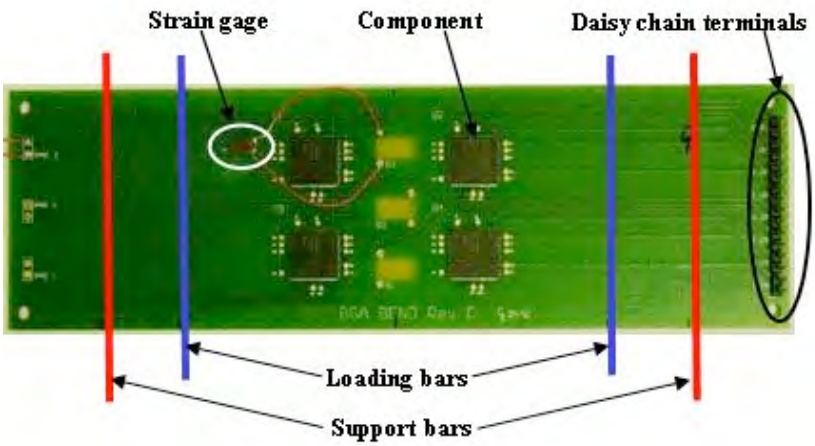

Figure 6-2: PWA specimen, showing location of components and strain gage.

Solid state diffusion at the solder-copper interface of the interconnect leads to formation of Ni_3Sn_4 and $Au_{0.5}Ni_{0.5}Sn_4$ intermetallic compounds on the copper and solder

sides, respectively. Some PWAs are tested in the unaged (as-reflowed) condition, while others are tested after isothermal aging at 135ºC for 168 hours. The thickness of the IMC layer is less than 0.3 microns for the unaged specimens, and in the range of 2 to 3 microns for the aged specimens. The IMC growth between the metal pad and the bulk solder on the component side of the as-reflowed and aged solder joints are illustrated in Figure 6-3 and Figure 6-4.

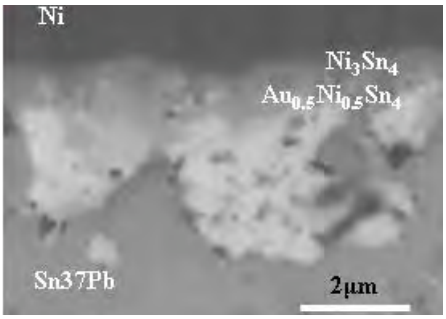

Figure 6-3: ESEM image of the IMC layer between the solder and the Cu-pad of the unaged PWA [85]

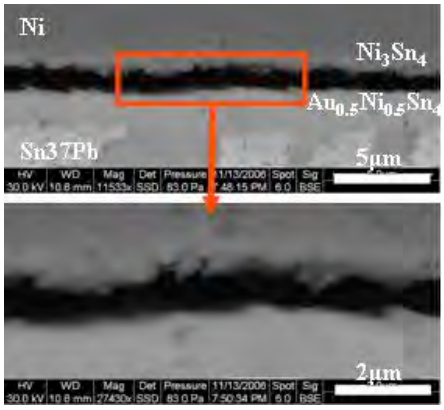

Figure 6-4: ESEM image of the IMC layer between solder and Cu-pad of the aged PWA [85].

The results of the four point bend test are characterized in terms of cycles to failure and the failure site, for different PWA flexural strain and PWA flexural strain rate. A brief summary of the solder and IMC failure data are presented in Table 6-1. Failures in the FR4/Cu-trace are not presented here as they are not relevant for the current study.

Table 6-1: Durabilty and failure sites of the PWAs

Num(-)	PWA Strain (με)	PWA Strain Rate (με/sec)	Aging	Avg. cycles to failure (-)	Failure Site
1	2397	1067	No	838.7	Solder
2	3040	1002	Yes	15.7	IMC
3	2060	1015	Yes	133	IMC
4	2010	990	Yes	204.2	IMC
5	1060	1055	Yes	1735	IMC
6	326	40750	Yes	2423.3	IMC
7	2060	338	Yes	269.2	IMC
8	2000	10000	Yes	102	IMC

Figure 6-5 and Figure 6-6 show typical cross-sectional images of the solder and IMC failures listed in Table 6-1. The failure site in the IMC is found to be at the interface between the Ni_3Sn_4 and the $Au_{0.5}Ni_{0.5}Sn_4$ layers, and is in agreement with other works in the literature [87][88].

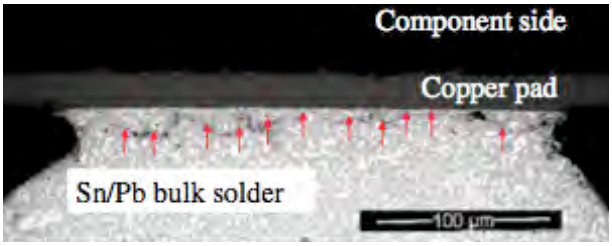

Figure 6-5: Fracture in the solder on the package side of the interconnect [86].

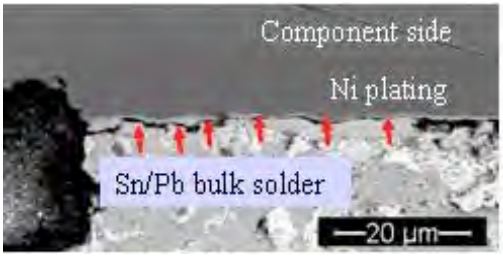

Figure 6-6: Fracture in the IMC layer on the package side of the interconnect [86].

6.4. Completing Failure Models

The models for the competing failure modes are summarized here for the solder failure and IMC failure. In order to use the failure models, transfer functions are first needed to deduce the stress levels at the failure site, for the given PWB deformation.

A numerical model is used to create transfer functions that relate the loading condition to the durability metrics at the two failure sites of interest: $\varepsilon_p/\varepsilon_f$ and G_t/G_c for the solder and IMC interface, respectively. A commercially available software is used to generate a 2-D finite element model of the specimen with 4-noded plane stress elements. The elements are given an appropriate out-of-plane thickness to reflect the geometry of the PWA. As shown in Figure 6-7, only one half length of the PWA is modeled because the specimen is symmetric and it's structural response is limited to the symmetric first mode [86]. Symmetry boundary conditions are applied about x=0, at the center of the model The copper trace connections are ignored in the FEA model. The IMC layer between the solder and the copper pad is also ignored in the FEA model, but it is addressed later in the analytical model.

Figure 6-7: 2D model of PWA with symmetric boundary conditions

The FEA transfer functions are obtained by plotting the average value of the stress at the brittle IMC layer and the maximum plastic strain in the solder, with respect to the PWA flexural strain. The solder transfer function is normalized with respect to failure strain in the solder. The failure strain is the solder plastic strain estimated from the PWA strain corresponding to overstress failure (N_f=1). Details of the technique are presented in [124].

Figure 6-8 shows the normalized solder transfer function for this specimen. One can see that the solder deformation is in the elastic regime till a PWA strain value of approximately 1E-3. Beyond that, the normalized solder plastic strain follows a power law relation with PWA strain.

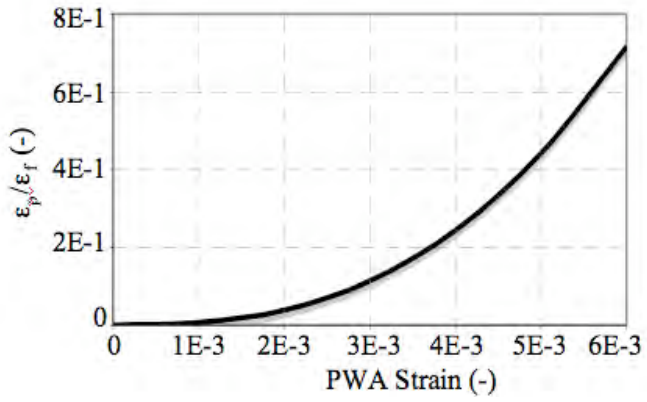

Figure 6-8: Solder transfer function.

Figure 6-9 is the FEA transfer function that relates the PWA strain to the peeling and shear stress in the intermetallic layer of this specimen. Once again, the modeling

details are presented elsewhere [133]. *However, this transfer function is not capable of quantifying the effect of the morphology at the interface between the two IMC layers.* This necessitates the use of an analytical fracture model. The next paragraph summarizes how the transfer function is used in the interfacial fracture mechanics model to obtain a more detailed transfer function that relates the normalized strain energy release rate at the wavy IMC interface to the PWA strain. Details are presented elsewhere [133].

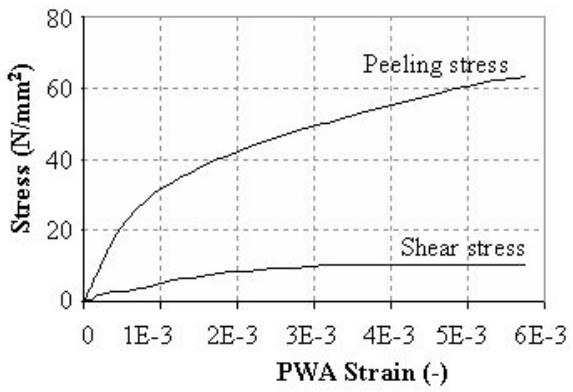

Figure 6-9: Variation of peeling and shear stress in the IMC layer with PWA strain

Let us assume the existence of a small crack that initiates at the interface of the $Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4 layers. Let us also assume that the crack length is 1% of the solder ball diameter at the neck. The mixed-mode stress intensity factors (K^t) and the energy release rate (G^t) at the wavy interface between the $Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4 IMC layers are given by [93][95][99]:

$$K_2^t + iK_1^t = K_2 + iK_1 - f(\xi)e^{i\omega}(K_1 Sin\theta + K_2 Cos\theta) \tag{6-1}$$

$$G^t = \frac{E_{Au-Ni-Sn} + E_{Ni-Sn}}{2E_{Au-Ni-Sn}E_{NiSn}}\left[\left(K_1^t\right)^2 + \left(K_2^t\right)^2\right] \tag{6-2}$$

where:

ξ is the size of the characteristic length on the crack surface, whose value in this

study is 1% of the crack length.

f(ξ) is a non-dimensional scaling factor for the stress intensity factors whose value, as obtained from [91], is 0.2

$\theta = -\tan^{-1}\left(\frac{h}{\lambda}\right)$ is the facet angle of the non-planar interface.

K_i are the interfacial stress intensity factors for a straight interface, derived [93] in terms of the bulk stress intensity factors, the Dundur's parameter (α) for the interface, a parameter ε that quantifies the oscillatory stress field at the interfacial crack tip, a parameter ω that gives the phase shift in the mode mixity due to the mismatch in the material properties at the interface, and the characteristic length (which in this case is the IMC thickness). In turn, the bulk stress intensity factors are derived from the crack length and the interfacial peeling and shear stresses shown in Figure 11. Details of these relationships are well established in literature [133] and are omitted here for brevity.

As shown in Table 6-2, the material properties of the intermetallic compounds (obtained from literature [96]) can be used to estimate all the relevant parameters in this derivation.

Table 6-2: Material properties [96] of the IMCs and calculated values of the interfacial parameters

$Au_{0.5}Ni_{0.5}Sn_4$		Ni_3Sn_4		α	ω (α, 0)
E (GPa)	ν (-)	E (GPa)	ν (-)	(-)	(^{o})
133.3	0.33	48	-0.47	-0.47	3.25^0

The above equations can be used to obtain a family of transfer functions between the interfacial strain energy release rate and PWA strain for different interfacial waviness. Environmental Scanning Electron Microscopy (ESEM) is used to quantify the waviness of the interfacial crack for the unaged and aged PWAs in this study. As noted earlier, the combined thickness of $Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4 in the unaged PWA is approximately 0.3 microns, which is too thin for accurate measurement of the interfacial waviness. Here, we make an approximation that the value of h/λ is 5 for the unaged PWA. For the aged PWA (Table 6-3), the average value of h/λ is approximately 0.5 with a variance of 0.13. The waviness often reduces with thermal aging due to diffusion, thus reducing the effective interfacial fracture toughness.

Table 6-3: Typical values of the interfacial waviness for the aged PWA

h (μm)	1.2	0.9	0.8	1.1	1.0	0.8	1.0
λ (μm)	3.1	1.7	1.9	3.0	2.9	1.2	1.6
h/λ (-)	0.39	0.53	0.42	0.37	0.35	0.67	0.63

Failure occurs when G^t reaches a critical value (G_c), which is a material property. Overstress failure of the IMC interface occurs at a PWA strain value of 4E-3, which can be used to estimate the value of G_c at that mode mixity. Figure 6-10 shows the normalized FEA transfer function for the IMC interface for different facet angles.

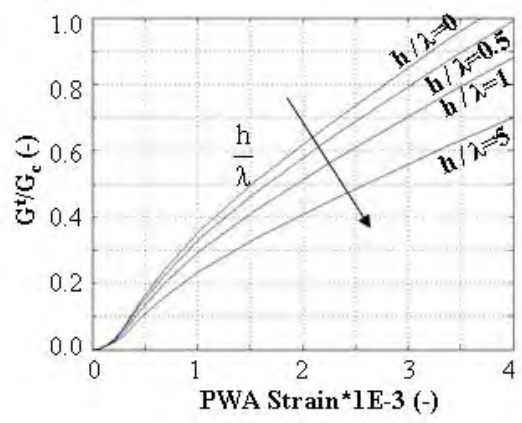

Figure 6-10: Normalized interfacial strain energy release rate as a function of PWA strain, for different morphologies between the IMC layers.

6.5. Competing Failure Envelopes

As shown in the following equations, the durability of the solder and the IMC interface have a power law relationship with $\varepsilon_p/\varepsilon_f$ [124] and G^t/G_c [133], respectively.

$$\frac{\varepsilon_p}{\varepsilon_f} = m(N_f)^n \tag{6-3}$$

where m= 1.13 and n= -0.43 are the durability constants for the solder material. The above equation characterizes the competing rate dependent mechanisms on the durability of the solder interconnect: strain rate hardening and exhaustion of ductility. Experimental data combined with explicit transient non-linear finite element analysis (FEA) was used to derive the damage constants. The ratio of solder plastic strain to its failure strain is used to quantify the rate-dependent durability of the solder interconnect, thus making the damage constants independent of the specimen geometry and dependent only on solder material properties. Details can be found in [124].

$$\frac{G^t}{G_c} = p(N_f)^q \tag{6-4}$$

where p= 1.64 and q = -0.18 are the durability constants for the interfacial IMC

layer. The above equation characterizes the durability of a crack at the interface of ($Au_{0.5}Ni_{0.5}Sn_4$ and Ni_3Sn_4). This equation also takes in to account the effect of non-planarity of the interface between the two intermetallic layers on the stress field at the crack tip. The use of mechanistic parameters to quantify durability makes the damage constants independent of the specimen geometry and dependent only on the properties of the materials that form the crack and the mode mixity of loading. Details can be found in [133].

Figure 6-11 shows the resulting failure envelopes of the competing failure sites in the solder and the IMC interface.

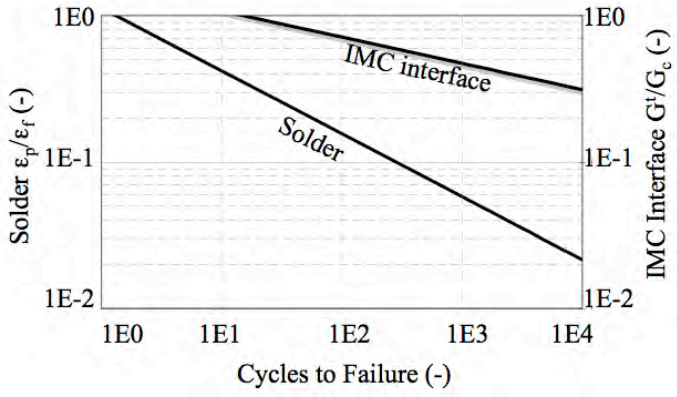

Figure 6-11: Competing failure envelopes for solder and interface between the IMC layers

For a given loading condition, damage can be estimated at each failure site by combining the transfer function with the failure envelope. *Failure is predicted to occur at the site with the maximum damage (lowest value of N_f).* This methodology is illustrated below for three selected examples.

Table 6-4: Examples for methodology

PWA strain (-)	PWA strain rate (sec-1)	aging (-)	h/λ (-)	G^t/G_c (from Figure 6-10)	$\varepsilon_p/\varepsilon_f$ (from Figure 6-8)	Cycles to failure (from Figure 6-11)		Predicted cycles to failure	Test cycles to failure
						IMC	Solder		
2.4E-3	1E-3	no	5	0.25	0.06	4806	833	N_f=833 Solder	N_f= 839 Solder
2E-3	1E-3	yes	0.5	0.58	0.042	110	2115	N_f=110 IMC	N_f=133 IMC
3.26E-4	4E-2	yes	0.5	0.06	3.2E-4	3E6	1.7E8	N_f=3E6 IMC	N_f=2434 IMC

The three examples tabulated above correspond to case numbers 1,3, and 6 of Table 6-1. The predicted durability for each failure site and the test data show very good correlation, as shown in Table 6-4 and Figure 6-12. In example 3, the PWA strain is almost one order of magnitude lower than those of examples 1 and 2, while the PWA strain rate is higher by one order of magnitude. Earlier studies have shown that the durability of the IMC interface [133] and the Sn37Pb solder [124] are only weakly dependent on the loading rate. Hence, as a simplifying step, we can use the failure envelopes shown in Figure 6-11.

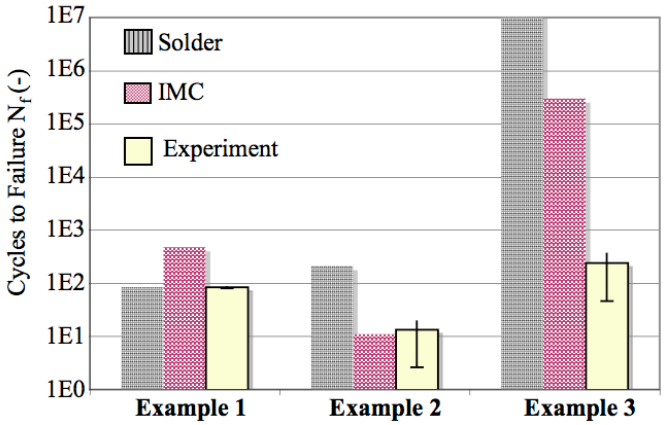

Figure 6-12: Comparison of predicted durability and experimental data.

These examples show how the durability of the IMC interface can decrease as the waviness at this interface decreases (due to aging, for example). This is observed in experiments [86], where aging reduces the interface waviness and moves the failure site from the solder to the IMC interface. There may also be an aging-induced degradation of the intrinsic fracture toughness of this interface and this is the subject of future work.

6.6. Discussion and Conclusion

Published literature [2][3][47][54][55][73][86][126][132] shows that depending on the specimen geometry, material properties and loading conditions, the generally observed failure sites during flexural loading or drop testing of PWAs are solder, copper trace, and the IMC layer. This study focused on the solder and the interface between the two IMC layers and proposed an approach to quantify and understand the interplay between the competing failure mechanisms. To the best knowledge of the authors, this is the first study that provides a mechanistic insight into the failure site transitions in the interconnect during flexural loading of the PWA.

The examples used in this study are quite simple because the crack path is limited

to either the solder to the IMC interface. Mixed-path cracks, where the propagation is through the IMC layers and the solder, have been observed during ball impact tests [132], uni-axial vibration of solder interconnects [126], and during drop testing of PWAs [2]. Similar mixed-path cracks have also been observed during decohesion of thin film on brittle substrates [127] and debonding failure of FRP-reinforced concrete beams [134].

The fracture strength of the IMC interface is in a state of constant evolution even at room temperature because the interfacial morphology and the inter-atomic forces across the interface are changing with time. While this study analyzes the effect of mechanical interlocking at the interface, it does not provide any materials-based insight into the competing failure sites. For example, a simplifying approximation has been made that the failure strain (ε_f) of the solder and critical strain energy release rate (G_c) of the IMC interface do not change with thermal aging. This may be a valid approximation for the limited amount of aging conducted in this study. An in-depth analysis of the effect of thermal aging on ε_f and G_c are beyond the scope of this study.

For the test coupons used in this study thermal aging, and hence the interfacial morphology of the IMC layer, was found to have a strong influence on the failure site of the solder interconnect. The strain energy release rate, calculated at the interfacial crack tip for a given loading condition, decreases with increasing waviness of the intermetallic interface. This could be why a jagged interface (associated with unaged PWAs or certain reflow profiles) rarely sees failure in the IMC layer during flexural testing, while a relatively smoother interface (associated with aged PWAs) is more prone to interfacial failure. The technique and insight developed in this study can be used to quantify the effect of thermal aging on solder to interfacial IMC failure site transitions for a variety of

solder and plating material combinations that have been reported in literature [3][116][126].

This focus of this study is limited to understanding damage initiation, which is why the crack length was assumed to be constant. Hence, the mode-mixity at the crack tip did not vary with the applied load, thus enabling the use of a single value for the fracture toughness of the interface, $G_c(\psi)$, at that phase angle. Future work needs to focus on characterizing the interfacial fracture toughness of the IMC layers as a function of aging. Characterizing the fracture toughness of the interface by using a brazil-nut or a double cantilever beam specimen could greatly enhance the accuracy of the proposed approach.

Chapter 7: Summary

The focus in this thesis is on the durability of surface mount area-array solder interconnects under dynamic loading of the PWA, and on the phenomenon of resulting transitions in the failure site, that has recently started receiving attention in literature. As discussed in the literature review in Chapter 2, the failure site can be in the bulk solder, in the interfacial intermetallic layers, in the copper traces or in the PWB under the bond-pad. Many factors can affect the transition of the failure site from the solder to the remaining sites listed above. This includes load amplitude, loading rate, material properties of the solder and the intermetallic compound, and thermal aging.

This study focuses in particular, on competing failures due to fatigue within the solder and at the interface between two IMC layers, and proposes an approach to quantify the competing mechanics. Detailed mechanistic understanding of damage accumulation in the solder and in the IMC interface are discussed in sections 7.1 and 7.2, respectively. An overall discussion about the dissertation is provided in section 7.3. Finally, sections 7.4 and 7.5 list the contributions and limitations of the dissertation.

7.1. Conclusions: Role of Solder

As discussed in Chapter 4, the test coupons used in this study generally experience PWA flexural strain rates ranging from 2.5E-3 sec-1 to 2.2E0sec-1, which corresponds to solder plastic strain rates ranging from 1E-1 to 1E1 sec^{-1}. These strain rates are too high for creep-dominated deformation and too low for damage due to adiabatic heating. The durability of the solder varies strongly with solder plastic strain, and very weakly with solder plastic strain rate. For a plastic strain rate of 1E0 sec^{-1}, a 100% increase in the

solder plastic strain from 0.1 to 0.2 decreases the durability by almost 83%. On the other hand, at a solder plastic strain of 0.1, an increase in the plastic strain rate by one order of magnitude from 1E0 sec^{-1} to 1E1 sec^{-1} changes the durability only by 40%.

A possible explanation for the weak dependence of solder durability on loading rate could be that the strain-rate hardening of solder at the strain rates encountered in this study (1E-1 to 1E1 sec^{-1}), is negligible. This could be attributed to changes in the deformation mechanisms at the microstructural level at these strain rates. For example: below a transitional strain rate of 1E-3 sec^{-1}, Sn37Pb solder deforms due to wedge cracking induced by grain boundary sliding, while it deforms due to cavitation on the colony boundaries when the strain rate is above the transitional strain rate [100] . Other studies have also reported that plastic deformation is dominated by dislocation motion at quasi-static loading rates, and by twinning at high strain rates [102][103], which can be attributed to the strain rate hardening of the solder because nucleation of twins requires a higher flow stress than dislocation motion does [103]. Analysis at the microstructural level, which is beyond the scope of this study, can provide further insight into the behavior of the solder at the strain rates of interest.

The weak dependence of durability on loading rate can also be explained by the competing effects of strain-rate hardening and ductility exhaustion. This study proposes that the ratio of plastic strain to failure strain be used as a metric to quantify durability of the solder for the strain rates observed in this study. The proposed durability model is a modification of the Coffin-Manson relationship. Another modified Coffin-Manson model, proposed by Eckel [104] is used to relate the durability of the solder to loading frequency. Several studies, including the ones by Shi, et al. [105] and Kanchanomai, et al.

[106] have used the Eckel model to describe solder durability as a function of loading frequency. One of the limitations of Eckel's model is that the value of the exponent is dependent on the strain amplitude. The effect of frequency is higher when the strain range is higher and when the elastic modulus is lower. In comparison, the durability model proposed in Chapter 4 of this dissertation is based on mechanistic concepts. Further work is needed to collect additional data to increase the robustness of the model constants, and make it applicable to a wider range of strain rates.

A direct result of the strain-rate hardening described above is an increase in the yield stress of the solder, which in turn increases the stress in the intermetallic layer during dynamic PWA flexure. The effect of this stress increase is discussed in Chapter 5 and summarized in Section 7.2 below.

7.2. Conclusions: Role of IMC Interface

In the test coupons used in this study, and described in Chapter 5, the diffusion of Sn and Ni leads to a steady change in the thickness and morphology of the two IMC layers of the interconnect. The intermetallic layer itself is made up of layers of different intermetallic compounds formed by the diffusion of Sn from the solder, Cu from the copper trace, and the plating material. Adhesion between the IMC layers is due to a combination of mechanical interlocking at the interface and inter-atomic forces across the interface, which is in a state of constant evolution even at room temperature. The following section discusses the effect of the IMC interfacial morphology on failure site transition and durability of the interface. Results show that as the interconnect is aged, the interface between different IMC species becomes less and less wavy (decreasing facet angles). Experimental results further suggest that the durability of the interface can be

described as a power-law function of the normalized energy release rate (G^t/G_c). For a given mixed-mode loading condition, G^t/G_c decreases with increasing slope of the facet. This provides a mechanistic explanation as to why a jagged interface (associated with unaged PWAs or certain reflow profiles) rarely sees failure in the IMC layer during flexural testing, while a relatively smoother interface (associated with aged PWAs) is more prone to interfacial failure.

The effective strain energy release rate (G_t) has been used in many studies to understand crack propagation in interfaces. Examples include de-cohesion of thin film on substrates [91], delamination of underfill/solder mask interface in electronic packages [107], delamination of epoxy/silicon interfaces [108] among others. In this study, the crack path was completely through the interface. However, this need not be the case all the time. Mixed-path cracks, where the propagation is partly through the IMC layers and partly through the solder, have been observed during ball impact tests [75] and uniaxial vibration of solder interconnects [109]. The tendency of the crack to either remain at the interfaces or deviate away into the bulk material depends on the sign and magnitude of the phase angle. This is specially true for ductile/brittle interfaces. As shown in Chapter 5, the phase angle at the crack tip depends on the geometry and material properties of the PWA. Hence, it is possible to design the PWA in a manner in which the crack follows a pre-planned trajectory.

Studies have also shown that the residual stress in the IMC layer, caused by negative volume changes, increases with aging time. The residual stress can change the value of the mode I and mode II stress intensity factors at the site of the micro-crack, and hence the value of the phase angle at the crack tip [91]. This will not only affect the

durability of the joint, but also the path of the crack as it could be diverted away or toward the interface.

This dissertation therefore provides mechanistic insights as well as related methodologies to assess the relative durability of two competing failure modes: fatigue cracking through the solder or at the interface between different IMC species at the bond pad. Fatigue failure in the solder is addressed with an exhaustion-of-ductility model and failure in the IMC interface is addressed with interfacial fracture mechanics. This study does not address the materials-based aspects of the competing failure sites. For example, the value of ε_f for the solder and G_c of the interface are assumed to not change with thermal aging. This may be an acceptable simplifying assumption for the limited amount of aging conducted in this study. An in-depth analysis of the effect of thermal aging on ε_f and G_c are beyond the scope of this dissertation.

7.3. Discussion

This dissertation presents a systematic approach to characterize the durability and failure site transitions of solder interconnects due to dynamic flexural loading of PWAs. Failure Maps are used to characterize the failure site transitions from the solder to other parts of the interconnect. Of all the potential competing failure sites within the interconnect (solder, Cu-trace, FR4, bulk IMC layer, IMC interfaces, etc), this study focuses on the solder and the interface between two IMC layers. Exhaustion of ductility and interfacial fracture mechanics are used to provide a mechanistic perspective to the failure site transitions between these two selected failure sites.

The failure mode with the lowest durability for a given loading condition governs

the durability and defines the dominant failure site for that condition. The fatigue failure envelopes of competing failure mechanisms at competing sites intersect along the failure site transition zone. As an example, for the test coupons and loading conditions used in this study, the failure site at low load amplitudes and loading rates is in the solder and the durability of the interconnect is defined by the solder failure envelope.

Empirical and mechanistic metrics are identified to understand and quantify the rate-dependent failure site transition between the two failure sites of interest: solder and IMC interface. 3D explicit numerical simulations with rate-dependent material properties, conducted as part of this dissertation, show that strain-rate hardening of the solder during dynamic flexural loading of the PWA increases the stress in the remaining failure sites while decreasing the plastic strain in the solder. The resultant loading conditions cause the interface between the IMC layers to reach their fatigue failure limit before the solder reaches its own. This leads to a transition in the failure site from the solder to IMC interface. This concept is discussed in detail in Chapter 6, along with examples of failure site transitions between the solder and the interfacial IMC.

While many researchers have observed failure site transitions from the solder to the IMC layer under dynamic flexural loading conditions, only some have tried to understand it from the materials perspective and very few have tried to characterize it experimentally. *Surprisingly, there has been no study where a detailed mechanistic analysis of the failure site transitions and durability damage metrics in terms of mechanistic parameters has been conducted.* This is partly because the dynamic behavior of IMC interfaces is unknown and partly because this is a very recent problem. Each aspect of solder interconnect durability investigated in this dissertation is a separate

research field in its own right and no single work can do justice to all these aspects. However, progress was made in assimilation, extension and development of all the aspects mentioned in this dissertation. A detailed description of the contributions of the dissertation is provided in the next section.

7.4. Contributions

As summarized in the earlier section, this dissertation provides a mechanistic perspective to the durability and failure site transition in the solder interconnects of a PWA. It is expected that development of new Pb-free solders will benefit from the insights provided in this dissertation. The findings of this thesis can also be used in other engineering applications; for example: competing failure mechanisms during the de-bonding of composite-plated concrete beams and loosening at the glenoid component at the bone-cement interface during treatment of osteoarthritis, among other problems. A detailed description of the contributions of the dissertation are discussed below

7.4.1 Test Methodology

A new test methodology was developed to quantify the durability of the solder interconnect of a PWA subjected to board level drop testing, irrespective of its boundary conditions and loading orientation. Compared to the existing techniques to conduct board level drop tests, the proposed methodology allows researchers to understand the individual and combined effects of load amplitude and rate on the durability of the solder interconnect. Empirical failure maps were also developed as part of the test methodology to characterize failure site transitions between the solder and other parts of the PWA.

The test methodology was demonstrated for PWA strains ranging from 2E-3 to

1.2E-2 strains, and PWA strain rates ranging from 2.5E-3 to 2.2E0 sec^{-1}. Although the test methodology was demonstrated on PWAs with Sn37Pb solder interconnects (which is a well-characterized material at high strain rates), the technique can easily be extended to Pb-free interconnects whose behavior under dynamic loading conditions is relatively unknown.

7.4.2 Empirical Dynamic Durability Model for the Solder

An empirical rate-dependent durability model, based on mechanistic principles, was developed to obtain fatigue failure envelopes for the solder under dynamic loading conditions. The model has been successfully used to compare the durability of solder interconnects with different material properties (Sn37Pb vs SnAgCu), and aging conditions (as-reflowed vs aged for 100 hours at 150^0C) for PWA strains ranging from 2E-3 to 1.2E-2 strains, and PWA strain rates ranging from 2.5E-3 to 2.2E0 sec^{-1}. The model showed good correlation with experimental data.

7.4.3 Mechanistic Insights into Solder Fatigue

For the test samples (Sn37Pb solder interconnects) and conditions used in this study, the experimental data showed that solder durability had a high dependence on PWA strain amplitude (which ranged from 2E-3 to 1.2E-2 strains) and a very weak dependence on the PWA strain rate (which ranged from 2.5E-3 to 2.2E0 sec^{-1}), even though the loading rate was varied over four orders of magnitude. The empirical rate-dependent durability model developed in this dissertation was combined with rate-dependent FEA to provide an insight into this atypical behavior, for the solder strain rates seen in this study (3E-1 to 3.2E0 sec^{-1}). Guidelines can be developed to optimize the

competing effects of strain–rate hardening and exhaustion of ductility to reduce the plastic deformation in the solder at high strain rates, thereby increasing solder durability.

7.4.4 Mechanistic Insight into Interfacial IMC Fracture

This thesis combines, for the first time, microstructural aspects of the interfacial IMC layer, as provided by Xu and Pang [55], and the fundamentals of non-planar interfacial fracture, as developed by Evans and Hutchinson [91], to understand the evolution of interfacial strength of the IMC layer as a function of thermal aging, material systems, and interfacial morphology. The insights provided in this study are limited to ENIG-Sn37Pb solder systems that have been isothermally aged at 135^0C for 168 hours. The PWA strains ranged from 3.25E-4 to 2.4E-3, and PWA strain rates ranged from 1E-3 to 4E-2 sec^{-1}. The approach developed in this study can easily be implemented for other material systems and thermal aging profiles.

7.4.5 Mechanistic Insight into Failure Site Transitions from Solder to IMC

A phenomenological model was proposed to characterize the failure site transitions, observed in this study, between the solder and the interface between the IMC layers. The proposed model takes into account, the effect of strain rate hardening and exhaustion of ductility in the solder due to high loading rates, the effect of interfacial morphology in the IMC interface due to manufacturing process and thermal aging, and the effect of mode mixity due to PWA geometry and loading orientation. The model was demonstrated for PWAs with ENIG-Sn37Pb solder interconnects, for PWA strains ranging from 3.25E-4 to 2.4E-3, and PWA strain rates ranging from 1E-3 to 4E-2 sec^{-1}. The mechanistic failure criteria proposed in this work can now be utilized for defining solder and IMC failure, as

opposed to empirical criteria used so far. To the best knowledge of the author, this is the first model that provides a mechanistic perspective on the failure site transitions between the solder and the IMC layer.

The contributions of this dissertation are expected to gain importance as solder interconnects become smaller, thus making them more susceptible to stresses during dynamic flexure of the PWA. However, there are many limitations in this dissertation that can be addressed in the future. The relevant ones are discussed in the following section.

7.5. Limitations and Suggestions for Future Work

The following suggestions are made for improvement and extension of the current work.

7.5.1 Range of Validity of Study

The test methodology developed in this study was demonstrated for PWA strains ranging from 2E-3 to 1.2E-2 strains, and PWA strain rates ranging from 2.5E-3 to 2.2E0 sec^{-1}. The phenomenological model developed in this study to understand and characterize failure site transitions from the solder to the interfacial IMC layer was demonstrated for PWA strains ranging from 3.25E-4 to 2.4E-3, and PWA strain rates ranging from 1E-3 to 4E-2 sec^{-1}. The material system of the solder interconnect was limited to Sn37Pb. While the proposed methods are generic because of its mechanistic foundations, their actual applicability outside of the parametric range requires further study.

7.5.2 Sample Size

The small sample sizes used in the test program in this study allow qualitative conclusions but the confidence in quantitative model constants is limited. This dissertation used only two data points per test condition to determine the solder fatigue properties at high strain rates. A larger sample size will strongly enhance the confidence in the solder fatigue properties determined in this thesis.

7.5.3 Effect of Thermal Aging on Solder Microstructure

The macroscopic (continuum mechanics) to microscopic (fracture mechanics) phenomenological model assumes that the microstructure of the solder for the given thermal aging condition (168 hours at 125^0 C) has a negligible effect on the results, when compared to the effect of interfacial morphology. Such an assumption may be valid for short durations of isothermal aging, as was the case in the tests conducted. However, changes in the solder material properties induced by the long-term thermal aging could play a definitive role in the failure site transition and durability under high strain rates. This needs to be investigated.

7.5.4 Effect of Strain Rate on Fracture Toughness

As shown in Chapter 5, the fracture toughness of the interfaces between two IMC layers of interest is unknown, especially at high strain rates. This is still an open field of research and the current lack of understanding in this area may prove to be a major bottleneck in the future. This is especially true because many of the solder compositions, plating materials and manufacturing processes for Pb-free solders are still in a state of evolution.

7.5.5. Material Science Based Perspective to Interfacial Fracture

Relatively few studies have been conducted to understand the failure site transitions from the solder to the IMC layer. This dissertation only considers the mechanistic aspects of the observed phenomenon for the load amplitudes, loading rates and test coupons used in this study. The dissertation does not consider the material aspects of interfacial IMC fracture. For example, it is not known if (and by how much) thermal aging weakens the adhesive bonds between the two interfaces of the IMC layer. It is also not known if the fracture toughness of the interface varies with loading rate. These material properties of the interface can have a very dominant effect on the failure site transitions, and must be investigated in detail.

7.5.6 FEA Approximations

The rate-dependent 3D numerical analysis conducted in this study uses dynamic material properties of the solder that were obtained using macroscopic specimens. The Hall-Petch effect on solder material properties is very well documented in literature and hence the length scale dependent material properties are required. Future studies should focus on accurate characterization of length scale dependent material properties of the solder. This will strongly enhance the results and conclusions provided by the numerical analysis.

Appendix A: Durability Estimation Methodology [1]

This chapter proposes a methodology to quantify durability of the solder interconnect of a PWA subjected to transient loading. The original draft of this chapter is published in the Microelectronics Reliability journal. The methodology, which uses experimentation, signal processing and numerical analysis, is presented to quantify the interconnect durability. It is shown that the proposed methodology can quantify durability, irrespective of the loading orientation and PWA boundary conditions. A case study, using a PWA of a simple design, is used to demonstrate the approach.

Test Methodology for Durability Estimation of Surface Mount Interconnects under Drop Testing Conditions

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This paper presents a generic methodology to determine the durability of surface mount interconnects in electronic assemblies, under drop loading conditions. Damage accumulated in the interconnects due to repeated drops is quantified in terms of local Printed Wiring Assembly (PWA) response (flexural strain, strain rate, acceleration, number of flexural cycles), rather than the loading (total impact energy, orientation and number of drops). The advantage is that the results are more generic and can be extrapolated to different assemblies and different loading/orientation conditions. A damage estimation model, based on the observed failure mechanism and mode, is used to

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determine the durability of the surface mount interconnects under the applied loading history. The same model can be used to extrapolate the results to field conditions. A case study, using a simple specimen, is presented to demonstrate the proposed methodology. Failures are observed in the interfacial intermetallic layer of the component bond pad in the corner solder joint. The generality of the method is demonstrated by calibrating the model constants with in-plane drop tests and then successfully predicting the durability for an out-of-plane drop test. Thus, the approach and model constants are shown to be independent of impact orientation and boundary conditions.

Keywords: Drop testing; Impact testing, Interconnect damage, Intermetallic fracture, Durability, Electronic Packaging.

Nomenclature

A_i: Mode shape dependent constant at the i^{th} mode

C_1, C_2: Constants in damage model

D: Damage in the intermetallic

N: Number of cycles to failure

W_i: Weight function of the i^{th} mode

a: Crack length

a_i: Crack length before the loading cycle

a_f: Crack length after the loading cycle

m: Total number of modes

n_{ij}: Number of cycles of the j^{th} bin at the i^{th} mode

p: Slope of Paris' curve

r: Number of bins at each mode

α: Crack tip angle

ΔK: Cyclic range of stress intensity factor

$\Delta\sigma$: Cyclic stress range

$(\Delta\sigma_{peeling})_{ij}$: Range of peeling stress at the failure site at the j^{th} bin at the i^{th} mode

A - 1. Introduction

Electronic devices in a variety of applications are often subjected to drop and vibration loading. Military electronics are subjected to repetitive shocks (artillery fire), sudden high G loading during launching or maneuvering of projectiles or during ballistic impact. Other electronic products may experience costly drop events during transportation and handling. Portable electronics may see similar drop events throughout the life cycle due to accidental abuse. These transient events can cause damage to the external housing, internal components, internal plastic mounts and snaps, and component-to-board interconnects, among others.

Electronic products subjected to this type of dynamic loading are expected to be rugged. However, the need for reduction in product weight and size leads to design features that make the products susceptible to failures induced by drop and impact. The drive towards finer pitch and high density packages exacerbates the risk of interconnect failure. This paper therefore focuses on design and testing of electronic interconnects for drop/impact loading.

At present, manufacturers of hand-held electronic devices use the JEDEC JESD22-B104-B standard for mechanical drop testing [1]. The drop-durability of portable electronic products is quantified and ranked by the number of drops to failure. The product is held in the desired orientation on a drop carriage that is allowed to fall on to a fixed target. But characterizing the drop durability of interconnects by running tests or simulations at the product level is a very complex task. Goyal and Buratynski [2] showed that even a single drop event of an electronic product can produce a complex multi-modal transient response history. Lim and Low [3] showed that the structural response of the PWA is strongly dependent on the mass distribution of the internal electronics, the mounting of the PWA, and the orientation of drop. Consequently, conventional testing approaches that attempt to correlate drop durability to loading parameters (total impact energy, orientation and number of drops to failure), typically report difficulties in correlating with drop durability under field conditions.

When a portable electronic product is dropped, part of the kinetic energy goes into the rigid body motion during rebound, part goes into the strain energy of deformation of the internal electronics and external housing, and the rest is lost to damping and friction. Only a portion of the energy absorbed by the internal electronics causes damage to the interconnects. The amount of energy responsible for the deformation of the interconnect depends on the loading conditions, component architecture, PWA mounting details (boundary conditions), housing structure, and material properties.

Drop tests conducted by Lim, et al. [3][4] and Seah, et al. [5] showed the extent of variation in PWA strains and accelerations, for different electronic devices and different drop orientations. Therefore, test specifications for drop durability of surface mount

interconnects, which are based on loading specifications (such as incident kinetic energy or shock response spectrum), are bound to be case-specific and will lack the generality for extrapolation across different product styles and different drop conditions. It is better to relate the damage in the interconnects to the local response of the PWA, close to the failure site, because the relationship between the local response and the damage amount is less sensitive to test conditions.

The test vehicle recommended by the JEDEC Standard JESD22-B111 [6] for studying interconnect durability is a daisy-chained PWA of standard form, with standard fixturing (i.e. with standard boundary conditions), in order to minimize some of the complexities discussed above. PWA level testing can be used to develop failure envelopes for the characteristic damage mechanisms in surface mount interconnects. From an industry perspective, testing the drop durability of the interconnect at the board level is easier and can be done by the component supplier.

In the JEDEC Standard [6], the PWA with daisy-chained components is mounted on to a drop carriage in the horizontal position, at four or six points. The drop carriage falls vertically along two guide rods on to a stationary impact surface and induces out-of-plane displacement in the PWA on impact. The impact surface can be changed to vary the profile of the impact force and deceleration histories. On impact, the PWA responds to the transient impact force applied to the base and then vibrates at its natural frequency. Instrumentation includes accelerometers on the drop carriage, strain gages on the PWA and a high speed data acquisition and failure monitoring system.

Durability of the interconnects is strongly dependent on the strain and strain rate of deformation. Tests conducted by Yu, et al. [7] and Juso, et al. [8] indicated that the

number of cycles to failure decreased as the PWA strain and strain rate increased. Varghese and Dasgupta [9] ran impact tests on PWAs in the in-plane and out-of-plane orientations and showed that the number of impacts to failure decreased with increasing PWA strain. The failure site for both impact orientations was the interfacial intermetallic layer. Researchers have also reported different failure sites for different loading conditions. Yu, et al. [7] observed a transition in the failure site from the solder to the interfacial intermetallic beyond a critical drop height. Varghese and Dasgupta [10] subjected PWAs to flexural strain rates ranging from 10^{-3} sec^{-1} to 10^{1} sec^{-1} and observed a failure site transition from the solder to the copper trace beyond a critical PWA strain rate. This change in failure site and in the failure mechanism caused the durability to vary non-monotonically with PWA strain rate, although it still varied monotonically with PWA strain amplitude. Heaslip, et al. [11] compared the drop durability of Sn-Pb and Pb-free solders and showed that the failure sites and failure mechanisms change with drop height and solder type.

Damage modeling methodologies have been proposed over the last few years to quantify interconnect durability under board level impact testing conditions. In Feb 2003, Varghese and Dasgupta [9] introduced a test methodology to predict impact durability of surface mount interconnects. PWA flexural strain was used as the damage metric and the damage model was based on brittle crack propagation because the failure site was in the brittle intermetallic layer. A damage quantification algorithm was proposed, which used wavelet decomposition to decompose the PWA strain history into its constituent modal contributions, and rainflow cycle-counting to assess the damage at each frequency level. The test methodology was demonstrated for a PWA with a single Sn-Pb Plastic Ball Grid

Array (PBGA) component, subjected to in-plane and out-of-plane impact on fixtures with different boundary conditions. Although the damage constants were verified to be independent of impact orientation, loading conditions and boundary conditions, the model constants were specific to the architecture of the PWA being tested. In Nov 2003 [12] the test methodology was modified to change the damage metric from PWA strain to solder strain by using Finite Element Analysis (FEA). This made the test methodology more generic, within the approximations of the analysis, because the model constants were a function of the material properties alone. Tee, et al. [13] proposed a durability model in May 2003 for out-of-plane drop testing of PWAs. Maximum peeling stress in the solder was used as the damage metric and the durability model was formulated using a power law relationship. The technique was demonstrated for boards mounted with Thin Profile Fine Pitch Ball Grid Array (TFBGA) and Very Thin Profile Fine Pitch Ball Grid Array (VTFBGA) components. In Nov. 2003, Heaslip and Punch [14] demonstrated the use of wavelet analysis to understand the complex spectral response of an unpopulated board subjected to drop tests. In 2004, Zhu and Marcinkiewicz [15] proposed the use of effective plastic strain in the solder ball as the damage metric and compared the component reliability at different loading conditions. Although a damage model was not developed, components with higher effective plastic strain were shown to fail earlier than those with lower values of plastic strain in the solder ball. In 2005, Lall, et al. [16] demonstrated the use of a damage quantification technique very similar to the one proposed by Varghese and Dasgupta [9][12], on test vehicles mounted with BGAs and CSPs, subjected to in-plane drop. Wavelets and cycle counting techniques were used to quantify the complex load history. PWA flexural strain was used as the damage metric

and the damage model was based on the Coffin-Manson relationship because the failure site was in the solder.

In summary, the literature shows that existing drop testing standards are not generic in nature. The durability of interconnects depends on a variety of parameters, such as the mass distribution on the PWA, drop height, drop orientation, impact surface, dynamic material properties of the structure and boundary conditions. The failed interconnect in most ball grid array (BGA) components is usually in the outermost row, implying that failure is driven by flexure of the PWA [13]. On the other hand, interconnects of heavy BGA components can also fail in the inner rows, implying that failure in this case may be primarily driven by inertial forces generated by the component mass [17]. The partitioning of the contribution of PWA flexure and component inertia to the damage in the interconnects under drop testing conditions is component-specific and has not yet been quantified. The damage parameter (plastic strain or peeling stress) is usually monitored in the bulk solder, even when experimental data indicates that the failure site under drop testing conditions could be not only in the solder, but also in the PWA under the bond pad, in a nearby copper trace, or in the intermetallic layer. The distribution of strain energy in the PWA must be understood to improve the test methodology for drop durability of interconnects.

To consider drop durability proactively in the design phase, there is a need for a methodology based on an understanding of the fundamental mechanics of the problem. The method developed in this study, is as follows:

- Establish an accurate and repeatable test methodology for different specimens, boundary conditions and loading conditions.

- Develop a generic & unified basis for damage estimation, which is independent of product geometry, loading & boundary conditions.

The organization of this paper is as follows: The proposed test methodology is first discussed in generic terms. A specific case study is then presented in the subsequent section to demonstrate the approach. The correlation of board and product level drop testing is discussed at the end of the paper.

A - 2. Approach

This work proposes a test methodology that characterizes the resulting interconnect failure in terms of the local structural response at the failure site. A summarized version of the test methodology, presented in [9], is repeated below, for completeness. Figure 1 presents the flowchart and the details are presented in the following sub-sections.

Step 1: Obtain the strain gage and accelerometer data for each test condition.

Step 2: Observe the number of drops to failure for each test condition. Conduct failure analysis and group the results according to the failure site and the failure mechanism.

Step 3: Identify modal participation of PWA transient response by wavelet decomposition of the strain and acceleration signatures.

Step 4: Obtain amplitude distribution functions (number of cycles at each amplitude) by using cycle counting analysis, to quantify the load history at each mode.

Step 5: Use FEA to obtain stress at the failure site for a given PWA strain, strain rate and component acceleration.

Step 6: Relate stress amplitude at failure site to damage, using relevant damage model.

Step 7: Repeat Step 4 and Step 6 to quantify damage for every mode decomposed by the wavelet transforms (D_{mode_i}).

Step 8: Sum the results for all modes to quantify the cumulative damage from all the response modes for a given drop event. (D_{drop}) using the results of Step 3 and Step 7.

The following simplifying approximations have been made in the development of this test methodology. The solder balls are approximated as isotropic, homogenous and defect free. The effect of initial defects and initial residual stresses on drop durability is neglected. Damage due to stress wave propagation in the solder ball is assumed to be negligible when compared to the damage induced by PWA flexure, flexural rate and component acceleration. It is also assumed that damage accumulation is linear and follows Miner's rule. The non-linear effects of load sequencing are beyond the scope of this paper.

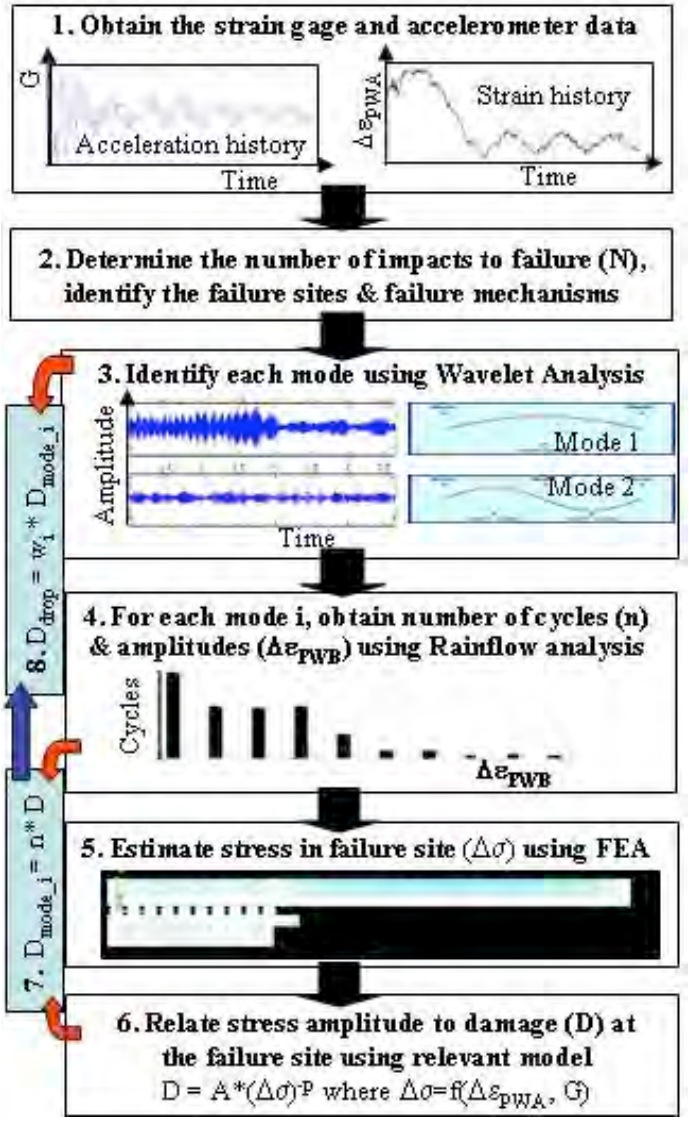

Figure A-1: Flowchart for quantifying damage in drop testing.

A - 2.1 Test Matrix

The response parameters of interest at the site of each failed interconnect are the local PWA flexural strain, flexural strain rate and average acceleration of the component. A test matrix is developed to systematically vary these three parameters, by varying the loading parameters such as incident kinetic energy, boundary conditions and impact orientation. The tests can be classified in to three types:

- **Flexural tests**: The specimen is impacted in different orientations, but constrained to prevent any rigid body acceleration. Durability of the interconnect is thus affected only by flexural strain and flexural strain rate of the PWA.
- **Inertial tests**: Specimen is dropped in different orientations, but constrained to prevent any curvature in the PWA. Durability of interconnect is affected only by inertia forces exerted by the component on the interconnect.
- **Combined tests:** The specimen is dropped in different orientations, but neither flexure, nor rigid-body accelerations are constrained. Interconnect durability is affected by both flexural and inertial loads.

The various combinations are shown in Table A-1 and Figure A-2. Each test condition is repeated to explore the consistency of the data

Table A-1: Test Matrix. X and 0 represent the active and inactive test variables respectively.

Test	Curvature	Curvature rate	Component acceleration	Drops to failure (N)
Flexural	X	X	0	$N = f(\varepsilon, \dot{\varepsilon})$
Inertial	0	0	X	$N = f(a)$
Combined	X	X	X	$N = f(\varepsilon, \dot{\varepsilon}, a)$

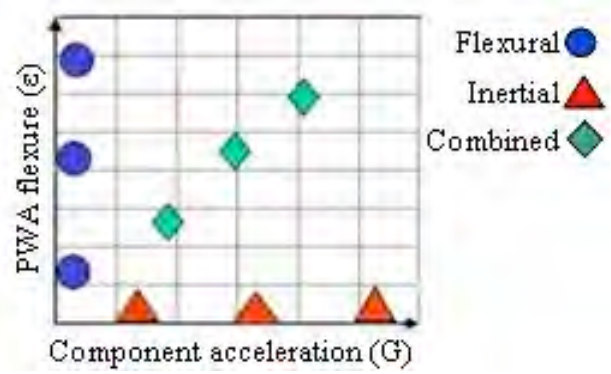

Figure A-2: Test matrix. Component acceleration is zero for flexural tests and PWA flexure is zero for inertial tests. Combined tests represent actual drop conditions.

A - 2.2 Test Setup and Instrumentation

A 6 ft tall pendulum-style impact test setup is designed and fabricated in-house for conducting in-plane and out-of-plane impact tests (Figure A-3). The kinetic energy of impact can be varied by changing the mass of the steel sphere and/or the impact velocity. The mass of the steel sphere can be varied from 25 grams to 450 grams. The impact velocity, which can reach a maximum value of 6m/sec, is varied by changing the pendulum release height.

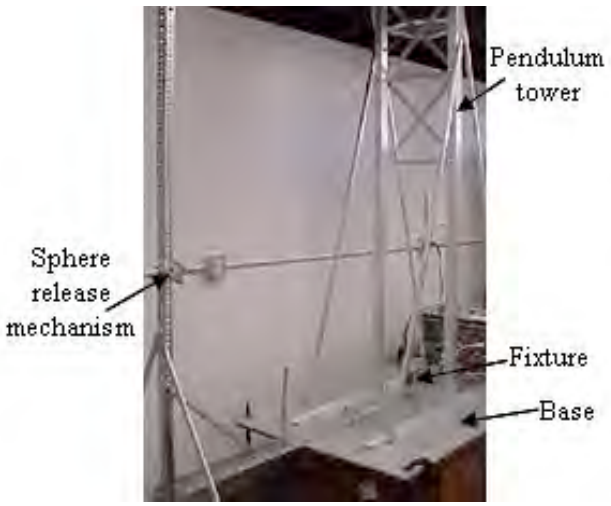

Figure A-3: Pendulum test setup for conducting flexural tests.

The out-of-plane and in-plane fixtures, shown in Figure A-4 and Figure A-5, respectively, are made of aluminum. A schematic diagram of the fixtures is shown in Figure A-6. For out-of-plane impact, the specimen is oriented vertically and clamped at its four corners. The sphere impacts the center of the PWA, causing out-of-plane displacement. For in-plane impact, the specimen is oriented horizontally and the two edges orthogonal to the impact axis are guided with leaf springs to remain in the impact plane. Horizontal motion of the impacted edge translates into bending of the specimen. The PWA is given a small initial flexure while mounting it to the in-plane fixture to induce bending toward the component side. This ensures the repeatability of the direction of PWA deflection. The value of the initial flexure is recorded by the strain gage mounted on the PWA. Ensuring repeatability of the test setup is a critical step in developing the drop test methodology and is discussed below, after the description of the instrumentation.

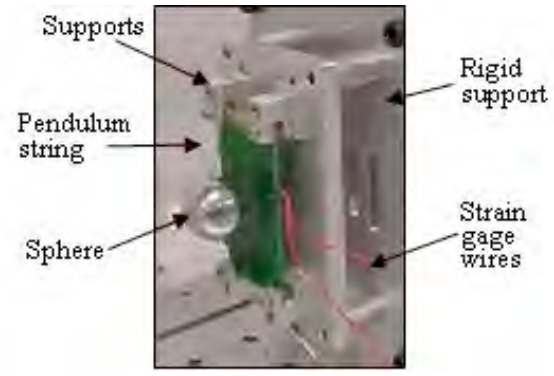

Figure A-4: Out-of-plane fixture.

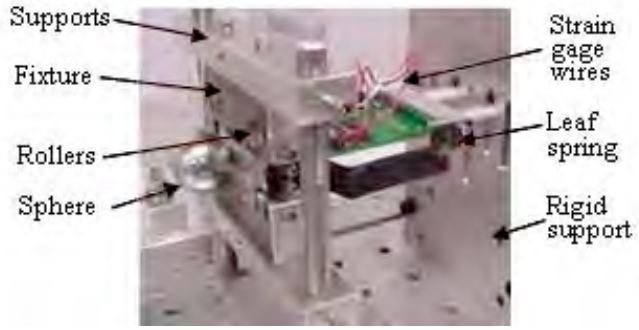

Figure A-5: In-plane fixture.

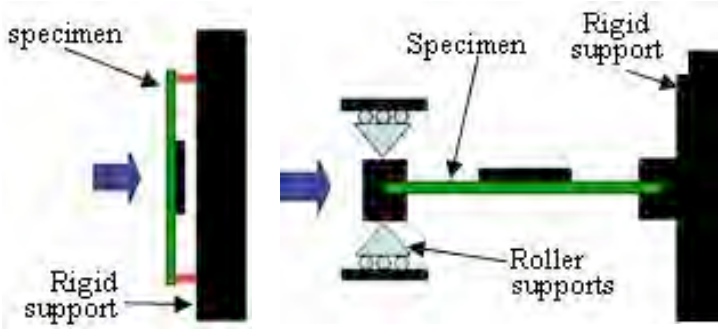

Figure A-6: Schematic diagram of the (a) out-of-plane fixture (b) in-plane fixture.

A 350 ohm resistance strain gage with 3.18 mm gage length and 2.54 mm grid width is attached to the PWA near the corner of the component (the site of maximum curvature) to measure the flexural strain and the flexural strain rate along the longitudinal axis of the PWA. Failure is defined as the increase in the resistance of the interconnect by 1000 ohms. Due to the transient nature of the test, the resistance spike can last for less than one millisecond. So, an in-situ high speed resistance measurement system is developed in-house for continuous failure monitoring. The high speed data acquisition system (Figure A-7) consists of a 4 channel, 16 bit DAQ card with a maximum sampling rate of 5MHz per channel. The sampling frequency during the tests is maintained at 25kHz.

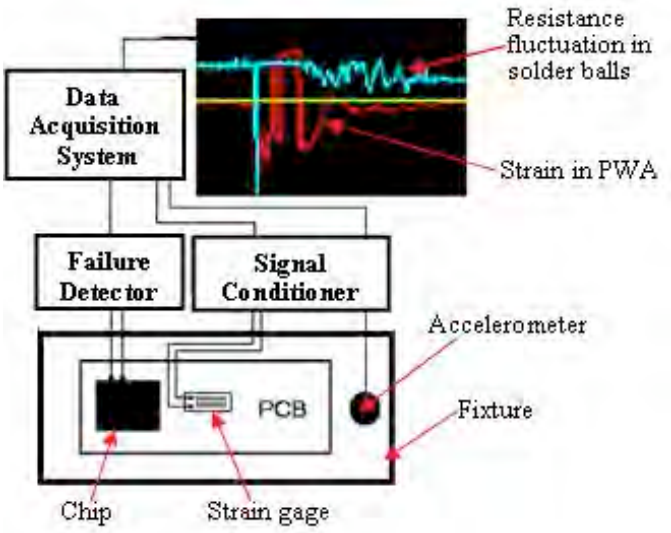

Figure A-7: In-situ resistance monitoring system.

The entire test setup is tested for repeatability. PWA strain histories of 10 consecutive impacts are compared to verify the repeatability of the out-of-plane and in-plane fixtures. The typical out-of-plane strain response looks like a damped sinusoidal wave, as shown in Figure A-8. The typical strain history of the in-plane impact looks like an impulse signal, as shown in Figure A-9. The first mode dominates the structural response of the PWA for both impact orientations. Repeatability of the test setup is quantified by calculating the mean and the standard deviation of the strain history at the point of maximum strain. The values are tabulated in Table A-2. Both fixtures show very good repeatability.

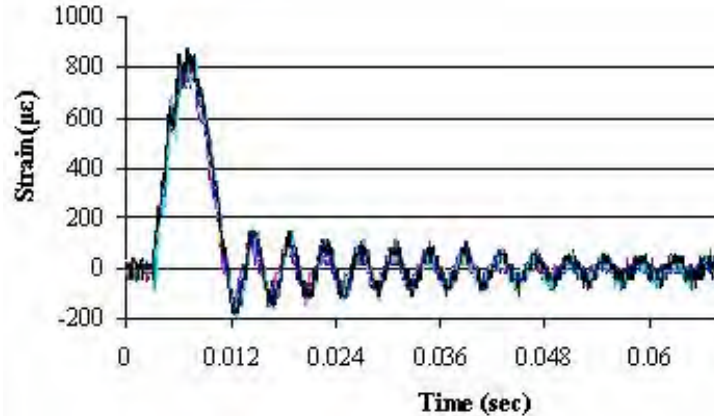

Figure A-8: Comparison of the strain histories of ten out-of-plane impacts to verify repeatability.

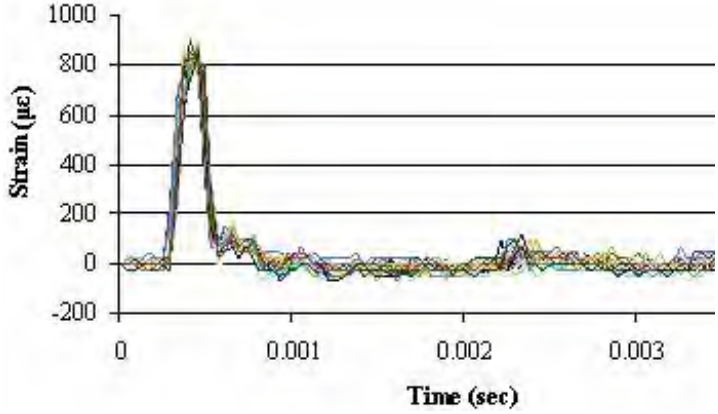

Figure A-9: Comparison of the strain histories of ten in-plane impacts to verify repeatability.

Table A-2: Repeatability of test setup.

	Maximum Strain	
	Out-of-plane (με)	In-plane (με)
Mean	796.7	823.1
Std. Deviation	18.4	48.1

A - 2.3 Signal Post-Processing

The problem of decomposing the structural response of a body to shock/vibration loading is not new. Much work has been done to understand the structural response

during missile launch/gun fire [18][19], occupant safety during vehicle collisions [20][21], durability of casks under drop test conditions [22], fatigue of aircraft parts [23], dynamic response of human beings during road/rail transportation [24], et cetera. A PWA subjected to drop testing vibrates in a non-stationary random manner. One way to decompose the complex signal is to use Discrete Wavelet Transform (DWT). Alternate techniques for temporal and spectral decomposition of transient and random signals include Fast Fourier Transform (FFT) or Short Term Fourier Transform (STFT). The relative advantages and disadvantages of DWT over FFT and STFT are described below.

The FFT, using sinusoidal basis functions, gives the average frequency spectrum of a signal, with no information about temporal variation. FFT is best suited for the analysis of stationary signals, or signals whose spectrum remains constant. The STFT is a windowed FFT that allows analysis of non-stationary signals. The STFT performs an FFT sequentially on small windowed sub-sections of data to obtain the frequency spectrum of the signal for that section. However, STFT requires a design tradeoff between time and frequency resolution. For an STFT to yield useful results, only small frequency changes can occur during the short sampled period, thus limiting its use for applications with transient signals.

DWT uses various types of functions with adjustable compact support, as basis functions in software filters, to separate a signal into frequency bands. DWT can be used to analyze non-stationary signals with greater flexibility than the STFT. Different basis functions, or mother wavelets, may be used in wavelet analysis to achieve the best results for a specific application. The windowing process for the DWT is variable, allowing for good time resolution of high frequency components and good frequency resolution of low

frequency components in the same analysis. Thus, wavelet analysis can show how frequency content changes with time. This makes DWT an ideal tool for decomposition of drop test data. Detailed information about signal processing of transient loading and random vibration signals can be found in the text by Newland [25].

The accuracy of the wavelet decomposition technique needs more investigation for narrow-band signals, as is the case in dynamic structural response, especially when the response frequencies are not very close to the frequencies corresponding to each wavelet levels. Dujari, et al. [26] discussed these issues in the context of complicated vibration response histories, and similar investigations for drop testing will be reported in a future paper.

In the present study, DWT is combined with cycle counting methods to quantify damage for relatively simple signals in drop testing, as proposed earlier by Varghese and Dasgupta [9][12], and demonstrated by Lall, et al. [16]. For demonstration purposes, Figure A-10 shows the DWT decomposition of the strain response of a loosely clamped PWA subjected to out-of-plane impact. The input signal can be described as a noisy damped sinusoidal wave. Daubechies 5 wavelets are used because the shape of this wavelet basis function best matches the input signal. The decomposition is conducted for four levels, beyond which, there is significant loss of temporal resolution. The high frequency component, called “detail” and the low frequency component, called “approximation”, are obtained for each level. The contribution of each level can be clearly observed in Figure A-10. Levels 1, 2 and 3 carry the low amplitude, high strain rate part of the signal; while Level 4 carries the high amplitude, low strain rate component.

The strain history at each level is then quantified by using a cycle-counting technique to express the signal as a superposition of many constant-amplitude signals, each with a specific number of cycles. Each of the selected amplitude levels is designated as a 'bin'. The result is a range-distribution function (RDF) for strain at each wavelet level.

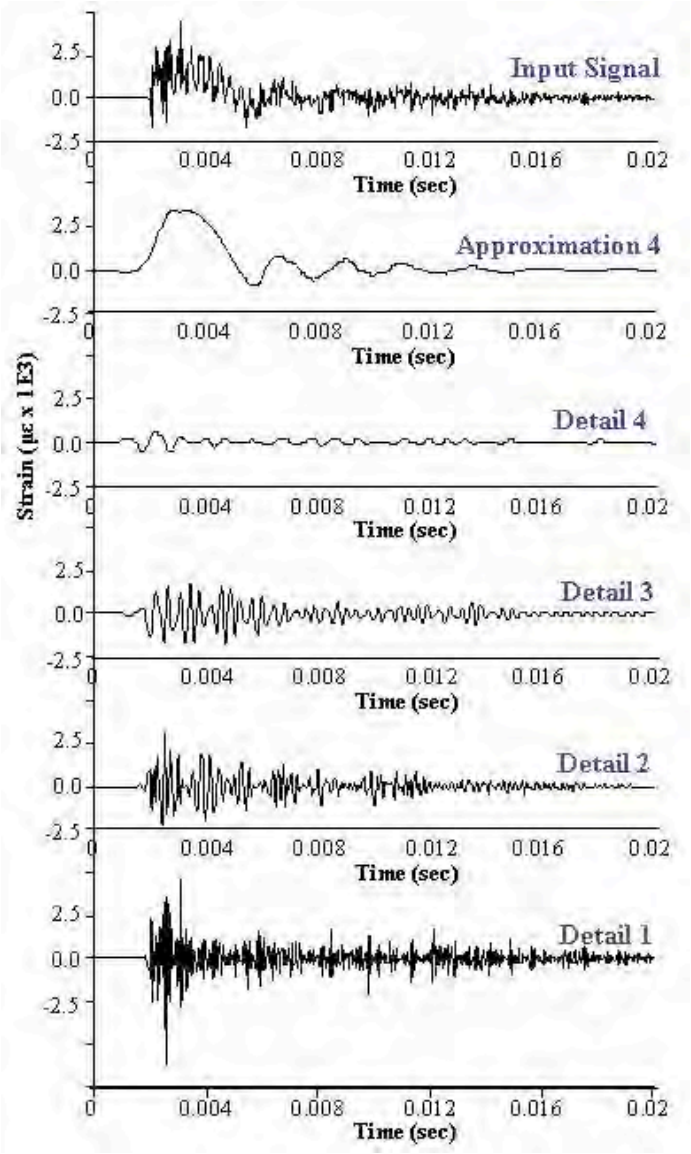

Figure A-10: Wavelet decomposition of PWA strain history.

A - 2.4 Finite Element Transfer Function

The local PWA response, obtained from the strain gage and accelerometer signals discussed in Section 2.2, has to be related to the stress history at the failure sites, so that the damage can be estimated using suitable damage models. In this study, a finite element model is used to obtain this transfer function. Wong, et al. [27] conducted a parametric study of board level drop test using FEA simulations and showed that peeling stress in the solder is the primary damage-inducing mechanism. The peeling stress in the solder is due to the curvature of the board and the inertial force of the component. Peeling stress increases linearly with increasing impact velocity, increases almost logarithmically with decreasing bump height, decreases asymptotically with increasing number of solder bumps, and increases with increasing PWA length.

In this study, the FEA transfer function is obtained by plotting the average peeling stress at the failure site with respect to the average PWA strain evaluated over the region of the strain gage. The averaging of the peeling stress decreases the dependence of the results on meshing approximation. The averaging technique is used extensively in the field of solder durability, but there are no standard averaging schemes. Various authors have reported different schemes for averaging the FEA results over a finite region. The averaging requires a trade off between loosing data resolution across a large region versus numerical errors in a very small region. The authors have chosen 20% of the solder cross-sectional length at the failure site to provide a qualitative estimate of stresses in the region. An ideal averaging scheme for solder stresses is a subject for future papers. The results of this study must be viewed within the context of this averaging scheme.

This FEA transfer function is then combined with the PWA strain RDF described

in section 2.3, to obtain the RDF of the peeling stress at the failure site.

A - 2.5 Durability Estimation Methodology

A simple, first-order failure model is proposed to quantify the damage in the interconnects. Since the failure in this study is by incremental crack propagation in the brittle intermetallic, the damage model has been motivated by Paris' law for cyclic fatigue crack propagation [28]:

$$\frac{da}{dN} = C_1(\Delta K)^p$$

where, $\Delta K = \alpha(\Delta\sigma)\sqrt{\pi a} = f_1(\Delta\sigma)$

Integrating for Number of cycles to failure:

$$N = \frac{a_f^{-((p/2)+1)} - a_i^{-((p/2)+1)}}{(-(p/2)+1)A\pi^{p/2}\alpha^p(\Delta\sigma)^p} = C_1(\Delta\sigma)^{-p} \quad \text{(A-1)}$$

Normalized damage in the solder for each cycle is related to the peeling stress by:

$$D = \frac{1}{N_f} = C_2(\Delta\sigma_{peeling})^p \quad \text{(A-2)}$$

The RDF of the peeling stress, discussed in Section 2.4, is described as:

$$(\Delta\sigma_{peeling})_i = [\sum_{j=1}^{r} n_j(\Delta\sigma_{peeling})_j]_i \quad \text{(A-3)}$$

Substituting Equations (3) in Equation (2), damage caused by the i^{th} response mode can be expressed as:

$$D_i = A_i[\sum_{j=1}^{r} n_j(\Delta\sigma_{peeling})_j]_i^p \quad \text{(A-4)}$$

Therefore, total damage per impact is given by:

$$D_{total} = \sum_{i=1}^{m} W_i \sum_{j=1}^{r} n_{ij} (\Delta\sigma_{peeling})_{ij}^{p} \quad \text{(A-5)}$$

Failure is assumed to finally occur when D_{total} reaches 1.

A - 3. Case Study

The methodology described above is demonstrated on a PWA test specimen. A simple test specimen is used to allow detailed study of the failure modes and failure mechanisms. The test vehicle is a 74mm × 40mm × 1.4mm FR4 board mounted with a 256 I/O, 0.88 mm diameter, 1.2 mm pitch PBGA (Figure A-11). The PBGA has a 27mm x 27mm x 0.5 mm FR4 substrate and a 24mm x 24mm x 1.1mm epoxy overmold, with eutectic Sn-Pb solder balls. The pad finish on the board side of the solder balls is Electroless Nickel Immersion Gold (ENIG) and that on the substrate side is 63Sn-37Pb.

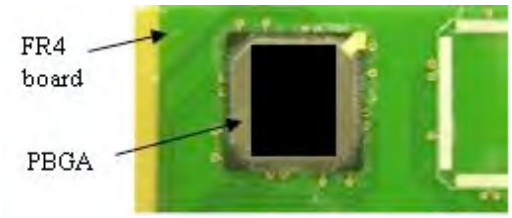

Figure A-11: Test specimen with component of interest.

The specimen is impacted using the pendulum test setup in the in-plane and out-of-plane orientations. The results of the flexural tests, as described in the test matrix, are discussed in this paper. The strain histories for out-of-plane and in-plane impacts are shown in Figure A-12 and Figure A-13 respectively. The strain histories are quite simple and lack the high frequency content seen in Figure 10.

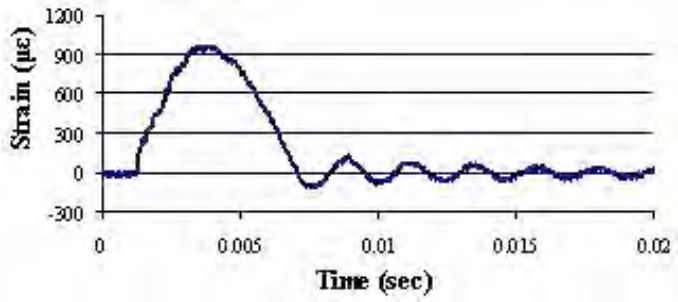

Figure A-12: PWA strain vs time for out-of-plane impact.

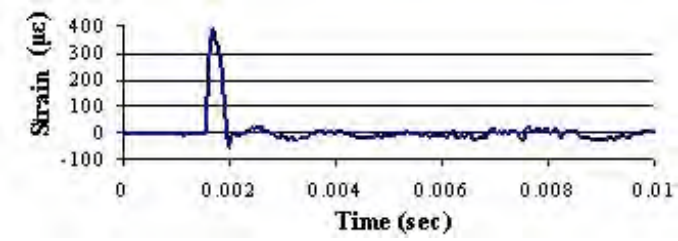

Figure A-13: PWA strain vs time for in-plane impact.

The test is repeated at each test condition to explore the consistency of data. The results, presented in Table A-3 and Figure A-14, show that the average number of impacts to failure has a monotonic relation to PWA flexural strain. The PWA flexural strain rates are around 10^0 sec^{-1}. Future papers will discuss the rate dependent effects of durability using tests conducted over wider range of PWA flexural strain rates.

Table A-3: Experimental results.

Case number	Impact Orientation	Peak PWA strain (με)	Average impacts to failure
1	In-plane	785	7
2	In-plane	1962	4
3	Out-of-plane	600	9
4	Out-of-plane	5613	1

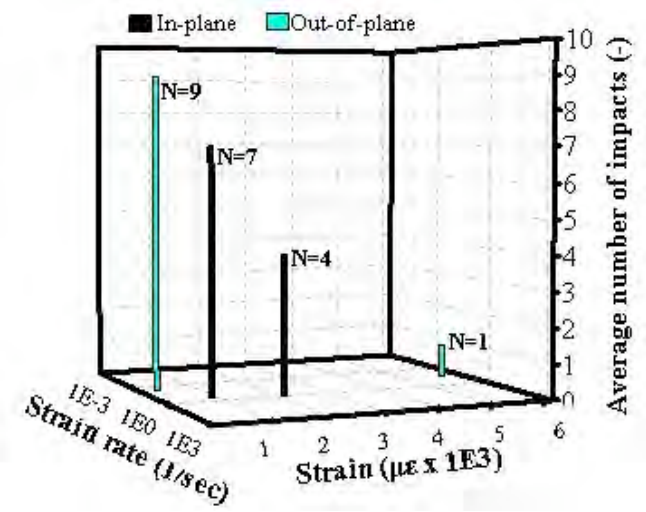

Figure A-14: Average number of impacts to failure for in-plane and out-of-plane impact testing shows a monotonic relationship to PWA strain.

The failure mechanism for all tests is fracture in the intermetallic layer on the PWA side (Figure A-15). This could be because the specimens were aged for nearly 24 months at room temperature. Aging causes the intermetallic thickness to increase to approximately 5 microns due to solid state diffusion. Studies by Jang, et al. [29] and Prakash and Sritharan [30] have shown that aging causes the failure site to change from the solder to the intermetallics.

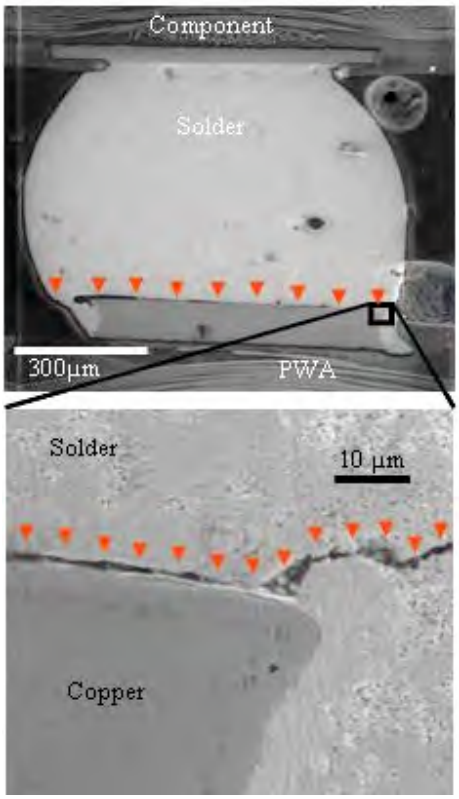

Figure A-15: Cross-sectioning picture shows that the failure site is at the intermetallics. The red arrows indicate the location and path of the crack.

Wavelet analysis and rainflow cycle counting is conducted on the test data. The resulting damage at each wavelet level is discussed later. The signals are dominated by mode 1 deformation.

A 2-D finite element model is generated using a commerically available software to obtain the FEA transfer function. 4-noded plane stress quadratic elements are used to model the specimen. The model is symmetric about the vertical axis, with 7408 elements and 8530 nodes. The mesh in the outermost interconnect is denser than in the inner interconnects (Figure A-16).

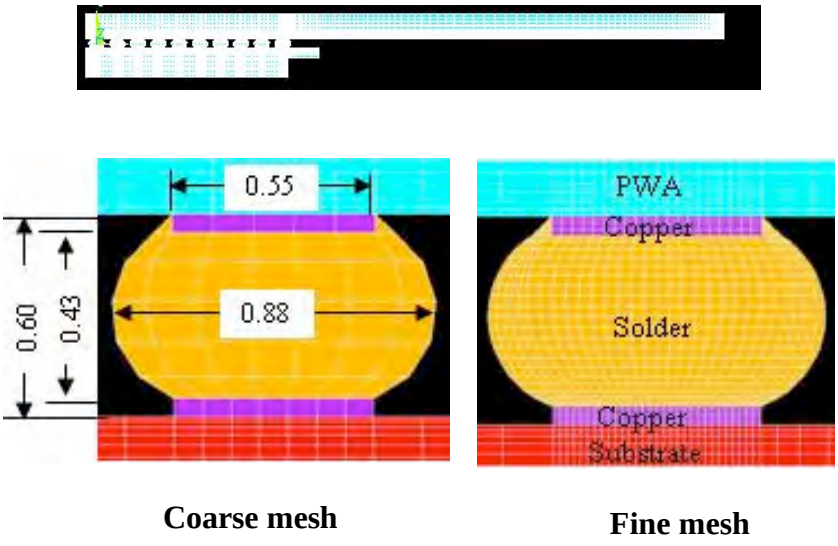

Figure A-16: 2D model of PWA with coarse mesh for inner solder balls and fine mesh for the outermost solder ball. All dimensions are in millimeters.

The mesh is scaled to provide maximum mesh density at regions of high stress gradients, for example at the solder/Cu pad interface, and at the Cu pad/PWA interface. Mesh convergence tests are conducted to optimize the mesh density for best results in the least computational time. Since our tests are conducted over a small range of strain-rates, the solder and copper trace are modeled as rate-independent bilinear materials. In future papers, where tests will be conducted over wider range of strain-rates, rate-dependent material properties will be used. All other materials are modeled as linear elastic. The material properties are listed in Table A-4.

Table A-4: Material Properties.

ELASTIC MATERIAL PROPERTIES			
Material	Elastic Modulus (GPa)	Poisson's Ratio (-)	Density (kg/m^3)
FR4	17.2	0.39	1000
Overmold	15.8	0.25	1900
Die	191	0.3	2330
Substrate	22	0.3	2800
Copper	120	0.34	8930
Sn-Pb solder	29.9	0.35	8400
PLASTIC MATERIAL PROPERTIES			
Material	Yield Stress (MPa)	Tangent Modulus (GPa)	
Copper	240	12	
Solder	32.7	2	

Figure A-17 shows a contour plot of the peeling stresses in the solder balls. The maximum stresses are in the outermost interconnect, at the interface between the solder and the copper pad on the PWA side. This is in agreement with the failure site obtained from the experiment. The curve shown in Figure A-18, is the transfer function needed to correlate PWA strain to the average peeling stress at the failure site.

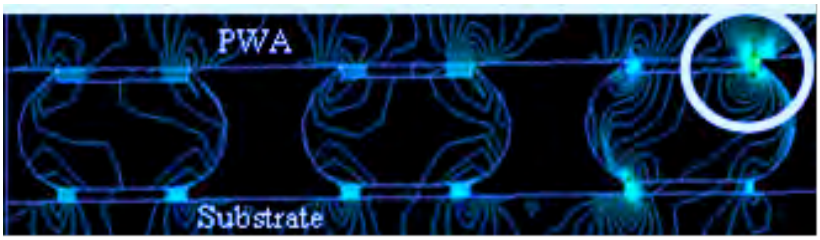

Figure A-17: Contour plot of peeling stress in the solder balls. The solder ball to the extreme right is the outermost solder ball. The region of maximum peeling stresses (encircled above) matches with the failure site from the experiments.

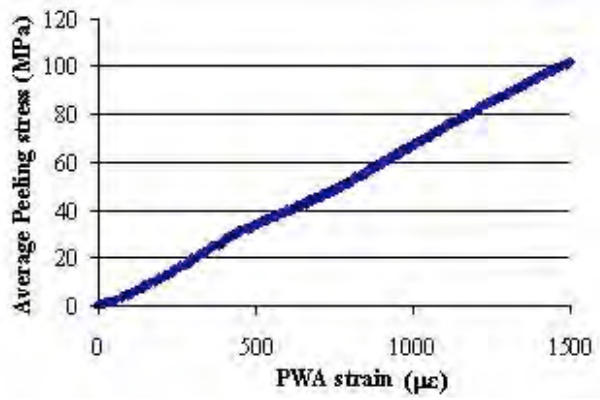

Figure A-18: Transfer function between peeling stress at the failure site and local flexural strain in the PWA.

As discussed in Section 2.5, damage per impact is given by Equation 5. The values of the unknown damage constants in Equation 5 are obtained from the results of the in-plane impact tests (cases 1 and 2 of Table A-3). The value of "W" is 80.13 and that of "p" is -0.611. For this approach to be generic, these constants should be independent of loading orientation and boundary conditions. This is verified in this study by evaluating their ability to predict the observed damage accumulation rate for a different type of loading (out-of-plane impact). In other words, the damage constants are used to calculate the durability for the out-of-plane impact tests, specifically, case 3 of Table A-3. Case 4 is an overstress failure and not used for the fatigue calculations. The calculated value of number of impacts to failure is 8.29, which agrees well with the experimental value of 9 impacts, as shown in Table A-3. *Thus, the methodology and the damage constants are*

independent of boundary conditions and impact orientation.

The damage calculations show that in the out-of-plane strain history, 94.3% of the interconnect damage is due to response in the first structural response mode. Although this is expected for the simple loading profile used in this study, it may not be so for complex loading histories.

The test data can be plotted in terms of peeling stress at the failure site and number of impacts to failure (Figure A-19). The durability shows a power law fit with the average peeing stress at the failure site. This verifies the generic nature of the damage constants and the use of peeling stress as a damage metric.

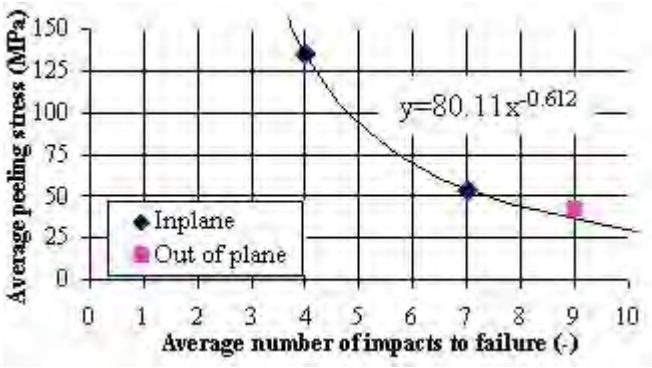

Figure A-19: Durability shows a power-law fit with the average peeling stress at the failure site.

A - 4. Discussion

It is generally difficult to correlate the board level drop test results to product level drop test results. The PWA is clamped to the fixture during board level drop testing and is allowed to vibrate after a single drop event. Product level drop testing usually involves multiple impacts and rotations after the first impact, termed as clattering. High-speed photography by Goyal and Buratynski [2] indicates that during a single product level drop event, one corner of the electronic product touches down first and there is

"clattering" as other corners strike repeatedly. The product then bounces or comes to rest after undergoing these multiple impacts at its ends. It has been shown that during clattering, the product can experience velocity shocks that are several times higher than those experienced in a single drop event. The details of the clattering motion, and the various impact parameters of interest to the designer (change in velocities and impulses, the duration of the clatter, et cetera) depend significantly on the mass distribution of the product and its effective coefficient of restitution at impact [31]. The mass distribution and boundary conditions of the PWAs used in the JEDEC board level drop tests is different from the PWAs mounted in an actual portable electronic device.

One of the factors that make correlation of board level and product level JEDEC drop test data difficult is the use of damage metrics that are very structure-specific, for example: incident force, incident kinetic energy, incident velocity. This paper quantifies damage in terms of the stresses at the failure site, caused by the local PWA response during the impact event. This makes the damage constants in Figure 19 independent of drop orientation and boundary conditions. Wavelet analysis, in conjunction with rainflow cycle counting analysis, can be used to decompose the complex PWA response associated with clattering. Thus, for a given failure mechanism, the proposed test methodology and damage constants can be used to extrapolate the board level test results to field conditions.

However, there are certain limitations to the application of the proposed drop test methodology. Goyal, et al. [32] showed that the impulses associated with individual clatter impacts are very significant because it could lead to resonances in the internal components. This may not be captured by the board level drop tests. Experimental work

by Goyal, et al. [33] also indicates that constraining the internal assembly to behave as a single system, as is done in board level drop tests, may even miss important failure mechanisms. The proposed drop test methodology is not a replacement for product level drop testing. Rather, it is a tool to bring about a better correlation between board and product level drop testing.

A - 5. Conclusion and Future Work

A generic methodology is presented to determine the drop durability of surface mount interconnects of PWAs. The proposed method combines impact testing, measurement of local PWA response, time-frequency decomposition to quantify the response histories, finite element simulations to assess the stress history at the failure site under the given response, and a damage model to predict durability for the given failure mechanism. A case study is presented for a PBGA assembly. Test data are presented for both in-plane and out-of-plane loading. The methodology and the resulting damage constants are demonstrated to be independent of boundary conditions and impact orientation, thus making the methodology quite generic.

In addition to estimating the durability of electronic packages under test conditions, the proposed methodology can also be used to extrapolate results to field conditions, and to quantitatively compare and rank the impact resistance of different styles of surface mount interconnects.

Future work will focus on the influence of PWA flexural strain rate on the durability and failure site of surface mount interconnects. The effectiveness of the wavelet signal processing technique for characterizing drop structural response will also

be investigated.

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References

[1] JEDEC Standard JESD22-B104-B, Mechanical Shock, 2001.

[2] Goyal, S., Buratynski, E., Methods For Realistic Drop Testing: International Journal Of Microcircuits And Electronic Packaging, Vol. 23, No 1, 2000.

[3] Lim, C.T., Low Y.J., Investigating The Drop Impact Of Portable Electronic Products, Electronic Components and Technology Conference, 2002.

[4] Lim, C.T., Ang, C.W., Tan, L.B., Seah, S.K.W., Wong, E.H., Drop Impact Survey Of Portable Electronic Products, Electronic Components and Technology Conference, 2003.

[5] Seah, S.K.W., Lim, C.T., Wong, E.H., Tan, V.B.C., Shim V.P.W., Mechanical Response Of PCBs In Portable Electronic Products During Drop Impact, Electronic Packaging and Technology Conference, 2002

[6] JEDEC Standard JESD22-B111, Board Level Drop Test Method Of Components For Handheld Electronic Products, 2001.

[7] Yu, Q., Kikuchi, H., Ikeda, S., Shiratori, M., Kakino, M., Fujiwara, N., Dynamic Behavior Of Electronics Package And Impact Reliability Of BGA Solder Joints, Proceedings of the Intersociety Conference On Thermal Phenomena, 2002.

[8] Juso, H., Yamaji, Y., Kimura, T., Fujita K., Kada, M., Board Level Reliability Of CSP, Electronic Components and Technology Conference, 1998.

[9] Varghese, J., Dasgupta, A.; Test Tailoring Methodology for Impact Testing of Portable Electronic Products, Proceedings of IMAC-XXI Conference on Structural Dynamics, 2003.

[10] Varghese, J., Dasgupta, A.; Failure Site Transition During Drop Testing of Printed Wiring Assemblies, Proceedings of ASME InterPACK Conference, 2005.

[11] Heaslip, G., Punch, J., Rodgers, B., Ryan, C., Reid, M., A Simulated and Experimental Comparison Of Lead-Free and Tin-Lead Solder Interconnect Failure Under Impact Stimuli, Proceedings of ASME InterPACK Conference, 2005.

[12] Varghese, J., Dasgupta, A.; Test Methodology for Impact Testing of Portable Electronic Products, Proceedings of ASME International Mechanical Engineering Congress and Exposition, Washington D.C., 2003.

[13] Tee T.Y., Ng, H.S., Lim, C.T., Pek, E., Zhong, Z., Board Level Drop Test And Simulation Of TFBGA Packages For Telecommunication Applications, Electronic Components and Technology Conference, 2003

[14] Heaslip, G.M., Punch, J., Analysis of Experimental Shock and Impact Response Data of a Printed Wire Board, Proceedings of the ASME International Mechanical Engineering Congress and Exposition, Washington DC, 2003.

[15] Zhu L., Marcinkiewicz W., Drop Impact Reliability Analysis Of CSP Packages At Board And Product System Levels Though Modeling Approaches, Intersociety Conference On Thermal Phenomena, 2004.

[16] Lall, P., Panchagade, D., Choudhary, P., Suhling ,J., Gupte, S., Models For Shock And Vibration Survivability Of Electronic And MEMS Packaging, Proceedings of ASME InterPACK Conference, 2005.

[17] Tan, L.B., Seah, S.K.W., Wong, E.H., Zhang, X., Tan, V.B.C., Lim, C.T., Board Level Solder Joint Failures By Static And Dynamic Loads, Electronics Packaging Technology, 2003

[18] Sherf, Z., Hopstone, P.; Ostrovski, G.; Klein, R.; Ben, D., Problems In The Analysis Of A Shock Sequence With Application To Gunfire Analysis And Simulation, Journal Of The IEST, V 45, N SPEC., 2002

[19] Schaeffel, J. A. Jr., Finite Element Analysis Of Launch Induced Stresses In TOW Missile Digital Electronic Unit Microprocessor Crystals, Collection Of Technical Papers - AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics & Materials Conference, N 4, AIAA-94-1615-CP, 1994

[20] Uenishi, K., Matsuhisa, H., Utsuno, H., Park, J., Impact Reduction Of An Automotive Occupant By "Ride Down" Effect In Head-On Collision, Transactions Of The Japan Society Of Mechanical Engineers, Part C, V 70, N 9, 2004

[21] Jacobsen, K., Tyrell, D., Periman, B., Rail Car Impact Tests With Steel Coil: Collision Dynamics, Proceedings Of IEEE/ASME Joint Rail Conference, 2003.

[22] Ettemeyer, A., Schreiber, D.; Voelzer, W., Strain Analysis On Ductile Cast Iron Containers At Drop Test Conditions, Nuclear Engineering And Design, Vol.172, No.3, 1997.

[23] Ferman, M. A., Unger, W. H.; Saff, C. R.; Richardson, M. D. , New Approach To

Durability Prediction For Fuel Tank Skins, Journal Of Aircraft, V 23, N 5, 1986.

[24] Mansfields, N. J., Holmlund, P., Lundstrog M, Comparison Of Subjective Responses To Vibration And Shock With Standard Analysis Methods And Absorbed Power, Journal Of Sound And Vibration, v230, n 3, 2000

[25] Newland, D.E., An Introduction to Random Vibrations, Spectral & Wavelet Analysis; 3rd Edition, Addison Wesley, 1996.

[26] Dujari, P., Upadhyayula, K., Dasgupta, A., and Balachandran, B., Applications of Wavelets for Cost-Effective Vibration Response Analysis of Electronic Circuit Card Assemblies, Experimental/Numerical Mechanics in Electronic Packaging Proceedings, Society of Experimental Mechanics, Bellevue, WA, pp. 67-74, June 2-4, 1997

[27] Wong, E.H., Lim, K.M., Lee, N., Seah, S., Hoe, C., Wang, J., Drop Impact Test – Mechanics And Physics Of Failure, Electronics Packaging Technology Conference, 2002.

[28] Dieter, G.E., Mechanical Metallurgy, 3rd edition, McGraw Hill Book Company – Singapore, p 398

[29] Jang, J-W; De Silva, A. P.; Lin, J-K; Frear, D. R., Tensile fracture behaviors of solid-state-annealed eutectic SnPb and lead-free solder flip chip bumps, Journal of Materials Research, v 19, n 6, June, 2004, p 1826-1834

[30] Prakash, K.H.; Sritharan, T., Tensile fracture of tin-lead solder joints in copper, Materials Science and Engineering A, v 379, n 1-2, Aug 15, 2004, p 277-285

[31] Goyal, S., Papadopoulos, J.M., Sullivan, P.A., The Dynamics Of Clattering I:

Equation Of Motion And Examples; Journal Of Dynamic Systems, Measurement, And Control, Vol 120, Pp 83-93, March 1998.

[32] Goyal, S., Papadopoulos, J.M., Sullivan, P.A., The Dynamics Of Clattering II: Equation Of Motion And Examples; Journal Of Dynamic Systems, Measurement, And Control, Vol 120, Pp 94-102, March 1998.

[33] Goyal, S., Upasani, S., Patel, D.M., Improving Impact Tolerance Of Portable Electronic Products: Case Study Of Cellular Phones; Experimental Mechanics

References

[1]. J.H. Lau, Low Cost Flip Chip Technologies: For Dca, Wlcsp, and PBGA Assemblies. 2000: McGraw-Hill.

[2]. Q. Yu, H. Kikuchi, S. Ikeda, M. Shiratori, M. Kakino, and N. Fujiwara. Dynamic Behavior of Electronics Package and Impact Reliability of BGA Solder Joints. Thermomechanical Phenomena in Electronic Systems -Proceedings of the Intersociety Conference, 2002. San Diego, CA, United States. p. 953-960

[3]. R. Darveaux, C. Reichman, and N. Islam. Interface Failure in Lead Free Solder Joints. Proceedings - Electronic Components and Technology Conference, 2006. p. 906-917

[4]. J. Varghese and A. Dasgupta. Failure Site Transition During of Printed Wiring Assemblies. Proceedings of the ASME/Pacific Rim Technical Conference and Exhibition on Integration and Packaging of MEMS, NEMS, and Electronic Systems: Advances in Electronic Packaging 2005, 2005. San Francisco, CA, United States. p. 845-848

[5]. W.J. Plumbridge and C.R. Gagg, Effects of Strain Rate and Temperature on the Stress–Strain Response of Solder Alloys Journal of Material Science: Materials in Electronics, 1999. 10(5): p. 461-468.

[6]. JEDEC Solid State Technology Association, JESD22-B104-B: Mechanical Shock, 2001

[7]. S. Goyal, J.M. Papadopoulos, and P.A. Sullivan, Shock Protection of Portable Electronic Products: Shock Response Spectrum, Damage Boundary Approach, and Beyond. Shock and Vibration, 1997. 4(3): p. 169-191.

[8]. C.T. Lim and Y.J. Low. Investigating the Drop Impact of Portable Electronic Products. Proceedings - Electronic Components and Technology Conference, 2002. San Diego, CA. p. 1270-1274

[9]. JEDEC Solid State Technology Association, JESD22-B111: Board Level Drop Test Method of Component for Handheld Electronic Products, 2001

[10]. J. Varghese and A. Dasgupta. Test Methodology for Impact Testing of Portable Electronic Products. American Society of Mechanical Engineers, EEP, 2003. Washington, DC, United States. p. 71-77

[11]. J. Varghese, B. Song, M.H. Azarian, A. Dasgupta, and M. Pecht. Failure Site Transition During Drop Testing of Printed Wiring Assemblies. American Society of Mechanical Engineers, Electronic and Photonic Packaging, EPP, 2005. Orlando, FL, United States. p. 139-146

[12]. T.Y. Tee, H.S. Ng, C.T. Lim, E. Pek, and Z. Zhong, Impact Life Prediction Modeling of Tfbga Packages under Board Level Drop Test. Microelectronics Reliability, 2004. 44(7): p. 1131-1142.

[13]. Z. Sherf, P. Hopstone, G. Ostrovski, R. Klein, and D. Ben, Problems in the Analysis of a Shock Sequence with Application to Gunfire Analysis and Simulation. Journal of the IEST, 2002. 45(SPEC): p. 161-177.

[14]. J.A. Schaeffel, Jr. Finite Element Analysis of Launch Induced Stresses in Tow Missile Digital Electronic Unit Microprocessor Crystals. Collection of Technical Papers - AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics & Materials Conference, 1994. Hilton Head, SC, USA. p. 2360-2370

[15]. K. Uenishi, H. Matsuhisa, H. Utsuno, and J.G. Park, Impact Reduction of an Automotive Occupant By "Ride Down" Effect in Head-on Collision. Nippon Kikai Gakkai Ronbunshu, C Hen/Transactions of the Japan Society of Mechanical Engineers, Part C, 2004. 70(9): p. 2624-2630.

[16]. K. Jacobsen, D. Tyrell, and B. Perlman. Rail Car Impact Tests with Steel Coil: Collision Dynamics. Proceedings of the IEEE/ASME Joint Railroad Conference, 2003. Chicago, IL, United States. p. 73-82

[17]. Ettemeyer, D. Schreiber, and W. Volzer, Strain Analysis on Ductile Cast Iron Containers at Drop Tests. Nuclear Engineering and Design, 1997. 172(3): p. 309-315.

[18]. M.A. Ferman, W.H. Unger, C.R. Saff, and M.D. Richardson, New Approach to Durability Prediction for Fuel Tank Skins. Journal of Aircraft, 1986. 23(5): p. 431-437.

[19]. N.J. Mansfield, P. Holmlund, and R. Lundstrom, Comparison of Subjective Responses to Vibration and Shock with Standard Analysis Methods and Absorbed Power. Journal of Sound and Vibration, 2000. 230(3): p. 477-491.

[20]. S. Goyal, S. Upasani, and D.M. Patel, Role of Case-Rigidity in Drop-Tolerance of Portable Products. International Journal of Microcircuits and Electronic Packaging, 1999. 22(2): p. 175-184.

[21]. S.K.W. Seah, C.T. Lim, E.H. Wong, V.B.C. Tan, and V.P.W. Shim. Mechanical Response of Pcbs in Portable Electronic Products During Drop Impact. Proceedings - Electronics Packaging Technology Conference, 2002. p. 120-125

[22]. S. Goyal, S.S. Upasani, and D.M. Patel, Designing Best-in-Class Impact-Tolerant Cellular Phones and Other Portable Products. Bell Labs Technical Journal, 1998. 3(3): p. 159-174.

[23]. S. Goyal, J.M. Papadopoulos, and P.A. Sullivan, The Dynamics of Clattering. I: Equation of Motion and Examples. Journal Of Dynamic Systems, Measurement, And Control, 1998. 120(1): p. 83-93.

[24]. S. Goyal, J.M. Papadopoulos, and P.A. Sullivan, The Dynamics of Clattering. Ii: Global Results and Shock Protection. Journal Of Dynamic Systems, Measurement, And Control, 1998. 120(1): p. 94-102.

[25]. K.H. Low, Drop-Impact Cushioning Effect of Electronics Products Formed by Plates. Advances in Engineering Software, 2003. 34(1): p. 31-50.

[26]. L. Hua, Y.Y. Wang, and T.Y. Lin, Drop-Impact Simulation and Experimental Verification for Spindle Fixation of Video and Audio Module. Mechatronics, 2003. 13(5): p. 427-440.

[27]. L. Zhu. Modeling-Technique for Reliability Assessment of Portable Electronic Product Subjected to Drop Impact Loads. Proceedings - Electronic Components and Technology Conference, 2003. New Orleans LA, United States. p. 100-104

[28]. K.H. Low, A. Yang, K.H. Hoon, X. Zhang, J.K.T. Lim, and K.L. Lim, Initial Study on the Drop-Impact Behavior of Mini Hi-Fi Audio Products. Advances in Engineering Software, 2001. 32(9): p. 683-693.

[29]. C.T. Lim, C.W. Ang, L.B. Tan, S.K.W. Seah, and E.H. Wong. Drop Impact Survey of Portable Electronic Products. Proceedings - Electronic Components and Technology Conference, 2003. p. 113-120

[30]. S. Goyal, S. Upasani, and D.M. Patel, Improving Impact Tolerance of Portable Electronic Products: Case Study of Cellular Phones. Experimental Mechanics, 1999. 39(1): p. 43-52.

[31]. E.H. Wong, K.M. Lim, N. Lee, S. Seah, C. Hoe, and J. Wang. Drop Impact Test - Mechanics & Physics of Failure. Proceedings - Electronics Packaging Technology Conference, 2002. p. 327-333

[32]. L. Jing-en, T. Tong Yan, E. Pek, L. Chwee Teck, and Z. Zhaowei. Modal Analysis and Dynamic Responses of Board Level Drop Test. Proceedings - Electronics Packaging Technology, 2003. p. 233-243

[33]. Y.Q. Wang, K.H. Low, F.X. Che, H.L.J. Pang, and S.P. Yeo. Modeling and Simulation of Printed Circuit Board Drop Test. Proceedings - Electronics Packaging Technology, 2003. p. 263-268

[34]. N. Fong Kuan, L. Chwee Teck, E. Pek, L. Jing-En, and T. Tong Yan. Study of PCB Strains and Component Position under Board Level Drop Test. Proceedings - Electronic Packaging Technology Conference, 2005. p. 7 pp.

[35]. P. Lall, D. Panchagade, Y. Liu, W. Johnson, and J. Suhling. Models for Reliability Prediction of Fine-Pitch Bgas and Csps in Shock and Drop-Impact. Proceedings - Electronic Components and Technology Conference, 2004. Las Vegas, NV, United States. p. 1296-1303

[36]. E.H. Wong, R. Rajoo, Y.W. Mai, S.K.W. Seah, K.T. Tsai, and L.M. Yap. Drop Impact: Fundamentals and Impact Characterisation of Solder Joints. Proceedings - Electronic Components and Technology Conference, 2005. Lake Buena Vista, FL, United States. p. 1202-1209

[37]. J. Varghese and A. Dasgupta. Drop Testing of Printed Wiring Assemblies. Proceedings of the 2005 SEM Annual Conference and Exposition on Experimental and Applied Mechanics, 2005. Portland, OR, United States. p. 1591-1595

[38]. S.K.W. Seah, E.H. Wong, Y.W. Mai, R. Rajoo, and C.T. Lim. High-Speed Bend Test Method and Failure Prediction for Drop Impact Reliability. Proceedings - Electronic Components and Technology Conference, 2006. p. 6 pp.

[39]. D. Reiff and E. Bradley. A Novel Mechanical Shock Test Method to Evaluate Lead-Free BGA Solder Joint Reliability. Proceedings - Electronic Components and Technology Conference, 2005. Lake Buena Vista, FL, United States. p. 1519-1525

[40]. P. Marjamaki, T.T. Matilla, and J. Kivilahti. A Comparative Study of the Failure Mechanisms Encountered in Drop and Large Amplitude Vibration Tests. Proceedings - Electronics Packaging Technology Conference, 2006. p. 95-101

[41]. L.B. Tan, S.K.W. Seah, E.H. Wong, Z. Xiaowu, V.B.C. Tan, and C.T. Lim. Board Level Solder Joint Failures by Static and Dynamic Loads. Proceedings-Electronics Packaging Technology Conference 2003. p. 244-251

[42]. P. Geng, P. Chen, and L. Yun. Effect of Strain Rate on Solder Joint Failure under Mechanical Load. Proceedings - Electronic Components and Technology Conference, 2002. p. 974-978

[43]. L. Jing-en, T. Tong Yan, G. Kim Yong, N. Hun Shen, X. Baraton, R. Bronner, M. Sorrieul, E. Hussa, T. Reinikainen, and A. Kujala. Drop Impact Life Prediction Model for Lead-Free BGA Packages and Modules. 2005. p. 559-565

[44]. G. Yu and D. Jin. Drop Test Simulation and Doe Analysis for Design Optimization of Microelectronics Packages. Proceedings - Electronic Components and Technology Conference, 2006. p. 6 pp.

[45]. S.-W.R. Lee, Y.-L.T. Li, and H.-W.B. Lui. Experimental Evaluation on Solder Joint Reliability of PBGA Assembly under Mechanical Drop Test. American Society of Mechanical Engineers, EEP, 2002. New Orleans, LA, United States. p. 181-185

[46]. G.M. Heaslip, J.M. Punch, B.A. Rodgers, and C. Ryan. Board Level Drop Tests Comparing Lead-Free and Eutectic Solder Interconnects on a BGA Package for Mobile Ict Applications. American Society of Mechanical Engineers, Electronic and Photonic Packaging, EPP, 2004. Anaheim, CA, United States. p. 353-362

[47]. G. Heaslip, J. Punch, B. Rodgers, C. Ryan, and M. Reid. A Simulated and Experimental Comparison of Lead-Fre and Tin-Lead Solder Interconnect Failure under Impact Stimuli. Proceedings of the ASME/Pacific Rim Technical Conference and Exhibition on Integration and Packaging of MEMS, NEMS, and Electronic Systems: Advances in Electronic Packaging 2005, 2005. San Francisco, CA, United States. p. 1283-1291

[48]. L. Yi-Shao, P.C. Chen, Y. Chang-Lin, and J.C.B. Lee. The Effect of Imc Microstructure of Solder Joint on the Mechanical Drop Performance in Snxagcu and Snagcux CSP Package. Proceedings - Electronic Components and Technology Conference, 2006. p. 1935-1939

[49]. E. Ibe, K. Loh, J.-E.N. Luan, and T.Y. Tee, Underfill Effects on BGA Drop, Bend, and Thermal Cycle Tests. Advanced Packaging, 2005. 14(2): p. 28-30.

[50]. T.T. Mattila, P. Marjamäki, L. Nguyen, and J.K. Kivilahti. Reliability of Chip Scale Packages under Mechanical Shock Loading. Proceedings - Electronic Components and Technology Conference, 2006. p. 584-589

[51]. S.K.W. Seah, E.H. Wong, Y.W. Mai, R. Rajoo, and C.T. Lim. Failure Mechanisms of Interconnections in Drop Impact. Proceedings - Electronic Components and Technology Conference, 2006. p. 1484-1492

[52]. D.Y.R. Chong, K. Ng, J.Y.N. Tan, P.T.H. Low, J.H.L. Pang, and F.X. Che. Drop Test Reliability Assessment of Leaded and Lead-Free Solder Joints for Ic Packages. Proceedings of 6th Electronics Packaging Technology Conference, EPTC 2004, 2004. Singapore, Singapore. p. 210-217

[53]. D.Y.R. Chong, F.X. Che, L.H. Xu, H.J. Toh, J.H.L. Pang, B.S. Xiong, and B.K. Lim. Performance Assessment on Board-Level Drop Reliability for Chip Scale Packages (Fine-Pitch BGA). Proceedings - Electronic Components and Technology Conference, 2006. p. 356-363

[54]. T.C. Chai, S. Quek, W.Y. Hnin, E.H. Wong, J. Chia, Y.Y. Wang, Y.M. Tan, and C.T. Lim. Board Level Drop Test Reliability of Ic Packages. Proceedings - Electronic Components and Technology Conference, 2005. Lake Buena Vista, FL, United States. p. 630-636

[55]. X. Luhua and J.H.L. Pang. Effect of Intermetallic and Kirkendall Voids Growth on Board Level Drop Reliability for Snagcu Lead-Free BGA Solder Joint. Proceedings - Electronic Components and Technology Conference, 2006. p. 275-282

[56]. T. Dewen, C. Hongtao, and W. Chunqing. Effect of Thermal Aging on Microstructure, Shear and Mechanical Shock Failures for Solder Ball Bonding Joint. Proceedings - Electronic Packaging Technology Conference, 2005. p. 663-669

[57]. Q. Yu, H. Kikuchi, S. Ikeda, M. Shiratori, M. Kakino, and N. Fujiwara. Dynamic Behaviour of Electronics Package and Impact Reliability of BGA Solder Joints. Structures and Materials, 2003. Maui, HI, United States. p. 55-64

[58]. H. Juso, Y. Yamaji, T. Kimura, K. Fujita, and M. Kada. Board Level Reliability of CSP. Proceedings - Electronic Components and Technology Conference, 1998. p. 525-531

[59]. Z. Liping and W. Marcinkiewicz. Drop Impact Reliability Analysis of CSP Packages at Board and Product System Levels through Modeling Approaches. Procedings - Thermal and Thermomechanical Phenomena in Electronic Systems, 2004. p. 296-303 Vol.2

[60]. S. Groothuis, C. Chen, and R. Kovacevic. Parametric Investigation of Dynamic Behavior of Fbga Solder Joints in Board-Level Drop Simulation. Proceedings - Electronic Components and Technology Conference, 2005. Lake Buena Vista, FL, United States. p. 499-503

[61]. Z. Junfeng and L.J. Garner. Mechanical Modeling and Analysis of Board Level Drop Test of Electronic Package. Proceedings - Electronic Components and Technology Conference, 2006. p. 436-442

[62]. G. Jie, C.T. Lim, and A.A.O. Tay. Equivalent Solder Joint and Equivalent Layer Models for the Simulation of Solder Column Failure under Drop Impact.

Proceedings of 6th Electronics Packaging Technology Conference, EPTC 2004, 2004. Singapore, Singapore. p. 547-552

[63]. J. Gu, C.T. Lim, and A.A.O. Tay. Simulation of Mechanical Response of Solder Joints under Drop Impact Using Equivalent Layer Models. Proceedings - Electronic Components and Technology Conference, 2005. Lake Buena Vista, FL, United States. p. 491-498

[64]. P. Lall, D.R. Panchagade, Y. Liu, R.W. Johnson, and J.C. Suhling, Models for Reliability Prediction of Fine-Pitch Bgas and Csps in Shock and Drop-Impact. IEEE Transactions on Components and Packaging Technologies, 2006. 29(3): p. 464-474.

[65]. T.Y. Tee, N. Hun Shen, and Z. Zhaowei. Design for Enhanced Solder Joint Reliability of Integrated Passives Device under Board Level Drop Test and Thermal Cycling Test. Proceedings - Electronics Packaging Technology Conference, 2003. p. 210-216

[66]. J.-E. Luan, T.Y. Tee, K.Y. Goh, H.S. Ng, X. Baraton, R. Bronner, M. Sorrieul, E. Hussa, T. Reinikainen, and A. Kujala. Drop Impact Life Prediction Model for Lead-Free BGA Packages and Modules. Proceedings of the 6th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems - EuroSimE 2005, 2005. Berlin, Germany. p. 559-565

[67]. T.Y. Tee, L. Jing-en, and N. Hun Shen. Development and Application of Innovational Drop Impact Modeling Techniques. Proceedings - Electronic Components and Technology Conference, 2005. p. 504-512 Vol. 1

[68]. J.H.L. Pang and F.X. Che. Drop Impact Analysis of Sn-Ag-Cu Solder Joints Using Dynamic High-Strain Rate Plastic Strain as the Impact Damage Driving Force. Proceedings - Electronic Components and Technology Conference, 2006. p. 49-54

[69]. K.R. Shah and M. Mello. Ball Grid Array Solder Joint Failure Envelope Development for Dynamic Loading. Proceedings - Electronic Components and Technology Conference, 2004. p. 1067-1074 Vol.1

[70]. J. Varghese and A. Dasgupta. Test Methodology for Impact Testing of Portable Handheld Devices. Proceedings - International Modal Analysis Conference on Structural Dynamics, 2003. Orlando, Florida, USA. p.

[71]. T.Y. Tee, H.S. Ng, C.T. Lim, E. Pek, and Z. Zhong. Board Level Drop Test and Simulation of Tfbga Packages for Telecommunication Applications. Proceedings - Electronic Components and Technology Conference, 2003. New Orleans LA, United States. p. 121-129

[72]. P. Lall, N. Islam, and J. Suhling. Prognostication and Health Monitoring of Leaded and Lead Free Electronic and Mems Packages in Harsh Environments. Proceedings - Electronic Components and Technology Conference, 2005. p. 1305-1313

[73]. J. Varghese and A. Dasgupta, An Experimental Approach to Characterize Rate-Dependent Failure Envelopes and Failure Site Transitions in Surface Mount Assemblies. Microelectronics Reliability, 2006. doi:10.1016 / j.microrel.2006.07.002..

[74]. S. Goyal and E.K. Buratynski, Methods for Realistic Drop-Testing. International Journal of Microcircuits and Electronic Packaging, 2000. 23(1): p. 45-52.

[75]. C.-L. Yeh and Y.-S. Lai. Transient Analysis of Board-Level Drop Response of Lead-Free Chip-Scale Packages with Experimental Verifications. Proceedings - Electronics Packaging Technology Conference, 2004. Singapore, Singapore. p. 695-700

[76]. Y. Chang-Lin, T. Tsung-Yueh, and L. Yi-Shao. Response Spectra Analysis for Transient Structural Responses of Board-Level Electronic Packages Subjected to Half-Sine Impact Acceleration Pulses. Proceedings - Electronic Packaging Technology Conference, 2005. p. 8 pp.

[77]. Y. Chang-Lin and L. Yi-Shao. Impact Force Characteristics of Package-Level Solder Joints under Ball Impact Test. Proceedings - Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, 2006. p. 1-7

[78]. C.-L. Yeh and Y.-S. Lai. Insights into Correlation between Board-Level Drop Reliability and Package-Level Ball Impact Test. Proceedings - Electronic Components and Technology Conference, 2006. p. 455-461

[79]. J.W. Jang, A.P. De Silva, J.K. Lin, and D.R. Frear, Tensile Fracture Behaviors of Solid-State-Annealed Eutectic Snpb and Lead-Free Solder Flip Chip Bumps. Journal of Materials Research, 2004. 19(6): p. 1826-1834.

[80]. K.H. Prakash and T. Sritharan, Tensile Fracture of Tin–Lead Solder Joints in Copper. Materials Science & Engineering A: Structural Materials: Properties, Microstructure and Processing, 2004. 379(1-2): p. 277-285.

[81]. G.E. Dieter, Mechanical Metallurgy 1988, New York: McGraw-Hill Book Company.

[82]. C.R. Siviour, D.M. Williamson, S.J.P. Palmer, S.M. Walley, W.G. Proud, and J.E. Field, Dynamic Properties of Solders and Solder Joints. Journal de Physique IV, 2003. 110: p. 477-82.

[83]. X.Q. Shi, W. Zhou, H.L.J. Pang, and Z.P. Wang, Effect of Temperature and Strain Rate on Mechanical Properties of 63sn/37pb Solder Alloy. ASME Journal of Electronic Packaging, 1999. 121(3): p. 179–186.

[84]. W.J. Plumbridge and C.R. Gagg, Effects of Strain Rate and Temperature on the Stress–Strain Response of Solder Alloys. Journal of Material Science: Materials in Electronics, 1999. 10(5): p. 461-468.

[85]. Song, Identification of Failure Mechanisms Relevant to Stacked Die Components, M.S. thesis in Mechanical Engineering. 2006, University of Maryland.

[86]. Song, M.H. Azarian, J. Varghese, A. Dasgupta, and M. Pecht, Dynamic Loading Durability and Failure Site Transition in Enig-Sn37pb Interconnects in a Stacked-Die BGA Package. IEEE Transactions on Components and Packaging Technologies, 2006. Submitted for publication.

[87]. Zribi, R.R. Chromik, R. Presthus, K. Teed, L. Zavalij, J. DeVita, J. Tova, E.J. Cotts, J.A. Clum, and R. Erich, Solder Metallization Interdiffusion in Microelectronicinterconnects. IEEE Transactions on Components and Packaging Technologies, 2000. 23(2): p. 383-387.

[88]. M. Li, K.Y. Lee, D.R. Olsen, W.T. Chen, B.T.C. Tan, and S. Mhaisalkar, Microstructure, Joint Strength and Failure Mechanisms of Snpb and Pb-Free

Solders in BGA Packages. IEEE Transactions on Electronics Packaging Manufacturing, 2002. 25(3): p. 185-192.

[89]. M.A. Meyers, Dynamic Behavior of Materials. 1994, New York: John Wiley & Sons.

[90]. Broek, Elementary Engineering Fracture Mechanics. 1981: Martinus Nijhoff.

[91]. A.G. Evans and J.W. Hutchinson, Effects of Non-Planarity on the Mixed Mode Fracture Resistance of Bimaterial Interfaces. Acta Metallurgica, 1989. 37(3): p. 909-916.

[92]. M.-Y. He and J.W. Hutchinson, Crack Deflection at an Interface between Dissimilar Elastic Materials. International Journal of Solids and Structures, 1989. 25(9): p. 1053-1067.

[93]. Z. Suo and J.W. Hutchinson, Sandwich Test Specimens for Measuring Interface Crack Toughness. Materials Science & Engineering A: Structural Materials: Properties, Microstructure and Processing, 1989. A107(1-2): p. 135-143.

[94]. J. Dundurs, ed. Mathematical Theory of Dislocations. American Society of Mechanical Engineering. 1969: New York. 70–115.

[95]. H.F. Nied, Mechanics of Interface Fracture with Applications in Electronic Packaging. IEEE Transactions on Device and Materials Reliability, 2003. 3(4): p. 129-143.

[96]. R.R. Chromik, D.N. Wang, A. Shugar, L. Limata, M.R. Notis, and R.P. Vinci, Mechanical Properties of Intermetallic Compounds in the Au–Sn System. Journal of Materials Research, 2005. 20(8): p. 2161-2172.

[97]. Z. Suo and J. Hutchinson, Sandwich Test Specimens for Measuring Interface Crack Toughness. Materials Science and Engineering A, 1989: p. 135-143.

[98]. J.R. Rice, Elastic Fracture Mechanics Concepts for Interface Cracks. Journal of Applied Mechanics, 1988. 55: p. 98–103.

[99]. J.W. Hutchinson and Z. Suo, Mixed Mode Cracking in Layered Materials. Advances in applied mechanics, 1992. 29: p. 63-191.

[100]. C. Kanchanomia, Y. Miyashita, Y. Mutoh. Strain-rate effects on low cycle fatigue mechanism of eutectic Sn–Pb solder. International Journal of Fatigue, 2002. 24(9): p. 987-993

[101]. K. Ishii. Journal of Physics Society, Japan, 1959. 14: p. 1315

[102]. P. Oberndorff. Doctoral Thesis, Eindhoven University of Technology, 2001.

[103]. T. T. Mattila, J.K. Kivilahti. Failure Mechanisms of Lead-Free Chip Scale Package Interconnections Under Fast Mechanical Loading. Journal of Electronic Materials, 2005. 34(7): p. 969-976

[104]. J. F. Eckel. The influence of frequency on the repeated bending life of acid lead. Proceedings ASTM, 1951. 51: p. 745–760.

[105]. X.Q. Shi, H.L.J. Pang, W. Zhou, Z.P. Wang. Low cycle fatigue analysis of temperature and frequency effects in eutectic solder alloy. International Journal of Fatigue, 2000. 22(3): p 217-228

[106]. C. Kanchanomai, Y. Miyashita, Y. Mutoh, S. L. Mannan. Influence of frequency on low cycle fatigue behavior of Pb-free solder 96.5Sn-3.5Ag. Materials Science and Engineering A, 2003. 345(1-2): p 90-98

[107]. T. Ferguson and J. Qu. Effect of Moisture on the Interfacial Adhesion of the Underfill/Solder Mask Interface. Journal of Electronic Packaging. 2002. 124 (2): p. 106-110.

[108]. L.L., Mercado, H. Wieser, T. Hauck. Multichip Package Delamination and Die Fracture Analysis. IEEE Transactions on Advanced Packaging. 2003. 26(2): 152-159.

[109]. S.K.W. Seah. Understanding and Testing for Drop Impact Failure, Proceedings of the ASME / Pacific Rim Tech. Conf. on Int. and Pack. Of MEMS, NEMS, and Electronic Systems, v Part B, Advances in Electronic Packaging, 2005. p 1089-1094

[110]. T.Y. Hin, K.S. Beh, K.N. Seetharamu. Development for Dynamic Test Board for FCBGA Solder Joint Reliability Assessment in Shock & Vibration. IEEE Electronics Packaging Technology Conference, 2003. p 256-262.

[111]. D.S. Steinberg. Vibration Analysis for Electronic Equipment. John Wiley & Sons, New York, 1988.

[112]. S. Sidharth, D. B. Barker. Vibration induced fatigue life estimation of corner leads of peripheral leaded components, Journal of Electronic Packaging, 1996. 118(4): p 244-249

[113]. J. Varghese, A. Dasgupta. Test Methodology for Durability Estimation of Surface Mount Interconnects under Drop Testing Conditions, Microelectronics Reliability, 2007. 47(1): p. 93-103

[114]. J. Varghese, A. Dasgupta, A., Drop Testing of Printed Wiring Assemblies, Proceedings of the SEM Annual Conference and Exposition on Experimental and

Applied Mechanics, 2005. p 1591-1595.

[115]. G. E. Deiter. Mechanical Metallurgy, 3rd Edition, McGraw Hill Book Company – Singapore, p 391

[116]. B. Wang, S. Yi. Dynamic Behavior of 63 wt % Sn 37% Pb Eutectic Solder Under High Strain Rates. Journal of Materials Science and Letters, 2002. 21(9): p 697-698

[117]. P. Lall, D. Panchagade, P. Choudhary, J. Suhling, S. Gupte. Failure-envelope approach to modeling shock and vibration survivability of electronic and MEMS packaging. Proceedings of the Electronic Components and Technology Conference, 2005. 1: p 480-490

[118]. J. Varghese, A. Dasgupta, The Role of Aging on Dynamic Failure Envelopes of OSP-Sn37Pb Interconnects in Plastic Ball Grid Array Packag*es*, Accepted for publication in IEEE Transactions on Components Packaging and Technologies, 2007.

[119]. L. Zhu, W. Marcinkiewicz. Drop Impact Reliability Analysis of CSP Packages at Board and Product Level Through Modelling Approaches. Proceedings of the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2004. 2: p 296-303

[120]. Y.R. Desmond, F.X. Chong, L.H. Che, H. J. Xu, J. H. L. Pang, B.S. Xiong, B.K. Lim. Performance Assessment on Board-level Drop Reliability for Chip Scale Packages (Fine-pitch BGA). Proceedings of the Electronic Components and Technology Conference, 2006. p 356-363

[121]. F.X. Chea, J.H.L. Pang. Modeling Board-Level Four-Point Bend Fatigue and

Impact Drop Tests. Proceedings of the Electronic Components and Technology Conference, 2006. p 443-448

[122]. K.C. Ong, V. B. Tan, C. T. Lim, E. H. Wong, X. W. Zhang. Dynamic Materials Testing and Modeling of Solder Interconnects. Proceedings of the IEEE Electronics Components and Technology Conference, 2004. p. 1075- 1079.

[123]. J. Varghese, A. Dasgupta. The Role of Aging on Dynamic Failure Envelopes of OSP-Sn37Pb Interconnects in Plastic Ball Grid Array Packages. Accepted for publication in IEEE Transactions on Components Packaging and Technologies, 2007

[124]. J. Varghese, A. Dasgupta. A Mechanistic Insight Into The Rate-Dependent Failure Envelopes of Solder Interconnects in Surface Mount Assemblies. Submitted for review in IEEE Transactions on Components Packaging and Technologies, 2007.

[125]. M. L. Williams. The Stresses Around A Fault Or Crack In Dissimilar Media. Bulletin of the Seismological Society of America, 1959. 49(2): p. 199-204

[126]. N. Barry, I.P. Jones, T. Hirst, I.M. Fox, J. Robbins. A New Method for the High-Cycle Fatigue Testing of Lead-Free Solder Joints, Proceedings - International Electronics Conference and Exhibition. 2006.

[127]. A.G. Evans, B.J. Dalgleish, M. He, J.W. Hutchinson. On Crack Path Selection And The Interface Fracture Energy In Bimaterial Systems. Acta Metallurgica, 1989. 37(12): p. 3249-3254

[128]. P. L. Liu, J. K. Shang. A Comparative Fatigue Study of Solder/Electroless-Nickel and Solder/Copper Interfaces. Journal of Material Research, 2000. 15(11): p.

2347-2355

[129]. J.W. Jang, J.K. Lin and D.R. Frear. Failure Morphology after the Drop Impact Test of the Ball Grid Array Package with Lead-Free Sn-3.8Ag-0.7Cu on Cu and Ni Under-Bump Metallurgies. Journal of Electronic Materials, 2007. 36(3): p. 207-213

[130]. P. L. Tu, Y. C. Chan, K. C. Hung and J. K. L. Lai. Growth Kinetics of Intermetallic Compounds in Chip Scale Package Solder Joints. Scripta Materialia, 2001. 44(2): p. 317-323

[131]. J-E. Luan, T.Y. Tee, E. Pek, C.T. Lim, Z. Zhong, J. Zhou. Advanced Numerical and Experimental Techniques for Analysis of Dynamic Responses and Solder Joint Reliability During Drop Impact. IEEE Transactions on Components and Packaging Technologies, 2006. 29(3): p. 449- 456

[132]. C.-L. Yeh and Y.-S. Lai. Transient Fracturing of Solder Joints Subjected to Displacement-Controlled Impact Loads. Microelectronics and Reliability, 2006. 46(5-6): p 885-895.

[133]. J. Varghese, A. Dasgupta. Failures in Intermetallic Layers of Solder Interconnects with ENIG Plating. Engineering Fracture Mechanics. Submitted for review, 2007

[134]. C. Au, and O. Büyüköztürk. Peel and Shear Fracture Characterization of Debonding in FRP Plated Concrete Affected by Moisture. Journal of Composites for Construction, 2006. 10(1): p 35-47