ABSTRACT

Title of Document: LOW NOISE PRE-AMPLIFIER/AMPLIFIER CHAIN FOR HIGH CAPACITANCE SENSORS.

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In the past two decades, imaging sensors and detectors have developed tremendously. This technology has found its way into a number of areas, such as space missions, synchrotron light sources, and medical imaging. Nowadays, detectors and custom ICs are routine in high-energy physics applications. Electronic readout circuits have become a key part of every modern detector system. Many sensing circuits in detectors depend upon accumulating charge on a capacitor. The charge uncertainty on the capacitor when it is reset causes a signal error known as reset noise. Therefore, low noise readout circuitry capable of driving high input capacitance is essential for detector systems.

A low noise pre-amplifier/amplifier readout circuitry has been designed and fabricated in 0.13 μm IBM CMOS8RF process technology. The pre-amplifier/ amplifier chain employs correlated double sampling at the input to suppress the *kTC* noise without any additional circuitry. In order to increase the signal-to-noise ratio,

capacitive matching is used at the amplifier input. The experimental results of the signal processing chain employing capacitive matching and correlated double sampling show more than 60 times improvement in the signal-to-noise ratio over the same circuit without these improvements.

In this dissertation a novel auto-zeroing technique is introduced as well. This technique uses a nulling point other than the amplifier's input and output to perform the auto-zeroing operation. The auto-zeroing is performed by taking advantage of emitter degeneration in the input transistor pair of the differential pair. For testing purposes this technique is implemented on a telescopic cascode differential amplifier. The auto-zeroed telescopic cascode differential amplifier has also been designed and fabricated in 0.13 μm IBM CMOS8RF process technology. This auto-zeroing technique reduces the input referred offset noise by an order of magnitude.

LOW NOISE PRE-AMPLIFIER/AMPLIFIER CHAIN FOR HIGH CAPACITANCE SENSORS.

By

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Dedication

To my parents for their unconditional love

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Table of Contents

Dedication ii
Acknowledgements iii
Table of Contents v
List of Tables vii
List of Figures viii
Chapter 1: Introduction 1
Chapter 2: Review of VLSI Read out in Detector Systems 4
2.1 Introduction 4
2.2 Signal Processing Chain in Radiation Detector Systems 4
2.2.1 Pre-amplifier/Amplifier 5
2.2.2 Pulse Shaper 8
Chapter 3: Amplifier Architectures 12
3.1 Telescopic Cascode Differential Amplifier 12
3.2 Folded Cascode Differential Amplifier 15
3.3 Introduction to the concept of Gain Boosting 21
3.3.1 Folded Cascode Gain Boosted Amplifier 24
3.4 Common Mode feedback 29
Chapter 4: Offset 34
4.1 Introduction 34
4.2 DC Offset 35
4.3 Offset Reduction Techniques 39
4.3.1 Auto-zeroing and Correlated Double Sampling 39
4.3.2 Correlated Double Sampling 43
4.3.3 The Chopper Stabilization Technique 43
4.4 Implementation Issues and Challenges 44
4.4.1 Switches and Their Non-ideal Effects 45
4.4.2 The Open Loop Offset Cancellation Technique 49
4.4.3 The Closed-Loop Offset Cancellation Technique 51
4.4.4 Multistage Offset Storage 53
4.4.5 Closed-Loop Offset Compensation Using an Auxiliary Offset Storage 56
4.4.6 Continuous-Time Auto-zeroing Amplifiers 67
4.5 A Novel Auto-zeroing Technique Using Emitter Degeneration 73
4.5.1 Description 74
4.5.2 Simulation Results 76
4.5.3 Experimental Results 91
4.5.3.1 Telescopic Cascode Differential Amplifier 91
4.5.3.2 Telescopic Cascode Amplifier with the Emitter Degeneration Auto-zeroing Technique 98
4.5.3.3 Comparison 106
Chapter 5: Noise Sources in Detector Sensors 111
5.1 Introduction 111
5.2 Noise Sources in Integrated Circuits 111

5.2.1 Thermal Noise 111
5.2.2 Shot Noise 112
5.2.3 Flicker Noise 114
5.2.4 Burst Noise 115
5.2.5 Avalanche Noise 116
5.3 Noise Models of Integrated Circuits 117
5.3.1 Junction Diodes 117
5.3.2 MOS Transistors 118
5.3.3 Bipolar Junction Transistors 119
5.3.4 Resistors 120
5.3.5 Capacitors and Inductors 121
5.4 Noise Analysis in Detector Circuits 121
5.4.1 Noise Contributions 122
5.4.1.1 Detector Leakage Current 122
5.4.1.2 Parallel Resistance 124
5.4.1.3 Series Resistance 125
5.4.1.4 Amplifier Input Noise 125
5.5 Equivalent Noise Charge in the Detector Front End 126
5.6 Effect of Feedback on Noise Performance 128
Chapter 6: Review of Previously Proposed Techniques for Noise Reduction in Sensor Arrays 132
6.1 Introduction 132
6.2 Capacitive Control 132
6.3 Bandwidth Control 140
6.4 Charge Control 145
6.5 Low Noise Pre-amplifier/Amplifier Chain 150
Chapter 7: A Novel Noise Reduction Technique for High Capacitance Sensor Arrays 153
7.1 Introduction 153
7.2 Pre-amplifier/Amplifier Readout Circuitry 155
7.3 Simulation Results 159
7.4 Experiment Results 168
Chapter 8: Conclusion 186
Bibliography 190

List of Tables

TABLE 1: TRANSISTOR PARAMETERS FOR THE DIFFERENTIAL TELESCOPIC CASCODE AMPLIFIER IN FIGURE 47 78
TABLE 2: TRANSISTOR PARAMETERS FOR THE AUTO-ZEROED DIFFERENTIAL TELESCOPIC CASCODE AMPLIFIER IN FIGURE 52 82
TABLE 3: CAPACITIVE CONTROL TECHNIQUE CIRCUIT PARAMETERS [41] 139
TABLE 4: SIMULATION PARAMETERS FOR THE BANDWIDTH CONTROL TECHNIQUE CIRCUIT [41] 144
TABLE 5: COMPONENT PARAMETERS FOR THE CHARGE CONTROL CIRCUIT [41] 149
TABLE 6: AMPLIFIER CIRCUIT PARMETERS 157
TABLE 7: SUMMARY AND COMPARISON FOR THE LOW NOISE PRE-AMPLIFIER/AMPLIFIER CHAIN 188
TABLE 8: AUTO-ZEROING TECHNIQUE SUMMARY 189

List of Figures

FIGURE 1: DETECTOR SIGNAL PROCESSING CHAIN 5
FIGURE 2: AMPLIFIER AND DETECTOR BLOCK DIAGRAM 5
FIGURE 3: CHARGE SENSITIVE AMPLIFIER CONFIGURATION 6
FIGURE 4: INPUT AND OUTPUT WAVEFORMS OF THE PULSE SHAPER [3] 8
FIGURE 5: A SIMPLE PULSE SHAPER USING CR DIFFERENTIATOR AS A HIGH PASS FILTER AND A RC INTEGRATOR AS A LOW PASS FILTER 9
FIGURE 6: PULSE SHAPER OUTPUT VS. NUMBER OF INTEGRATORS [3] 10
FIGURE 7: CORRELATED DOUBLE SAMPLING PULSE SHAPER 11
FIGURE 8: SIMPLE DIFFERENTIAL AMPLIFIER 13
FIGURE 9: TELESCOPIC CASCODE OPERATIONAL AMPLIFIER 13
FIGURE 10: TRANSFORMATION OF A TELESCOPIC CASCODE WITH NMOS INPUT TO A FOLDED CASCODE 15
FIGURE 11: TRANSFORMATION OF A TELESCOPIC CASCODE WITH PMOS INPUT TO A FOLDED CASCODE 15
FIGURE 12: (A) TELESCOPIC CASCODE OPERATIONAL AMPLIFIER (B) FOLDED CASCODE OPERATIONAL AMPLIFIER 17
FIGURE 13: FOLDED CASCODE DIFFERENTIAL AMPLIFIER 17
FIGURE 14: THE EQUIVALENT HALF CIRCUIT FOR THE FOLDED CASCODE DIFFERENTIAL AMPLIFIER 18
FIGURE 15: HALF CIRCUIT OF THE FOLDED CASCODE DIFFERENTIAL AMPLIFIER USED TO CALCULATE THE TRANSCONDUCTANCE 18
FIGURE 16: EQUIVALENT HALF CIRCUIT USED TO CALCULATE THE OVERALL TRANSCONDUCTANCE 19
FIGURE 17: EQUIVALENT HALF CIRCUITS USED TO CALCULATE THE OUTPUT RESISTANCE 20
FIGURE 18: (A) GAIN BOOSTED CASCODE AMPLIFIER (B) SMALL SIGNAL MODEL FOR THE GAIN BOOSTED CASCODE USED TO FIND THE OUTPUT RESISTANCE 21
FIGURE 19: (A) GAIN BOOSTED CASCODE CIRCUIT (B) SMALL SIGNAL EQUIVALENT CIRCUIT TO CALCULATE THE OVERALL TRANS-CONDUCTANCE 22
FIGURE 20: GAIN BOOSTING TECHNIQUE APPLIED TO A FOLDED CASCODE DIFFERENTIAL AMPLIFIER 25
FIGURE 21: SINGLE-ENDED GAIN BOOSTING AMPLIFIERS REPLACED BY DIFFERENTIAL COUNTERPARTS 25
FIGURE 22: FULLY DIFFERENTIAL AMPLIFIER 26
FIGURE 23: PMOS BOOSTER SCHEMATIC 28
FIGURE 24: COMMON MODE FEEDBACK CIRCUIT APPLIED TO A SIMPLE DIFFERENTIAL AMPLIFIER 30
FIGURE 25: COMMON MODE FEEDBACK CIRCUIT REALIZED USING TWO RESISTORS 31
FIGURE 26: COMMON MODE FEEDBACK REALIZED BY TWO NMOS TRANSISTORS 33
FIGURE 27: SIMPLE DIFFERENTIAL AMPLIFIER 36
FIGURE 28: AUTO-ZEROING TECHNIQUE 40
FIGURE 29: INPUT REFERRED OFFSET VS. THE CONTROL VARIABLE (A) LARGE INITIAL OFFSET (B) SMALL INITIAL OFFSET 42
FIGURE 30: THE CHOPPER STABILIZATION TECHNIQUE 43
FIGURE 31: SAMPLE AND HOLD CIRCUIT USED IN AUTO-ZEROING TECHNIQUES 46
FIGURE 32: SAMPLE AND HOLD CIRCUIT WITH EQUAL CAPACITORS ($C_p = C_h$) AND HALF-SIZED DUMMY SWITCHES 47
FIGURE 33: FULLY DIFFERENTIAL STRUCTURE TO CANCEL THE CHARGE INJECTION EFFECTS 48
FIGURE 34: OPEN LOOP OFFSET CANCELLATION TECHNIQUE 49

FIGURE 35: CLOSED LOOP OFFSET CANCELLATION (A) AUTO-ZEROING PHASE (B) AMPLIFICATION PHASE 51
FIGURE 36: MULTISTAGE OFFSET CANCELLATION USING OPEN-LOOP OFFSET REDUTION IN EACH STAGE 53
FIGURE 37: MULTISTAGE OFFSET CANCELLATION USING CLOSED-LOOP OFFSET REDUCTION IN EACH STAGE 53
FIGURE 38: OFFSET REDUCTION USING AN ADDITIONAL AUXILIARY POINT 57
FIGURE 39: A SIMPLE REALIZATION OF A NULLING POINT IN A DIFFERENTIAL AMPLIFIER 61
FIGURE 40: ACTUAL REALIZATION OF A NULLING POINT IN THE DIFFERENTIAL AMPLIFIER 62
FIGURE 41: REALIZING THE INTERMEDIATE NULLING POINT FOR AUTO-ZEROING USING A CURRENT MIRROR 64
FIGURE 42: CURRENT MIRROR SCHEMATIC 64
FIGURE 43: CURRENT MIRROR: LOAD RESISTORS REPLACED WITH TRANSISTOR 65
FIGURE 44: CURRENT MIRROR CURRENT CHANGE VS. THE NULLING VOLTAGE 66
FIGURE 45: CONTINUOUS-TIME AUTO-ZEROING AMPLIFIER 68
FIGURE 46: AUTO-ZEROING TECHNIQUE USING EMITTER DEGENERATED RESISTORS FOR OFFSET CANCELLATION 74
FIGURE 47: DIFFERENTIAL TELESCOPIC CASCODE AMPLIFIER WITHOUT THE AUTO-ZEROING TECHNIQUE 77
FIGURE 48: GAIN VS. FREQUENCY FOR THE TELESCOPIC CASCODE AMPLIFIER IN FIGURE 47 78
FIGURE 49: PHASE VS. FREQUENCY FOR THE TELESCOPIC CASCODE AMPLIFIER IN FIGURE 47 79
FIGURE 50: SIMULATED DIFFERENTIAL DC OUTPUT VOLTAGES OF THE TELESCOPIC CASCODE AMPLIFIER 80
FIGURE 51: SIMULATED OUTPUT OFFSET VOLTAGE FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER 80
FIGURE 52: TELESCOPIC CASCODE AMPLIFIER WITH THE EMITTER DEGENERATION AUTO-ZEROING TECHNIQUE 82
FIGURE 53: GAIN VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER 83
FIGURE 54: PHASE VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER 83
FIGURE 55: SIMULATED OUTPUT OFFSET VOLTAGE AND CLOCK SIGNAL FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER SHOWN IN FIGURE 52 84
FIGURE 56: GAIN VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A CLOSED LOOP GAIN OF 10V/V 85
FIGURE 57: PHASE VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A CLOSED LOOP GAIN OF 10V/V 86
FIGURE 58: SIMULATED OUTPUT OFFSET VOLTAGE FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A FEEDBACK CONFIGURATION OF 10K/100K 86
FIGURE 59: SIMULATED OUTPUT OFFSET VOLTAGE FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A FEEDBACK CONFIGURATION OF 1M/10M 87
FIGURE 60: GAIN VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A CLOSED LOOP GAIN OF 100V/V 88
FIGURE 61: PHASE VS. FREQUENCY FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A CLOSED LOOP GAIN OF 100V/V 88
FIGURE 62: SIMULATED OUTPUT OFFSET VOLTAGE FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A FEEDBACK CONFIGURATION OF 10K/1M 90

FIGURE 63: SIMULATED OUTPUT OFFSET VOLTAGE FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A FEEDBACK CONFIGURATION OF 100K/10M 90
FIGURE 64: THE CHIP LAYOUT FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER SHOWN IN FIGURE 47 92
FIGURE 65: THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER LAYOUT 93
FIGURE 66: TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER CHIP 94
FIGURE 67: TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER SHOWN IN A FEEDBACK CONFIGURATION WITH A CLOSED LOOP GAIN OF 10V/V 95
FIGURE 68: EXPERIMENTAL TRANSIENT INPUT AND OUTPUT WAVEFORMS FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A 10K/100K FEEDBACK RESISTOR CONFIGURATION 95
FIGURE 69: EXPERIMENTAL TRANSIENT INPUT AND OUTPUT WAVEFORMS FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A 1M/10M FEEDBACK RESISTOR CONFIGURATION 96
FIGURE 70: EXPERIMENTAL TRANSIENT INPUT AND OUTPUT WAVEFORMS FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A 100K/10M FEEDBACK RESISTOR CONFIGURATION 97
FIGURE 71: EXPERIMENTAL TRANSIENT INPUT AND OUTPUT WAVEFORMS FOR THE TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A 10K/1M FEEDBACK RESISTOR CONFIGURATION 98
FIGURE 72: THE CHIP LAYOUT FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER SHOWN IN FIGURE 52 99
FIGURE 73: THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER LAYOUT 100
FIGURE 74: THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER CHIP 101
FIGURE 75: EXPERIMENTAL TRANSIENT INPUT AND OUTPUT WAVEFORMS FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER WITH A 10K/100K FEEDBACK RESISTOR CONFIGURATION 102
FIGURE 76: EXPERIMENTAL OUTPUT OFFSET VOLTAGE, OUTPUT VOLTAGES AND THE CONTROL VOLTAGE VS. TIME FOR THE AUTO-ZEROED TELESCOPIC CASCODE DIFFERENTIAL AMPLIFIER USED WITH A 10K/100K FEEDBACK CONFIGURATION 102
FIGURE 77: EXPERIMENTAL OUTPUT OFFSET VOLTAGE, OUTPUT VOLTAGES AND THE CONTROL VOLTAGE VS. TIME FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER USED WITH A 1M/10M FEEDBACK CONFIGURATION 104
FIGURE 78: EXPERIMENTAL OUTPUT OFFSET VOLTAGE, OUTPUT VOLTAGES AND THE CONTROL VOLTAGE VS. TIME FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER USED WITH A 100K/10M FEEDBACK CONFIGURATION 105
FIGURE 79: EXPERIMENTAL OUTPUT OFFSET VOLTAGE, OUTPUT VOLTAGES AND THE CONTROL VOLTAGE VS. TIME FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER USED WITH A 10K/1M FEEDBACK CONFIGURATION 106
FIGURE 80: EXPERIMENTAL OUTPUT OFFSET VOLTAGES FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER AND THE TELESCOPIC CASCODE AMPLIFIER USED WITH A 10K/100K FEEDBACK CONFIGURATION 107
FIGURE 81: EXPERIMENTAL OUTPUT OFFSET VOLTAGES FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER AND THE TELESCOPIC CASCODE AMPLIFIER USED WITH A 1M/10M FEEDBACK CONFIGURATION 108
FIGURE 82: EXPERIMENTAL OUTPUT OFFSET VOLTAGES FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER AND THE TELESCOPIC CASCODE AMPLIFIER USED WITH A 100K/10M FEEDBACK CONFIGURATION 109
FIGURE 83: EXPERIMENTAL OUTPUT OFFSET VOLTAGES FOR THE AUTO-ZEROED TELESCOPIC CASCODE AMPLIFIER AND THE TELESCOPIC CASCODE AMPLIFIER USED WITH A 10K/1M FEEDBACK CONFIGURATION 110
FIGURE 84: THERMAL NOISE REPRESENTATION 112

FIGURE 85: SMALL SIGNAL EQUIVALENT CIRCUIT FOR JUNCTION DIODE..... 113
FIGURE 86: FLICKER NOISE SPECTRUM DENSITY AS A FUNCTION OF FREQUENCY 115
FIGURE 87: BURST NOISE SPECTRAL DENSITY 116
FIGURE 88: NOISE MODEL FOR THE JUNCTION DIODE 117
FIGURE 89: MOSFET SMALL SIGNAL EQUIVALENT CIRCUIT WITH NOISE SOURCES.... 118
FIGURE 90: EQUIVALENT BJT MODEL WITH NOISE 120
FIGURE 91: A TYPICAL DETECTOR FRONT END CIRCUIT 121
FIGURE 92: EQUIVALENT SMALL SIGNAL CIRCUIT FOR DETECTOR NOISE ANALYSIS 122
FIGURE 93: DETECTOR SHOT NOISE MODEL 123
FIGURE 94: NOISE MODEL FOR THE BIAS RESISTOR 124
FIGURE 95: EQUIVALENT NOISE CHARGE VS. SHAPING TIME [2] 127
FIGURE 96: FEEDBACK IN A NOISY CIRCUIT 130
FIGURE 97: (A) SERIES-SHUNT FEEDBACK CIRCUIT (B) SERIES-SHUNT FEEDBACK CIRCUIT WITH NOISE SOURCES (C) EQUIVALENT REPRESENTATION OF (D) WITH TWO NOISE SOURCES..... 131
FIGURE 98: CAPACITIVE CONTROL TECHNIQUE SCHEMATIC 133
FIGURE 99: TIMING WAVEFORMS FOR THE CAPACITIVE CONTROL TECHNIQUE 134
FIGURE 100: ANALOGY- HIGH TO LOW POTENTIAL 135
FIGURE 101: ANALOGY- LOW TO HIGH POTENTIAL 135
FIGURE 102: ANALOGY- NO POTENTIAL DIFFERENCE..... 135
FIGURE 103: ANALOGY FOR THE CAPACITIVE CONTROL TECHNIQUE 137
FIGURE 104: INPUT AND OUTPUT WAVEFORMS FOR THE CAPACITIVE CONTROL TECHNIQUE CIRCUIT [41]..... 138
FIGURE 105: TRANSIENT NOISE WAVEFORMS FOR THE CAPACITIVE CONTROL TECHNIQUE [41]..... 138
FIGURE 106: BANDWIDTH CONTROL TECHNIQUE CIRCUIT SCHEMATIC..... 141
FIGURE 107: TIMING CONTROL TRANSIENT WAVEFORMS [41] 141
FIGURE 108: ANALOGY FOR THE BANDWIDTH CONTROL TECHNIQUE 142
FIGURE 109: INPUT AND OUTPUT WAVEFORMS FOR THE BANDWIDTH CONTROL TECHNIQUE [41]..... 143
FIGURE 110: TRANSIENT NOISE WAVEFORMS FOR THE BANDWIDTH CONTROL TECHNIQUE [41]..... 144
FIGURE 111: CHARGE CONTROL TECHNIQUE CIRCUIT SCHEMATIC..... 145
FIGURE 112: ANALOGY FOR THE CHARGE CONTROL NOISE REDUCTION TECHNIQUE 147
FIGURE 113: INPUT AND OUTPUT TRANSIENT WAVEFORMS FOR THE CHARGE CONTROL TECHNIQUE [41]..... 148
FIGURE 114: TRANSIENT NOISE WAVEFORM FOR THE CHARGE CONTROL NOISE REDUCTION TECHNIQUE [41]..... 148
FIGURE 115: SIMPLIFIED SIGNAL PROCESSING CHAIN SCHEMATIC 150
FIGURE 116: DETAILED SCHEMATIC OF THE PRE-AMPLIFIER/AMPLIFIER SECTION [42] 152
FIGURE 117: PRE-AMPLIFIER/AMPLIFIER CHAIN USED IN A MULTIPLEXED DETECTOR 155
FIGURE 118: PRE-AMPLIFIER/AMPLIFIER CHAIN BLOCK DIAGRAM..... 156
FIGURE 119: FOLDED CASCODE AMPLIFIER SCHEMATIC FOR EACH STAGE 156
FIGURE 120: FREQUENCY RESPONSE OF THE PRE-AMPLIFIER/AMPLIFIER EMPLOYING CORRELATED DOUBLE SAMPLING WITHOUT CAPACITIVE MATCHING 161
FIGURE 121: (A) SIMULATED INPUT AND (B) OUTPUT TRANSIENT WAVEFORMS OF THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY EMPLOYING CORRELATED DOUBLE SAMPLING WITHOUT CAPACITIVE MATCHING 162
FIGURE 122: SIMULATED EQUIVALENT OUTPUT NOISE OF THE PRE-AMPLIFIER/AMPLIFIER EMPLOYING CORRELATED DOUBLE SAMPLING WITHOUT CAPACITIVE MATCHING 163
FIGURE 123: FREQUENCY RESPONSE OF THE PRE-AMPLIFIER/AMPLIFIER USING CAPACITIVE MATCHING WITHOUT CORRELATED DOUBLE SAMPLING 163

FIGURE 124: SIMULATED EQUIVALENT OUTPUT NOISE OF THE PRE-AMPLIFIER/AMPLIFIER EMPLOYING CAPACITIVE MATCHING WITHOUT CORRELATED DOUBLE SAMPLING 164
FIGURE 125: FREQUENCY RESPONSE OF THE PRE-AMPLIFIER/AMPLIFIER USING CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING 165
FIGURE 126: (A) SIMULATED INPUT AND (B) OUTPUT TRANSIENT WAVEFORMS OF THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY USING CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING 166
FIGURE 127: SIMULATED EQUIVALENT OUTPUT NOISE OF THE PRE-AMPLIFIER/AMPLIFIER USING CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING 167
FIGURE 128: THE CHIP LAYOUT FOR THE LOW NOISE PRE-AMPLIFIER/AMPLIFIER CHAIN SHOWN IN FIGURE 118 168
FIGURE 129: THE PRE-AMPLIFIER/AMPLIFIER LAYOUT FOR THE LOW NOISE SIGNAL PROCESSING CHAIN SHOWN IN FIGURE 118 169
FIGURE 130: ENHANCED VIEW OF THE LOW NOISE AMPLIFIER 169
FIGURE 131: LOW NOISE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY CHIP 170
FIGURE 132: THE PRE-AMPLIFIER STAGE TEST SETUP 171
FIGURE 133: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER STAGE WITH A FEEDBACK RESISTOR COMBINATION OF 10K/100K 172
FIGURE 134: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER STAGE WITH A FEEDBACK RESISTOR COMBINATION OF 10K/100K AT THE 3DB BANDWIDTH FREQUENCY OF 10MHZ 172
FIGURE 135: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER STAGE WITH A FEEDBACK RESISTOR COMBINATION OF 10K/1M 173
FIGURE 136: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER STAGE WITH A FEEDBACK RESISTOR COMBINATION OF 10K/1M AT THE 3DB BANDWIDTH FREQUENCY OF 600KHZ 174
FIGURE 137: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER STAGE WITH A FEEDBACK RESISTOR COMBINATION OF 10K/1M AT 10MHZ 174
FIGURE 138: TEST SETUP FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITHOUT CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING 176
FIGURE 139: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITH A CLOSED LOOP GAIN OF 100V/V 176
FIGURE 140: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITH A CLOSED LOOP GAIN OF 100V/V 177
FIGURE 141: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITHOUT CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING WITH A CLOSED LOOP GAIN OF 100V/V 178
FIGURE 142: FREQUENCY SPECTRUM FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITHOUT CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING WITH A CLOSED LOOP GAIN OF 100V/V 179
FIGURE 143: TEST SETUP FOR THE PRE-AMPLIFIER/AMPLIFIER CHAIN EMPLOYING CORRELATED DOUBLE SAMPLING 180
FIGURE 144: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY WITH A CLOSED LOOP GAIN OF 100V/V 180
FIGURE 145: FREQUENCY SPECTRUM FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY EMPLOYING CORRELATED DOUBLE SAMPLING WITH A CLOSED LOOP GAIN OF 100V/V 181
FIGURE 146: TEST SETUP FOR THE PRE-AMPLIFIER/AMPLIFIER CHAIN EMPLOYING CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING 183

FIGURE 147: EXPERIMENTAL INPUT AND OUTPUT TRANSIENT RESPONSE FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY EMPLOYING CAPACITIVE MATCHING AND CORRELATED DOUBLE SAMPLING WITH A CLOSED LOOP GAIN OF 100V/V 183
FIGURE 148: FREQUENCY SPECTRUM FOR THE PRE-AMPLIFIER/AMPLIFIER READOUT CIRCUITRY EMPLOYING CORRELATED DOUBLE SAMPLING AND CAPACITIVE MATCHING WITH A CLOSED LOOP GAIN OF 100V/V 184

Chapter 1: Introduction

In the past two decades, imaging sensors and detectors have developed tremendously. This technology has found its way into a number of areas, such as space missions, synchrotron light sources, and medical imaging. Nowadays, detectors and custom ICs are routine in high-energy physics applications. Electronic readout circuits are a key part of every modern detector system. Although the readout electronics for different experiments may be different, the same basic principles of optimization of signal-to-noise ratio apply to all.

NASA is one of the agencies integrating new sensor technologies for earth resource management surveillance and astronomy. Unique materials used in these new sensors require innovative pre-amplifier/amplifier readout circuitry chains, in order, to fully exploit the potential of these devices. In particular, most detectors exhibit exceptional high output impedance. As a result, standard voltage amplification techniques become difficult, as voltage divider effects “de-magnify” the signal. Additional problems occur when the detectors present large capacitances to the pre-amplifier inputs. This gives rise to charge division which further lowers usable signal. Also, the generated capacitances in conjunction with the resistance are responsible for introducing reset noise in detector systems. So the means to provide low noise readout circuitry which can amplify the signal is essential for detector systems.

Many sensing circuits in detectors, such as CdZnTe detectors used by NASA for gamma ray detection, depend upon accumulating charge on a capacitor. The charge uncertainty on the capacitor when it is reset to a reference voltage causes noise, reset noise, as a result of shot and thermal processes. Reset noise is enhanced by the sensing capacitor. Therefore, low noise readout circuitry capable of driving a high input capacitance is essential for detector systems. The main goal of this dissertation is to provide a flexible signal processing chain for high capacitance sensors. This innovative signal processing chain is aimed at increasing the signal-to-noise ratio in pixel detectors and sensors. The resulting system can be used in wide variety of detectors with a range of applications such as random access pixel detectors, fully depleted CCDs, hybrid detector systems, and superconducting detector arrays.

In this dissertation, a novel auto-zeroing technique for amplifiers is proposed as well. This novel technique uses a nulling point other than the amplifier's input and output to perform the auto-zeroing operation. The auto-zeroing is performed by taking advantage of emitter degeneration in the input transistor pair of the differential pair to cancel the offset at the output of the amplifier. This technique reduces the input referred offset voltage of the amplifiers by approximately an order of magnitude.

The unique contributions of this dissertation are as follows:

- Developed a low noise pre-amplifier/amplifier chain employing correlated double sampling and capacitive matching
- Implemented correlated double sampling absent of additional circuitry,

using a reset switch

- Designed a readout circuit which includes signal processing at the point of signal reception
- Invented a novel auto-zeroing technique by taking advantage of the emitter degeneration resistors to reduce the input referred offset by an order of magnitude

This dissertation is organized as follows. Chapter 2 reviews the VLSI readout circuitry used in detector systems. Chapter 3 discusses different amplifier architectures and the advantages and disadvantages for each one. Chapter 4 reviews output offset in amplifiers and the techniques used to reduce the input referred offset voltage. This chapter introduces the novel auto-zeroing technique and discusses the test results. Chapter 5 investigates the noise sources which contribute to the noise in sensors. Chapter 6 reviews the previously proposed techniques for noise reduction in sensor arrays. Finally Chapter 7 presents in detail, the novel noise reduction technique for high output capacitance sensor arrays. It discusses the results achieved using the proposed low noise pre-amplifier/amplifier chain. Chapter 8 concludes this dissertation and gives a brief summary of the novel techniques used for auto-zeroing and noise reduction in high output capacitance sensors.

Chapter 2: Review of VLSI Read out in Detector Systems

2.1 Introduction

VLSI readout circuitry is a key component in all detector systems [1], [2]. It usually consists of a pre-amplifier/amplifier, pulse shaping section, and detect/hold circuitry. This chapter will mainly focus on the pre-amplifier/amplifier section while providing a brief overview of the pulse shaping. Although the experiments and their associated readout circuitry might have different forms, the basic fundamentals of the readout circuitry are the same.

2.2 Signal Processing Chain in Radiation Detector Systems

In order to describe the detector signal processing chain, a scintillation detector is used as an example. Figure 1 shows a scintillation detector block diagram. Radiation primarily consisting of Gamma rays, in this example, is absorbed by a scintillating crystal which produces light photons proportional to the absorbed energy. The photocathode absorbs the photons and releases electrons which correspond to the number of photons detected. At this point, the energy absorbed by the scintillation detector is converted into an electrical signal whose charge is proportional to the energy. The pre-amplifier/amplifier increases this charge by a constant factor. The signal is then passed through a pulse shaper which feeds the analog-to-digital converter (ADC). The ADC converts the signal into a digital signal which is used for

digital processing and storage. In the following sections, a brief review of each of the components used in the signal processing chain will be provided.

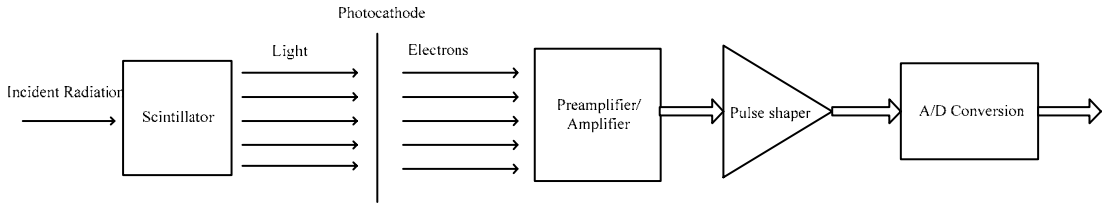


Figure 1: Detector Signal Processing Chain

2.2.1 Pre-amplifier/Amplifier

One of the most important building blocks in the readout circuits for radiation detectors is the pre-amplifier/amplifier block. Figure 2 shows an amplifier block connected to a detector. The detector has a capacitor, C_d, while the amplifier has an input capacitance and resistance, C_i and R_i respectively.

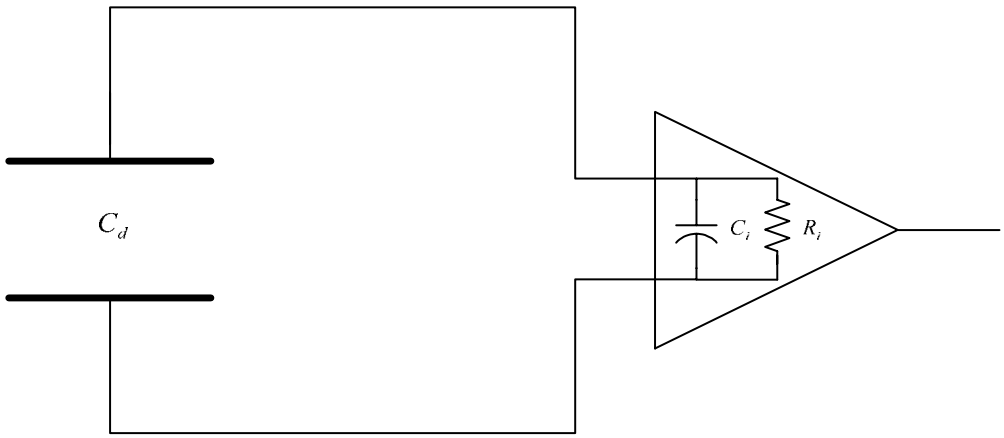


Figure 2: Amplifier and Detector Block Diagram

The sensor signal is modeled as a short current pulse. The amplifier detects the sensor signal and integrates it to get the charge signal. If the amplifier has a small

input resistance, R_i, then the time constant, $\tau = R_i\left(C_d + C_i\right)$, for discharging the sensor capacitor is small. As a result, the amplifier will sense the current signal. On the other hand if the amplifier input resistance is large, the input time constant is large compared to the duration of the current pulse. Therefore, the amplifier will sense the voltage stored on the detector capacitance.

Figure 3 shows a charge sensitive amplifier with a capacitive feedback which performs integration. The amplifier has a gain of A and infinite input impedance. The voltage difference across the feedback capacitor is $v_f = \left(A+1\right)v_i$, where v_i is the input signal. The charge deposited on the feedback capacitance becomes $Q_f = C_f v_f = C_f\left(A+1\right)v_i$. Since no current flows into the amplifier input, all of the signal current must charge up the feedback capacitor so $Q_i = Q_f$, and the amplifier dynamic input capacitance is given by equation (2.1).

$$C_i = \frac{Q_i}{v_i} = C_f\left(A+1\right) \qquad (2.1)$$

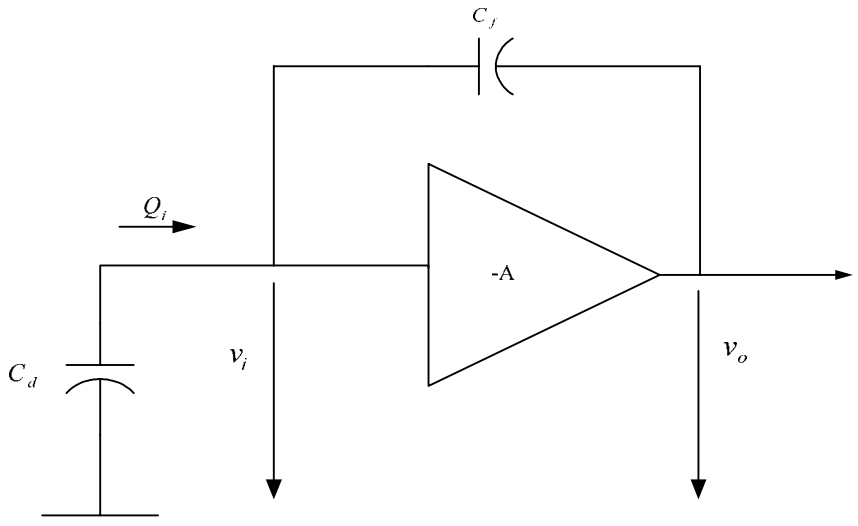


Figure 3: Charge Sensitive Amplifier Configuration

The output voltage per unit input charge can be represented by equation (2.2) in which it is assumed $A \gg 1$.

$$A_Q = \frac{dv_o}{dQ_i} = \frac{Av_i}{C_i v_i} = \frac{A}{C_i} = \frac{A}{A+1}.\frac{1}{C_f} \approx \frac{1}{C_f} \qquad (2.2)$$

Note that the gain declines inversely with the size of the feedback capacitor. The gain is determined by the feedback capacitor which is well defined. In this discussion, the amplifiers are assumed to be infinitely fast. This is not always the case, such as in charge sensitive amplifiers. Charge sensitive amplifiers usually respond more slowly than the time duration of the sensor current signal. However, this does not present a problem since the signal current is first integrated on the sensor capacitor. Then as the amplifier responds, the charge is transferred to the amplifier. The important factor is the amplifier time response. From basic feedback theory, the input impedance of the feedback amplifier is as follows $Z_i = \frac{Z_f}{A+1} \approx \frac{Z_f}{A}$ for $A \gg 1$. At low frequencies, the gain is constant causing the input impedance to be the same as the feedback impedance but reduced by $1/A$. At high frequencies beyond the amplifiers 3dB bandwidth, f_{3dB} , the gain drops linearly with an additional 90 degrees phase shift. Therefore, the following relationship describes the gain of the amplifier: $A = -j\frac{\omega_o}{\omega}$ in which ω_o is the unity gain bandwidth of the amplifier. So the input impedance of the charge sensitive feedback amplifier is represented by equation (2.3).

$$Z_i = \frac{1}{j\omega C_f}.\frac{1}{-j\frac{\omega_o}{\omega}} = \frac{1}{\omega_o C_f} \qquad (2.3)$$

At frequencies above the 3dB bandwidth of the amplifier $\left(f > f_{3dB}\right)$, the input impedance is resistive. Usually, radiation detector frequencies are above the 3dB bandwidth of the amplifier. This results in resistive input impedance. The sensor capacitance is discharged with the time constant which now can be expressed as $\tau = R_i C_d = \frac{1}{\omega C_f} C_d$. The rise time of the charge sensitive amplifier increases with the detector capacitance. Even though the amplifier response time can be longer than the sensor current pulse, it is always required to be faster than the peaking time of the pulse shaper.

2.2.2 Pulse Shaper

The pulse shaper is used to achieve two seemingly conflicting goals. The first goal is to increase the signal-to-noise ratio by restricting the bandwidth. A large bandwidth will increase the noise without increasing the signal. The pulse shaper takes a narrow pulse and turns it into a broader pulse with a gradually rounded peak. Figure 4 shows the input and output waveforms of a pulse shaper.

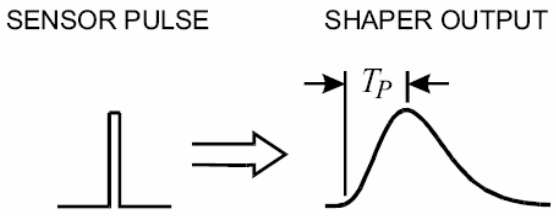


Figure 4: Input and Output Waveforms of the Pulse Shaper [3]

The pulse shaper transforms a short pulse into a longer pulse with a rounded peak. The pulse shaping is also necessary for the ADC. The input pulse to the ADC cannot be too short, and it should have a gradually rounded peak since the ADC takes

a finite time to acquire the signal. Occasionally the pulse shaper is integrated into the ADC.

The second goal is to limit the pulse width, in order, to measure consecutive signal pulses without pileup or overlap. A tradeoff exists due to the fact that reducing the signal pulse width will increase the signal rate but at the expense of higher noise. It is necessary to find balance between these conflicting goals. Optimum shaping depends on the application. Sometimes, the primary consideration is to reduce noise whereas other times a high signal rate becomes the more important design aspect.

A very simple implementation of the pulse shaper is shown in figure 5. This design consists of a high pass filter (differentiator) followed by a low pass filter (integrator). The high pass filter sets the duration of the pulse by introducing a decay time constant of τ_d, while the low pass filter increases the rise time to reduce the noise bandwidth. The key design parameters in this simple pulse shaper implementation are low frequency bound, high frequency bound and signal attenuation.

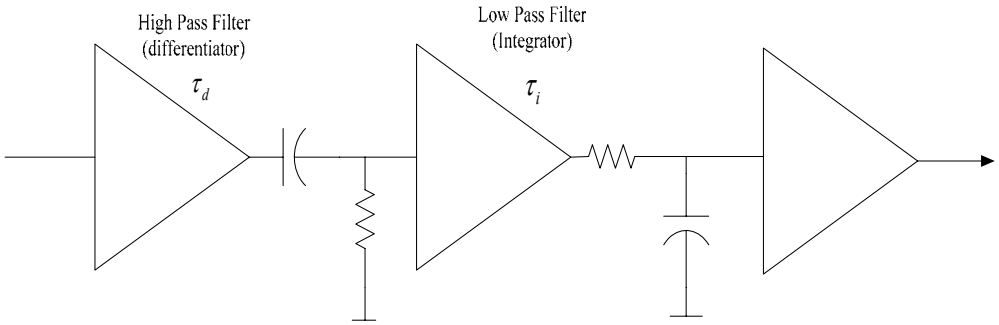


Figure 5: A Simple Pulse Shaper Using CR Differentiator as a High Pass Filter and a RC Integrator as a Low Pass Filter

After the output waveform of a simple CR-RC shaper peaks, it returns to baseline very slowly. If the pulse is made more symmetric, higher signal rates for the same peak time can be achieved. A simple way to do this is by increasing the number of integrators causing the integration time to become smaller than the differentiation time with the purpose of keeping the same peaking time. This is illustrated in figure 6. Peaking time is a very important design parameter since it affects the noise bandwidth, and it should also accommodate the sensor response time.

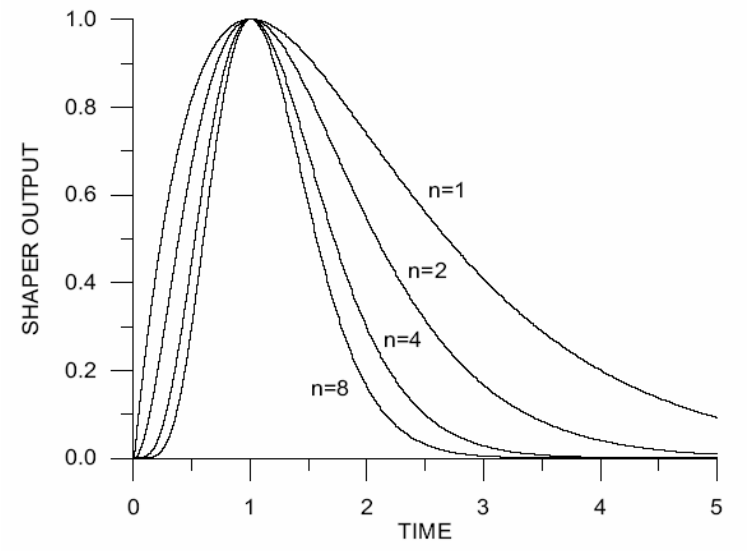


Figure 6: Pulse Shaper Output vs. Number of Integrators [3]

Another type of pulse shaper which is used widely in integrated circuits is the correlated double sampler. This circuit is shown in figure 7. Signals are superimposed on slowly fluctuating baseline noise. To remove the baseline fluctuations, the baseline is sampled before signal. Then, the signal plus baseline is sampled. These two samples are subtracted from each other to give the signal. The pre-filter is necessary to limit the noise bandwidth of the system. Filtering after the

sampler is ineffective since noise fluctuations faster than the sample time will not be removed.

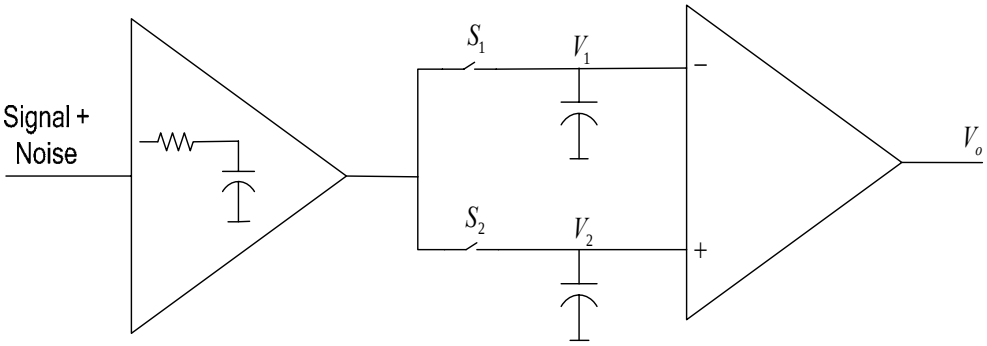


Figure 7: Correlated Double Sampling Pulse Shaper

Chapter 3: Amplifier Architectures

Operational amplifiers are one of the most important building blocks of many different circuits and systems. Different amplifiers are used in a wide range of applications for different purposes such as high speed amplification, filtering, or simply providing a DC bias. This chapter briefly reviews different amplifier architectures such as telescopic cascode differential amplifier, folded cascode differential amplifier and the gain boosted folded cascode amplifier. Emphasis will be on folded cascode and telescopic cascode amplifiers which are used later in this dissertation.

3.1 Telescopic Cascode Differential Amplifier

Telescopic cascode structures are used to increase the gain by stacking transistors [4]-[6]. Consider the simple differential amplifier shown in figure 8. The gain of this circuit is equal to $g_{m1}\left(r_{o1}\|r_{o3}\right)$, which is the transconductance of the input transistor times the output resistance of the circuit. The gain of this circuit is relatively low and may not be enough for many applications. To increase the gain the differential cascode topology can be used. Cascoding increases the gain by increasing the output resistance. One way to increase the gain for the simple differential amplifier shown in figure 8 is to increase the output impedance of both NMOS and PMOS devices. This is done by cascoding two NMOS and two PMOS transistors as shown in figure 9. This circuit is called the telescopic cascode

differential amplifier [7] and has a gain equal to $g_{m1}\left[\left(g_{m3}r_{o3}r_{o1}\right)\left\|\left(g_{m5}r_{o5}r_{o8}\right)\right.\right]$, which is the transconductance of the input transistor multiplied by the output impedance of the NMOS cascode in parallel with the output impedance of the PMOS cascode.

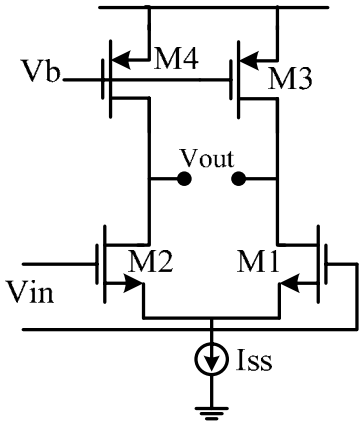


Figure 8: Simple Differential Amplifier

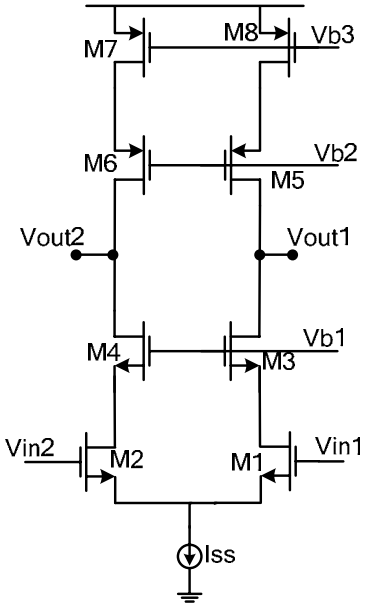


Figure 9: Telescopic Cascode Operational Amplifier

This circuit is a good amplifier, exhibiting a moderate gain. The only drawback of this circuit is its limited output swing when it is in the feedback loop. In some applications such as analog to digital converters the output and input are shorted

together during some portion of the operation and the amplifier is in a unity gain feedback. When a unity gain feedback is applied to the differential cascode amplifier shown in figure 9, M_1 and M_3 must be in saturation region in order for the amplifier to function correctly. As we know for an NMOS transistor to be in saturation, $V_{ds} \geq V_{gs} - V_{th}$ or equivalently $V_{gd} \leq V_{th}$. Thus equations (3.1) and (3.2) hold for M_1 and M_3.

$$V_{in1} \leq V_{b1} - V_{gs3} + V_{th1} \qquad (3.1)$$

$$V_{out1} \geq V_{b1} - V_{th3} \qquad (3.2)$$

The output and input are shorted together when we have unity gain feedback so $V_{out1} = V_{in1}$. From the above relations the following relationship is derived.

$$V_{b1} - V_{th3} \leq V_{out1} \leq V_{b1} - V_{gs3} + V_{th1} \qquad (3.3)$$

As can be seen from equation (3.3) the voltage range is equal to $V_{\max} - V_{\min} = V_{th1} - \left(V_{gs3} - V_{th3}\right)$. This voltage range is less than V_{th1}. This means that if the output swing is more than this voltage range then M_1 and M_3 will enter the triode region. This is not desired so this circuit is not a good candidate for applications where a large output swing is needed. Even if we have a closed loop gain of larger than one, output swing is still limited.

3.2 Folded Cascode Differential Amplifier

As seen in the previous section telescopic cascode amplifiers have a limited swing specially when used in a unity gain feedback. In order to solve the headroom drawback of the telescopic cascode op amps, folded cascode op amps are used [7]. Figures 10 and 11 show how a telescopic cascode amplifier is transformed into a folded cascode amplifier. The upper PMOS cascode is modeled by a current source as shown in figure 10.

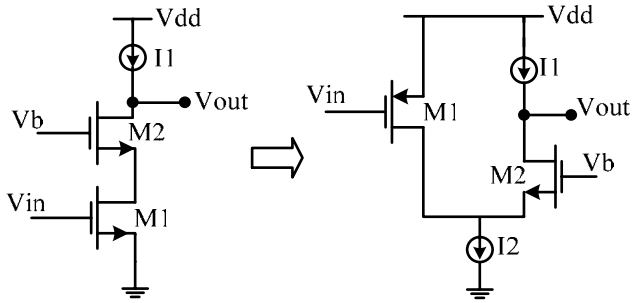


Figure 10: Transformation of a Telescopic Cascode with NMOS Input to a Folded Cascode

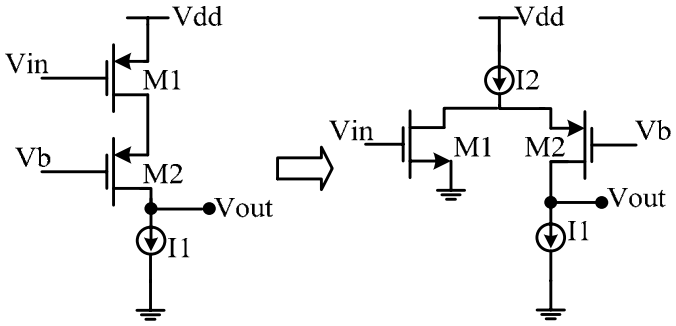


Figure 11: Transformation of a Telescopic Cascode with PMOS Input to a Folded Cascode

As mentioned in the previous section, the drawback of the telescopic cascode circuit is that its swing with unity gain feedback is limited. If the output node swings up more than the threshold voltage of the input transistor, the gate voltage of the input transistor will increase by V_{th} with respect to its drain voltage which is fixed and it

will enter triode region. If the input device is replaced by the opposite type it will still change the input voltage signal to current and inject it to the source of the output device. This time the difference is if output swing is larger than V_{th}, the input device will not enter triode region.

The folding idea can be applied to the telescopic cascode differential pair as can be seen in figure 12. There are no problems in applying a unity gain feedback to the folded cacode differential amplifier. The reason is that in the telescopic cascode in figure 12(a), for M_1 to be in saturation the input common mode level cannot exceed $V_{b1} - V_{gs3} + V_{th1}$. We can not short the input to output as it would cause the common mode level to exceed $V_{b1} - V_{gs3} + V_{th1}$. But as can be seen in the folded cascode differential amplifier in figure 12(b), for M_1 to be in saturation the input CM level cannot be less than $V_{b1} - V_{gs3} + \left|V_{thp}\right|$. Therefore the folded cascode differential amplifier can be designed to allow shorting the input and output together. The differential folded cascode differential amplifier is shown in figure 13.

In order to find the gain of the folded cascode amplifier, R_{out} and G_m, the amplifier's overall output resistance and transconductance, are calculated first. For this purpose consider the half circuit of the folded cascode differential amplifier in figure 13 as shown in figure 14.

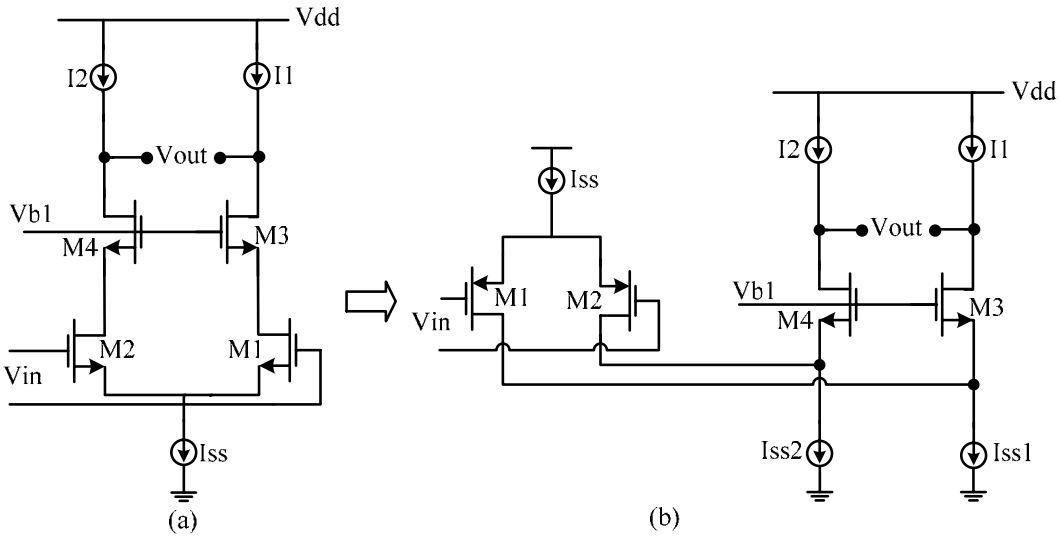


Figure 12: (a) Telescopic Cascode Operational Amplifier (b) Folded Cascode Operational Amplifier

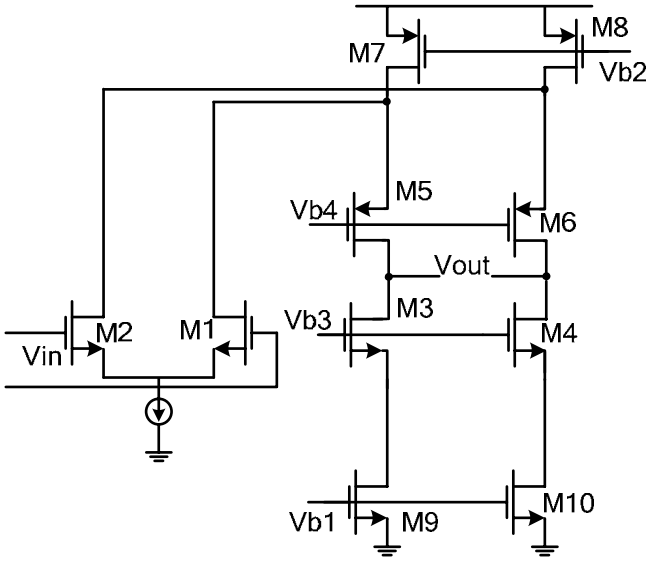


Figure 13: Folded Cascode Differential Amplifier

In order to find the overall transconductance, G_m for the folded cascode differential amplifier, consider the circuit shown in figure 15 in which the output is shorted to ground. As can be seen M_3, M_9 are shorted to ground, so the equivalent circuit is as shown in figure 16(a).

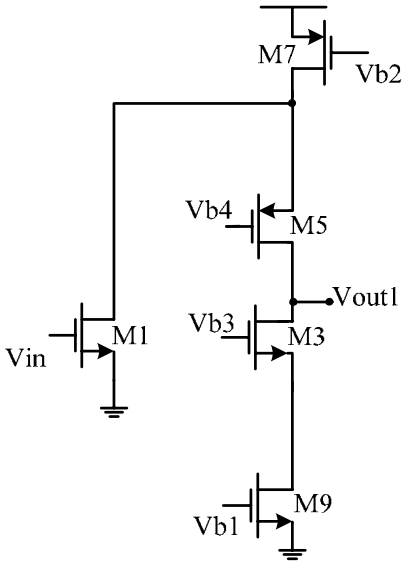


Figure 14: The Equivalent Half Circuit for the Folded Cascode Differential Amplifier

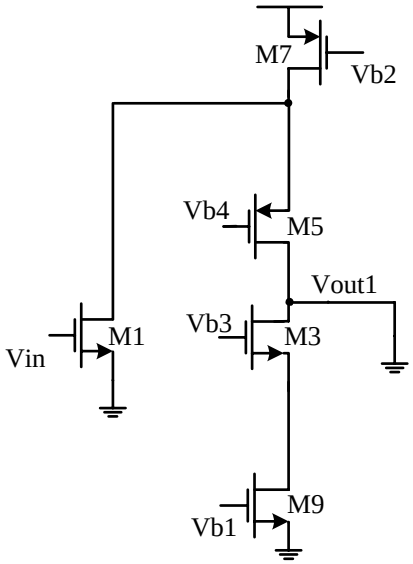


Figure 15: Half Circuit of the Folded Cascode Differential Amplifier used to Calculate the Transconductance

The resistance seen looking up at node X is $r_{o7} \| r_{o1}$ as shown in figure 16(b).

The resistance seen looking down at node X is $\frac{1}{g_{m5}} \| r_{o5}$ which is approximately $\frac{1}{g_{m5}}$.

The current entering node X through the drain of M_1 is $g_{m1} V_{in}$. This current is split

between the two resistances seen looking up and down at node X. Since the resistance seen at this node looking down, $\frac{1}{g_{m5}}$ is a lot smaller than the resistance seen at this node looking up, $r_{o7} \| r_{o1}$, almost all the current entering this node, enters M_5. So the output current I_{out} is approximately equal to $g_{m1}V_{in}$. This tells us that the overall trans-conductance of the circuit, G_m is equal to g_{m1}, which is the transconductance of M_1.

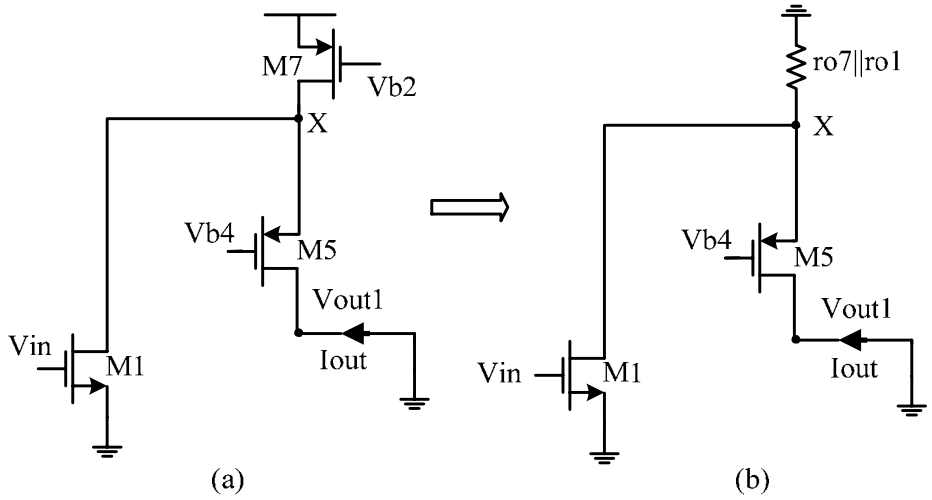


Figure 16: Equivalent Half Circuit used to Calculate the Overall Transconductance

Now in order to calculate the output resistance R_{out} seen at the output node, consider the circuit shown in figure 17(a) in which the input is shorted. The lower NMOS cascode consisting of transistors M_3 and M_9 is replaced by its equivalent resistance, $R_{ON} = g_{m3}r_{o3}r_{o9}$ as shown in figure 17(b). The resistance seen at node X looking up is $r_{o7} \| r_{o1}$ as seen in figure 17(b).

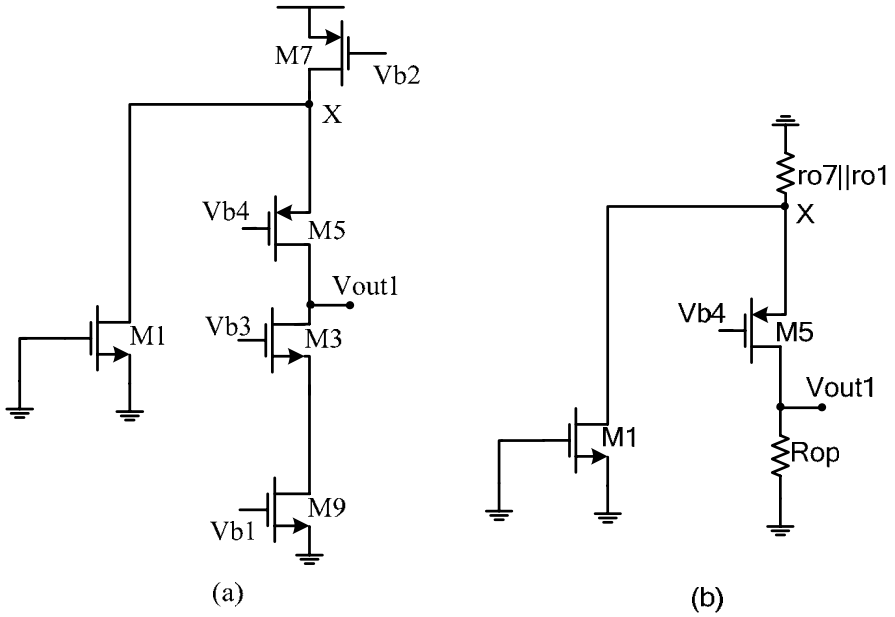


Figure 17: Equivalent Half Circuits used to Calculate the Output Resistance

The output resistance R_{out} is given by equation (3.4) as follows:

$$R_{out} = R_{OP} \left\| \left(g_{m5} r_{o5} \left(r_{o1} \| r_{o7} \right) \right) = g_{m3} r_{o3} r_{o9} \right\| \left(g_{m5} r_{o5} \left(r_{o1} \| r_{o7} \right) \right) \qquad (3.4)$$

Now that both the transconductance and output resistance of the folded cascode differential amplifier are known, the midband gain of the circuit is derived in equations (3.5) and (3.6).

$$A_v = G_m R_{out} \qquad (3.5)$$

$$A_v = g_{m1} \left(g_{m3} r_{o3} r_{o9} \left\| \left(g_{m5} r_{o5} \left(r_{o1} \| r_{o7} \right) \right) \right. \right) \qquad (3.6)$$

3.3 Introduction to the concept of Gain Boosting

In section 3.1, cascoding was discussed as a way to increase the output resistance and hence increase the gain of the operational amplifier. In order to be comprehensive the gain boosting technique is briefly discussed in this section [8]-[12]. We start by calculating the output impedance of the gain boosted cascode circuit.

Figure 18(a) shows a gain boosted NMOS cascode in which the lower transistor is replaced by its equivalent output resistance for simplicity.

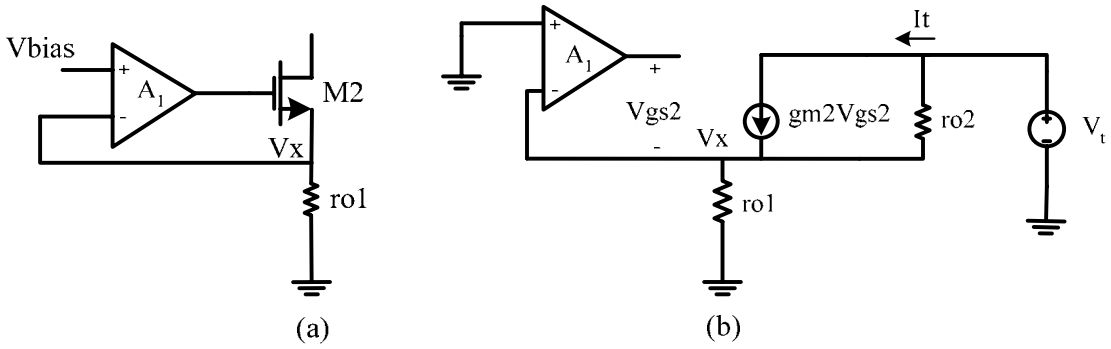


Figure 18: (a) Gain Boosted Cascode Amplifier (b) Small Signal Model for the Gain Boosted Cascode used to Find the Output Resistance

From the small signal model shown in figure 18(b), it can be verified that R_{out}, the output resistance after applying the feedback is approximately $A_1 g_{m2} r_{o1} r_{o2}$. By analyzing the small signal model, we have the following:

$$I_t = g_{m_2} V_{gs_2} + \frac{(V_t - V_x)}{r_{o2}}$$

$$V_{gs_2} = -(A_1 + 1) V_x$$

$$V_x = I_t r_{o1}$$

From these equations the output resistance R_{out} is given in equation (3.7) and derived as follows:

$$V_t = I_t r_{o2}\left(1 + g_{m_2} r_{o1}\left(A+1\right) + \frac{r_{o1}}{r_{o2}}\right)$$

$$\frac{V_t}{I_t} = r_{o1} + r_{o2} + g_{m_2} r_{o1} r_{o2}\left(A+1\right) \qquad (3.7)$$

Since $A_1 \gg 1$ and r_{o1} , $r_{o2} \ll g_{m_2} r_{o1} r_{o2} A_1$, equation (3.7) is simplified to equation (3.8).

$$\mathrm{R_{out}} = \frac{V_t}{I_t} = \mathrm{A_1} g_{m2} r_{o1} r_{o2} \qquad (3.8)$$

In other words, the output resistance of the cascode after connecting the booster amplifier is A_1 times that of the cascode without the booster. So adding the booster increases the output resistance of the cascode and multiplies it by the gain of the booster.

At this point the transconductance for the simple gain boosted cascode shown in figure 18 is derived. The circuit and the small signal equivalent model for it are shown in figure 19.

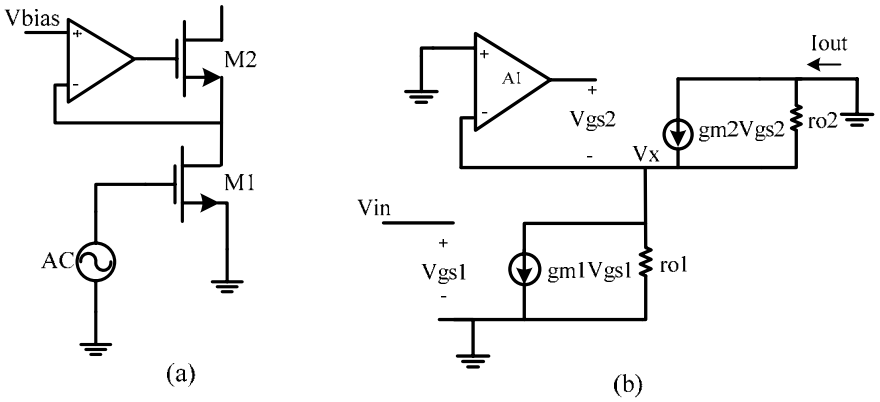


Figure 19: (a) Gain Boosted Cascode Circuit (b) Small Signal Equivalent Circuit to Calculate the Overall Trans-conductance

The transconductance is derived as follows:

$$I_{out} = g_{m1}V_{in} + \frac{V_X}{r_{o1}} \Rightarrow V_X = r_{o1}\left(I_{out} - g_{m1}V_{in}\right)$$

$$I_{out} = g_{m2}V_{gs2} - \frac{V_X}{r_{o2}}$$

$$V_{gs2} = -A_1V_X - V_X = -\left(A_1 + 1\right)V_X$$

$$I_{out} = -g_{m2}\left(A_1 + 1\right)V_X - \frac{V_X}{r_{o2}}$$

$$I_{out} = \left(-g_{m2}\left(A_1 + 1\right) - \frac{1}{r_{o2}}\right)V_X = \left(-g_{m2}\left(A_1 + 1\right) - \frac{1}{r_{o2}}\right)r_{o1}\left(I_{out} - g_{m1}V_{in}\right)$$

$$I_{out}\left(\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1} + 1\right) = V_{in}g_{m1}\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_{m1}\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1}}{\left(\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1} + 1\right)} = \frac{g_{m1}}{\left(\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1} + 1\right)\Big/\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1}} \quad (3.9)$$

Equation (3.9) is simplified as follows and the transconductance G_m is given by equation (3.10).

$$G_m = \frac{g_{m1}}{1 + \frac{1}{\left(g_{m2}\left(A_1 + 1\right) + \frac{1}{r_{o2}}\right)r_{o1}}} \approx g_{m1} \quad (3.10)$$

It can be seen from these calculations that the gain boosting technique increases the output resistance by multiplying it by the booster gain A_1 but it does not change the transconductance of the circuit appreciably.

3.3.1 Folded Cascode Gain Boosted Amplifier

The gain boosting technique can be incorporated in both differential telescopic and folded cascode circuits to get a high gain from a single stage amplifier [13]. Although this technique is not used in this dissertation, it will be briefly discussed for the sake of completeness. As discussed in section 3.1, by cascoding transistors we can get a higher resistance. There is always a limit to the number of the stages that can be cascoded since it will limit the output swing.

In order to get a higher gain from a one-stage differential folded cascode amplifier, the gain boosting technique can be applied to the amplifier as shown in figure 20. The gain boosting technique is applied to the upper PMOS cascode and the lower NMOS cascode the same way it was applied to the cascode in figure 19(a). Since the signals at the inputs of the two upper and lower gain boosting amplifiers are differential, the upper single ended output amplifiers with the DC gain of A_1 can be replaced by one differential output amplifier with a DC gain of B. The same can be applied to the two lower single ended output gain boosting amplifiers with the DC gain of A_2. These two single ended amplifiers can be replaced by one differential output amplifier with a DC gain of A as shown in figure 21.

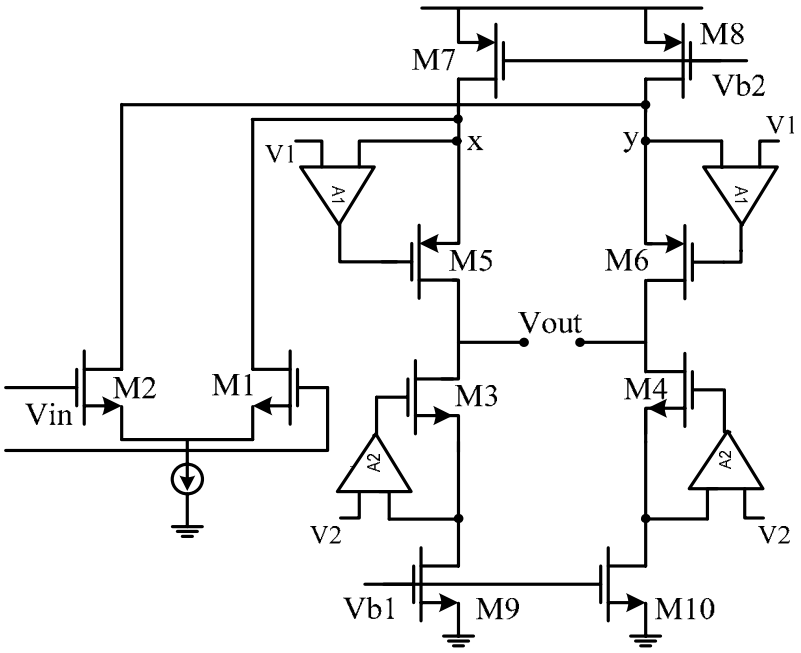


Figure 20: Gain Boosting Technique Applied to a Folded Cascode Differential Amplifier

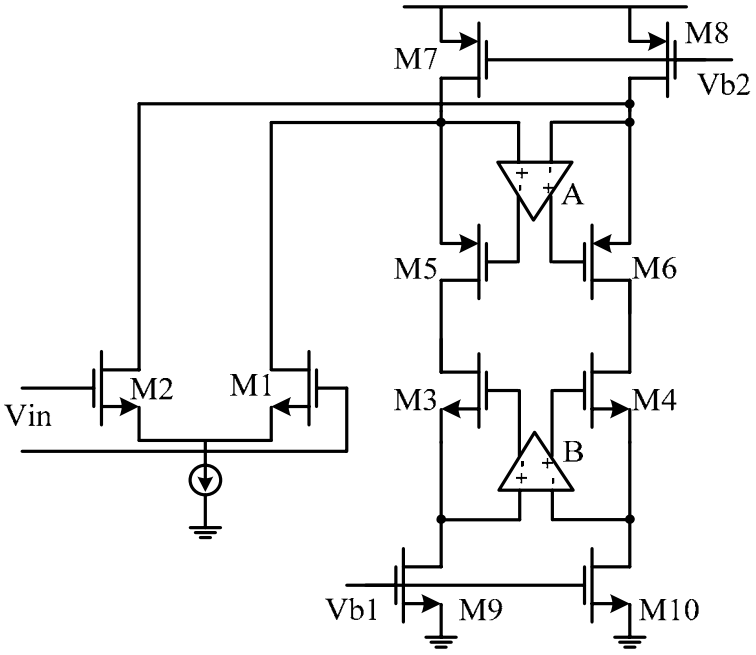


Figure 21: Single-ended Gain Boosting Amplifiers Replaced by Differential Counterparts

In order to understand this better consider the fully differential amplifier shown in figure 22.

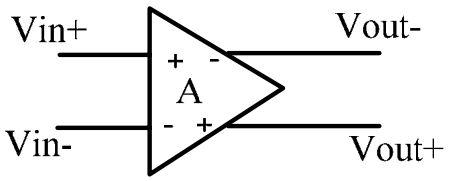


Figure 22: Fully Differential Amplifier

Assuming the voltage at the positive input V_{in+} changes by ΔV then the voltage at the corresponding output shown by V_{out-} changes by $-A\Delta V$. Since the input signals to the fully differential amplifiers used as the boosters are differential, if V_{in+} changes by ΔV, the voltage at the negative input, V_{in-} changes by $-\Delta V$. Since the input voltage to the negative input is $-\Delta V$ the corresponding output voltage shown by V_{out+} changes by $+A\Delta V$. The following relationship holds for the differential input and output voltages as shown below.

$$V_{out} = V_{out+} - V_{out-} = 2A\Delta V$$

$$V_{in} = V_{in+} - V_{in-} = \Delta V - (-\Delta V) = 2\Delta V$$

In which V_{out} is the differential output voltage and V_{in} is the differential input signal. So the following relationship holds between the input and output and output voltages.

$$V_{out} = V_{out+} - V_{out-} = AV_{in} = A(V_{in+} - V_{in-})$$

Now in figure 20, assuming the signals at the input of the upper boosters at nodes X and Y are then the signals at the output of the boosters are respectively, A_1V_X and A_1V_Y. Since the input signals for the boosters are coming form the fully differential folded cascode amplifier these signals are differential. So if one increases

with the amount of ΔV the other decreases with the same amount. Hence, the voltage at the output of the single ended boosters are respectively $A_1\Delta V$ and $-A_1\Delta V$. Comparing these output voltages with the output voltages of the fully differential amplifier shown above, it can be seen that the fully differential amplifier has the same outputs. As a result the two single ended boosters can be replaced with one fully differential booster in order to save space and to reduce the amount of redundant circuitry.

The gain boosted folded cascode amplifier shown in figure 21 consists of a main amplifier and two boosters. Each booster is a differential folded cascode amplifier just like the main amplifier without the boosters. The upper booster, which from now on will be referred to as the NMOS booster is just like the core amplifier. The lower booster will be referred to as the PMOS booster. PMOS input transistors are chosen for the PMOS booster as shown in figure 23. This choice is due to the fact that the input voltages for this booster, the drain voltages of M_9 and M_{10}, are small and close to the ground voltage. In order to make sure that the input transistors of the boosters are always on PMOS input transistors are chosen for the lower booster and for this reason it is referred to as the PMOS booster.

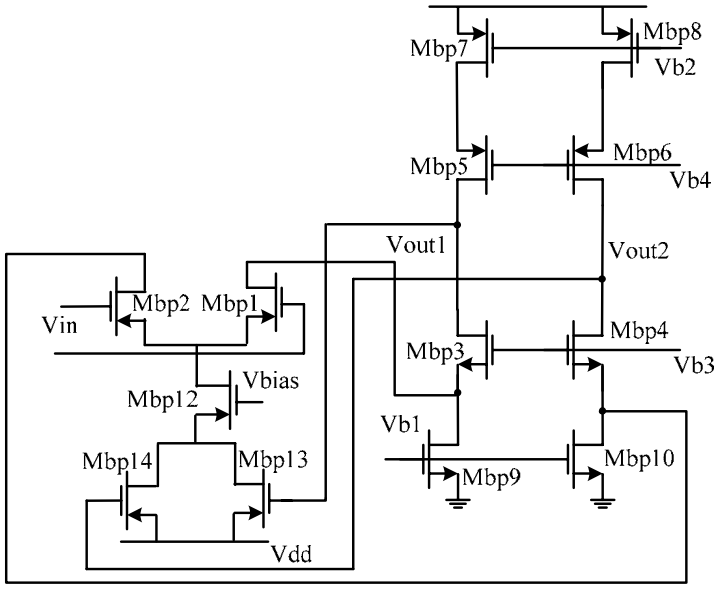


Figure 23: PMOS Booster Schematic

Using the output resistance and transconductance of the folded cascode differential amplifier calculated in section 3.2, the output resistance and transconductance for the gain boosted folded cascode differential amplifier can be derived. It was shown in section 3.3 that the gain boosting technique multiplies the output resistance by the gain of the gain boosting amplifier and it does not change the transconductance.

The output resistance for the folded cascode differential amplifier is the parallel combination of the resistance seen at the output looking up and down. The resistance seen looking down is $g_{m3}r_{o3}r_{o9}$ which is the resistance for the lower NMOS cascode. Now that we are boosting the gain of this lower cascode, the output resistance seen looking down is multiplied by the gain of the gain boosting amplifier, B. So the resistance seen looking down is $g_{m3}r_{o3}r_{o9}B$.

The resistance seen looking up before applying the gain boosting technique was $\left(g_{m5}r_{o5}\left(r_{o1}\|r_{o7}\right)\right)$. By applying the gain boosting technique the resistance seen looking up is multiplied by the gain of the booster, A. So the resistance seen looking up is $\left(g_{m5}r_{o5}\left(r_{o1}\|r_{o7}\right)\right)A$. The output resistance of the gain boosted folded cascode R_{out} is the parallel combination of the resistance seen looking up and the resistance seen looking down at the output node. The output resistance is given by equation (3.11) while the transconductance is the same as the transconductance of the input transistor and is given by equation (3.12).

$$R_{out} = g_{m3}r_{o3}r_{o9}B\left\|\left(g_{m5}r_{o5}\left(r_{o1}\|r_{o7}\right)\right)A\right. \qquad (3.11)$$

$$G_m = g_{m1} \qquad (3.12)$$

The midband gain for the gain boosted folded cascode differential amplifier is shown in equation (3.13).

$$A_v = G_m R_{out}$$

$$A_v = g_{m1}\left(g_{m3}r_{o3}r_{o9}B\left\|\left(g_{m5}r_{o5}\left(r_{o1}\|r_{o7}\right)\right)A\right.\right) \qquad (3.13)$$

3.4 Common Mode feedback

In high gain differential circuits, depending on the load, the output common mode (CM) level may not be well defined. In a differential pair with resistive loads, the output common mode voltage is well defined. If current sources replace the resistive loads then the common mode output voltage is not defined. The reason is that the output node is a node where two drains are connected together, which is like connecting two current sources in series. There is some resistance between the

common node of the two current sources and ground. If these current sources are perfectly matched one of them will source current to the output node and the other will sink the same current and the output bias voltage will be some undefined voltage between V_{dd} and V_{ss}, but if they are not matched, the difference between the currents will flow through the output resistance and the output voltage will become very large or very small. A differential feedback circuit can not define the common mode voltage level because it does not detect the common mode level at the output. To solve this problem, a common mode feedback circuit can be used which detects the common mode level of the output, compares it with a reference voltage and returns the error to the bias network to change the current of the tail current source. This ensures that the desired output common mode level is obtained as shown in figure 24.

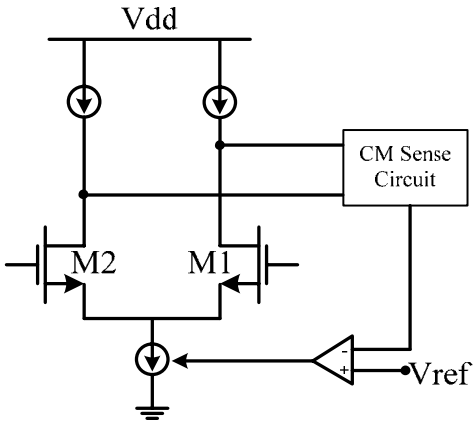


Figure 24: Common Mode Feedback Circuit Applied to a Simple Differential Amplifier

Recall that the common mode output voltage is $(V_{out1} + V_{out2})/2$, so the common mode feedback circuit can be two resistors in series [7], [14], [15], which connect the outputs together as shown in figure 25. It can be seen that if R_1 and R_2 have the same value, the voltage of the common node of R_1 and R_2 will be equal to

the common mode level of the output. If V_{out1} and V_{out2} increase, common mode output voltage increases and the feedback circuit will increase the current of M_1 and M_2. This causes the output voltage to be restored. There is a drawback in using R_1 and R_2 as the common mode level sensing circuitry. R_1 and R_2 should be large such that the output resistance of the op amp is not reduced. A large value for these resistors means more noise which appears directly at output, and it demands a lot of real estate in the chip layout.

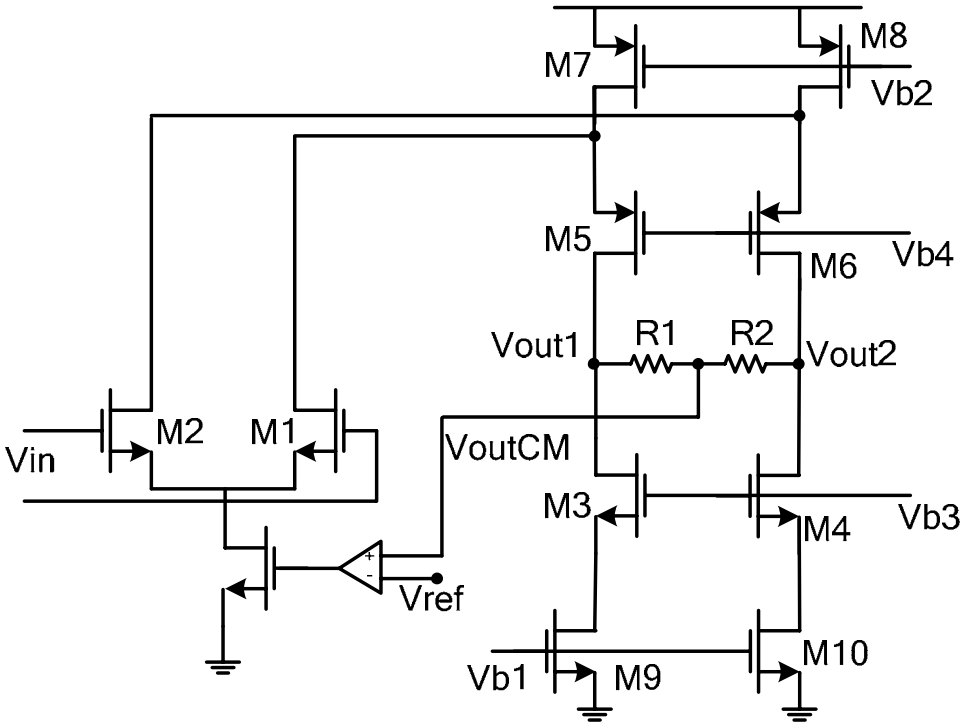


Figure 25: Common Mode Feedback Circuit Realized using Two Resistors

Another type of common mode feedback is shown in figure 26. Here two NMOS transistors M_{13} and M_{14} are placed in parallel, and are biased to operate in the triode region. The equivalent resistance of the two transistors is derived as follows and is given by equation (3.14).

$$R_{tot} = R_{o13} \| R_{o14} =$$

$$\frac{1}{\mu_n c_{ox} \frac{w}{l}(V_{out1} - V_{th})} \| \frac{1}{\mu_n c_{ox} \frac{w}{l}(V_{out2} - V_{th})}$$

$$R_{tot} = \frac{1}{\mu_n c_{ox} \frac{w}{l}(V_{out1} + V_{out2} - 2V_{th})} \qquad (3.14)$$

From equation (3.13), R_{tot} depends on $V_{out1} + V_{out2}$, so if V_{out1} and V_{out2} increase, R_{tot} decreases. This causes the current through M_1 and M_2 to increase and the current through M_5 and M_6 to decrease. As a result the output voltage drops to its common mode level. It must be mentioned that this kind of common mode feedback circuit is very sensitive to the circuit parameters.

Since the common mode feedback transistors which are in parallel with each other are in series with the rest of the circuit, these transistor sizes are chosen such that the voltage drop across these transistors is on the order of milli Volts. By doing this the common mode feedback transistors will have very negligible effect on the operation of the circuit in any way except keeping the common mode voltage at a specific voltage.

One reason to use common mode feedback in the folded cascode differential circuit as shown in figure 26 is that this amplifier is used in applications such as analog to digital converters, digital to analog converters, sigma delta modulators and switch capacitors. In order for these circuits to work properly, at some portion of the operation the input and output are shorted together. So it is necessary to make sure that the output common mode voltage stays at a specific voltage. By using the common mode feedback circuit as shown in figure 26 we make sure that the output

common mode voltage stays at the specific voltage equal to the input common mode voltage.

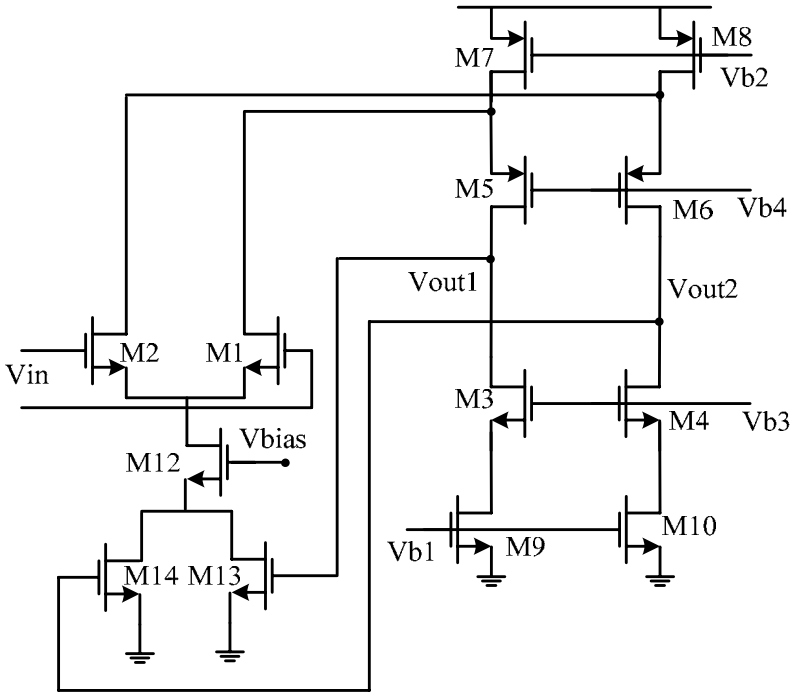


Figure 26: Common Mode Feedback Realized by Two NMOS Transistors

Chapter 4: Offset

4.1 Introduction

In the ideal study of amplifiers, it is usually assumed that they are symmetric. This means that the two sides of a differential amplifier have the same characteristics and the same bias current.

In reality though, identical devices exhibit a finite mismatch. This is because of the uncertainties in each of the processing steps. For example, two transistors that are intended to have the same nominal length and widths suffer from mismatch. Also, MOSFET transistors have threshold voltage mismatch. Threshold voltage is a function of doping levels in the channel and the gate. These doping levels change randomly from one device to the other. The MOSFET characteristic when in saturation is given by equation (4.1).

$$I_D = (1/2)\,\mu C_{ox}\,(W/L)\,(V_{GS} - V_{TH})^2 \qquad (4.1)$$

It can be seen that the mismatches between μ, C_{ox}, W, L, and V_{TH} cause mismatch between the drain currents assuming a given V_{GS}. In the case where we assume a given drain current, I_D, the mismatch in the above parameters causes mismatch in the gate source voltage, V_{GS}. As W and L increase their relative mismatches, $\Delta W/W$ and $\Delta L/L$ decrease. So, larger devices exhibit smaller mismatches. To better understand this, assume that the transistor size is increased so $\Delta W/W$ is decreased.

In this case, $\Delta L/L$ is decreased as well since an increase in WL causes random variations to experience greater averaging such that their magnitude is reduced. In this scenario, the device can be viewed as a parallel combination of smaller devices. The equivalent length L_{eq} and the overall variation ΔL_{eq} are as given in equations (4.2) and (4.3).

$$L_{eq} \approx \left(L_1 + L_2 + ... + L_n\right)/n \qquad (4.2)$$

$$\Delta L_{eq} \approx \left(\Delta L_1{}^2 + \Delta L_2{}^2 + ... + \Delta L_n{}^2\right)^{1/2} \Big/ n = \frac{\left(n\Delta L_0^2\right)^{1/2}}{n} = \frac{\Delta L_0}{\sqrt{n}} \qquad (4.3)$$

As can be seen from (4.3), as the width of the transistor increases, the equivalent change in the transistor length will decrease due to the increase in n. These results can be used for other device parameters such as V_{TH}, μC_{ox}. These parameters have smaller mismatch when the device size is increased. Device mismatches affect the performance of the circuit in different ways. One of the results of mismatch is DC offset. DC offset voltage and techniques used to reduce its effects will be discussed in more detail in the following sections.

4.2 DC Offset

Considering the differential amplifier shown in figure 27, in ideal case, $V_{out} = 0$ for $V_{in} = 0$, with perfect symmetry. But, due to mismatch there is a DC offset. DC offset is the value of V_{out} when $V_{in} = 0$. In practice, the input referred offset shown in equation (4.4) is used as a factor of merit. The input referred offset is the input voltage that causes the output dc voltage to be zero.

$$V_{OS,in} = V_{OS,out} / A_v \qquad (4.4)$$

Offset affects the performance and limits it in a number of ways. Consider a differential amplifier with a small signal input. Hence, the output includes both the amplified signal and the dc offset. If the gain is high then the offset may saturate the amplifier and cause nonlinear operation.

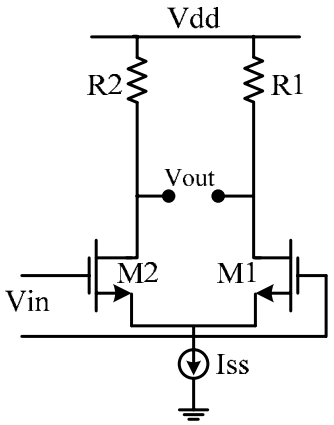


Figure 27: Simple Differential Amplifier

Offset also affects the precision limit in signal measurements. For example in a comparator that compares an input signal with a reference voltage V_{ref}, the input referred offset imposes a lower bound on $V_{in} - V_{ref}$.

We begin by calculating the offset voltage in the simple differential pair shown in figure 27. The input referred offset is calculated for $V_{out} = 0$. It is assumed that both the input transistors and loads have mismatch. These mismatches are formulated as follows (it is assumed that $\lambda = \gamma = 0$ and μC_{ox} is mismatch free):

$$V_{TH1} = V_{TH} \qquad V_{TH2} = V_{TH} + \Delta V_{TH}$$

$$(W/L)_1 = W/L \qquad (W/L)_2 = W/L + \Delta(W/L)$$

$$R_1 = R_D \qquad R_2 = R_D + \Delta R$$

In order to have $V_{out} = 0$, $R_1 I_{D1} = R_2 I_{D2}$. Therefore, the current in the two branches are not equal. As a result, the following relationships hold.

$$I_{D1} = I_D$$

$$I_{D2} = I_D + \Delta I_D .$$

$$V_{OS,in} = V_{GS1} - V_{GS2}$$

$$V_{OS,in} = \sqrt{\frac{2I_{D1}}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1} - \sqrt{\frac{2I_{D1}}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)_2}} - V_{TH2}$$

$$\begin{aligned} V_{OS,in} &= \sqrt{\frac{2}{\mu \cdot C_{ox}}}\left[\sqrt{\frac{I_D}{\frac{W}{L}}} - \sqrt{\frac{I_D + \Delta I_D}{\frac{W}{L} + \Delta\left(\frac{W}{L}\right)}}\right] - \Delta V_{TH} \\ &= \sqrt{\frac{2}{\mu \cdot C_{ox}}}\sqrt{\frac{I_D}{W/L}}\left[1 - \sqrt{\frac{1+\frac{\Delta I_D}{I_D}}{1+\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)}}\right] - \Delta V_{TH} \end{aligned} \qquad (4.5)$$

It is assumed that $\frac{\Delta I_D}{I_D}$ and $\Delta\left(\frac{W}{L}\right)\Big/\left(\frac{W}{L}\right)$<<1. Also for $\varepsilon << 1$, the following relationships are well known: $\sqrt{1+\varepsilon} \approx 1 + \varepsilon/2$ and $\left(\sqrt{1+\varepsilon}\right)^{-1} \approx 1 - \varepsilon/2$. Equation (4.5) is reduces to equation (4.6).

$$\begin{aligned} V_{OS,in} &= \sqrt{\frac{2I_D}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)}}\left\{1 - \left(1 + \frac{\Delta I_D}{2I_D}\right)\left[1 - \frac{\Delta(W/L)}{2(W/L)}\right]\right\} - \Delta V_{TH} \\ &= \sqrt{\frac{2I_D}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)}}\left[\frac{-\Delta I_D}{2I_D} + \frac{\Delta(W/L)}{2(W/L)}\right] - \Delta V_{TH} \end{aligned} \qquad (4.6)$$

The products of two small quantities can be neglected. So,

$$I_D R_D = (I_D + \Delta I_D)(R_D + \Delta R_D) \approx I_D R_D + \Delta I_D R_D + I_D \Delta R_D$$

$$\Delta I_D / I_D \approx -\Delta R_D / R_D$$

$$V_{OS,in} = \frac{1}{2}\sqrt{\frac{2I_D}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)}}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH} \qquad (4.7)$$

We also know that $\sqrt{\frac{2I_D}{\mu \cdot C_{ox}\left(\frac{W}{L}\right)}}$ is equal to the overdrive voltage, $V_{GS} - V_{TH}$.

Reducing equation (4.7), the input referred offset voltage for the simple differential amplifier is given by equation (4.8).

$$V_{OS,in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH} \qquad (4.8)$$

As can be seen from equation (4.8), the input referred offset voltage is dependent on mismatches in device size and load. It is also dependent on the overdrive voltage and threshold voltage mismatch which are directly transferred to the input.

Different techniques have been proposed to reduce the input referred offset voltage of the amplifiers. Some of the previous offset reduction techniques will be reviewed in the following section.

4.3 Offset Reduction Techniques

The purpose of this section is to review the offset reduction techniques used in amplifiers. There are two main categories of offset reduction techniques: auto-zeroing and chopper stabilization (CHS). Correlated double sampling (CDS) which is a special case of auto-zeroing will be discussed as well. It has to be noted that auto-zeroing is a sampling technique, while chopper stabilization is a modulation technique. In this chapter, we will briefly review the auto-zeroing and the chopper stabilization technique, but the main focus is on the auto-zeroing techniques. These techniques are used in different circuits such as voltage amplifiers, ADCs, DACs, integrators, and comparators.

In the following sections, the auto-zeroing techniques are reviewed, and practical implementation issues are discussed.

4.3.1 Auto-zeroing and Correlated Double Sampling

As mentioned before, auto-zeroing techniques are based on sampling. In this technique, the offset plus noise is sampled in one cycle usually called the sampling phase. Then it is subtracted from the contaminated signal at the input or the output of the amplifier during the amplification phase. The cancellation can also be done at some other point between the input and the output called the nulling point. This can be seen in figure 28. The nulling point is shown by letter N.

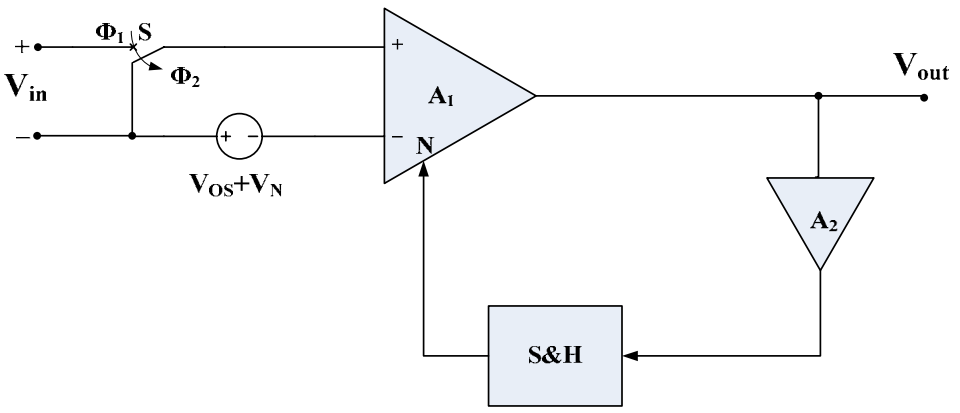


Figure 28: Auto-zeroing Technique

This technique will cancel the offset at the amplifier input. Also if the noise at the amplifier input is almost constant over time, it will be reduced significantly. Low frequency noise, such as 1/f noise will be reduced significantly.

The auto-zeroing process has two phases; a sampling phase and signal processing phase. In the sampling phase, the offset and the noise are sampled and stored. During the signal processing phase, the amplifier is theoretically offset free and ready for amplification. As can be seen in figure 28, during the sampling phase ϕ_1, the amplifier inputs are connected to a common mode voltage. The offset is canceled using a nulling point N thru an appropriate feedback configuration, and the output is forced to a very small value. During the signal processing phase ϕ_2, the input of the amplifier is connected back to the signal and is ready for amplification.

At this point the effectiveness of the auto-zeroing technique is investigated. The control variable at the nulling input can be a voltage or a current. We will denote it by C_N. Assume V_{os} is the input referred offset of the amplifier, which is the output offset during the sampling phase divided by the gain of the amplifier during the signal processing phase. The relationship between the control variable and input referred

offset is shown in figure 29. This relationship can be linear or non-linear. Assume that the amplifier has a large initial offset. The feedback loop configuration has to bring this large offset very close to zero. At the end of the sampling phase, the control variable C_N is stored. During this process an error might occur in the control variable for example due to charge injection of the sampling switch. This error will lead to residual offset, shown in figure 29 by V_{OS_lin} and V_{OS_NL} depending on whether the relationship between the control variable and the input referred offset is linear or not. Using a linear or non-linear control characteristic depends on the initial offset. Assume the difference between the initial offset and the offset for which the gain of the non-linear characteristic is equal to the slope of the linear characteristic, is ΔV. As can be seen in figure 29(a) for an initial offset greater than ΔV, the non-linear characteristic has a larger offset. For an initial offset smaller than ΔV, the non-linear characteristic has a smaller residual offset. So it is better to use a non-linear characteristic only if the initial offset is small.

The auto-zeroing technique can also be used to reduce the low frequency noise in amplifiers such as $1/f$ noise. The offset voltage is assumed constant since it is a DC voltage. This assumption can not be made for low frequency noise. The efficiency of the auto-zeroing technique depends on the correlation between the noise sample and the signal sample it is being subtracted from. The correlation between the two samples of $1/f$ noise that are separated by a certain time interval decreases much slower than it does for a broad band noise such as white noise.

A low frequency noise such as $1/f$ noise can be reduced significantly by auto-zeroing but this does not hold for a broadband noise such as white noise. Since auto-zeroing is subtracting from noise a recent sample of the same noise, for DC or low frequency noise this results in cancellation or reduction in the offset or noise.

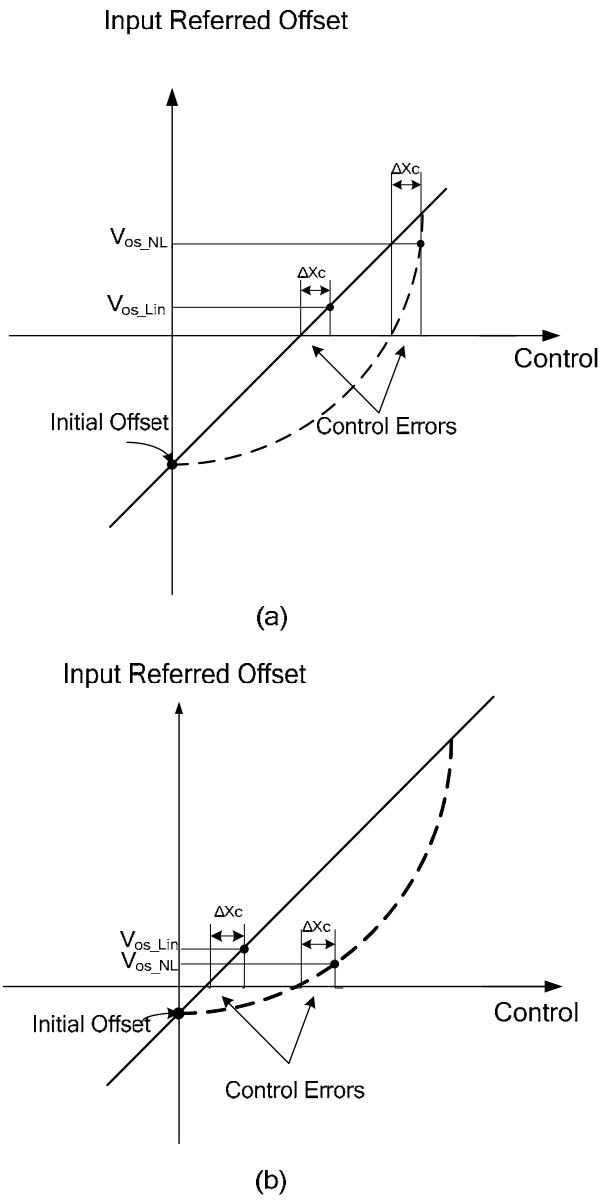


Figure 29: Input Referred Offset vs. the Control Variable (a) Large Initial Offset (b) Small Initial Offset

4.3.2 Correlated Double Sampling

Correlated double sampling is a special case of the auto-zeroing technique that is followed by a sample and hold. It was originally used in charged coupled devices (CCDs) to reduce the noise [16], [17].

In the auto-zeroing process the amplifier is disconnected from the signal during the sampling phase. So the amplifier can only be used during the amplification phase. As a result this technique is not suitable for continuous-time applications. It can be used in sampled data systems where the amplifier is disconnected, its noise and offset are sampled and stored and then the amplifier is connected back to the signal for amplification.

4.3.3 The Chopper Stabilization Technique

In this section, the second category of offset and noise reduction techniques called the chopper stabilization technique (CHS) will be briefly described. As seen before, the auto-zeroing technique reviewed in the previous section is based on sampling. The chopper stabilization technique is different in the sense that it uses modulation to reduce the offset and noise. This technique modulates the signal to a higher frequency, amplifies it, and then demodulates it back to base band. This technique is shown in more detail in figure 30.

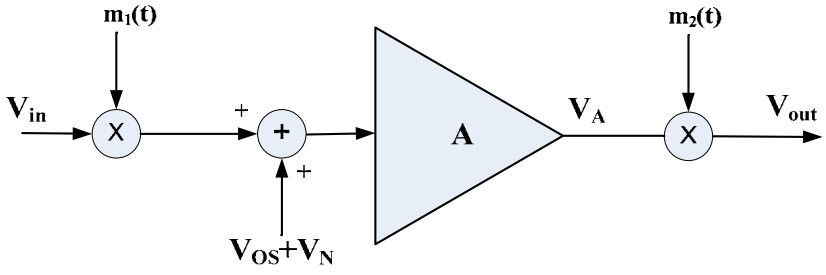


Figure 30: The Chopper Stabilization Technique

As can be seen in figure 30, the input signal is multiplied by a square wave signal with amplitude of 1 and period $T = 1/f_{Chop}$. Assuming that the input signal frequency is less than half of the chopper frequency, there will be no aliasing. After modulation, the signal is amplified and then demodulated back to the base band. So if the input signal has an amplitude of V_{in}, the output of the modulator is a square wave with period T and amplitude V_{in}. If the amplifier has a gain of A and an unlimited bandwidth then the output of the amplifier is a square wave with period T and amplitude AV_{in}. In this case, the signal at the output of the demodulator is $A \cdot V_{in}$. But in reality the amplifier has a limited bandwidth. Assume that the amplifier has a gain of A and a bandwidth that is two times the chopper frequency acting like a low pass filter. The output of the amplifier is a sine wave with amplitude of $(4/\pi) AV_{in}$. The amplitude of the dc output after filtering is equal to $(8/\pi^2) AV_{in}$. The finite gain of the amplifier will add some spectral components and in order to cancel these components low pass filtering needs to be done. After low pass filtering, this will correspond to a dc value of approximately $0.8A$.

4.4 Implementation Issues and Challenges

In this section, different auto-zeroing techniques used for offset reduction are briefly reviewed. Practical implementation issues for each technique will be investigated and solutions are provided for each problem. As we know the simplest way to implement auto-zeroing techniques for offset reduction is utilizing a simple switch. In practice, a simple switch has non ideal effects which will cause problems in the auto-zeroing technique implementation. So before reviewing the auto-zeroing

techniques, the non idealities of a simple switch used in all of the auto-zeroing techniques are investigated.

4.4.1 Switches and Their Non-ideal Effects

Auto-zeroing techniques often use a MOS switch for sample and hold circuits. The modulators in the chopper stabilization technique are implemented using MOS switches as well. The MOS switch has non idealities such as clock feedthrough, channel charge injection, sampled noise, leakage current, non-zero and non-linear on-resistance.

Clock feedthrough and charge injection are caused by the charge in the MOS channel during conduction. When the MOS switch is turned off, the charges in the conduction channel are removed thru the source, drain and substrate. The charges released to the substrate can be ignored. The charges removed thru the source and the drain will be stored on the source and drain capacitances. The partitioning of these charges depend on the source and drain capacitances, the transistor's on resistance and the slope of the clock signal applied to the gate terminal. A simple sample and hold MOS switch is shown in figure 31.

As can be seen in the figure, the channel charge will be divided equally between the source and the drain if the source and drain capacitors, C_p and C_h are equal or if the switching time is much less than time constant $R_{on}C$. If there is slow transition clock signal, the channel charge will be unequally divided between the source and drain capacitors. Also, most of the charge will be stored on the larger

capacitor. In this case, it is very difficult to accurately predict the charge stored on the hold capacitor C_h. This is called charge injection.

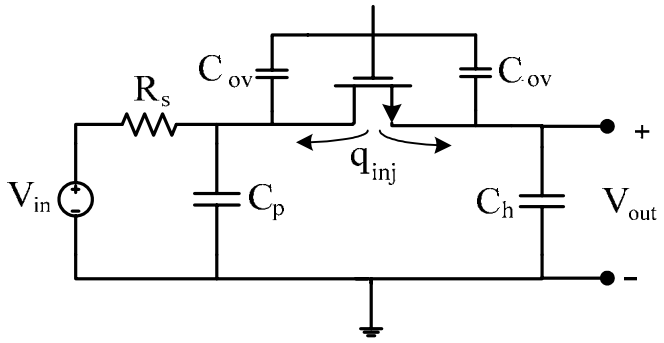


Figure 31: Sample and Hold Circuit used in Auto-zeroing Techniques

There are techniques to alleviate the effects of charge injection. The simplest one is to use complementary switches such that the charge that is injected by one transistor is absorbed by the complementary transistor building its channel. This technique is very inefficient. It is very difficult to match the complementary devices together. The clock phase jitter also degrades the charge mismatch even more. Here, we will describe more efficient techniques to deal with the effects of charge injection.

1. If capacitor C_p is much larger than C_h and the clock transition is very slow, then almost all of the injected charge will be stored on the source capacitor C_p. The charge stored on the source capacitor, q_{inj} will be almost reduced to zero. This can be done by adding a capacitor to the drain of the MOS switch. This technique requires the clock transition to be very slow, and as a result it will set a limit on the operating frequency. Also as can be seen in figure 31, the charge injection due to the gate drain overlap capacitance, C_{ov}, still exists.

2. Make the source and drain capacitors C_h and C_p equal. This forces an equal amount of charge to be stored on these capacitors. Also, use half size dummy switches to compensate for the stored charge. These dummy switches turn on when the MOS switch turns off and absorb the charge stored on the source and drain capacitors. This is shown in figure 32.
3. Design the sample and hold switch such that the transition time is very fast. This will force the charges injected when the switch turns off to be divided equally between the source and the drain capacitors. As well, dummy sized switches should be used as to compensate for the injected charge.
4. Use a fully differential structure as shown in figure 33. As long as the differential drain capacitors are matched, the charge stored on them will be equal. The charges will be canceled due to the differential nature of the structure; since, it is a common mode voltage.

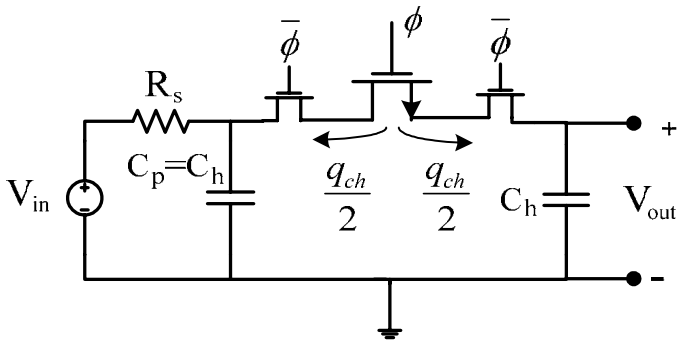


Figure 32: Sample and Hold Circuit with Equal Capacitors ($C_p = C_h$) and Half-sized Dummy Switches

The techniques mentioned above are not perfect. None of these techniques offer complete charge injection cancellation. For example in the cases where the half sized dummy transistors are used, attention should be paid to the layout to match the

dummy switches. The most efficient way is to combine techniques 3 and 4 while using a fully differential structure with half sized dummy switches.

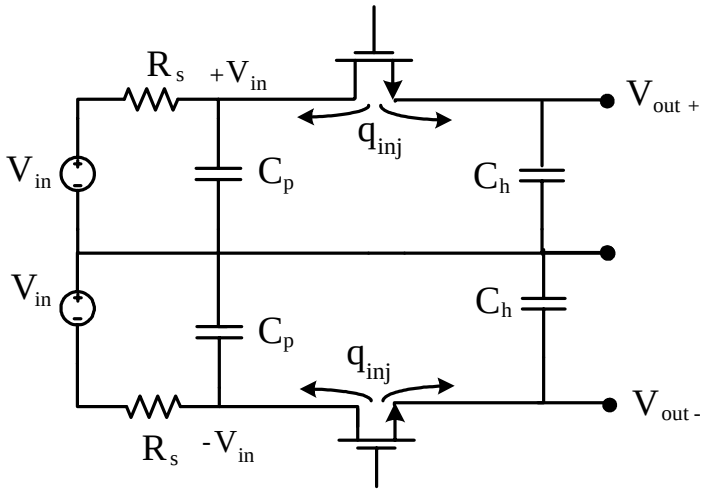


Figure 33: Fully Differential Structure to Cancel the Charge Injection Effects

The other important factor is that simulation software, like SPICE, do not give accurate results for charge injection simulations [18]-[22]. This inaccuracy occurs due to the incorrect modeling of the MOS transistor intrinsic charges. The inaccurate charge conservation of the simulator and the division of the channel charge between the source and the drain invalidate models generated by simulation software.

There are other factors affecting the charge injection as well. Each time the switch opens, the thermal noise of the switch will be stored on the hold capacitor C_h. This noise charge which is equal to kTC_h causes an additional error charge. This is usually called reset noise and corresponds to a noise voltage variance of kT/C_h.

In the situation where there is a long hold time or a high operating temperature [23], the source-bulk leakage current, I_{leak}, will introduce an error charge. The error charge is created due to the discharge of the hold capacitor.

The charge error stored on the hold capacitor, C_h, is due to clock feedthrough, charge injection, thermal noise of the switch, and leakage current. The relationship is expressed by equation (4.9).

$$\sigma_v = \alpha \frac{C_{ov}}{C_{ov} + C_h} V_{pk-pk} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{leak} T_h}{C_h} \qquad (4.9)$$

Here, V_{pk-pk} is the peak to peak voltage swing of the clock signal. The factor α is an attenuation factor, making the first term smallest. It accounts for the amount of charge from the overlap capacitor that flows to the substrate instead of the hold capacitor.

As can be seen from equation (4.9), the voltage error introduced at the output of the sample and hold will reduce by increasing the hold capacitor.

At this point, we will briefly review different auto-zeroing techniques for offset cancellation.

4.4.2 The Open Loop Offset Cancellation Technique

One of the easiest ways to perform offset reduction is to sample the offset at the output. This is also called output offset storage [24]-[26]. This technique is shown in figure 34.

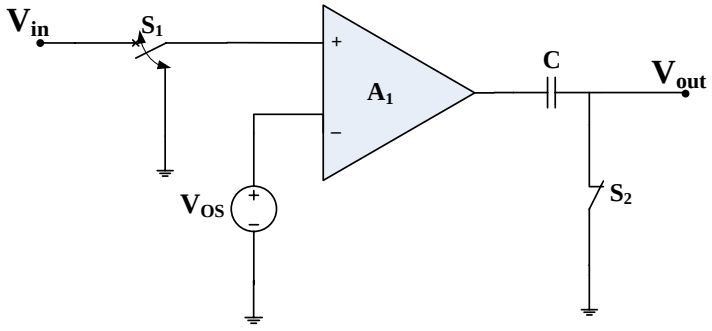


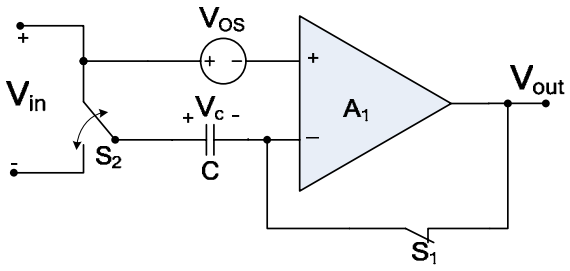
Figure 34: Open Loop Offset Cancellation Technique

As can be seen in figure 34, V_{os} is the offset voltage at the input of the amplifier, and C is the hold capacitor at the amplifier output. This capacitor is used to store the output offset voltage. In the auto-zeroing phase, switch S_1 and S_2 are both connected to ground. The output which is due to the offset at the input of the amplifier is stored on capacitor C. When switch S_2 is opened, the output offset voltage remains on the capacitor C. Ideally, this voltage would be equal to AV_{os} which is the amplifier input offset voltage multiplied by the amplifier gain. But in practice when switch S_2 opens, the charge injection of this switch causes an error in the voltage stored on the output capacitor C. This error voltage is approximately equal to q_{inj}/C. In the signal amplification phase, switch S_2 is open, and switch S_1 is connected to the signal at the input of the amplifier. So the input referred residual offset is limited by the charge injection of S_2. This can be referred to the input and is equal to $q_{inj}/(AC)$. In the case where a differential configuration is used, the input referred offset is limited by the charge injection mismatches Δq_{inj} between the two switches at the output nodes.

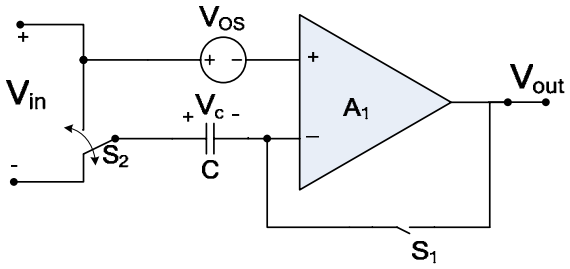
This technique will work if the amplifier does not saturate during the auto-zeroing phase. Since the input offset is unknown, the amplifier gain should be small, on the order of $10V/V$ or less to avoid saturation. In order to solve this problem, the amplifier should be used in a closed loop configuration. The closed-loop offset cancellation technique is described below.

4.4.3 The Closed-Loop Offset Cancellation Technique

As described in the previous section, it is not desirable to use an open loop configuration for offset cancellation since the high amplifier open loop gain causes the output to saturate. So, the offset cancellation techniques used usually have closed loop configurations. The closed loop offset cancellation technique is shown in figure 35.



(a)



(b)

Figure 35: Closed Loop Offset Cancellation (a) Auto-zeroing Phase (b) Amplification Phase

Figure 35(a) shows the auto-zeroing phase, while figure 35(b) shows the signal amplification phase. As can be seen in figure 35(a) during the auto-zeroing phase, switch S_1 is closed and switch S_2 is disconnected from the signal path. Switch S_2 shorts the amplifier inputs together. So, the amplifier is connected in a unity gain feedback configuration. Capacitor C at the input is used to store the offset voltage at the input of the amplifier during the auto-zeroing phase. The voltage on

this capacitor is referred to as V_c. This voltage will be subtracted from the signal during the amplification phase. Here, we assume that the amplifier has an open loop gain A which is much larger than unity. In this case, the voltage stored on capacitor C is given by equation (4.10).

$$V_c = \frac{A}{1+A} V_{os} \tag{4.10}$$

Assuming $A >> 1$, then V_c is equal to V_{os}.

In practice when S_1 opens, its charge injection causes an error equal to q_{inj}/C, so we have $V_c = \frac{A}{1+A} V_{os} - \frac{q_{inj}}{C}$. During the amplification phase, switch S_1 is opened. While, switch S_2 is connected to the amplifier input as shown in figure 35(b). The input referred residual offset is equal to the voltage stored on capacitor C subtracted from the offset voltage at the input. This is depicted in equation (4.11).

$$V_{res\_offset} = V_{os} - V_c = V_{os} - \left(\frac{A}{1+A} V_{os} - \frac{q_{inj}}{C} \right) \cong \frac{V_{os}}{A} + \frac{q_{inj}}{C} \tag{4.11}$$

As can seen from equation (4.11), the input referred residual offset is equal to the offset voltage V_{os} divided by the amplifier gain A. The input referred residual offset is limited by the error induced due to charge injection. This error could be reduced if the amplifier is used in a fully differential mode. The error will be limited to the mismatch error of the charge injections.

In the closed loop offset cancellation technique, the amplifier is not available for amplification during the auto-zeroing phase. This is acceptable for most applications but becomes a draw back in applications where continuous-time

amplification is necessary. For these applications, the problem can be solved by duplicating the auto-zeroed amplifier and using it in a configuration called ping-pong. This technique will be described in the section 4.4.6.

4.4.4 Multistage Offset Storage

In most applications, a high gain amplifier structure is necessary to provide the necessary precision. In order to have a high gain, multiple amplifiers are used in series [26], [27]. In this case the open loop offset or closed loop offset cancellation techniques are used for each of the amplifiers in the series. Figures 36 and 37 show the multistage offset cancellation technique. Figure 36 shows the open loop offset cancellation method used for auto-zeroing in each of the amplifier stages. Figure 37 shows the closed loop offset cancellation technique used for auto-zeroing in each of the amplifier stages.

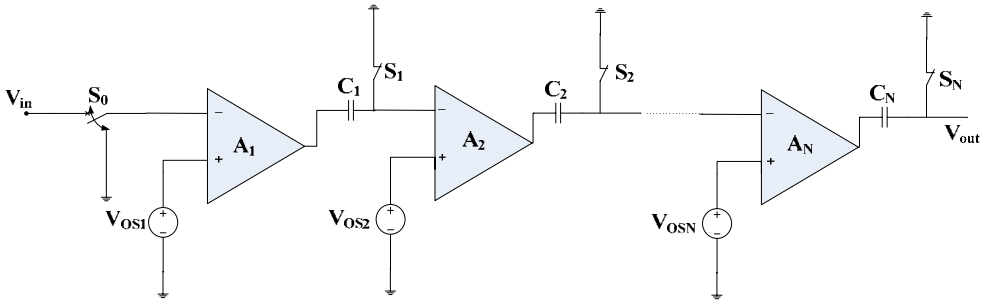


Figure 36: Multistage Offset Cancellation using Open-Loop Offset Redution in Each Stage

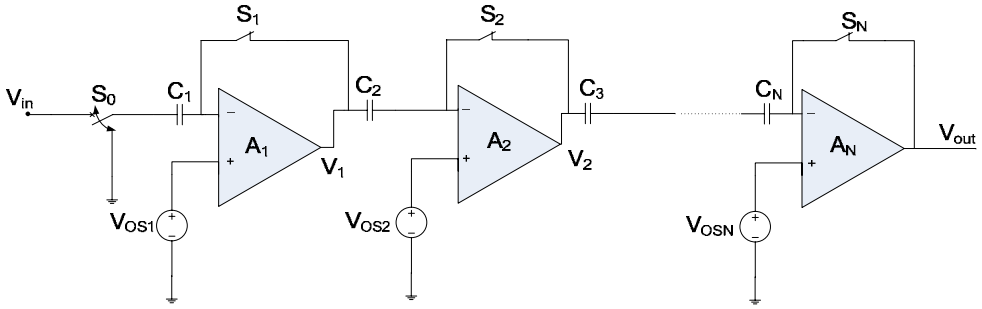


Figure 37: Multistage Offset Cancellation using Closed-Loop Offset Reduction in Each Stage

As shown in figure 36 during the auto-zeroing phase switches S_0, S_1, S_2,…, and S_N are connected to ground . Then, switch S_1 is opened first. This will cause an error on the charge stored on capacitor C_1 due to the charge injection of the switch. This error can be considered as part of the input referred offset voltage of the second amplifier and will be canceled along with V_{os2}. Then switch S_2 is opened, and the same process for switch S_1 is repeated. The other switches S_3... S_N are opened consecutively, and the process is repeated for each one of them. This way the only offset voltage that affects the output voltage is the one caused by the charge injection error of switch S_N. The gain is the multiplication of the gain of each stage. The equivalent input-referred offset is shown in equation (4.12).

$$V_{res\_offset} = \frac{1}{A_1 A_2 ... A_N} \cdot \frac{q_{inj-N}}{C_N} \qquad (4.12)$$

This is basically the charge injection error caused by switch S_N divided by the total gain which is the equal to multiplication of the gain of all of the stages.
At the end of the auto-zeroing technique switch S_0 is connected to the input signal and the amplifier is in the amplification mode. As can be seen from equation (4.12), the input referred residual offset in this case is much smaller than the same voltage in the open loop and closed loop offset reduction techniques. This is due to the high gain delivered by multiple stages.

Figure 37 shows the multistage offset cancellation technique using closed loop offset reduction for each stage. In this case during the auto-zeroing phase, switch S_0 is connected to ground, and switches S_1, S_2,…, and S_N are connected to form a

closed loop configurations. When switch S_1 opens, the error caused by charge injection is stored on capacitor C_1. The output voltage of the first amplifier is equal to $V_{os1} + A_1 q_{inj1}/C_1$. When switch S_2 opens, the output voltage of the first amplifier, the output offset voltage and charge injection voltage of switch S_2, q_{inj2}/C_2 are stored on capacitor C_2. This process is repeated for all of the switches $S_3 ... S_N$. So when switches S_1 and S_2 are opened sequentially one after the other, then the output of the second amplifier is independent of the output voltage of the first amplifier stage and equal to $V_{os2} + A_2 q_{inj2}/C_2$. This is a very positive result as it demonstrates that the output of the second amplifier does not magnify the offset voltage and charge injection voltage of the first stage. The offset and charge injection errors do not propagate through the stages in this case. The output offset is defined by the last stage (N th stage) and it equal to $V_{osN} + A_N q_{injN}/C_N$. The residual input referred offset is as shown in equation (4.13) below.

$$V_{res\_offset} \cong \frac{V_{osN} + A_N \frac{q_{inj} N}{C_N}}{A_1 A_2 ... A_N} \qquad (4.13)$$

As can be seen, this input referred residual offset is much lower than the input referred offset of the open loop and close loop offset cancellation techniques used in single stage amplifiers with a low gain.

It can be concluded from this discussion, that in multistage offset cancellation technique if the switches are opened sequentially then the output offset is determined by the last stage. This is the case whether open loop or closed loop offset

cancellation techniques are used. Furthermore, the high gain achieved by cascading the amplifier stages will cause the input referred residual offset to be very small.

4.4.5 Closed-Loop Offset Compensation Using an Auxiliary Offset Storage

As seen in the previous techniques used for offset reduction, there is an error in the residual offset term. This error, called charge injection voltage is caused at the end of the auto-zeroing phase when the switch used for sampling is opened. This term is equal to q_{inj}/C and is seen in equation (4.9).

There are different ways to reduce the effect of the charge injection error in the input referred residual offset. One is to store the offset voltage at some point other than the amplifier input during the auto-zeroing phase. This node is called the nulling node and is usually denoted as N. Assume A_1 is the gain from the amplifier input to the output and A_2 is the gain from the nulling point to the amplifier output. As we know $A_1 >> A_2$. Unlike the previous cases where the charge injection error voltage was multiplied by A_1, in this case it will be multiplied by A_2. So the charge injection voltage is going to be reduced by A_2/A_1. This ratio should be set much smaller than one. One configuration to achieve this auxiliary point offset reduction is shown in figure 38.

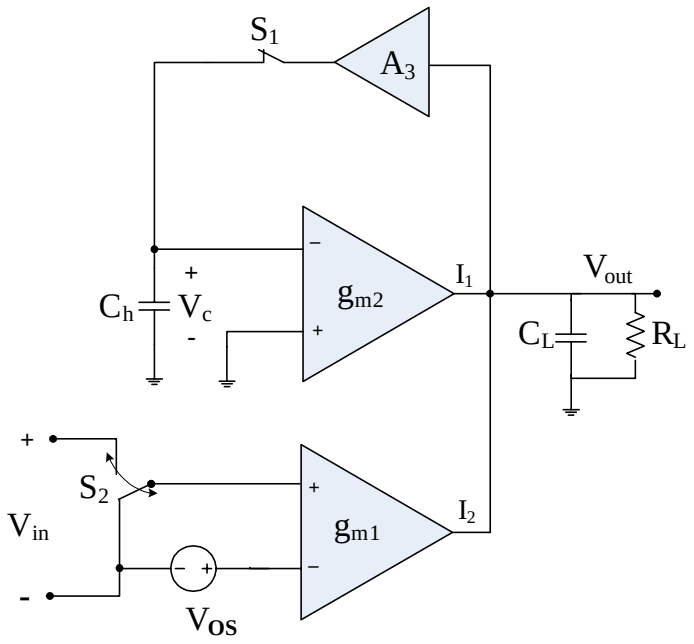


Figure 38: Offset Reduction using an Additional Auxiliary Point

As seen in figure 38, transconductance stages g_{m1} and g_{m2} effectively implement gain stages A_1 and A_2. Amplifier A_3 is a buffer amplifier which isolates gain stage A_1 from the offset storage capacitor C_h. Unless gain stage A_2 does not provide enough gain, A_3 can be a simple voltage follower stage. This way a large offset storage capacitor can be used without slowing down the auto-zeroing process. The large hold capacitor is mainly used to reduce the charge injection voltage which is q_{inj}/C_h. It also reduces the switch reset noise which is equal to kT/C_h and is sampled on the offset storage capacitor along with the offset voltage and the charge injection error voltage.

In the block diagram shown in figure 38, it is assumed that the inputs of the main amplifier A_1 are shorted together but switch S_1 is still open. So the compensation loop is not activated yet. In order to have zero input referred offset at

the input of the main amplifier A_1, the output currents of the amplifiers A_1 and A_2, denoted by I_1 and I_2 need to be equal. So we have the following:

$$I_1 = -g_{m1}V_{os}$$

$$I_2 = -g_{m2}V_c$$

$$I_1 + I_2 = 0 \;\Rightarrow\; V_c = -\frac{g_{m1}}{g_{m2}}V_{os} \qquad (4.14)$$

As mentioned before the ratio for g_{m1}/g_{m2} which is equal to A_1/A_2 should be chosen much larger then one. This way the control voltage V_c will be much larger then the offset voltage, V_{os} at the input of A_2. This offset is caused by the non-idealities of gain stages A_2 and A_3. There is also an upper limit on the maximum value of the control voltage which from now on will be referred to as $V_{c\max}$. This maximum voltage should be chosen such that the maximum input offset voltage $V_{os\max}$ can still be compensated for. Taking this into consideration the maximum value for the ratio of the transconductance of the first and second gain stages, g_{m1}/g_{m2} is $\left|V_{c\max}/V_{os\max}\right|$. This sets the upper bound for g_{m1}/g_{m2}.

During the auto-zeroing phase switch S_1 is closed. The initial offset at the output before switch S_1 is closed is equal to $-A_1V_{os}$. After switch S_1, is closed the output offset voltage is the initial offset at the output, $-A_1V_{os}$, divided by the loop gain of the compensation loop and is equal to $-A_1V_{os}/(A_2A_3)$. As a result, the input referred offset voltage at the input of the main amplifier is given by equation (4.15).

$$V_{res\_offset} = -\frac{A_1V_{os}}{A_1A_2A_3} \cong -\frac{V_{os}}{A_2A_3} \qquad (4.15)$$

From figure 38, it can be seen that $A_1 = g_{m1}R_L$ and $A_2 = g_{m2}R_L$. Equation (4.15) shows that the input referred residual offset can be made small by increasing the loop gain, A_2A_3. If amplifiers A_2 and A_3 are designed with a high gain then the input referred residual offset will be small.

In the analysis above, the charge injection error when switch S_1 is opened has been ignored. By taking into account the charge injection error when S_1 is opened, the following relationship holds for the input referred residual offset:

$$V_{res\_offset} \cong -\frac{V_{os}}{A_2A_3} - \frac{A_2}{A_1}\frac{q_{inj}}{C_h} = -\frac{V_{os}}{A_2A_3} - \frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h} \qquad (4.16)$$

As can be seen in equation (4.16), the input referred offset voltage is a combination of the offset voltage and the charge injection error. It can be seen that the charge injection error is reduced by g_{m2}/g_{m1} which is less than one. As mentioned before the first term can be made very small by increasing the loop gain A_2A_3. Assuming the first term in equation (4.16) can be ignored, we have the following:

$$V_{res\_offset} \cong -\frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h} \quad \Rightarrow \quad V_{res\_offset\_\max} \geq \left| -\frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h} \right|$$

$$g_{m1}V_{res\_offset\_\max} \geq g_{m2}\frac{q_{inj}}{C_h} \qquad (4.17)$$

$$\frac{g_{m1}}{g_{m2}} \geq \frac{q_{inj}/C_h}{V_{res\_offset\_\max}} \qquad (4.18)$$

$g_{m2}\frac{q_{inj}}{C_h}$ is the current at the output of amplifier A_2 which is caused by charge injection. $g_{m1}V_{res\_offset\_\max}$ is the output current of amplifier A_1 which is due to the maximum residual input referred offset at the input of the main amplifier stage. Equations (4.17) and (4.18) show that the minimum value for the ratio g_{m1}/g_{m2} should be chosen such that, $g_{m2}\frac{q_{inj}}{C_h}$ is less than $g_{m1}V_{res\_offset\_\max}$. This is the lower bound for g_{m1}/g_{m2}. As analyzed before, the upper bound is defined by the ratio of the maximum control voltage, $V_{c\max}$ before A_2 saturates to the maximum initial offset, $V_{os\max}$ at the input of the main amplifier.

$$\frac{q_{inj}/C_h}{V_{res\_offset\_\max}} \le \frac{g_{m1}}{g_{m2}} \le \frac{V_{c\max}}{V_{os\max}} \tag{4.19}$$

If the maximum input referred residual offset is kept very small then this auto-zeroing technique will be limited by the charge injection error voltage term which is reduced by the ratio of g_{m2}/g_{m1}. It is desirable to keep the maximum input referred residual offset contribution, $V_{os\max}/(A_2A_3)$ much smaller than the charge injection contribution $\frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h}$. Equation (4.20) and (4.21) set a condition on the gain of A_2.

$$\frac{V_{os\max}}{A_2A_3} < \frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h} \quad \Rightarrow \quad \frac{V_{os\max}}{A_2A_3} < \frac{A_2}{A_1}\frac{q_{inj}}{C_h} \tag{4.20}$$

$$A_2 > \sqrt{\frac{A_1V_{os\max}}{A_3\frac{q_{inj}}{C_h}}} \tag{4.21}$$

At this point it is desirable to know how the intermediate nulling point can actually be implemented. There are several different ways of implementing the nulling point to achieve auto-zeroing. We will briefly describe two different ways to realize this.

This first implementation is shown in figure 39 [28]. In this implementation a differential amplifier pair is put in parallel with the input differential pair in the main amplifier.

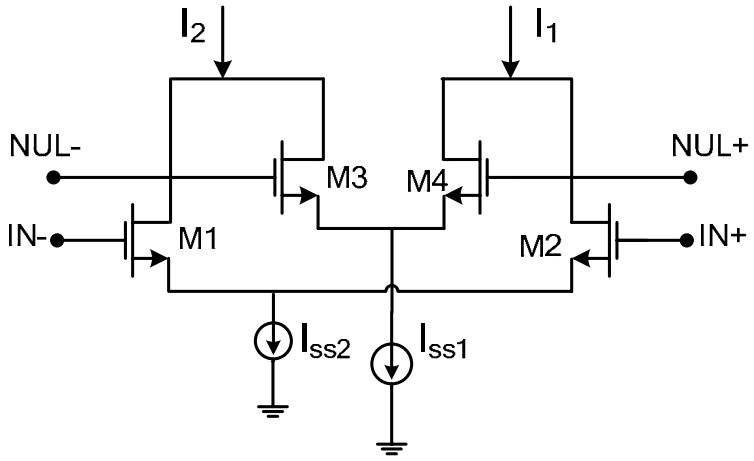


Figure 39: A Simple Realization of a Nulling Point in a Differential Amplifier

The main differential amplifier corresponding to the transconductance g_{m1} is realized using transistors M_1 and M_2. The nulling amplifier stage corresponding to transconductance g_{m2} is realized by adding the differential pair $M_3 - M_4$. In figure 39 in the auto-zeroing phase the inputs of the two differential pairs, $M_1 - M_2$ and $M_3 - M_4$ are connected together and shorted to the common mode voltage. In this case the offset voltage at the input will cause a difference in the output currents I_1 and I_2 of the differential pair. The difference between the two currents can be used

to reduce the input referred offset during the amplification period by applying the appropriate voltage to the inputs of the differential pair $M_3 - M_4$. In other words based on the difference between the currents, the output current of the differential pair $M_3 - M_4$ can be changed in such a way that the two currents I_1 and I_2 at the output branches are equal. In this case the output voltages of the differential pair are ideally equal during the amplification phase. So in the ideal case the input referred offset voltage would be zero.

The circuit shown in figure 39 is actually implemented as shown in figure 40. Here the differential pair $M_1 - M_2$ is the main amplifier and corresponds to g_{m1} in figure 38. The differential pair $M_9 - M_{10}$ corresponds to transconductance g_{m2} in figure 38. The inputs of this differential pair are the nulling points for the main differential amplifier. Capacitors C_1 and C_2 are the hold capacitors in this case. These capacitors are used at the inputs of the nulling differential amplifier $M_9 - M_{10}$ for offset storage. Transistors M_{11} and M_{12} are acting as buffers to isolates the outputs of the main differential amplifier from the hold capacitors C_1 and C_2.

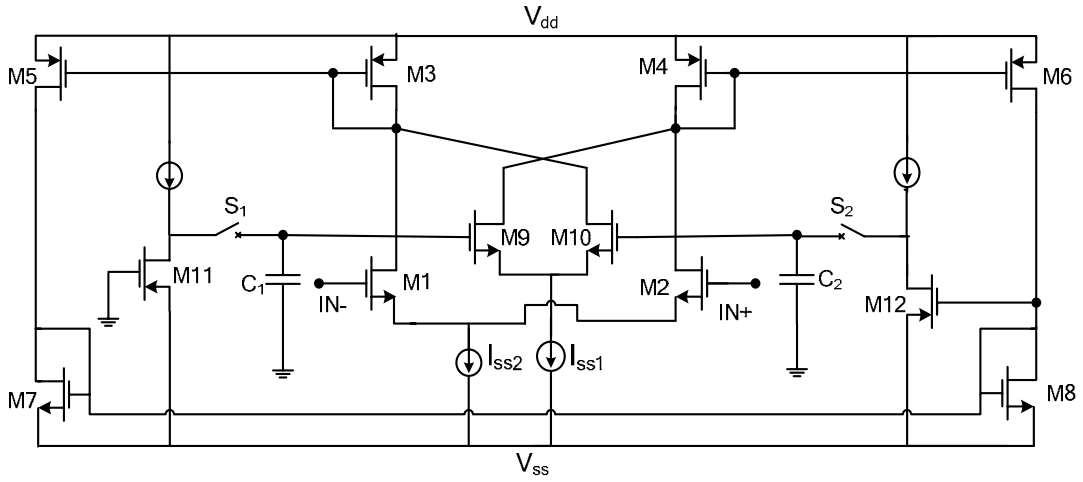


Figure 40: Actual Realization of a Nulling Point in the Differential Amplifier

During the auto-zeroing phase the main amplifier inputs, V_{in+} and V_{in-} are connected to a common mode voltage and switches S_1 and S_2 are closed. During this phase the output voltages of the main amplifier V_{out+} and V_{out-} will be stored on the hold capacitors C_1 and C_2 through the buffer amplifiers M_{11} and M_{12}. During the amplification phase switches S_1 and S_2 are opened and the main amplifier is in the amplification mode. As we know the current at the output stage is equal to the current in the current mirrors M_3 and M_4. The offset voltage at the input of the main amplifier is going to cause the drain currents of M_1 and M_2 to be different. This difference is compensated for by the differential pair $M_9 - M_{10}$. This is due to the fact that the drain currents in M_9 and M_{10} are controlled by the offset voltage stored on capacitors C_1 and C_2. So the difference in the drain currents of M_1 and M_2 are compensated by the opposite difference in the currents of M_9 and M_{10}. Hence the current at the current mirrors M_3 and M_4 would be ideally equal. This would cause the input referred offset voltage to be zero, but this is not the case in practice. When switches S_1 and S_2 are opened for the amplification phase there is an error due to the charge injection voltage stored on the capacitors C_1 and C_2. So the input residual offset is limited by the mismatch between the charge injection voltage errors stored on the hold capacitors.

The second implementation of the auto-zeroing technique using an intermediate nulling point is shown in figure 41. This technique implements the nulling point by using a current mirror shown in figure 42.

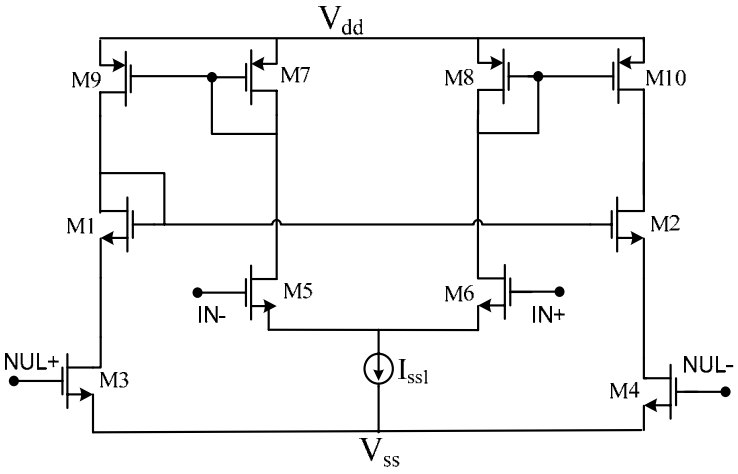


Figure 41: Realizing the Intermediate Nulling Point for Auto-zeroing using a Current Mirror

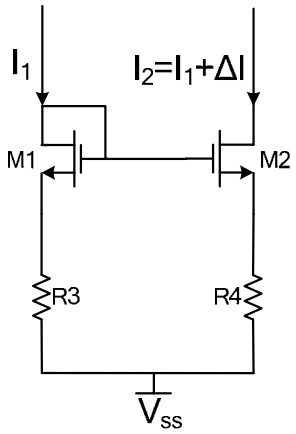


Figure 42: Current Mirror Schematic

Equation (4.22) shows the gain of the current mirror.

$$A = \frac{I_{out}}{I_{in}} \simeq \frac{g_{m2}}{g_{m1}}\left(\frac{1+g_{m1}R_3}{1+g_{m2}R_4}\right) \qquad (4.22)$$

Assuming, $g_{m1}R_3 >> 1$ and $g_{m2}R_4 >> 1$ then equation (4.22) can be simplified to the ratio of the two resistors R_3 and R_4. Resistors R_3 and R_4 can be realized with two transistors biased to operate in the triode region i.e. $V_{gs} - V_{th} >> V_{ds}$. The on resistance for a transistor operating in the triode region is shown in equation (4.23).

$$R = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{gs} - V_{th}\right)} \qquad (4.23)$$

A current mirror with transistors biased in triode region is shown in figure 43.

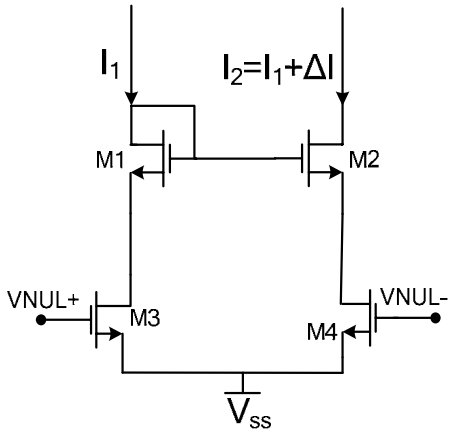


Figure 43: Current Mirror: Load Resistors Replaced with Transistor

Equation (4.23) shows that the resistor is inversely proportional to the input gate source voltage V_{gs}. So by changing the gate source voltage at the transistor input the resistor changes and hence the current in the current mirror will change. By changing the bias voltages V_{nul+} and V_{nul-}, the resistor values can be changed, hence the current mirror gain can be adjusted with this scheme. So any change in the control voltages V_{nul+} and V_{nul-}, changes the output and input currents accordingly. For example if V_{nul+} is higher than V_{nul-} then from equation (4.23) resistor R_4 becomes smaller than resistor R_3. The ratio of the input current to the output current in the current mirror is approximately proportional to the ratio of the resistors, R_3/R_4 as shown in equation (4.22). For a fixed I_{in}, since R_3 is larger than R_4 now, the gain increases and the output current increases by ΔI. The change in the output current I_{out}, ΔI is linearly proportional to the input offset as shown in figure 44.

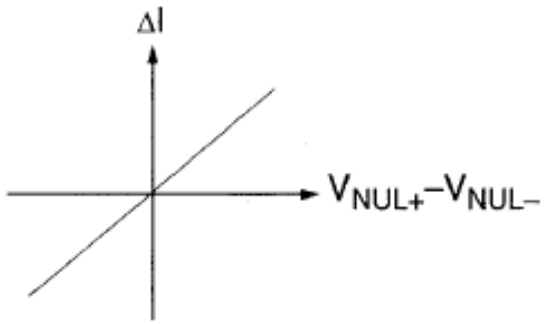


Figure 44: Current Mirror Current Change vs. the Nulling Voltage

The current mirror gain is adjustable and its range depends on resistors R_3 and R_4. Hence, the adjustable gain range depends on the size of the transistors M_3 and M_4. Since the current mirror gain is approximately the ratio of the two resistors, the larger the resistors, the wider the possible gain range. As a result the width and size of transistors M_3 and M_4 should be chosen such that W/L is a small value. By making W/L small, the resistor ranges are increased and hence the adjustable gain range is increased.

In figure 41, transistors M_1 and M_2 form the current mirror and transistors M_3 and M_4 are biased in triode and operate in the linear region acting like two resistors R_3 and R_4. The gates of M_3 and M_4 are the intermediate nulling points in this configuration. Assume switches S_1 and S_2 connect the outputs of the differential amplifier to the nulling points and store the offset voltage on the hold capacitors. During the auto-zeroing phase, the amplifier inputs are shorted together to a common mode voltage and switches S_1 and S_2 are closed. The output voltages of the differential amplifier, V_{out+} and V_{out-} are stored on the hold capacitors C_1 and C_2. The difference between the voltages stored on capacitors C_1 and C_2 represents the

offset voltage. Then S_1 and S_2 are opened and the voltage stored on the capacitors changes the resistances of M_3 and M_4. This changes the current mirror currents and hence the output currents of the main amplifier. So the output current changes proportional to the output offset voltage. The resulting change in the current compensates for the output offset voltage. In the ideal case the output offset voltage and as a result the input referred offset voltage would be zero. But the charge injection error voltages stored on the hold capacitors when switches S_1 and S_2 are opened does not allow this. The residual input referred offset voltage at the differential amplifier input is limited by the charge injection mismatch between the two capacitors. This method has been used in several different applications [29].

4.4.6 Continuous-Time Auto-zeroing Amplifiers

In the techniques mentioned previously the amplifier is disconnected from the signal during the auto-zeroing phase and connected back to the signal path during the amplification phase. This is acceptable for most applications but some applications need continuouse-time amplification. In these applications the amplifier can not be disconnected from the signal path to perform auto-zeroing. One solution for this is to copy the auto-zeroed amplifier and have two amplifiers instead of one. The amplifiers are auto-zeroed in two consecutive cycles so when one is in the auto-zeroing phase, the other is connected to the signal path and provides signal amplification. This technique is called time sharing and sometimes is referred to as the ping-pong technique. The problem with this technique is that switching between

two amplifiers will cause a spike in the output signal. To avoid the spikes the technique illustrated in figure 45 is used [30].

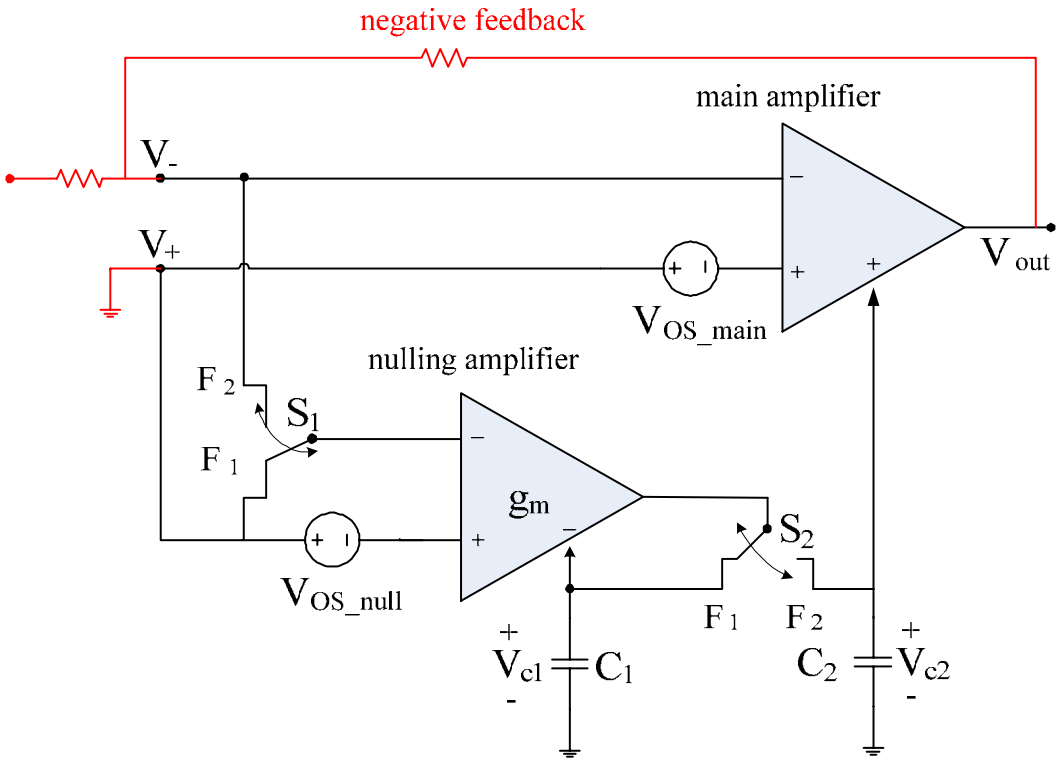


Figure 45: Continuous-Time Auto-zeroing Amplifier

As seen in Figure 45 this technique uses two amplifiers, a main amplifier and a nulling amplifier. The main amplifier is always connected to the signal path and amplifies the signal continuously. The nulling amplifier is a low offset amplifier which is supposed to perform the auto-zeroing and feed the control voltage to the nulling port of the main amplifier. The goal in this technique is for the nulling amplifier to perform auto-zeroing for itself and also produce an output correction voltage to cancel the offset of the main amplifier.

This technique operates in two phases. During phase ϕ_1, the nulling amplifier performs auto-zeroing to cancel its own offset so its inputs are shorted together and

connected to a common mode voltage. In this phase switch S_2 is connected to capacitor C_1 and switch S_1 is connected such that the inputs of the nulling amplifier are shorted together to a common mode voltage which is ground in this case. The output offset for the nulling amplifier is stored on capacitor C_1 and is fed to the nulling input. Ideally this will cancel the offset of the nulling amplifier. The nulling voltage is held on C_1 during phase ϕ_2. As a result the nulling amplifier is almost offset free during phase ϕ_2.

During phase ϕ_2, the nulling amplifier's inputs are connected to the inputs of the main amplifier and switch S_2 is connected to capacitor C_2. Assuming the nulling amplifier is offset free, it will only sense the input offset of the main amplifier and store the nulling voltage on the capacitor C_2. At the end of phase ϕ_2 the nulling voltage necessary for the main amplifier's offset free operation is stored on capacitor C_2 and will remain there during ϕ_1, when the nulling amplifier is auto-zeroed. This technique only works if the main amplifier is used in a negative feedback configuration so that the nulling amplifier can sense the main amplifiers offset during second phase of operation.

Now we will discuss this technique in more detail. As mentioned before, during phase ϕ_1 the nulling amplifier is disconnected from the signal path and is auto-zeroed. The offset correction voltage is stored on capacitor C_1 and applied to the nulling input. Capacitor C_1 is a large off chip capacitor on the order of $100\,nF$. The control voltage stored on capacitor C_1 is given by equation (4.24).

$$V_{C_1} = -\frac{A_n}{1+A_n^{'}} V_{os-null} + \Delta V_{C_1} \cong -\alpha_n V_{os-null} + \Delta V_{C_1} \qquad (4.24)$$

In the equation above, A_n is the gain of the nulling amplifier from its input to its output, $A_n^{'}$ is the gain from the nulling input to the output and $\alpha_n = A_n / A_n^{'}$. ΔV_C is the change in the voltage stored on capacitor C_1 which can be due to charge injection, sampled noise, and leakage current and is shown in equation (4.25).

$$\Delta V_{C_1} = \alpha \frac{C_{ov}}{C_{ov}+C_1} V_{pk-pk} + \frac{q_{inj}}{C_1} + \sqrt{\frac{kT}{C_1}} + \frac{I_{leak} T_h}{C_1} \qquad (4.25)$$

The origins of this formula were discussed in more detail in section 4.4.1. In most practical cases, the second term which is the charge injection term is dominant. For simplicity the other terms will be neglected and it is assumed that the error voltage is only due to charge injection of the switch as given by equation (4.26)

$$\Delta V_{C_1} = \frac{q_{inj}}{C_1} \qquad (4.26)$$

During phase ϕ_2, the negative input of the nulling amplifier is connected to the main amplifier's negative input and switch S_2 is connected to the nulling input of the main amplifier. The voltage at the output of the main amplifier is given by equation (4.27) in which A_m is the gain of the main amplifier from the input to the output, V_{os_main} is the offset voltage of the main amplifier, $A_m^{'}$ is the gain of the main amplifier from the nulling input to the output, and V_{C_2} is the nulling voltage stored on the capacitor C_2.

$$V_{out} = A_m \left(V_+ - V_- - V_{os\_main} \right) + A_m^{'} V_{C_2} \qquad (4.27)$$

V_{C_2} is the correction voltage stored by the nulling amplifier on capacitor C_2 to autozero the main amplifier. This voltage is derived as follows.

$$V_{C_2} = A_n\left(V_+ - V_- - V_{os\_null}\right) - A_n^{'}V_{C_1} \qquad (4.28)$$

In the equation above A_n is the gain from the nulling amplifier input to the output, $A_n^{'}$ is the gain of the nulling amplifier from its nulling input to the output, and V_{os_null} is the nulling amplifier offset. Replacing V_{C_1} from equation (4.24) and after simplification assuming $A_n^{'}$>>1, V_{C_2} is shown in equation (4.29).

$$V_{C_2} = A_n\left(V_+ - V_-\right) - \alpha_n V_{os\_null} - A_n^{'}\Delta V_{C_1} \qquad (4.29)$$

At this point, it is desirable to derive the relationship for the residual input referred offset, $V_{os(\phi_2)}$ during phase ϕ_2. In order to do this we are going to assume the ideal case first. In the ideal case the input residual offset voltage would be the input offset voltage that would make the output offset zero. By setting V_{out} to zero, replacing $V_+ - V_-$ by $V_{os}\left(\phi_2\right)$ and substituting V_{C_2} from equation (4.29) into equation (4.27) we have the following:

$$V_{os(\phi_2)} \cong \frac{\alpha_m V_{os\_main} + \alpha_n V_{os\_null}}{A_n} + \frac{\Delta V_{C_1}}{\alpha_n} \qquad (4.30)$$

In equation (4.30) it is assumed that the gain $A_n A_m^{'}$ from the input through the nulling amplifier and from the nulling input of the main amplifier to the output is much larger than the gain of the main amplifier A_m.

At the end of phase ϕ_2 switch S_2 is opened and the error due to charge injection, sampled noise and leakage current is stored on capacitor C_2. Assuming the

nulling voltage stored on the capacitor is changed by ΔV_{C_2}, the output voltage of the amplifier will change by $\Delta V_{out} = A_m^{'} \Delta V_{C_2}$. $V_{os(\phi_1)}$, the input referred offset voltage during phase ϕ_1 will be reduced by this change in the output voltage. Converting this change in the output voltage to the input of the main amplifier, will give $\Delta V_{out} / A_m = A_m^{'} \Delta V_{C_2} / A_m = \Delta V_{C_2} / \alpha_m$. This shows that the input referred offset voltage during phase ϕ_1 should be reduced by this amount in order for the output voltage to stay zero. So the input referred offset is given by equation (4.31).

$$V_{os(\phi_1)} = V_{os(\phi_2)} - \frac{\Delta V_{C_2}}{\alpha_m}$$

$$V_{os(\phi_1)} \cong \frac{\alpha_m V_{os\_main} + \alpha_n V_{os\_null}}{A_n} + \frac{\Delta V_{C_1}}{\alpha_n} - \frac{\Delta V_{C_2}}{\alpha_m} \qquad (4.31)$$

By comparing (4.30) with (4.31), it can be seen that residual input referred offset voltage for phase ϕ_1 is a little different from that of phase ϕ_2 due to the charge injection of switch S_2. As can be seen from equation (4.31) when $\alpha_n = \alpha_m = 1$, the residual input referred offset is the sum of the main and nulling amplifier offsets divided by the nulling amplifier gain plus the charge injection terms. The charge injection terms can be reduced by decreasing the gain from the nulling input to the output, causing α_m and α_n to be greater than one. These terms can also be reduced by using differential amplifiers. This will reduce the error to the mismatch between the charge injections.

4.5 A Novel Auto-zeroing Technique Using Emitter Degeneration

In this section, a novel auto-zeroing technique is proposed. This technique uses a nulling point other than the amplifier's input and output to perform the auto-zeroing operation. The auto-zeroing is performed by taking advantage of emitter degeneration in the input transistor pair of the differential amplifier to cancel the offset at the output. So in order to perform the auto-zeroing operation two emitter degeneration resistors are added to the input transistors. MOS transistors biased in triode region are used as resistors.

Many techniques have been proposed for offset cancellation in the past but none of them have used the emitter degeneration resistor based approach to cancel the offset voltage. By using emitter degeneration to cancel the offset, this technique increases the linearity of the amplifier which is very important in these circuits.

Some other techniques achieve offset cancellation by correcting the offset at the input nodes of the amplifier, which are moving nodes of the circuit. In this method, the offset cancellation is done by correcting the output nodes in the circuit, which are stationary nodes. The output voltage is fed back to the emitter degenerated resistors and, based on the voltage, the current in each branch of the circuit is changed such that the output offset is canceled.

This technique is discussed in more detail in the next section.

4.5.1 Description

As described before, the offset cancellation technique uses emitter degeneration resistors to cancel the offset. MOSFET transistors biased to operate in the triode region are used as resistors. Here, we have applied this technique to a telescopic cascode amplifier which is shown in figure 46.

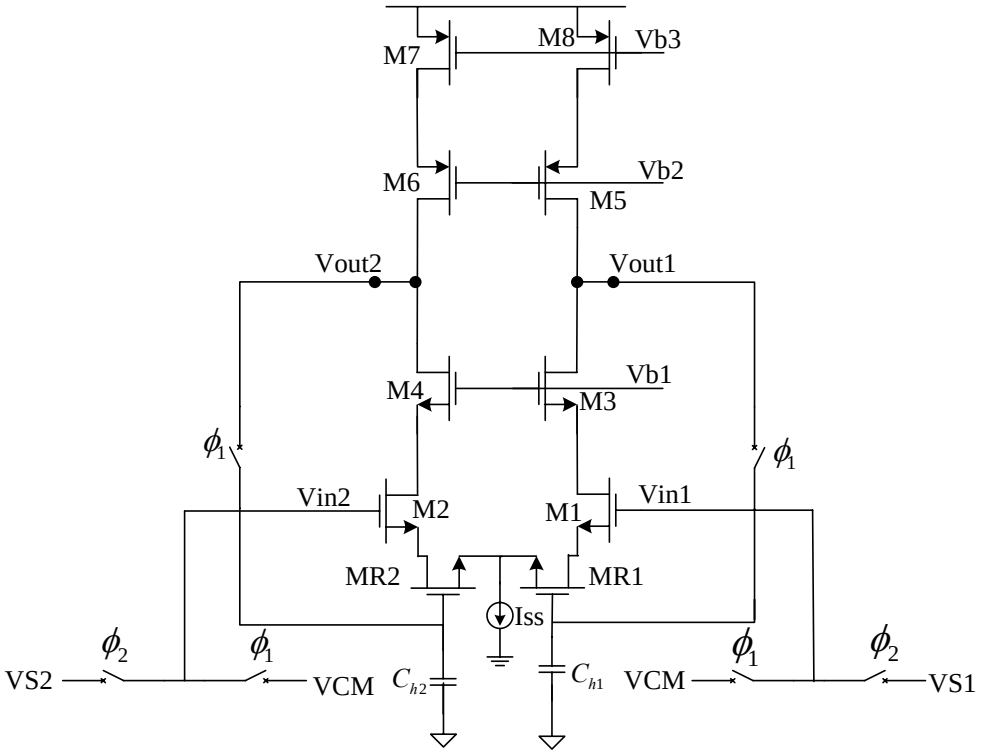


Figure 46: Auto-zeroing Technique using Emitter Degenerated Resistors for Offset Cancellation

As can be seen in figure 46 two MOS transistors biased in the triode region are used for the emitter degeneration. Two 10 *pf* hold capacitors are used at the gate of the MOS transistors to store the nulling voltage for use during the amplification phase. The MOS transistors biased in the triode region follow the relationship shown in equation (4.32).

$$R = \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{gs} - V_{th}\right)} \qquad (4.32)$$

As can be seen from equation (4.32), the resistor is inversely proportional to the gate source voltage of the MOS transistor. As a result when the gate source voltage of the MOSFET changes, it causes the resistor to change linearly.

The offset cancellation takes place in two phases. During the first phase ϕ_1, the amplifier is auto-zeroed. Then the amplifier is ready for amplification during phase ϕ_2. In the auto-zeroing phase, ϕ_1 the inputs are shorted together and connected to a common mode input voltage. In this case the output voltage is the input offset voltage multiplied by the gain of the amplifier, $V_{out} = AV_{os}$. This output voltage is fed back to the gate terminals of the MOS transistors acting as the emitter degeneration resistors and stored on the hold capacitors. If one output voltage is higher than the other, then the gate source voltage of the respective MOS transistor will be larger than the other and the resistor on that side is reduced compared to the other. In this case more current is drawn in the branch with the smaller emitter degeneration resistor, so the output voltage on that branch is reduced compared to the output voltage of the other branch. The exact opposite occurs in the other branch so the output voltage in the other branch is slightly increased. This causes the current in the two branches of the circuit to change in proportion to the difference between the outputs and the offset voltage is thus cancelled.

If the switches were ideal, then the difference between the output voltages of the amplifier would be zero and hence the input referred offset voltage would be zero as well. But when the switches open, the charge injection error voltage is stored on

the hold capacitor. This error voltage is equal to q_{inj}/C_h. Since the telescopic cascode amplifier has a differential architecture, the output offset voltage is limited by the mismatch between the two charge injection mismatches. The charge injection term is multiplied by the gain from the nulling input to the output of the amplifier and divided by the amplifier gain. The ratio of the gain from the nulling input to the output of the amplifier, to the amplifier gain is less than one. Hence, the input residual offset voltage would be the mismatch between the charge injection voltages stored on the hold capacitors reduced by a factor that is less than one.

In the next phase, ϕ_2, the amplifier is ready for amplification. The nulling offset is stored on the hold capacitors during ϕ_2 and the inputs of the amplifier are connected to the signal. The auto-zeroing telescopic differential amplifier is designed in $0.13\mu m$ IBM CMOS8RF process technology using Cadence Spectre. In the following sections the simulation and experimental results for the auto-zeroing telescopic cascode amplifier are discussed.

4.5.2 Simulation Results

The auto-zeroing circuit is designed in $0.13\ \mu m$ CMOS8RF IBM process using Cadence Spectre. For means of comparison, a telescopic cascode differential amplifier without the auto-zeroing technique was designed in a $0.13\ \mu m$ CMOS8RF IBM process as well. The simulation results for the two telescopic amplifiers are compared together and the advantage of the proposed auto-zeroing technique is shown by comparison.

The telescopic cascode designed for this purpose is shown in figure 47. The transistor parameters for this amplifier are shown in table 1. Figure 48 and 49 show the gain and phase response of the telescopic amplifier vs. frequency. The amplifier has an open loop gain of $45\,dB$ and a unity gain bandwidth of above $1\,GHz$. The $3\,dB$ bandwidth is approximately $10\,MHz$. As can be seen from the phase response in figure 49, the phase margin is more than 65 degrees which makes this a very stable amplifier.

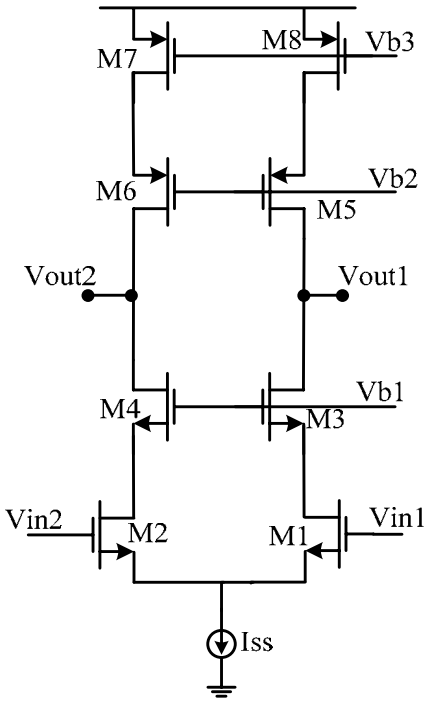


Figure 47: Differential Telescopic Cascode Amplifier Without the Auto-zeroing Technique

Transistor	**Size** (W/L)
M_1, M_2	25/1
M_3, M_4	25/1
M_5, M_6	25/1
M_7, M_8	30/1
M_9	50/1

Table 1: Transistor Parameters for the Differential Telescopic Cascode Amplifier in Figure 47

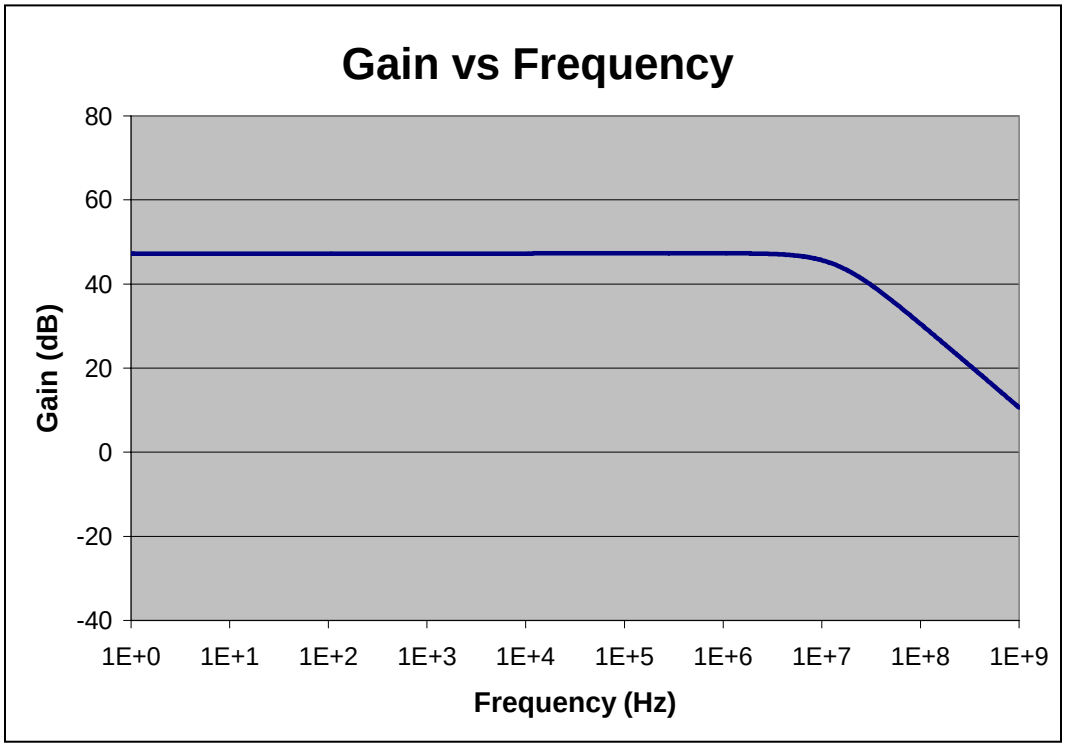


Figure 48: Gain vs. Frequency for the Telescopic Cascode Amplifier in Figure 47

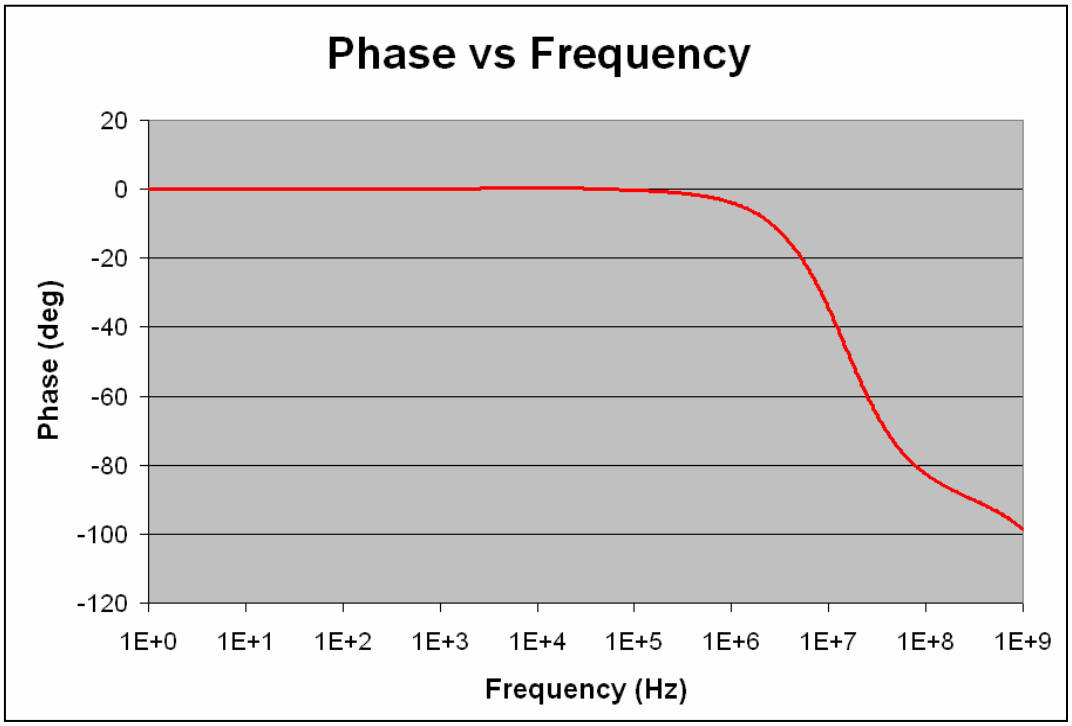


Figure 49: Phase vs. Frequency for the Telescopic Cascode Amplifier in Figure 47

Figure 50 shows the differential DC output voltages at nodes V_{out1} and V_{out2} of the open loop telescopic cascode amplifier. The difference between these voltages is the output offset voltage and it is approximately equal to $323\,mV$. This can also be seen in figure 51.

As seen from the frequency response of the amplifier in figure 48, the telescopic cascode amplifier has a DC gain of $45\,dB$. This translates to $177\,V/V$. The input referred offset is the output offset voltage divided by the gain of the amplifier. Hence, the input referred offset voltage at the input of the open loop telescopic cascode amplifier is $1.824\,mV$.

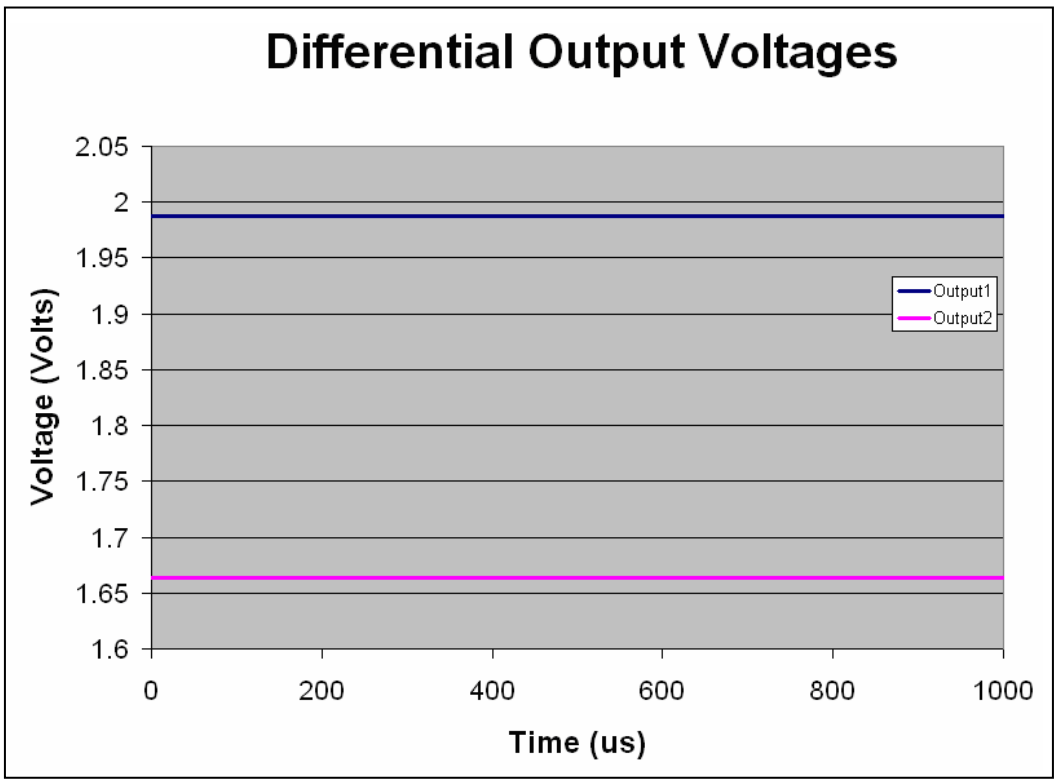


Figure 50: Simulated Differential DC Output Voltages of the Telescopic Cascode Amplifier

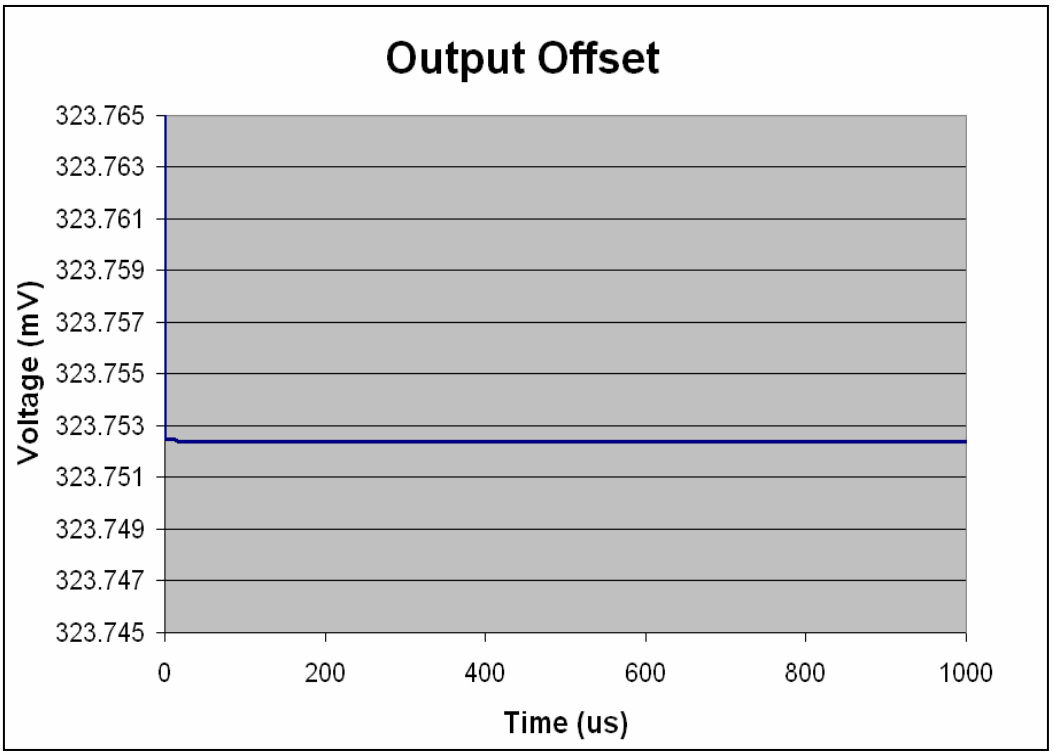


Figure 51: Simulated Output Offset Voltage for the Telescopic Cascode Differential Amplifier

At this point we will apply the emitter degeneration auto-zeroing technique to the differential telescopic amplifier shown in figure 47. This is shown in figure 52. The transistor parameters for this differential amplifier are shown in table 2. The two transistors in the source of the input transistors, MR_1 and MR_2 are biased in the triode region and are acting as emitter degeneration resistors. The rest of the transistors are biased to operate in the saturation region. As described before, during phase ϕ_1 in which the clock is high, the outputs are connected to the emitter degeneration resistors and the nulling voltages are stored on the hold capacitors C_{h1} and C_{h2}. This voltage is the gate voltage controlling the two transistors MR_1 and MR_2. The change in these resistors is inversely proportional to the change in gate voltages stored on the hold capacitors. So the current in the output branches of the differential telescopic cascode amplifier is changed such that the two output voltages are ideally equal. As mentioned before, due to non-ideal effects such as the charge injection of the switches and sampled noise on the hold capacitors, the output offset voltage will be not be zero but it will be reduced.

The gain and phase response of the auto-zeroed telescopic amplifier is shown in figures 53 and 54 respectively. As can be seen in figure 53, the amplifier has a gain of $55\,dB$ and a $3\,dB$ bandwidth of approximately $5\,MHz$. Figure 54 shows that the phase margin is 60 degrees for the unity gain bandwidth of $1\,GHz$, so the amplifier is stable.

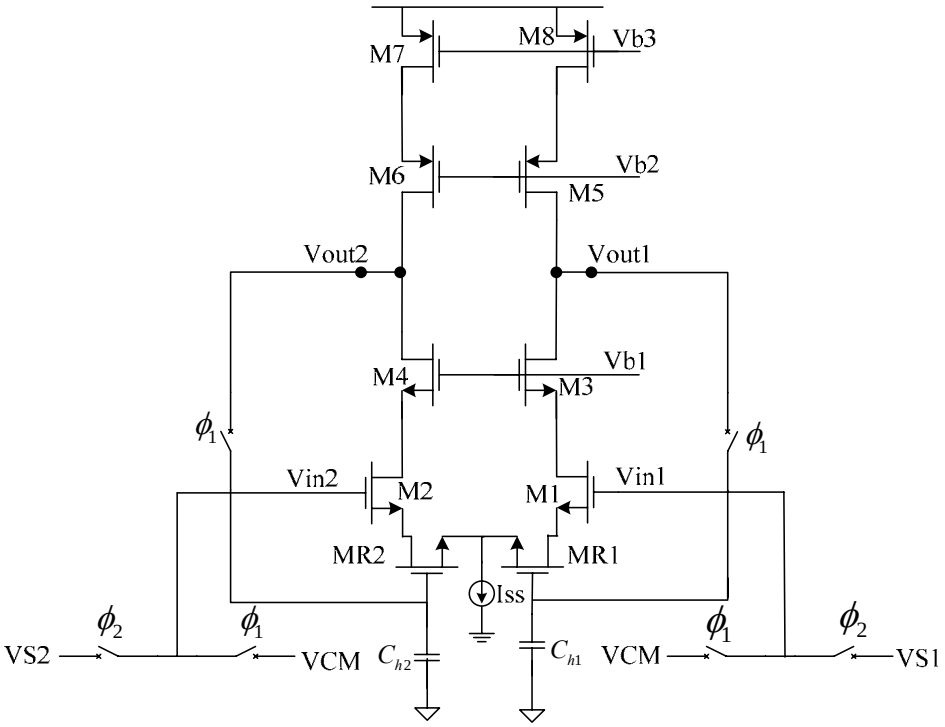


Figure 52: Telescopic Cascode Amplifier with the Emitter Degeneration Auto-zeroing Technique

Transistor	**Size** (W/L)
M_1, M_2	25/1
M_3, M_4	25/1
M_5, M_6	25/1
M_7, M_8	30/1
M_9	50/1
MR_1, MR_2	220/1
M_{Nsw}	2/1
M_{Psw}	4/1

Table 2: Transistor Parameters for the Auto-zeroed Differential Telescopic Cascode Amplifier in Figure 52

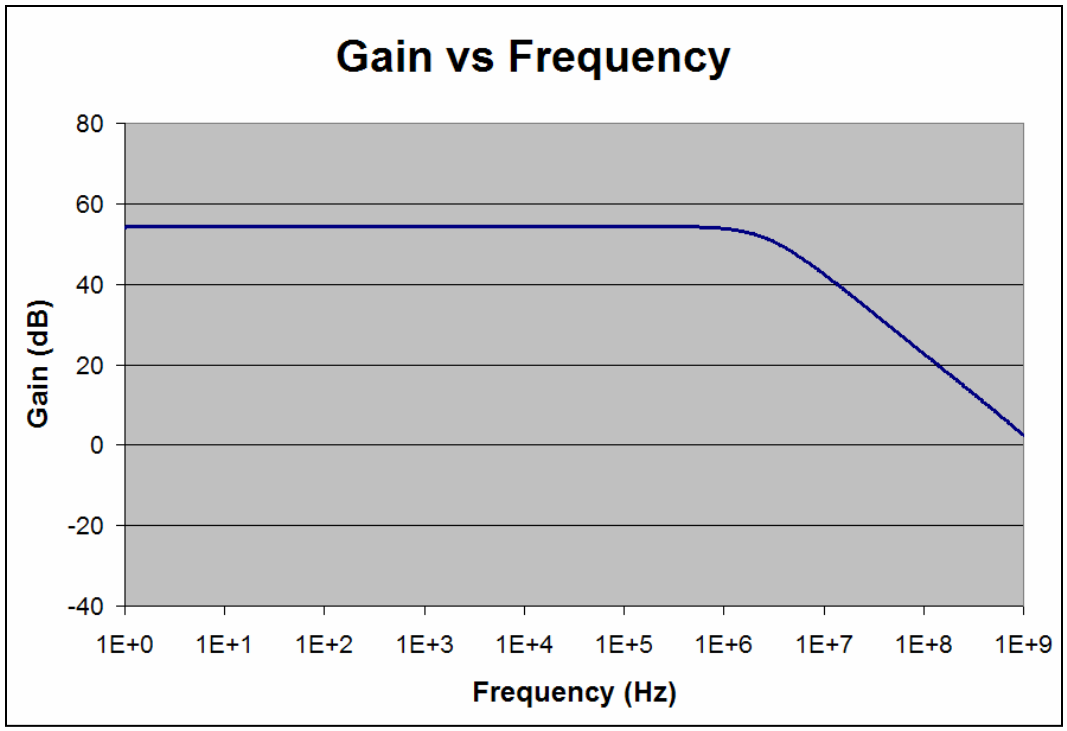


Figure 53: Gain vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier

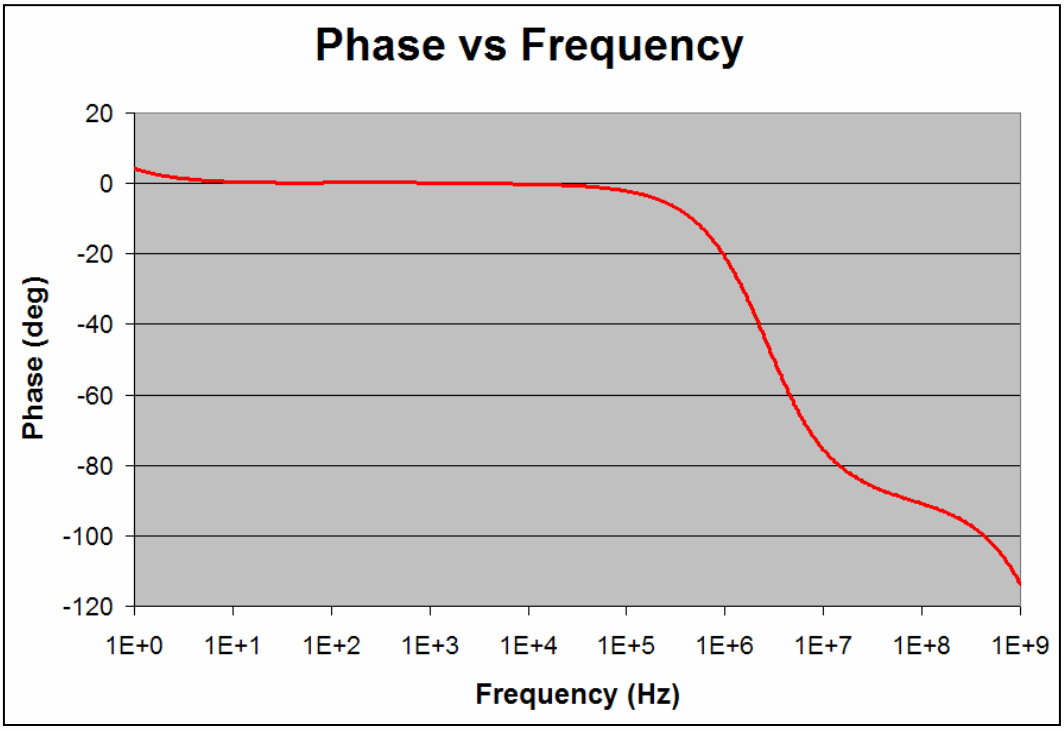


Figure 54: Phase vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier

The open loop output offset voltage for the auto-zeroed telescopic amplifier is $118\,mV$. The output offset voltage is shown along with the clock signal in figure 55. This offset voltage is referred to the amplifier's input by dividing it by the gain. Hence, the input referred offset voltage for the auto-zeroed telescopic amplifier is approximately $200\,\mu V$. The input referred offset voltage is approximately an order of magnitude less than the case where the auto-zeroing technique was not incorporated in the telescopic cascode differential amplifier.

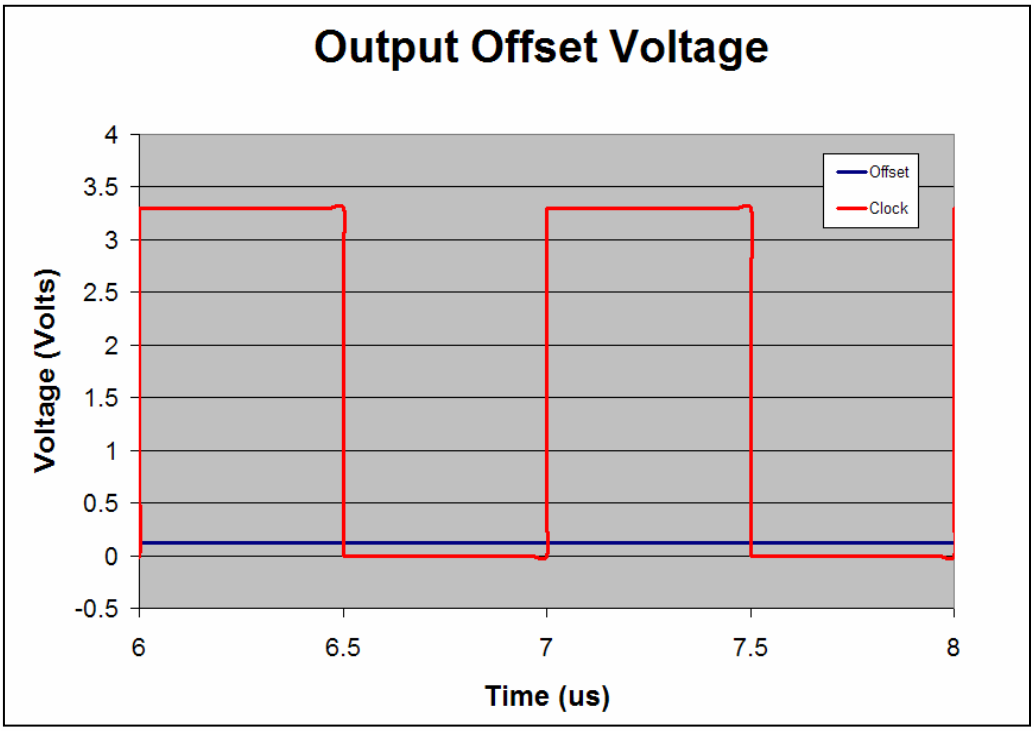


Figure 55: Simulated Output Offset Voltage and Clock Signal for the Auto-zeroed Telescopic Cascode Differential Amplifier Shown in Figure 52

Next the auto-zeroed telescopic cascode differential amplifier is used in a feedback configuration. In order to achieve a closed loop gain of $10\,V/V$, different feedback resistor configurations are used. Gain vs. frequency for a closed loop gain of $10\,V/V$ is shown in figure 56. The unity gain bandwidth is approximately $1\,MHz$.

The phase response vs. frequency is depicted in figure 57. The phase margin is 90 degrees so the amplifier is stable. Figures 58 and 59 show the output offset voltages along with the clock signal for the feedback configurations of $10\,k\Omega/100\,k\Omega$ and $1\,M\Omega/10\,M\Omega$ respectively. As can be seen in figure 58, the output offset voltage for the $10\,k\Omega/100\,k\Omega$ feedback resistor combination is $2.3\,mV$. This voltage is referred to the amplifier input by dividing it with the amplifier gain. The input referred offset voltage is $230\,\mu V$. Figure 58 shows the output offset voltage for the feedback resistor combination of $1\,M\Omega/10\,M\Omega$. This voltage is $3\,mV$. This voltage is referred to the amplifier input by dividing it with the amplifier gain. The input referred offset voltage is $300\,\mu V$. The input referred offset voltage is around 200 to $300\,\mu V$, which is approximately an order of magnitude improvement compared to the telescopic cascode differential amplifier without the auto-zeroing technique.

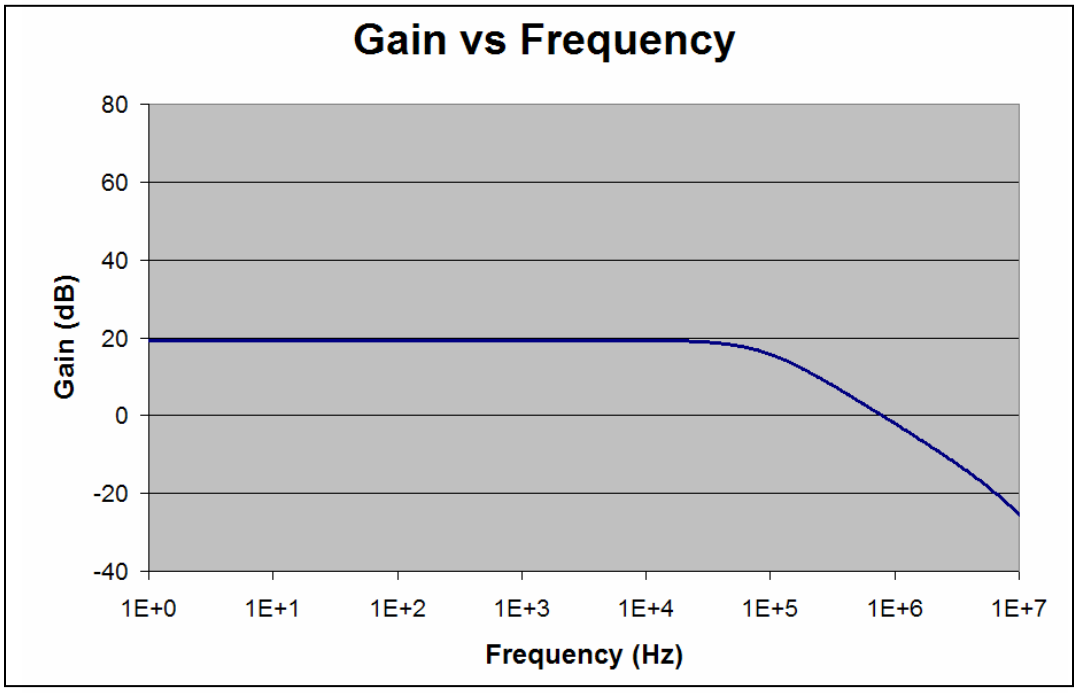


Figure 56: Gain vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Closed Loop Gain of 10V/V

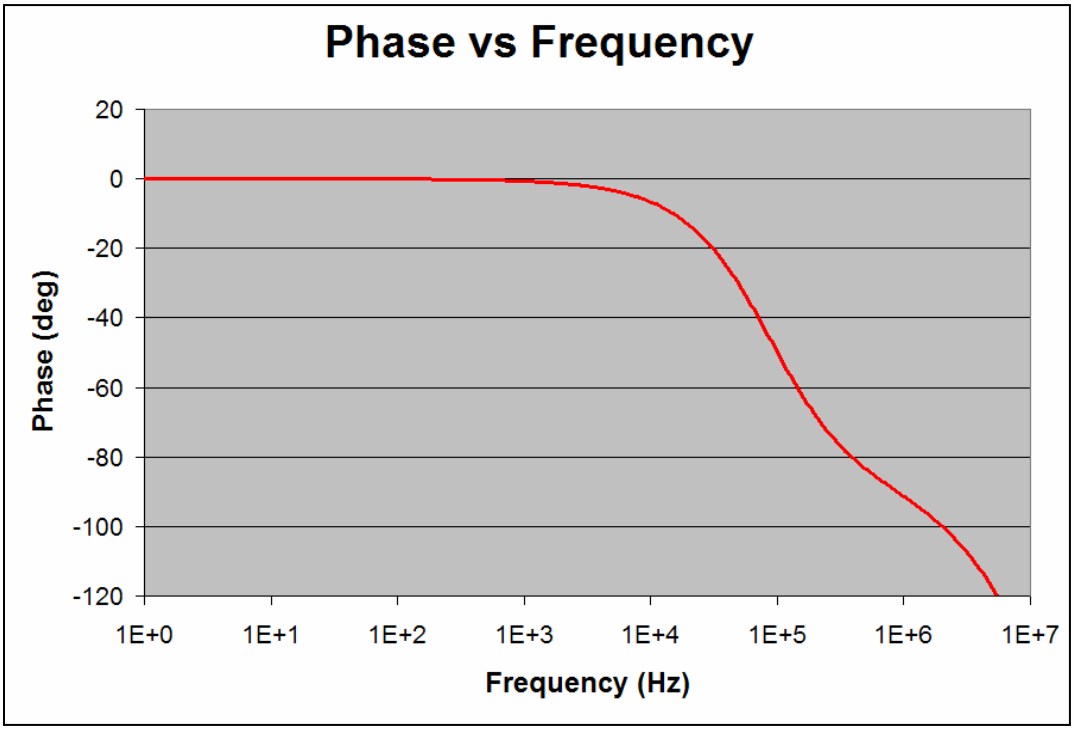


Figure 57: Phase vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Closed Loop Gain of 10V/V

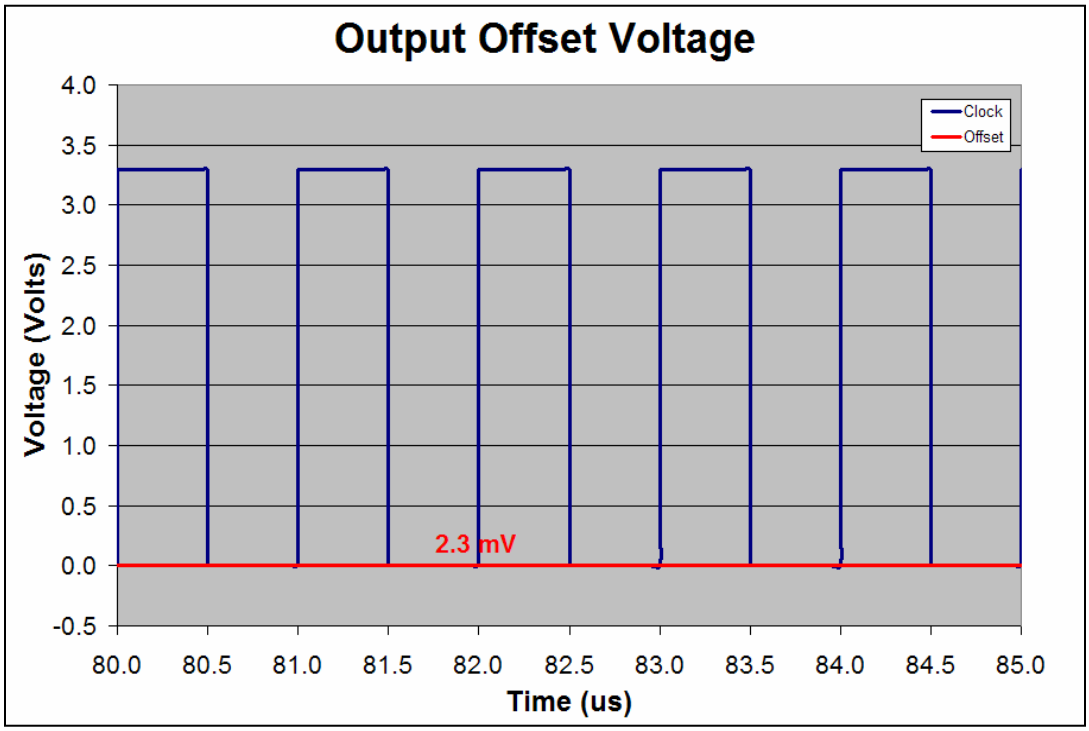


Figure 58: Simulated Output Offset Voltage for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Feedback Configuration of 10k/100k

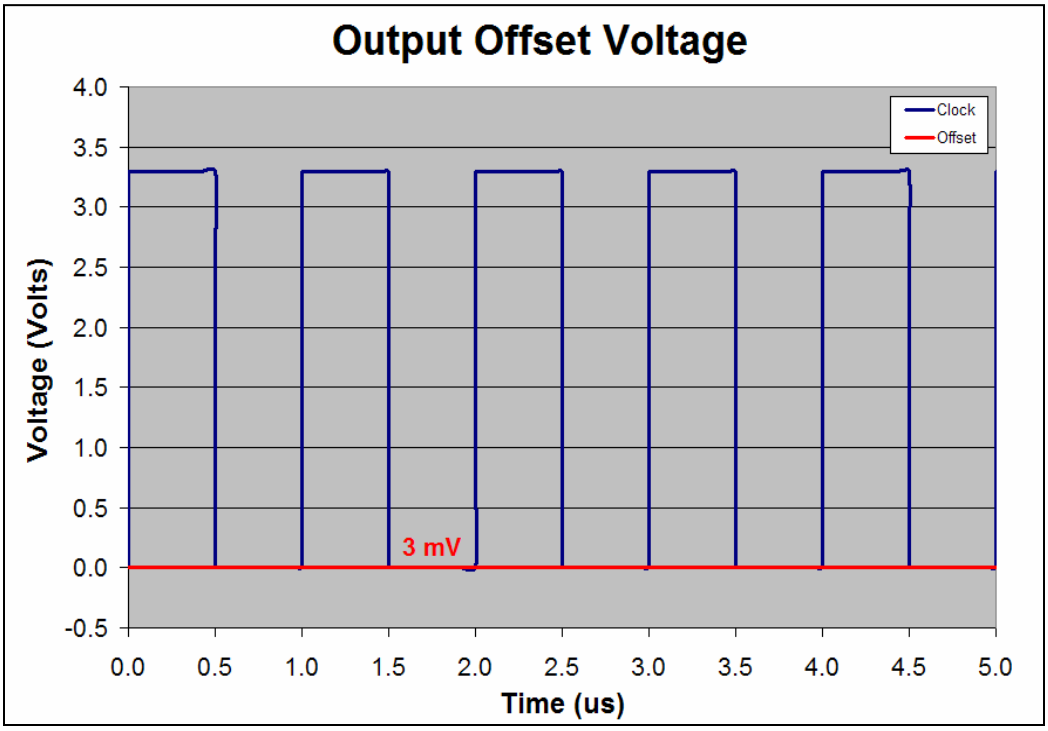


Figure 59: Simulated Output Offset Voltage for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Feedback Configuration of 1M/10M

Next the telescopic cascode amplifier is used in a feedback configuration with a closed loop gain of $100\,V/V$. In order to achieve a closed loop gain of $100\,V/V$, different feedback resistor configurations are used. Gain vs. frequency for a closed loop gain of $100\,V/V$ is shown in figure 60. The unity gain bandwidth is approximately $10\,MHz$. The phase response vs. frequency is depicted in figure 61. The phase margin is 90 degrees so the amplifier is stable.

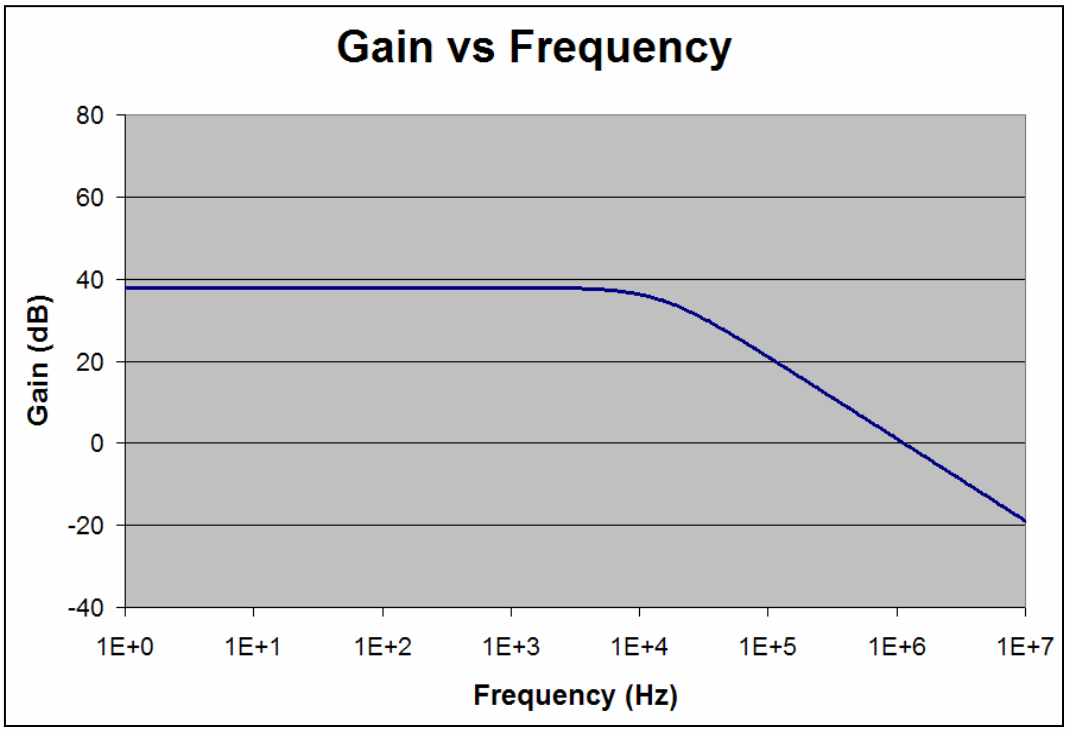


Figure 60: Gain vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Closed Loop Gain of 100V/V

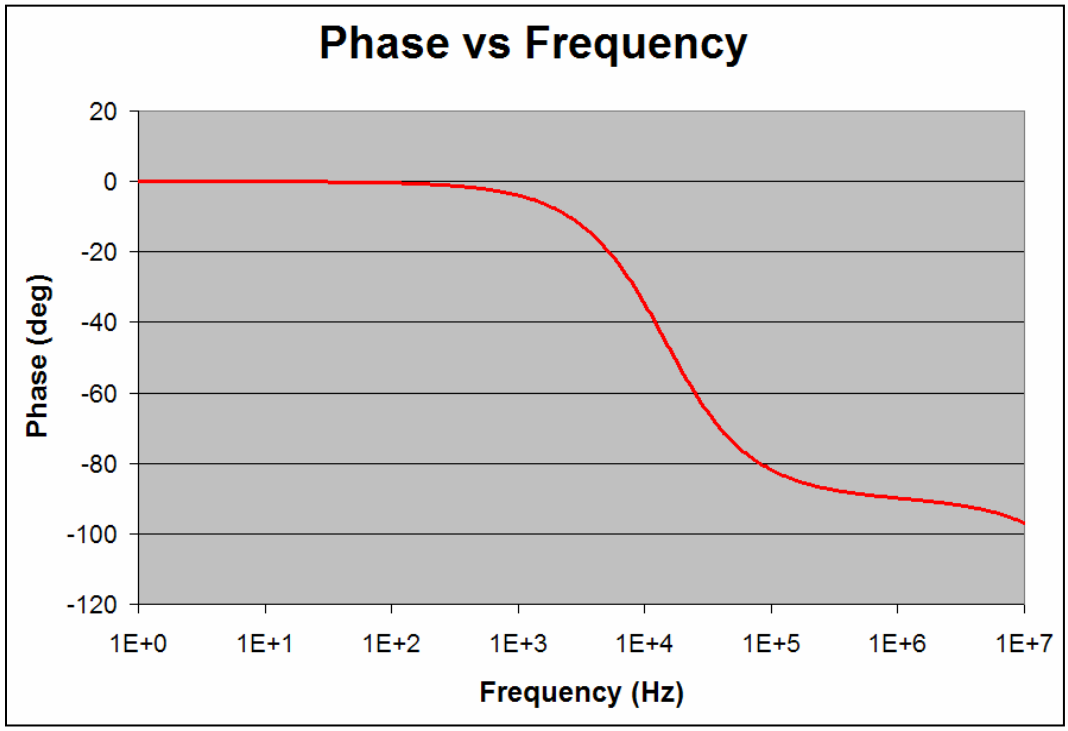


Figure 61: Phase vs. Frequency for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Closed Loop Gain of 100V/V

Figures 62 and 63 show the output offset voltages along with the clock signal for the feedback configurations of $10\,k\Omega/1\,M\Omega$ and $100\,k\Omega/10\,M\Omega$ respectively. As can be seen in figure 62, the output offset voltage for the $10\,k\Omega/1\,M\Omega$ feedback resistor combination is $28.2\,mV$. This voltage is referred to the amplifier input by dividing it with the amplifier gain. As a result the input referred offset voltage is $282\,\mu V$. Figure 63 shows the output offset voltage for the feedback resistor combination of $100\,k\Omega/10\,M\Omega$. This voltage is $33.7\,mV$. This voltage is referred to the amplifier input by dividing it with the amplifier gain. Hence, the input referred offset voltage is $337\,\mu V$.

The simulation results show that the auto-zeroing technique reduces the output offset and hence the input referred offset of the telescopic cascode amplifier by approximately an order of magnitude. The input referred offset voltage is typically between 200 to 300 μV for different feedback configurations and different gains.

The telescopic cascode amplifier and the auto-zeroed telescopic cascode amplifier are both layed out and fabricated in $0.13\,\mu m$ CMOS8RF IBM process technology. Verification tests have been done on both chips. In the next section the test results are discussed and compared together for these two amplifiers.

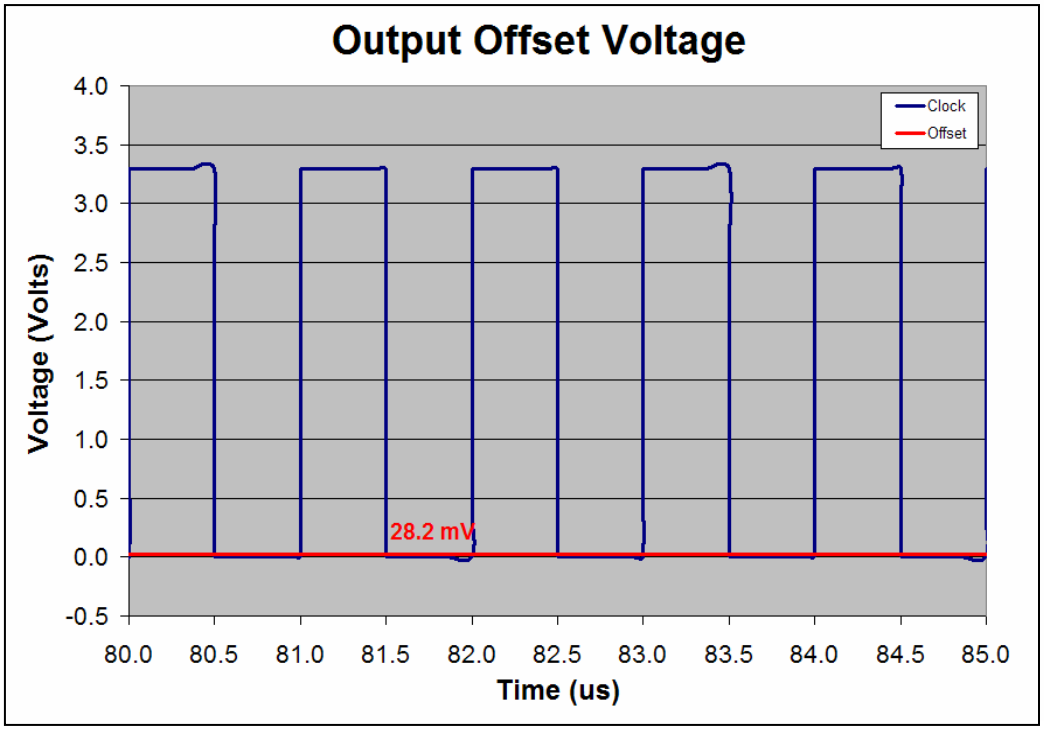


Figure 62: Simulated Output Offset Voltage for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Feedback Configuration of 10k/1M

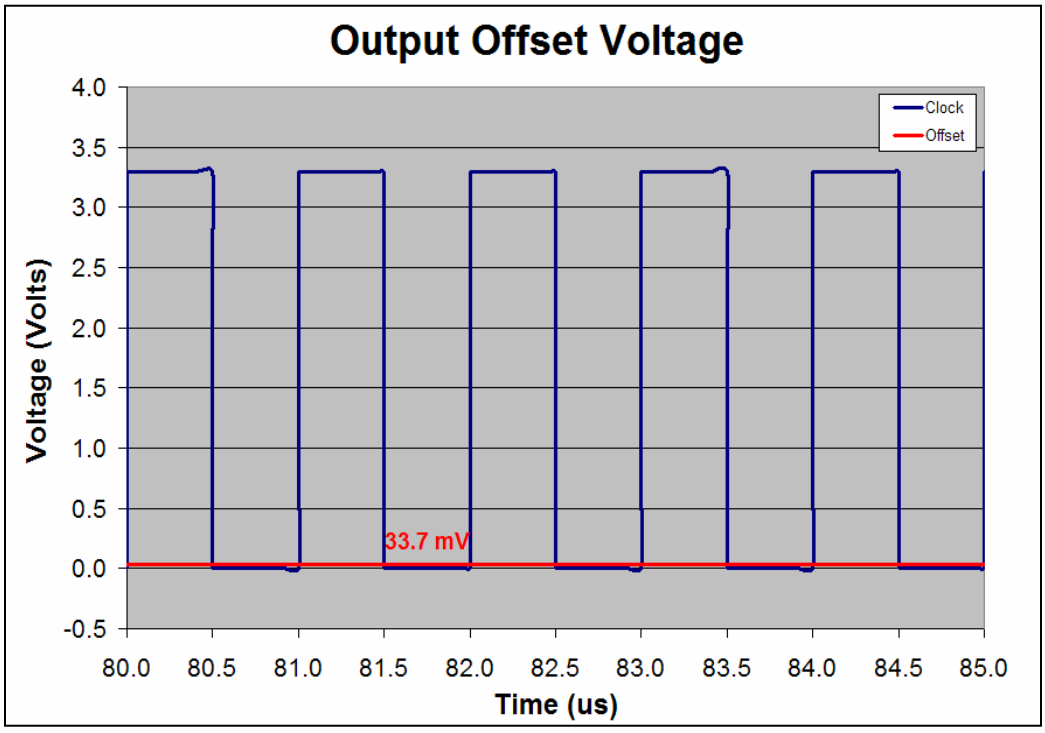


Figure 63: Simulated Output Offset Voltage for the Auto-zeroed Telescopic Cascode Differential Amplifier with a Feedback Configuration of 100k/10M

4.5.3 Experimental Results

In this section we will analyze the results obtained from testing the corresponding chips for the telescopic cascode differential amplifier and the auto-zeroed telescopic cascode differential amplifier.

Both amplifiers are design in 0.13 μm CMOS8RF IBM process and layed out using Cadence. The design verification process including design rule check (DRC), layout vs. schematic (LVS) and extraction is done using Cadence Assura package. The design is then taped out for fabrication.

In section 4.5.3.1, the experimental results for the frequency response, output offset voltage and input referred offset voltage for the telescopic amplifier are discussed. Section 4.5.3.2 shows the frequency response, output offset voltage, and input referred offset voltage for the auto-zeroed telescopic amplifier. The results are then compared together in section 4.5.3.3.

4.5.3.1 Telescopic Cascode Differential Amplifier

The telescopic cascode differential amplifier is designed and layed out in 0.13 μm CMOS8RF using Cadence. Figure 64 shows the chip layout of the telescopic amplifier. The enhanced view of the telescopic cascode amplifier layout is depicted in figure 65. A picture of the chip is shown in figure 66.

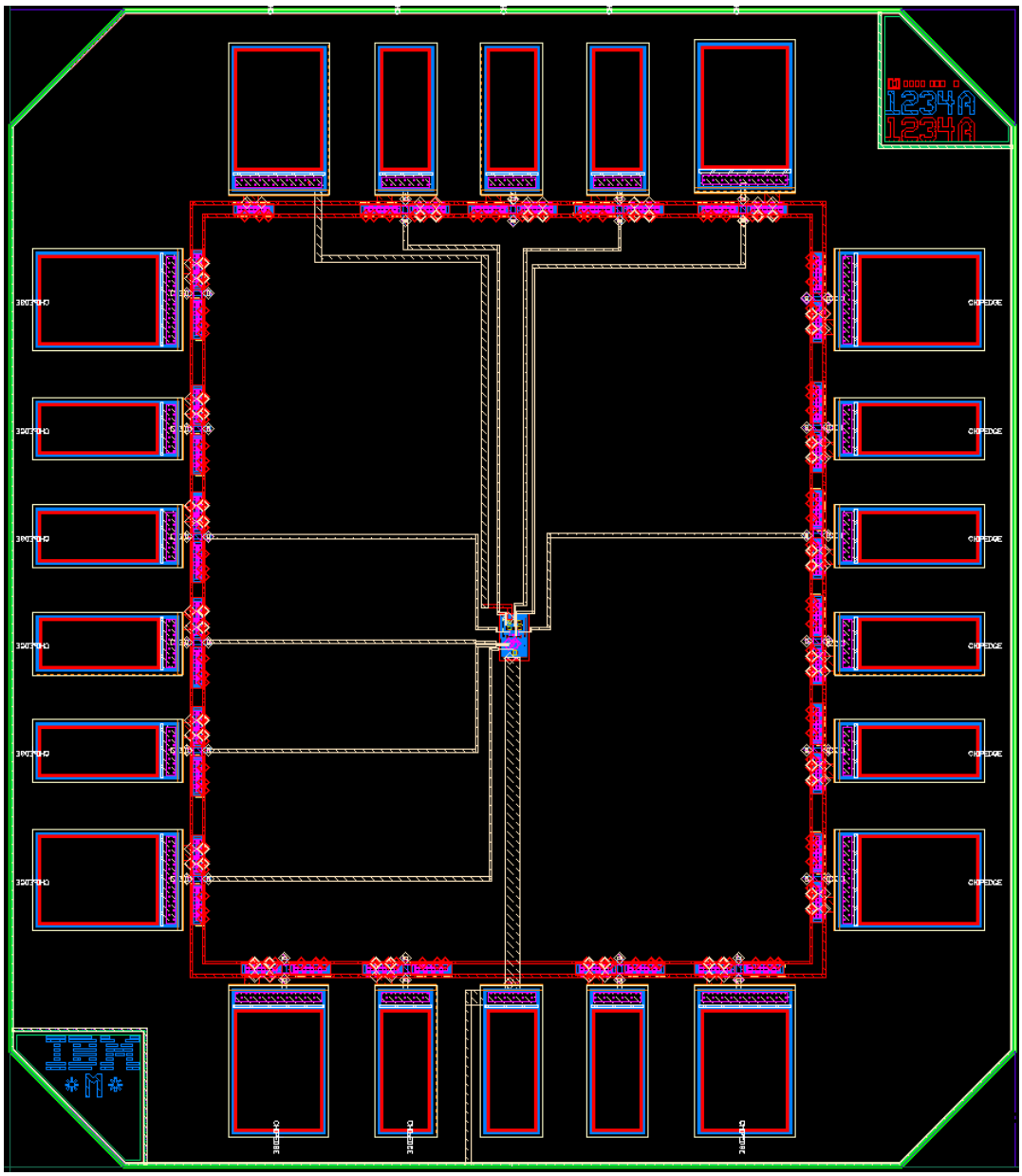


Figure 64: The Chip Layout for the Telescopic Cascode Differential Amplifier Shown in Figure 47

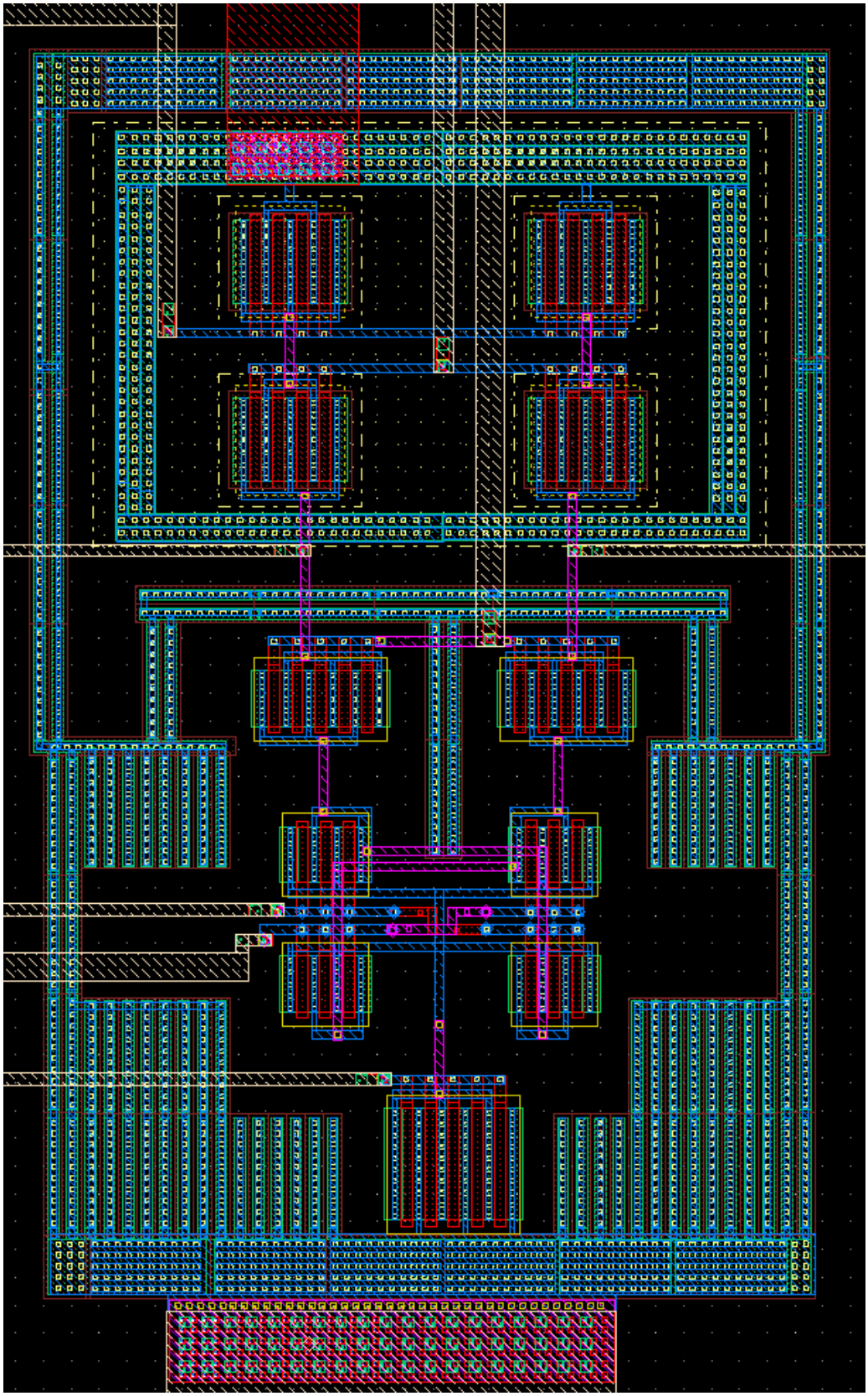


Figure 65: The Telescopic Cascode Differential Amplifier Layout

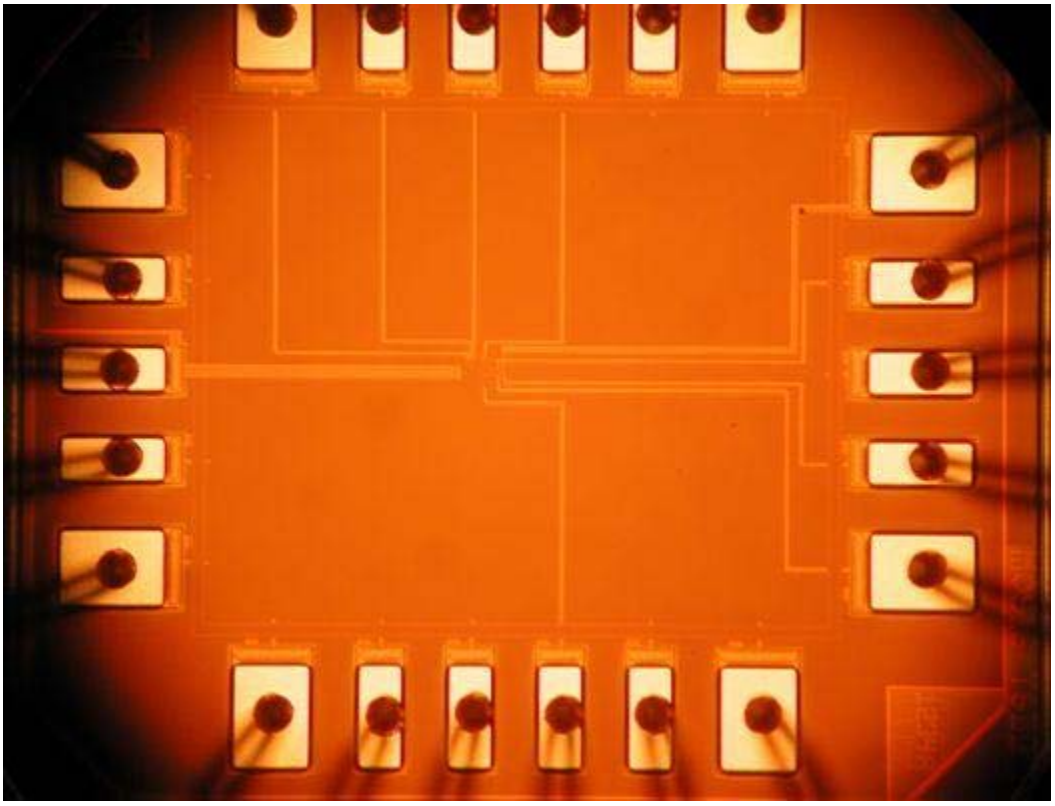


Figure 66: Telescopic Cascode Differential Amplifier Chip

In order to test the telescopic cascode amplifier chip, the amplifier is used in different feedback loop configurations. First the telescopic cascode differential amplifier is setup with a closed loop gain of $10\,V/V$ using a $10\,K\Omega/100\,K\Omega$ feedback resistor combination. This setup is shown in figure 67. The transient input and output voltages are shown in figure 68. From this figure, the actual measured gain is $9.14\,V/V$.

The measured average output offset voltage for the telescopic cascode differential amplifier used in this feedback configuration is $30.8\,mV$. This voltage is referred to the amplifier input by dividing it with the gain of $9.14\,V/V$. This means that the input referred offset voltage at the amplifier input is $3.37\,mV$.

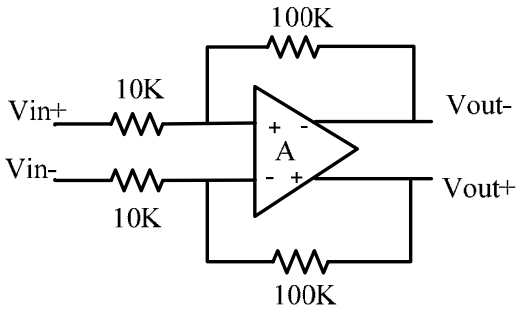


Figure 67: Telescopic Cascode Differential Amplifier shown in a Feedback Configuration with a Closed Loop Gain of 10V/V

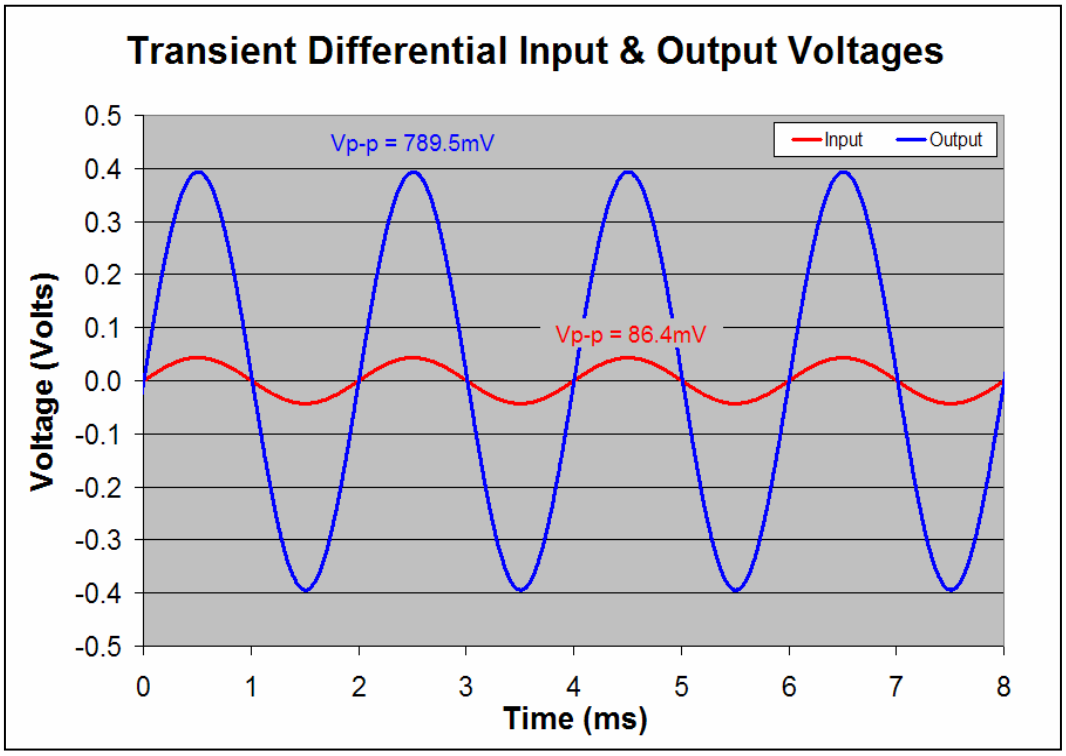


Figure 68: Experimental Transient Input and Output Waveforms for the Telescopic Cascode Differential Amplifier with a 10k/100k Feedback Resistor Configuration

Next the amplifier is setup with a closed loop gain of $10V/V$ using a $1M\Omega/10M\Omega$ feedback resistor combination. The transient input and output voltages are shown in figure 69. Experimental results show that the actual measured gain is $9.16V/V$.

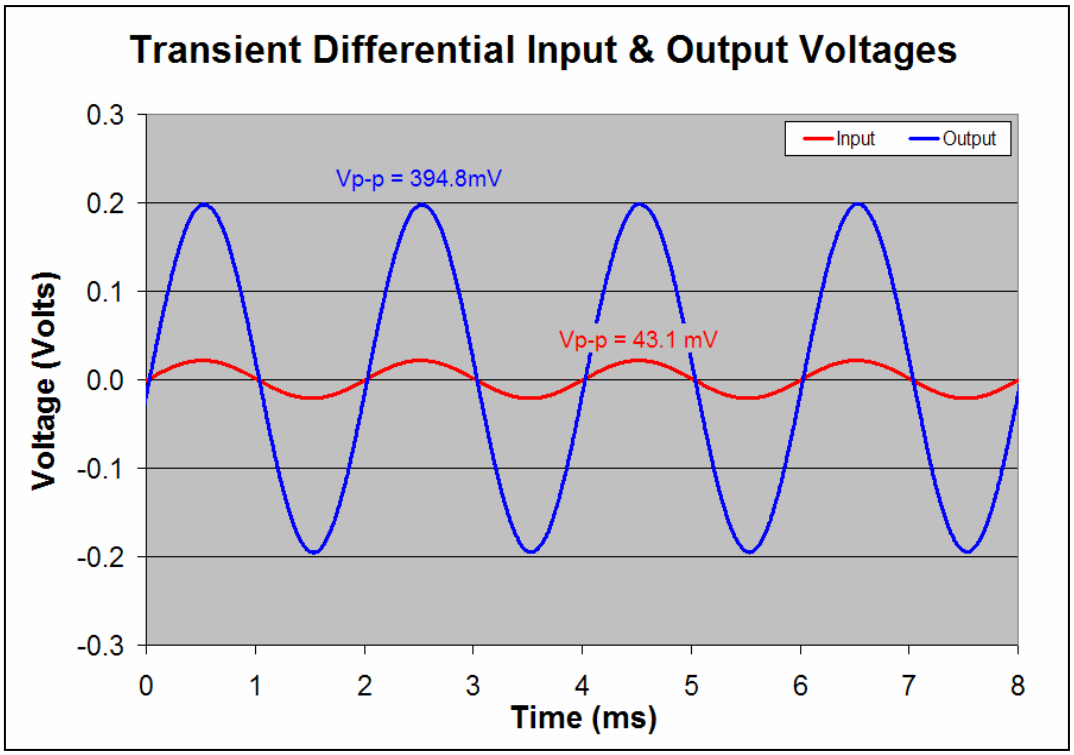


Figure 69: Experimental Transient Input and Output Waveforms for the Telescopic Cascode Differential Amplifier with a 1M/10M Feedback Resistor Configuration

The output offset voltage for the measured closed loop gain of $9.16 V/V$ with this feedback resistor configuration is $54.8 mV$. This voltage is referred to the amplifier input by dividing it by the amplifier gain. Hence, the input referred offset voltage at the telescopic amplifier input is $5.98 mV$. It can be observed that the input referred offset voltage is a few milli volts in both cases with a closed loop gain of $10 V/V$.

Next the telescopic cascode differential amplifier is used in a feedback configuration with a gain of $100 V/V$. In order to achieve this gain, two different feedback resistor combinations are used. First the amplifier is setup with feedback resistors of $100 k\Omega$ and $10 M\Omega$. The measured transient input and output waveforms for this amplifier are shown in figure 70.

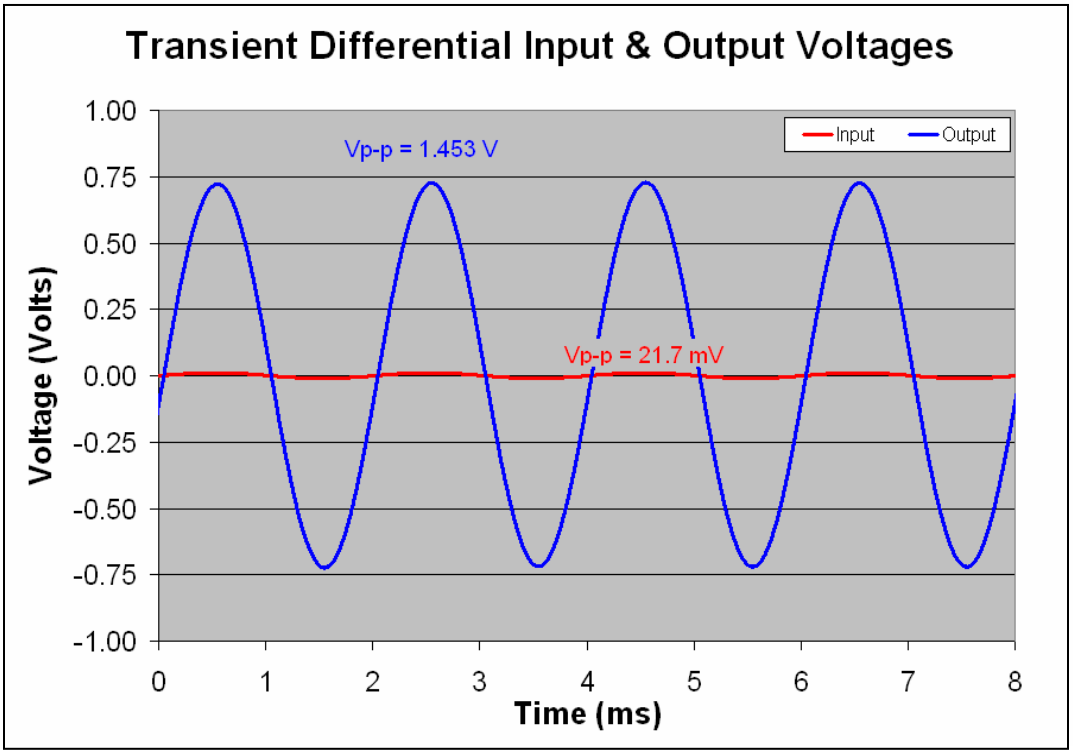


Figure 70: Experimental Transient Input and Output Waveforms for the Telescopic Cascode Differential Amplifier with a 100k/10M Feedback Resistor Configuration

The measured output offset in this case is equal to $203\,mV$. The actual measured gain for this feedback configuration is $67\,V/V$. Hence, the input referred offset voltage is $3.02\,mV$.

Next the amplifier is setup with a closed loop gain of $100\,V/V$ using a $10\,k\Omega/1\,M\Omega$ feedback resistor combination. The transient input and output voltages are shown in figure 71. As can be seen the actual measured gain is $65\,V/V$. The measured output offset voltage for this feedback configuration is $215\,mV$. The input referred offset voltage derived by dividing the output offset voltage with the amplifier gain. As a result, the input referred offset voltage is $3.3\,mV$.

The input referred offset voltage for the folded cascode differential amplifier with a gain of $100\,V/V$ is approximately $3\,mV$.

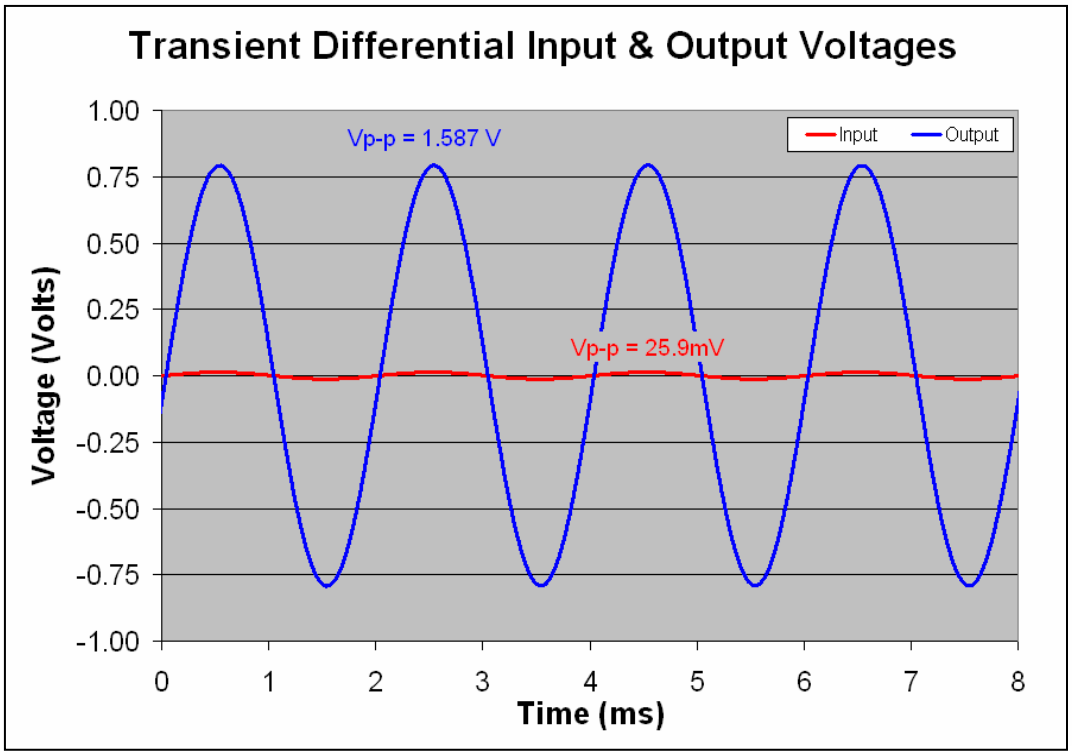


Figure 71: Experimental Transient Input and Output Waveforms for the Telescopic Cascode Differential Amplifier with a 10k/1M Feedback Resistor Configuration

The next section presents the test results for the same telescopic cascode differential amplifier which uses the proposed emitter degeneration resistors for means of auto-zeroing. At the end the results for the two telescopic amplifiers are compared.

4.5.3.2 Telescopic Cascode Amplifier with the Emitter Degeneration Auto-zeroing Technique

In this section, the test results for the auto-zeroed telescopic cascode amplifier are investigated. This chip is designed in 0.13 μm CMOS8RF IBM process technology. The circuit schematic for this chip can be seen in figure 52. It is basically the same as the telescopic cascode differential amplifier tested in the previous section with the added emitter degeneration resistors to perform the auto-

zeroing process. The layout for this amplifier chip is done in Cadence Virtuoso Layout Editor along with the design rule check (DRC), layout vs. schematic (LVS) and extraction from the Assura package. The chip layout is shown in figure 72. The enhanced view of the layout for the auto-zeroed telescopic cascode differential amplifier is shown in figure 73. A picture of the chip is shown in figure 74.

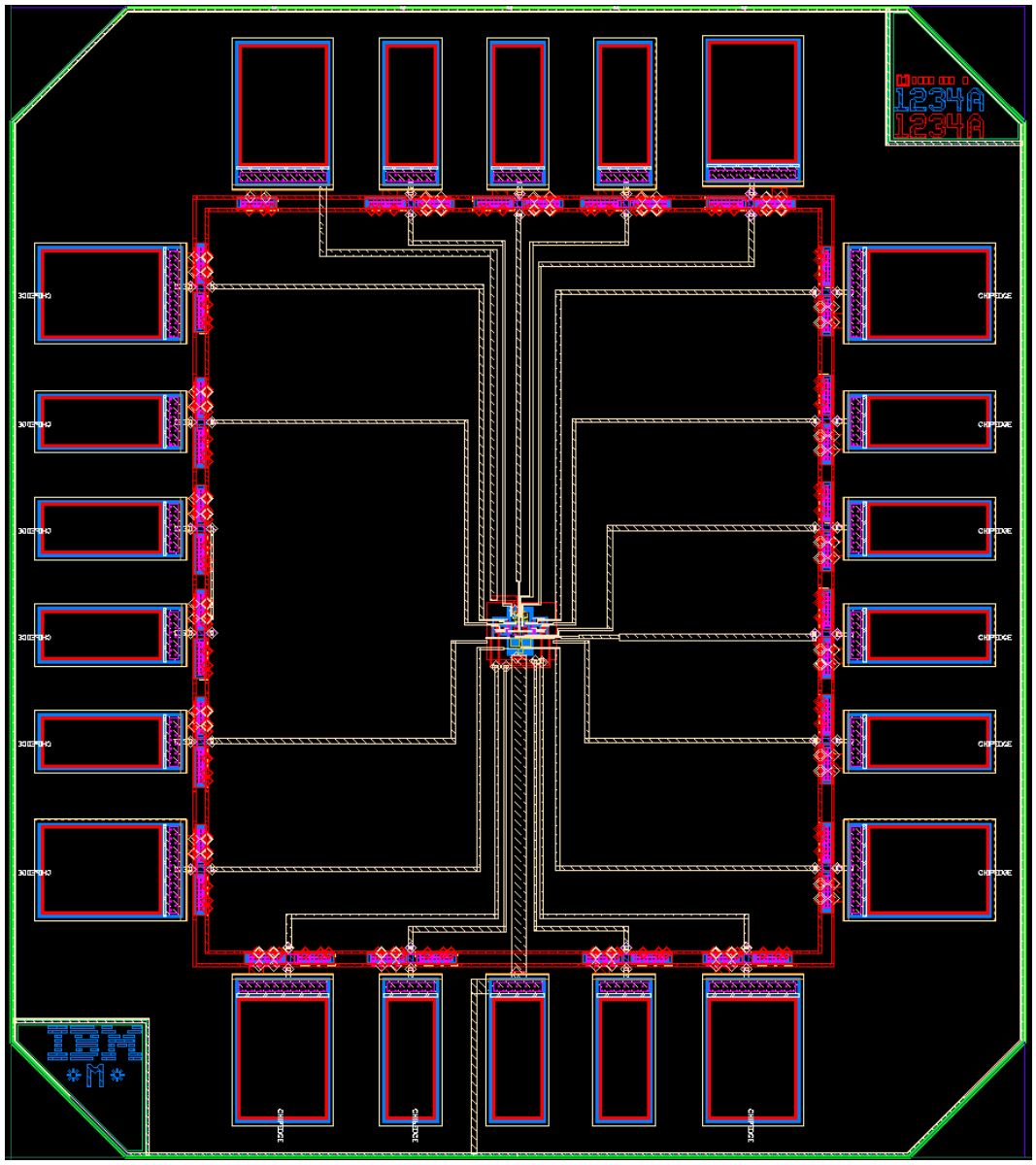


Figure 72: The Chip Layout for the Auto-zeroed Telescopic Cascode Differential Amplifier Shown in Figure 52

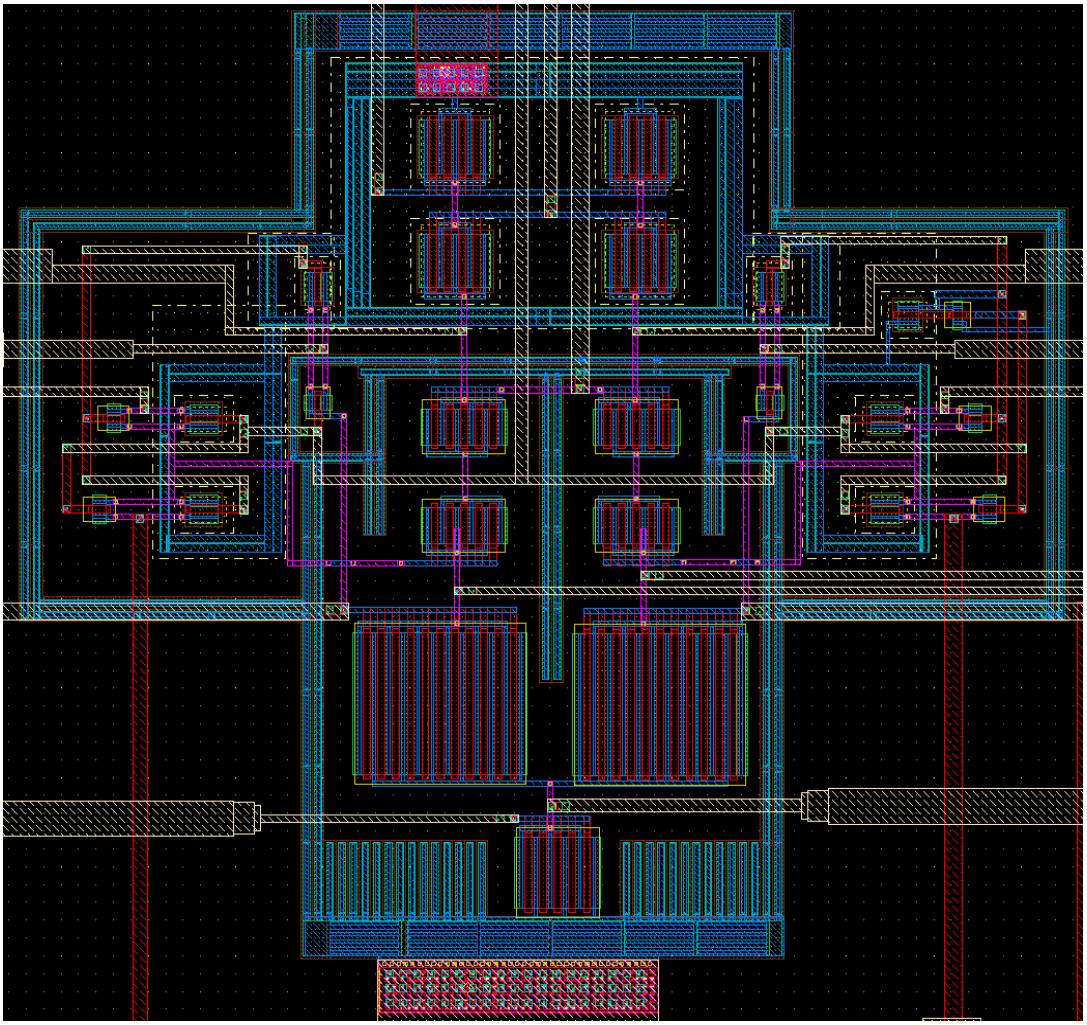


Figure 73: The Auto-zeroed Telescopic Cascode Differential Amplifier Layout

In order to test the auto-zeroed telescopic cascode differential amplifier, it is placed in a feedback loop. First different feedback configurations are used to provide a gain of $10V/V$. The first feedback resistor combination is $10k\Omega/100k\Omega$. The gain is almost the same as that shown for the telescopic cascode differential amplifier and is shown in figure 75. The output voltages and the output offset voltages for the auto-zeroed telescopic cascode amplifier with the control signal are shown in figure 76. The amplifier is in the auto-zeroing phase when the control voltage is high and it is in the amplification mode when the control voltage is low. The average output

offset voltage is $1.8\,mV$. The test results reveal that the output offset voltage for the auto-zeroed telescopic cascode amplifier is 17 times less than the output offset voltage for the telescopic cascode differential amplifier without the auto-zeroing technique. The input referred offset voltage is calculated by dividing the output offset voltage with the amplifier gain. This voltage is $196\,\mu V$.

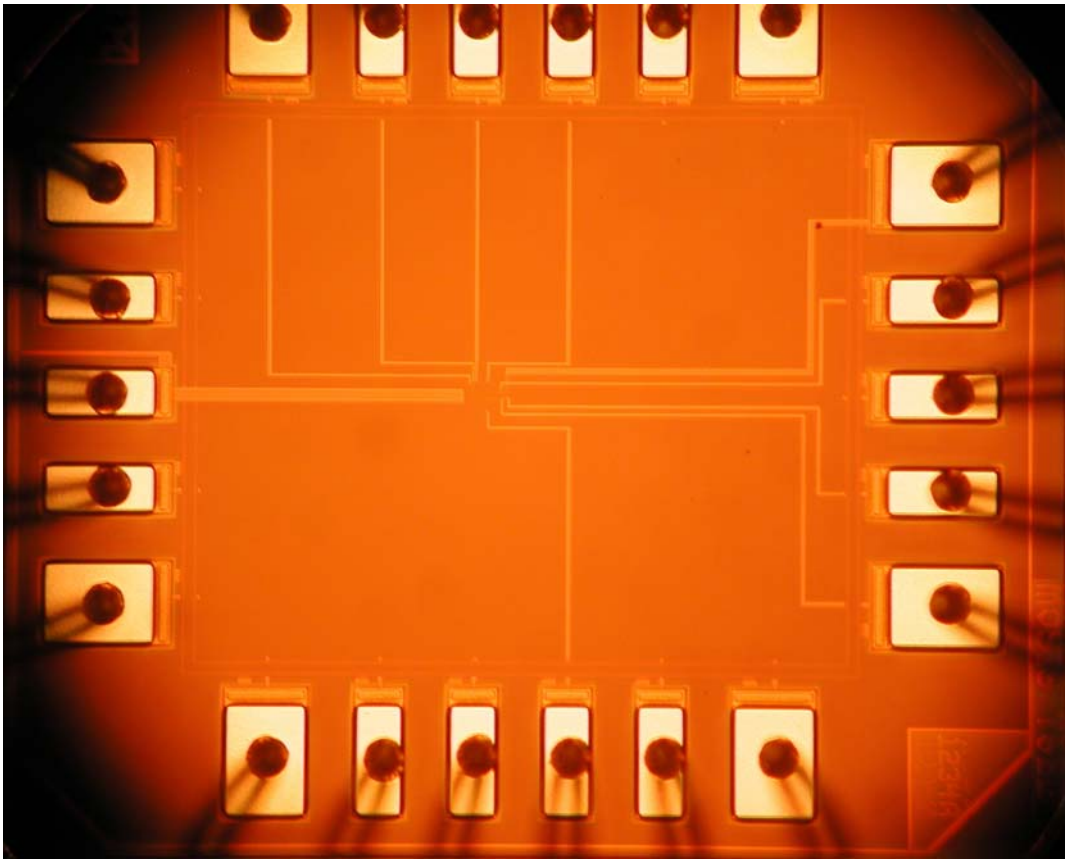


Figure 74: The Auto-zeroed Telescopic Cascode Differential Amplifier Chip

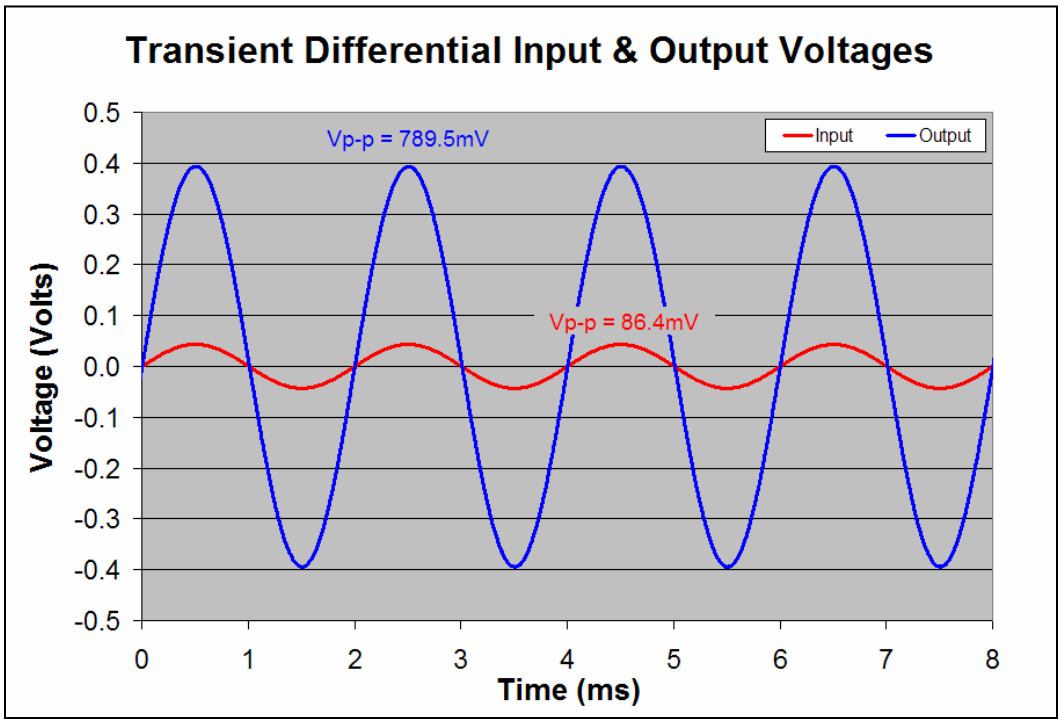


Figure 75: Experimental Transient Input and Output Waveforms for the Auto-zeroed Telescopic Cascode Differential Amplifier with a 10k/100k Feedback Resistor Configuration

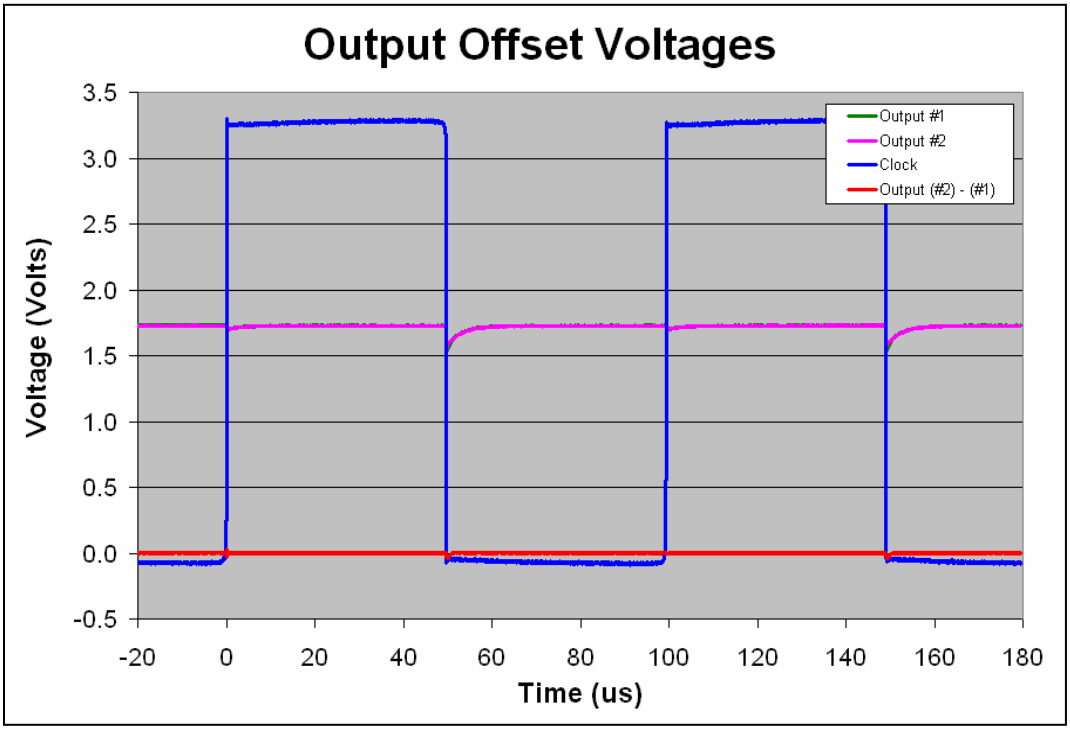


Figure 76: Experimental Output Offset Voltage, Output Voltages and the Control Voltage vs. Time for the Auto-zeroed Telescopic Cascode Differential Amplifier used with a 10k/100k Feedback Configuration

Next the closed loop gain of $10 V/V$ is realized with a feedback resistor combination of $1 M\Omega/10 M\Omega$. The gain is the same as that for the telescopic cascode. The output voltages and the output offset voltages for the auto-zeroed telescopic cascode amplifier along with the control signal are shown in figure 77. The amplifier is in the auto-zeroing phase when the control voltage is high and it is in the amplification mode when the control voltage is low. The average output offset voltage during the auto-zeroing period is $9.5 mV$. This average offset voltage is reduced to 5.1 mV during the amplification period when the amplifier is connected to the signal path. The input referred offset voltage for the auto-zeroed telescopic cascode differential amplifier is the output offset voltage divided by the amplifier gain and is equal to $556 \mu V$.

This value is an order of magnitude smaller than the input referred offset voltage for the telescopic cascode in section 4.5.3.1 with the same feedback configuration.

At this point, different feedback configurations are used to provide a gain of $100 V/V$. The first feedback resistor combination is $100 k\Omega/10 M\Omega$. The output voltages and the output offset voltages for the auto-zeroed telescopic amplifier with the control signal are shown in figure 78. The amplifier is in the auto-zeroing phase when the control voltage is high and it is in the amplification mode when the control voltage is low. The average output offset voltage during the auto-zeroing period is $98.4 mV$. This average offset voltage is reduced to 35.4 mV during the amplification period when the amplifier is connected to the signal path. This output offset voltage for the telescopic cascode amplifier for the same feedback resistor combination

without the emitter degeneration auto-zeroing technique is 203 mV . The test results reveal that the output offset voltage for the auto-zeroed telescopic cascode amplifier is approximately an order of magnitude less than the output offset voltage for the telescopic cascode amplifier without the auto-zeroing technique. It has to be mentioned that both amplifiers are used in the same feedback resistor configuration and with the same feedback resistor combinations. The input referred offset voltage is calculated by dividing the output offset voltage with the amplifier gain. This voltage is approximately 500 μV .

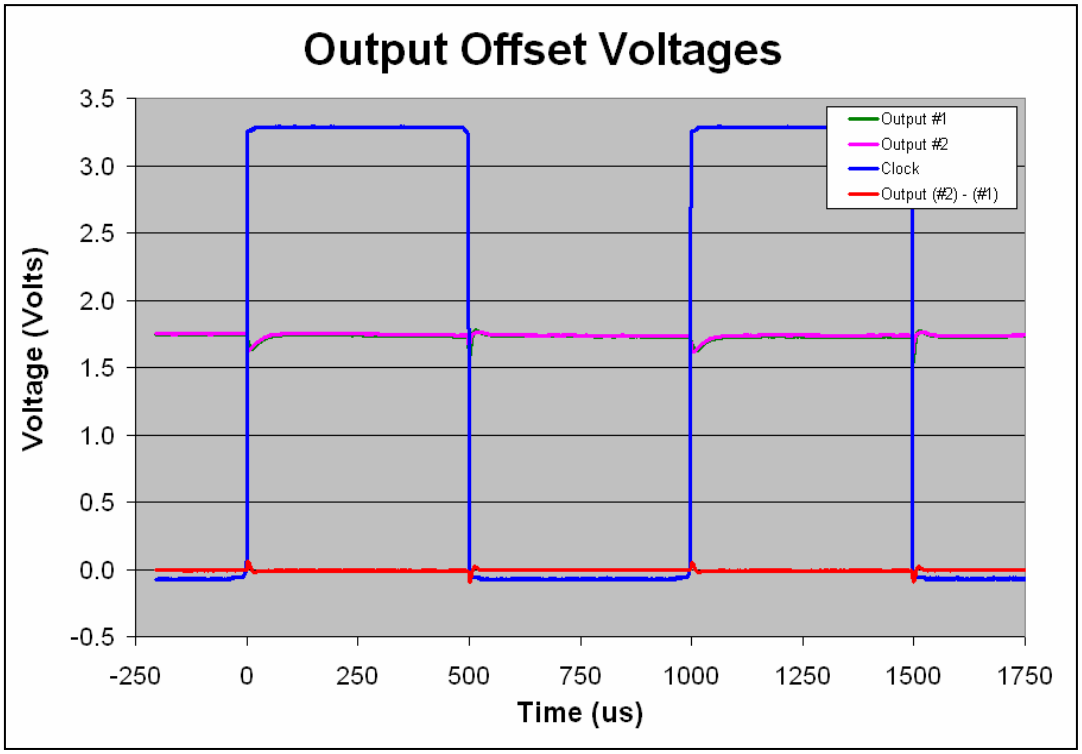


Figure 77: Experimental Output Offset Voltage, Output Voltages and the Control Voltage vs. Time for the Auto-zeroed Telescopic Cascode Amplifier used with a 1M/10M Feedback Configuration

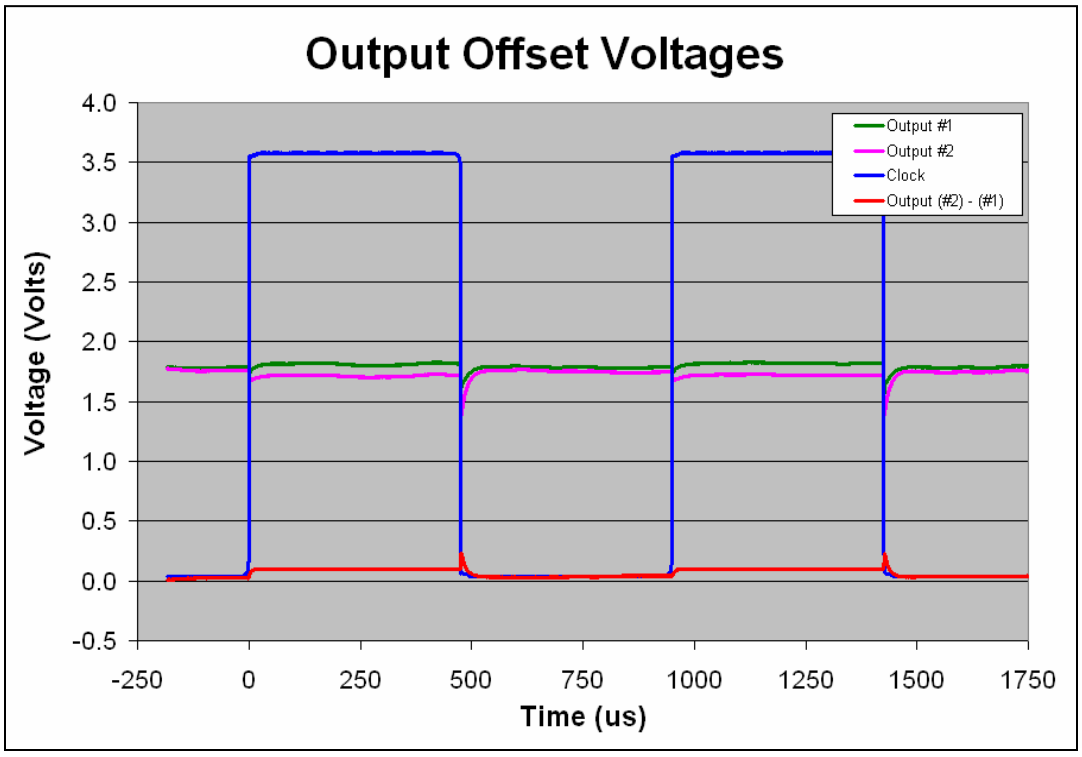


Figure 78: Experimental Output Offset Voltage, Output Voltages and the Control Voltage vs. Time for the Auto-zeroed Telescopic Cascode Amplifier used with a 100k/10M Feedback Configuration

Next the closed loop gain of $100\,V/V$ is realized with a feedback resistor combination of $10\,k\Omega/1\,M\Omega$. The gain is the same as that shown for the telescopic cascode differential amplifier. The output voltages and the output offset voltages for the auto-zeroed telescopic amplifier with the control signal are shown in figure 79. The average output offset voltage during the auto-zeroing period is $67.8\,mV$. This average offset voltage is reduced to $30.7\,mV$ during the amplification period when the amplifier is connected to the signal path. The input referred offset voltage for the auto-zeroed telescopic cascode amplifier is the output offset voltage divided by the amplifier gain and is approximately $430\,\mu V$. This is approximately an order of magnitude smaller than the input referred offset voltage seen in the previous section for the folded cascode differential amplifier.

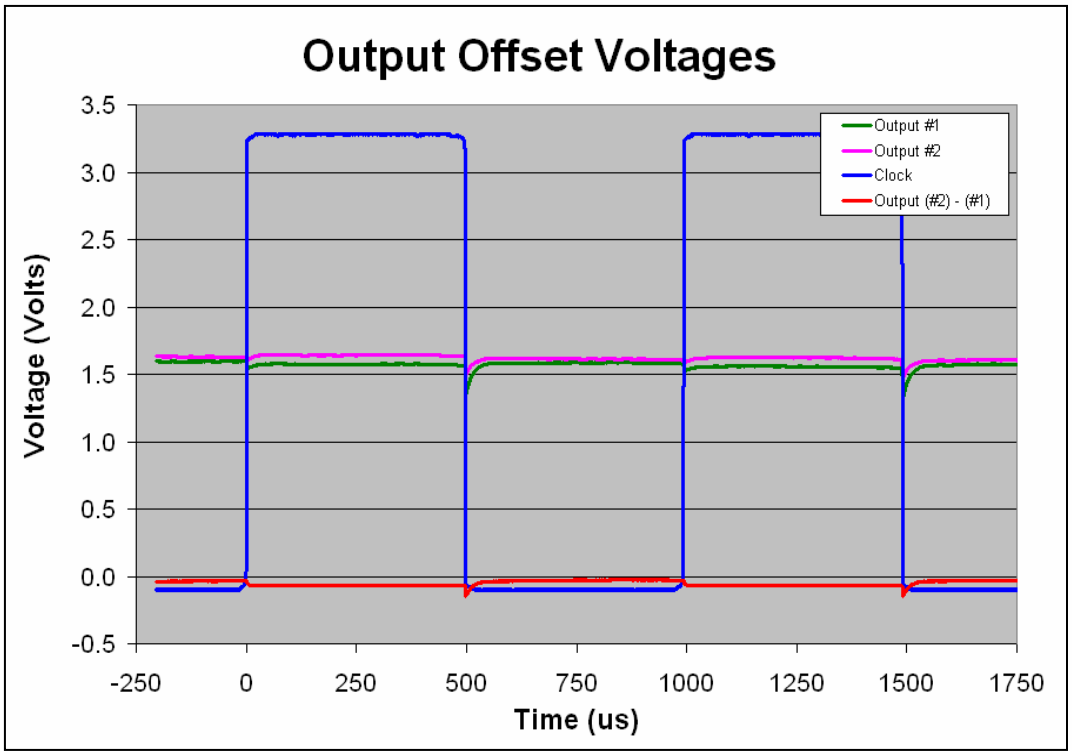


Figure 79: Experimental Output Offset Voltage, Output Voltages and the Control Voltage vs. Time for the Auto-zeroed Telescopic Cascode Amplifier used with a 10k/1M Feedback Configuration

4.5.3.3 Comparison

In this section the experimental results for the telescopic cascode differential amplifier and the auto-zeroed telescopic cascode differential amplifier are compared. For the closed loop gain of $10\,V/V$ with $10\,k\Omega/100\,k\Omega$ feedback resistor combination, the average output offset voltage for the telescopic cascode differential amplifier is $30.8\,mV$. This output offset voltage for the telescopic cascode differential amplifier with the auto-zeroing technique is $1.8\,mV$. This translated to input referred offset voltage of $196\,\mu V$. The experimental results obtained for the output offset voltage of the telescopic cascode differential amplifier with and without the auto-zeroing technique are shown in figure 80. These results reveal that the output offset voltage for the auto-zeroed telescopic cascode amplifier is 17 times less

than the output offset voltage for the telescopic cascode differential amplifier without the auto-zeroing technique. It has to be mentioned that both amplifiers are used in the same feedback resistor configuration and with the same feedback resistor combinations.

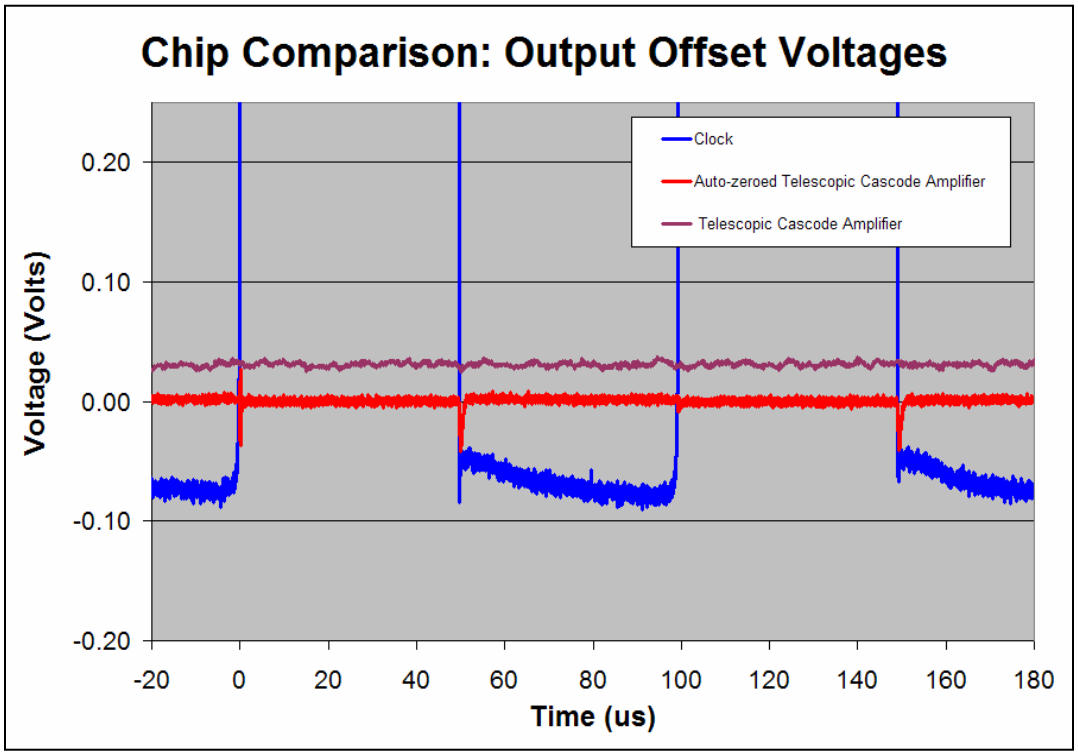


Figure 80: Experimental Output Offset Voltages for the Auto-zeroed Telescopic Cascode Amplifier and the Telescopic Cascode Amplifier used with a 10k/100k Feedback Configuration

Next the test results for the closed loop gain of $10\,V/V$ realized with a feedback resistor combination of $1\,M\Omega/10\,M\Omega$ are compared. The average output offset voltage is reduced to $5.1\,mV$ during the amplification period when the amplifier is connected to the signal path. This translates to an input referred offset voltage of $556\,\mu V$. The output offset voltage for the telescopic cascode amplifier with the same feedback resistor combination without the emitter degeneration auto-zeroing technique is $54.8\,mV$ as seen is section 4.5.3.1. The test results obtained for the

output offset voltage for the telescopic cascode differential amplifier with and without the auto-zeroing technique are shown in figure 81. These results show that the output offset voltage is reduced by an order of magnitude.

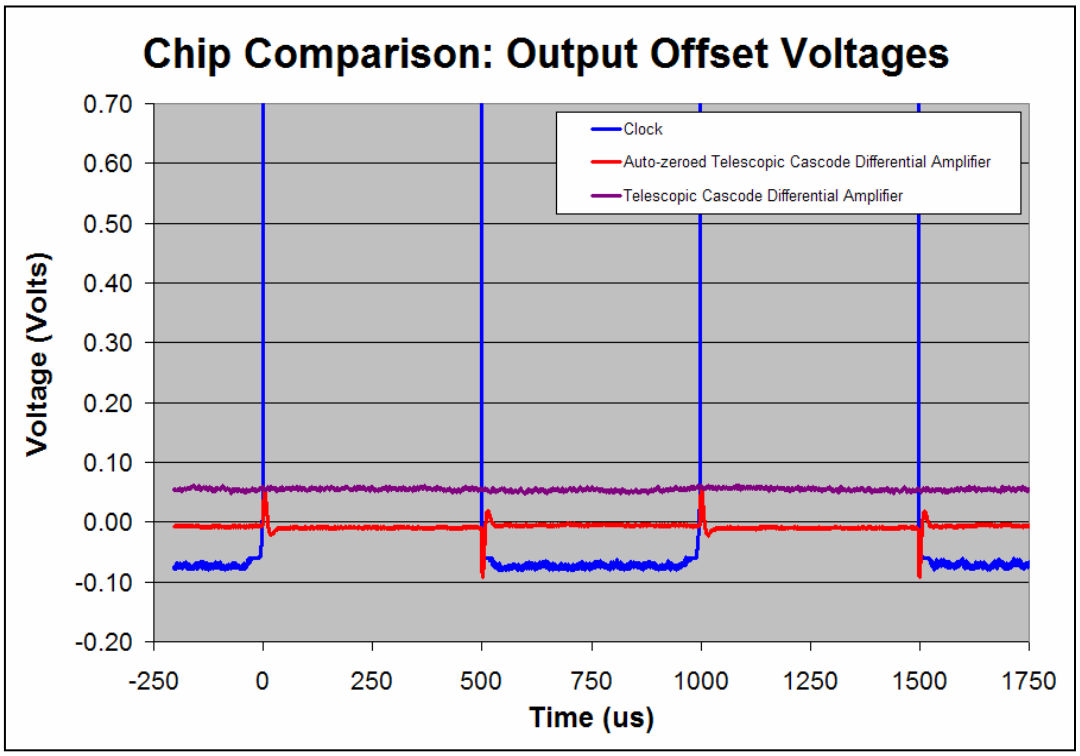


Figure 81: Experimental Output Offset Voltages for the Auto-zeroed Telescopic Cascode Amplifier and the Telescopic Cascode Amplifier used with a 1M/10M Feedback Configuration

To compare the results for the different feedback resistor combinations which provide a gain of $100\,V/V$, we will start by comparing the results for the feedback resistor combination of $100\,k\Omega/10\,M\Omega$. The average output offset voltage is reduced to 35.4 mV during the amplification period when the amplifier is connected to the signal path. This translates to the input referred offset voltage of $500\,\mu V$. The output offset voltage for the telescopic cascode amplifier with the same feedback resistor combination without the auto-zeroing technique is $203\,mV$ as seen in section 4.5.3.1. The experimental results obtained for the output offset voltage for the telescopic

cascode differential amplifier with and without the auto-zeroing technique are shown in figure 82. It can be seen that the output offset voltage for the auto-zeroed telescopic cascode amplifier is approximately an order of magnitude smaller than the output offset voltage for the telescopic cascode amplifier without the auto-zeroing technique.

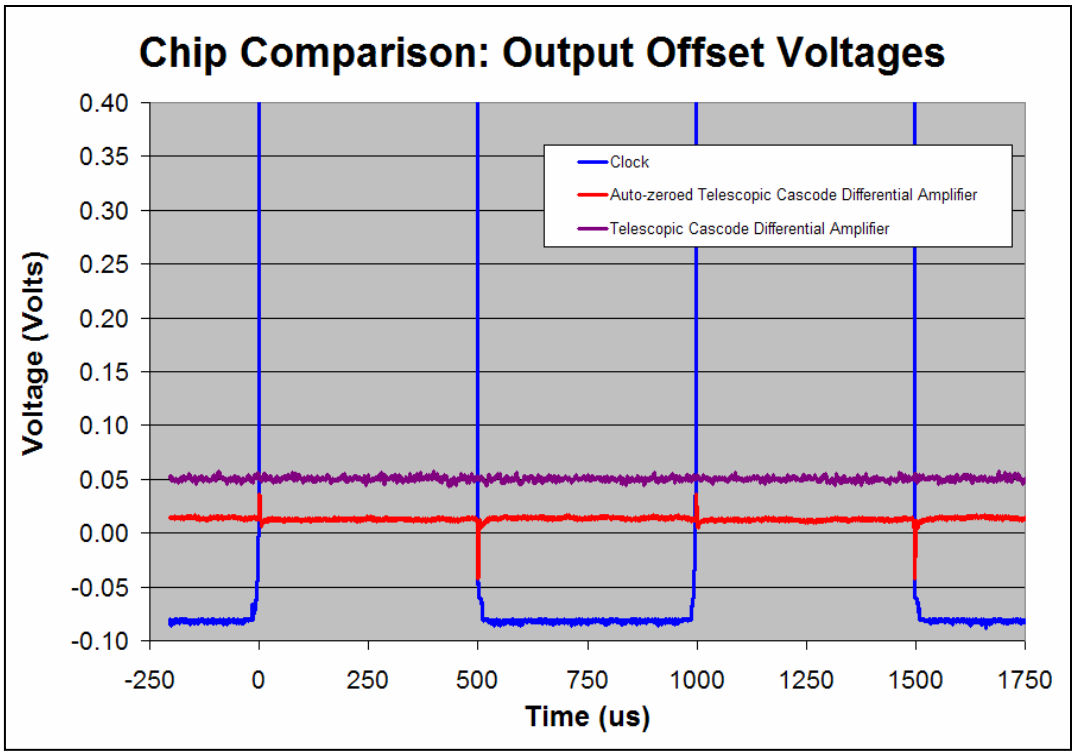


Figure 82: Experimental Output Offset Voltages for the Auto-zeroed Telescopic Cascode Amplifier and the Telescopic Cascode Amplifier used with a 100k/10M Feedback Configuration

The last feedback resistor combination which leads to a closed loop gain of $100\,V/V$ is realized with a feedback resistor combination of $10\,k\Omega/1\,M\Omega$. The average output offset voltage in this case is $30.7\,mV$ during the amplification period when the amplifier is connected to the signal path. This translates to the input referred offset voltage of $430\,\mu V$. The output offset voltage for the telescopic cascode amplifier with the same feedback resistor combination without the emitter

degeneration auto-zeroing technique is $215\,mV$ as shown in section 4.5.3.1. These experimental results are shown together in figure 83. As can be seen from the test results, the output offset voltage approximately an order of magnitude less than the case where the telescopic cascode amplifier is not used with the auto-zeroing technique.

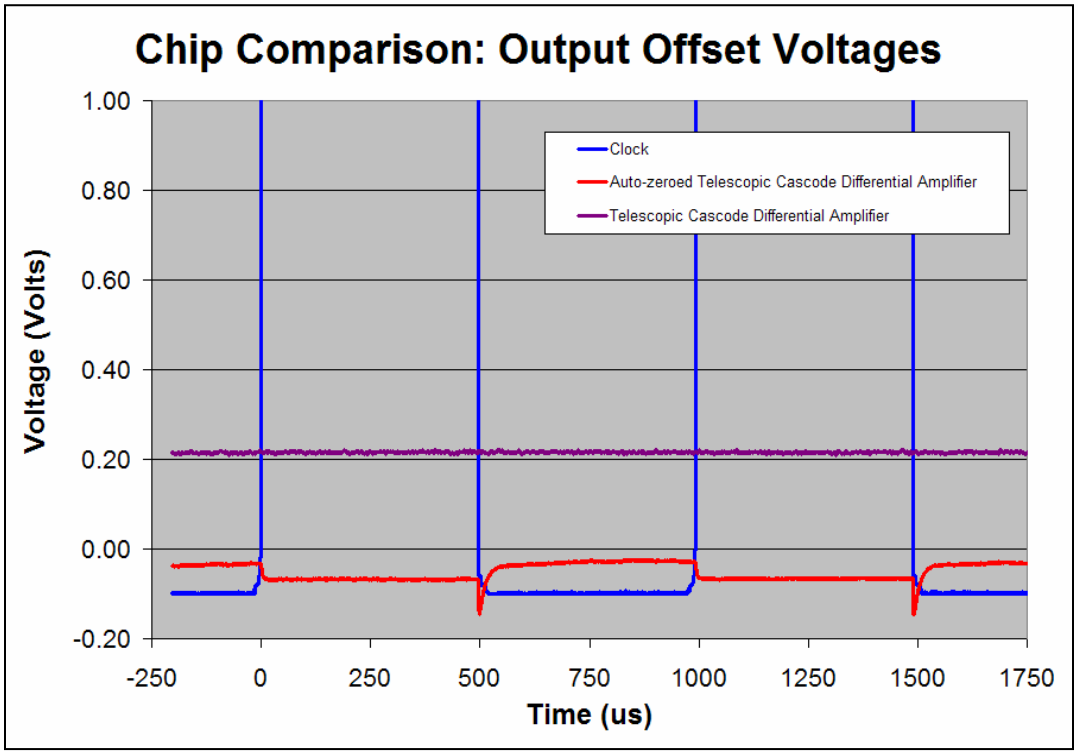


Figure 83: Experimental Output Offset Voltages for the Auto-zeroed Telescopic Cascode Amplifier and the Telescopic Cascode Amplifier used with a 10k/1M Feedback Configuration

From the comparisons made in this section, it is obvious that the emitter degeneration auto-zeroing technique reduces the output offset voltage and as a result the input referred offset voltage. The emitter degeneration auto-zeroing technique reduces the input referred offset voltage by more than an order of magnitude.

Chapter 5: Noise Sources in Detector Sensors

5.1 Introduction

Reset noise defines the limit on signal detection in capacitive sensors. Reset noise occurs in sensing circuits when sensor capacitor is reset causing charge to accumulate on the capacitor. And ultimately the charge value on the capacitor is sensed. Reset noise in capacitive sensors is mainly caused by thermal noise and shot noise since thermal and shot noise are an inherent part of transistors, resistors, and diodes [31]-[33]. $1/f$ noise is typically not the dominant noise term in these circuits. For the sake of completeness, all the noise sources in integrated circuits are reviewed in this chapter.

5.2 Noise Sources in Integrated Circuits

In this section, noise sources in integrated circuits are briefly reviewed.

5.2.1 Thermal Noise

Thermal noise in a resistor is due to the random motion of electrons caused by temperature. The power spectral density of the thermal noise in a resistor is given by equation (5.1).

$$V_R^2(f) = 4kTR \quad \mathrm{V}^2/Hz \qquad (5.1)$$

The amplitude distribution of thermal noise is white noise in which k is the Boltzman constant, T is temperature in Kelvin, and R is resistance in ohms. The thermal noise of the resistor can be modeled as a current source in parallel with a resistor or a voltage source in series with a resistor as shown in figure 84.

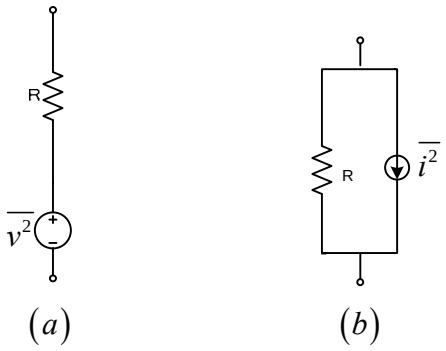


Figure 84: Thermal Noise Representation

5.2.2 Shot Noise

Shot noise is the time-dependent fluctuations in the current. Shot noise results from the fact that current in semiconductor devices is not a continuous flow, instead it is the sum of discrete pulses in time. Each of these pulses corresponds to the discrete transfer of an electron through the conductor. Shot noise is well known to occur in devices such as Schottky barrier diodes and p-n junctions. Passage of an electron or a hole across the barrier is dependent upon the energy and velocity of the carrier. Theoretically, this electron or hole transfer can be modeled as a random event. Shot noise in these devices is given by (5.2).

$$I_{shot}{}^2(f) = 2qI_{DC} \quad A^2/Hz \qquad (5.2)$$

The effect of shot noise in a diode can be modeled with a current source in parallel with a diode as can be seen in figure 85.

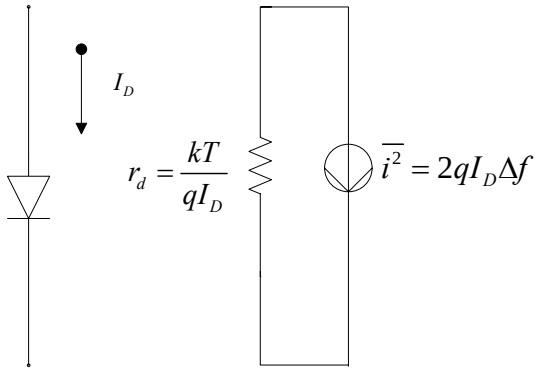


Figure 85: Small Signal Equivalent Circuit for Junction Diode

Most textbooks mention that shot noise does not exist in resistors but this is not true [34], [35]. Shot noise is present in any current stream composed of discrete charges. It is usually just less than thermal (Johnson) noise at room temperature. In a macroscopic resistor, inelastic electron-phonon scattering smoothes out the current fluctuations that are caused from the discreteness of an electron. Shot noise is observed in mesoscopic resistors although at lower levels than in a tunnel junction.

Shot noise in a resistor may be a function of its length. When the resistor is shorter than the mean free path for any scattering process, the electrons can not be scattered, so the probability of an electron being transmitted is unity and there is no shot noise. When the resistor is longer than the mean free path for electron scattering, the electrons will be scattered by the same process. For the elastic scattering regime, the shot noise is $2/3qI \quad A^2/Hz$, which is one third of the shot noise seen in tunnel junctions [35]. If a resistor is longer than the electron-electron scattering length, the electrons will experience inelastic collisions. The electrons will be heated above the

lattice temperature. This is called the hot electron regime [35]. The shot noise in the hot electron regime is enhanced to $(3/4)^{1/2} qI \ \ A^2/Hz$.

As can be seen in both situations the shot noise is proportional to the full Poissonian shot noise. The proportionality constant is just a simple numerical coefficient and does not depend in shape of the resistor or the material it is made of.

Shot noise and thermal noise are very different from each other. In order to have thermal noise, it is not required for current flow to be present. The electrons can move in and out of the resistor in a random motion. However, current flow is necessary for shot noise, thus, the electrons must move randomly, scattered out of pure rectilinear motion.

5.2.3 Flicker Noise

Flicker noise is present in all active devices. Flicker noise is caused by traps and crystal defects. The traps, caused by contamination, capture and release carriers in a random manner. Time constants of this process cause noise which is dominant at low frequencies. Flicker noise is the result of the direct flow of current and contains a spectral density of the form given by (5.3).

$$\overline{i^2}(f) = K_1 \frac{I^{\mathrm{a}}}{f^b} \Delta f \qquad (5.3)$$

where, Δf is a small bandwidth at frequency f, I is direct current, and K_1 is the constant for a particular device, a is a constant in the range 0.5 to 2, and b is a constant of about unity.

Flicker noise has an arbitrary constant K_1 which depends on the device type. The constant has also been known to vary for different integrated circuits from the

same process wafer. This happens since the flicker noise is dependent on contamination and crystal imperfections which can vary on the same silicon wafer. The value of K_1 is measured for devices from the same process, and the average value is used to predict the flicker noise performance for the integrated circuits in that process.

The amplitude distribution of flicker noise is a non-Gaussian function. The flicker noise spectrum density is shown in figure 86.

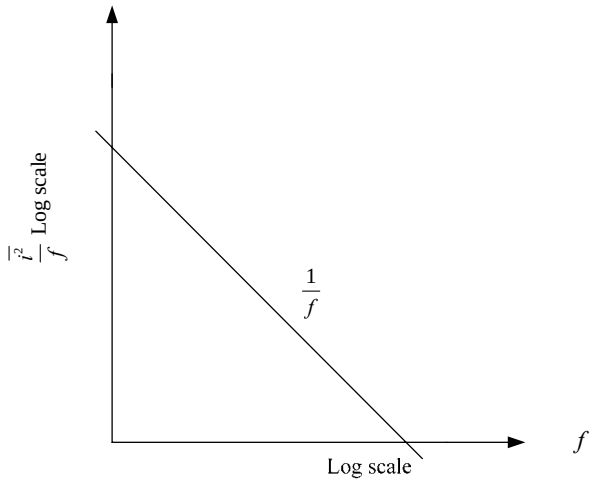


Figure 86: Flicker Noise Spectrum Density as a Function of Frequency

5.2.4 Burst Noise

Burst noise is a low frequency noise present in transistors. This noise is related to the presence of heavy-metal contamination. For example, gold doped devices show high levels of burst noise. Burst noise resembles a pulse, and the repetition rate is usually located in the audio frequency range. The spectral density of burst noise is given by (5.4) as follows:

$$\overline{i^2} = K_2 \frac{I^c}{1+\left(\frac{f}{f_c}\right)^2} \Delta f \qquad (5.4)$$

where, K_2 is a constant for the particular device, I is the direct current, c is a constant in the range of 0.5 to 2, and f_c is the particular frequency for a given noise process.

A burst noise spectrum is plotted in figure 87. It can be observed that the noise spectrum falls as $1/f^2$ at higher frequencies. The amplitude distribution of burst noise is non-Gaussian. The factor K_2 varies and consequently, should be determined using experiments.

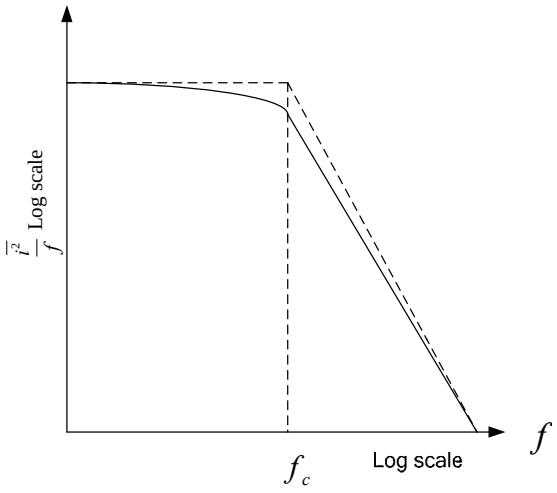


Figure 87: Burst Noise Spectral Density

5.2.5 Avalanche Noise

Avalanche noise is present in devices such as Zener diodes or *pn* junctions, operating near the internal breakdown field of the materials from which they are made. Holes and electrons in the depletion region of a reverse-biased *pn* junction

receive energy to generate electron-hole pairs by collision with silicon atoms. One carrier can start an avalanche process which will result in many carriers moving together. This process causes large noise spikes, much greater in amplitude than shot noise with the same current. This explains why Zener diodes are avoided in low noise circuits.

5.3 Noise Models of Integrated Circuits

In this section, the noise models for different devices used in integrated circuits are investigated.

5.3.1 Junction Diodes

To model the noise for the junction diode, following model of a diode in forward bias as shown in figure 88 will be considered. The resistor, r_s, is due to the resistivity of silicon. This resistance exhibits thermal noise which is represented as a voltage source in series with r_s. The diode in forward bias is modeled with a resistance, r_d. The diode's shot noise and flicker noise are symbolized as a current source in parallel with the diode resistance, r_d.

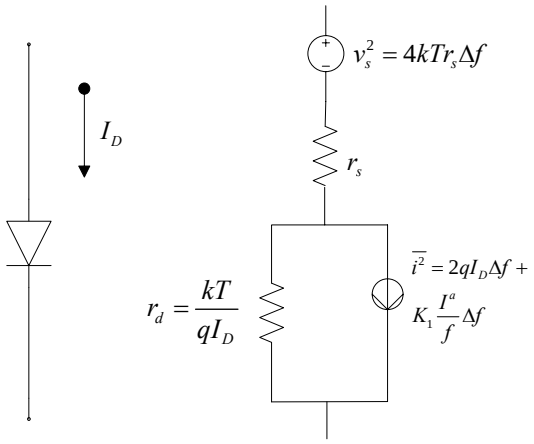


Figure 88: Noise Model for the Junction Diode

The noise sources are expressed in equations (5.5) and (5.6).

$$\overline{v_s^2} = 4kTr_s\Delta f \qquad (5.5)$$

$$\overline{i^2} = 2qI_D\Delta f + K\frac{I_D^a}{f}\Delta f \qquad (5.6)$$

5.3.2 MOS Transistors

The drain current in the MOSFET is controlled by the gate source voltage through the resistive channel under the gate. This channel behaves as a resistor introducing thermal noise. This noise can be represented by a current source in parallel with the output resistance of the MOSFET in the small signal model as shown in figure 89.

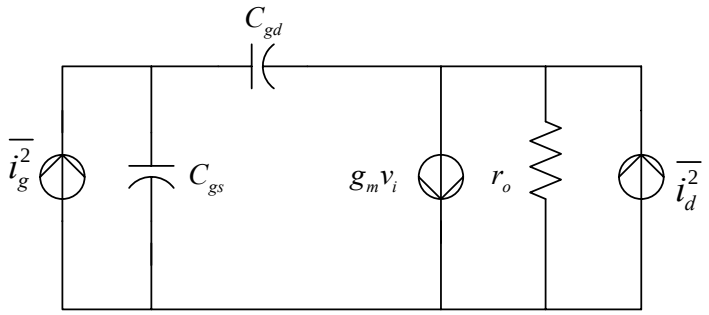


Figure 89: MOSFET Small Signal Equivalent Circuit with Noise Sources

Since MOS transistors conduct current near the surface of the silicon, surface states act as traps. The surface states capture and release the carriers generating flicker noise in MOS transistors. Flicker noise can also be represented by a current source in parallel with the output resistance of the MOS transistor in the small signal model. The flicker noise and thermal noise can be combined into one noise generator $\overline{i_d^2}$, as shown in equation (5.7).

$$\overline{i_d^2} = 4kT\left(\frac{2}{3g_m}\right)\Delta f + K\frac{I_D^a}{f}\Delta f \qquad (5.7)$$

Where, I_D is drain bias current, K is an arbitrary constant for a given device, a is a constant between 0.5 and 2, and g_m is the device transconductance at the operating point. Equation (5.7) holds for long channel devices. The thermal noise in short channel devices is 2 to 5 times more than the first term in equation (5.7) and results from the hot electron effects in short channel devices.

Another source of noise in deeply-scaled MOSFET transistors is the shot noise caused by the gate leakage current. Here, the gate oxide is thin enough for the electrons to tunnel through. This noise is expressed in (5.8).

$$\overline{i_g^2} = 2qI_G\Delta f \qquad (5.8)$$

Since the gate leakage current is very small in MOS transistors, this type of noise is of the order of $10^{-15}\ A/\sqrt{Hz}$.

5.3.3 Bipolar Junction Transistors

When the bipolar transistor is in the forward active region, the collector current shows shot noise. The minority carriers diffuse and drift in the base region to be collected at the collector-base junction. The arrival time of the carriers at the collector is a random variable. The collector shot noise is given in (5.9).

$$\overline{i_c^2} = 2qI_C\Delta f \qquad (5.9)$$

The noise at the base is due to shot noise and thermal noise. The base current is caused by recombination in the base and carrier injection from base to the emitter. Since the previous processes are random in nature, the base current contains shot

noise. The base resistor exhibits thermal noise as shown in equation (5.10). Similarly, the collector resistor also shows thermal noise; however, it can be neglected since the collector resistance is in series with the high impedance collector.

$$\overline{v_b^{\,2}} = 4kTr_b\Delta f \qquad (5.10)$$

Flicker noise and burst noise have been experimentally characterized by current sources in parallel with the base emitter junction. The flicker noise, burst noise, and base shot noise can be combined into one equation, as shown in (5.11).

$$\overline{i_b^2} = 2qI_B\Delta f + K_1\frac{I_B^a}{f}\,\Delta f + K_2\frac{I_B^c}{1+\left(\frac{f}{f_c}\right)^2}\,\Delta f \qquad (5.11)$$

The equivalent noise model for a bipolar transistor is shown in figure 90.

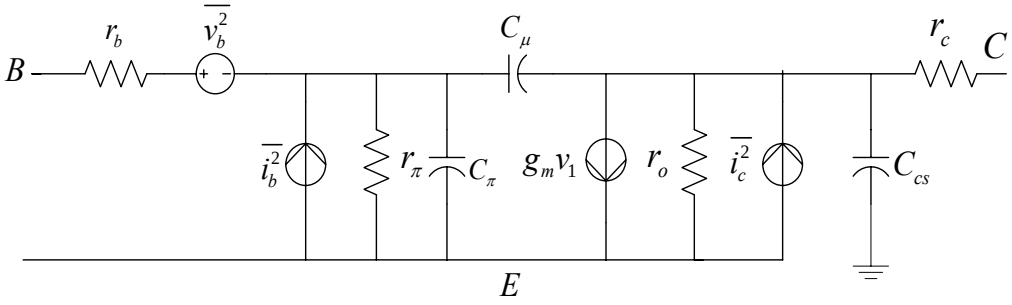


Figure 90: Equivalent BJT Model with Noise

5.3.4 Resistors

Resistors display thermal noise given by (5.1). Carbon resistors, in addition, present flicker noise. Therefore when carbon resistors are used as external components, flicker noise should be taken into account.

5.3.5 Capacitors and Inductors

Integrated circuits often contain capacitive elements. Inductors are used in high frequency integrated circuits. Ideal capacitors and inductors are noiseless. However, real capacitors and inductors have parasitic resistances which introduce thermal noise.

5.4 Noise Analysis in Detector Circuits

In this section, noise of the detector front end is investigated. The diagram of a detector front-end is shown in figure 91.

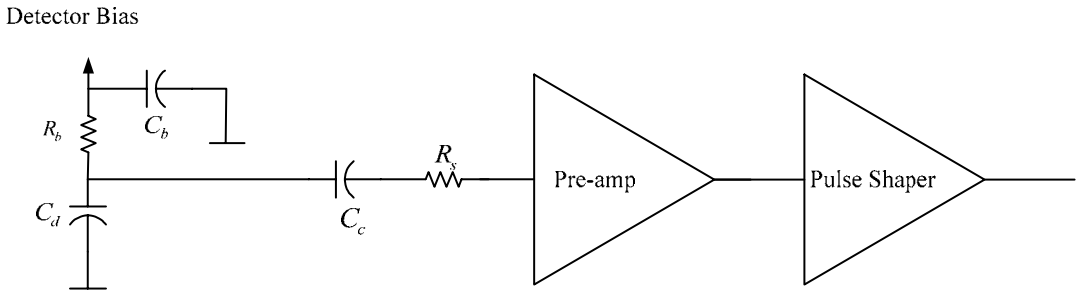


Figure 91: A Typical Detector Front End Circuit

The detector capacitor is represented by C_d. The sensor bias voltage is applied through a bias resistance, R_b. Capacitor, C_b, is a bypass capacitor used to avoid any external interference from the supply line to ground. Capacitor, C_c, is a coupling capacitor which blocks the sensor bias voltage from the amplifier input. The series resistance, R_s, includes any resistance in the connection from the sensor to the amplifier. This resistance includes the sensor electrode resistance, the connecting wire resistance, parasitic resistances in the input transistor of the amplifier, and

amplifier input protection resistance which is used to protect the amplifier against large voltage transients.

The equivalent small signal noise model for this circuit is shown in figure 20. To analyze the circuit, it is assumed that a voltage amplifier is being used so the noise contributions of all the components will be introduced as noise voltages at the amplifier input. First, the frequency distribution of all the noise sources present in the circuit is determined. Then, it is integrated over the frequency response of the pulse shaper to find the total noise present at the pulse shaper output. At the end, the equivalent noise charge for the detector front end is obtained.

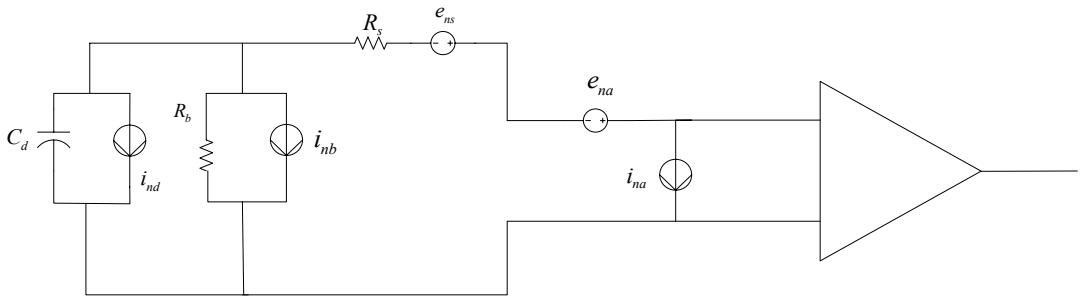


Figure 92: Equivalent Small Signal Circuit for Detector Noise Analysis

5.4.1 Noise Contributions

As the first step, the noise contribution from each individual component is ascertained.

5.4.1.1 Detector Leakage Current

The shot noise of the sensor leakage current is represented by a current noise generator, i_{nd}, in parallel with a sensor capacitor. Below the model is shown in figure 93.

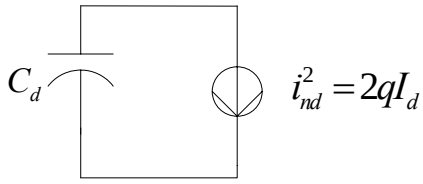


Figure 93: Detector Shot Noise Model

In the model, it is assumed that the input impedance of the amplifier is infinite. In addition, the shunt resistance, signified by R_b, is much larger than the capacitive reactance of the detector in the frequency range of the pulse shaper. The second assumption rises from the fact that if R_b is too small, the signal charge in the detector capacitance will discharge before the pulse shaper output peaks. In order to avoid this, R_b is chosen such that (5.12) holds.

$$R_b C_d \gg T_P \approx \frac{1}{\omega_P} \qquad (5.12)$$

Where, ω_P is the mid-band frequency of the shaper so $R_b \gg \frac{1}{C_d \omega_P}$, which is the assumption made earlier. With these assumptions, the noise current will flow through the detector capacitance yielding the following noise voltage contribution:

$$e_{nd}^2 = i_{nd}^2 \frac{1}{\left(\omega\, C_d\right)^2} = 2qI_d \frac{1}{\left(\omega\, C_d\right)^2} \qquad (5.13)$$

It can be seen from (5.13) that as frequency increases, the noise decreases. In other words, the noise decreases with shorter shaping time.

5.4.1.2 Parallel Resistance

The bias resistor, R_b, is effectively in parallel with the amplifier input so the noise generator for this resistor is modeled as a current source, i_{np}, in parallel. The equivalent circuit is portrayed in figure 94.

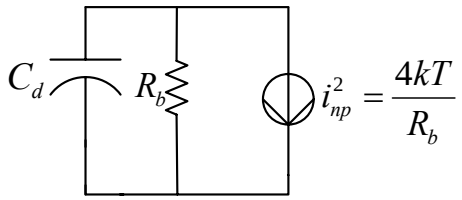


Figure 94: Noise Model for the Bias Resistor

The noise voltage applied to the amplifier input is given by (5.14).

$$e_{np}^2 = \frac{4kT}{R_b}\left(\left|\frac{R_b.\frac{1}{j\omega C_d}}{R_b+\frac{1}{j\omega C_d}}\right|\right)^2 = 4kTR_b\frac{1}{1+\left(\omega R_b C_d\right)^2} \qquad (5.14)$$

Integration of (5.14) over the frequency range which is infinite in this case is given by (5.15) as follows:

$$\int_0^\infty e_{np}^2(\omega)d\omega = \int_0^\infty \frac{4kTR_b}{1+\left(\omega R_b C_d\right)^2}d\omega = \frac{kT}{C_d} \qquad (5.15)$$

Obviously the result is independent of R_b and referred to as "*kTC"* noise. "*kTC"* noise is commonly interpreted as the detector capacitance noise erroneously. The detector capacitor is noiseless as it does not source or sink charge, it merely stored it. Although, noise is generated in the resistor, it is independent of the resistance, R_b. The reason for this is that R_b defines both the primary noise and

noise bandwidth of the circuit. As R_b increases, its thermal noise increases. At the same time, the noise bandwidth decreases. This makes the total noise independent of R_b.

5.4.1.3 Series Resistance

The noise generator for the series resistance, R_s, is signified by a voltage source $e_{ns}^2 = 4kTR_s$, which is simply in series with the other noise sources in the circuit.

5.4.1.4 Amplifier Input Noise

Amplifier noise sources are not physically present at the amplifier input. The amplifier noise is generated in the amplifier and appears at the output. This noise is referred to the input by dividing the output noise by the amplifier gain.

The amplifier noise is described by a combination of voltage and current sources at its input, e_{na} and i_{na}, respectively. The noise voltage sources are in series and add in quadrature as shown in (5.16).

$$e_{na}^2 = e_{nw}^2 + \frac{A_f}{f} \qquad (5.16)$$

The first term is the white noise distribution while the second term represents the $1/f$ noise. The noise coefficient, A_f, is device specific on the order of 10^{-10} to 10^{-12} V^2. White noise distributions remain white. However, some of the noise current will flow through the detector capacitor resulting a frequency dependent noise voltage, $i_{na}/(\omega C_d)$. Here the original white noise spectrum of the shot noise and the bias resistor thermal noise now has a $1/f$ behavior.

5.5 Equivalent Noise Charge in the Detector Front End

At this point, we have calculated the noise contribution of each component in the amplifier front-end. The frequency distribution of the noise voltage at the amplifier input from each of the individual noise sources determined in the previous sections can be used to find the equivalent noise charge in the detector front end. The equivalent noise charge is defined as the input signal charge for a signal-to-noise ratio of one. In order to calculate the equivalent noise charge, the equivalent output noise is measured. The output signal is found for a known input signal. Next, an equivalent noise charge, which corresponds to a signal charge where $S/N = 1$, is determined.

In this case, it is assumed that the pulse shaper is a simple RC-CR shaper with equal differentiation and integration time constants, $\tau_d = \tau_i = \tau$. The equivalent noise charge is given in (5.17).

$$Q_n^2 = \left(\frac{e^2}{8}\right)\left[\left(2qI_d + \frac{4kT}{R_b} + i_{na}^2\right)\tau + \left(4kTR_s + e_{na}^2\right)\frac{C_d^2}{\tau} + 4A_f C_d^2\right] \qquad (5.17)$$

The pre-factor $\left(e^2/8\right)$ normalizes the noise to signal gain. The first term is a combination of all the noise currents which increases with shaping time and has no dependence upon detector capacitance. The second term is a combination of all the noise voltages. Unlike the previous term, the second term decreases with shaping time and increases with detector capacitance. The third term represents the $1/f$ noise as a voltage source and increases with sensor capacitance. The $1/f$ noise is independent of the shaping time because the total noise of the $1/f$ source depends on

the ratio of the lower to upper cutoff frequencies, not on the absolute noise bandwidth. If τ_i and τ_d are scaled by the same factor, this ratio stays constant.

The equivalent noise charge as a function of shaping time is shown in figure 95. At short shaping times, the voltage noise is noticeably the dominant factor, while at long shaping times the current noise is the dominant factor. The equivalent noise charge is at its minimum when the current and voltage noise contributions are equal. The minimum noise is flattened by the $1/f$ noise. An increase in the sensor capacitor will increase the noise voltage contribution and shift the minimum to longer shaping times. In addition, it will increase the minimum noise.

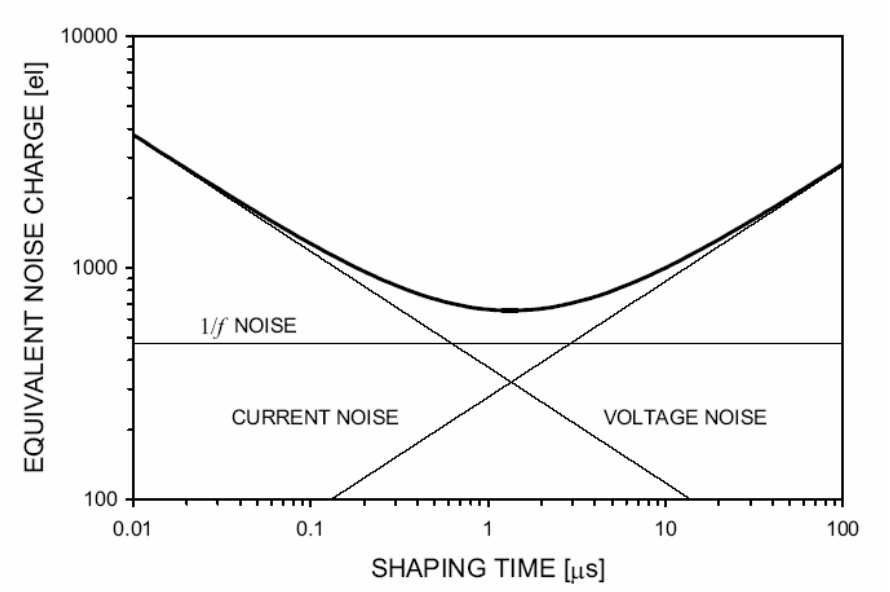


Figure 95: Equivalent Noise Charge vs. Shaping Time [2]

Noise can be decreased by reducing the detector capacitance and leakage current. Noise reduction can also be accomplished by careful selection of all resistances in the circuit and choosing the optimum time constant for the pulse shaper. By reducing the detector leakage current and increasing the bias resistor R_b, longer shaping times with lower noise are achieved.

The noise of a well designed amplifier depends mainly on the input transistor. Fast and high gain transistors are the most effective. In MOSFETS, the noise current contribution is very small. The equivalent input noise voltage is $e_n^2 \alpha 4kT/g_m$ where g_m is the transconductance which increases with operating current. Considering a specific operating current, the transconductance is increased if the channel length is reduced. In other words, scaling the feature size will cause a reduction in noise. At a given channel length, the noise is minimized when the device is operating at its maximum transconductance. To decrease the noise, the width of the device can be increased. Along with an increase in transconductance, the device input capacitance also increases. If the width of the device further increases, the reduction in noise is outweighed by an increase in total input capacitance. Optimum noise performance is obtained when the MOSFET's input capacitance is equal to the external capacitance which includes sensor plus stray capacitances.

Capacitive matching increases the power dissipation. The circuit can operate at significantly lower currents with just a minor increase in noise. Power dissipation is critical in large detector array sensors therefore MOSFETS are never operated at their minimum noise. It is best to find a compromise between power dissipation and minimum noise tradeoff.

5.6 Effect of Feedback on Noise Performance

It is very important to note that feedback does not improve the noise performance of the circuit. Considering the feedback network shown in figure 96(a), the input referred noise of the amplifier, A_1, is represented by a voltage source, V_n. It

is assumed that the feedback network is noiseless. The following relationship holds between the input and output.

$$V_{out} = (V_{in} + V_n)\frac{A_1}{1+\beta A_1} \qquad (5.18)$$

Using the above expression in (5.18), the circuit of figure 96(a) can be simplified to the circuit of figure 96(b). The overall noise of the circuit with the feedback network can still be represented by V_n. As can be observed, the input-referred noise voltage and current remain the same if the feedback network is noiseless. However, the previous statement is valid as long as the output of the circuit is the same quantity sensed by the feedback network.

In practice, the feedback network introduces noise to the circuit. The feedback network usually consists of resistors which introduce thermal noise in the circuit. As an example, figure 97(a) considers a feedback network realized by a resistive divider using R_E and R_F. The noise of the amplifier a is represented by equivalent input noise generators, $\overline{i_{ia}^2}$ and $\overline{v_{ia}^2}$, as shown in figure 97(b). Thermal noise in R_F and R_E are represented by the voltage sources $\overline{v_f^2}$ and $\overline{v_e^2}$. The equivalent input referred noise voltage and current are represented by $\overline{v_i^2}$ and $\overline{i_i^2}$, as shown in figure 97(c).

The equivalent input referred noise voltage is found by short circuiting the inputs of the circuits, shown in figures 97(b) and 97(c). The following relationship describes the effect of short circuiting the inputs:

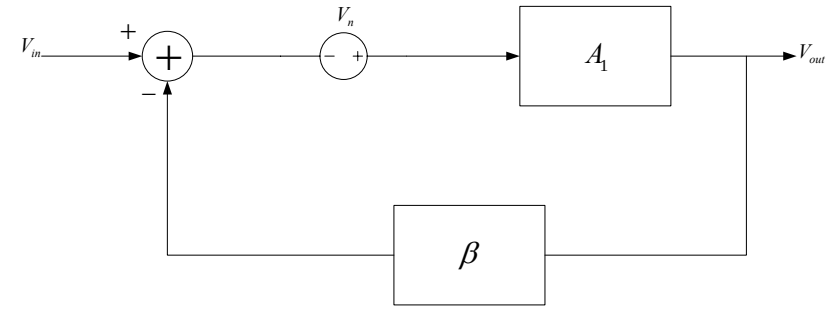
$$v_i = v_{ia} + i_{ia}R + \frac{R_F}{R_F + R_E}v_e + \frac{R_E}{R_F + R_E}v_f$$

$$R = R_F \| R_E$$

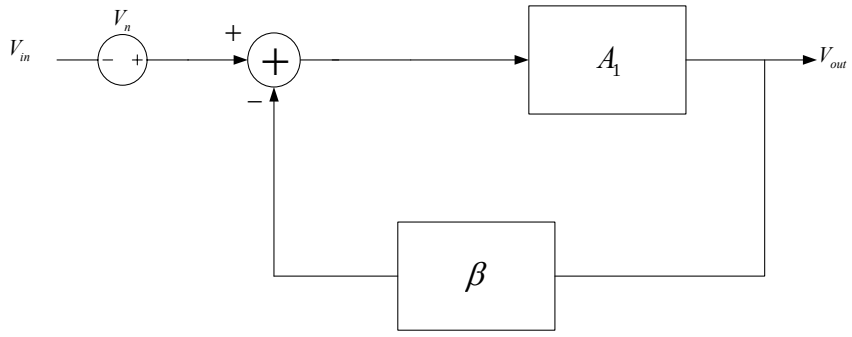
Assuming all noise sources in the circuit are independent and expressed as $\overline{v_e^2} = 4kTR_E\Delta f$ and $\overline{v_f^2} = 4kTR_F\Delta f$, the following relationship for the equivalent input-referred noise voltage can be characterized by (5.19).

$$\overline{v_i^2} = \overline{v_{ia}^2} + \overline{i_{ia}^2}R^2 + 4kTR\Delta f \qquad (5.19)$$

This expression in (5.19) describes the basic amplifier noise voltage plus two other terms. The second term is small and, therefore, can be neglected. However, the third term is the thermal noise of the resistive feedback network and is usually large.



(a)



(b)

Figure 96: Feedback in a Noisy Circuit

The input referred equivalent noise current is found by opening the inputs of the circuits shown in figures 97(b) and 97(c) which is given by $\overline{i_i^2} = \overline{i_{ia}^2}$.

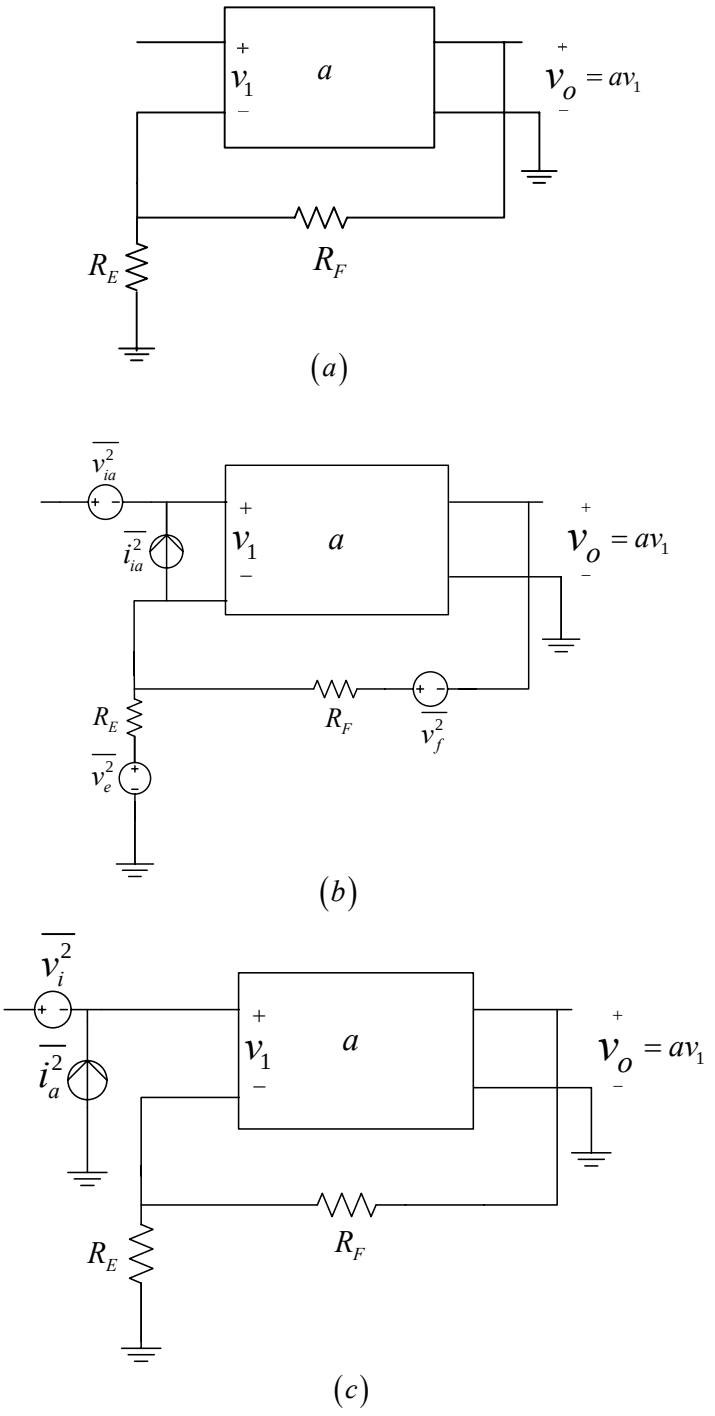


Figure 97: (a) Series-Shunt Feedback Circuit (b) Series-Shunt Feedback Circuit with Noise Sources (c) Equivalent Representation of (d) with Two Noise Sources

Chapter 6: Review of Previously Proposed Techniques for Noise Reduction in Sensor Arrays

6.1 Introduction

In this chapter, a review of the work previously done for noise reduction in capacitive sensors will be provided, and four different techniques for noise reduction in capacitive sensors will be described. The first three techniques reduce noise by precise measurement and feedback control [36]-[41]. The fourth technique accomplishes noise reduction by focusing upon the pre-amplifier/amplifier chain in the readout circuit [42]-[44].

To summarize four techniques appearing in the literature are reviewed. They are as follows:

1. Capacitive control
2. Bandwidth control
3. Charge control
4. Low noise pre-amplifier/amplifier chain

6.2 Capacitive Control

The capacitive control technique was first introduced by Fowler et al [36]. The process can be described in three steps. First of all, hard reset is performed on the capacitive sensor. An amplifier, called an error amplifier, is used in a feedback loop and connected to the sensor with a capacitor. The amplifier compares the output

of the sensor to a reference voltage, V_{ref}, and attenuates the noise on the capacitor node by keeping it as close as possible to the reference voltage. After this process is complete, the loop is opened, and the sensor can detect the signals again. As a result, the reset noise is reduced because the error amplifier compares the sensor voltage with a reference voltage. This of course assumes correlated noise sources of the sensor and reference nodes. Figure 98 shows a circuit implementing capacitive control.

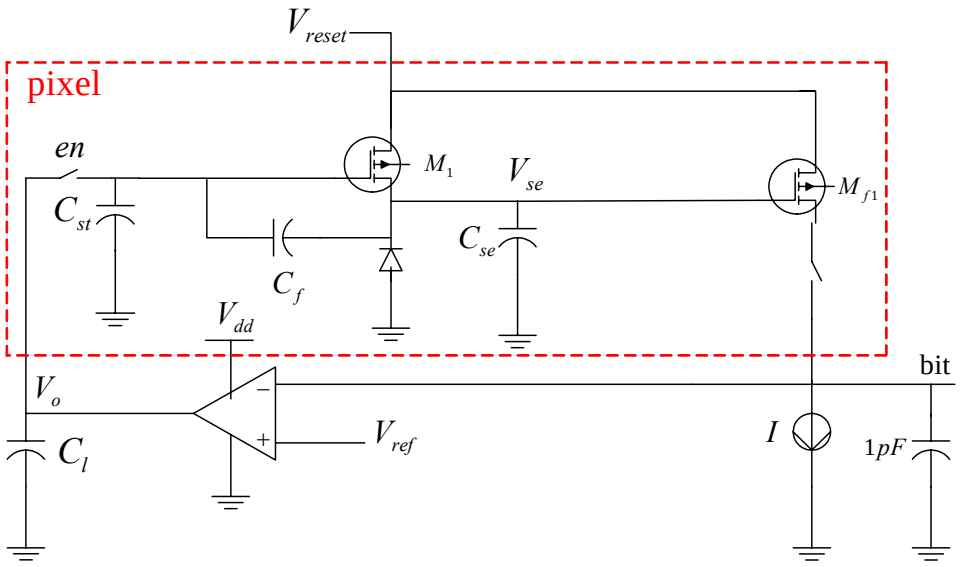


Figure 98: Capacitive Control Technique Schematic

Figure 99 shows the timing diagram for the capacitive control. Hard reset is performed between t_1 and t_2. The feedback loop is connected to the sensor capacitor, C_{se}, via the feedback capacitor, C_f, between t_3 and t_4 as shown in the timing diagram of figure 99. The duration defined by $t_1 - t_2$ is chosen such that the sensing node reaches its steady state, and $t_3 - t_4$ is chosen such that the feedback loop reaches

steady state during the noise reduction period. Also, t_3 is required to be larger than t_2.

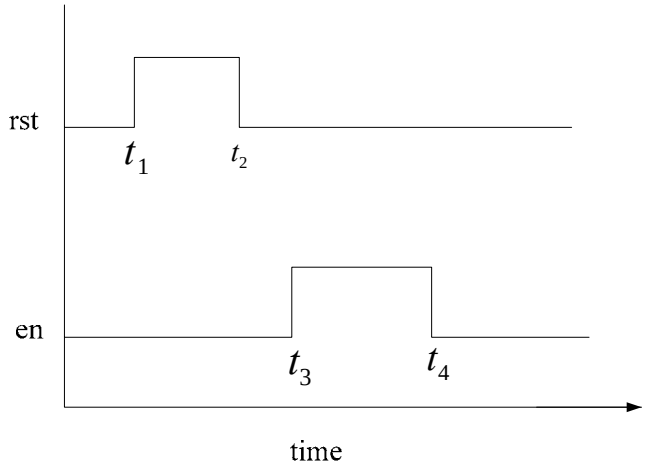


Figure 99: Timing Waveforms for the Capacitive Control Technique

Analogies can be used to help visualize the noise reduction technique. The analogy is shown in figures 100, 101 and 102. Although the analogy is far from perfect, considering how the noise reduction technique works, it will be mentioned for the sake of completeness. In each of these figures, two buckets of balls are connected together using a ramp. The balls represent the holes and their corresponding level represents the voltage of the bucket. Some use another analogy called the hydraulic analogy considering water and water vapor being the natural medium. However, only the analogy using the balls is described in this section.

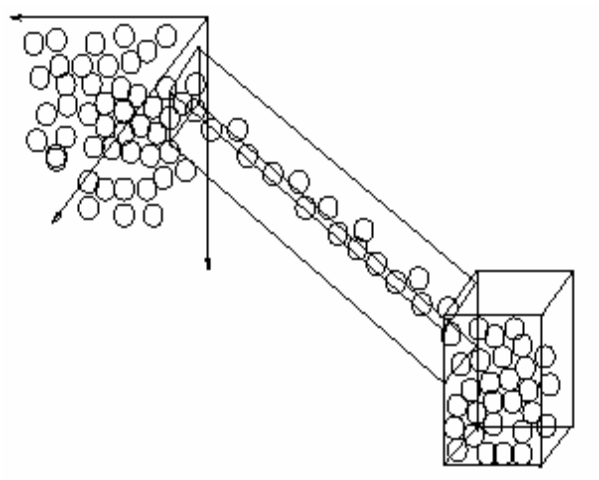


Figure 100: Analogy- High to Low Potential

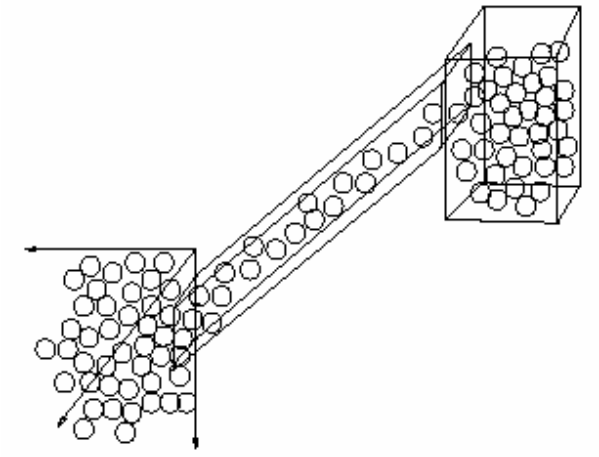


Figure 101: Analogy- Low to High Potential

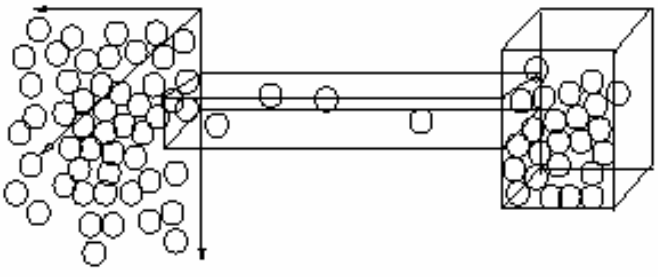


Figure 102: Analogy- No Potential Difference

In each of the figures, the bucket on the left hand side has an infinite volume and represents a perfect voltage source. The bucket on the right hand side has a finite capacity and represents a perfect capacitor. The ramp that connects the buckets signifies a finite resistance where the length divided by the width of the ramp is proportional to the resistance. In figure 100, the potential difference drives the balls from left to right. In figure 101, the potential difference between the buckets derives the balls from right to left. In figure 102, there is no potential difference between the buckets causing the balls to move from one bucket to the other just by diffusion. The analogy can even be used to describe the reset noise on the sensor capacitor. When the ramp is level, meaning the levels of balls in the two buckets are the same, the balls move from one bucket to the other due to their thermal motion. So at any time t, the number of balls in the bucket on the right hand side is a random variable. If at time $t = t_{sw}$, the width of the ramp is suddenly set to zero; the balls can not travel back and forth between the buckets anymore. Therefore, the number of balls in the right hand side bucket is suddenly frozen. The uncertainty in the number of balls in the right hand side bucket at $t > t_{sw}$ is analogous to the charge noise on the sensor capacitor after hard reset.

In this analogy, it is assumed that the sensor capacitor is a bucket with a finite number of balls and the feedback capacitor is another bucket used to either add or subtract balls to the sensor capacitor bucket.

After the hard reset, the number of balls in the sensor capacitor bucket is a random value. If the number of balls in the sensor capacitor bucket can be measured

to a sufficient accuracy, then the balls can be added or subtracted from the sensor bucket using the feedback capacitor bucket. This analogy is shown in figure 103.

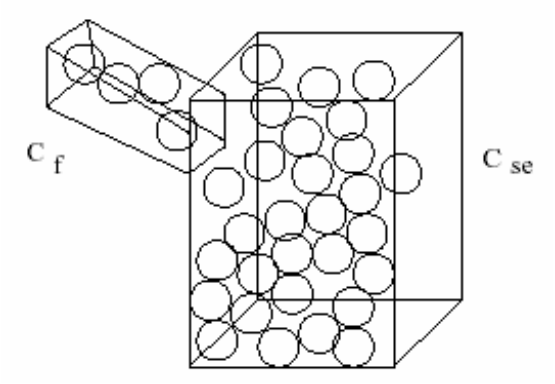


Figure 103: Analogy for the Capacitive Control Technique

The relative ratio of C_f to C_{se}, determines how well the balls in the sensor capacitor bucket can be controlled. If C_f is large enough to hold 2 balls then you can easily add or subtract one ball at a time from the sensor capacitor bucket. If C_f is twice as large as C_{se}, then we can either fill or empty C_{se} completely. As a result, less control is obtained over the final number of balls in the sensor capacitor bucket. One of the most important parts of designing any circuit that uses capacitive feedback to reduce the noise is finding the optimal ratio of $\frac{C_f}{C_{se}}$.

At this point, a review of the simulation results presented for the capacitive control noise reduction technique by Fowler et al is provided. The measure of noise reduction techniques used is the reset noise reduction factor (RNRF) which is defined as the hard reset noise power divided by the active reset noise power. The simulation results presented were generated using HSPICE. A 0.18 μm CMOS process was used in the simulations. The simulations were performed with $V_{dd} = 2.8$ V and

$V_{reset} = 2.0$ V at $T = 25$ C$^{\circ}$. The reset period was held constant. The fixed pattern noise is not taken into account in these simulations. Figure 104 shows the input and output waveforms for the circuit in figure 98.

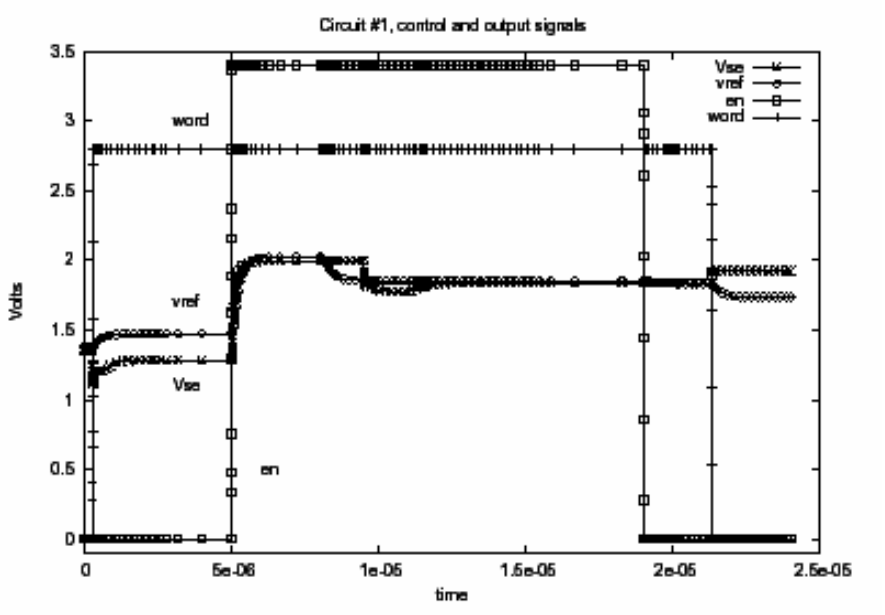


Figure 104: Input and Output Waveforms for the Capacitive Control Technique Circuit [41]

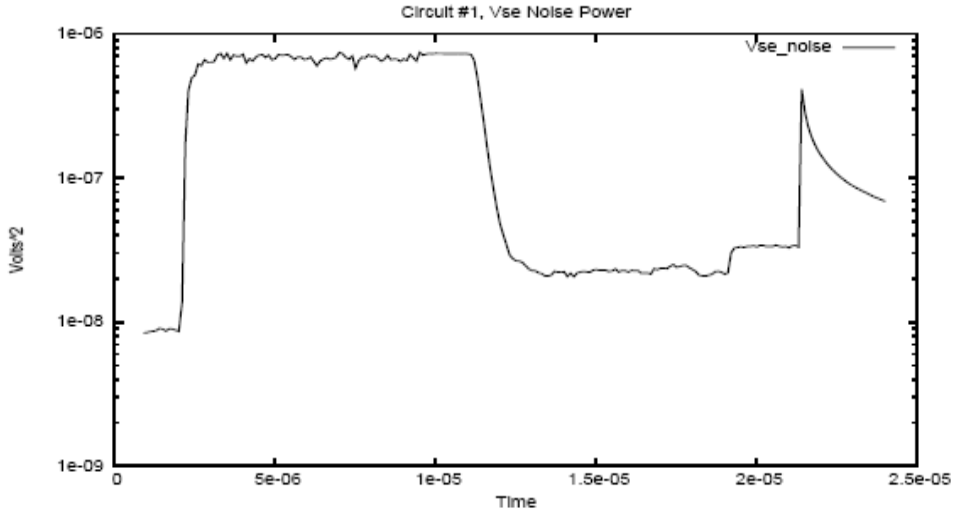


Figure 105: Transient Noise Waveforms for the Capacitive Control Technique [41]

Table 3 gives all the parameters used for capacitors, transistors, and amplifiers in figure 98. The transient noise simulation of the capacitive control circuit is shown in figure 105. The noise voltage on the sensor capacitor corresponding to the hard reset at 10ms is $0.72\mu V^2$. The noise power after $20\mu s$ is $0.33nV^2$. Therefore, the RNRF of the circuit is $7.2/0.331 = 21.8$.

Component/Parameter	**Value**
C_l	0.3pF
C_f	0.4fF
C_{se}	5.4fF
C_{st}	5fF
$M_1, W/L$	$0.4\mu m/0.6\mu m$
M_1, V_{th}	0.45 V
$M_{f1}, W/L$	$0.7\mu m/1.2\mu m$
M_{f1}, V_{th}	0.45 V
M_{f1}, transconductance	$21.3\mu S$
M_{f1}, body effect conductance	$6.2\mu S$
M_{f1}, output conductance	$49nS$
Opamp transconductance	$24.5\mu S$
Opamp output conductance	$84.7nS$

Table 3: Capacitive Control Technique Circuit Parameters [41]

6.3 Bandwidth Control

Another technique to reduce the reset noise is using bandwidth control. This technique uses a feedback loop to directly attenuate the thermal noise of the reset transistor. It was first described by Loose et al. [37] Bandwidth control is a two step process. The circuit that uses bandwidth control to reduce the reset noise is shown in figure 106. In the first step, the sensor capacitor is hard reset. In the second step, an error amplifier is connected to the sensor capacitor in a feedback loop using a time varying resistor. The time varying resistor is increased until the bandwidth of the amplifier is larger than the noise bandwidth of the resistor. The bandwidth of the time varying resistor is approximately $\frac{1}{\left(4r\left(t\right)\left(C_{se}+C_{f}\right)\right)}$. The time varying resistor that connects the feedback amplifier to the sensor capacitor must be disconnected by the end of the reset period since $r\left(t\right)\to\infty$ as $t\to\infty$. The timing waveforms for the models are shown in figure 107.

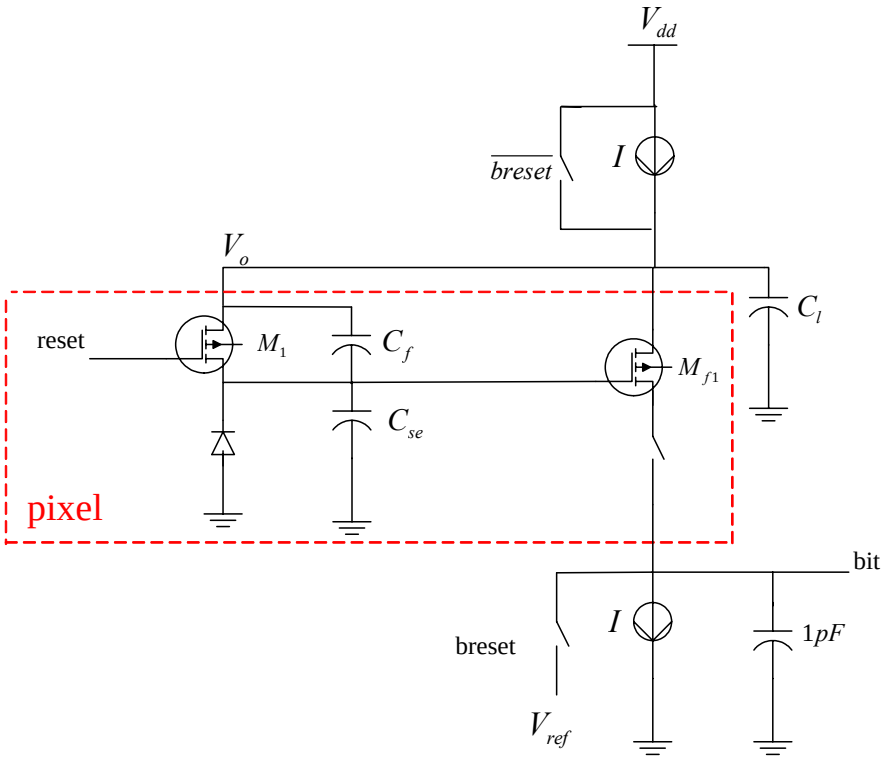


Figure 106: Bandwidth Control Technique Circuit Schematic

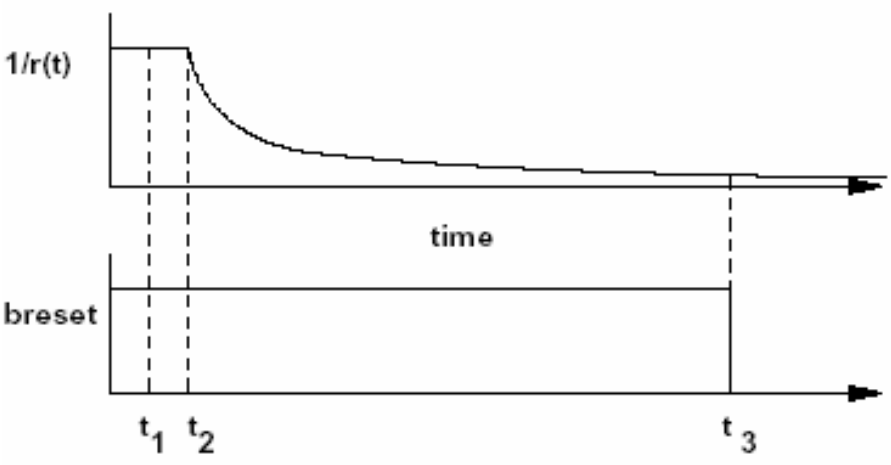


Figure 107: Timing Control Transient Waveforms [41]

The analogy used to help visualize the noise reduction technique will be now considered for bandwidth control. This analogy is shown in figure 108. Just as in last section, assume that the sensor capacitor C_{se} is realized as a bucket that contains a

finite number of balls. The resistance, $r(t)$, is assumed to be a ramp that connects the sensor capacitor, C_{se}, to a bucket that contains an infinite number of balls. After hard reset, the number of balls in the sensor capacitor bucket is some random value. Assuming we can measure the number of balls in the C_{se} bucket to a good accuracy while reducing the width of the ramp, the difference in the number of balls in the C_{se} bucket and infinite bucket can be used to control the number of balls in the sensor capacitor bucket. For example when the width of the ramp is wide enough for one ball to be added or subtracted from the sensor capacitor bucket, the slope of the ramp can be used to control the number of the balls in the C_{se} bucket. It has to be mentioned that the slope of the ramp is actually the difference between the levels of balls in the buckets which corresponds to the voltage difference between the two buckets as defined before. So if we can adjust the ramp faster than the balls can jump on to or fall off the ramp due to their thermal motion the uncertainty of the number of balls in C_{se} can be reduced.

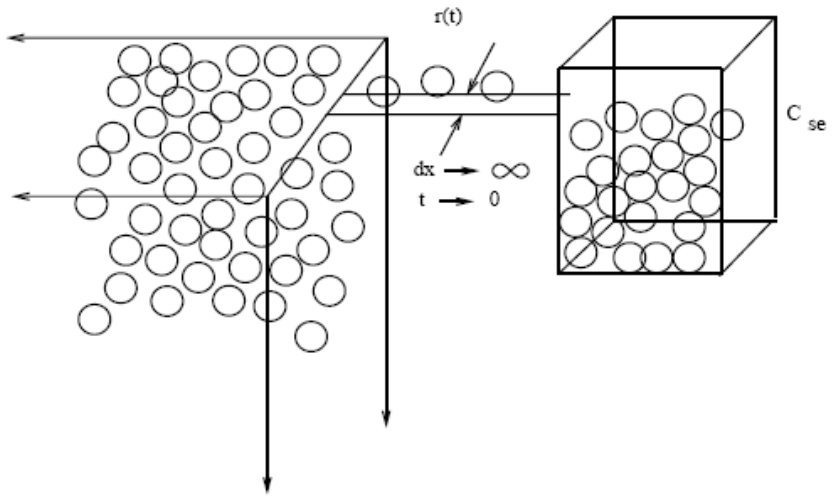


Figure 108: Analogy for the Bandwidth Control Technique

In this case, determining the best waveform for $r(t)$ as a function of time is one the most important factors in the design. The width of the ramp as a function of time is what defines the waveform of $r(t)$. Also, it is required to be able to measure the charge stored on C_{se} accurately and change $r(t)$ accurately in this technique. The input and output waveforms for this noise reduction technique are shown in figure 109. The circuit parameters for the circuit shown in figure 106 are shown in table 4. A transient noise simulation for the bandwidth control circuit is shown in figure 110. The hard reset noise voltage power on the sensor capacitor at $5\mu s$ is approximately $0.4\mu \mathrm{V}^2$. This result corresponds to about 60% of the predicted hard reset value $\frac{kT}{C_{se}+C_f}$. The noise power after $25\mu s$ is $68n\mathrm{V}^2$. Therefore, the RNRF of this circuit is $6.5/0.68 = 9.5$.

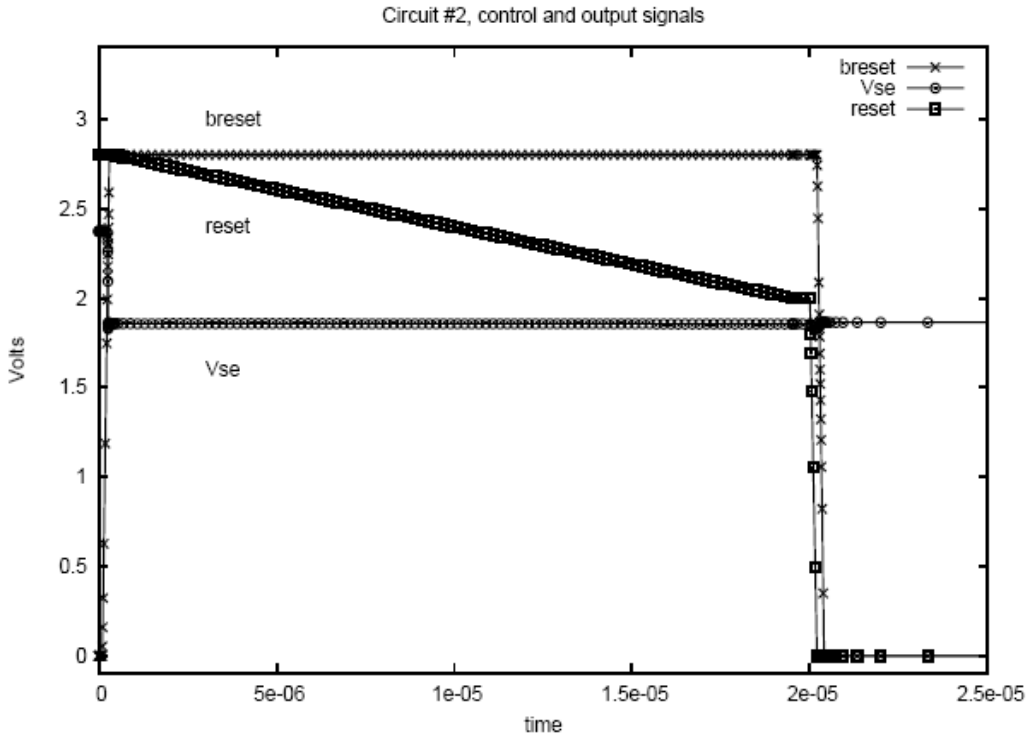


Figure 109: Input and Output Waveforms for the Bandwidth Control Technique [41]

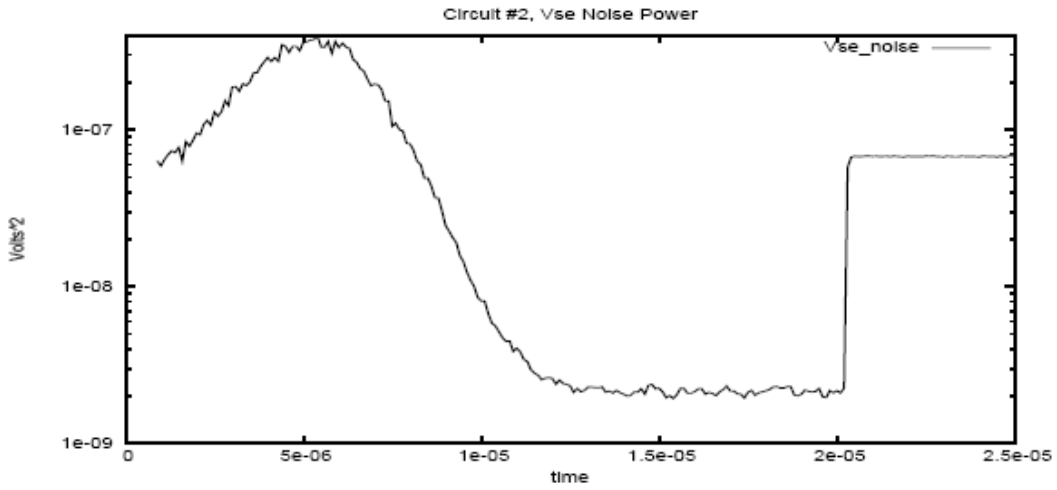


Figure 110: Transient Noise Waveforms for the Bandwidth Control Technique [41]

Component/Parameter	**Value**
C_l	0.3pF
C_f	0.4fF
C_{se}	6fF
$M_1, W/L$	$0.42\mu m/0.6\mu m$
M_1, V_{th}	0.45V
$M_{f1}, W/L$	$1.2\mu m/0.5\mu m$
M_{f1}, V_{th}	0.45V
M_{f1}, transconductance	$36.2\mu S$
M_{f1}, body effect conductance	$8.3\mu S$
M_{f1}, output conductance	$360nS$
v_{ref}	1.0V

Table 4: Simulation Parameters for the Bandwidth Control Technique Circuit [41]

6.4 Charge Control

Charge control reduces reset noise by determining when to stop charging the sensor capacitor after the hard reset. This technique was first introduced by Lee et al [38]. In charge control, the reset noise in the sensor capacitor is reduced in three steps. First a hard reset is done. After a conventional hard reset operation, a current source is connected to the sensor capacitor. The current source discharges the sensor capacitor node until it reaches a reference voltage, V_{ref}. When the voltage across the sensor capacitor falls below the reference voltage, the current source is disconnected from the capacitive sensor. The schematic of a circuit that utilizes charge control to reduce the reset noise of the capacitive sensor is shown in figure 111.

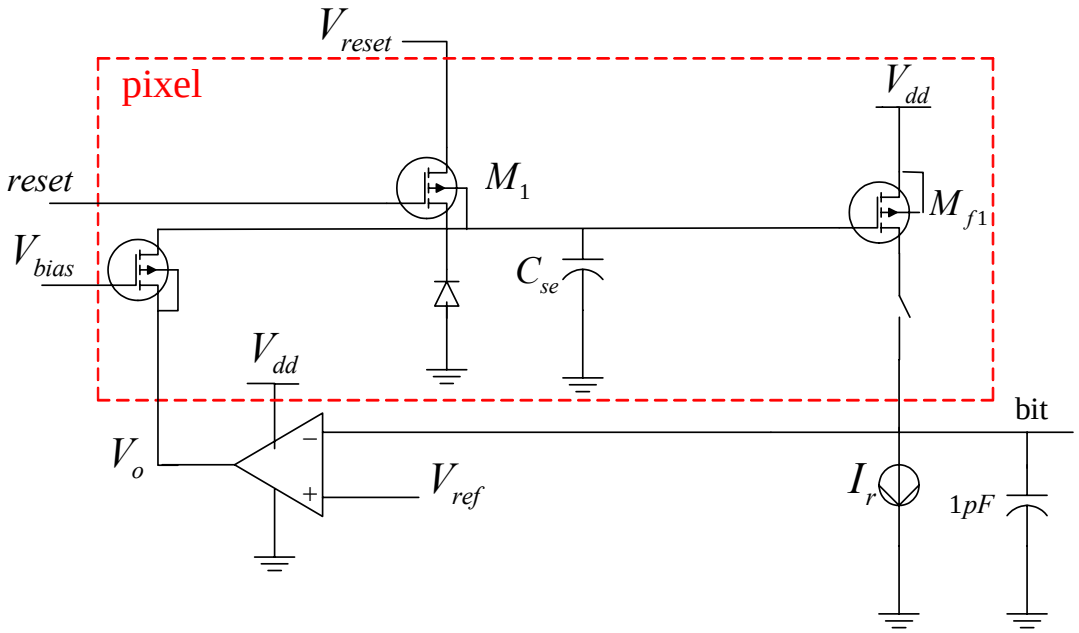


Figure 111: Charge Control Technique Circuit Schematic

The input referred noise of the amplifier, $V_{n1}(t)$, is assumed to be a white Gaussian random process with zero mean and variance $\sigma_{V_{n1}}^2$. The reset current source, I_r, is implemented using a transistor that operates in the subthreshold regime. The current source is assumed to have a shot noise given by a two sided power spectral density of $qI_R\ A^2/Hz$. Ignoring the output impedance of the transistor, the noise power spectral density of the sensor capacitor node voltage fluctuation is given by $qI_R/(2\pi f C_{se})^2\ V^2/Hz$. The noise power spectral density is concentrated at the low frequencies. If the bandwidth of the feedback amplifier is high enough to follow the voltage fluctuation of the capacitive node during discharge, reset noise reduction is achieved.

Using the same analogy used for the previous noise reduction techniques, the charge control technique can also be visualized. The capacitive sensor, C_{se}, is a bucket which has a finite number of balls. $I_r(t)$ is a stream of balls that fall into the sensor capacitor bucket. This analogy is shown in figure 112. It assumes that after hard reset C_{se} is filled with a fixed number of balls, n. If the number of balls in C_{se} can accurately be measured fast enough, $I_r(t)$ can switch out of the circuit such that the number of balls in C_{se} is exactly n. It is assumed that the speed at which $I_r(t)$ can be switched out of the circuit is much faster than the average rate that the balls fall into C_{se}. In order to have a good design in this case, three things should be taken into account: accurate measurement of the number of balls in C_{se}, speed at which $I_r(t)$ is switched out of the circuit, and the magnitude of $I_r(t)$.

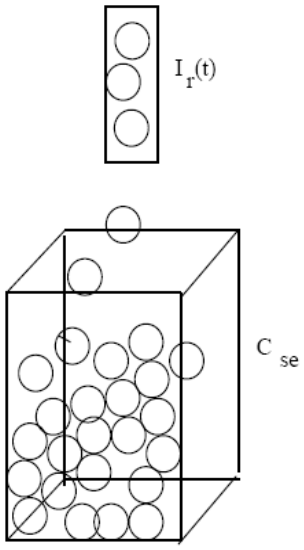


Figure 112: Analogy for the Charge Control Noise Reduction Technique

The input and output waveforms for this noise reduction technique are shown in figure 113. The circuit parameters for the circuit shown in figure 111 are shown in table 5. The transient noise simulation for the bandwidth control circuit is shown in figure 114. The noise power after $20\mu s$ is $0.1\mu V^2$. Therefore, the RNRF of this circuit is $0.62/0.1 = 6.2$.

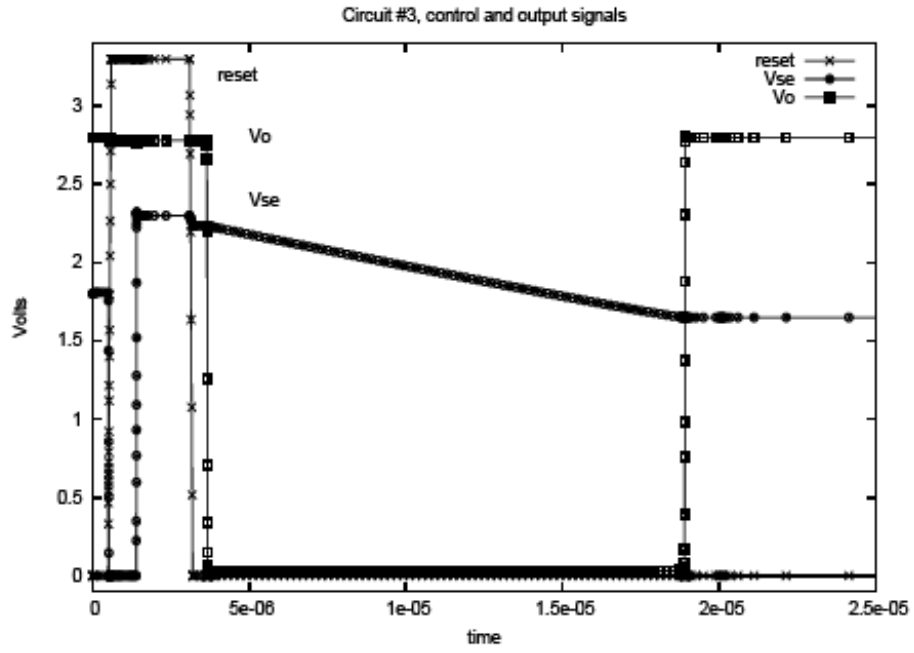


Figure 113: Input and Output Transient Waveforms for the Charge Control Technique [41]

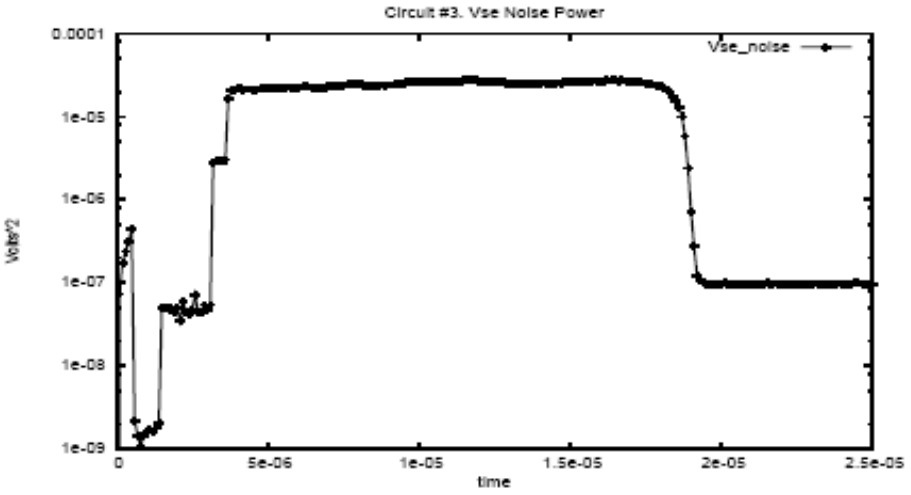


Figure 114: Transient Noise Waveform for the Charge Control Noise Reduction Technique [41]

Component/Parameter	**Value**
C_l	0.3pF
C_f	0.4fF
C_{se}	6fF
$M_1, W/L$	$0.42\mu m/0.6\mu m$
M_1, V_{th}	0.45V
$M_{f1}, W/L$	$1.2\mu m/0.5\mu m$
M_{f1}, V_{th}	0.45V
M_{f1}, transconductance	$36.2\mu S$
M_{f1}, body effect conductance	$8.3\mu S$
M_{f1}, output conductance	$360nS$
v_{ref}	1.0V
I_r	0.23nA
*Comp*1, gain bandwidth	167MHz
*Comp*1, DC gain	2311
*Comp*1, Input referred noise	$5.79\,nV^2$

Table 5: Component Parameters for the Charge Control Circuit [41]

6.5 Low Noise Pre-amplifier/Amplifier Chain

The idea of a low noise pre-amplifier/amplifier chain to reduce the noise in capacitive sensors was first introduced by Cook et al [42]-[44]. The VLSI readout is designed to work with indium bump bonding to a CdZnTe pixel detector. Each pixel is read out by a self-triggering signal processing chain which includes a pre-amplifier, shaping amplifier, and peak detect/hold circuit. The schematic of the simplified pulse processing chain is shown in figure 115. The signal is amplified in the first two low-noise pre-amplifier stages. In order to have a low noise operation, long restoration time constants are necessary. This can be achieved by using large resistance in the feedback loop and implemented using active circuitry. The shaping of the signal occurs in the third and fourth stages. Shaping is necessary for optimum noise performance. The peak detect/hold circuitry includes a comparator and the minimum logic to detect and hold the signal peak for off-chip analog-to-digital conversion.

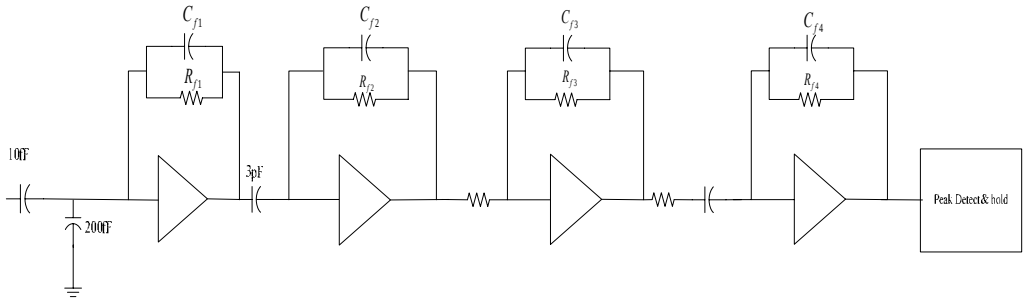


Figure 115: Simplified Signal Processing Chain Schematic

The detailed schematic of the pre-amplifier/amplifier section is shown in figure 116. In this circuit, the detector pixel is simulated using an on-chip capacitor and a leakage current source representing the detector leakage current. Cook et al [42]-[44] mentioned having plans for a second prototype chip that can be bonded to a detector.

The pre-amplifiers, A_1 and A_3, shown in the figure are folded cascode single ended differential amplifiers. In this case, the input amplifier A_1 is designed to work with a low input capacitance of 200 fF. The large feedback resistance in the first stage is implemented using a PMOS transistor, M_1, biased in sub-threshold by amplifier, A_2, with a gain of one half.

The large resistance in the second stage feedback is implemented using a combination of a smaller value resistor, current divider and amplifier. All of the resistances, R_2 through R_6, are implemented this way. For example, the 2 gΩ resistor, R_2, is implemented using a 25 $k\Omega$ resistor working together with amplifier, A_4, and current mirrors and dividers M_3, M_4, M_5, and M_6. The amplifier, A_4, holds one side of the 25 $k\Omega$ resistor at a constant voltage converting the signal at the output of A_3 to a current. This current is divided by the current mirrors/dividers to implement the desired feedback resistance.

Cook et. al. [42]-[44] reported that the noise performance was acceptable but not as good as predicted by SPICE. For the 40usec peak time settling and 0.1 pA detector leakage current, the measured noise referred to the input was approximately 50 electrons or 0.25keV FWHM energy loss in CdZnTe. This could be due to the possibility that the flicker noise coefficients for the PMOS and NMOS transistors used in SPICE are not the same as these on the particular prototype chip used. The signal-to-noise ratio for the amplifier was $60 V/V$.

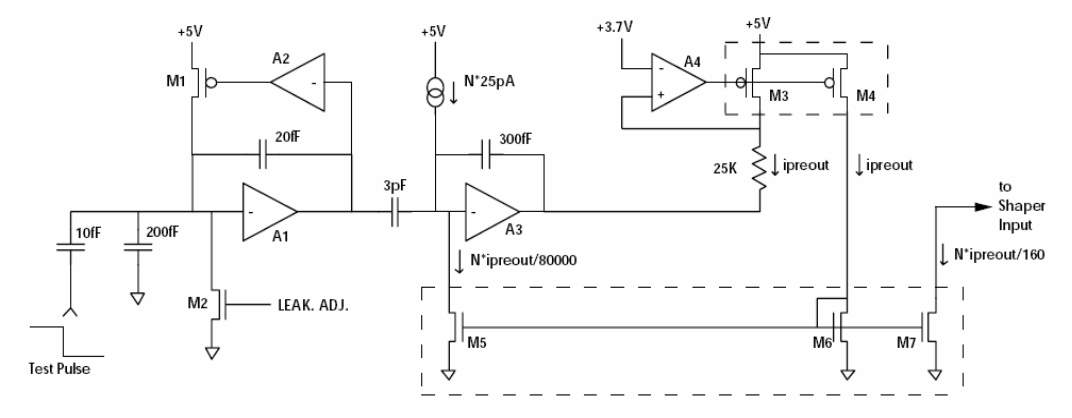


Figure 116: Detailed Schematic of the Pre-amplifier/Amplifier Section [42]

Chapter 7: A Novel Noise Reduction Technique for High Capacitance Sensor Arrays

7.1 Introduction

The past two decades have witnessed a considerable improvement in image sensors and detectors, aimed at low noise and clear signal output. Detectors and sensors have become routine in high energy physics applications, leading to low noise electronic read-out arrays - an indispensable component in a broad range of applications such as space missions, synchrotron light sources, and medical imaging.

NASA is one of the world's leading agencies in integrating new sensor technologies for earth resource management surveillance and astronomy. Innovative signal processing chain electronics are required to fully exploit the potential of these devices. Many sensing circuits in detectors, such as CdZnTe detectors used by NASA for gamma ray detection, depend upon accumulating charge on a capacitor. The charge uncertainty on the capacitor when it is reset to a reference voltage causes noise, reset noise, as a result of shot and thermal processes. Reset noise is enhanced by the sensing capacitor. Therefore, low noise readout circuitry capable of driving a high input capacitance is essential for detector systems. Our goal is to provide a flexible signal processing chain for high capacitance sensors. This innovative signal processing chain is aimed at increasing the signal-to-noise ratio in pixel detectors and sensors. The resulting system can be used in wide variety of detectors with a range of

applications such as random access pixel detectors, fully depleted CCDs, hybrid detector systems, and superconducting detector arrays.

In this chapter, a noise reduction technique for high capacitance sensor arrays is introduced. Here, we are dealing with charge sensing sensors, where the charge is stored on the sensor capacitor node. This technique is a low noise signal processing chain that consists of a pre-amplifier/amplifier chain. The low noise pre-amplifier/amplifier chain is used as the signal processing readout circuitry for high capacitance sensors. This is shown in figure 117.

The requirements for this amplifier include (but are not limited to):

1. Low noise
2. The ability to drive a high input capacitance
3. High gain
4. High bandwidth

The most important factor to consider is the reduction of the pre-amplifier/amplifier noise without inflicting any limitations on the gain or the bandwidth as far as the signal is concerned. A folded cascode amplifier is used for amplification. The amplifier is described in more detail in section 7.2. The amplifier needs to be able to drive a high input capacitance which is the case in sensor detectors.

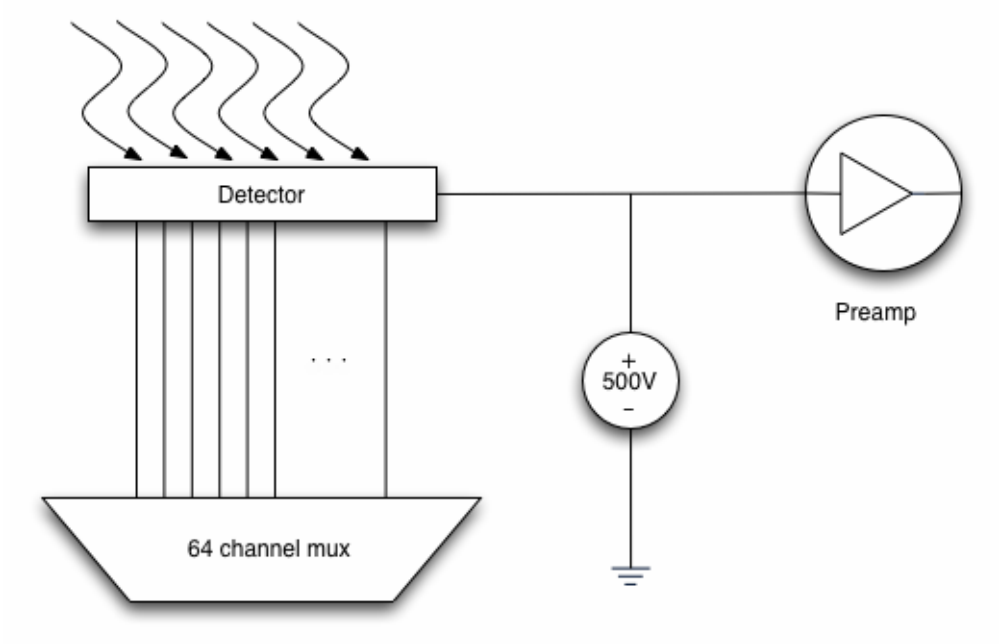


Figure 117: Pre-Amplifier/Amplifier Chain used in a Multiplexed Detector

7.2 Pre-amplifier/Amplifier Readout Circuitry

A low noise pre-amplifier/amplifier readout circuitry is designed for the pixel detector system. The amplifier has two stages. Each stage is a folded cascode amplifier with a class AB push-pull output stage. Figure 118 shows the block diagram of the pre-amplifier/amplifier chain. Figure 119 portrays the detailed schematic of the pre-amplifier/amplifier readout block diagram previously shown in figure 118. The two stages are exactly identical. The circuit parameters for the amplifiers are shown in table 6. Each amplifier consumes 100 μA . The power dissipation for each amplifier is 330 μW .

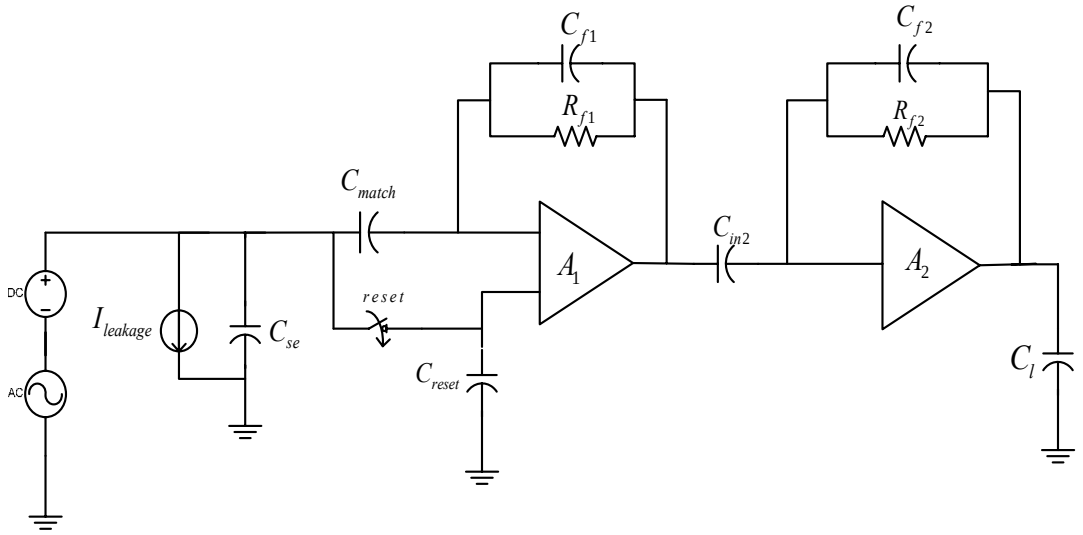


Figure 118: Pre-amplifier/Amplifier Chain Block Diagram

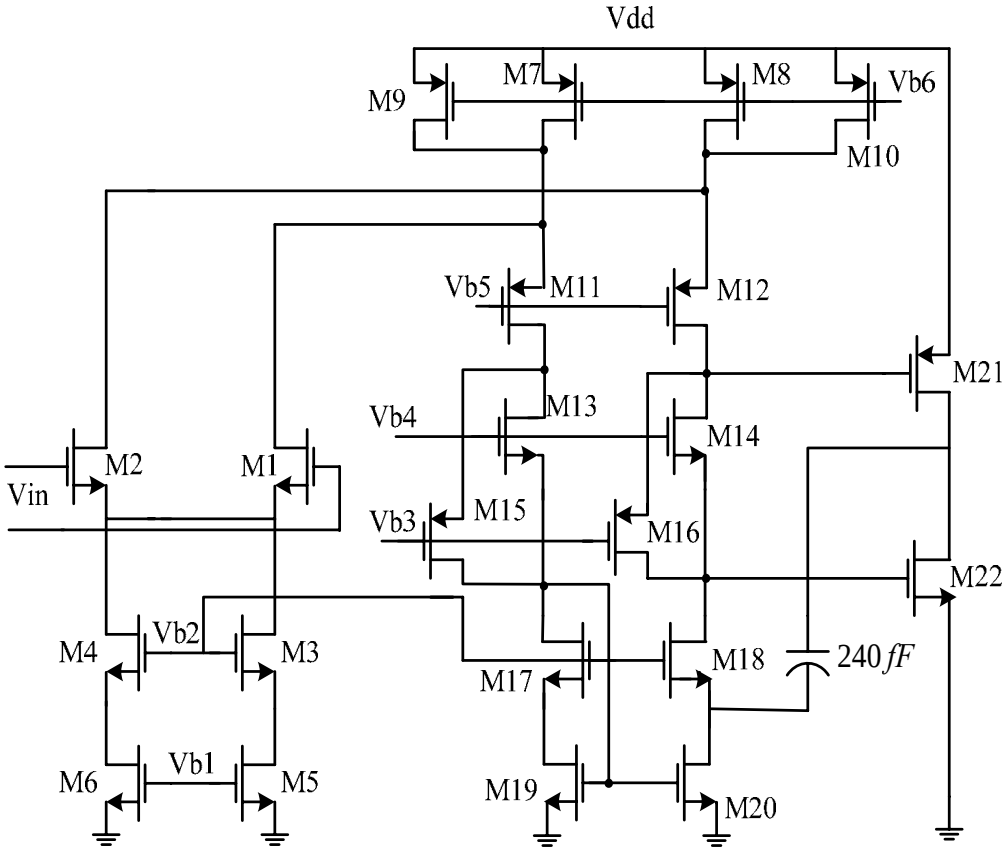


Figure 119: Folded Cascode Amplifier Schematic for Each Stage

Transistor	**Size** (W/L)
M_1, M_2	25/2
M_3, M_4	25/2
M_5, M_6	25/2
M_7, M_8, M_9, M_{10}	50/2
M_{11}, M_{12}	50/2
M_{13}, M_{14}	25/2
M_{15}, M_{16}	15/2
M_{17}, M_{18}	25/2
M_{19}, M_{20}	25/2
M_{21}	330/1
M_{22}	50/1

Table 6: Amplifier Circuit Parmeters

A capacitor and a leakage current source are used for electronic simulation of the detector circuit. The detector leakage current is simulated with a current source represented by a transistor biased in sub-threshold, while the detector capacitance is simulated by a $100\,nF$ capacitor. The capacitor used for simulating the detector is much higher than the capacitor used by Cook et al [42]. Cook et al used a 200 *fF* capacitor. This capacitor is more than 5 orders of magnitude smaller than the capacitor employed in this scenario at the amplifier input. In a case dealing with such a high sensor capacitance, the signal is the voltage stored on the sensor capacitance.

The large sensor capacitance increases the charge uncertainty on the sensor node after reset. Due to the fact that a large capacitance enhances the reset noise component of the system's signal-to-noise-ratio, innovative techniques need to be incorporated in readout arrays to increase the signal-to-noise ratio. In order to reduce the higher reset noise at the amplifier input, correlated double and capacitive matching are used.

Correlated double sampling is used at the amplifier input by taking advantage of the fact that the amplifier can perform correlated double sampling without the need of additional circuitry. Correlated double sampling can be incorporated into the pre-amplifier/amplifier chain by adding only a reset switch and capacitor. In order to implement correlated double sampling, a reset switch is used which is closed during the reset cycle. During the reset cycle, the reset noise is stored on the capacitor used at the input for this purpose. During the signal cycle, the reset switch is opened, and the amplifier cancels the reset noise while amplifying the signal. By taking two samples and subtracting them, any noise source that is correlated to the two samples will be ideally removed or minimized. Even a slowly varying noise source that is not correlated completely will be reduced in magnitude. Noise introduced at the output of the pre-amplifier/amplifier chain consists primarily of *kTC* noise from the charge sensing node. The *kTC* noise will be removed by correlated double sampling. Low frequency noise sources will be attenuated by correlated double sampling.

Capacitive matching is also used at the amplifier input to reduce the reset noise at the sensor node. This method calls for an additional capacitor to be placed at the input of the pre-amplifier/amplifier chain. This capacitor must be equivalent to

the capacitance seen at the pre-amplifier input. The capacitance seen at the input of the pre-amplifier is the feedback capacitor, C_{f1}, multiplied by the open loop gain of the pre-amplifier, A_1. The capacitor referred to as C_{match} in figure 118 is used at the amplifier input for the purpose of matching, in order, to increase the signal-to-noise ratio at the input of the pre-amplifier/amplifier chain. The matching capacitor is chosen to be equal to the product of C_{f1} and A_1. By using capacitive matching, we are following the principle of impedance matching which maximizes the signal power transmission into the amplifier system.

The Low noise pre-amplifier/amplifier readout circuitry shown in figures 118 and 119 is designed and simulated in 0.13 μm CMOS8RF IBM process technology using Cadence Spectre. In the next section the simulation results for the pre-amplifier/amplifier readout circuitry is presented and analyzed.

7.3 Simulation Results

The pre-amplifier/amplifier chain is designed and simulated in 0.13 μm CMOS8RF IBM process technology using Cadence Spectre. It can be observed from the simulation results that the pre-amplifier/amplifier chain with correlated double sampling has a higher signal-to-noise ratio than the pre-amplifier/amplifier chain that does not employ correlated double sampling or capacitive matching.

In order to show the effect of capacitive matching on the performance and the to demonstrate it's advantages, two different scenarios are used. One scenario is the pre-amplifier/amplifier chain using only the correlated double sampling technique and the other is the same signal processing chain with both the correlated sampling and capacitive matching. The two results are then compared to illustrate the signal-

to-noise ratio improvement due to capacitive matching along with correlated double sampling.

In the first setup, the matching capacitance is not used at the input of the pre-amplifier in the readout circuitry. The input to the pre-amplifier/amplifier chain from the capacitive sensor is simulated by a pulse with a pulse width of 0.5μs and amplitude of $1\,mV$. The pulse contains a DC offset of $1.8\,V$ to provide the necessary input DC bias voltage for the signal processing chain. In this case the pre-amplifier/amplifier frequency response is shown in figure 120 and it has a gain of $40\,dB$. Each stage provides a gain of $20\,dB$. The bandwidth of the pre-amplifier/amplifier circuit ranges from $1\,kHz$ to $10\,MHz$. The transient input and output waveforms for the readout circuitry are shown in figure 121. The equivalent output noise of the signal processing chain is shown in figure 122. The amplifier has a maximum equivalent output noise of $145\mu V/\sqrt{Hz}$. This is equivalent to approximately 170 electrons. The signal-to-noise ratio for the pre-amplifier/amplifier chain is about $680\,V/V$. This signal-to-noise ratio is 10 times larger than the signal-to-noise ratio for the amplifier designed by Cook et. al [42].

The results for when capacitive matching is used without correlated double sampling are shown in figure 123 and 124. Figure 123 shows the frequency response. In this case the pre-amplifier/amplifier has a gain of $63\,dB$. Figure 124 shows the equivalent output noise of the pre-amplifier/amplifier chain. The signal-to-noise ratio in this case is approximately 500 V/V. This signal-to-noise ratio is 10 times larger than the signal-to-noise ratio for the amplifier designed by Cook et. al [42].

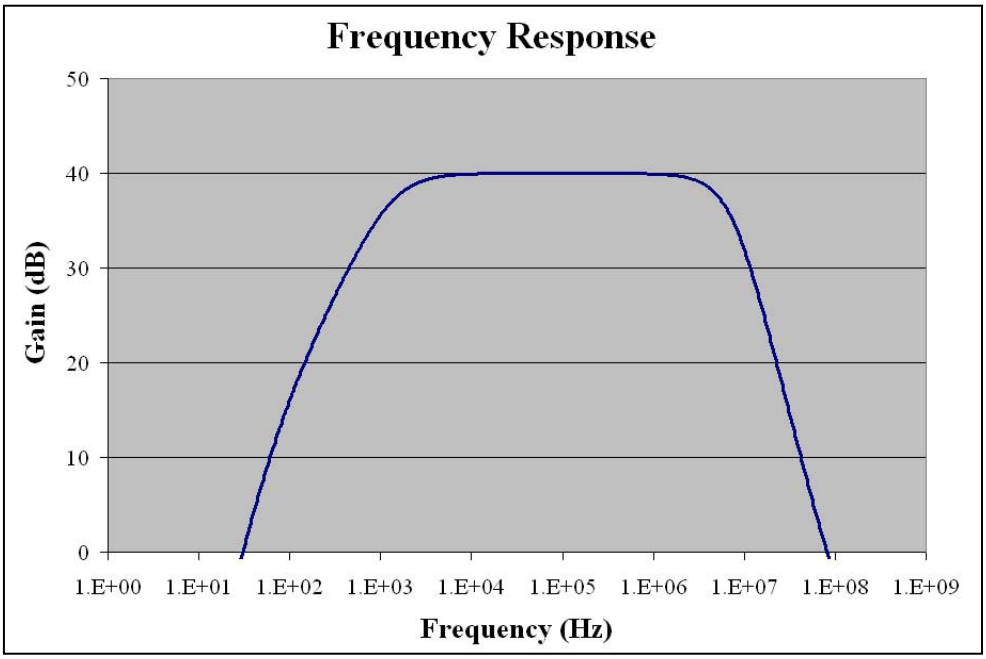
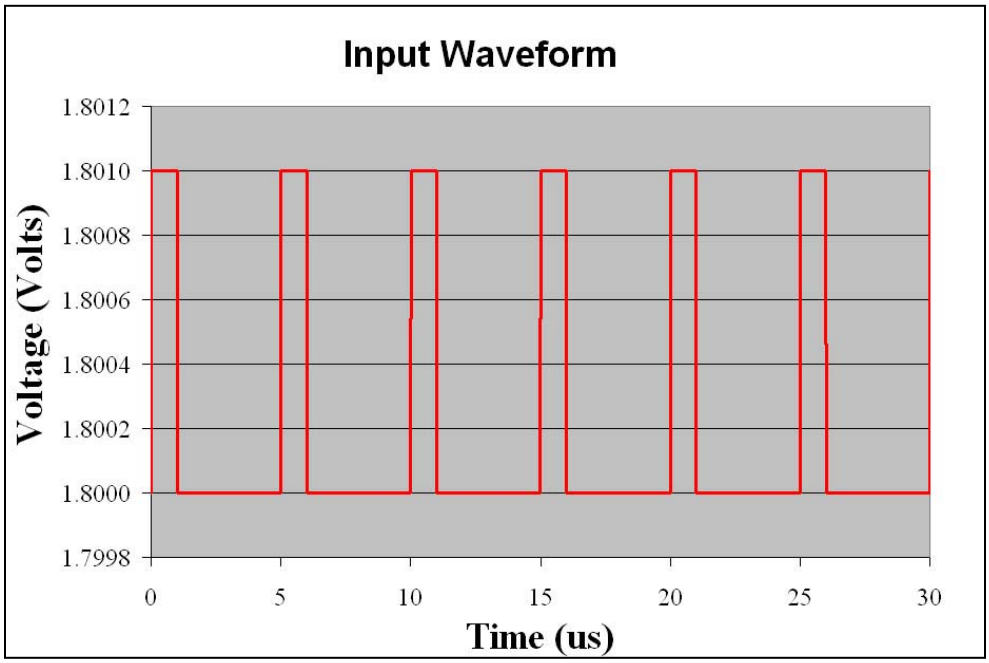
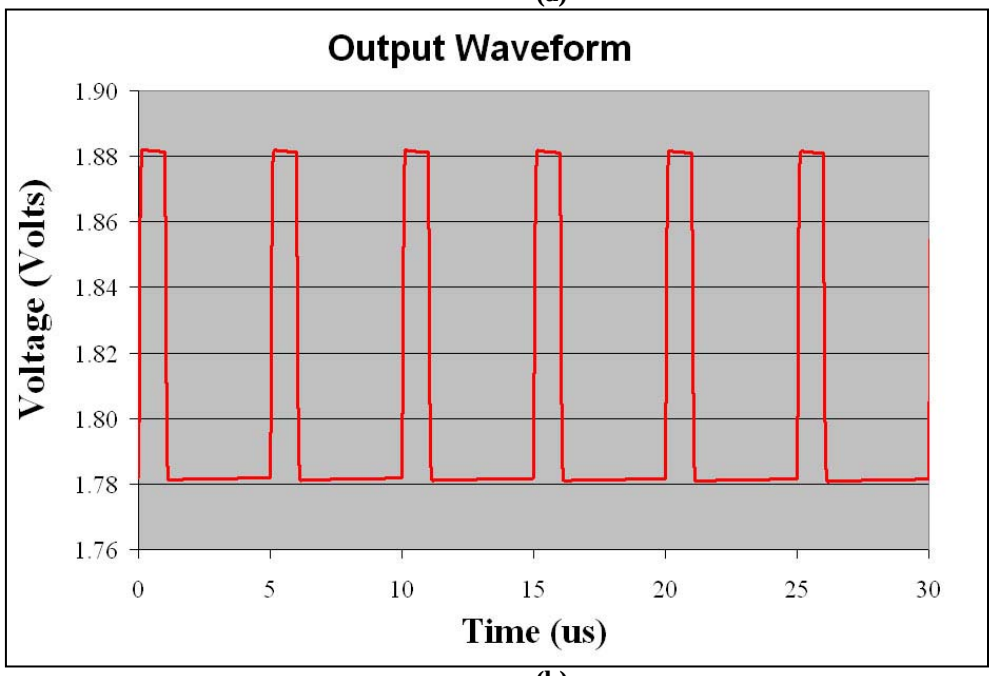


Figure 120: Frequency Response of the Pre-amplifier/Amplifier Employing Correlated Double Sampling without Capacitive Matching

In the second setup the matching capacitor is used to provide capacitive matching at the pre-amplifier input and to maximize the signal-to-noise ratio. In this case the pre-amplifier/amplifier has a gain of $63\,dB$. The frequency response is shown in figure125. The transient input and output waveforms for the pre-amplifier/amplifier chain are shown in figure 126. The equivalent output noise of the signal processing chain is shown in figure 127. The amplifier has a maximum equivalent output noise of $280\mu V/\sqrt{Hz}$. This is approximately equivalent to 90 electrons. The signal-to-noise ratio for the pre-amplifier/amplifier chain is about $5300\,V/V$. This value is more than 80 times larger than the signal-to-noise ratio of the signal processing chain reported previously by cook et.al [42].



(a)



(b)

Figure 121: (a) Simulated Input and (b) Output Transient Waveforms of the Pre-amplifier/Amplifier Readout Circuitry Employing Correlated Double Sampling without Capacitive Matching

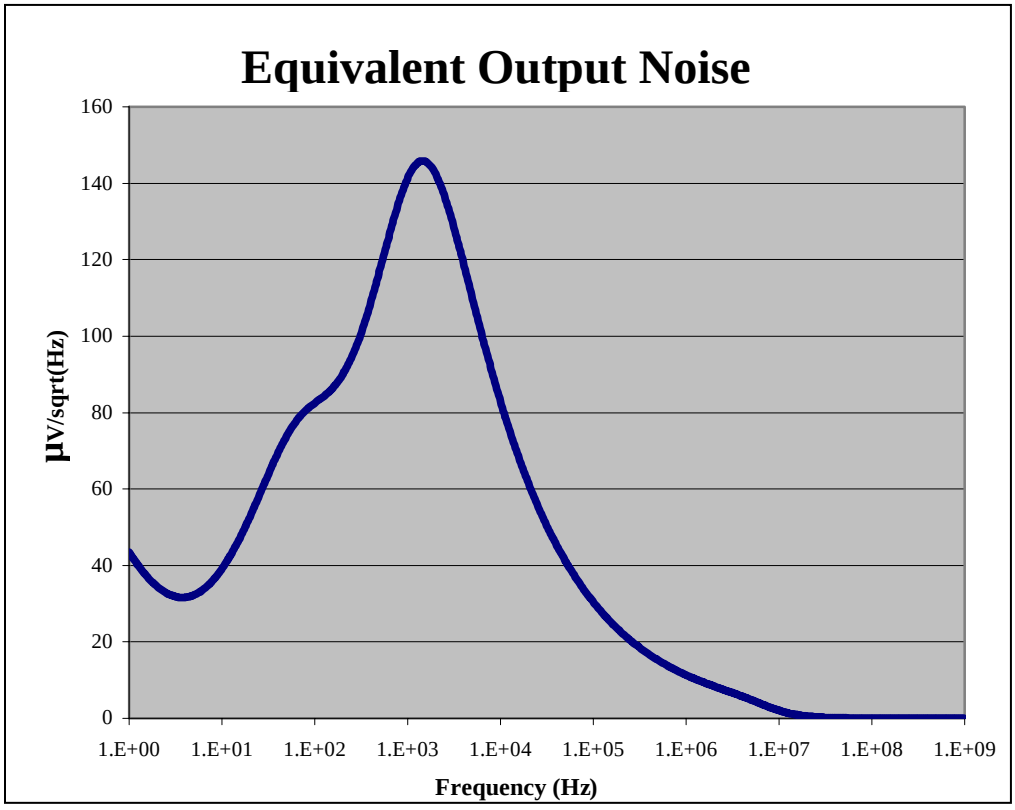


Figure 122: Simulated Equivalent Output Noise of the Pre-amplifier/Amplifier Employing Correlated Double Sampling without Capacitive Matching

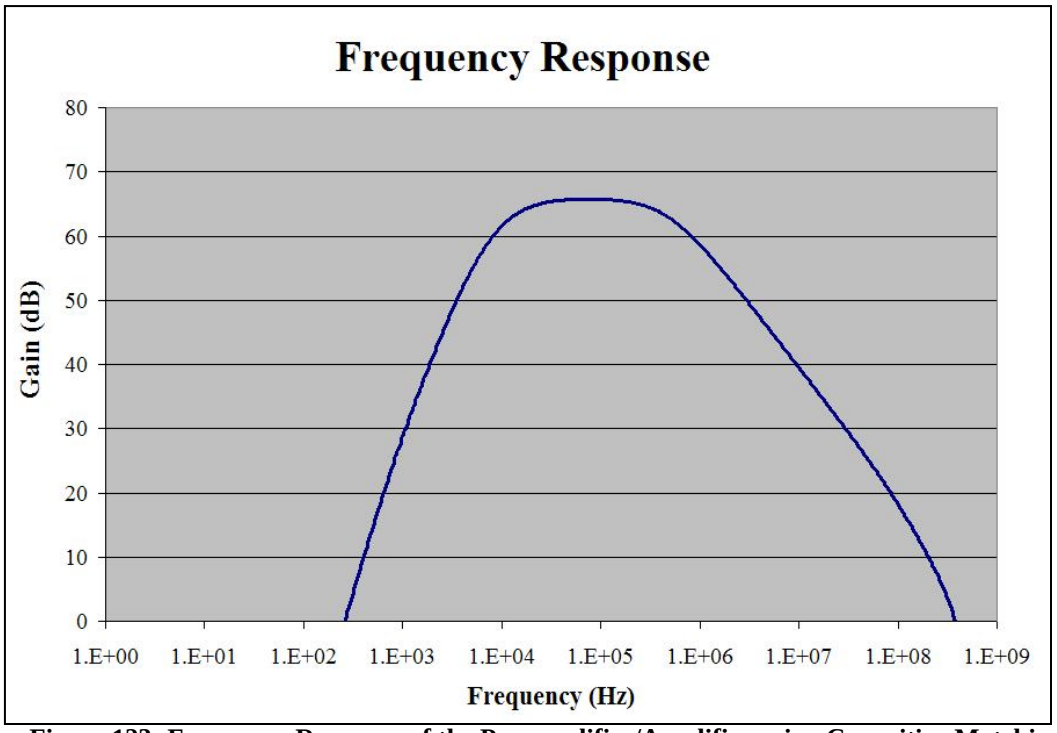


Figure 123: Frequency Response of the Pre-amplifier/Amplifier using Capacitive Matching without Correlated Double Sampling

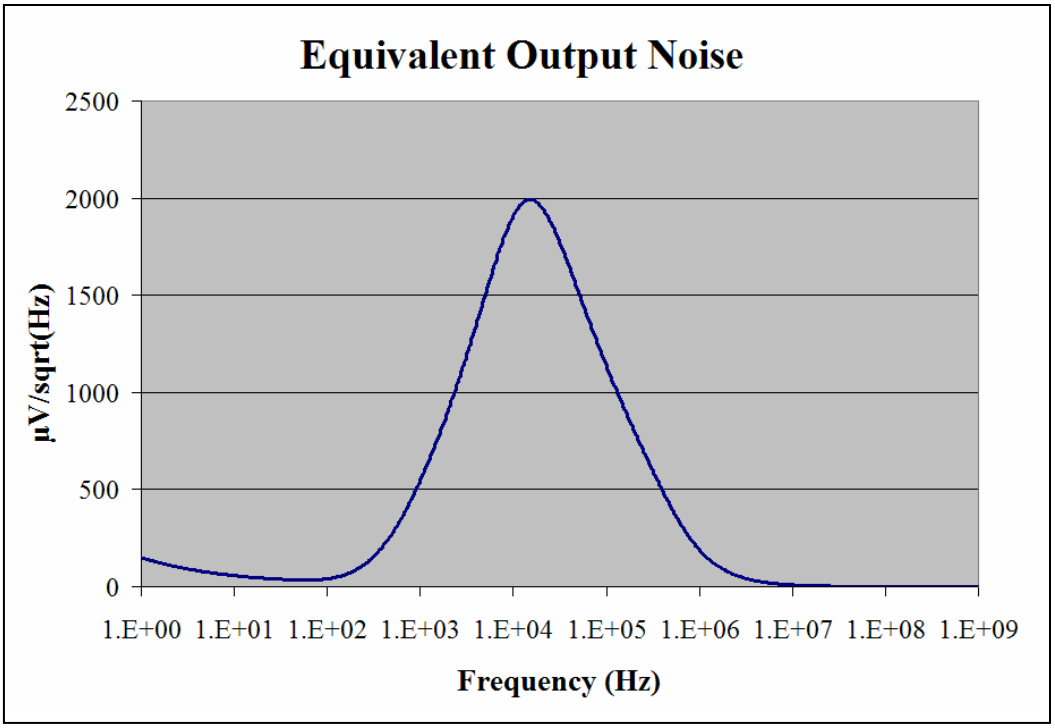


Figure 124: Simulated Equivalent Output Noise of the Pre-amplifier/Amplifier Employing Capacitive Matching without Correlated Double Sampling

It is evident from the simulation results that capacitive matching makes a significant difference in the equivalent output noise of the pre-amplifier/amplifier chain. As can be seen the equivalent output noise for the case using the capacitive matching is $280\mu V/\sqrt{Hz}$. The equivalent output noise for the case that does not employ the capacitive matching technique is $145\mu V/\sqrt{Hz}$. The maximum equivalent output noise for the setup with the capacitive matching is more than the equivalent output noise for the case without the capacitive matching. Though, attention has to be paid to the fact that the gain in the scenario with the capacitive matching is $60\,dB$, while the gain for the case not using the capacitive matching is $40\,dB$. So although the equivalent output noise is larger for the capacitively matched pre-amplifier/amplifier, the equivalent signal-to-noise ratio in this case is much larger

than the SNR for the pre-amplifier/amplifier chain that does not use the capacitive matching.

As can be seen from the simulation results, the correlated double sampling and capacitive matching techniques used along with the low noise pre-amplifier/amplifier chain improve the signal-to-noise ratio by 80 times compared to the previous technique which was proposed by Cook et. al. The signal-to-noise ratio for the pre-amplifier/amplifier chain employing correlated double sampling and capacitive matching is $5300 V/V$. This value reduces to $680 V/V$ when only correlated double sampling is used to reduce the noise and increase the signal-to-noise ratio. This shows that capacitive matching increases the signal-to-noise ratio by approximately an order of magnitude.

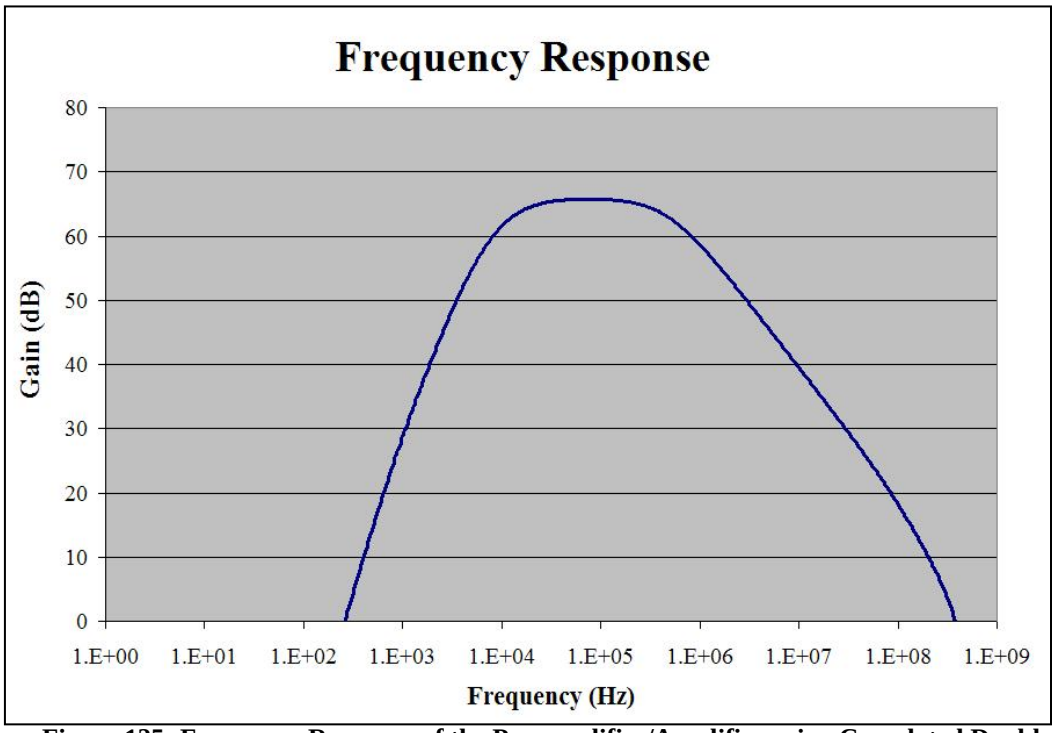
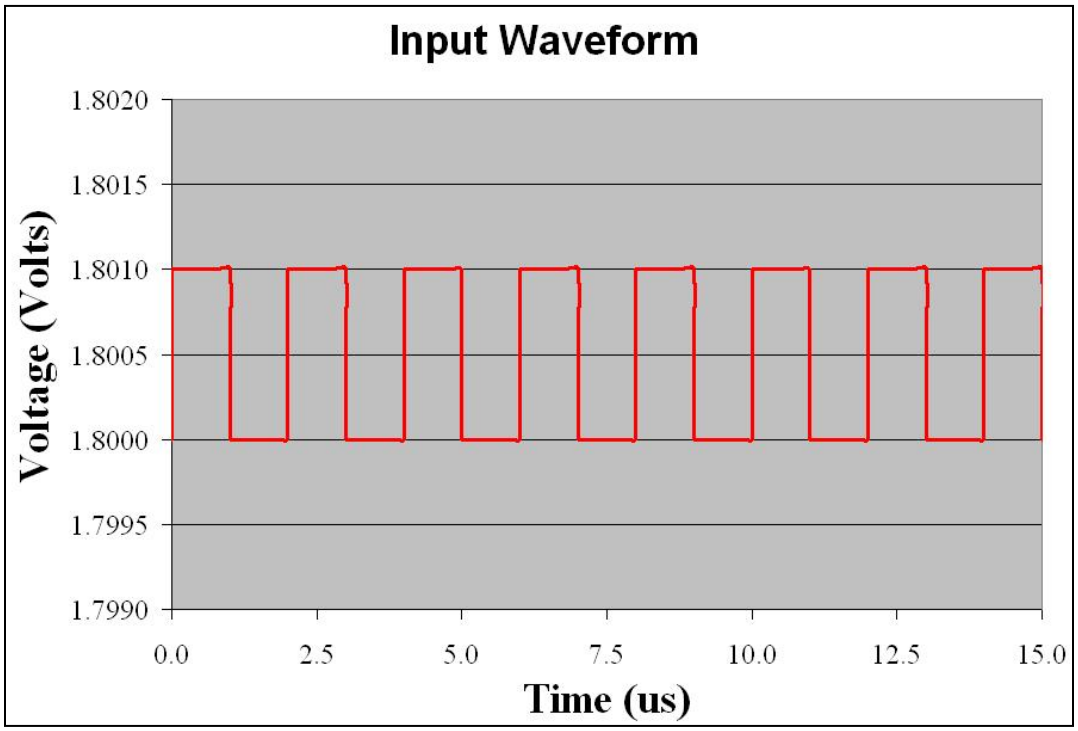
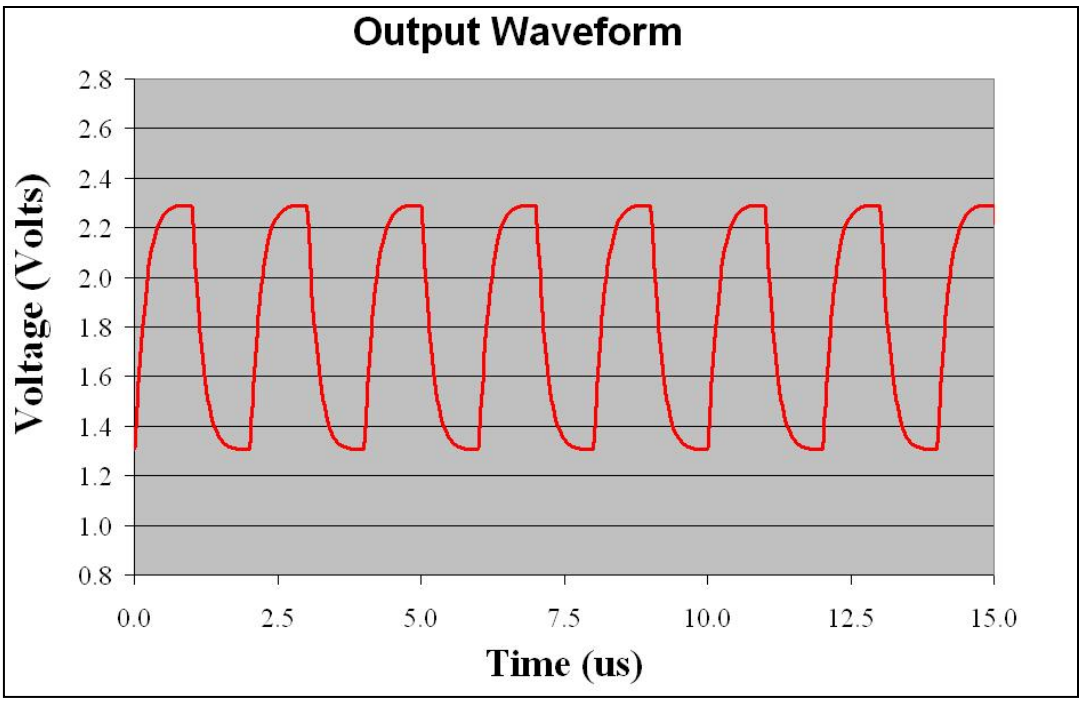


Figure 125: Frequency Response of the Pre-amplifier/Amplifier using Correlated Double Sampling and Capacitive Matching



(a)



(b)

Figure 126: (a) Simulated Input and (b) Output Transient Waveforms of the Pre-amplifier/Amplifier Readout Circuitry using Correlated Double Sampling and Capacitive Matching

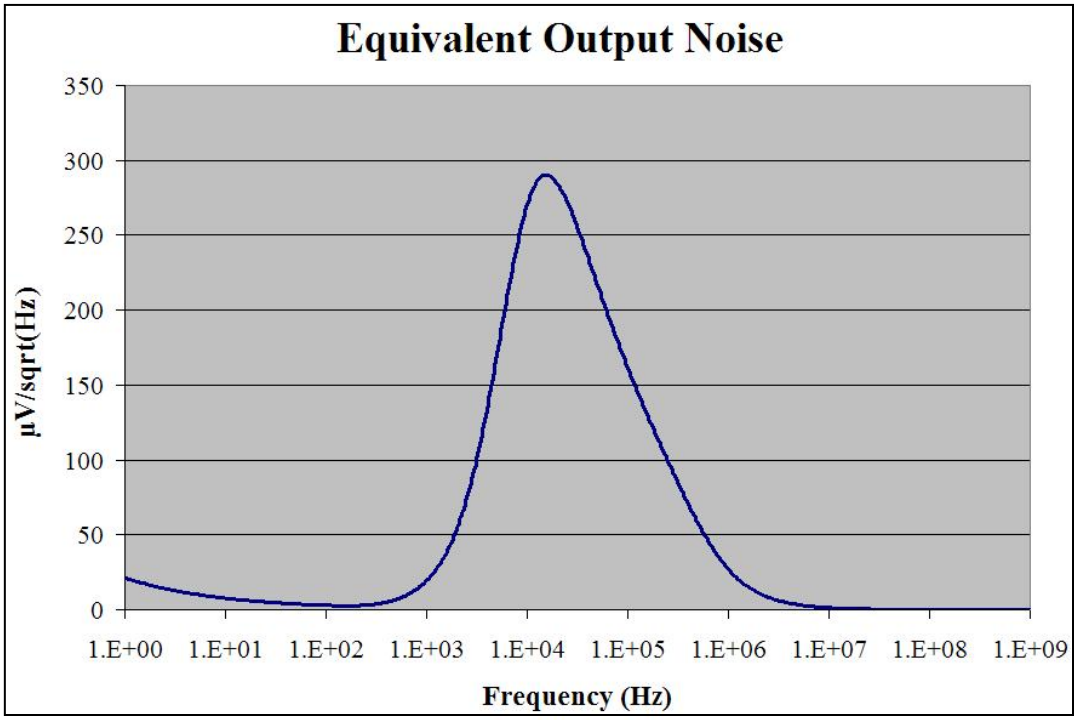


Figure 127: Simulated Equivalent Output Noise of the Pre-amplifier/Amplifier using Correlated Double Sampling and Capacitive Matching

In the next section the pre-amplifier/amplifier readout circuitry chip is tested and the experiment results are analyzed.

7.4 Experiment Results

The pre-amplifier/amplifier readout circuitry is designed and fabricated in 0.13 μm CMOS8RF IBM process technology. The layout of this chip is shown in figure 128. The enhanced views for the layout of the pre-amplifier/amplifier readout circuitry are shown in figures 129 and 130. A picture of this chip is shown in figure 131.

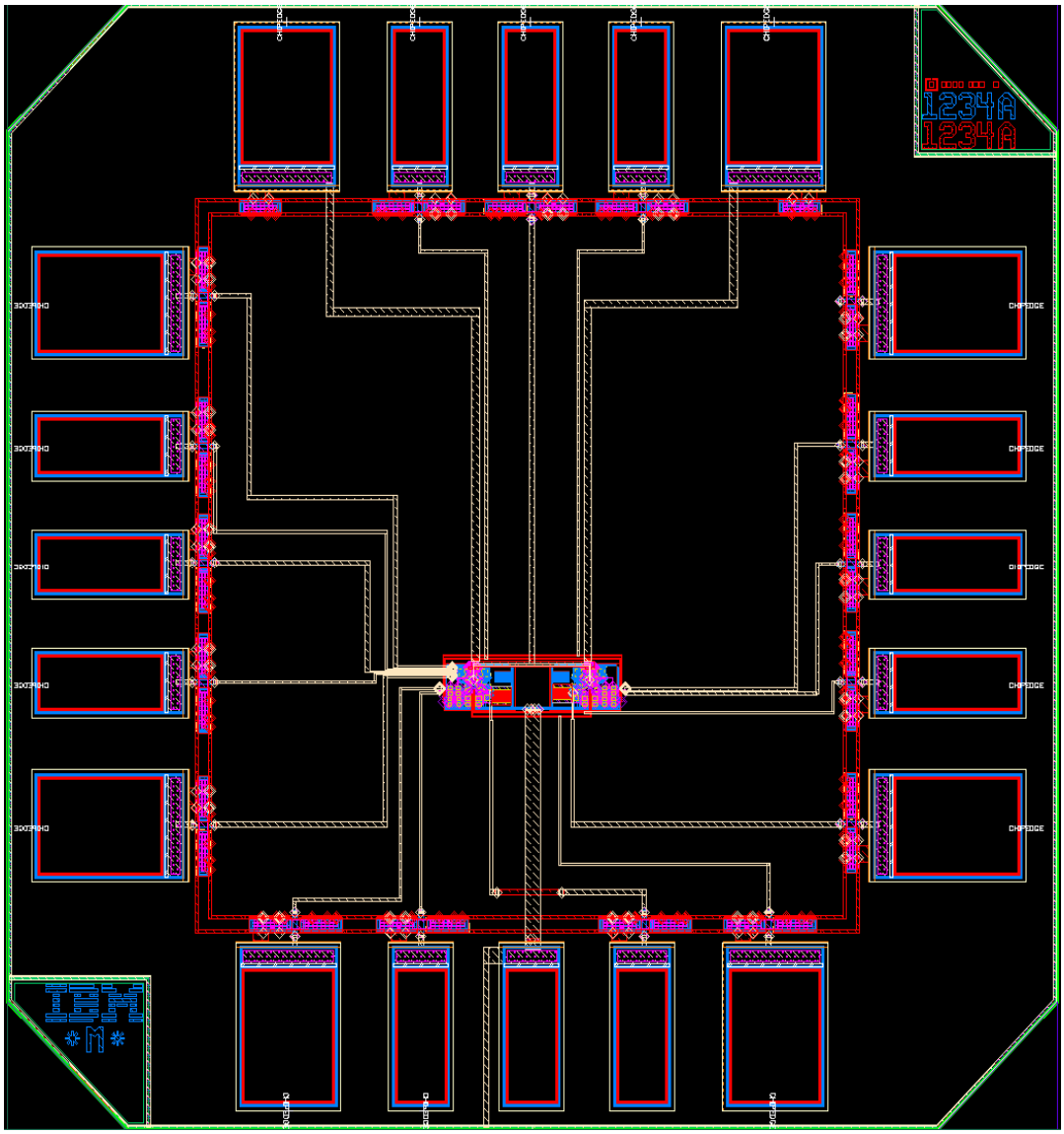


Figure 128: The Chip Layout for the Low Noise Pre-amplifier/Amplifier Chain Shown in Figure 118

Right now, the feedback capacitors are implemented as off chip capacitors. This is due to the fact that 0.13 μm CMOS8RF IBM process technology does not include capacitors yet. This is also useful for testing and debugging purposes. In future, once the 0.13 μm CMOS8RF IBM process is developed further, these capacitors can be implemented on chip.

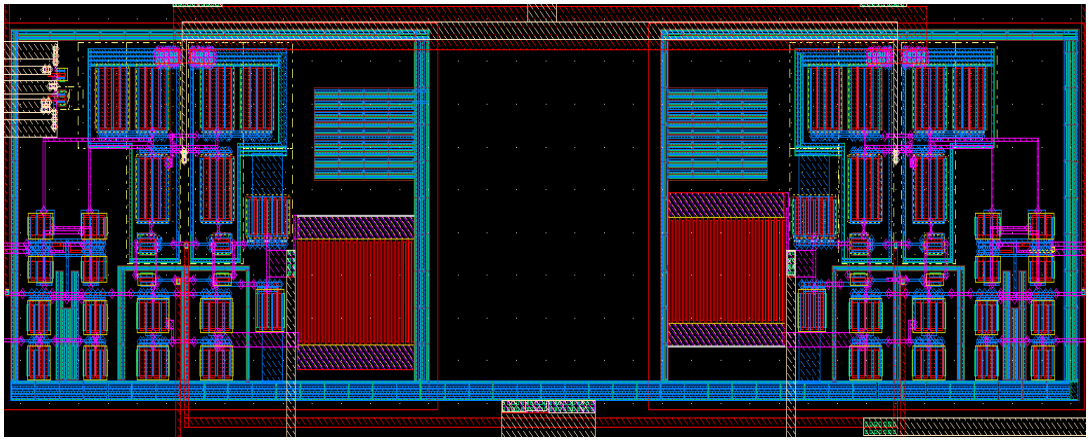


Figure 129: The Pre-amplifier/Amplifier Layout for the Low Noise Signal Processing Chain Shown in Figure 118

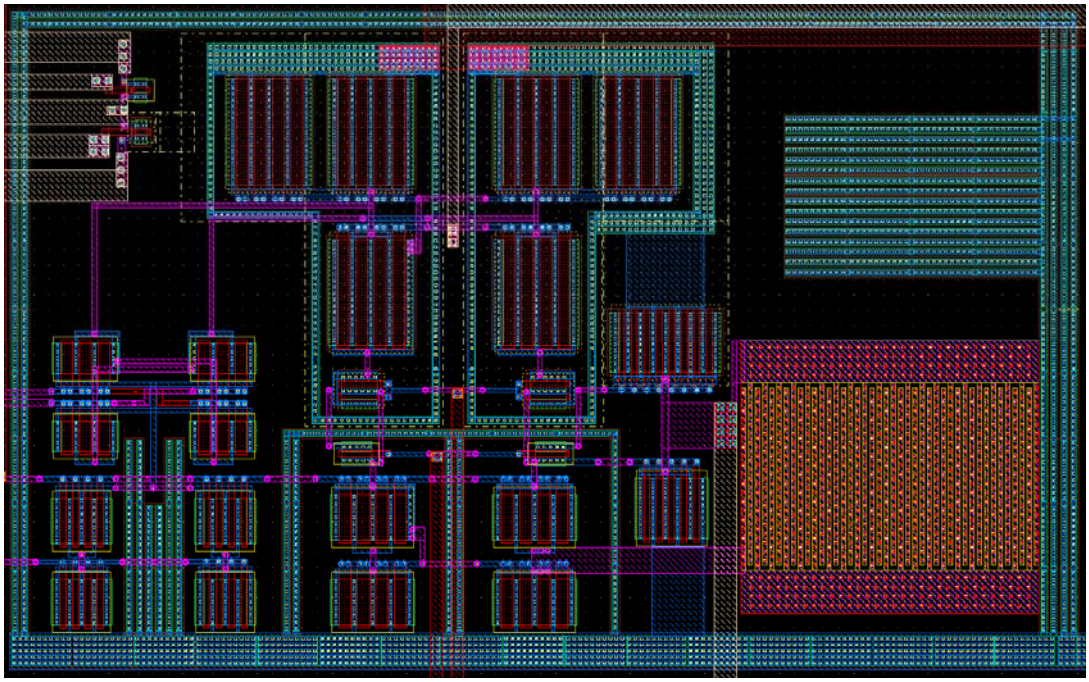


Figure 130: Enhanced View of the Low Noise Amplifier

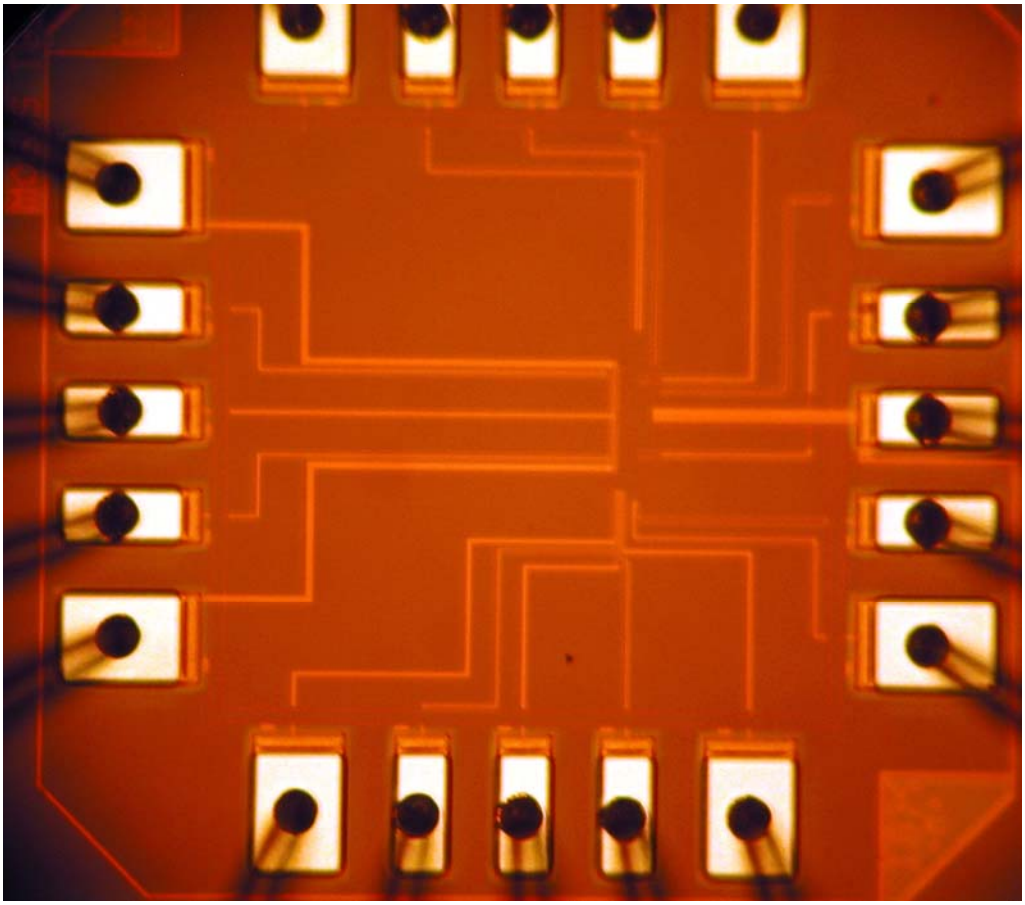


Figure 131: Low Noise Pre-amplifier/Amplifier Readout Circuitry Chip

First a single stage of the pre-amplifier/amplifier chain is tested individually to make sure that each stage functions properly. The setup for this is shown in figure 132. A sine wave with a frequency of $100\,kHz$ is used at the input of the pre-amplifier. The pre-amplifier stage is set up with a feedback loop with a closed loop gain of $10\,V/V$. This closed loop gain is achieved using a $10\,k\Omega/100\,k\Omega$ resistor combination realized by R_1 and R_2 shown in figure 132. The input and output transient waveforms are shown in figure 133. The $3\,dB$ bandwidth for the pre-amplifier is the bandwidth where the gain for this stage is reduced by $3\,dB$. This means that the gain is about 0.707 times the DC gain. The $3\,dB$ bandwidth of the pre-

amplifier stage is about 10 *MHz* . The transient input and output waveforms at the 3dB bandwidth frequency of 10 *MHz* can be seen in figure 134.

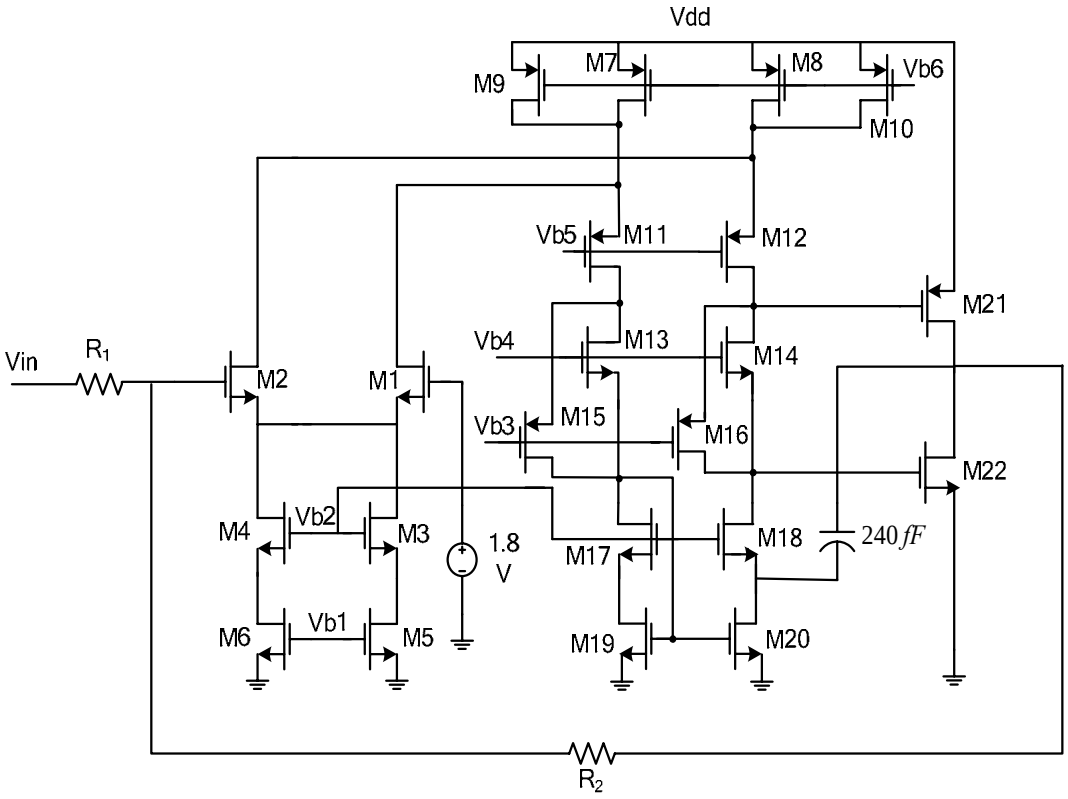


Figure 132: The Pre-amplifier Stage Test Setup

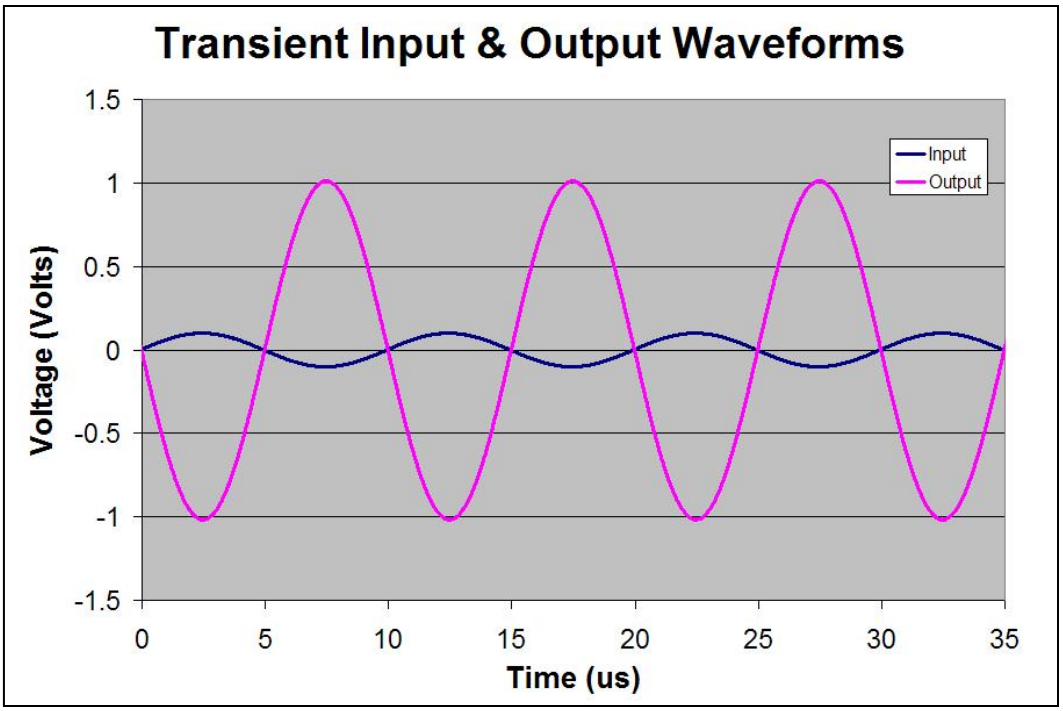


Figure 133: Experimental Input and Output Transient Response for the Pre-amplifier Stage with a Feedback Resistor Combination of 10k/100k

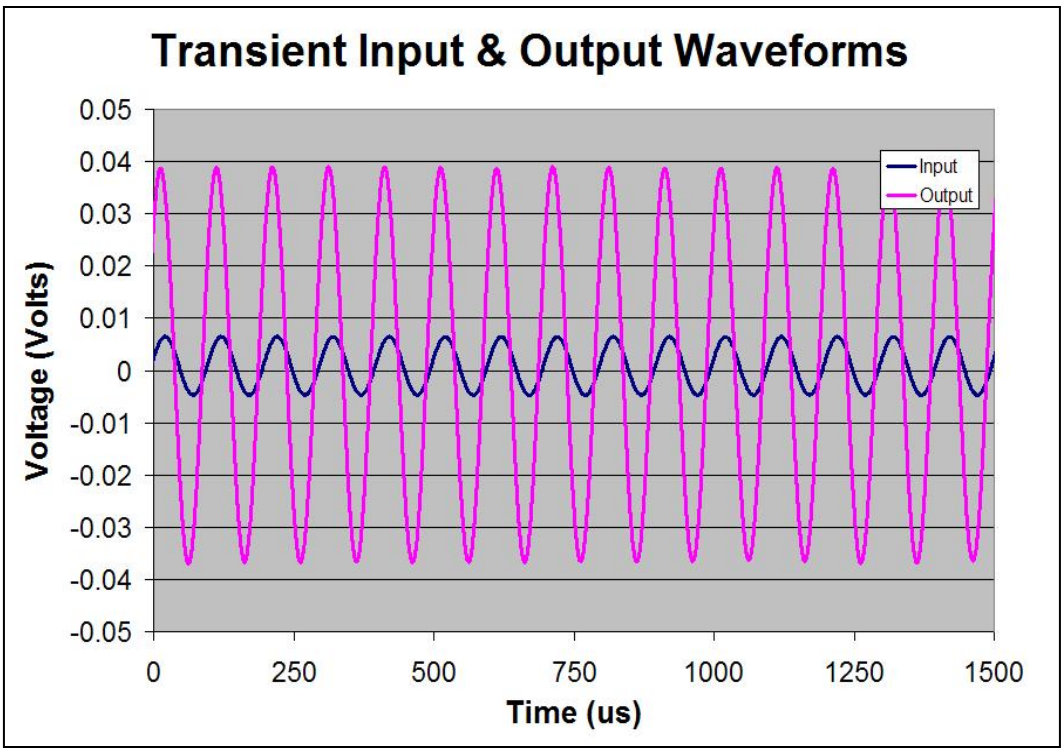


Figure 134: Experimental Input and Output Transient Response for the Pre-amplifier Stage with a Feedback Resistor Combination of 10k/100k at the 3dB Bandwidth Frequency of 10MHz

Next the pre-amplifier stage is tested with a close loop gain of $100\,V/V$. The amplifier is setup with a feedback resistor combination of $10\,k\Omega/1\,M\Omega$, realized by resistors R_1 and R_2 shown in figure 130. The setup stays the same as that shown in figure 132 except for the feedback resistors which are replaced by the $10\,k\Omega/1\,M\Omega$ combination. The input and output transient waveforms for the pre-amplifier stage with a closed loop gain of $100\,V/V$ are shown in figure 135. As can be seen in figure 136 the 3dB bandwidth is $600\,kHz$ in this case. The unity gain bandwidth of the pre-amplifier stage is above $16\,MHz$ and could not be measured. This is due to instrument limitation since the function generator did not work above $16\,MHz$. Figure 137 shows the input and output transient waveforms at $10\,MHz$. As can be seen from this figure the output is still not equal to the input transient waveform at $10\,MHz$.

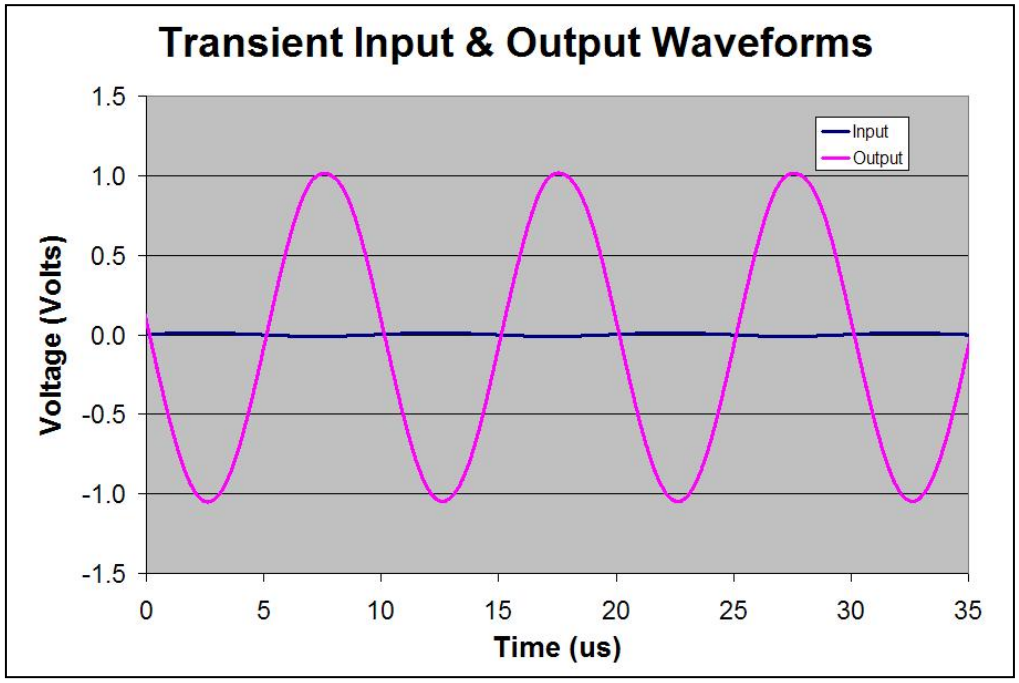


Figure 135: Experimental Input and Output Transient Response for the Pre-amplifier Stage with a Feedback Resistor Combination of 10k/1M

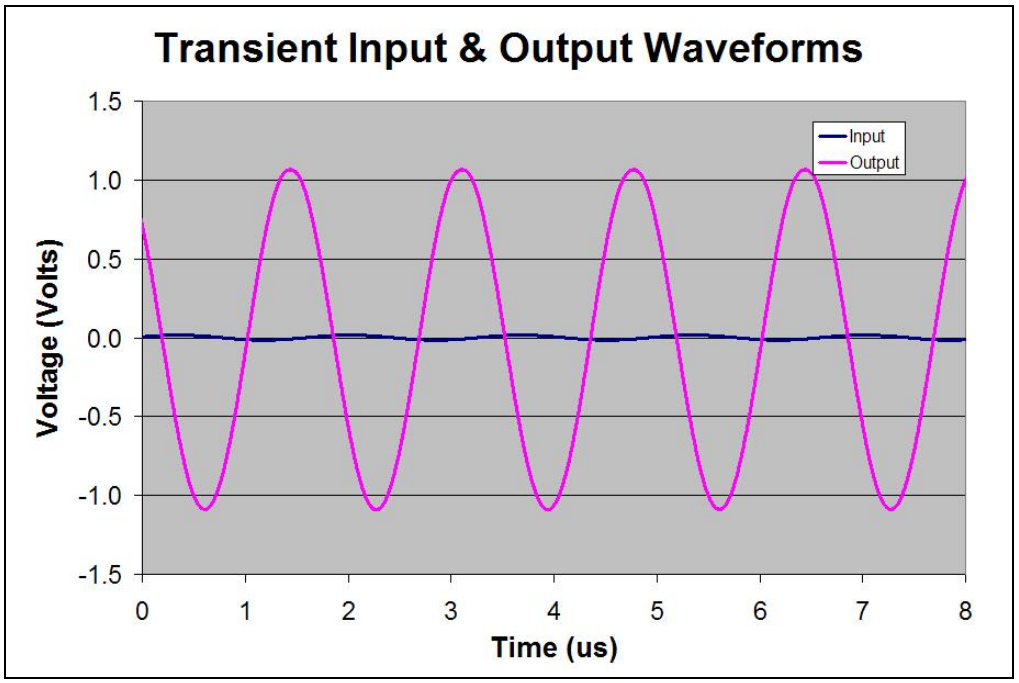


Figure 136: Experimental Input and Output Transient Response for the Pre-amplifier Stage with a Feedback Resistor Combination of 10k/1M at the 3dB Bandwidth Frequency of 600KHz

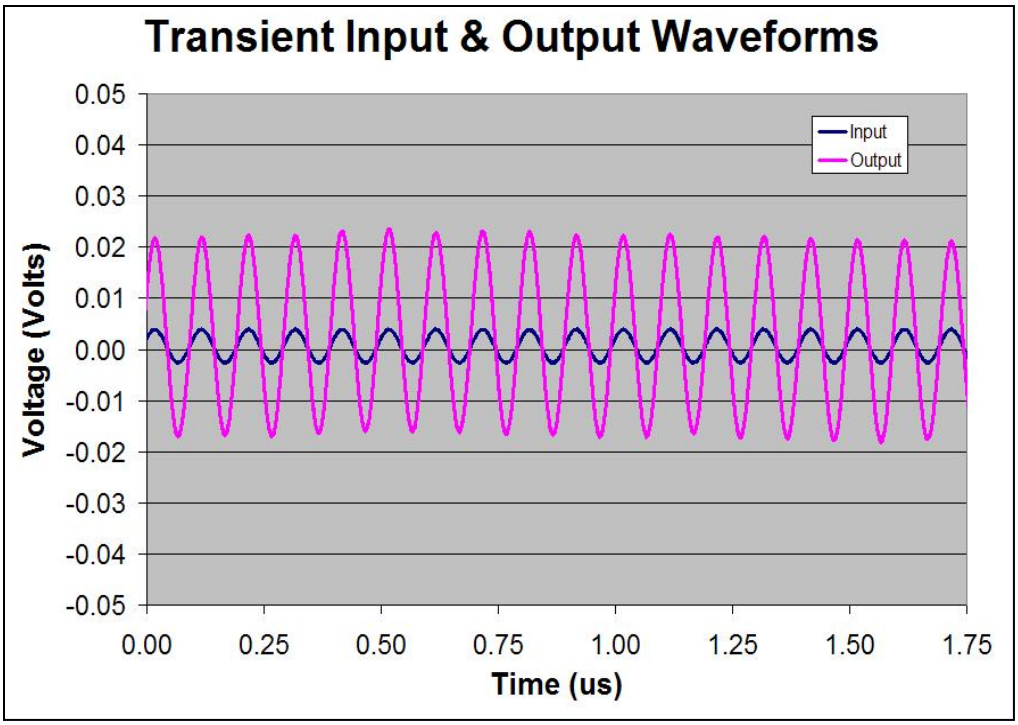


Figure 137: Experimental Input and Output Transient Response for the Pre-amplifier Stage with a Feedback Resistor Combination of 10k/1M at 10MHz

After testing the first stage of the pre-amplifier/amplifier chain and validating the experimental setup and results, at this point the two stages of the pre-amplifier/amplifier are tested together. First the readout circuitry is tested without using the capacitive matching and correlated double sampling techniques. This is to make sure that the pre-amplifier/amplifier readout circuitry functions properly. The test setup is shown in figure 138. The amplifier and pre-amplifier are each setup in resistor feedback combination such that they have a closed loop gain of $10 V/V$. So the pre-amplifier/amplifier cascade has a total gain of $100 V/V$. In order to perform this test, a $1 kHz$ sinusoidal signal is fed to the pre-amplifier's input. The transient input and output waveforms for the readout circuitry are shown in figure 139. The first stage has a closed loop gain of $9.6716 V/V$ and the second stage has a gain of $10.0277 V/V$. The total gain of the pre-amplifier/amplifier is $96.984 V/V$. The unity gain bandwidth is above $16 MHz$ and could not be measured due to the function generator limitations.

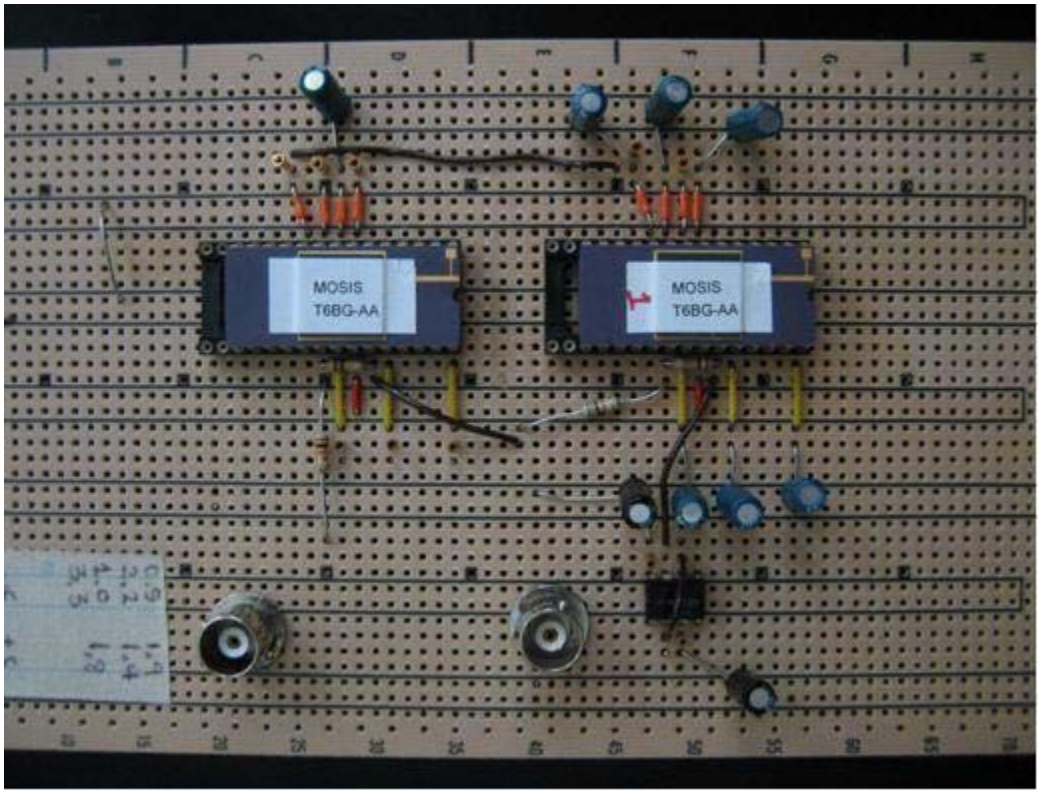


Figure 138: Test Setup for the Pre-amplifier/Amplifier Readout Circuitry without Correlated Double Sampling and Capacitive Matching

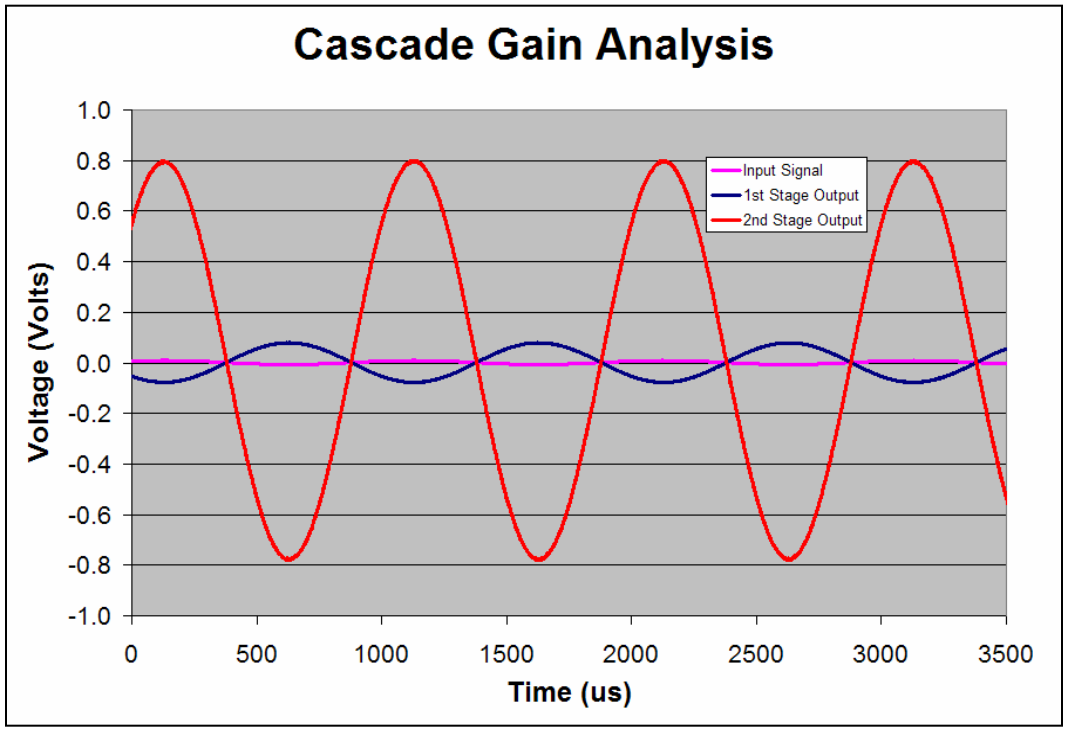


Figure 139: Experimental Input and Output Transient Response for the Pre-amplifier/amplifier Readout Circuitry with a Closed Loop Gain of 100V/V

Now the same test described above is preformed with a $1\,kHz$ square wave fed into the pre-amplifier/amplifier readout circuitry input. The transient input and output waveforms for the readout circuitry are shown in figure 140. The first stage has a closed loop gain of $9.833\,V/V$ and the second stage has a gain of $10.0377\,V/V$. The total gain of the pre-amplifier/amplifier is $98.7\,V/V$. The unity gain bandwidth is above $16\,MHz$ and could not be measured due to the function generator's limitations.

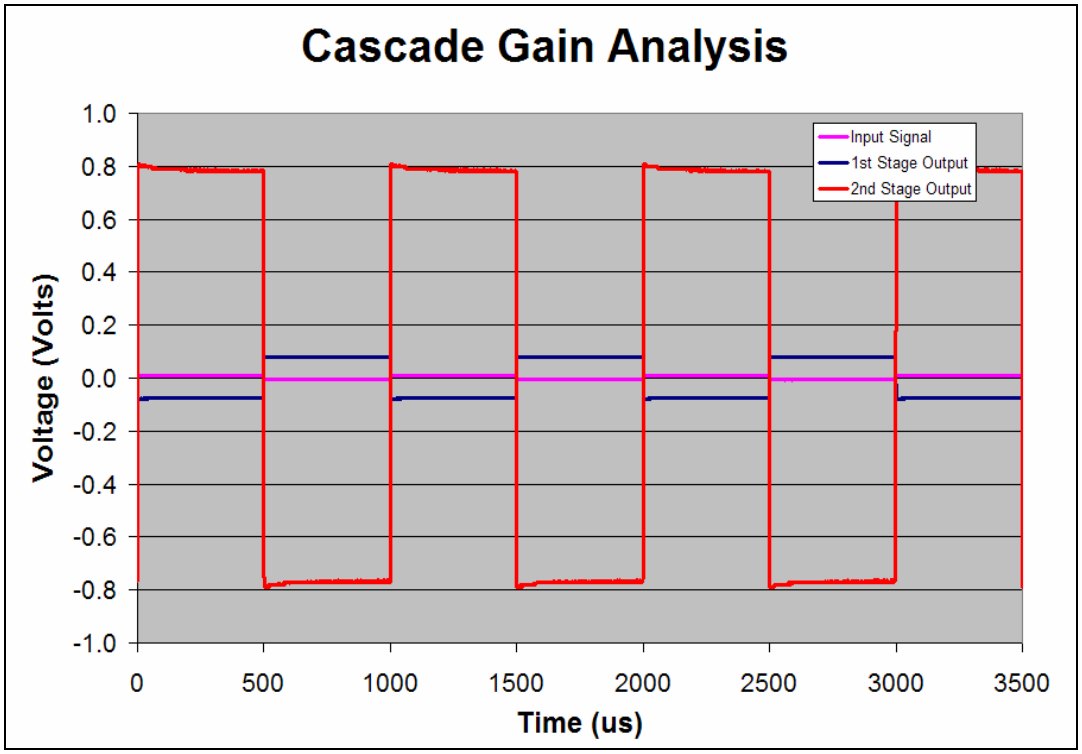


Figure 140: Experimental Input and Output Transient Response for the Pre-amplifier/amplifier Readout Circuitry with a Closed Loop Gain of 100V/V

In order investigate the frequency spectrum, a $100\,kHz$ square wave signal is fed to the input of the pre-amplifier/amplifier readout circuitry. The input and output transient waveforms for the pre-amplifier/amplifier chain with the $100\,kHz$ square wave signal are shown in figure 141. The frequency spectrum of the pre-amplifier/amplifier chain is captured using a spectrum analyzer. The frequency

spectrum for the readout circuitry with a closed loop gain of $100\,V/V$ is shown in figure 142. The frequency spectrum is zoomed to the frequencies ranging from $75\,kHz$ to $275\,kHz$. The first harmonic is at $100\,kHz$ and the second harmonic is at $200\,kHz$ as expected. As can be seen from figure 142, the noise peak levels are at about -50 dBm. The first harmonic is measured at -16 dBm so the noise level is $34\,dB$ below the first harmonic. This means that the signal-to-noise ratio is $50\,V/V$.

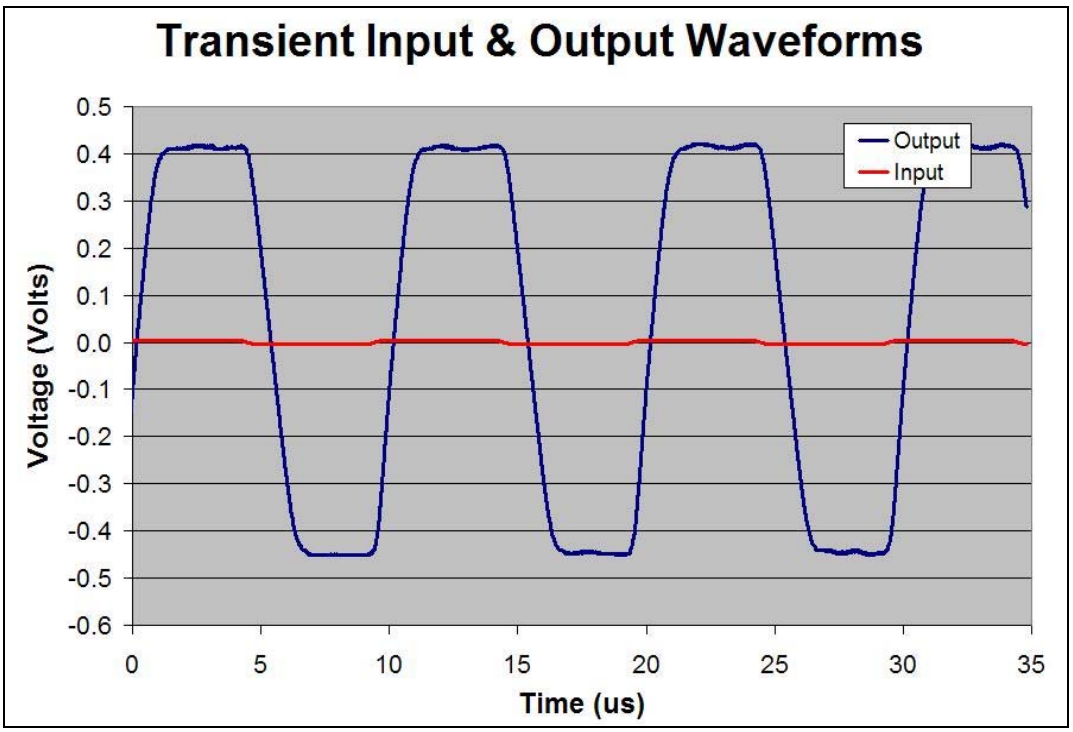


Figure 141: Experimental Input and Output Transient Response for the Pre-amplifier/amplifier Readout Circuitry without Correlated Double Sampling and Capacitive Matching with a Closed Loop Gain of 100V/V

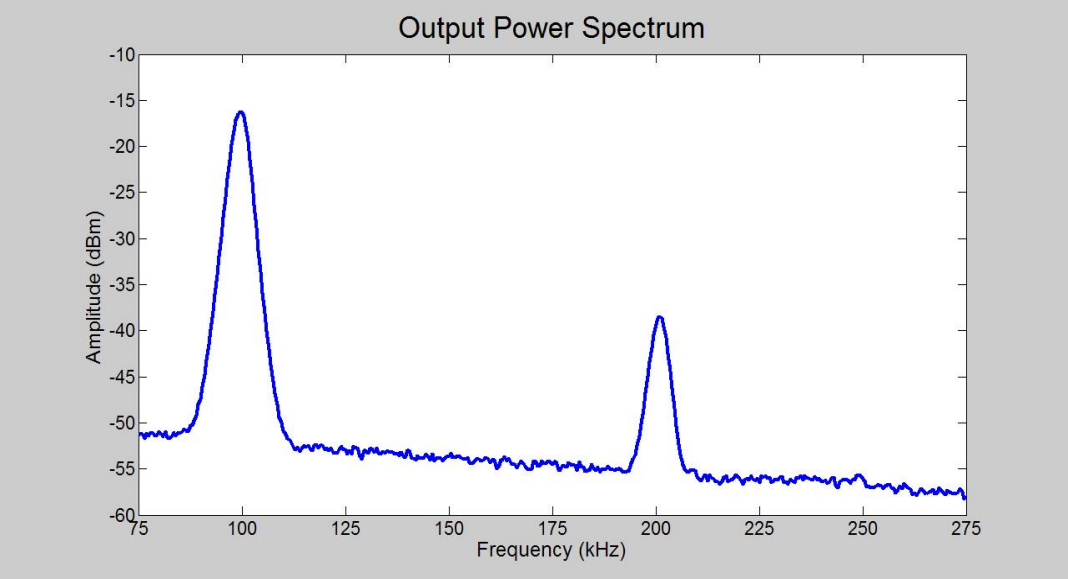


Figure 142: Frequency Spectrum for the Pre-amplifier/amplifier Readout Circuitry without Correlated Double Sampling and Capacitive Matching with a Closed Loop Gain of 100V/V

Now we would like to test the pre-amplifier/amplifier readout circuitry with the correlated double sampling employed in the readout circuitry. The test setup is as shown in figure 118 without the matching capacitor C_{match}. The Circuit diagram is shown in figure 143. The transient input and output signals for the pre-amplifier/amplifier chip employing correlated double sampling are shown in figure 144. As can be seen the pre-amplifier/amplifier chain has a gain of $96.47 V/V$. The apparent distortion of the output signal is due to pulse shaping.

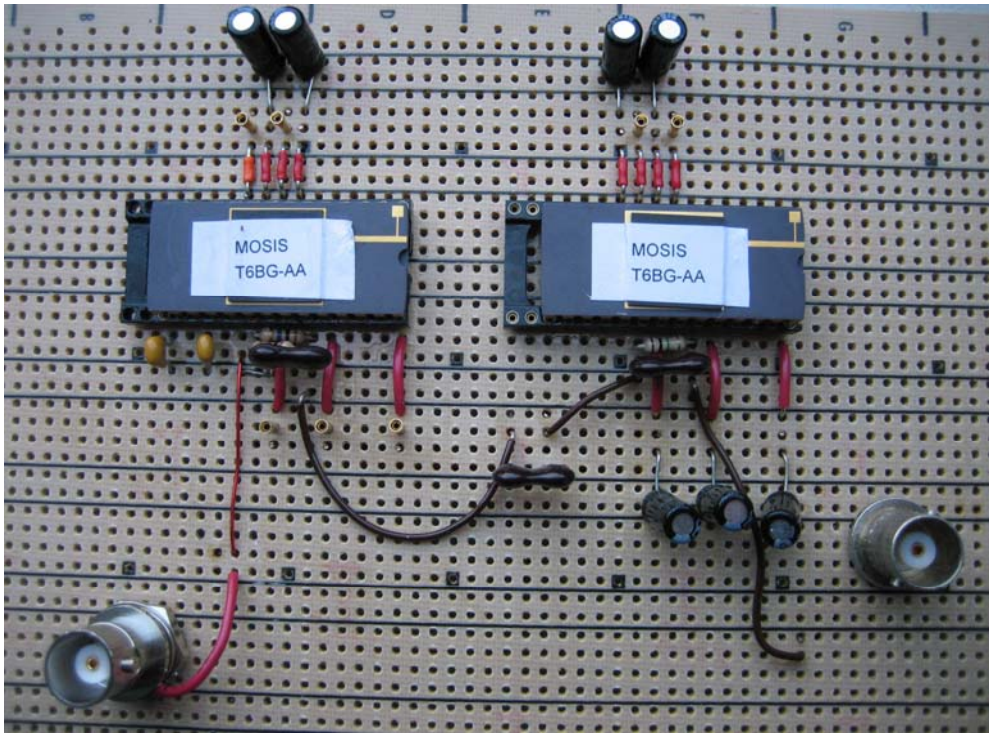


Figure 143: Test Setup for the Pre-amplifier/Amplifier Chain Employing Correlated Double Sampling

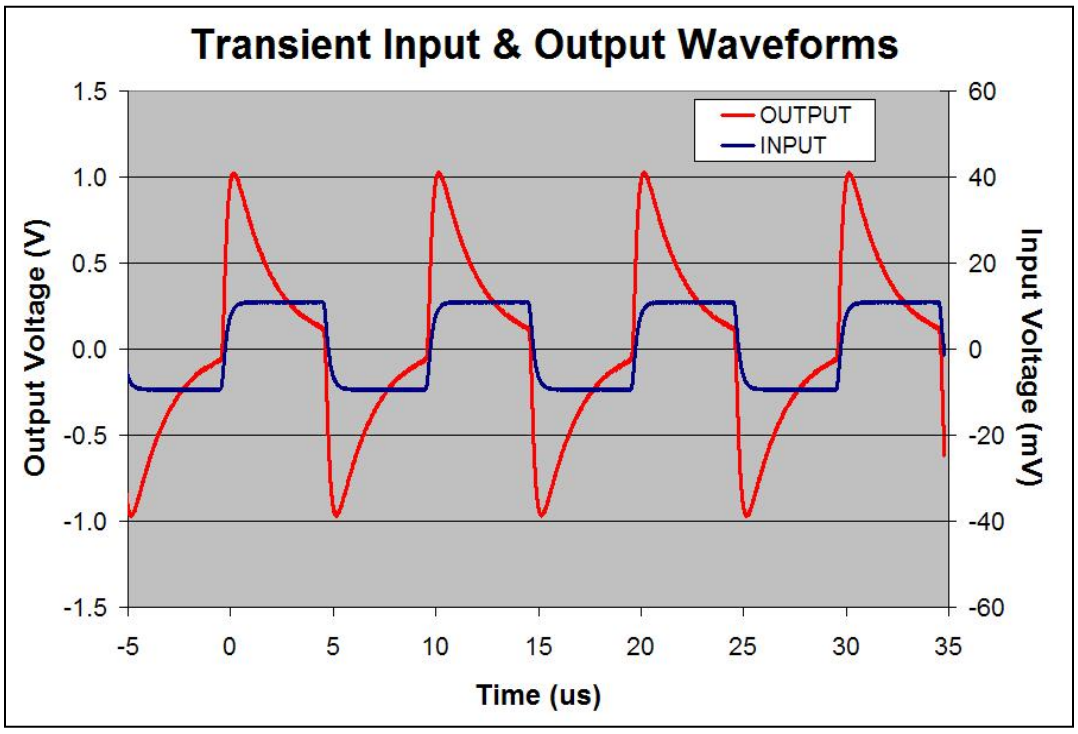


Figure 144: Experimental Input and Output Transient Response for the Pre-amplifier/amplifier Readout Circuitry with a Closed Loop Gain of 100V/V

The frequency spectrum for the pre-amplifier/amplifier readout circuitry employing correlated double sampling is shown in figure 145. The first and second harmonics can be seen at $100\,kHz$ and $200\,kHz$ respectively. The signal level is at $-14\,dBm$. The peaks of the noise floor are at $-70\,dBm$. Hence, figure 145 shows that the peaks of the noise floor are $56\,dB$ below the carrier's first harmonic. This means that the signal-to-noise ratio for the pre-amplifier/amplifier chain employing correlated double sampling is $630\,V/V$. This matches the simulation results derived in the previous section for the readout circuitry employing correlated double sampling without capacitive matching.

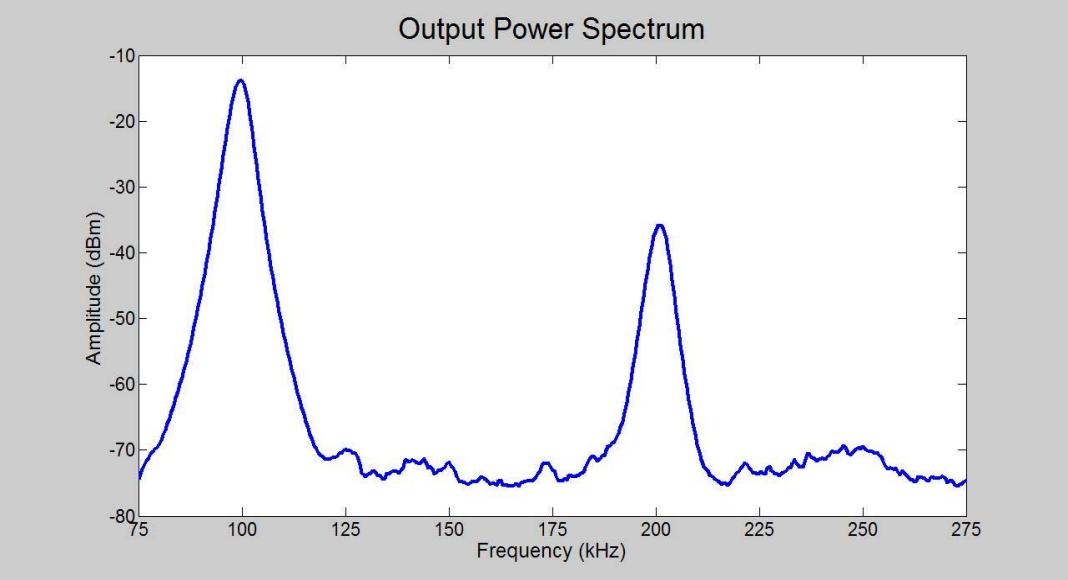


Figure 145: Frequency Spectrum for the Pre-amplifier/amplifier Readout Circuitry Employing Correlated Double Sampling with a Closed Loop Gain of 100V/V

We would like to compare the experimental results for the pre-amplifier/amplifier readout circuitry with and without the correlated double sampling being employed. It can be seen from figures 141 and 144 that the gain for the two cases are almost the same. For the scenario where correlated double sampling is not

employed, the noise floor peaks are $34\,dB$ below the first carrier harmonic. This value is increased to $56\,dB$ for the scenario where correlated double sampling is used in the pre-amplifier/amplifier chain. Experimental results show that with the correlated double sampling used in the readout circuitry, the peaks of the noise floor are $22\,dB$ lower with respect to the first harmonic of the carrier. The signal-to-noise ratio is increased by more than an order of magnitude when correlated double sampling is added to the circuit.

Now we would like to test the pre-amplifier/amplifier readout circuitry with the correlated double sampling and capacitive matching employed in the readout circuitry. The circuit diagram is as shown in figure 118 and this time the capacitor C_{match} is included for matching purposes. The actual test setup is shown in figure 146. The transient input and output signals for the pre-amplifier/amplifier chip employing correlated double sampling are shown in figure 147. This figure shows that the pre-amplifier/amplifier chain has a gain of $92.34\,V/V$.

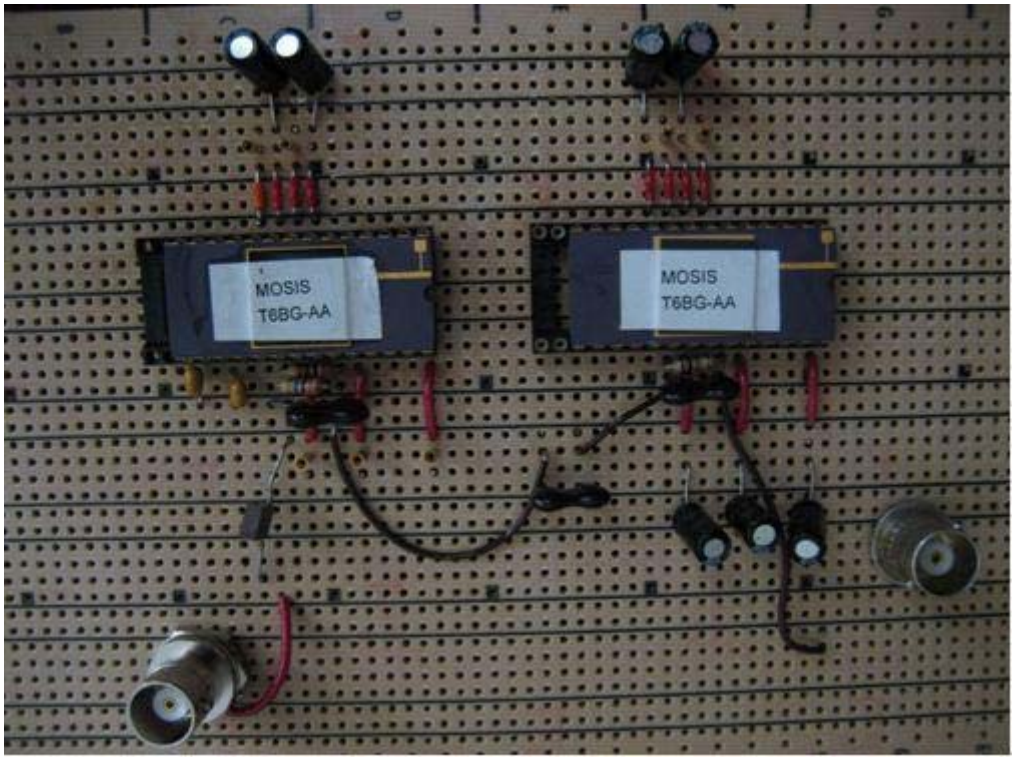


Figure 146: Test Setup for the Pre-amplifier/Amplifier Chain Employing Correlated Double Sampling and Capacitive Matching

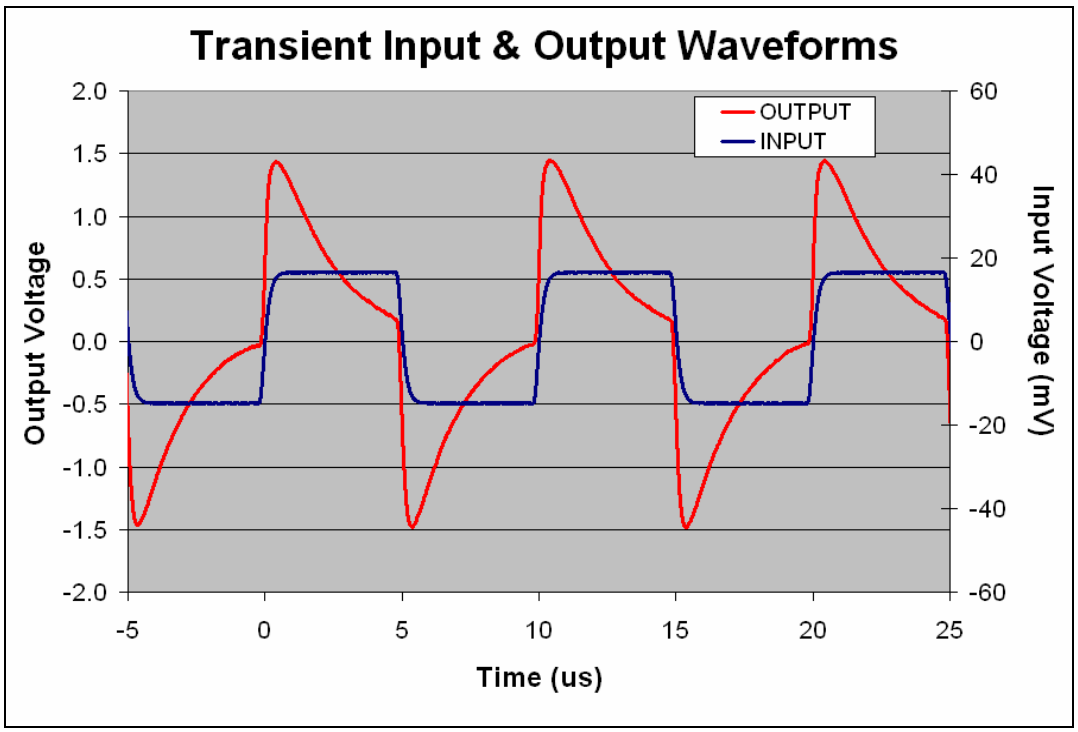


Figure 147: Experimental Input and Output Transient Response for the Pre-amplifier/amplifier Readout Circuitry Employing Capacitive Matching and Correlated Double Sampling with a Closed Loop Gain of 100V/V

The frequency spectrum for the pre-amplifier/amplifier readout circuitry employing correlated double sampling and capacitive matching is shown in figure 148. The first and second harmonics can be seen at $100\,kHz$ and $200\,kHz$ respectively. The signal level is at -10 dBm. The peaks of the noise floor are at -80 dBm. Hence, figure 148 shows that the peaks of the noise floor are $70\,dB$ below the signal's first harmonic. The signal-to-noise ratio is more than $3000\,V/V$. This value is a significant improvement over the case where correlated double sampling and capacitive matching techniques are not used in the pre-amplifier/amplifier readout circuitry. This SNR is also a considerable and noteworthy advancement over the previously proposed technique by Cook et. al [42].

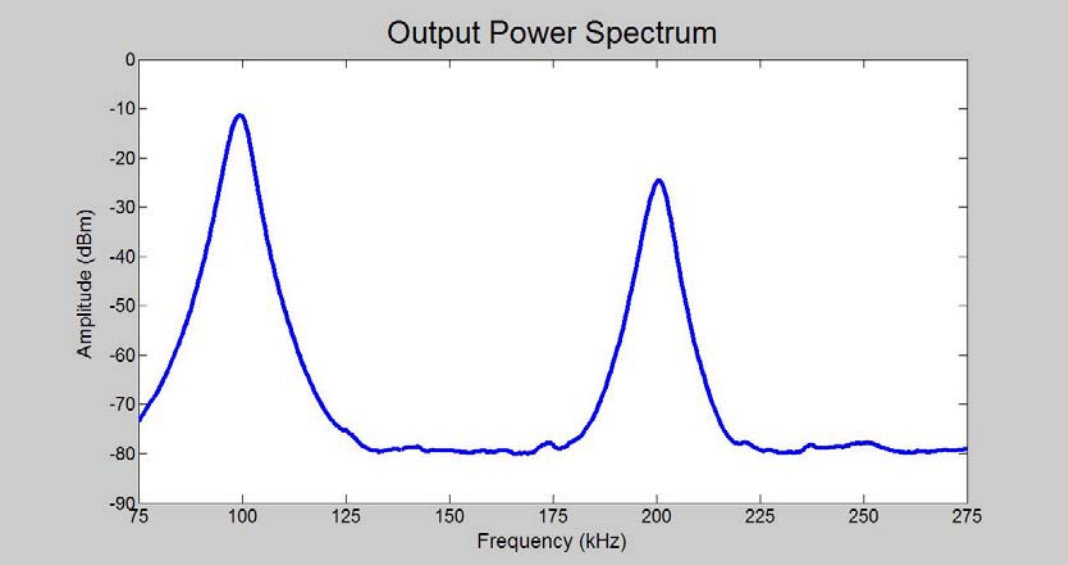


Figure 148: Frequency Spectrum for the Pre-amplifier/amplifier Readout Circuitry Employing Correlated Double Sampling and Capacitive Matching with a Closed Loop Gain of 100V/V

At this point the results for the pre-amplifier/amplifier chain employing capacitive matching and correlated double sampling are compared with the same readout circuitry lacking these techniques. It can be seen from figures 141 and 147 that the gain for the two cases are almost the same. For the scenario where correlated

double sampling and capacitive matching are not employed, the noise floor peak is $34\,dB$ below the first harmonic. This value is $70\,dB$ for the pre-amplifier/amplifier chain employing correlated double sampling and capacitive matching. The difference is $36\,dB$ which is more than an order of magnitude. This shows that the signal-to-noise ratio is increased by 63 times compared to the case where correlated double sampling and capacitive matching are not used.

To show the importance of capacitive matching, we would also like to compare the experimental results for the pre-amplifier/amplifier readout circuitry with correlated double sampling, with and without capcitive matching. It can be seen from figures 144 and 147 that the gain for the two cases are almost the same. For the scenario where capacitive matching is not employed, the noise floor peak is $56\,dB$ below the first harmonic. This value is increased to $70\,dB$ for the scenario where capacitive matching is used in the pre-amplifier/amplifier chain. As can be seen when capacitive matching is used along with correlated double sampling in the readout circuitry the peak of the noise floor is $14\,dB$ lower with respect to the first harmonic of the carrier.

Chapter 8: Conclusion

This dissertation focuses on a novel low noise signal processing chain for high output capacitor sensors. This innovative signal processing chain is aimed at increasing the signal-to-noise ratio in pixel detectors and sensors. The resulting system can be used in wide variety of detectors with a range of applications such as random access pixel detectors, fully depleted CCDs, hybrid detector systems, and superconducting detector arrays.

A large number of sensors and detectors depend upon accumulating charge on a capacitor. Reset noise resulting from the shot and thermal noise when the sensor is reset, causes a charge uncertainty, which is enhanced by the large sensor capacitor. As a result, nowadays low noise readout circuitry are of great importance in sensors and detectors. A low noise readout pre-amplifier/amplifier chain is designed for CdZnTe gamma ray radiation detectors used by NASA. The circuit is designed and laid out using Cadence. The circuit is fabricated in 0.13 μm CMOS8RF IBM technology. In order to achieve low noise performance correlated double sampling and capacitive matching are used in the readout circuitry.

As discussed in chapter 7, Correlated double sampling is implemented at the amplifier input by taking advantage of the fact that the amplifier can perform correlated double sampling without the need of additional circuitry. Correlated double sampling can be incorporated into the pre-amplifier/amplifier chain by adding only a reset switch and capacitor. This technique takes a sample of the noise during

the reset cycle and a sample of the signal plus noise during the amplification cycle. By subtracting the two samples any noise source that is correlated to the two samples will be ideally removed or minimized. A slowly varying noise source that is not correlated will be reduced in magnitude. Noise introduced at the output of the pre-amplifier/amplifier chain consists primarily of *kTC* noise from the charge sensing node. The *kTC* noise will be removed by correlated double sampling. Low frequency noise sources will be attenuated by correlated double sampling. The simulation results showed a signal-to-noise ratio of $680 V/V$ which is an order of magnitude improvement compared to the previous work done by Cook et. al [42]. The actual experimental results revealed a signal-to-noise ratio of $630 V/V$ which matches the simulation results very well. The test results give proof that by using correlated double sampling alone the signal-to-noise ratio is actually an order of magnitude more than the previously used technique by Cook et. al [42].

In order to complete the noise reduction technique, capacitive matching is also used along with correlated double sampling at the pre-amplifier input. This method calls for an additional capacitor to be placed at the input of the pre-amplifier/amplifier chain. By using capacitive matching, we are following the principle of impedance matching which maximizes the signal power transmission into the amplifier system. Simulation results using Cadence Spectre show that the signal-to-noise ratio is $5300 V/V$. This is approximately 7 times better than using correlated double sampling alone. The signal-to-noise ratio is 80 times more than the previously used techniques. The experimental results achieve a signal-to-noise ratio of more than $3000 V/V$ which is very close to the simulation results. The signal-to-noise ratio

achieved from the test results is more than 60 times better than the previously used techniques. Table 7 summarizes the results for the low noise pre-amplifier/amplifier chain.

Simulation	Experiment		Cook's readout Circuitry	
SNR	Dimensions	SNR	Dimensions	SNR
5300 V/V	100 µm ×100 µm	>3000 V/V	650 µm ×670 µm	60 V/V

Table 7: Summary and Comparison for the Low Noise Pre-amplifier/Amplifier Chain

A novel auto-zeroing technique has also been introduced in this dissertation. This novel technique uses a nulling point other than the amplifier's input and output to perform the auto-zeroing operation. The auto-zeroing is performed by taking advantage of emitter degeneration in the input transistor pair of the differential pair to cancel the offset at the output of the amplifier. So in order to perform the auto-zeroing operation two emitter degeneration resistors are added to the input transistors. In this method, the offset cancellation is done by correcting the output nodes in the circuit, which are stationary nodes. The output voltage is fed back to the emitter degenerated resistors. And based on the voltage, the current in each branch of the circuit is changed such that the output offset is canceled. By using emitter degeneration to cancel the offset, this technique increases the linearity of the amplifier which is very important in these circuits. In order to show the improvement in the input referred offset, the emitter degeneration auto-zeroing technique was applied to a telescopic cascode. Test results reveal that the input referred offset is reduced by approximately an order of magnitude or more. In most of the test

scenarios, the input referred offset voltage is less than 300 μV . The results for the auto-zeroing technique are summarized in table 8.

Telescopic Cascode		Auto-zeroed Telescopic Cascode	
Gain	Input referred offset voltage	Gain	Input referred offset voltage
9.16 V/V	5.98 mV	9.14 V/V	196 μV
67 V/V	3.02 mV	65 V/V	430 μV

Table 8: Auto-zeroing Technique Summary

To summarize, the unique contributions of this dissertation are as follows:

- Developed a low noise pre-amplifier/amplifier chain employing correlated double sampling and capacitive matching
- Implemented correlated double sampling absent of additional circuitry, using a reset switch
- Designed a readout circuit which includes signal processing at the point of signal reception
- Invented a novel auto-zeroing technique by taking advantage of the emitter degeneration resistors to reduce the input referred offset by an order of magnitude

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