ABSTRACT

Title of Document: **THE IMPACT OF INTERFACE STATES ON SUB-THRESHOLD LEAKAGE AND POWER MANAGEMENT IN CMOS DEVICES AND CIRCUITS**

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Space applications expose electronic systems to levels of radiation that are damaging to the individual components. Considerable effort has gone into the "hardening" of electronic components against total-dose damage by ionizing radiation. This thesis explores the degree to which commercial-of-the-shelf parts are affected by ionizing radiation. In particular, concentration is on the effect of interface state generation resulting from ionizing radiation on overall device performance. Various sized 0.13μm MOSFET devices were simulated, fabricated, irradiated and tested. Significant increases in the sub-threshold swing and leakage current were observed following a 1MRad total-dose gamma ray irradiation. Subsequently, logic inverter structures exhibited increased sub-threshold swing and total power dissipation following simulations that modeled increasing radiation exposure. Finally, an 11-stage ring oscillator experiment was conducted. A decrease in power for increased

irradiations was observed in previous work [49], but without explanation. This work attempts to provide a logical framework for understanding this observation.

THE IMPACT OF INTERFACE STATES ON SUB-THRESHOLD LEAKAGE AND POWER MANAGEMENT IN CMOS DEVICES AND CIRCUITS

By

James Patrick Wienke

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Chapter 1: Introduction

Space exploration has long been a topic of major interest and research. It continues to be extremely important in worldwide applications and to various organizations and agencies. These applications require the use of large systems to accomplish a vast range of tasks and assignments; one of the most important being satellite communications. Satellite systems contain not only numerous mechanical systems, but also electrical systems that are irreplaceable to complete the required overall functionality. Furthermore, in order for the systems to work properly, the different space environments that expose these systems to various unfavorable phenomena need to be well understood to combat the damaging effects.

Radiation is one such problematic phenomenon that results from space environments, such as the Van Allen belts, and as satellites and other space systems travel around or through these belts they experience large amounts of radiation exposure. This exposure results in drastic changes in the electrical properties of many devices and circuits. And this can further lead to full system malfunction which then becomes extremely difficult and expensive to restore. Thus, it is imperative to incorporate the understanding of such events in the design phase of a system. More specifically, the radiation leads to defects in many materials, with one of the most important of which being silicon dioxide (SiO_2). This material serves as the gate-insulating layer of metal-oxide-semiconductor field-effect-transistors (MOSFETs), which are the typical building blocks of most electronic circuitry. MOSFET gates

control the flow of current through the device, defining the characteristics of such a component in a larger system. The main focus of this research is to observe the effects of radiation exposure on sub-threshold characteristics and power management in MOS devices and circuits, because one of the dominating consequences is the increased leakage currents that result from increased interface state density, which in turn leads to an increase in undesired power dissipation.

1.1 Relevant/Related Work

As with any topic, it is appropriate to review the studies that have previously been conducted to gain the best understanding of the topic at hand. Extensive research has been completed in the area of radiation hardening of semiconductor device components for decades; some work has been completed in circuit applications, but not as much as compared to the device level. Therefore, this section is intended to provide a brief description of the space environment, followed by a review of the literature pertaining to radiation effects. Topics of previous work include studies on radiation effects in MOS capacitors, MOS transistors, techniques for physically measuring the amount of increased interface state density, and techniques to better model these effects, based on acquired data, and compensate the radiation-induced performance degradations. While these areas may tend to be more specific in nature, there exist some more general review papers in this area of radiation effects [1, 8, 11, 18, 21].

The cited literature indicates two things. First, as component geometries scale smaller over time, the amount of easily damaged gate oxide decreases. In general, threshold voltages shift when MOSFETs are exposed to ionizing radiation. This

shifting is known as a "total-dose" (TD) effect, as it is proportional to the total dose of absorbed ionizing radiation. The degree of shifting is also proportional to the volume of the sensitive gate oxide. As these volumes decrease, threshold shifting becomes less of an issue. As a result, the second observation is that research has shifted to what are known as "transient" radiation effects. These include single event upset (SEU) of logic states, usually caused by high-energy ionizing particles incident on the circuits.

Scaling and new material processes can eliminate a considerable amount of the damage caused by TD irradiation; this is particularly true of threshold shifts. But interfaces states are more difficult to control, as they can be formed as a result of mobile charges released in the bulk substrate on which the device is built. Also, most currently used parts are made on commercial factory or foundry production lines, which do not use many of the material hardening techniques currently in use on US Department of Defense (DoD) radiation-hard foundries. In this thesis, the issue of hardness of COTS parts fabricated in a state-of-the-art commercial foundry is revisited. The foundry studied was the IBM CMOS-RF foundry producing the 8RF (130nm) circuit family. In addition, the effects of ionizing radiation damage on integrated circuits composed of components fabricated on this foundry are studied.

1.1.1 Space Environment

The space environment contains a variety of sources and types of radiation particles that cause damage to surrounding electronics and components. Such damage can result from radiation particles like electrons, protons, photons, alpha particles, and other heavy ions [1]. There are several properties that the radiation

damage depends on, including mass, charge and kinetic energy, supporting the notion that each radiation source will have varying effects on the target it strikes. Furthermore, there are five general damage processes that may result from radiation exposure: generation, recombination, trapping, compensation, and tunneling [1], all of which can occur simultaneously or independently. These processes lead to disastrous consequences, one of which being an increase in the leakage current in MOS transistors. Static leakage currents become critically important to the power dissipation of a circuit and will be one of the focuses of this work.

Single event upset (SEU), also considered transient responses, resulting from single high energy particle interactions with integrated circuits is another consequence of radiation and important in natural space environments [2], but not focused on for these studies (for reasons discussed above). Since the environment and phenomena in space cannot be exactly replicated, exposure of circuits to a single form of radiation, rather than multiple forms, is the typical strategy used for experiments to study the resulting characteristics. For the purposes of this research, a Co^{60} gamma ray source was used to emulate total dose exposure of radiation particles. Other forms of radiation sources include electron beam, proton and X-ray irradiations. Table 1 below, [11], presents the different sources, the corresponding type of particle and energy, along with that of the space environment for comparison. Finally, it is worth noting again that this work focuses on total dose irradiation although single event phenomena are also of interest in some circumstances.

Table 1 Total Dose Simulator Characteristics Compared to the Space Ionization Environment

	Particle Type	Energy	Range of Dose Rates rad (SiO_2)/s	Pulse Width
Dynamitron	electrons	2.5 MeV	10^2–10^7	1 ms-dc
LINAC	electrons	5–60 MeV	10^3–10^{10} 10^6–10^{11}	1–10 μs 10–100 ns
^{137}Cs	photons	670 keV	10^{-2}–10^2	dc
^{60}Co	photons	1.1 MeV	10^{-2}–5×10^2	dc
X-ray tubes	photons	10 keV to >100 keV	10^3–10^4	dc
Space	electrons, photons, protons	<1 MeV to >100 MeV	$<10^{-3}$ ave.	variable

Table 1: Comparison of Different Experimental Radiation Sources to Space Levels (from [11])

1.1.2 MOS Capacitors

Again, the most critical material of MOS devices is the gate oxide layer, and the simplest way to study the change in material properties of oxides is to observe the radiation-induced effects on MOS capacitors. Reports have been published on the ionizing radiation effects of MOS capacitors including shifts in the capacitance-voltage (C-V) plots and surface potential plots. Chauhan and Chakrabarti [3] have modeled and shown radiation effects on the high frequency C-V plots for a MOS capacitor fabricated on p-type silicon substrate; these results are reproduced below in Figure 1. The figure illustrates the negative plot shift resulting from irradiation, as well as the validity of the developed theoretical model for analyzing the induced damage.

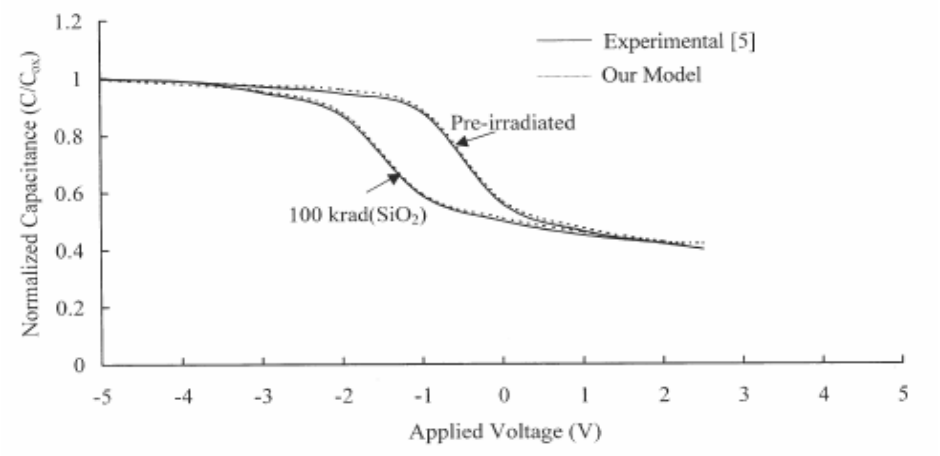


Figure 1: Normalized High Frequency C-V Plot of pMOS Capacitor Before and After Total Dose Irradiation (from [3])

Chauhan and Chakrabarti [3] have further studied the C-V responses during irradiation, and not simply after total dose exposure; see Figure 2 below. It is evident from the curves, that during continuous exposure the shifts depend on the irradiation dose rate, leading to an implicit dependence of the electronics on the surrounding environment. This result can lead to further complications when modeling and designing systems that will be used in radiation environments, which is already difficult enough.

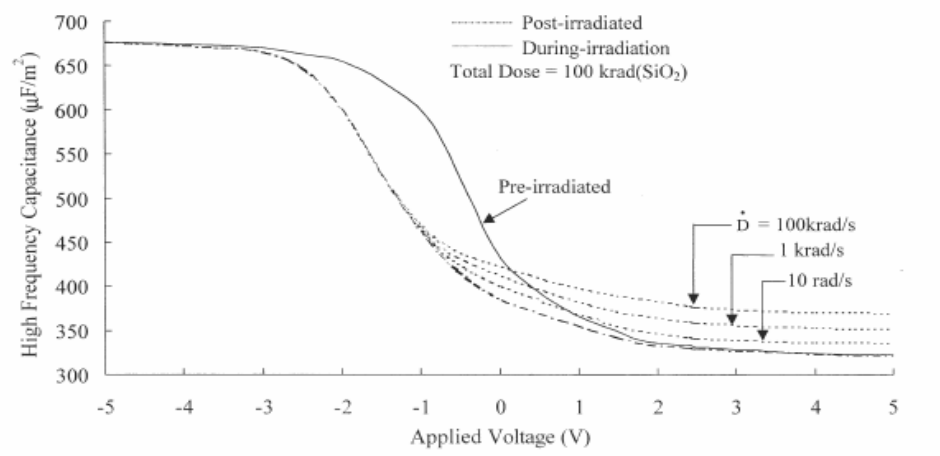


Figure 2: High Frequency C-V Plot of pMOS Capacitor Before, During and After Irradiation (from [3])

Other researchers, such as Candelori et al. [4], have reported on similar effects of total dose exposure, most of which resulting from electron radiation sources. Messenger and Ash [6], among others, have observed "stretching-out" effects of C-V curves as a function of increased interface states. Ma and Dressendorfer [5] have further reported on the shifts in C-V plots as a function of timed electron irradiation pulses, where the plot makes the initial shift and then begins to recover to the pre-irradiation characterization as the number of pulses, and in turn, time, increase.

Related to the work on C-V response shifts resulting from irradiation is the response of surface potential, φ_s, due to exposure. Chauhan and Chakrabarti [3] have also reported on such work, indicating effects similar to those of the capacitance plots. Surface potential was found to have a dependence on the irradiation dose rate, where the potential versus gate voltage plot decreases for increasing dose rate; see Figure 3 below. All of these findings, from both the capacitance- and surface potential-gate voltage plots, become critically important to understanding the current and future device characteristics while in an environment of continuous exposure.

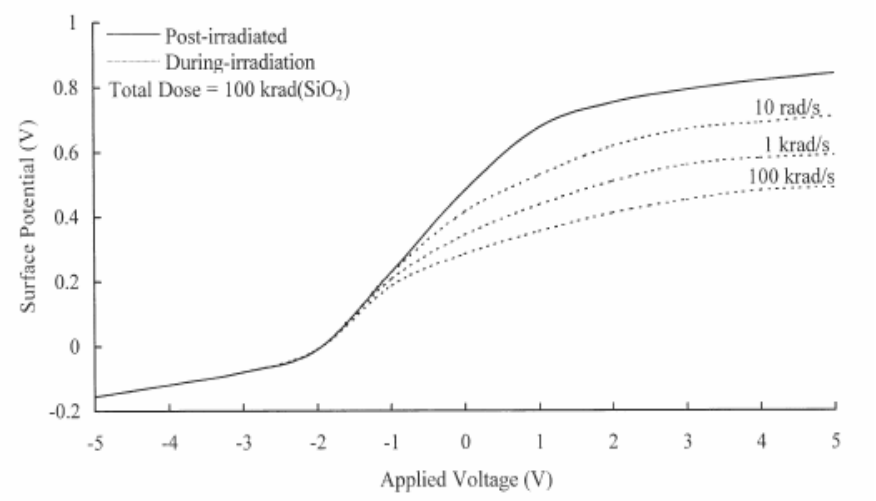


Figure 3: Surface Potential versus Gate Voltage Plot as Function of Dose Rate (from [3])

1.1.3 MOS Transistors (MOSFETs)

Although MOS capacitors represent one of the simplest devices to study the damaging effects of radiation, transistors are of much more interest considering they are the building blocks of electronics. Based on this fact, great amounts of research have focused on transistor related effects due to radiation-induced damage. Studies can be found that focused on damage related to silicon-junction field-effect-transistors (Si-JFETs) [12], power MOSFETs [13-15], and in more exotic processes such as silicon-on-insulator (SOI) transistors [16], and gallium-arsenide (GaAs) transistors [12]. Furthermore, other topics of interest have been in the areas of radiation effects in programmable technologies including FPGAs and flash memory [17, 18].

A considerable amount of information on radiation damage of MOSFETs can be gleaned by studying MOS capacitors. The MOSFET gate region has the same structure as the MOS capacitor and damage in both cases manifests itself as a change in the apparent turn-on voltage. Radiation-induced gate oxide defects include those from trapped oxide charge, N_{ot}, and trapped interface charge, N_{it}, where trapped oxide charge is the net trapped charge in the bulk of the oxide and interface traps are those near/at the oxide-bulk interface [21]. Numerous device characteristics have proven to be affected as a result of these gate oxide defects, such as the threshold voltage [22, 46] (related to the shift in C-V curves of MOS capacitors), sub-threshold swing and leakage currents [23, 24], and transconductance and channel mobility [21, 25], among other characteristics. Figure 4 below shows the trend of threshold voltage versus total dose of radiation for a p-MOS and n-MOS transistor [2].

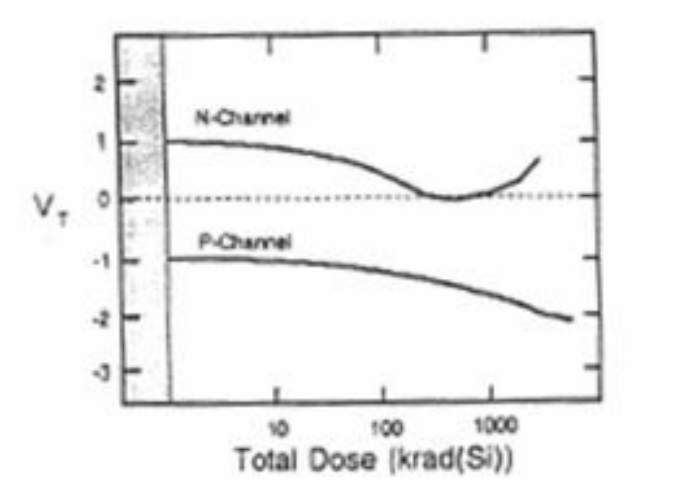


Figure 4: Threshold Voltage Shift in n- and p-MOS Transistors versus Radiation Total Dose (from [2])

In addition, since these effects are present in transistors, they too will have subsequent effects on integrated circuit (IC) performance in areas like speed [21, 45] and functional failure [26]. Some of these characteristics, such as threshold voltage shift, leakage currents, and transconductance have even been shown to have dependencies on the temperature of the irradiation, with the largest changes occurring at lower temperatures around 30 °C [30]. This is an important result since space temperatures can be even lower leading to a potential for even larger variations. Figure 5 below shows this temperature dependence for drain current versus gate voltage plots before and after varying temperature electron irradiations.

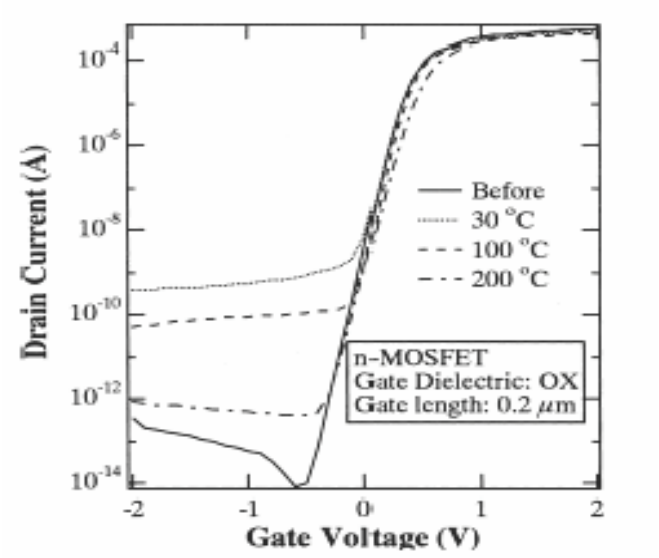


Figure 5: Drain Current versus Gate Voltage for Varying Temperature Electron Irradiations (from [30])

Furthermore, modeling techniques and strategies are necessary to properly account for these radiation-induced effects when designing and simulating, and this has also been an area of research. Some of these studies have included modeling total dose effects in narrow channel MOSFETs [27], and leakage currents of ultra-thin gate oxides [28]. General sub-threshold models have also been investigated [23, 31, 32]. In all cases, it has been noted that the accuracy of sub-threshold radiation modeling can be limited by the sub-threshold model itself. Furthermore, many studies have been conducted to observe interface state generation during and after radiation exposure to then be used in predicting and understanding the process by which damaging effects arise [29]. Finally, just to reiterate, an explanation regarding some of these generalizations can be found in chapter 2 that describes in detail the processes by which radiation induces problems and alters the characteristics of MOSFETs and circuits.

1.1.4 Measurement Techniques

The increase in interface state densities is of prime concern in this study. In general, it may be difficult to know exactly what interface state density is generated based solely on a given total dose exposure; techniques are needed to determine this characteristic. There are a few strategies that have been reported in the literature and will briefly be mentioned here. The first technique is named the Berglund method and utilizes a MOS capacitor to measure the density [7]. The way this technique works is to construct a capacitive divider network, much like a resistive divider, in which the device under test (DUT) is placed in series with a capacitor of known value. By placing a known voltage, typically a small AC signal imposed on a slow-varying DC ramp, across the divider, the measured divider total capacitance is found where the only remaining unknown is the capacitance of the DUT. Generally speaking, the interface state capacitance, C_{it}, which is related to the interface state density, can be solved for using the following equation:

$$C_m = \frac{C_{ox}(C_{sc} + C_{it})}{C_{ox} + C_{sc} + C_{it}} \quad \textbf{(1)}$$

where C_m represents the total measured capacitance, C_{ox} is the oxide capacitance, and C_{sc} is the space charge capacitance. As C_{ox} and C_{sc} are known from either computation or from measurement, equation 1 can be solved for C_{it}. The problem in applying this method is that it's desired to make all capacitance measurements at a given surface potential, or band bending. Berglund has developed a method for ascertaining the surface potential as a function of gate bias to within an additive, integration constant. Generally, it is assumed that minimum C_{it} occurs at mid-band.

Estimates of C_{it} as a function of band-bending can be iterated upon until this condition is reached.

Two other techniques exist that use a MOS transistor rather than a MOS capacitor to measure the interface state density. The first technique requires only the use of the drain current versus gate voltage plot, which is a very standard and trivial testing procedure. For MOSFETs, the sub-threshold swing is a parameter of interest when discussing radiation-induced damage because the swing increases with increased interface state density [49]; this is the underlying principle of the "sub-threshold" method. Ma and Dressendorfer [5] have reported the following equation relating the change in interface state density, ΔD_{it}, with respect to measured swing characteristics

$$\Delta D_{it} = \left[\frac{C_{ox}}{kT \ln(10)} \right] \left(S_{D2} - S_{D1} \right) \quad \textbf{(2)}$$

where C_{ox} represents the oxide capacitance per unit area, k is Boltzmann's constant, T is temperature in degrees Kelvin, and S_{D1} and S_{D2} are the sub-threshold swing measured at radiation level D1 and D2, respectively. This is the method of choice used throughout the simulations and testing for this research.

The second transistor measurement technique, called the charge pumping method, is more complex than the first. For this technique, a reversed bias is applied across the drain and source junctions of the MOSFET with respect to the body contact, followed by a square wave gate voltage to switch the channel under the gate from inversion to accumulation [2, 19, 20]. When the gate voltage is pulsed back and

forth, a pulsed current is generated resulting from charge and discharge of the interface traps. This current is related to the interface trap concentration, N_{it}, by

$$I_{cp} = qfA_g N_{it} \quad \textbf{(3)}$$

where I_{cp} represents the pulsed current, q is the charge on an electron, f is the frequency of the pulsed gate voltage, and A_g is the gate area. This technique can be varied to use different pulse magnitudes and transitions, but the underlying idea remains the same [5].

1.1.5 Reducing Radiation-Induced Effects

Since the radiation-induced damage has been a topic of interest for some time, focus has also been given towards correcting, or at least reducing, the effects. A large collection of radiation hardening techniques can be found in references [8, 21] with regards to complimentary-MOS (CMOS), bipolar (BJT), silicon-on-sapphire (SOS), and gallium-arsenide (GaAs) technologies. Many techniques focus on the areas of design, layout and processing steps to limit the amount of radiation-induced damage [21]. For example, fully enclosed (circular gate) FETs are used to eliminate the effects of sneak-path leakage. Furthermore, different material properties and growth processes have been studied with intensions for counteracting the damage caused by radiation. Such studies, and even submitted patents, have included use of fluorinated oxides to reduce the generation of interface state densities resulting from radiation exposure [9, 10]; however, the effects on MOSFET operation must be greatly understood for this method to be accurate. Finally, as of 2003 Honeywell and BAE Systems [21] were two remaining foundries capable of producing devices and circuits for DoD that are radiation-hardened for environments of around 100KRad using

special techniques and processes. Thus, current efforts have been to use the commercial foundries as well, making it all the more important to understand the impacts of radiation damage on these commercial technologies. Osborn et al. have reported such comparisons of available commercial foundries, including HP, Orbit and AMI technologies [49]. This work builds on these by working in the deeply scaled domain and by including integrated circuit network performance studies.

1.2 Research Motivation and Scope

Traditionally, the sub-threshold power dissipation may be considered negligible in comparison with "crowbar" currents in logic structures; "crowbar" referring to the region where all transistors are turned on and maximum current flows. However, due to the scaling of devices and increase in switching speeds, the hypothesis is that the sub-threshold power is becoming more significant when compared with the "crowbar" power. Furthermore, as a result of radiation exposure the sub-threshold power increases even more, which leads to an even larger impact on the power dissipation of logic devices. Thus, these radiation-induced effects on MOS devices and circuits are studied from the theoretical standpoint via simulations to testing and acquisition of measured data, comprising the main scope of this research.

The initial objective of this work was to gain sufficient understanding of the impacts of radiation-induced damage on MOS device characteristics from a theoretical stand-point to speculate as to how these effects would translate into circuit performance issues. This knowledge led to searching through previous work in related fields to observe practical implications and tests on similar devices. Recent experiments directly associated with power dissipation and radiation have not been

reported and/or found in the open literature, which sparked the interest and motivation in this topic. One conference paper was reported by reference [21] to include potentially related issues, [47], but a full article was not found.

The process used to observe data supporting the hypothesized ideas was to simulate the effects through device model modifications and then conduct tests similar to the simulations for verification. These simulations and experiments were first conducted on MOS devices and then extended to MOS logic circuits. The acquired data was then compared against initial claims to draw necessary conclusions about radiation-induced impact on MOS circuit design. The notion described above about the sub-threshold power dissipation becoming more significant is one of the ideas that are intended to be proven and supported by the simulated and measured data. The total power dissipation is also one of the most important observations to conclude upon following simulated and measured irradiation data. A secondary notion to investigate is the idea that the sub-threshold power dissipation becomes an increasingly important consideration for longer logic chains where more gates are connected in series because of quicker transition speeds. Finally, an overarching objective behind this work is that these results can be coupled with other research environments, for instance ultra low temperature, to best understand, model and design systems that can withstand the harsh phenomena and environments in space.

1.3 Report Structure

In chapter 2, the background information necessary to understand the effects of radiation on MOS transistors will be presented, including some important notes on semiconductor physics and generation of radiation-induced damage. Such effects

include threshold voltage fluctuations, sub-threshold swing degradation and other alterations of physical parameters. The damage to MOS devices from radiation will then be extended to circuits to describe the resulting decline in performance because of these radiation-induced effects. The most important result from this discussion, which is used throughout this work, is the fact that radiation exposure leads to an increase in the interface state density of MOS structures.

In chapter 3, individual MOS devices will be more specifically discussed and presented. Simulated data obtained using the IBM 8RF 0.13μm CMOS technology and Cadence software package will be given. The experiments for conducting individual transistor tests prior to and after irradiation exposure will be provided as well. The measured data acquired from the radiation tests will be given for various sized n-MOS and p-MOS transistors. Further measured data will be presented for larger, commercial transistors of two commercial inverter chips: MC14007UB and CD4007UBE. Comparisons will then be made between the pre- and post-irradiation data, the simulated and measured data, and the sizing and types of transistors.

In chapter 4, effects of radiation-induced damage on circuit performance will more specifically be presented and focused on for logic structures. Again, the simulated data for the power dissipation of a chain of logic inverters will be displayed as a function of interface state capacitance; this capacitance is used to model the radiation-induced defects. The trends of the power dissipated will be the important consideration for these simulations, along with the effects of increasing sub-threshold power. Furthermore, the measured data obtained via individual transistor measurements and irradiations will be used in additional simulations to project the

power for the actual irradiation levels. Finally, the radiation-induced power effects on an 11-stage ring oscillator are simulated and presented, similar to the logic chains.

In chapter 5, the final conclusions from this work will be discussed. Primary focus will be on comparing the initial hypotheses with the observed data via simulations and measurements. The contributions of this research, as well as future work in the area of radiation-induced power damage will bring this report to a close.

Chapter 2: Radiation Damage

The mechanism of TD damage seems to be fairly consistent from exposure source to exposure source. Damage is confined to charging of the oxide insulating layer (SiO_2), of MOS devices; this gate layer is the most sensitive element of MOS structures in terms of ionizing radiation [5]. Thus, the scope of this chapter is to provide adequate explanations of the generation process of radiation-induced damage, followed by an extension of these effects to resulting consequences of device and circuit performance. Furthermore, discussions will emphasize and center around increasing interface state densities resulting from radiation exposure, although other consequences can occur as well.

2.1 Semiconductor Physics

A brief background will be given here on semiconductor device physics to aid in later explanations and understanding of radiation-induced damage. The scope of this brief description will only include information that is relevant to the topic; many books have been published, and can be viewed, that provide much more detailed descriptions of device physics, including reference [32].

2.1.1 Energy Band Diagrams

Some of the most important diagrams for understanding and studying semiconductor device physics are the energy band diagrams and the band-edge versus position diagrams. These two types of diagrams are often closely related, if not

identical, because the band-edge versus position diagram tends to simply incorporate multiple energy band diagrams of the materials composing a given system. The energy band diagram for silicon is shown below in Figure 6. The forbidden gap is the region defined between the bottom of the conduction band edge, E_c, and the top of the valence band edge, E_v, and is so named because electrons are considered incapable of occupying the energy levels within this gap for a pure Si material. Furthermore, the difference in levels is called the bandgap of the material; for silicon the bandgap energy is about 1.12eV at 300K [32]. At room temperature, this energy barrier is small enough that limited amounts of electrons are capable of excitation from the valence to conduction band leading to partial conductivity; this is what makes silicon a semiconductor material, rather than pure metal or insulator. The Fermi level, E_f, is another important energy level in the diagram and it represents the energy at which the probability of occupancy by an electron is one half. These diagrams will become important when discussing the properties of interface states generated by irradiation.

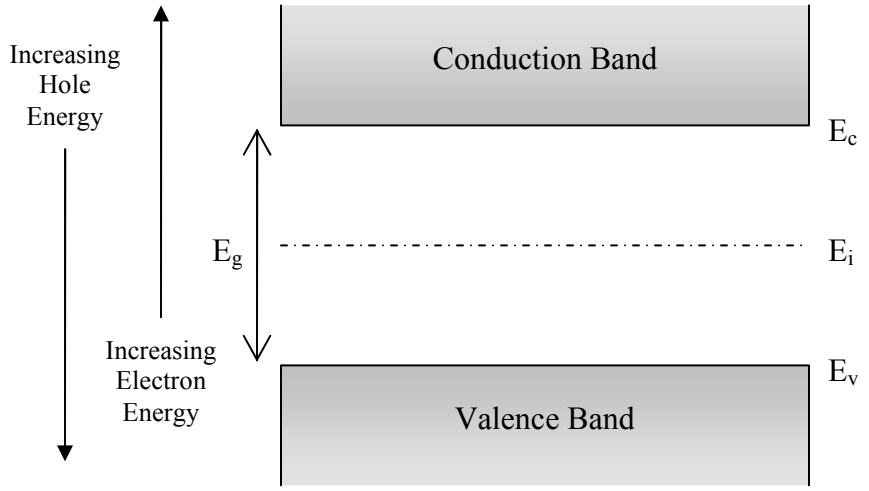


Figure 6: Energy Band Diagram of Intrinsic Silicon (based on [32])

More specifically, the figure above portrays the energy diagram of intrinsic silicon, which is not the typical material used in microelectronic design. Extrinsic silicon, the preferred material of choice, is doped with impurities to alter the electrical properties of the original silicon. These impurities, or dopants, are one of two types, donor or acceptor, and introduce new levels of energy within the forbidden gap capable of being occupied by electrons. Donor dopants become positively charged when ionized resulting in n-type material in which electrons dominate electrical conductivity [32]. Conversely, acceptor dopants become negatively charged when ionized resulting in p-type material where electrical conductivity is governed by holes, or the absence of electrons [32]. The impurities also affect the Fermi level, E_f, of silicon which is a parameter that determines the operating conditions of the silicon material; the Fermi level moves toward the conduction band and valence band for n-type and p-type silicon, respectively. Donor impurities above the Fermi level will contribute to conduction, whereas acceptor impurities below the Fermi level will contribute to conduction; those donors and acceptors below and above the Fermi level, respectively, become de-ionized. The energy band diagrams of n- and p-type extrinsic silicon are shown below in Figure 7, where E_d and E_a represent the energy levels associated with the donor and acceptor impurities, respectively [32].

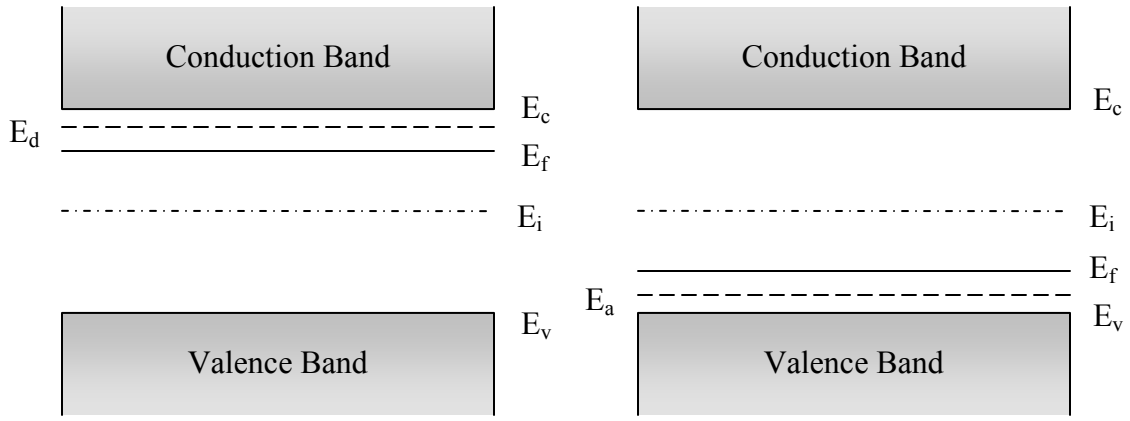


Figure 7: Energy Band Diagrams for N- and P-type Extrinsic Silicon (based on [32])

2.1.2 Characteristics of an MOS System

A MOSFET is an example of a metal-oxide-semiconductor (MOS) system, shown below in Figure 8, where the metal electrode serves as the gate contact of the transistor. The metal could also be replaced with a doped poly-silicon material, which is typically done in modern VLSI technologies. The band-edge versus position diagram is, of course, dependent upon the applied gate voltage. One such diagram, for a poly-silicon gate, is given below as an example in Figure 9 for positive gate biasing [32].

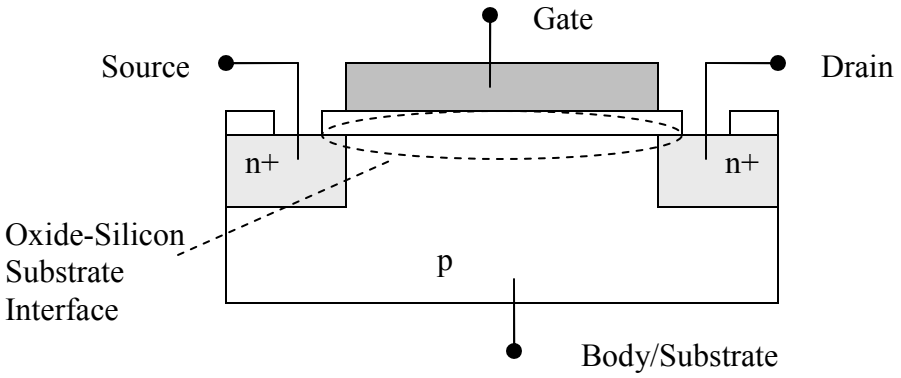


Figure 8: Schematic Cross Section of a n-MOSFET System

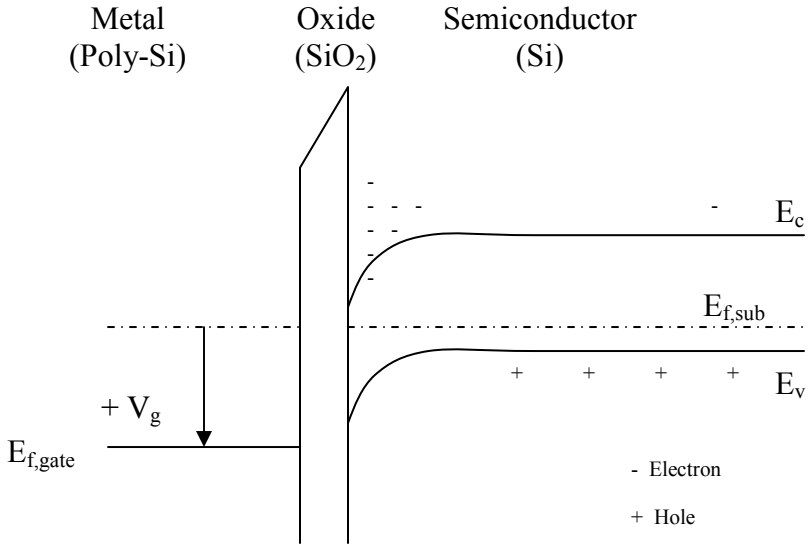


Figure 9: Band Edge versus Position Diagrams for a Poly-Gate n-MOSFET under Inversion Gate Bias Condition

Additionally, Figure 9 illustrates the condition of band bending that occurs in all MOS systems, both MOS transistors and capacitors, as a result of applied gate voltage. Depending on the magnitude and sign of the bias, bending of the energy bands in the silicon substrate will occur. The Fermi level remains constant [32], as gradients in the Fermi level create charge currents. As transport in the direction of

the gate oxide from the bulk is blocked by the oxide insulator, there can be no net transport in this direction and the Fermi gradient is zero. But the separation of the Fermi level from the band edges will change as a result of gate-bias induced band-bending. This alters the density and type of mobile and fixed carriers at the oxide-silicon interface.

Inversion, also portrayed above in Figure 9, is one of the operating conditions of an MOS system in which the material in the region directly below the gate oxide is effectively inverted, hence the name, acting like the opposite material type [32]; a p-type substrate will be effectively inverted to n-type material under the gate, and vice versa. This condition is favorable for a MOSFET device because it allows considerable current flow from drain to source under the influence of a potential difference. The gate voltage corresponding to the inversion condition is called the threshold voltage, V_{TH}, of the transistor, and is related to the band bending and surface potential of the substrate.

Ideally, the oxide material would be completely free of imperfections, but in a practical sense this is not the case. Oxide defects exist that further contribute to modifications of the surface potential, and threshold voltage, of the MOS device. There are four main types of oxide defects: mobile ionic charge, oxide trapped charge, fixed oxide charge, and interface trapped charge [32]. While these must all be accounted for when analyzing devices, only interface trapped charge, and/or states, will be considered here because this work focuses on the increase of interface state densities resulting from radiation exposure.

An interface trap, corresponding to an interface state, occurs as a result of a dangling silicon bond located directly at the oxide-silicon interface, hence the name. The dangling bond is usually the result of the interface being oxygen deficient [37], resulting in SiO_x material where x = 2 for "dangling-bond-free" oxide. Typically, the trap must exist within one or two bond distances, around 0.5nm, from the interface to allow for quantum mechanical transitions of the electrons and holes of the silicon conduction and valence bands into and out of these interface states [5]. Thus, interface traps/states introduce extra energy levels within the forbidden gap that can be occupied by an electron. Furthermore, these states can exist along the entire surface. However, the fluctuations resulting from the additional interface states become dependent upon the surface potential of the oxide-silicon interface because only certain states will contribute to changes. Moreover, the time constants associated with these states become dependent upon the position of the energy levels within the forbidden gap, where traps located more toward the midgap level will take longer to respond than those traps located closer to the band edges [5]. Further discussion of the nature and properties of interface states will be given in the next section, following a description of the process by which additional interface states are generated as consequences of irradiation. A diagram showing the relative position of interface states in the MOS system is shown below in Figure 10.

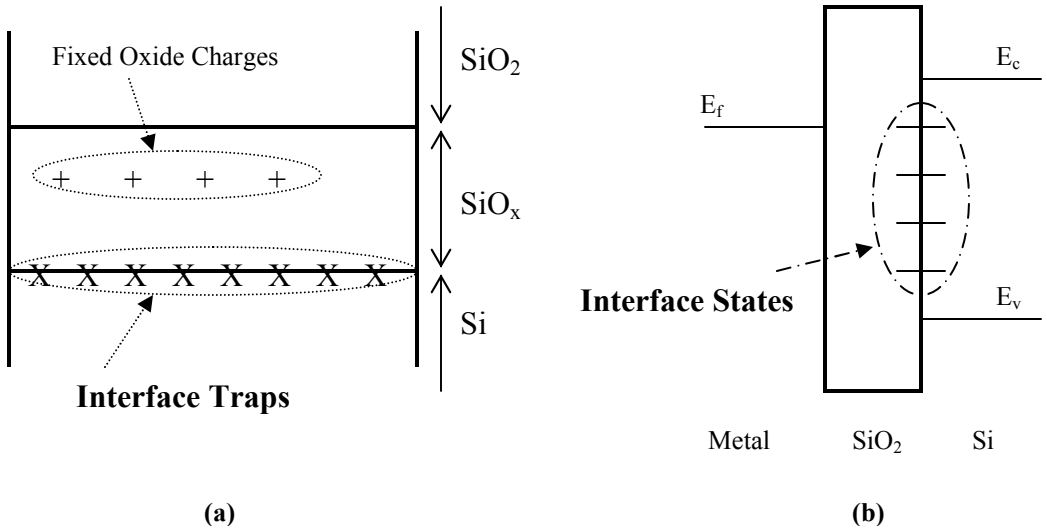


Figure 10: Illustration of (a) Physical Location and (b) Energy Level Position of Interface States in an MOS System

2.2 Radiation-Induced Interface State Generation/Contribution Process

Damage from ionizing radiation happens when this radiation is absorbed in the oxide layer. Most radiation encountered in device operation is too low in energy to cause "displacement" damage – i.e., knock-out of a substrate atom from its equilibrium position. In most cases, an electron-hole pair is created in the oxide. The electron is far more mobile than the hole; experiments have discovered that one electron-hole pair requires about 18eV [33], or 17 ± 1eV [34] of energy for generation. With a positive bias applied to the gate electrode, the created electrons are quickly swept out of the oxide leaving the less mobile holes behind. Mobility of electrons and holes in silicon dioxide are about 20 $cm^2V^{-1}s^{-1}$ and 10^{-4} – 10^{-11} $cm^2V^{-1}s^{-1}$, respectively, giving rise to the quick electron sweeping [5]. Some recombination of the electron-hole pairs will occur, but again recalling the speed with which the radiation-generated electrons move and the very small time window for the recombination, it is not as significant to consider.

Therefore, under low gate-bias conditions, the radiation-induced holes that do not recombine will remain in their initial generation position. However, for a continuous positive applied bias on the gate, even these holes will eventually undergo a transport process toward the oxide-substrate interface [5]. This transport process terminates when the hole is trapped taking one of two forms, where one depends on the substrate surface potential and the other is independent of this surface potential. The independent traps are called "positive oxide traps" whereas the dependent traps are called "interface traps" or states [5]; these positive oxide and interface traps are the same as the fixed oxide and interface trapped charges, respectively, that were previously discussed in section 2.1.2. Figure 11 below illustrates this initial generation and transport process of the electrons and holes, along with the positions of the two trap types.

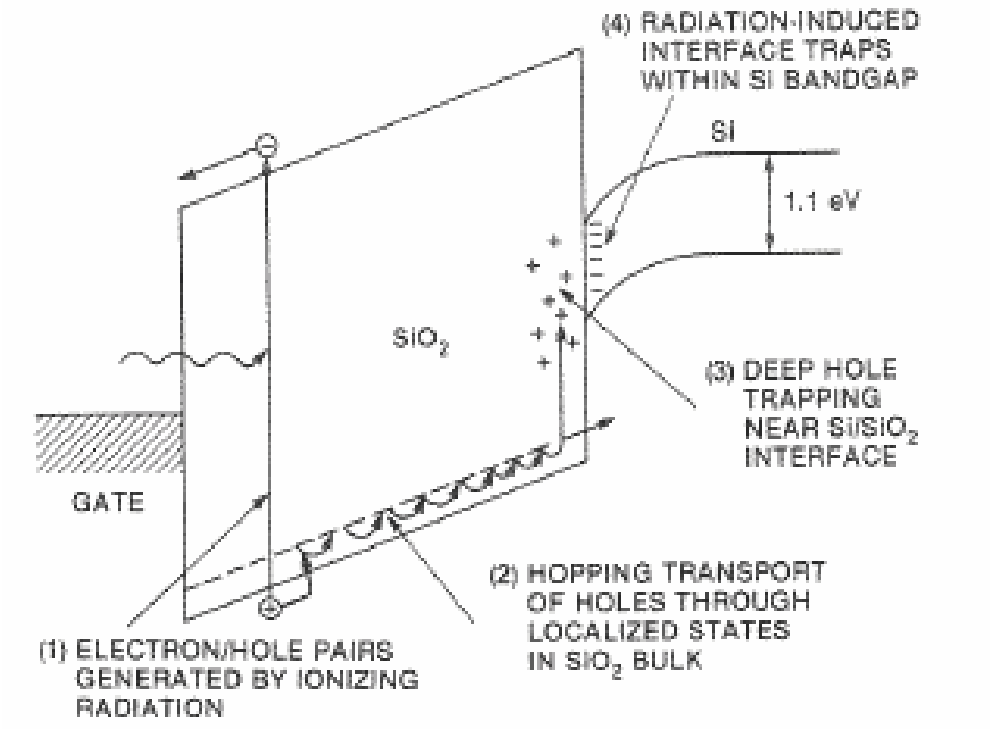


Figure 11: Generation and Transport Process of Radiation-Induced Electron-Hole Pairs (from [5])

2.2.1 Interface State/Trap Characterization

Due to the fact that the interface traps result from dangling silicon bonds at the oxide-substrate interface, these traps become dependent upon the surface potential of the silicon substrate. Furthermore, interface traps can be net charged positive, negative or neutral, depending on the allowable charge states of the trap [5]. Much like extrinsic impurities introduced in bulk silicon, interface traps can also be donor-like and acceptor-like in nature. Conventionally, trap energy levels above midgap exhibit acceptor-like characteristics, and those levels below midgap exhibit donor-like behavior [5]. Only those donor-like interface states above the Fermi level will contribute to device variations by donating an electron for conduction, resulting in a net positive charge. Similarly, only those acceptor-like interface states below the Fermi level will contribute to device fluctuations by accepting an electron, or donating a hole, which results in a net negative charge. The remaining donor-like and acceptor-like states above and below the Fermi level, respectively, are in charge neutral states, which is the reason no changes result from these states. Simply putting it, interface states above the Fermi level will be in its more positive charge state and its resulting contribution to variations will depend on the nature of the trap [5].

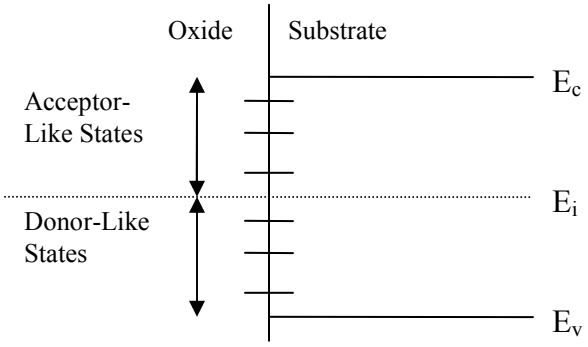
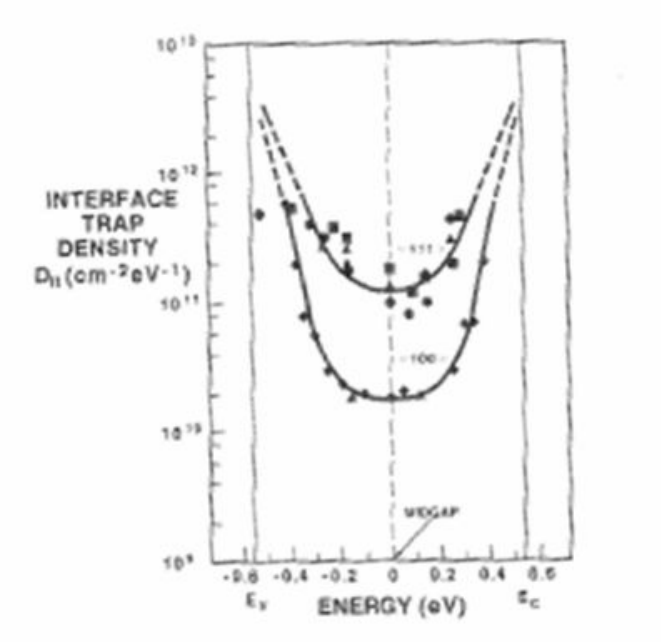
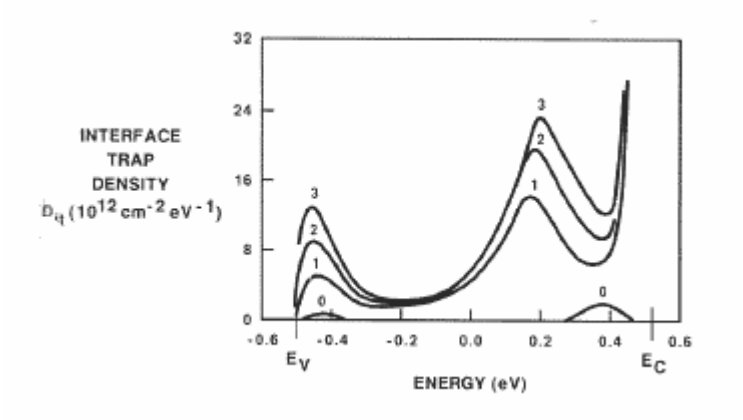


Figure 12: Nature of Interface States in Relation to Silicon Band Diagram

Also important to note is the distribution of interface traps relative to the energy levels in silicon. Prior to irradiation, the interface distribution follows a U-shaped curve as portrayed in Figure 13(a) below. The post-irradiation distribution tends to follow the same U-shaped curve, but one important contrast is the presence of "characteristic" peaks centered near specific energy levels; this is also shown below in Figure 13(b). It was reported that these peaks result for higher levels of radiation exposure [5]. It is important to note that interface state generation can be triggered by mobile carriers introduced in the silicon wafer bulk and not just in the oxide. Holes generated in the bulk, for example, can migrate to the interface creating broken, or dangling, bonds and surface relaxation. Thus, interface state generation is still significant, even as the gate oxide volume is reduced.



(a)



(b)

Figure 13: Example of (a) Pre- and (b) Post-Irradiation Interface Distributions versus Energy Levels in the Silicon Gap (from [5])

2.2.2 Interface State Example

Figure 12 above shows a general picture portraying the nature of the interface states in relation to the band diagram of bulk silicon; a simple example may help with better understanding the contributions of the interface states. Consider the example band edge versus position diagram below in Figure 14 that helps illustrate the band bending dependence of the interface state induced changes. For simplicity, assume all interface states are donor-like in nature and the device operating in inversion on a p-type substrate.

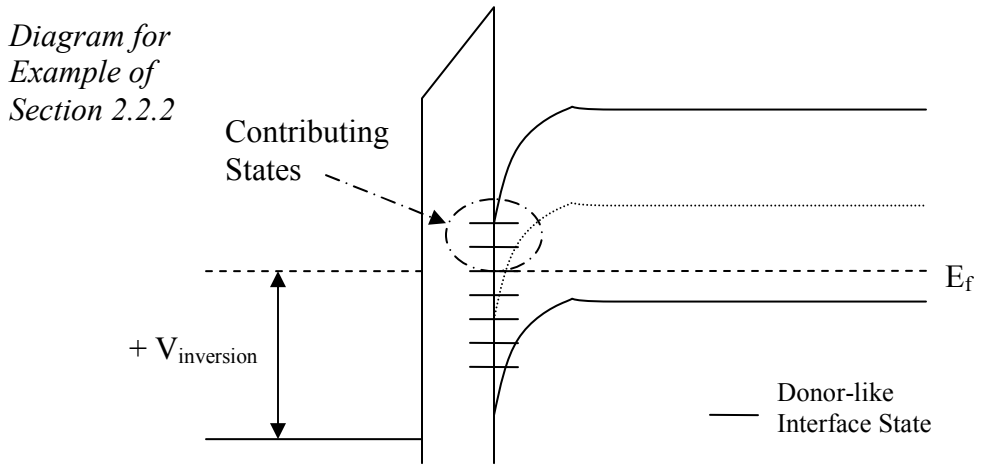


Figure 14: Example of Interface State Dependence on Band Bending

From the diagram above, the band bending, or surface potential, at inversion is assumed to be about 0.7V where only a fraction of the total donor states will result in changes; contributing states are those above the Fermi level and are circled in the example diagram. Moreover, the Fermi level is constant throughout the silicon substrate, and the bandgap of silicon is known to be 1.12eV, corresponding to 1.12V, and a 0.551V midgap. Finally, the difference between one half the bandgap of silicon, about 0.55V, and one half the total band bending, about 0.35V, which equals 0.2V, corresponds to the region of interest. Thus, converting this voltage into a percentage, via the ratio of 0.2V to 1.1V, results in approximately 18.2% of the donor-like interface states contributing effects to the device. While more complex situations arise in practical devices, this example portrays the main principles behind interface state induced effects.

2.3 MOS Device Effects

While the necessary background is now in place, it's even more important to analyze the effects of the additional radiation-induced interface states on device performance. The major MOSFET characteristic changes that occur because of radiation exposure relate to the threshold voltage, V_{TH}, sub-threshold swing, S, and leakage currents, I_{leak}. This section will describe the effects of increased interface state density from irradiation on the individual device parameters.

2.3.1 Threshold Voltage

In general, the threshold voltage shifts for MOS transistors follow the same trend as in Figure 4 in section 1.1.3 above. These shifts are the result of the

additional positive oxide traps and interface traps from radiation exposure, and thus the shifts can be broken down into individual contributions from each type of trap. While positive oxide traps are not the main focus of this work, it is still important to at least consider them when relating the shifts due to interface traps. Typically, MOS transistors operate under strong inversion where the gate bias is larger than the threshold voltage of the device. Under such conditions, interface traps in n-MOS transistors tend to contribute negative charge to the conduction band and thus exhibit a positive shift in the threshold voltage. Conversely, under similar conditions, the interface traps in a p-MOS transistor tend to contribute positive charge resulting in an effective negative shift in the threshold voltage. The relationship between the concentration of interface states at the oxide-silicon boundary, N_{it}, and the threshold shift, ΔV_{TH} or ΔV_{it}, is represented as [2]:

$$\Delta V_{TH} = \Delta V_{it} = \frac{q}{C_{ox}} \Delta N_{it} \quad \text{for n-MOS} \tag{4}$$

$$\Delta V_{TH} = \Delta V_{it} = -\frac{q}{C_{ox}} \Delta N_{it} \quad \text{for p-MOS.} \tag{5}$$

Positive oxide traps contribute positive charges regardless of the applied gate bias, where the resulting threshold voltage fluctuation is similar to that for a p-MOS represented as:

$$\Delta V_{TH} = \Delta V_{ot} = -\frac{q}{C_{ox}} \Delta N_{ot} \tag{6}$$

where ΔV_{ot} and N_{ot} are the oxide trap voltage shift and oxide trap concentrations, respectively. Furthermore, it is important to separate the threshold voltage shifts shown in Figure 4 to the individual parts associated with the trap type. Figure 15

below illustrates this breakdown in a n-MOS transistor where the positive oxide and interface trap contributions increase and decrease, respectively, for larger total doses.

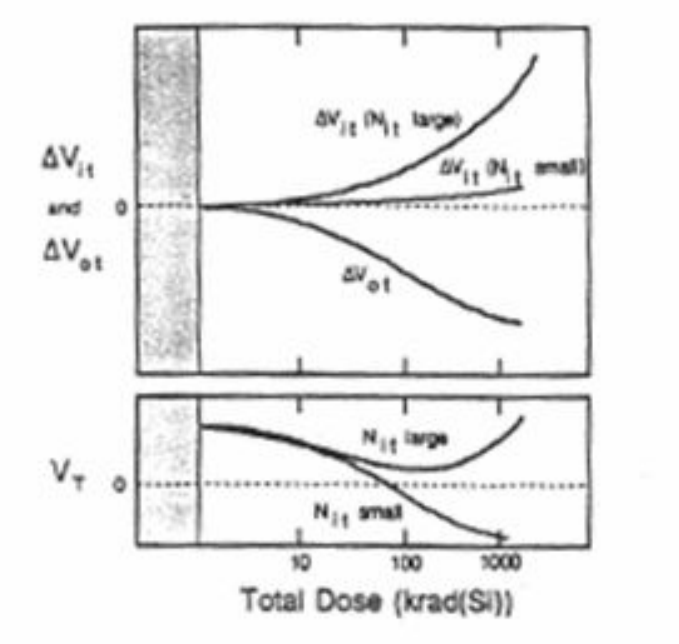


Figure 15: Breakdown of Threshold Voltage Shifts into Individual Contributions from Positive Oxide Traps and Interface Traps (from [2])

2.3.2 Sub-Threshold Swing

A figure of merit when talking about the sub-threshold region of operation is the sub-threshold swing of the transistor, denoted S; see Figure 16 below for a graphical portrayal. This is also sometimes known as the reciprocal of the sub-threshold slope, and is defined as the inverse ratio of the logarithmic change in drain current to the change in applied gate voltage [36]. Since the sub-threshold drain-source current, I_{ds}, is exponentially related to the gate voltage, V_g, translation of this definition into terms of circuit parameters yields the following equation [32]:

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{sc}}{C_{ox}} \right) \quad (7)$$

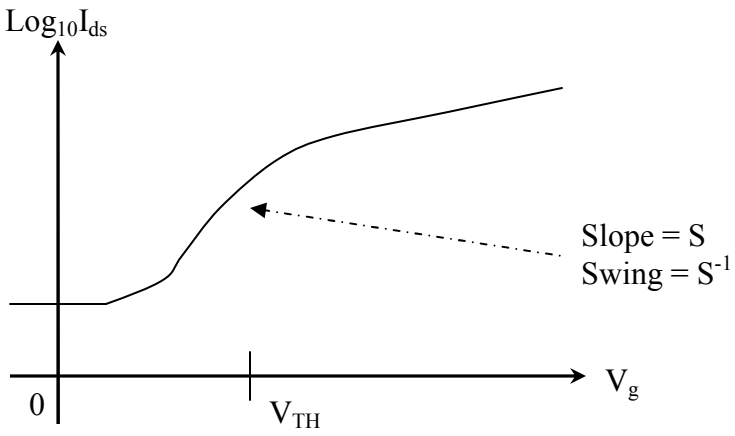


Figure 16: Graphical Portrayal of the Sub-Threshold Swing Device Characteristic

In equation 7 above, the term C_{ox} represents the oxide capacitance per unit area, C_{sc} represents the space charge capacitance per unit area, k is Boltzmann's constant, T is the temperature and q is the charge of an electron; a schematic illustration of the capacitance terms is given in Figure 17(a) below [32]. From the equation, it is clear that for a typical transistor the sub-threshold swing is a constant parameter. This has to do with the notion that the oxide capacitance per unit area is constant for a given fabrication process, and the space charge capacitance per unit area remains relatively constant; standard swing values tend to vary between 70-100 mV/decade [32].

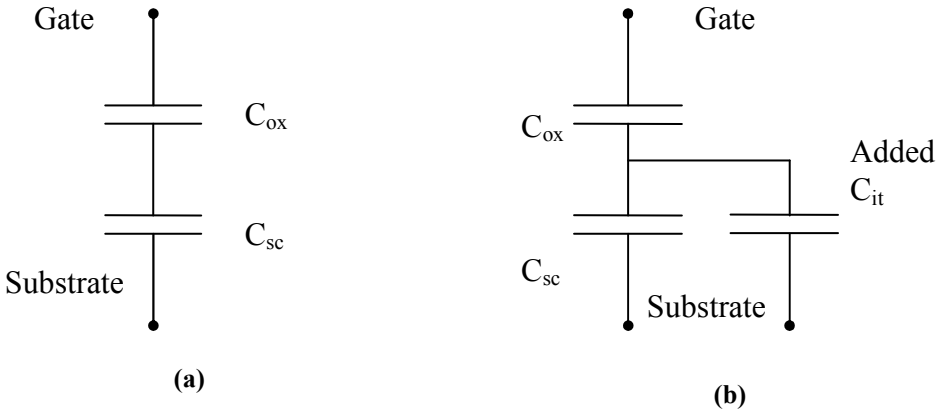


Figure 17: Schematic of Capacitances Associated with (a) Pre- and (b) Post-Irradiated MOS Transitors [32]

Following radiation exposure, the resulting interface states contribute an additional capacitance in parallel, C_{it}, with the space charge capacitance as portrayed in Figure 17(b) above. Clearly, since more interface states arise from higher doses of irradiation, this term also increases for larger levels of radiation exposure. A further consequence of the additional interface capacitance is a modification of the sub-threshold swing equation to contain this added term, given below in equation 8 [23]. Thus for an increase in the radiation exposure, and in turn the interface state capacitance per unit area, the sub-threshold swing follows a linearly increasing trend as well.

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{sc} + C_{it}}{C_{ox}} \right) \quad \textbf{(8)}$$

2.3.3 Leakage Current

An important device characteristic when considering operation and power dissipation is the leakage current of the transistor. Circuit design tends to keep a transistor in the "off" state when it is not required to perform the given functionality, The component current must be negligible under this condition. However, radiation exposure reduces the control of the gate oxide over the current flowing through the transistor. Another way of interpreting the sub-threshold swing parameter is the amount of necessary gate voltage to "turn off" a decade of drain current. Therefore, comparing similar sized devices at increased total dose levels with ones at decreased or non-irradiated levels results in a larger sub-threshold, or leakage, current of the higher dose transistors for a given gate voltage. Effectively, the gate looses control of the active channel density, and the device requires wider voltage swings to shut off.

Another source of leakage that must be considered is called "sneak-path" (SP) leakage. Here, the radiation-soft boundary between the gate and field oxide charges more strongly under irradiation than would normally be the case. This permanently turns on an active channel from source to drain. This channel is very narrow and doesn't necessarily destroy device function. It does contribute to power dissipation, though.

For purposes of this work, leakage currents are all grouped together into one main leakage current that was just explained in this subsection. This generalization includes such leakage sources as the gate oxide, "sneak" path leakage from the field oxide surrounding the active device window, and all other existing leakages while a transistor is in the "off" state.

2.4 MOS Circuit Effects

Ultimately, the MOSFET effects discussed above lead to further performance problems with integrated circuits, and more specifically in logic structures, which is the principle idea behind the motivation for conducting this research. The radiation-induced device changes in threshold voltage, sub-threshold swing, and leakage current in the individual transistors lead to issues in power dissipation of logic structures and circuits. More specifically, the transistors remain in the sub-threshold region of operation for extended periods of time where the sub-threshold power dissipation becomes not as negligible in comparison with "crowbar" power. This section will explain how the transistors spend longer times in sub-threshold, how this results in variations of power dissipation, and how these relate to the concepts speculated upon in the motivation section 1.2, of the introduction chapter.

2.4.1 Increased Sub-Threshold Region

The sub-threshold region of operation refers to the voltages where the transistor is out of cut-off near linear triode region but still does not have a fully inverted channel under the gate. More specifically, the sub-threshold region is defined as the region where the gate voltage is between $1\varphi_b$ and $2\varphi_b$; this is the definition of sub-threshold used for this research, and is reproduced below in equation 9 for easier referencing. Moreover, this also directly relates to the amount of band bending of the silicon substrate energy levels.

$$\textit{Sub-threshold Region Definition}: \quad 1\varphi_b \le V_g \le 2\varphi_b \tag{9}$$

The term φ_b is known as the quasi-Fermi potential of the bulk silicon substrate, and can be solved for using the threshold voltage. The equation relating these two terms is given as:

$$V_{TH} = 2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_a (2\phi_b)}}{C_{ox}} \tag{10}$$

where V_{TH} is the threshold voltage, φ_b the quasi-Fermi potential, C_{ox} the oxide capacitance per unit area, q the charge on an electron, N_a the doping concentration of the inversion channel or substrate, and ε_{Si} the permittivity of silicon. While equation 10 represents V_{TH} as a function of φ_b, simple manipulation of the equation, using the quadratic formula with respect to $\sqrt{\phi_b}$, will yield an explicit solution of φ_b in terms of V_{TH}, given below in equation 11.

$$\phi_b = \left[\frac{\sqrt{qN_a\varepsilon_{Si}}}{2C_{ox}} \pm \frac{\sqrt{qN_a\varepsilon_{Si} + 2V_{TH}C_{ox}{}^2}}{2C_{ox}} \right]^2 \tag{11}$$

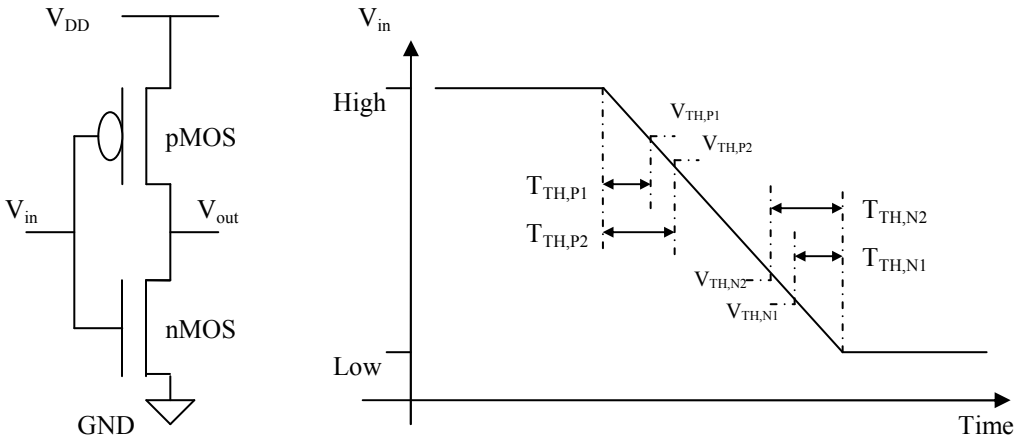
Notice that the equation for φ_b contains a plus-minus sign, but typically the two values are fairly close together where the difference can be considered negligible. Furthermore, based on these equations the sub-threshold region of operation can generally be approximated with fairly good accuracy by:

$$\textit{Sub-threshold Region Approximation}: \quad \frac{V_{TH}}{2} \le V_g \le V_{TH}. \tag{12}$$

This approximation assumes that the second term of equation 10 is small in comparison with the first term, resulting in $V_{TH} = 2\phi_b$. Similarly, this estimate will occur from equation 11 assuming the second term is larger than the first, and that $qN_a\varepsilon_{Si}$ is considerably smaller than $2V_{TH}C_{ox}^{\ 2}$. Finally, it is clear that for higher threshold voltages resulting from radiation exposure, the region of sub-threshold operation increases as well.

This increase in the sub-threshold region further relates to switching in logic structures. For instance when the input gate of an inverter, which consists of an n-MOS and p-MOS transistor and shown below in Figure 18(a), switches from high to low the p-MOS transistor switches from cutoff to sub-threshold to saturation and the n-MOS from saturation to sub-threshold to cutoff. These switching characteristics are shown below in Figure 18(b), and are slightly exaggerated for illustration purposes. As was briefly touched upon in the introduction, the "crowbar" region of operation occurs when maximum current flows through the gate and this happens when both transistors are in their respective saturation regions. Therefore, considering the switching takes place over a given period of time, more of this time interval will correspond with sub-threshold operation for larger threshold voltages associated with

the individual devices. This is shown in Figure 18(b) where the times $T_{TH,P2}$ and $T_{TH,N2}$, corresponding to the larger threshold voltages $V_{TH,P2}$ and $V_{TH,N2}$, respectively, are larger than the those times, $T_{TH,P1}$ and $T_{TH,N1}$, corresponding to smaller threshold voltages $V_{TH,P1}$ and $V_{TH,N1}$, respectively. Furthermore, this will deduct from the amount of available time the device can operate in the "crowbar" region. This has further implications when concerning power dissipation, which is the topic of the next subsection.



(a) **(b)**

Figure 18: (a) Schematic Representation of an Inverter, and (b) Illustration of an Inverter Switching Characteristics

2.4.2 Power Dissipation Issues

The increased time spent in sub-threshold of the transistors of an inverter corresponds to an increase in the average amount of sub-threshold power dissipated for this logic gate. This can easily be seen from the equation for average power:

$$P_{average} = \frac{1}{T}\int_0^T v(t)i(t)dt \qquad \textbf{(13)}$$

where v(t) represents the drain-source voltage across transistor, i(t) the current through the transistor from drain to source, and T the period. For sub-threshold

average power, the integration takes place over the amount of time spent in sub-threshold and the current represents the sub-threshold leakage. In logic structures, such as inverters, the drain to source voltage tends to simply equal the rail voltage, which remains constant and is independent of time. Simple multiplication and division following the integration of the current over the region can calculate the average sub-threshold power dissipated. More time spent in sub-threshold corresponds to a larger value of the integral and a subsequent increase in the average power associated with sub-threshold. Furthermore, increased sub-threshold swing characteristics and larger leakage currents directly lead to larger average power dissipation values as well.

While the magnitude of the average power dissipated in sub-threshold is an important parameter by itself, it has further implications related to the average power dissipated over a switching cycle in an inverter. A switching cycle can correspond to either a transition from low-to-high or high-to-low of the input gate voltage. As was described in section 2.4.1, during a switching cycle an inverter has two associating sub-threshold regions; one each for the n-MOS and p-MOS transistors. Thus, the total average sub-threshold power dissipated over one cycle is the sum of powers during both regions. Since the p-MOS and n-MOS transistors are connected in series, the current flow through the gate is limited to the operation of one or both of the individual transistors. Intuitively, in the "crowbar" region the limitation in current flow does not relate to sub-threshold because both transistors are on. However, when either transistor is in sub-threshold, the current is limited to the leakage current flowing through the device under sub-threshold conditions. Figure 19 below shows

the expected current flow through an inverter during a switching cycle from low-to-high.

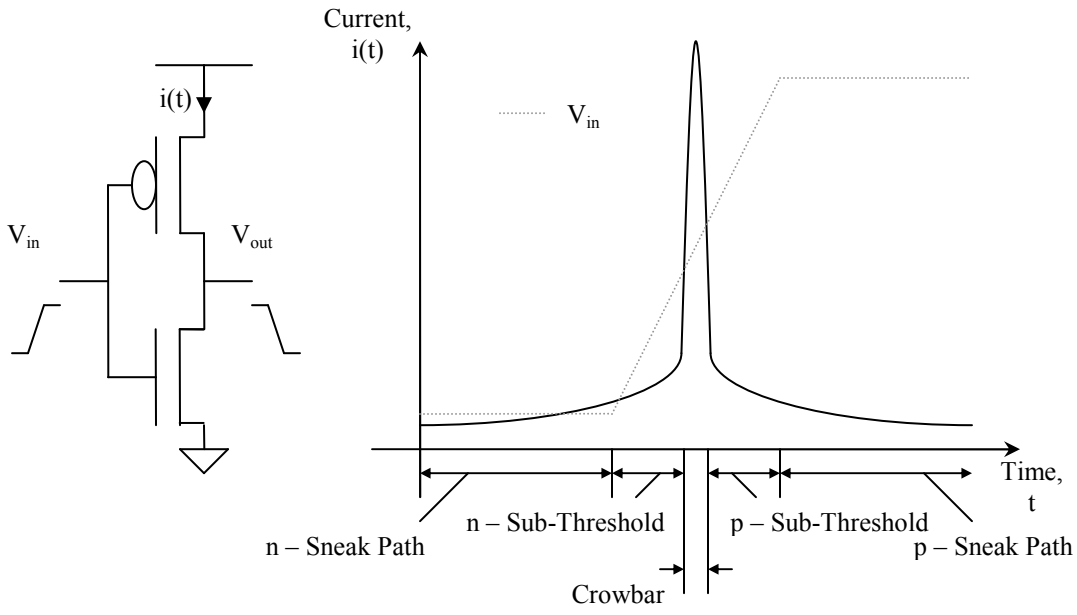


Figure 19: Illustration of Current Flow During an Inverter Switching Cycle

It is clear from the figure above that if either transistor, or even just one, remain in sub-threshold for a longer time, the total average power associated with sub-threshold over this switching cycle will rise as well. Effectively, this subtracts from the time spent in the "crowbar" region of operation where maximum current flows and where it is considered that the significant power dissipated occurs. In other words, a consequence of radiation-induced damage is that the ratio, or percentage, of total average sub-threshold power to total average power over one cycle will increase and become more important to consider. Increasing sub-threshold power directly adds to the total power of the given structure, increasing it as well.

If this increased power dissipation is considered negligible, more logic structures and inverters connected together will result in even larger inaccuracies in determining the total power associated with a circuit. For example, inverter chains

are typically used as output buffers to drive larger capacitive loads like bond pads. Theoretically, this ratio of sub-threshold to total average power dissipated over a switching cycle will become even larger for stages further toward the end of the chain because the switching transitions get faster and faster. An example illustration of these quicker transitions is shown below in Figure 20 for a six stage inverter chain; a stage simply corresponds to an inverter. Therefore, for faster transitions from high-to-low or low-to-high, the interval of time associated with the "crowbar" region will be smaller. This translates into the p-MOS and n-MOS transistors remaining in sub-threshold longer, further supporting the importance of considering this effect as a result of increased radiation exposure leading to device degradation.

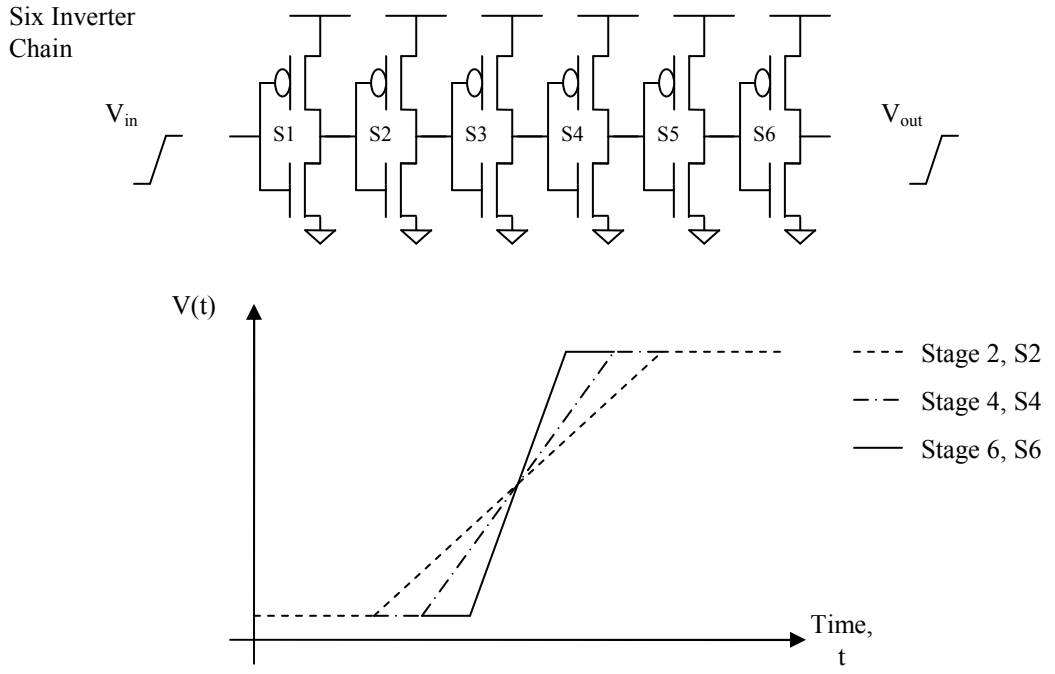


Figure 20: Example Illustration of Faster Transitions of Later Stages in an Inverter Chain

Chapter 3: Individual MOS Transistor Experiments

This chapter focuses on the simulations and experiments used for characterization of individual MOS transistors. These tests are important in verifying the theory behind the radiation effects on circuit characteristics since individual components are the root of all circuitry. Transistor current-voltage (I-V) characteristics are simulated and measured for various sized devices; the drain current is taken twice, once versus gate voltage and the other against drain voltage at various gate biases. Device characteristics that are affected by radiation, such as the threshold voltage, sub-threshold swing and leakage current parameters described in the previous chapter, can then be extracted from these I-V curves, and the techniques used to do so will be discussed as well. Many of the transistors tested were designed and simulated using the Cadence software package and the IBM 8RF process design kit (PDK), which consists of the 0.13μm CMOS technology. Other devices were also tested, but not simulated, as they were commercial-off-the-shelf (COTS) components and simulation models were not readily available.

3.1 Experimental Procedures

An explanation of the individual MOS transistor experiments, both simulation and testing, will begin this section. The experimental setups will be displayed and followed by descriptions of the procedures and measurements used to obtain the

required information. The results of these procedures will be held and presented later in the two sections to follow.

3.1.1 Simulation Setup

The current-voltage characteristics required are relatively simple in nature, but are extremely useful for extracting numerous device parameters such as those affected by irradiation. Figure 21 below shows the Cadence schematic setup of a few of the MOS transistor sizes tested. Note that each transistor could be run using separate simulations, but the transistors are all run together since the setups are identical. As seen from the figure below, the voltage rails for these transistors are 1.5V for V_{DD} and 0V for ground [38], where the source and body of the n-MOS and p-MOS transistors are connected to ground and V_{DD}, respectively. The transistor models used are BSIM4v4 models for the Spectre simulator, which are provided in the IBM 8RF, CMRF8SF PDK.

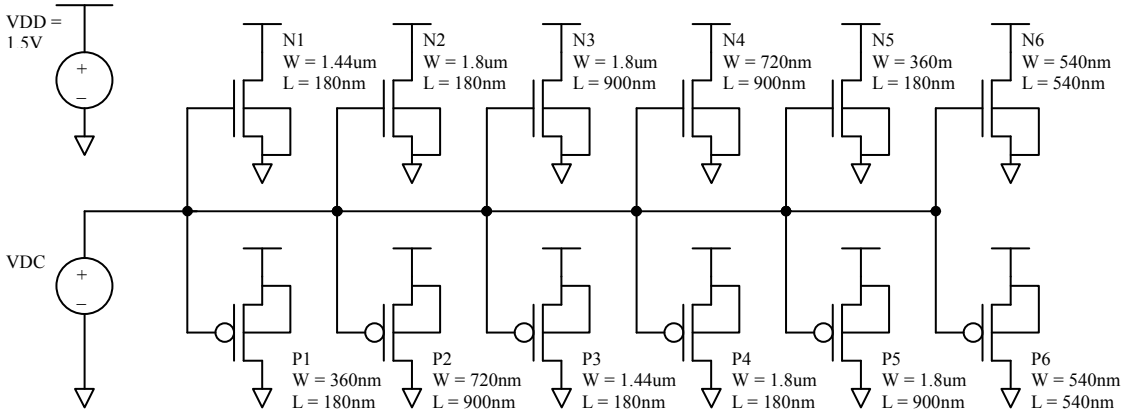
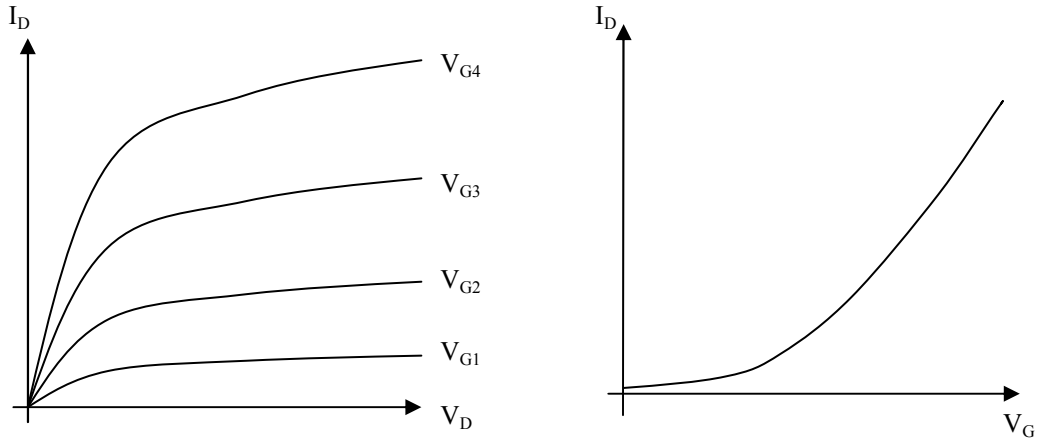


Figure 21: Cadence Setup for Individual Transistor Simulations

Two sets of sweeps are completed for this configuration to obtain the current-voltage relationships. Drain voltage is first swept from 0V to 1.5V, or ground to V_{DD}, in 5mV increments for various gate biases. The gate voltages increase from 0V to 1.5V as well, but in larger, 300mV increments, and remain constant while the drain voltage is swept. By monitoring the current flowing into the drain node, this simulation results in the characteristic "family of curves" for the individual transistors displaying drain current, I_D, versus drain voltage, V_D; a general example of which is shown below in Figure 22(a) where $V_{G1} < V_{G2} < V_{G3} < V_{G4}$. The second, and more significant, simulation sweeps the gate voltage from 0V to 1.5V in 5mV increments where the drain voltage is now fixed to V_{DD} or ground for the n-MOS and p-MOS transistors, respectively. Similar to the drain sweep, monitoring the current into the drain results in the drain current versus gate voltage plot shown in Figure 22(b).



(a) **(b)**

Figure 22: Examples of the Required I-V Relationships

To observe the effects of radiation exposure on current-voltage characteristics, the transistor models were altered to represent the induced changes. More specifically, the models contain an interface state capacitance term, C_{it} [38]. This was

the parameter of interest and was adjusted to model irradiation because, as was described in detail in chapter 2, radiation exposure results in an increase of the interface states, and consequently in the associated capacitance. Therefore, the two sweeps, of the drain and gate voltages, were run for zero C_{it} and values ranging from 10^{-4} to 10^{-2} where four points were taken per decade of C_{it}. The varying results for each interface state capacitance can then be used to extract the radiation induced modifications in the device parameters.

3.1.2 Testing Setup

Based on the simulated transistor sizes, an integrated circuit (IC) chip containing these same sized devices was designed and fabricated using the same IBM 8RF 0.13µm technology. The layout followed and successfully passed Cadence Assura design rule checks (DRC) of the revised CMRF8SF rules file dated 07/19/2006; these rules are included in the design guidelines [39]. The width-to-length (W/L) ratios simulated above were not the only devices included on this IC, as a large array of sizes were fabricated as well. In total, the chip contained 42 transistors of various W/L ratios; 21 n-MOS and 21 p-MOS devices on the same chip. For both sets, the widths included 360nm, 540nm, 720nm, 900nm, 1.44µm, 1.62µm, and 1.8µm in size, while the lengths were 180nm, 540nm, and 900nm. Figure 23 below shows the large scale view of the fabricated chip indicating the sizes corresponding with each device, where the widths and lengths are listed down the left side and across the top of the figure, respectively. Each device has four associated bond pads, one for each terminal of the MOSFET, which are the numerous square-

shaped figures in the layout below; the lone bond pad on the left of the figure is the CHIPEDGE ground.

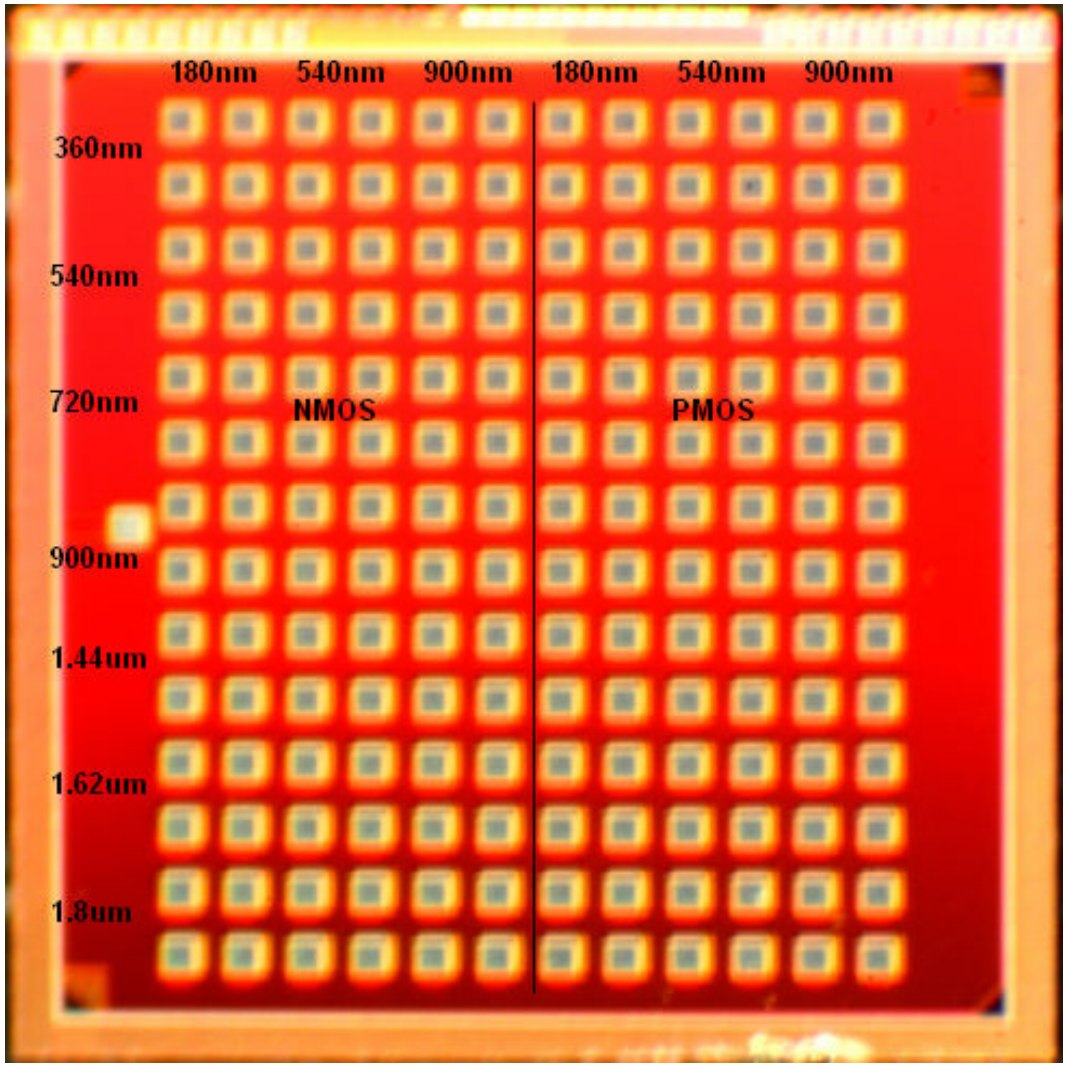


Figure 23: Layout of Various Sized Transistor Arrays

The layout above portrays the physical bare die chip that is fabricated and returned, which could then be tested using a probe station to contact each of the bond pads corresponding to the four terminals of a given MOSFET. Another way, not requiring a complex probe station and used for this research, is to package the bare die in a dual in-line package (DIP) via gold wire bonding. DIP packages are limited to the number of pins and since the layout contains 169 total pads, only six individual

transistors can be bonded per package. This requires 24 pins for the devices and one pin for the chip ground, so a 40 pin DIP package was chosen; the reason for unused leads is a result of the wire bonds not overlapping one another to avoid short circuits and undesired problems. Furthermore, all transistors bonded on a single package were of the same type, meaning either all n-MOS or p-MOS. The following W/L ratios per chip were chosen for wire bonding: 4/5, 3/3, 2/1, 8/1, 10/5, and 10/1.

Once the packaged devices were complete, a prototype printed circuit board (PCB) was constructed for testing the different chips; a picture of the board can be seen in Figure 24 below. Zero insertion force (ZIF) sockets were used to connect the packaged chips to the rest of the board, which was then connected to the testing equipment; the test equipment will be further discussed below. Both one n-MOS and one p-MOS chip can be placed on the testing board at a given time, which is the reason for the two ZIF sockets. Each used pin of the packaged devices is connected to a standalone lead, where the gates, sources, and bodies of each chip are shorted together and the drains are left as separate, individual connections. Again, the reason for doing this is because the sweeps are the same for all transistors, and the drain is the most critical node for measuring the current through each individual component. The fabricated transistor arrays did not incorporate electrostatic discharge (ESD) protection on the chip, which can potentially lead to malfunctions in device performance. Therefore, ESD protection using diodes was also included on the board to help alleviate the possibility of device breakdown; for voltages used with this testing, the worse-case reverse biasing leakage current associated with a single diode was about 2nA. Finally, since the required testing was at the DC level, wire wrapping

was used to connect the ESD diodes, ZIF sockets and connecting leads to one another.

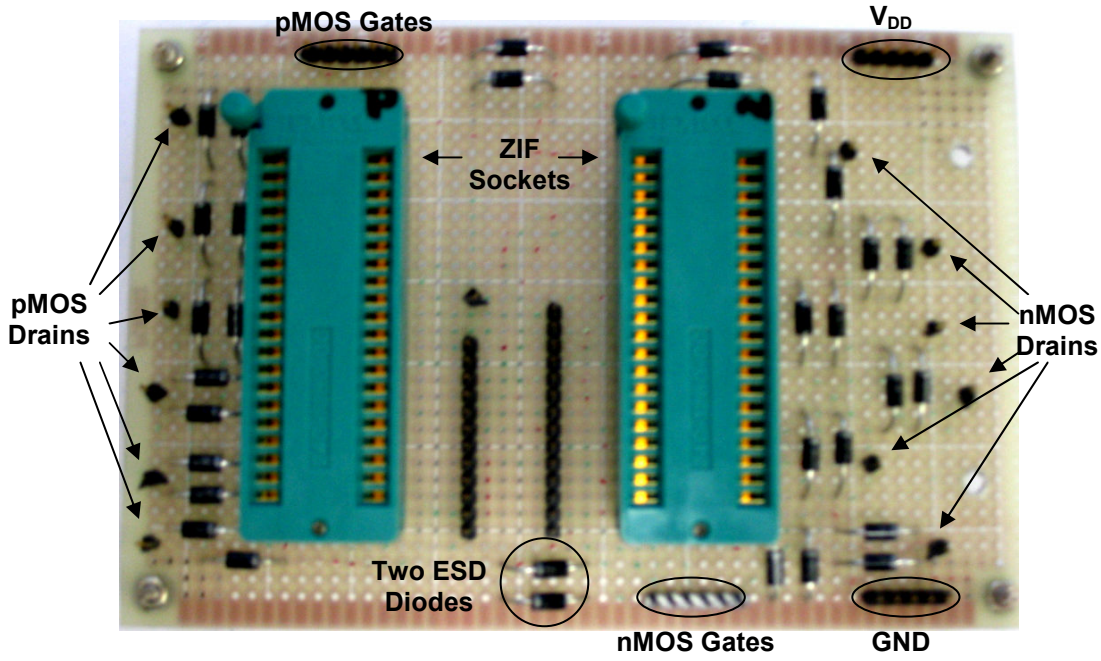


Figure 24: Prototype Testing PC Board Including ESD Protection

As was briefly mentioned above, this testing board was primarily needed to connect with the testing equipment. Excluding this test board, the equipment used was an HP4156B Semiconductor Parameter Analyzer and an accompanying HP16058A Personality Box; see Figure 25 below for a picture of the setup. Note in the figure that the parameter analyzer pictured is an HP4145B, rather than HP4156B, but the setup is identical for either version; the HP4145B is an older version. Four triaxial cables were used to attach the four SMU outputs of the parameter analyzer to the personality box where individual probe clips then connected to the leads of the testing board. The SMU outputs of the parameter analyzer are capable of sourcing voltage or current while also measuring the voltage or current at the same node, and so, one SMU corresponded to each terminal of a given transistor. In other words, two

SMU outputs supplied the rail voltages, V_{DD} and ground, another SMU sourced the gate voltage, and the final SMU supplied the drain voltage while monitoring the drain current. In this configuration, the two required test sweeps were conducted and the data acquired was saved to a floppy disk and transferred to a computer for further analysis.

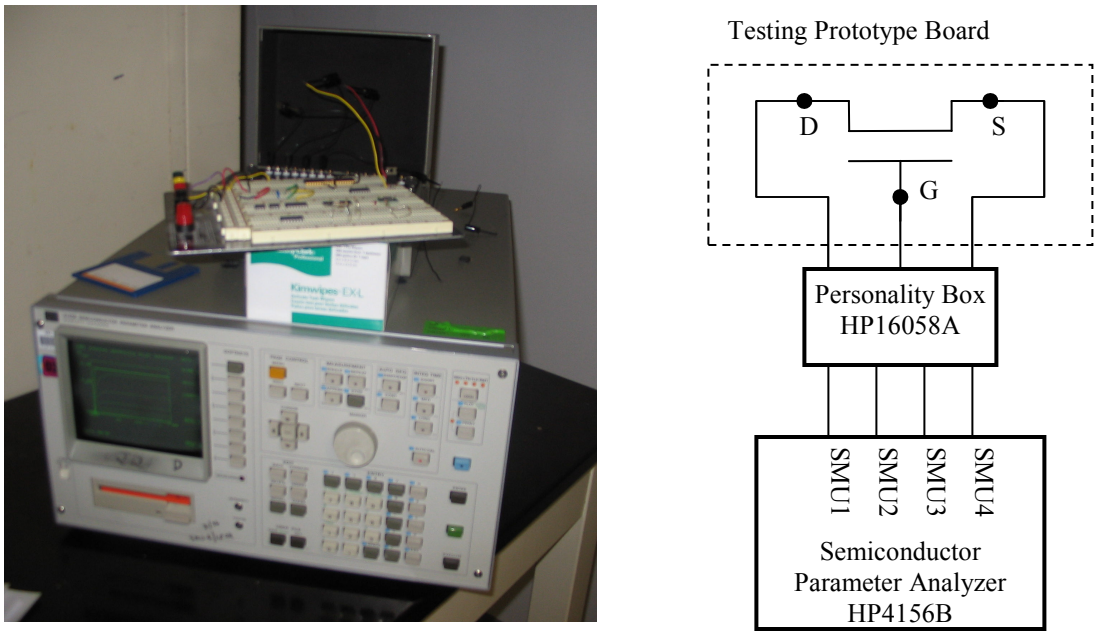


Figure 25: Testing Equipment Setup with Prototype Testing Board

The packaged devices were subjected to various levels of radiation exposure and then tested using both voltage sweeps for comparison against one another, which allows for observation of the effects of radiation-induced damage. To eliminate the possibility of irradiation damage on the testing board, a separate prototype PC board was constructed to connect the devices during exposure; see Figure 26 below. For this board, only two output connections are provided, one each for V_{DD} and ground, and the reason for this was to supply a bias to the devices during irradiation [2, 11, 49]. Specifically, the source and drain were connected together to either ground or

V_{DD} for the n-MOS and p-MOS devices, respectively, where the gate biasing was V_{DD} for n-MOS and ground for p-MOS transistors; these biasing arrangements represent maximum, worse-case conditions [49]. Again, two ZIF sockets, one each for a p-MOS and n-MOS chip, and wire wrapping were employed to connect all pins to the appropriate supply line.

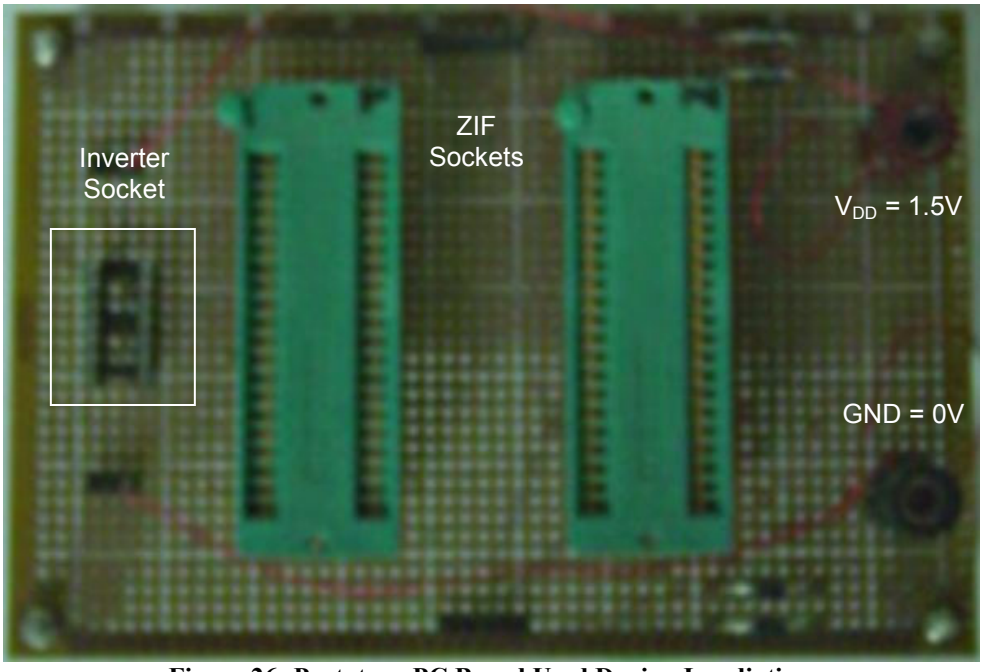


Figure 26: Prototype PC Board Used During Irradiations

Together with the transistor array chips, two COTS inverter chips were irradiated and tested using similar procedures; see Figure 27 below for a schematic representation of the circuits [40, 41]. These chips, MC14007UB from ON Semiconductor and CD4007UBE from Texas Instruments, are 14 pin DIP packages containing three p-MOS and three n-MOS transistors capable of being connected into inverter configurations. The main difference between the COTS and fabricated devices is the supply voltages used for the inverter chips are 5V V_{DD} rather than 1.5V, as for the 130nm devices. Notice in the irradiation board above that there is a third

socket on the left side of the board, which houses and supplies bias to the inverter chips during irradiations. Since there are only two supply connections to the irradiation board, the inverter chips are biased at the same 1.5V condition, not the 5V bias corresponding to the V_{DD} used for these chips. Furthermore, the individual n-MOS and p-MOS transistors are not all biased the same because the gates and drains of some n-MOS and p-MOS are tied together for the inverter representation. Wherever possible, a biasing technique similar to that used for the fabricated devices is employed for the inverter chips; pin 12, which is connected to the drain of both an n-MOS and p-MOS transistor, is the lone exception and is grounded for each chip. For some variety, gate pins 3 and 10 are biased at 1.5V whereas gate pin 6 is biased at ground. Between irradiations, these chips are taken out of the socket and tested using simple breadboard connections with the parameter analyzer and personality box described above. Finally, note that the transistor characteristics, such as width-to-length ratio, oxide thickness and feature size, are considered company proprietary information [48], resulting in the inability to run simulations on these devices.

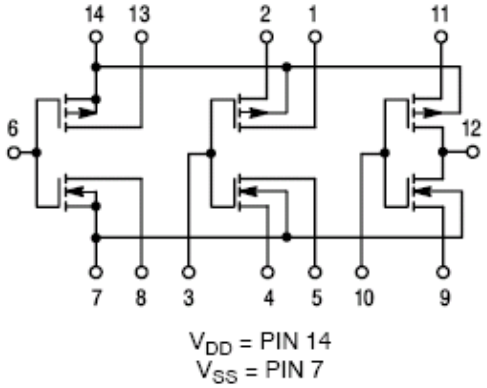
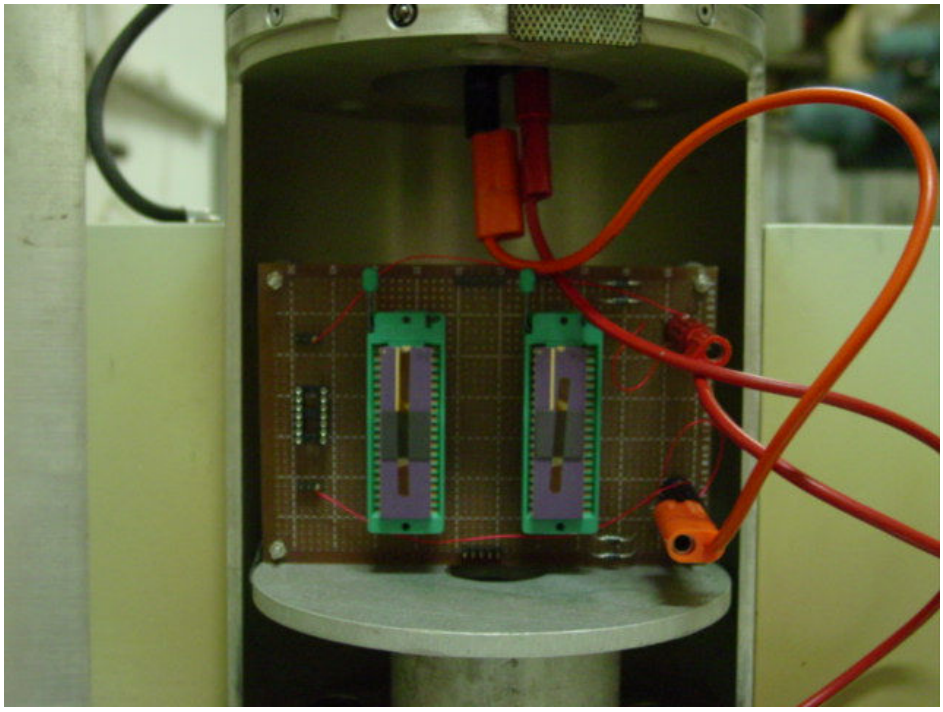


Figure 27: Schematic Representation of Inverter Chips, MC14007UB and CD4007UBE [40, 41]

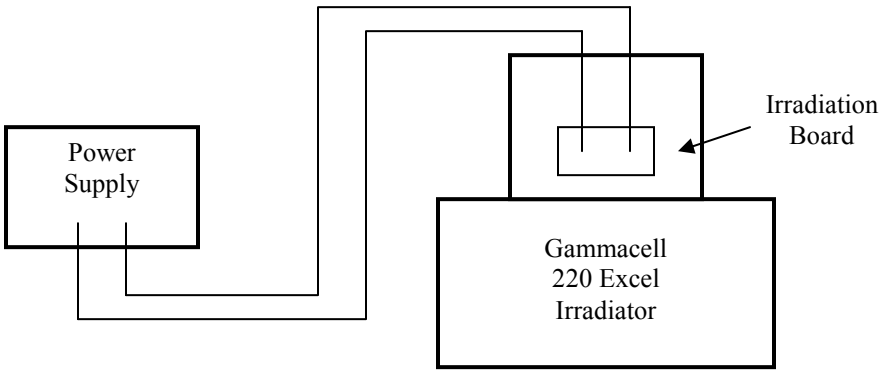
The irradiation board was then used in conjunction with the Gammacell 220 Excel facility at the Breazeale Nuclear Reactor, of Pennsylvania State University's (PSU) Radiation Science and Engineering Center (RSEC), to expose the devices to gamma radiation; this was the source type chosen for this research. MDS Nordion, who's Dosimetry Laboratory is recognized under NIST's National Voluntary Laboratory Accreditation Program (NVLAP), manufactured the Gammacell 220 irradiator, and provided a certificate of measurement for the facility [42]. This irradiator allowed electrical connections to components inside the chamber, which permitted the use of a power supply to generate the necessary 1.5V biasing of the devices during exposures. Figure 28(a) below shows the irradiation board, with chips, connected inside the Gammacell chamber where the two cables seen on the right side of the picture are run through the chamber to the power supply; a general schematic of the setup is also provided in Figure 28(b).

The total dose levels used for this work included 0.1MRad, 0.25MRad, 0.5MRad, 0.75MRad and 1MRad to obtain a relatively large range of radiation exposure. The measured dose rate, obtained using the Fricke Dosimetry System, was on the order of 750 – 1250 KRad/hour [42]. It was desirable to have such a high dose rate because the interface states generated during irradiation can undergo an annealing process [11], which was to be avoided. The measured total dose and dose rate values were made in air, where the corresponding values in silicon are slightly lower; multiply the values in air by 0.899. However, since the chips are relatively small in comparison with the chamber, the amount of silicon is small and the best dose rate and total dose values to use are those in air [42]. The overall uncertainty in

the absorbed dose rate is about ± 2.4% at a confidence level of 95% [42]. Thus, the board and devices were positioned in the optimal location within the chamber to receive maximum exposure. As an interesting side note, Appendix A shows a comparison of the testing board, which was not irradiated, and the irradiation board and how the irradiations drastically darkened the color of the prototype boards.



(a)



(b)

Figure 28: (a)Close-Up of Irradiation Board Inside Gammacell 220 Chamber and (b) General Illustration of the Irradiator Setup

Finally, to acquire the necessary data, resulting from the two current monitoring voltage sweeps previously described, the devices were exposed to each irradiation level, and then removed to be tested using the parameter analyzer and personality box setup [11]. For instance, the device is first exposed to 0.1MRad of radiation, removed for testing, placed back in the chamber and exposed to 0.15MRad irradiation to achieve the next level of 0.25MRad. This is the process used to accomplish all of the irradiation levels in order to eliminate the possibility of fabrication variations between chips that would result in comparison issues during later data analysis. The test data and associating extracted parameters are presented and discussed in section 3.3 below, following an explanation of the methods used to extract the characteristics of interest, or the threshold voltage, sub-threshold swing, and leakage current, and a presentation of the simulated data in section 3.2.

3.1.3 Measurement Techniques of Device Parameters

This subsection is intended to provide brief explanations of how the leakage current, threshold voltage, and sub-threshold swing device parameters were extracted from the acquired current-voltage relationships. Again, the leakage current is considered the current flowing through the device during zero bias on the gate terminal. Obtaining this value then requires a trivial method where the value is simply extracted from the drain current versus gate voltage (I_D-V_G) plot at $V_G = 0V$. The average leakage could also be obtained via a relatively more complex technique of integrating the gate-voltage-dependent current through the device over the region from zero gate bias to the voltage corresponding to the start of the sub-threshold region, which is $1\varphi_b$, or about $0.5V_{TH}$. Similarly, to calculate the average sub-

threshold leakage current, integrate the current through the transistor over the voltage range from $0.5V_{TH}$ to $1V_{TH}$, which is the approximate sub-threshold region previously defined in section 2.4.1. It is clear that the threshold voltage needs to be computed before these average current calculations can be accomplished since it establishes the limits of integration over the two regions of interest.

Several techniques exist to calculate the threshold voltage of a given component since it is one of the most crucial parameters associated with a MOSFET transistor. These techniques all rely on certain regions of device operation such as the sub-threshold, linear and saturation regions [43]. Furthermore, while these different methods vary in complexity, they can all be derived from the drain current versus gate voltage plots. The method that focuses on the saturation region of the transistor is the technique employed in this research. In this approach, and due to the squared dependence, a linear regression is fit about a point on the $\sqrt{I_D} - \mathrm{V_G}$ plot corresponding to the transistor being in the "on" region of operation [43]; see Figure 29 below for a graphical illustration of this technique. In other words, the gate voltage must be larger than the threshold voltage, which is to be extracted, and the saturation current is:

$$I_D = \mu C_{ox} \frac{W}{2L}\left(V_G - V_{TH}\right)^2 \qquad for\ V_G - V_{TH} < V_D \qquad \textbf{Eqn. 14}$$

where μ is the mobility, C_{ox} the oxide capacitance per unit area, and W and L are the device width and length, respectively. The linear regression is then extrapolated back to zero current, $I_D = 0$, where the corresponding gate voltage represents the threshold voltage, V_{TH}, of the transistor [43]. More specifically, this linear regression is fit

around the point where $I_D = 2\mu A(W/L)$, or $\sqrt{I_D} = \sqrt{2\mu A(W/L)}$, because it is considered to be just within the required "on" region [43]. Furthermore, series resistance and mobility degradation effects related to this relatively small "on" current are considered negligible for parameter calculations [43]. Note that this is important for irradiation work because decreasing mobility is also a damaging effect resulting from radiation exposure. Further note that the inequality in equation 14 will be satisfied at all times for the simulations and tests run on these devices because the drain current is set at 1.5V, or V_{DD}. Therefore, this will be larger than any difference between the gate voltage and threshold voltage since the gate sweep is to V_{DD} as well.

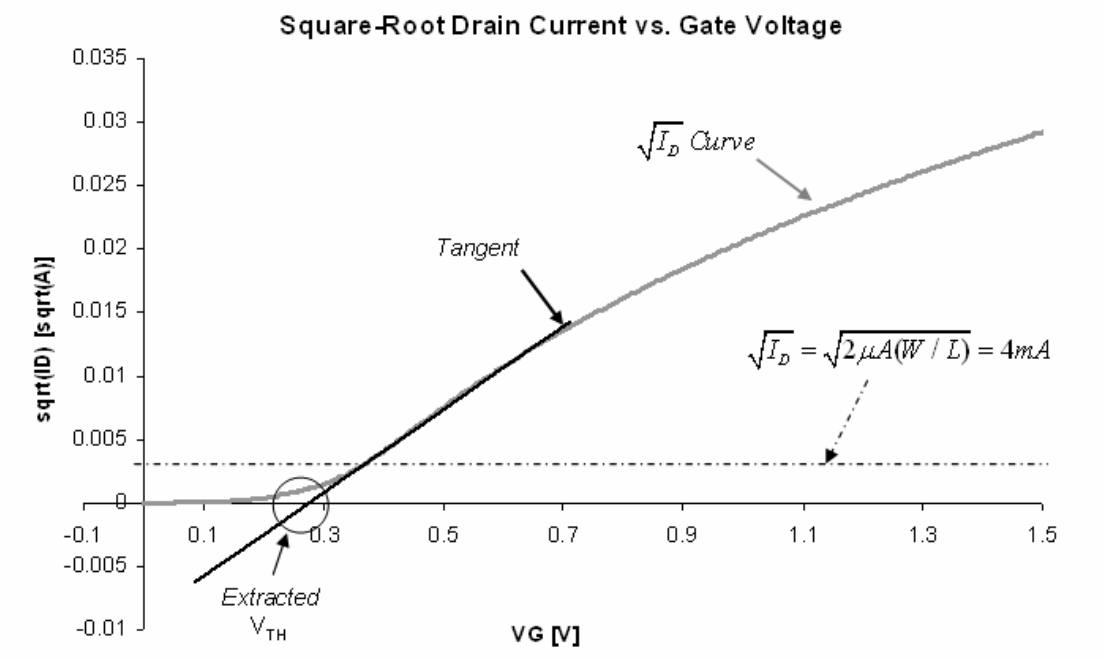


Figure 29: Graphical Illustration of the Saturation Method of Threshold Voltage Extraction

Once the threshold voltage of the device is extracted, it can then be used to find the sub-threshold swing of the transistor. Similar to that for the threshold voltage extraction, a linear regression approach is used to extract the swing; Figure 30 below

graphically illustrates this approach. However, for this parameter, the regression is fit to the $\log_{10} I_D - V_G$ curve rather than the $\sqrt{I_D} - \mathrm{V_G}$ plot. Moreover, this regression is fit about the threshold voltage, and/or over the entire sub-threshold region, where the inverse of the linear regression slope represents the sub-threshold swing of the transistor [36]; this was described in more detail in section 2.3.2 above.

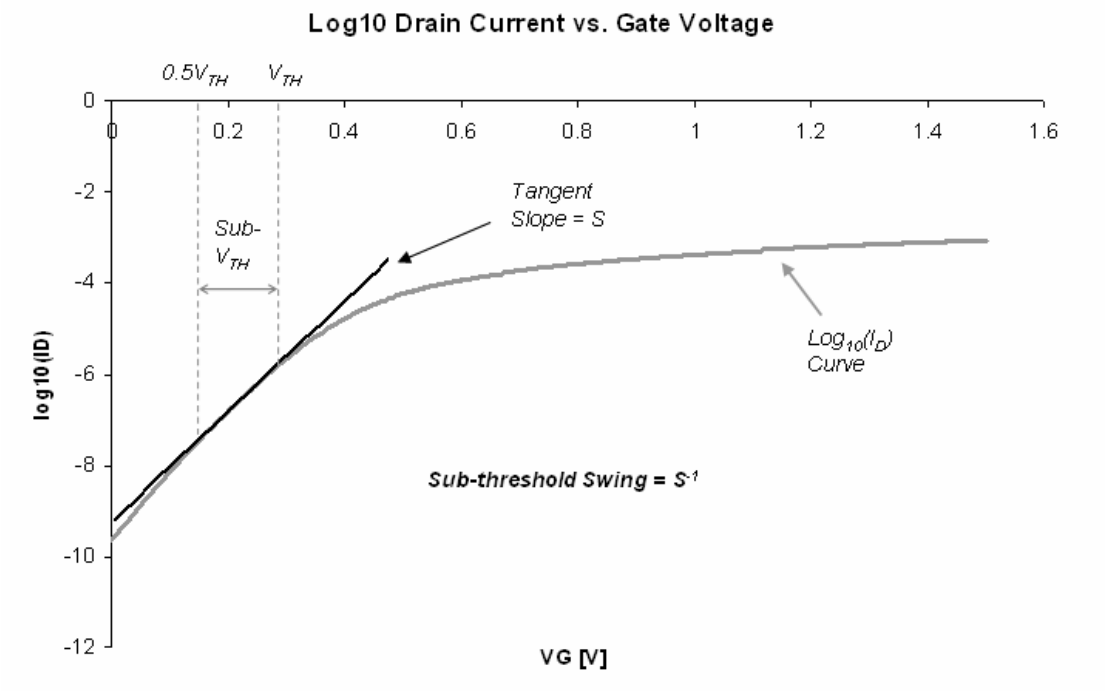


Figure 30: Graphical Illustration of Sub-threshold Swing Extraction Method

Finally, having extracted the sub-threshold swing device parameter, the resulting interface state generation can then be estimated. The theoretical equation for the sub-threshold swing, equation 8 of section 2.3.2, could be used to solve for the interface state capacitance, C_{it}, corresponding to each measured swing value. Or, the interface state density, D_{it}, could be found with respect to the pre-irradiation level via equation 2 of section 1.1.4, and then using the relationship $\frac{C_{it}}{q} = D_{it}$. Note that either

equation requires additional device characteristics such as the oxide thickness in order to carry out the calculations.

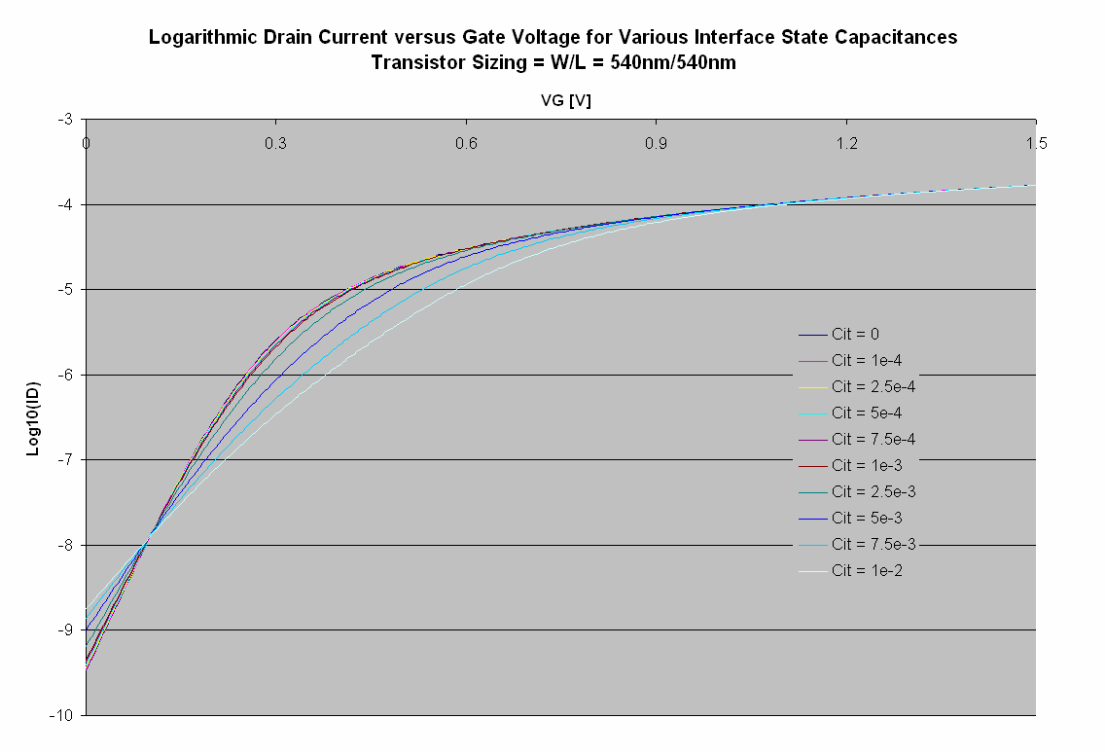
3.2 MOS Transistor Simulation Results

While the transistor array chips contain 42 total transistors, of both n-MOS and p-MOS type, only the six width-to-length ratios bonded to the DIP packages were simulated. Moreover, only those transistors whose experimental results will be presented in section 3.3 below will be provided in this section; specifically, the 8/1, 2/1 and 3/3 n-MOS sizes and 8/1, 10/1, and 10/5 p-MOS sizes are given. Also, to reiterate, simulations will not be provided for the MC14007UB and CD4007UBE COTS inverter chips since model files and/or device geometries are not readily available information [48]. The main objectives of these simulations are to observe the trends and verify the effects of radiation-induced damage on sub-threshold characteristics and the device parameters of interest. The results should also agree with similar observations presented in the open literature.

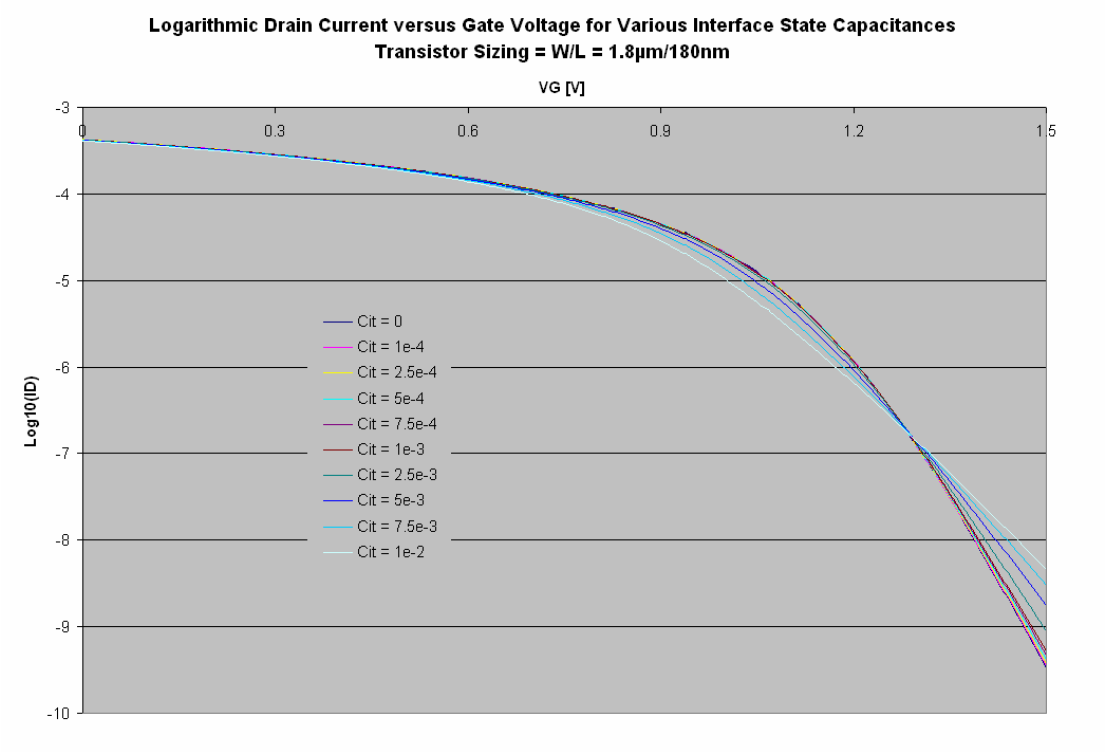
3.2.1 Sub-Threshold Swing

Two sets of n-MOS, and p-MOS, transistors were simulated and irradiated, where the following width-to-length (W/L) ratios were bonded out: 8/1, 10/1, 10/5, 4/5, 2/1, and 3/3. Furthermore, one of the sets utilized a 0.12µm scale while the other set was a 0.18µm scale; for instance, W/L = 8/1 equates to 960nm/120nm in the 0.12µm scale and 1.44µm/180nm on the 0.18µm scale. Based on these scales and transistor sizes, Figure 31(a) and (b) below display the logarithmic of the drain current versus the gate voltage of an n-MOS and p-MOS transistor for a constant

drain voltage of 1.5V and gate sweep from ground to 1.5V; the n-MOS size is W/L = 3/3 = 540nm/540nm, whereas the p-MOS size is W/L = 10/1 = 1.8µm/180nm. Similar graphs were obtained for the other sized devices, but are not reproduced here since the trends are identical where the magnitudes are the only differences. More important are the sub-threshold swing, threshold voltage, and leakage current changes, which are presented further below.



(a)

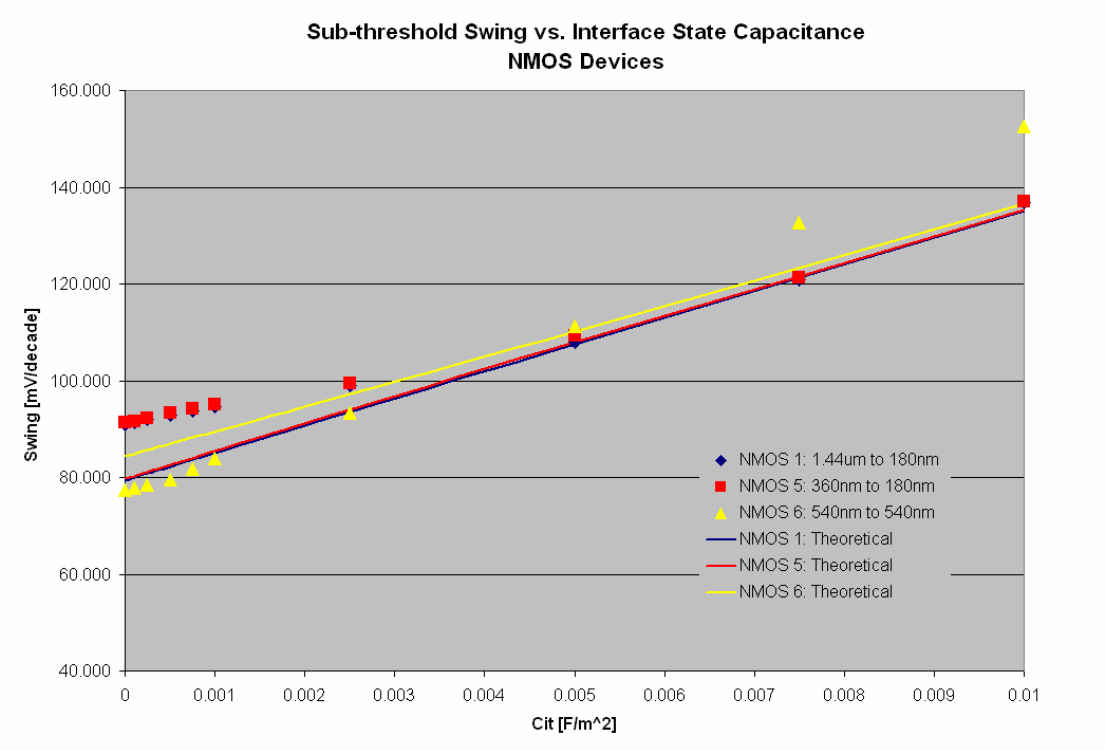


(b)

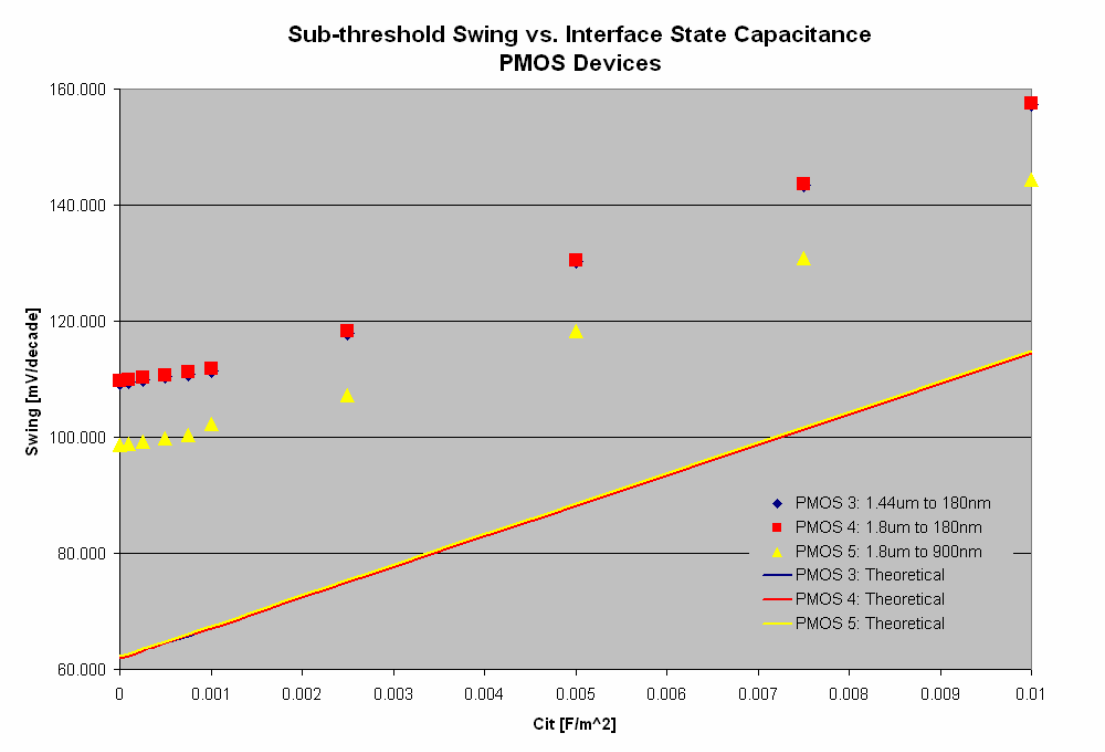
Figure 31: Log Drain Current versus Gate Voltage for (a) 540nm/540nm Sized NMOS Transistor and (b) 1.8µm/180nm Sized PMOS Transistor at Various Interface State Capacitances

The collection of plots in the above figure clearly portrays the change in sub-threshold slope, and consequently sub-threshold swing, as a function of interface state capacitance. Again, the interface state capacitance is used in simulation to model the radiation-induced damage. It is obvious that as the interface state capacitance is increased, the slope of the drain current plots decrease, which corresponds to an increase in the sub-threshold swing; swing is the inverse of the slope. Using the measurement technique described above, a direct comparison between the extracted sub-threshold swing parameters and interface state capacitance is shown in Figure 32(a) and (b) below. Furthermore, the graphs contain similar plots for the 8/1 and 2/1 sized n-MOS transistors and 10/1 and 8/1 sized p-MOS transistors, allowing for a

comparison amongst the various sized components. These increases in the sub-threshold swing, which are linear with respect to the interface capacitance, agree with the theoretical predictions and result in a loss of gate control. In most cases, the increase in the sub-threshold swing for a given device was about 55.1% from the zero to 10^{-2} interface capacitance levels; 65.82% and 44.43% average increases for n-MOS and p-MOS devices, respectively. More specifically, the average change in n-MOS swing was from 86.591mV/decade to 142.143mV/decade, and that for the p-MOS swing was from 102.974mV/decade to 153.076mV/decade; these values correspond to the beginning and end of the interface capacitance range. Consequently, an increase in the gate voltage is required to turn off a given amount of current compared to that needed prior to irradiations.



(a)



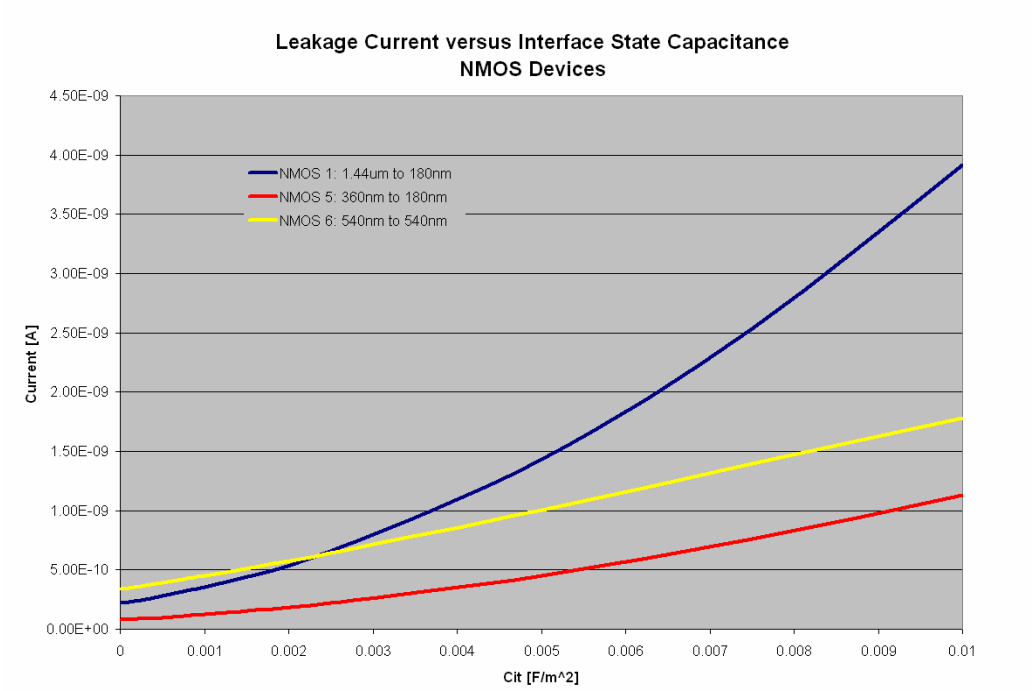
(b)

Figure 32: Sub-threshold Swing versus Interface State Capacitance for Various Sized (a) NMOS and (b) PMOS Devices

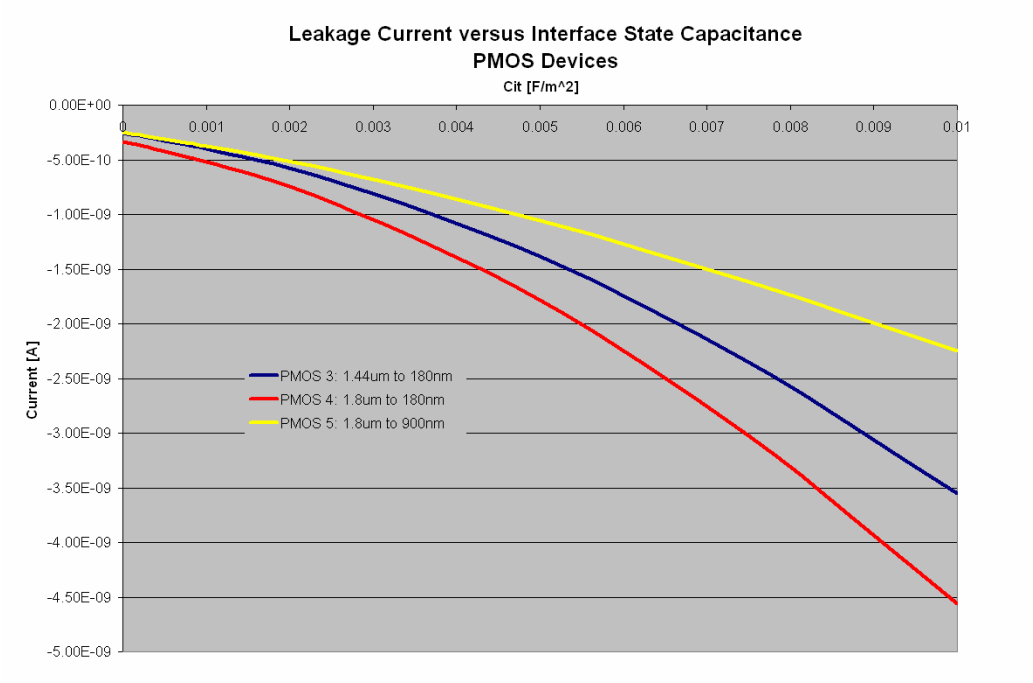
Notice that Figure 32(a) and (b) above also illustrate the comparison between the theoretical sub-threshold swing, calculated using an equation, and the simulated swing from the model files. In the figure, the symbols represent the simulated values while the linear plots represent the equation-calculated values at the same interface state capacitances. While the equation represents the n-MOS devices fairly well, the simulation based extracted parameters for p-MOS devices are slightly higher than would be calculated from the swing equation; the equation underestimates the parameter for p-MOS. However, the trend of the extracted parameters and equation calculations are in relatively good agreement, and thus can still be used to draw similar conclusions.

3.2.2 Leakage Current

Figure 31 above also portrays the effects of modeled radiation exposure on device leakage currents. Observing the current level on the left and right side of the n-MOS and p-MOS plots, respectively, shows that the leakage current is also increasing for larger interface state capacitance values. This can more easily be seen in Figure 33 below, which plots the leakage current directly as a function of interface capacitance. Similar to before, the first graph shows the n-MOS while the p-MOS are given in the second graph. The increase in leakage current is dependent upon the sub-threshold swing because for larger swing values, the corresponding sub-threshold slopes decrease, which means the current magnitudes of the higher capacitance levels cannot reach previously lower values. Quantitatively, the average leakage current at $C_{it} = 0$ was 0.2118nA and 0.2853nA for n-MOS and p-MOS devices, respectively, while that at $C_{it} = 10^{-2}$ was 2.277nA for n-MOS and 3.453nA for p-MOS. These values correspond to average ratio increases of about 12.48 and 11.96 for n-MOS and p-MOS transistors, respectively. This order of magnitude larger will translate into larger leakage power dissipation for a single transistor, and an even more significant increase in power over an entire chip and system comprised of millions of transistors.



(a)

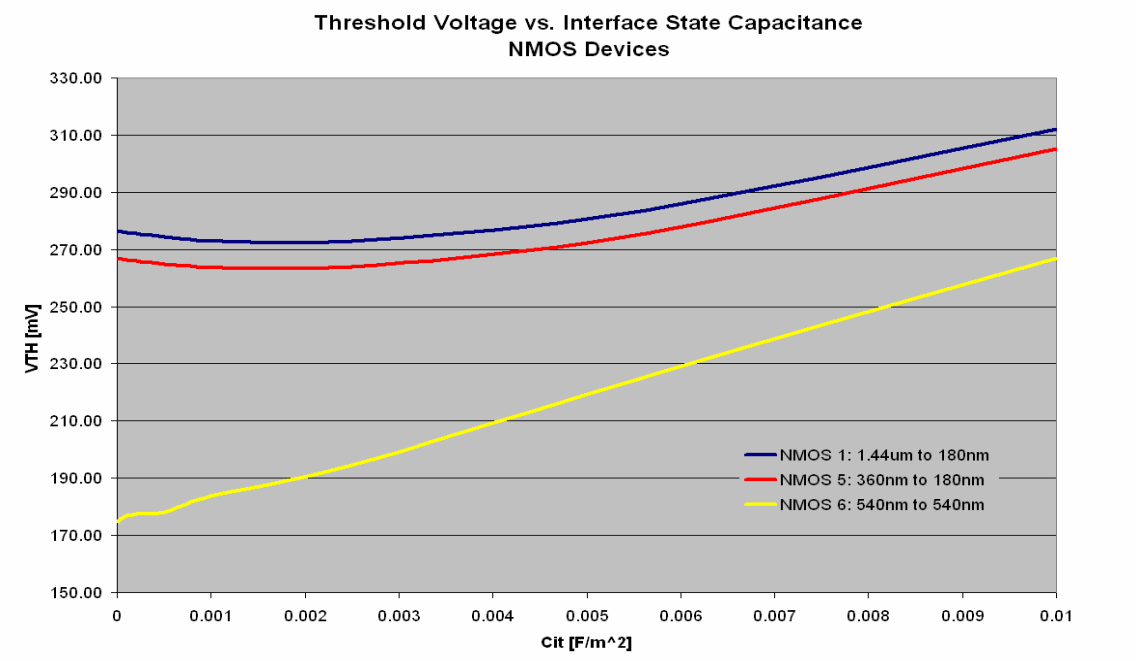


(b)

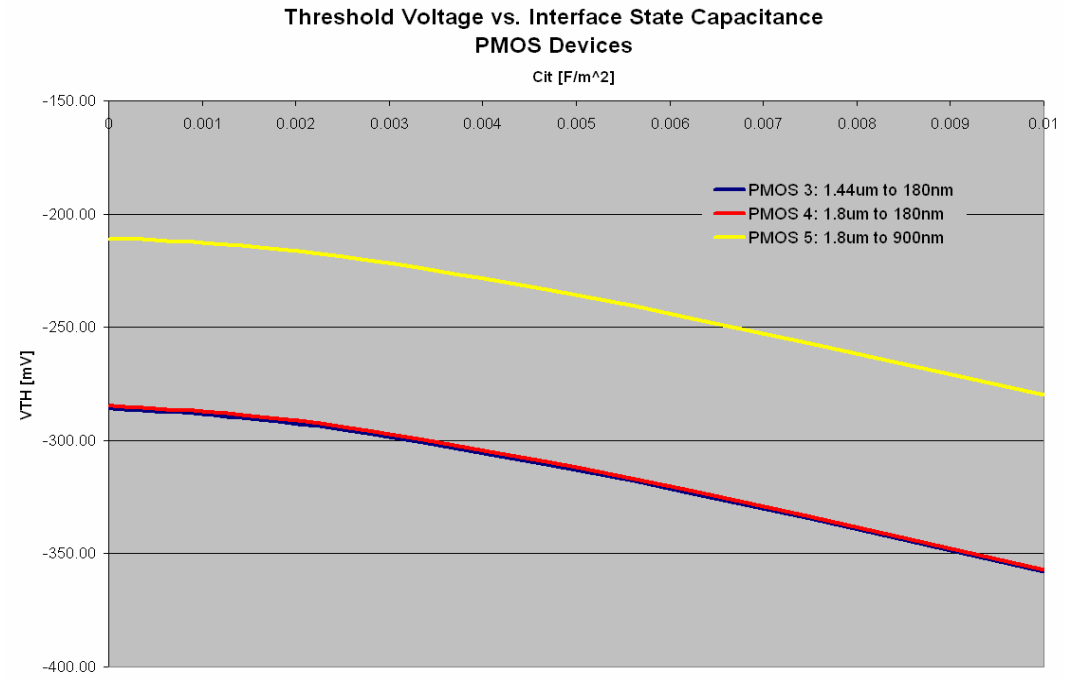
Figure 33: Leakage Current versus Interface State Capacitance for Various Sized (a) NMOS and (b) PMOS Devices

3.2.3 Threshold Voltage

The threshold voltage effects resulting from increased irradiations may not be as easily noticeable in Figure 31 as the sub-threshold swing and leakage current changes. Therefore, Figure 34(a) and (b) below presents the threshold voltage versus interface state capacitance plots for the n-MOS and p-MOS devices. It is clear that the device parameters are following a similar trend to those portrayed in Figure 4 [2] of section 1.1.3 above. More specifically, the p-MOS devices are strictly increasing whereas the n-MOS devices tend to initially decrease from the pre-irradiation level and then increase beyond the pre-irradiation level for higher levels of interface state capacitance. For the n-MOS devices, the average percentage increase in threshold voltage at the highest level with respect to the initial value was around 26.758%, compared to that of the p-MOS transistors that was about 27.776%. These percentages correspond to increases from 239.08mV to 294.67mV for n-MOS devices and from 260.53mV to 331.65mV for p-MOS devices following the 10^{-2} F/m^2 interface capacitance.



(a)



(b)

Figure 34: Threshold Voltage versus Interface State Capacitance for Various Sized (a) NMOS and (b) PMOS Transistors

Notice in both Figure 34(a) and (b) that the threshold voltages for the devices corresponding to the yellow curves are significantly different than those for the other

devices shown. The possible explanation for this may have to do with the lengths of these transistors, which are each three times larger than those associated with the other devices. The normalized square root Id vs. Vg plot for the larger devices are shifted in comparison with the plots associated with the other components, where a linear extrapolation back to zero current will lead to a smaller intercept. This seems to indicate that the larger-dimensioned devices are less susceptible to second order effects which cause variations in the threshold voltage of smaller sized components; more specifically, the increase in threshold that is observed in the figures for the smaller sized transistors. This further indicates an inverse second order effect on the threshold voltage of the device. However the measured results, which will be given in more detail in the following section, are supported by results from the IBM PDK design model files and simulations; some simulation and measured data is produced in Table 2 below for varied dimensions of an n-MOS at zero interface state capacitance and pre-irradiation levels.

SIMULATION DATA

Width [nm]	Threshold [mV]
180	273
360	304.5
540	312
720	315
900	315
1080	315
1260	315
1440	315
1620	315
1800	315

Length kept constant at 180nm

Length [nm]	Threshold [mV]
120	354
180	305
360	223.5
540	198
720	181.5
900	171

Width kept constant at 360nm

MEASURED DATA POINTS

N: W/L = 360nm/180nm

Width [nm]	Threshold Voltage [mV]
360	285

N: W/L = 1.44um/180nm

Width [nm]	Threshold Voltage [mV]
1440	310

N: W/L = 1.8um/180nm

Width [nm]	Threshold Voltage [mV]
1800	315

N: W/L = 360nm/180nm

Length [nm]	Threshold Voltage [mV]
180	285

Table 2: Threshold Voltage Comparison of Simulated and Measured Data Points Showing Inverse Second Order Effects

3.2.4 Impact on Circuit Power Characteristics

Table 3 below presents a summary of the simulated percentage increases in the three transistor parameters of interest: threshold voltage, sub-threshold swing, and leakage current.

Transistor Array Simulations	% Increase Threshold Voltage	% Increase Sub-threshold Swing	Ratio Increase Leakage Current	% Increase Sub-threshold Region
NMOS	27.776	65.824	11.964	27.776
PMOS	26.758	44.427	12.49	26.76

Table 3: Summary of Increases in Device Parameters Following Radiation Simulations

In summary, these simulation results indicate and support the claim that the increase in interface state capacitance, resulting from irradiations, will lead to increases in undesired power dissipation of CMOS circuits. The increase of the sub-threshold swing decreases the control of current flow via the gate, which assists in the increase of leakage current through the device. Due to the increase in leakage, the standby power will increase as well. Moreover, it also directly corresponds to an increase in dynamic power dissipation since the power is simply the product of voltage across a device, which typically remains constant, and current through the device. Thus an order of magnitude increase in leakage resulting at higher exposure levels equates directly to an order of magnitude increase in the associating power dissipation. Furthermore, an increase in the threshold voltage of the device translates into an increase in the sub-threshold region of the device. A larger sub-threshold region leads to a larger integration when calculating the sub-threshold power. On average, the interval of voltages corresponding to the sub-threshold region increases 26.76% for the n-MOS and 27.77% for the p-MOS components; these values are the same as those for the threshold voltage. Finally, along with the increase in sub-

threshold power, the increase of time spent in sub-threshold takes away from the possible time in "crowbar", resulting in a more significant consideration of the total power dissipated corresponding to the sub-threshold region of operation.

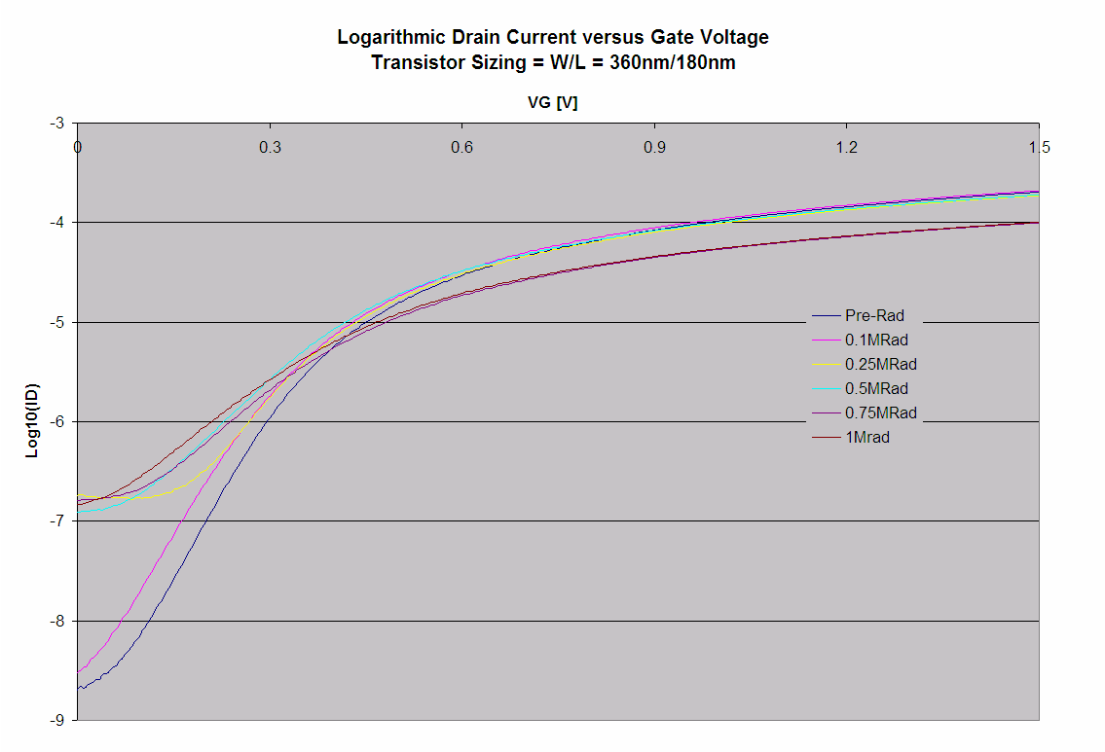
3.3 MOS Transistor Test Results

Following the simulation of the transistor array chips, the fabricated structures and COTS inverter chips were experimentally tested according to the procedure described in section 3.1 above. During the testing of the transistor arrays, several of the devices did not remain in working condition throughout the entire experimental procedure; this was to be expected considering radiation exposure is a destructive process. Furthermore, all of the transistors that survived the entire range of radiation exposures were from the 0.18μm scaled array. Specifically, full data was acquired for those sized devices corresponding to the simulation results shown in the previous section, which are repeated here: 8/1, 2/1 and 3/3 n-MOS W/L ratios and 8/1, 10/1, and 10/5 p-MOS W/L ratios. With regards to the COTS chips, on both components the only devices to stop working were the n-MOS transistors whose gates correspond to pins 3 and 10; all of the other components continued working properly. The goal behind the following testing results was to provide physical characterization evidence and support of the simulation trends and results previously discussed. The measured extracted parameters will then be used in simulations to project the impact on power dissipation in the next chapter.

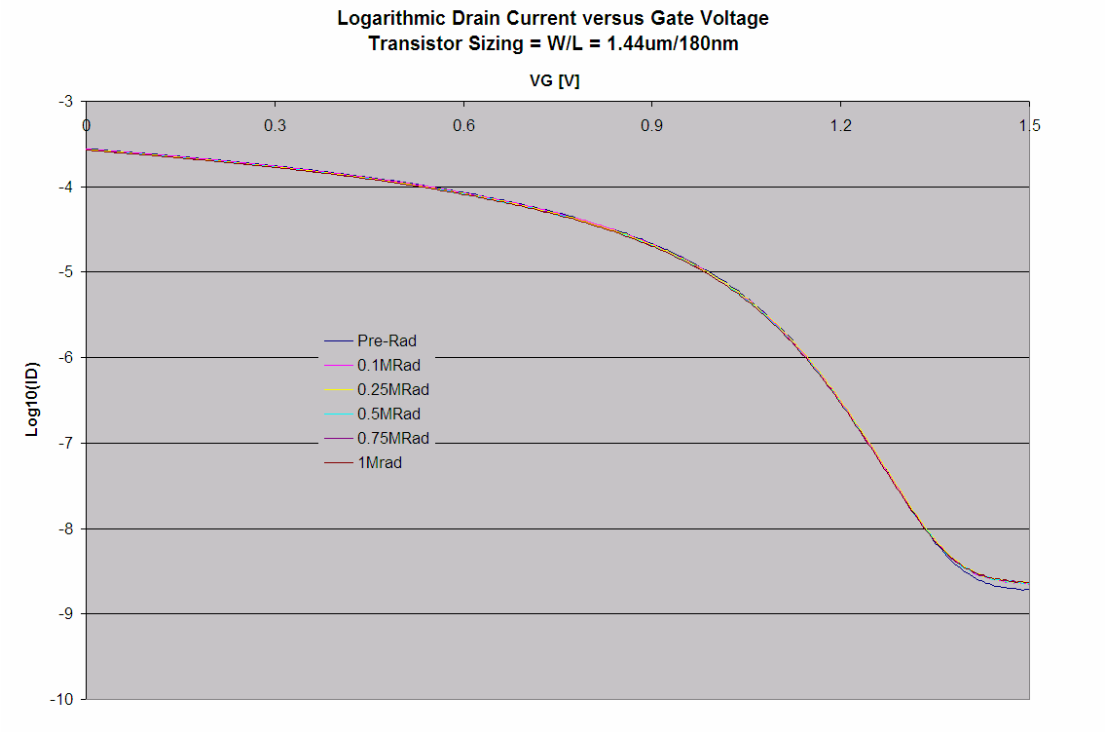
3.3.1 Fabricated 0.18μm Structures

It should be mentioned that while there may be some parasitics associated with the testing board used, the effects from these are negligible for two reasons: the testing conducted is DC testing and all of the testing was completed using the same procedure and board. Thus any testing board related effects will be included across all irradiations, and the trends are also more important than the absolute magnitudes. It is important to note that while the worse-case leakage current for a single diode is about 2nA, as previously mentioned in section 3.1.2, this should only slightly affect the current-voltage characteristics. More specifically, this will only have effects at the extremes of the voltage sweeps, where maximum reverse biasing conditions exist, because the leakage currents associated with the board at the drain pins decreases to the order of hundreds of picoAmps for the mid-range, or majority, of sweep voltages.

Similar to the simulations, changes that occur from increased radiation exposure can be seen in the logarithmic drain current plot. Figure 35(a) and (b) depict such measured plots for a W/L = 2/1 = 360nm/180nm n-MOS fabricated device, and W/L = 8/1 = 1.44μm/180nm p-MOS fabricated device. Again, the levels of radiation exposure used were pre-irradiation, 0.1MRad, 0.25MRad, 0.5MRad, 0.75MRad and 1MRad gamma irradiations. Notice that the plots of the p-MOS transistor are less fluctuating at different radiation levels compared to the n-MOS plots. In other words, the acquired data indicates that perhaps radiation has a greater effect on n-MOS rather than p-MOS devices. Notice also in the later graphs that data is only provided up to the 0.75MRad level for the 10/1 sized p-MOS structure because the device stopped properly functioning after this exposure.



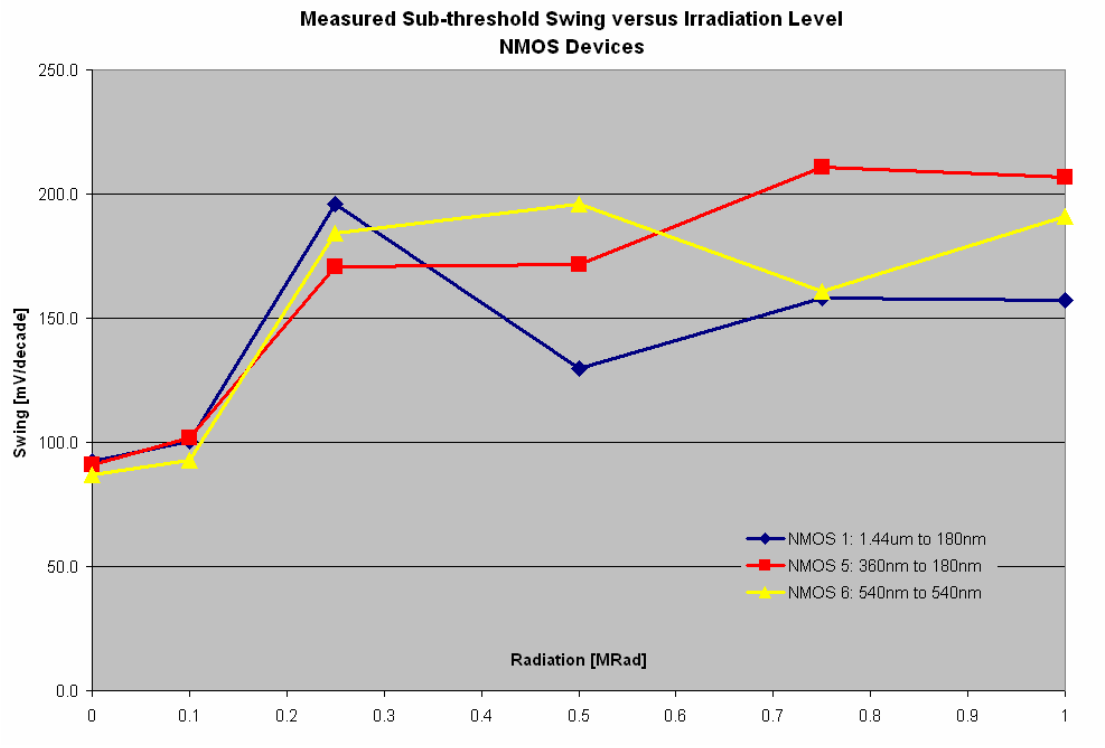
(a)



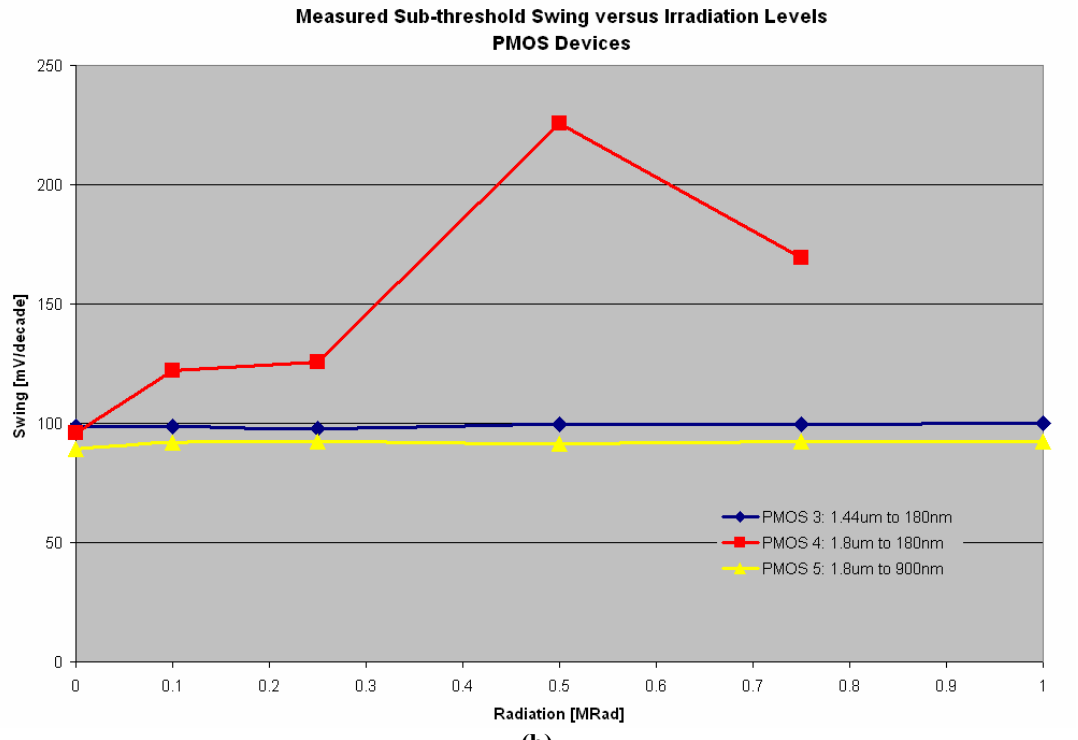
(b)

Figure 35: Measured Logarithmic Drain Current versus Gate Voltage after Various Irradiation Levels for Fabricated (a) 360nm/180nm Sized NMOS and (b) 1.44um/180nm PMOS Devices

It is evident from the n-MOS plots above that similar observations as those found through simulation are occurring to the sub-threshold swing; the p-MOS plots do not as easily portray this result. In general, as the radiation level increases, the sub-threshold swing also becomes larger because the slope of the logarithmic plots decreases. This is directly shown in Figure 36(a) and (b), which graphs the sub-threshold swing as a function of radiation levels for the n-MOS and p-MOS transistors that continued to function properly across all irradiations. These plots further suggest that the n-MOS devices were more susceptible to the irradiation than the p-MOS devices because the swing was relatively constant for the majority of the p-type structures, while all three of the n-type devices increased in sub-threshold swing. Moreover, the maximum percent increase of the n-MOS transistors was about 123.03% on average, compared to that of the p-MOS transistors of about 46.85%, which was slightly skewed by the lone device that showed significant changes. These percentages correspond to average increases from 90.119 to 185.098mV/decade and 94.595 to 120.485mV/decade for the n-MOS and p-MOS transistors, respectively, following the 1MRad total dose exposure; again, the p-MOS measurement is slightly skewed.



(a)

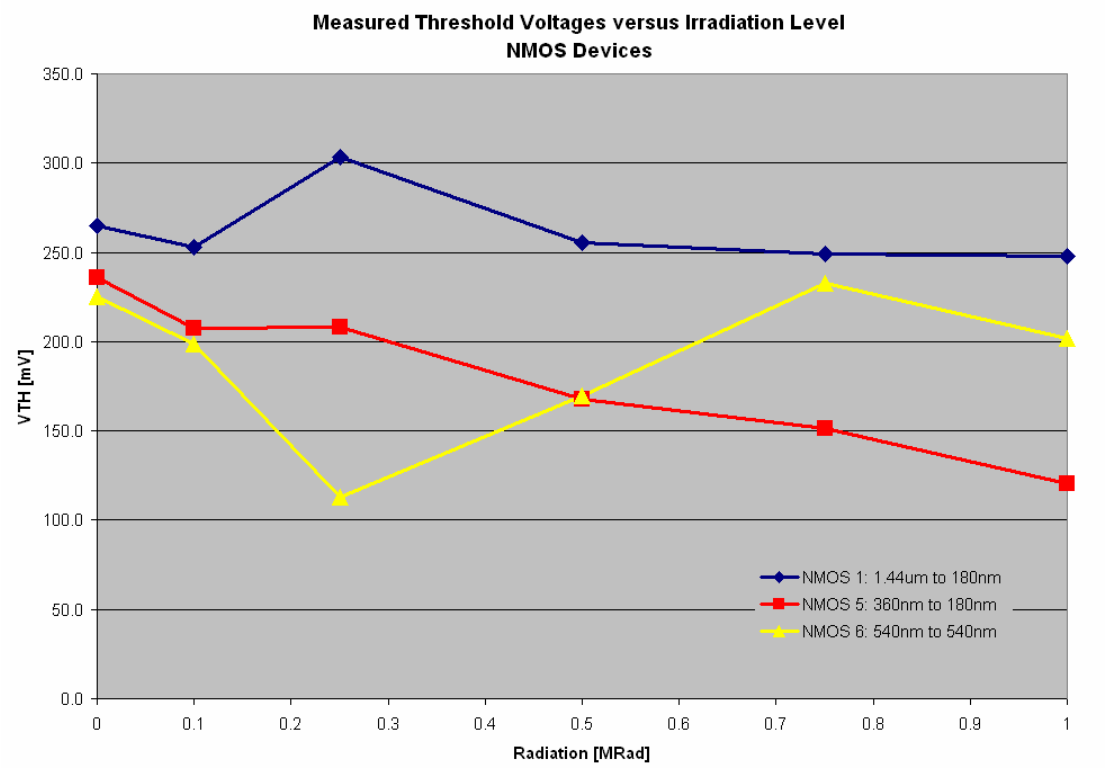


(b)

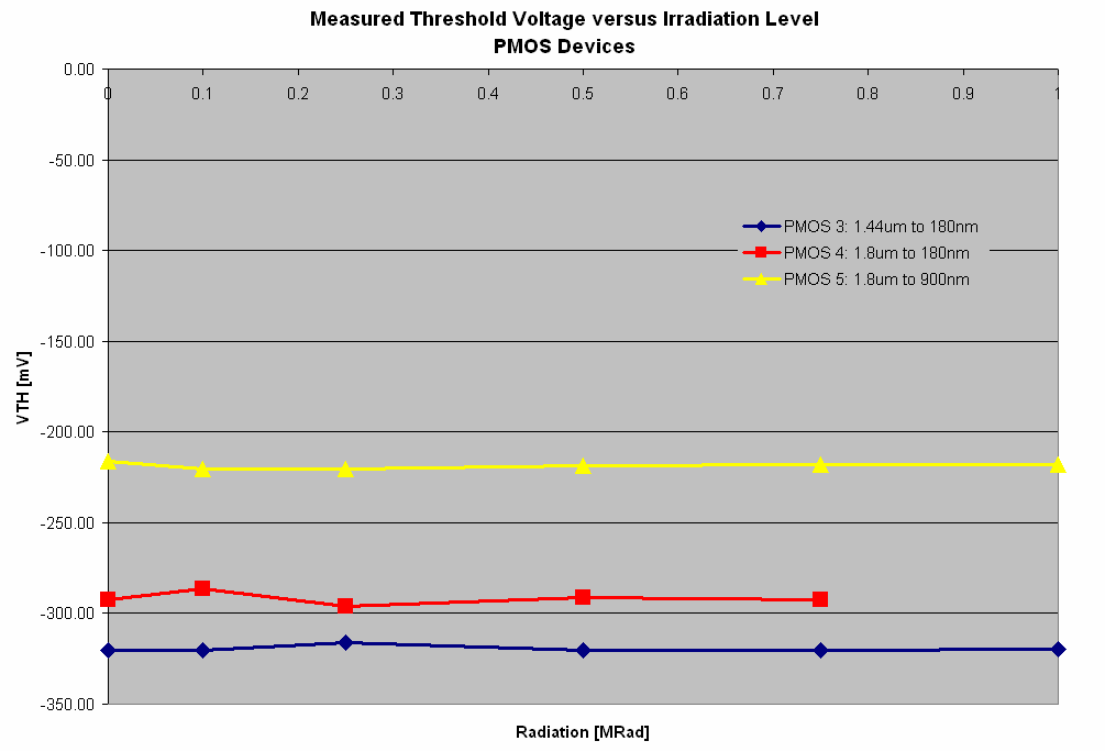
Figure 36: Measured Sub-threshold Swing versus Irradiation Level for Fabricated 0.18µm (a) NMOS and (b) PMOS Devices

Similarly, the threshold voltage and leakage current plotted against the irradiation levels seem to indicate that the p-MOS transistors were less affected by radiation than the n-MOS counterparts. Figure 37(a) and (b) and Figure 38(a) and (b) below present these threshold voltage and leakage current plots, respectively. It is clear that the p-MOS threshold voltages are not nearly as affected as the threshold voltage for the n-MOS devices. This can be seen quantitatively considering the average threshold voltage for the n-MOS devices started at 241.853mV, declined to 160.447mV and increased back to 190.25mV, compared with fairly small fluctuations around 276mV for the p-MOS components. The threshold voltage for the n-MOS 6 device shown in Figure 37(a) follows the reported trend for such devices by initially decreasing in magnitude to then return and surpass the initial value. However, after the 0.75MRad irradiation, the threshold voltage was lowered again; this indicates that the device may have begun breaking down.

The ultimate result is how the combination of the three altered parameters affects the power dissipation of the device and circuit it is a part of; this is the subject of the next chapter. Therefore, while the threshold voltages may not indicate typical trends, the leakage current is certainly increasing in magnitude for increased irradiation levels. For most of the devices, the leakage current is starting off on the order of nano-Amps and increasing to values on the order of hundreds of nano-Amps, two orders larger, following 1MRad total dose irradiation; on average, from 1.964nA to 161.5nA for the n-MOS, and 1.86nA to 131.8nA for the p-MOS. Similar as before, this increase in leakage directly equates to a couple orders of magnitude increase in the leakage, and total, power dissipated via these devices.

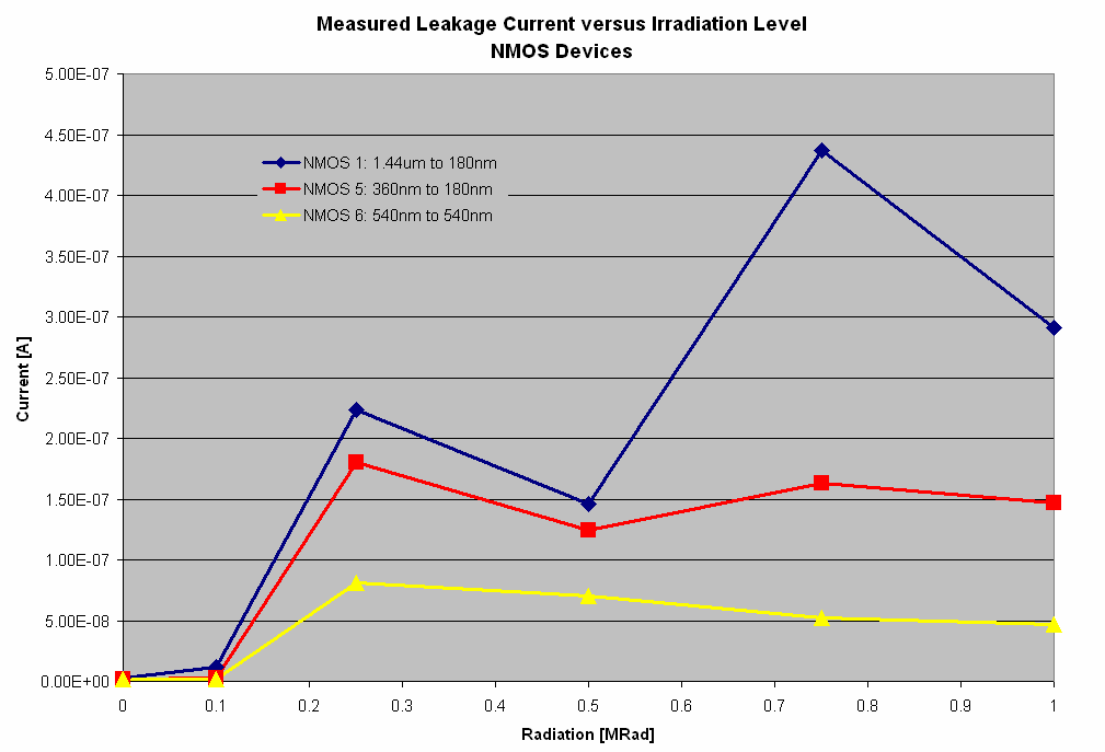


(a)

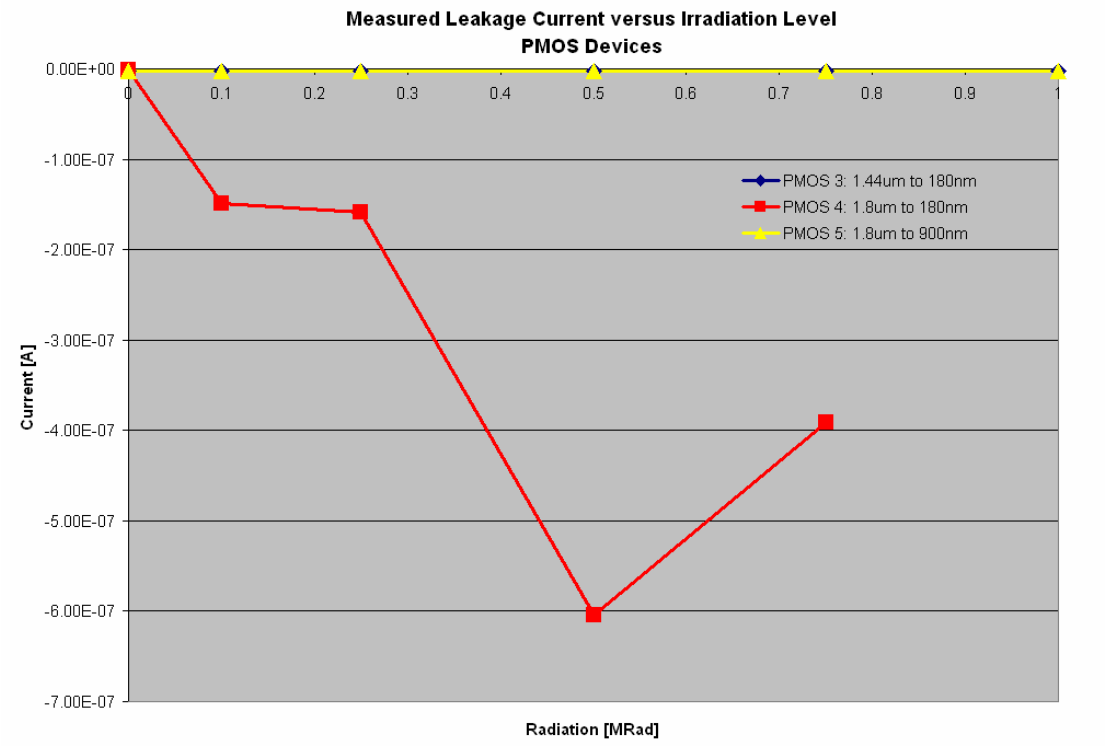


(b)

Figure 37: Measured Threshold Voltage versus Irradiation Level for Various Sized (a) NMOS and (b) PMOS Transistors



(a)



(b)

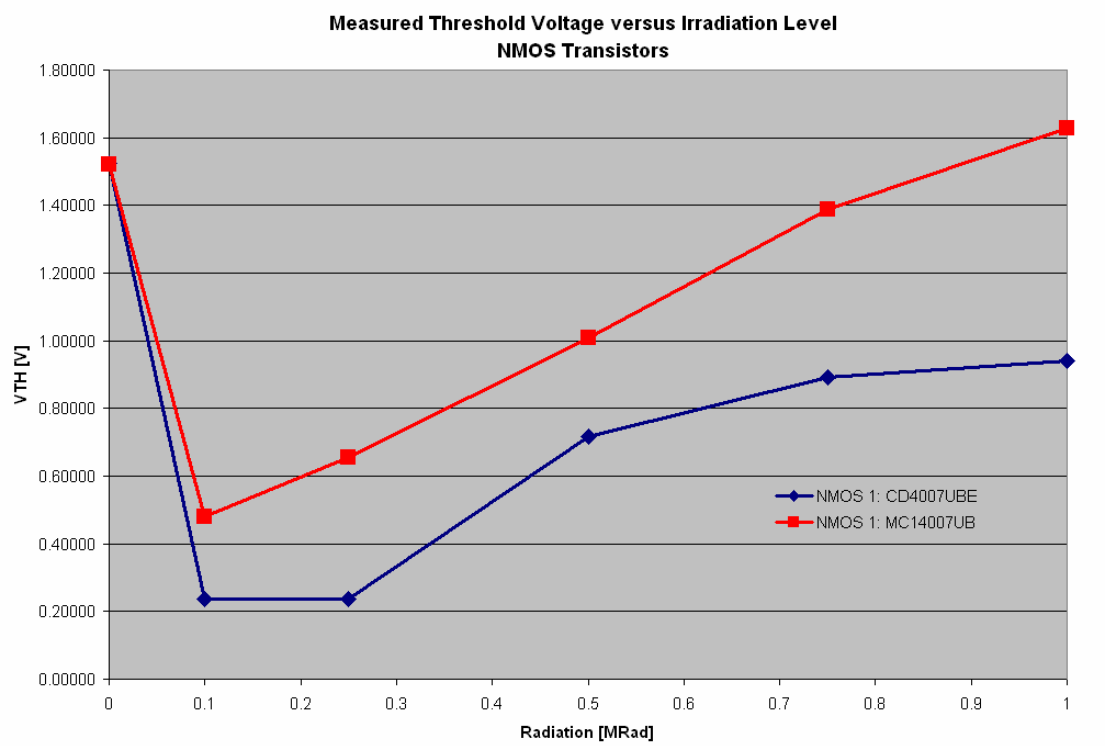
Figure 38: Measured Leakage Current versus Irradiation Level for Various Sized (a) NMOS and (b) PMOS Transistors

3.3.2 Individual Transistors of Inverter Chips

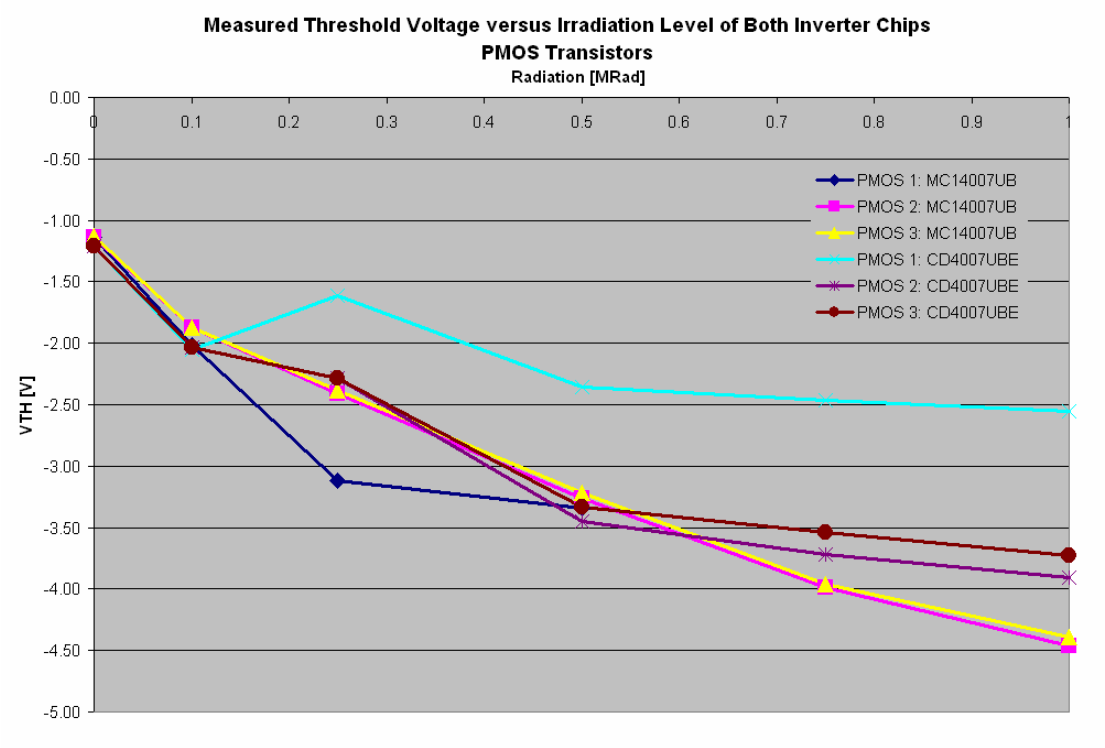
As a comparison of the radiation-induced effects on smaller and larger devices, transistors fabricated on commercial components were tested as well. While specific sizing and fabrication information is not available for the individual transistors on the two inverter chips tested, the devices are believed to be rather larger. This notion is based on the measured maximum currents drawn from the devices prior to radiation exposure, which were about 7.2mA for the components on MC14007UB and about 5.5mA and 3.1mA for the p-MOS and n-MOS components, respectively, on CD4007UBE. Furthermore, the datasheets for these chips indicate that these devices are capable of handling larger voltage rails of ±18V max [40, 41], which is not at all possible with devices on the order of 0.13μm. For sake of comparison, the maximum voltage allowable for the fabricated devices in this work is rated at about 1.6V [38], after which many undesirable characteristics begin. Based on the larger sizes, these devices may be even more susceptible to radiation induced damage because of the increased gate oxide thickness [23]. This is easily illustrated via the sub-threshold swing equation, which is inversely proportional to the oxide capacitance per unit area, C_{ox}. Therefore, the larger oxide thicknesses of the commercial components will result in an increased sub-threshold swing parameter.

Since these devices operate at larger voltages, the corresponding threshold voltage is bigger as well. Rather than on the order of millivolts, the thresholds are on the order of volts under normal operating conditions. Following the total dose irradiation process, the threshold voltage plots of Figure 39 resulted; (a) and (b) show the curves for the n-MOS and p-MOS structures, respectively. Again, it is noted that

only the first n-type transistor of each inverter chip survived the procedure, while all of the p-type parts endured. The trends observed in these devices are exactly the same as those shown in Figure 4 [2] in chapter 1 where the magnitude of the p-type threshold strictly increase in value and the n-type threshold start out decreasing only to return, and potentially surpass, the pre-irradiation value. On average, threshold voltage for the n-MOS components begins at 1.523V, decreases to 359.05mV, and returns to 1.284V, just below the initial level. Furthermore, the radiation is drastically reducing the threshold voltage of the p-MOS transistors from about -1.173V to -3.808V on average. This has even greater implications on the operating conditions when implemented in a logic circuit, and this will be discussed in more detail below in section 3.3.3.



(a)

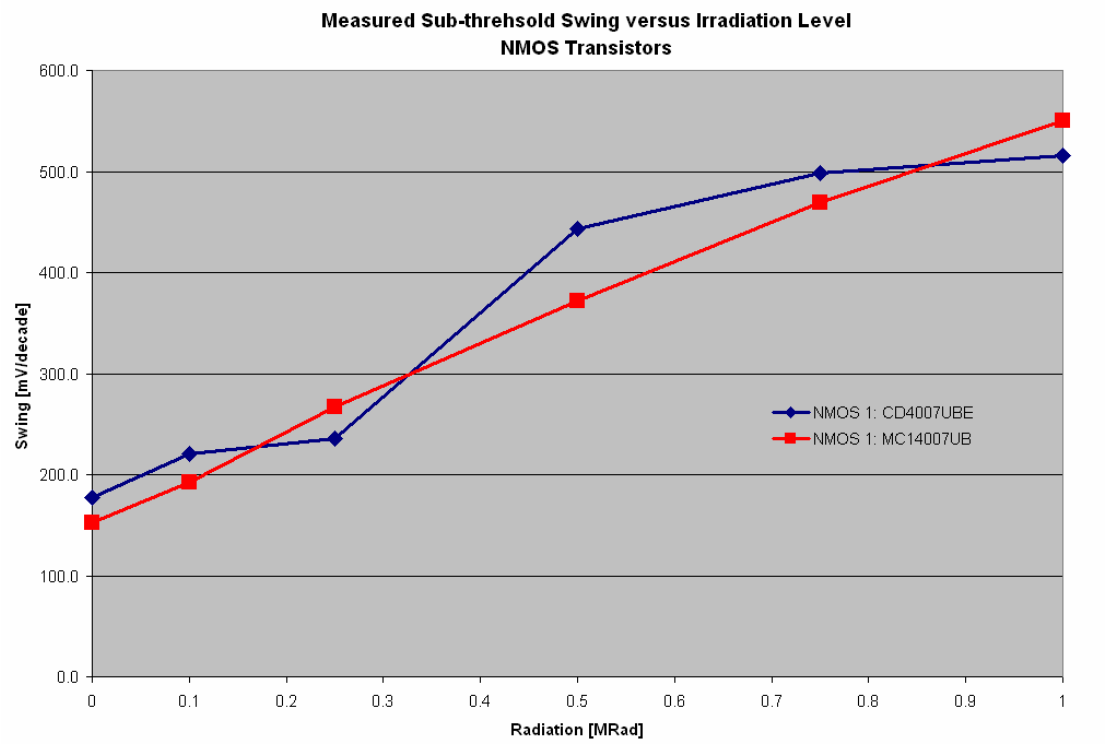


(b)

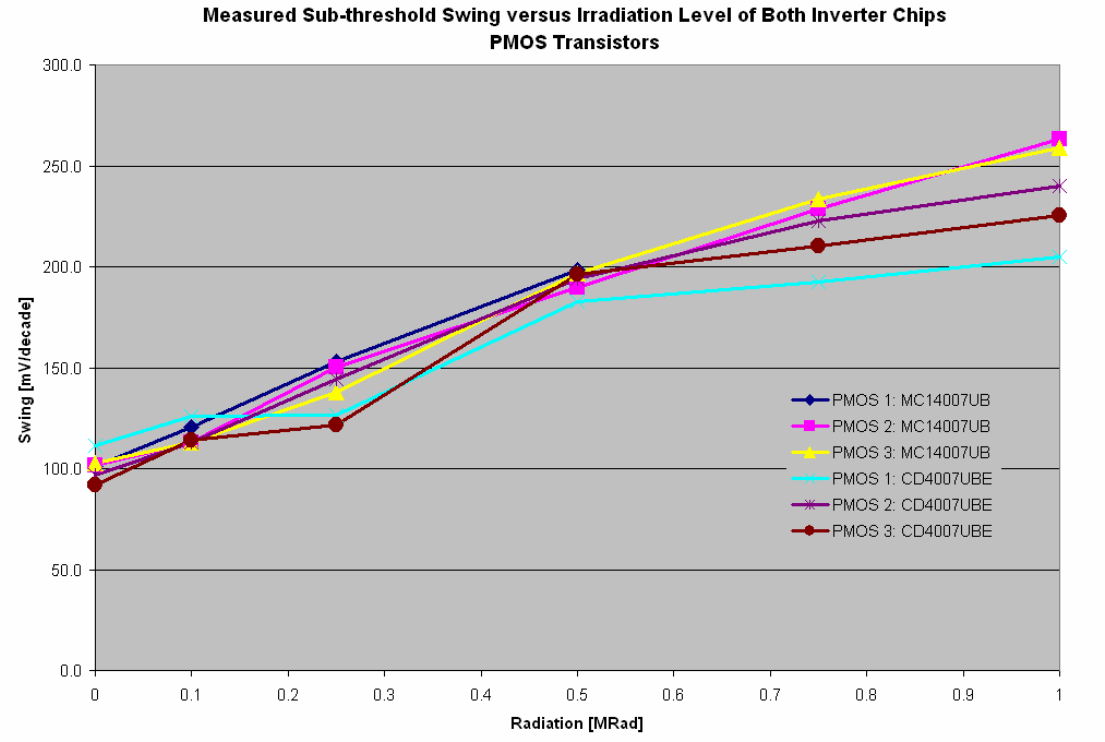
Figure 39: Measured Threshold Voltage versus Irradiation Level for the Individual (a) NMOS and (b) PMOS Transistors of the MC14007UB and CD4007UBE Inverter Chips

Not only are the threshold voltages being greatly affected, but the sub-threshold swing and leakage currents are also substantially altered and following the trends observed in the smaller 0.13µm fabricated structures. Figure 40 and Figure 41 below present the sub-threshold swing and leakage currents against the total dose, respectively, for the individual transistors of both tested inverter chips. Logarithmic leakage current is plotted in order to compare the results amongst the devices on both inverter chips, since the order of magnitudes are slightly different. Although the pre-irradiation swing values are slightly higher compared to those for the transistor array chips, the percent increase is even larger. This is exactly the result to be expected considering the increase in the oxide thickness for these larger devices. On average, the swing of the n-MOS devices was increased by about 225% from 165.159 to

532.858mV/decade, whereas that for the p-MOS devices was around 130.74% from 100.906 to 231.773mV/decade. These results also indicate a potential tendency for the n-MOS device to be more affected by irradiation than the p-MOS parts, which was similarly observed for the 0.13µm transistors. Moreover, the average ratios of pre-irradiation to post-irradiation leakage current increased as well, and were 1365.0 and 108.44 for the n-MOS and p-MOS devices, respectively. These percent and ratio increases are much larger than those for the smaller devices, providing more support of the observation these larger devices were more susceptible to fluctuations as a result of irradiation than their smaller 0.13µm counterparts. Clearly, these larger parameters will have more significant effects on power performance when utilized in a full system.

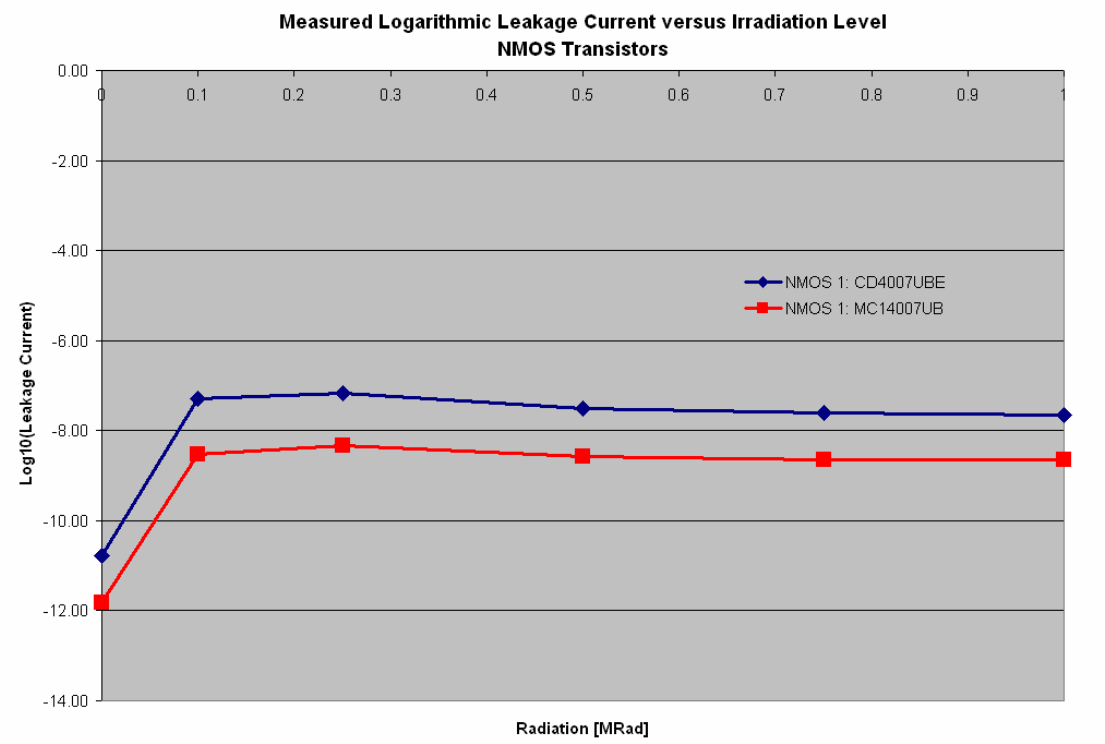


(a)

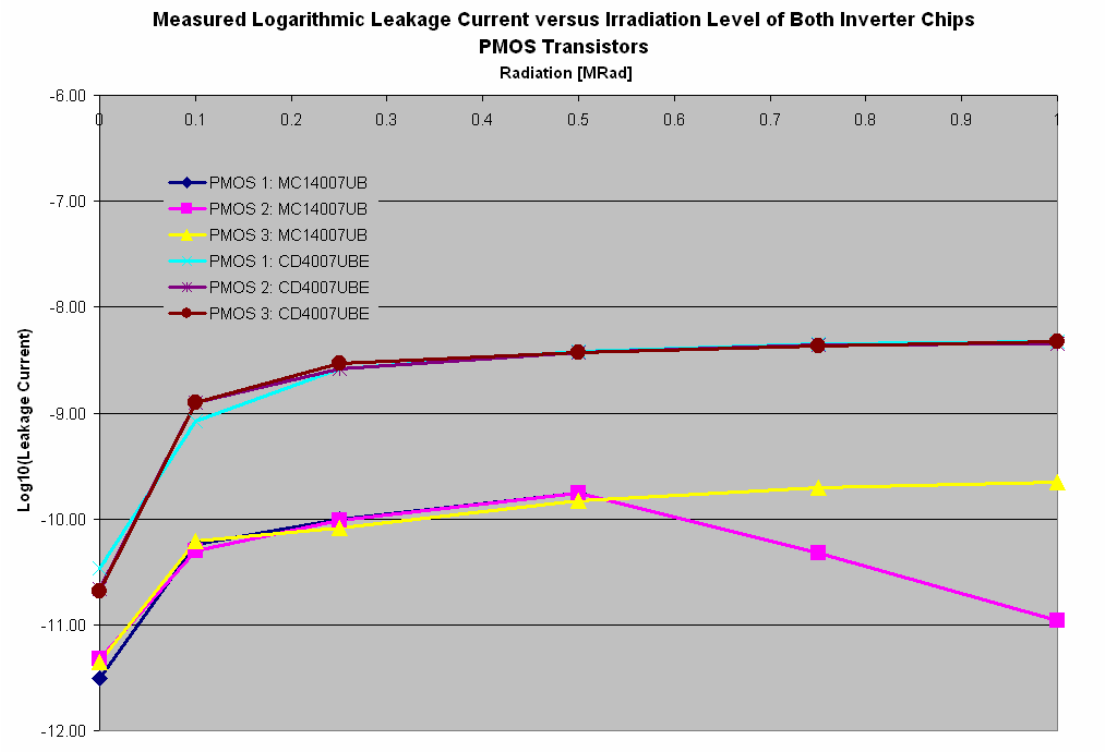


(b)

Figure 40: Measured Sub-threshold Swing versus Irradiation Level for (a) NMOS and (b) PMOS Transistors on the MC14007UB and CD4007UBE Inverter Chips



(a)



(b)

Figure 41: Measured Logarithmic Leakage Currents versus Irradiation Level for (a) NMOS and (b) PMOS Transistors on the MC14007UB and CD4007UBE Inverter Chips

3.3.3 Summary of Measured Testing Results

For ease of comparison, Table 4 below presents the quantitative changes in device parameters for the individual devices of the transistor array, MC14007UB, and CD4007UBE chips. Since the maximum changes of the 0.13µm devices did not necessarily correspond with the final total dose of 1MRad, the maximum change is also provided in the table. Moreover, unless otherwise specified, the values for the inverter chips were measured from the beginning to the end of the irradiation procedure. Note that the reason for the negative value for the percent increase in threshold voltage of the n-MOS at the end of the irradiations is due to the fact that the threshold did not fully return to the initial value. Similarly, the maximum percent

change of threshold for the n-MOS represents a negative shift since the threshold initially decreased, although a positive value is shown.

	% Increase Threshold Voltage	% Increase Sub-threshold Swing	Ratio Increase Leakage Current
Transistor Arrays			
Maximum			
NMOS	74.83	123.03	1.10E+02
PMOS	-2.22	46.849	1.24E+02
Begin to End			
NMOS	-21.79	105.75	7.61E+01
PMOS	0.222	27.071	8.08E+01
MC14007UB			
NMOS	239.11 (Max)	260.631	1.43E+03
PMOS	258.01	135.5	2.49E+01
CD4007UBE			
NMOS	544.92 (Max)	189.99	1.30E+03
PMOS	180.58	125.98	1.92E+02

Table 4: Comparison of Measured Average Transistor Fluctuations Resulting From Radiation Exposure

In summary, and which has briefly been mentioned throughout the presentation of the results, these increases in device parameters will have great implications on the power dissipation when used in circuits. The total sub-threshold power will increase for larger irradiations and have an impact on the total power dissipation of the circuits. Moreover, the commercial devices will result in even larger power issues for multiple reasons. The simplest of reasons is due to the larger sizes, but also because they are more susceptible to the radiation damage than the smaller 0.13μm devices. Even more, the voltages used for these devices are larger as well as the current flowing through the devices; this obviously directly leads to a larger power dissipation. Finally, these radiation-induced power dissipation changes will be the main focus of the next chapter where graphs and projections will be presented based on the data obtained via the individual transistor work.

Chapter 4: Logic Circuit Experiments

Characterizing the individual transistors is important to verify that theoretical trends are valid, while the extension of these device changes to fluctuations in circuit performance becomes the next investigation. This is the purpose of the work presented in this chapter. As was previously described toward the end of chapter 2, logic inverter circuits were simulated; as well as a similar 11-stage ring oscillator. More specifically, the power dissipation related effects were the primary focus of the testing procedures. The experimental setups will be described below and followed by an explanation of the measurement methods used to acquire the desired data. Then, the results of the simulations will be presented and discussed. Finally, the device characteristics of the measured devices will be applied to simulations for modeling the actual irradiation levels and projecting the resulting effects of radiation damage on the power dissipation in these similar logic inverter circuits.

4.1 Experimental Procedures

4.1.1 Simulation Setup

Similar to the simulations of the individual transistors, the Cadence software package and the IBM 8RF PDK, which consists of the 0.13µm CMOS technology, were used for simulation of the logic inverters. The effects of radiation on power dissipation of a single inverter is the main objective of these simulations, but also of interest is how the power is affected by the length of the logic chain. To this end, the

logic chains consisted of ten stages of identical sized inverters connected in series, where a stage simply means an inverter; 11 stages are actually pictured but the last is used to simply model a non-ideal output load. The stages were picked to be identical so that the effects of different transistor sizing were eliminated; although this is not typically employed in actual circuits. Furthermore, the sizing of the inverter transistors was chosen to center the "crowbar" region, which is the transition region, and offset the mobility differences between n-MOS and p-MOS devices as much as possible. Even more, two logic chains were constructed and simulated, one each for the 0.13µm and 0.18µm sized scales; same scales used for the different transistor array chips discussed in chapter 3. Figure 42 below illustrates the Cadence schematic and simulation setup for the logic chains of inverters.

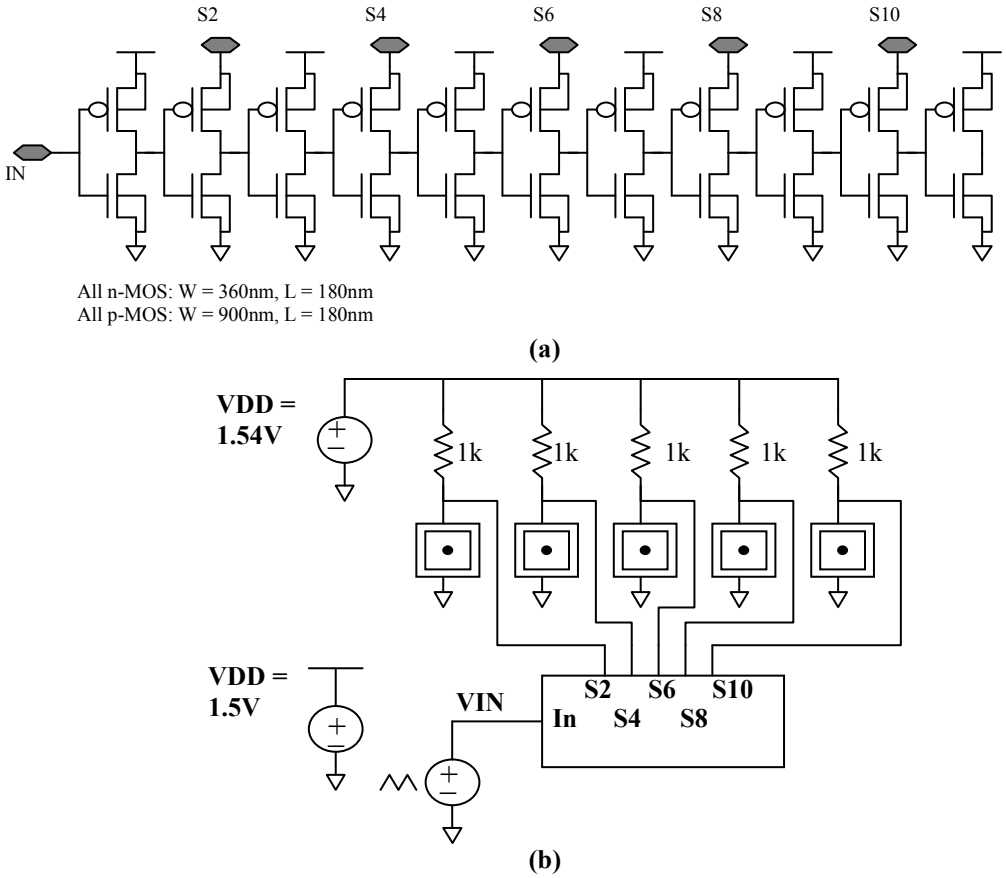


Figure 42: Cadence (a) Schematic and (b) Simulation Setup for the Logic Inverter Chains

The bottom schematic in the figure above contains bond pads and resistors along with the logic chain. These are used to model the physical testing setup, which will help the simulations better account for the possible effects of such extra components. In this configuration, the resistors are connected to the drains of the stages of desired monitoring, where the current through the resistor will equal the current through the associated inverter. Because of the relatively small current through the inverters, the voltage across them should have relatively low fluctuations, and remain fairly constant. The current through stages 2, 4, 6, 8, and 10 are being monitored and used for comparison. This is because the input and output voltages of these stages will be on the same cycle, resulting in easier graphical comparisons. Two input voltage sources were used for these simulations to observe the impacts of radiation on sub-threshold and total power dissipation. The initial input was a 1ms periodic ramp voltage from ground, 0V, to V_{DD}, which again is 1.5V for these sized transistors; this represents a linear sweep of possible input voltages. The second input was a square wave pulse where the high and low values were 1.5V and 0V, respectively, at a duty cycle of 50% and period of 1ms. In this fashion, the first stage acted as a non-ideal input into the second stage where the transition from high to low is not instantaneous as may be with an ideal source. Finally, just as was used for the single transistor simulations, the radiation exposure is modeled via the interface state capacitance term of the model files. The same range of values was used from 10^{-4} to 10^{-2}, including zero capacitance.

4.1.2 Measurement Techniques

Following the above procedure will result in the acquisition of the current versus time, and subsequently voltage versus time, for the various interface state capacitance values; these current plots will be much like the general graph previously shown in Figure 19. Having this data allows for the required calculation of average power dissipated over a switching cycle of the input voltage to the given gate. Using equation 13, and noting that the voltage across each inverter is constant and equal to the V_{DD} voltage rail, the average power is found by relatively simple integration of the current flow; of course, then multiplied by the voltage and divided by the period.

A MATLAB script was created to carry out the computations, where the only required inputs are the file containing the current flow data, and the corresponding φ_b parameters for the p- and n-type transistors; see Appendix B for the MATLAB script. The technique of integration employed was the trapezoidal method [44], which gets its name since the area over one interval is approximated by the product of the length of the interval and an average of the current values at the end points; this is the area of a trapezoid. Finally, this MATLAB file is used to generate the following graphs versus interface state capacitance to observe the trends of radiation induced damage: sub-threshold power over one cycle, total power over one cycle, percentage of total power associated with sub-threshold power over one cycle, and percentage of power related to sub-threshold power plotted against stage number for the various capacitances.

4.2 Logic Chain Simulation Results

The first subsection here will present the current through and output voltage of an inverter over one cycle of the input voltage at various interface state capacitances. The latter subsection will present the graphical representations of the calculated power via MATLAB over the capacitance range. Note that the input voltage used to generate the plots in section 4.2.1 was the periodic ramp signal, while those in section 4.2.2 utilized both the ramp and the periodic pulse signal.

4.2.1 Current and Voltage Over A Cycle

The current through a single inverter will reflect the operating conditions of the individual transistors creating the structure. In other words, and as was described in section 2.4.2 above, the graphical representation of current flow is expected to look like a spike in current around the center of the interval or cycle. This is exactly what occurs and shown in Figure 43 below for the simulated inverters. Furthermore, the figure illustrates how the increase in interface state capacitance affects this current plot. For larger capacitance values, the width of the spike decreases, which corresponds to the "crowbar" region of operation. The plot also becomes slightly shifted to the right for higher capacitances because of the increase in the threshold voltages of the individual transistors. The voltage input to this inverter is switching from high to low, so the p-MOS transistor will initially be 'off' while the n-MOS is 'on'. Thus for the higher capacitances, a larger input voltage is required before the current spike begins because the threshold of the p-MOS transistor is larger. Similar effects occur for the right side of the graph and the n-MOS transistor, however, the results are less drastic because the n-MOS threshold initially decreases, and results in

a smaller overall increase in threshold compared with the p-MOS device. This will decrease the "crowbar" region, and consequently increase the sub-threshold power, accompanied by the increase in leakage current through the inverter for larger capacitances, which is not easily seen in the graph below.

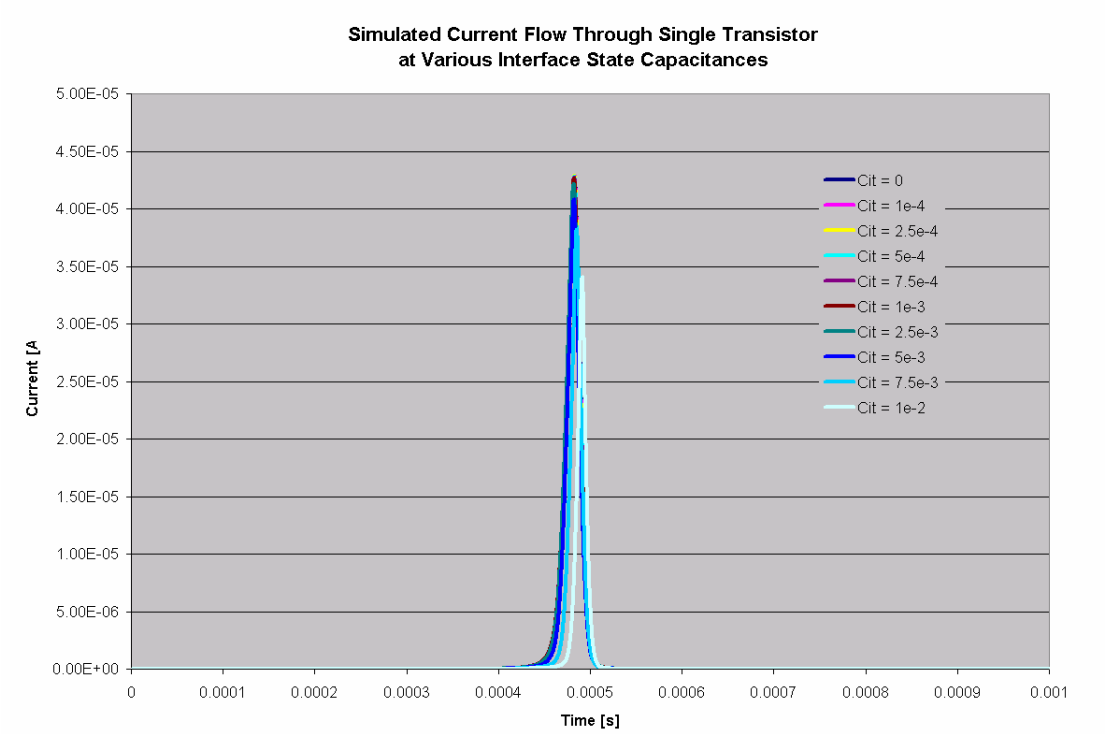
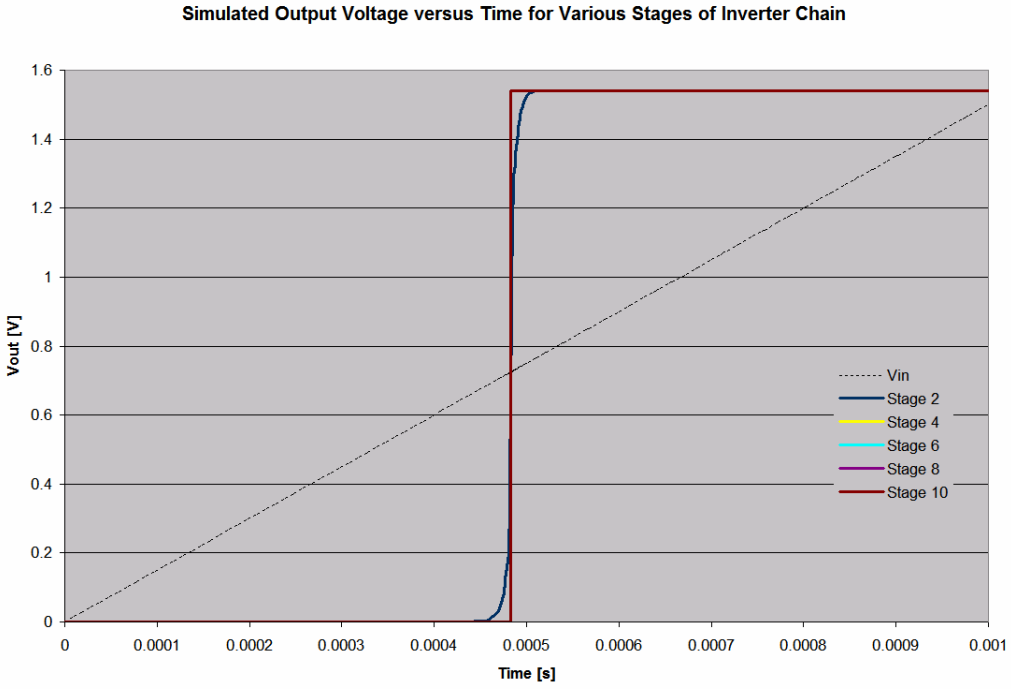


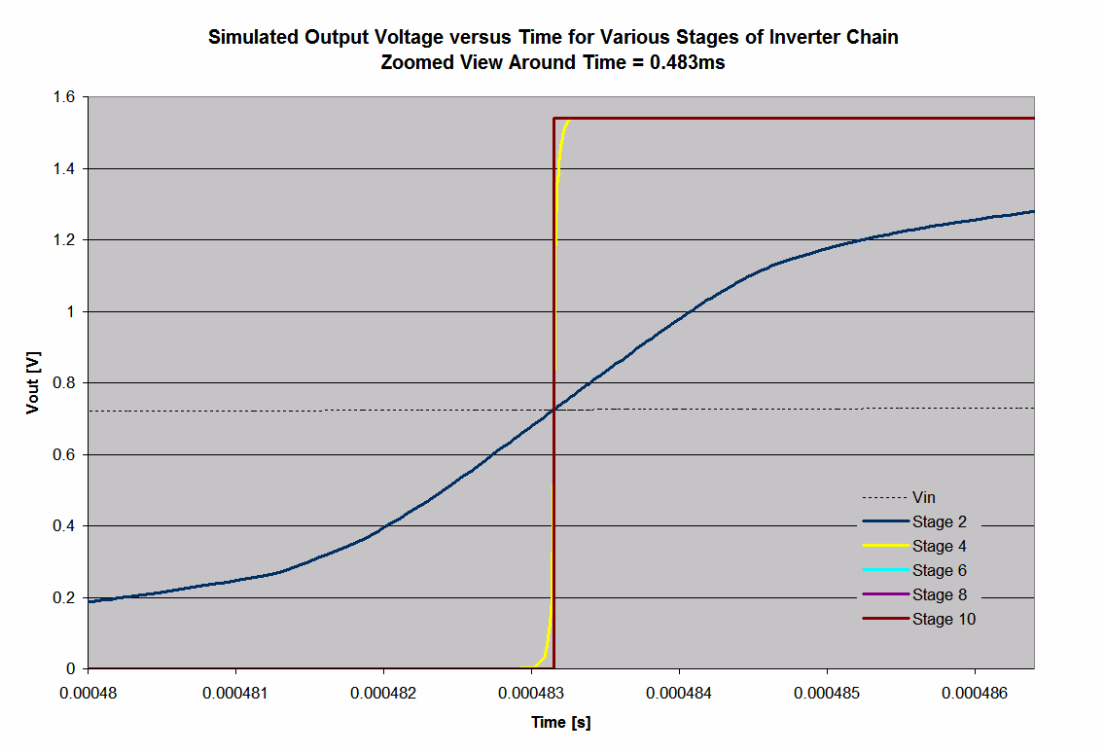
Figure 43: Current Flow Through a Single Inverter at Various Interface State Capacitances

Similar to the graph above is the plot of the current through the separate inverters of a logic chain, and how the width of the spikes decreases for the later stages. This can be inferred from the output voltage plot for the individual stages, which is shown below in Figure 44. This figure shows the output voltage for the even numbered stages of the 0.18µm scaled inverter chain at zero interface state capacitance. As expected, and clear from the plot below, the transition from low to high for the inverters is getting faster and faster for the later stages; this is clearer from the zoomed-in view, which is a little easier to see the additional stages. This

quicker transition further supports a shorter period of time in the "crowbar" region where both transistors are on and max current flows. In other words, the width of the current spike, similar to that in Figure 43 above, will decrease. Consequently, the sub-threshold interval will get larger and become more significant in terms of power dissipated; this is the subject of the next subsection.



(a)



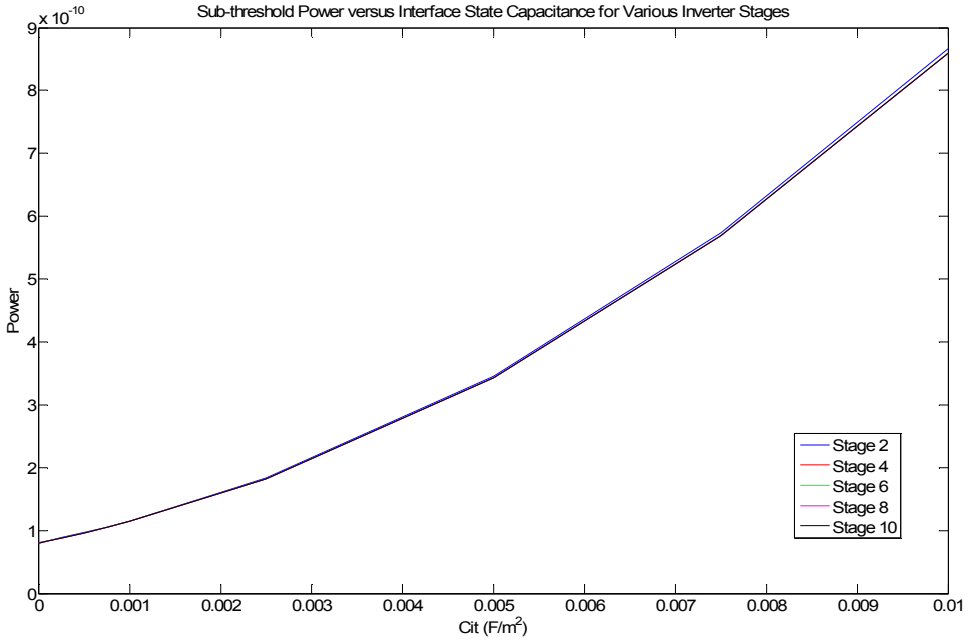
(b)

Figure 44: (a) Simulated Output Voltage for Individual Stages of a Logic Inverter Chain, (b) Zoomed-In View Around Transition Point

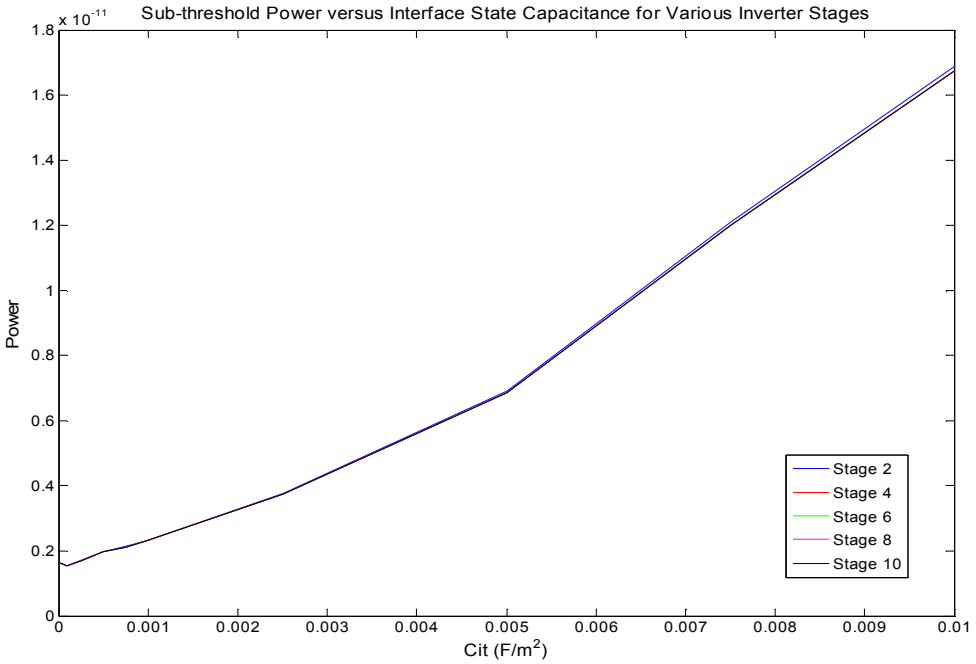
4.2.2 Power Over A Cycle

The current and voltage plots presented in the previous section are then used along with the MATLAB script to observe the effects on power. Again, the power measurements are average, simulated values and are found over one switching cycle of the input voltage. The first observation that is made from the power calculations is the increase in sub-threshold power as a result of increased interface state capacitance. Figure 45 below illustrates this trend, which is a combination of the increases in sub-threshold swing, threshold voltage and leakage currents of the individual devices; Figure 45(a) and (b) correspond to the periodic ramp and square signals, respectively. Note that the plots of the different stages are fairly identical, which is to be expected since the inverters are sized the same. Furthermore, the

increase is just about an order of magnitude larger at the end of the capacitance range compared with the beginning.



(a)



(b)

Figure 45: Simulated Sub-threshold Power Increase Against Interface State Capacitance for Various Inverter Stages: (a) Periodic Ramp Input and (b) Periodic Square Wave Input

Moreover, this increase in sub-threshold power becomes a larger percentage of the total power dissipated over the entire cycle; it can also be inferred from these percentages that the "crowbar" region is getting shorter. Figure 46 below portrays this power relationship for the various stages of the inverter chain. This plot was obtained using the ramp input voltage rather than the square wave because it better portrayed the increase as a result of increased interface density since the signal represents a gradual sweep of all input voltages. The percentage corresponding with stage 2 of the inverter chain is very difficult to observe in the figure because the transition of this stage is much longer where larger currents flow. Thus, the sub-threshold power will have a smaller effect on the total power of the logic gate; although less than 1%, the percent increase for this stage is a couple orders of magnitude.

This figure also portrays the observation that the sub-threshold power for later stages is more significant because the percent is much higher for stage 6, stage 8 and stage 10. The percentage appears to reach a maximum indicating that the "crowbar" contribution remains fairly constant for any later stages, since the percentage can be interpreted as a ratio of sub-threshold region to "crowbar" region. The greatest increase in percentage over the interface capacitance range seems to be associated with stage 4 where the increase is from about 1.5% to 15%. A more direct comparison of percentage corresponding with sub-threshold and stage number is illustrated further below in Figure 47; this plots percentage against stage number for the various interface state capacitance values. Furthermore, if the input signal to this type of circuit was changed to switch must faster, between high to low or low to high,

than the ramp signal used in this simulation, the sub-threshold region of operation would be expected to increase even further in significance.

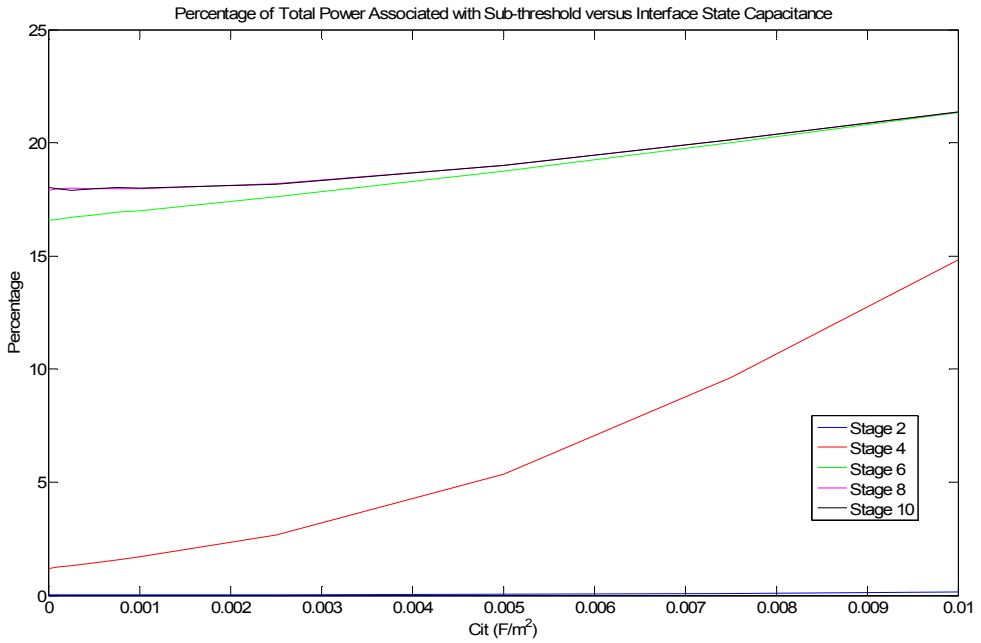


Figure 46: Simulated Percentage of Total Power Associated with Sub-threshold Region versus Interface Capacitance for Various Stages

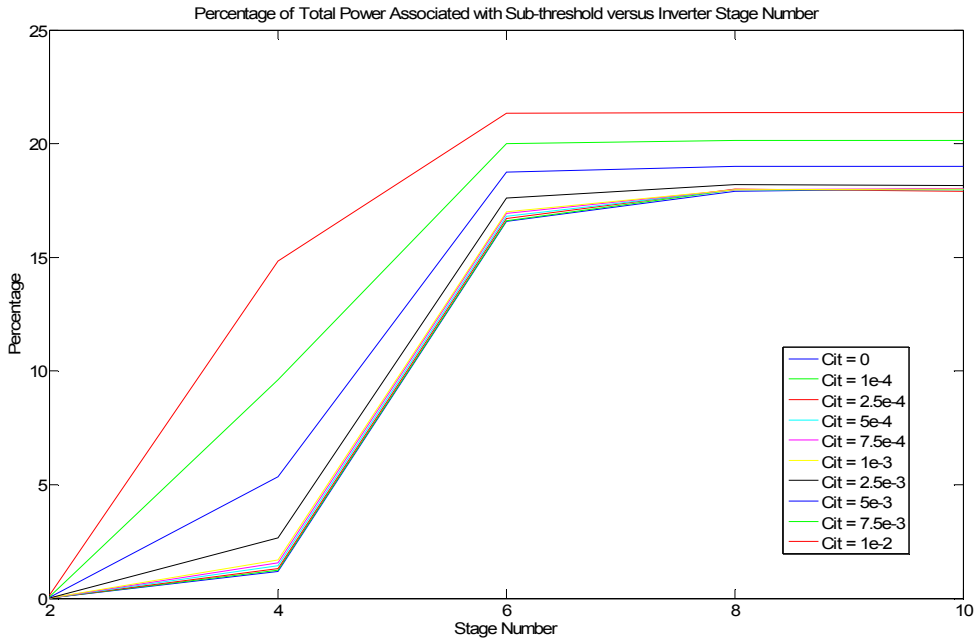


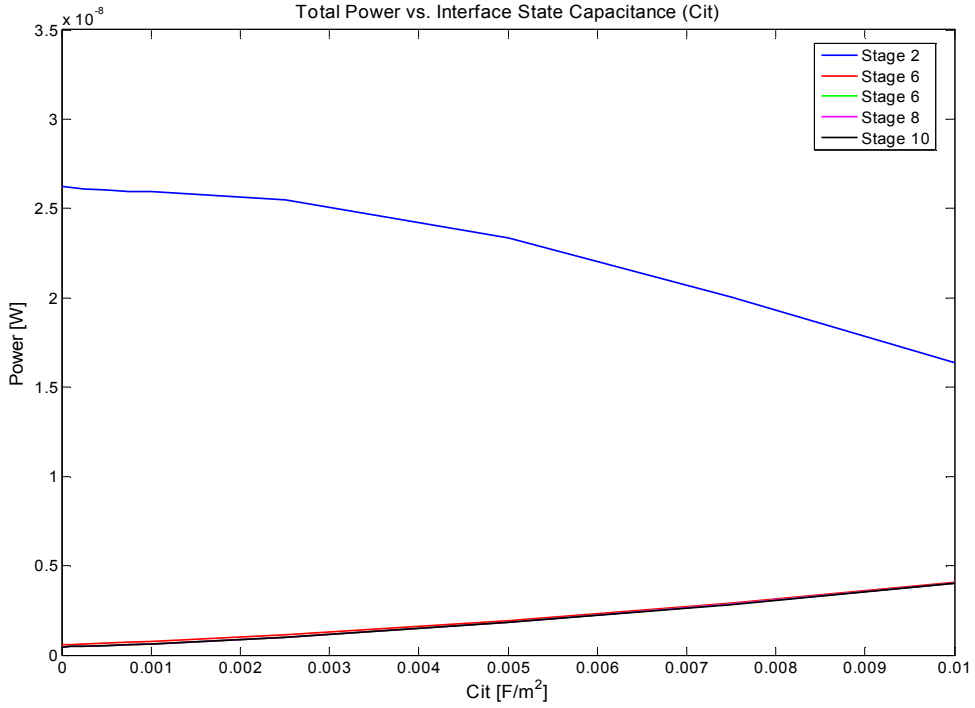
Figure 47: Simulated Percentage of Power Corresponding to Sub-threshold versus Stage Number for Various Interface Capacitances

While the periodic ramp signal helps illustrate the sub-threshold power related effects of irradiation, a more realistic input signal for inverters and logic structures is the square wave signal. Figure 45(b) above shows the increase in sub-threshold power for a square wave input signal and larger interface state capacitances, but the total power dissipated is also of considerable importance. The simulated total power versus interface state capacitance for the inverter chain is shown below in Figure 48; (a) portrays the contributions from the individual stages while (b) shows the summation of all five stages together.

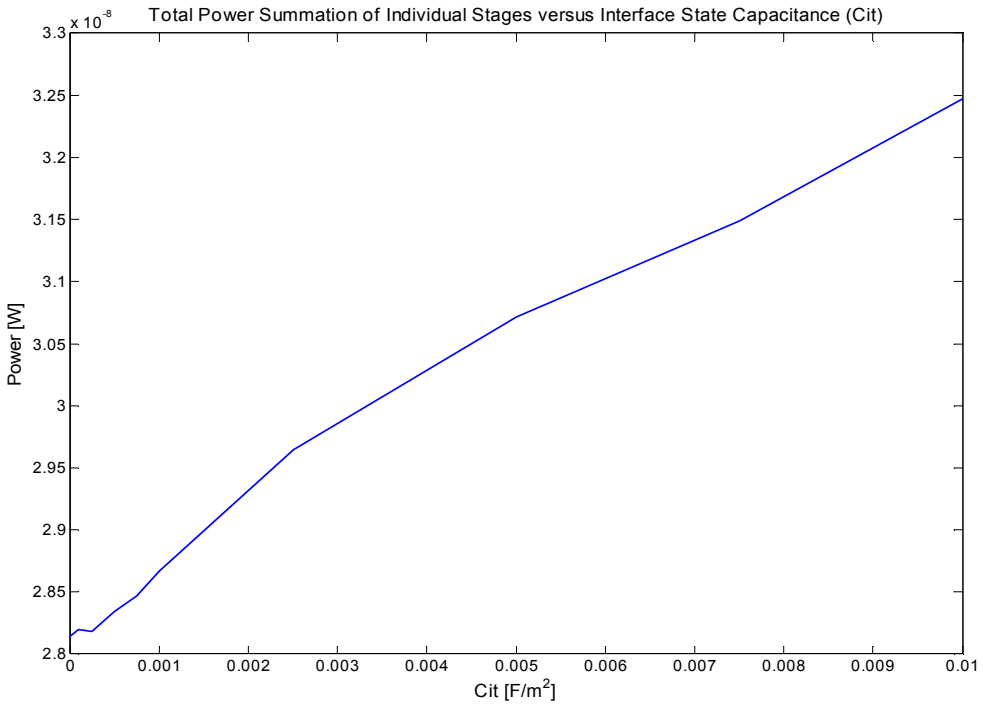
The total power associated with stage 2 decreases for increasing interface capacitance, whereas the power increases for the later stages, 4 through 10. The reason for this observation is that the width of the stage 2 "crowbar" region is decreasing for larger capacitance levels, and thus the contribution from the larger currents is becoming less significant as well. This is due in part to the fact that the earlier stages in the chain are much more dependent on the driving input source, which has constant, defined rise and fall times. Therefore, the earlier stages, including stage 2, are being driven more slowly where the components are remaining in the "crowbar" region longer, making the sub-threshold less effective. Furthermore, the increase in interface states are weakening the channel flow, subsequently decreasing the mobility [2, 25], which is the reason for the decrease in power dissipation; the mobility degradation can be seen from Figure 43 above where the peak current is decreasing for larger capacitance values. Moreover, the transitions for stages 4, 6, 8, and 10 are more dependent on the driving of the previous stages and becoming sharp enough that the corresponding "crowbar" contribution is remaining

relatively constant for the larger interface capacitances, while the sub-threshold contributions continually increase.

Despite the decrease in the second stage power, the summation of the total power over the individual stages still increases for larger capacitances. Thus, the total power associated with the circuit increases as well; the percent increase from beginning to end was about 15.389% from 28.14nW to 32.47nW. While these numbers may not seem very larger, when large amounts of similar circuits are connected within an entire system the total power will increase simply as a result of more components, making it even more susceptible to this percent increase as a result of radiation. Moreover, many of the inverter chains used within systems make use of an increase in transistor sizing for the later stages, typically a fixed ratio between a given stage and the previous stage. And so, the later stages dissipate even more power due to the larger current flow, resulting in an even more significant total power increase associated with the full circuit. If not accounted for, this increase can cause a fairly substantial inaccuracy in the projected total power dissipation. Finally, the increase appears to be relatively linear with respect to the interface state capacitance. This is to be expected because of the fairly linear dependence of the sub-threshold swing, threshold voltage, and leakage current increases with respect to interface capacitance.



(a)



(b)

Figure 48: Simulated Total Power Dissipation for Logic Inverter Chain versus Interface State Capacitance: (a) Individual Stage Contributions and (b) Sum of Stages

As a final remark here, the summation of total power increase with respect to the interface capacitance levels used is not solely dependent on the increases in sub-threshold power dissipation previously defined. This can be inferred from Figure 45 and Figure 46 above because the sub-threshold power is a couple orders of magnitude lower than the total power values; this is also reflected in the percentage plot. Although there is an increase in the sub-threshold region definition due to the increase in threshold voltage, Figure 49 below illustrates that there the total power is relatively independent of the threshold voltage. Note, the threshold voltage values in the plots were those measured values corresponding with the W/L = 360nm/180nm n-MOS transistor. Thus, while the increase in sub-threshold power does contribute to the increase in total power dissipated, the interface states are keeping the inverters in the linear triode region longer as well, taking away from the "crowbar" region, which remains relatively constant for higher levels and later stages. Therefore, the increase in total power dissipated is a combination of the increase in sub-threshold and linear triode regions, which translates into a shortening of the "crowbar" region when both transistors are in saturation.

The initial thought was that the sub-threshold region would be the main reason for an increase in total power since the "crowbar" region decreased, and that is why the sub-threshold definition in section 2.4.1 was used. However, following these simulations and results, the region of interest could be altered to include the linear triode region, providing a more accurate reasoning behind the increase in total power dissipation; the reason for this is due to the increases in current and swing. Furthermore, the leakage power may also need to be considered as a contributor

because the leakage currents are on the same order of magnitude as the sub-threshold currents. Finally, while the major contribution of power increase as a result of increased interface density may come from a few different regions, the underlying principle here is that the "crowbar" region is losing significance because of shorter times being spent in this region where both transistors are conducting maximum current and power dissipation.

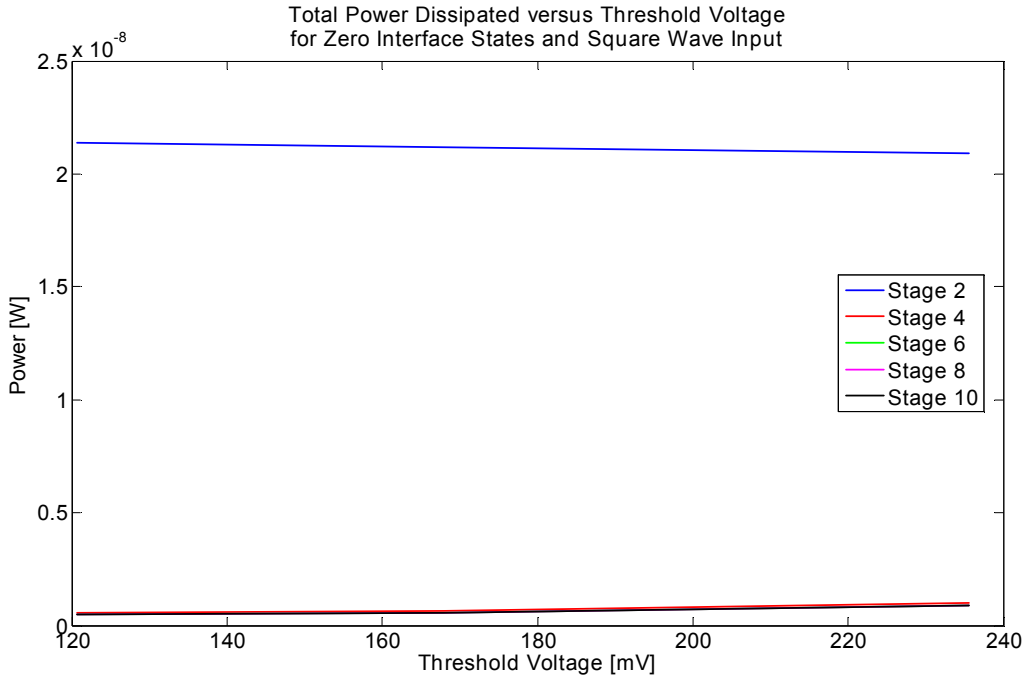


Figure 49: Simulated Total Power Dissipated versus Measured Threshold Voltage Variations in 360nm/180nm n-MOS Device

4.3 Projected Power Measurements Based on Single Transistor Data

Following extraction of device parameters via the experimental data, these results were then used to run similar simulations as those above. These new simulations will lead to a better projection of the power dissipated for the various physical radiation levels. The basic idea was to find the interface capacitance associated with the different radiation levels and then input these values into the

model files. Cadence would then be used to simulate the same logic chains as before, where the sizes corresponded to the devices used to extract the interface capacitances. Finally, the new simulations would be input into the same MATLAB script for computation of the different power plots versus radiation level.

The initial step of this process was to calculate the approximate change in interface state density, and subsequently interface capacitance, using sub-threshold swing parameters taken from the 0.18μm transistors. The devices of interest for these simulations were those that survived all, or at least most, of the irradiations. Equation 8 above was used to find the pre-irradiation interface capacitance; these non-zero interface states are not necessarily associated with radiation, but rather inherent interface states of the devices. Then, equation 2 was used to find the change in interface state density where the pre-irradiation values were used as reference levels; S_{D1} and D1 corresponded to the pre-irradiation values. An interface state capacitance was then calculated by dividing the change by an electron charge, q, and adding the result to the pre-irradiation interface capacitance. Figure 50 below shows the estimated interface state capacitance for the various transistors used in these projection simulations at the testing irradiation levels. The range of capacitance values calculated was on the order of 10^{-3} and 10^{-2} F/m^2. This is the same order of magnitude corresponding to the range of C_{it} values used in all prior simulations and provides support that they were appropriate for modeling the physical irradiation levels used in this work. Notice that these values follow the same trend as the corresponding sub-threshold swing and increase for larger radiation exposures.

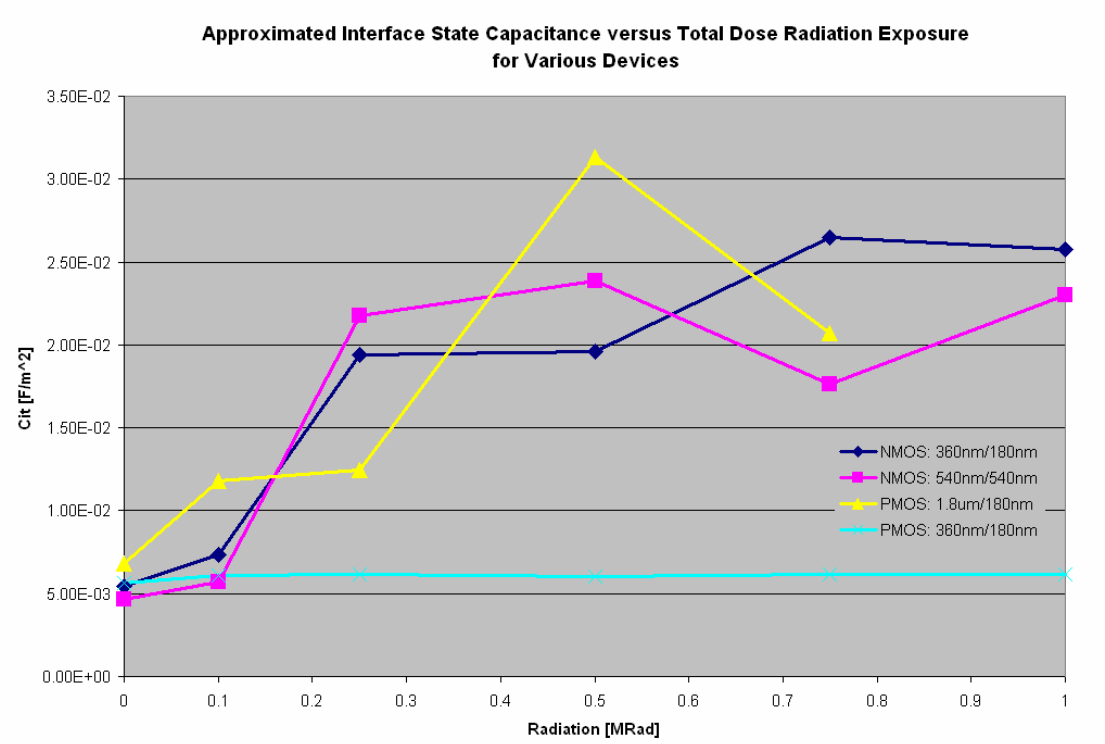


Figure 50: Approximated Interface State Capacitance Associated with Various Transistors at the Different Irradiation Levels

After knowing these interface state capacitances, they were then input into the different model files for the n-MOS and p-MOS transistors to model the actual irradiation levels used [38]. This was accomplished just as previously described in this chapter. The transistors used to construct these inverters were not exactly the size of those used in the previous simulations, and thus were chosen to get the transition and offset as close as possible to the previous inverters. Based on this idea, the inverters used here were of the following configuration: n-MOS W/L = 3/3 = 540nm/540nm and p-MOS W /L = 2/1 = 360nm/180nm; Figure 51 shows the schematic used for simulations. Note that this N-to-P ratio of 2, discounting the gate length difference, is fairly close to the ratio of 2.5 for the previously simulated inverters.

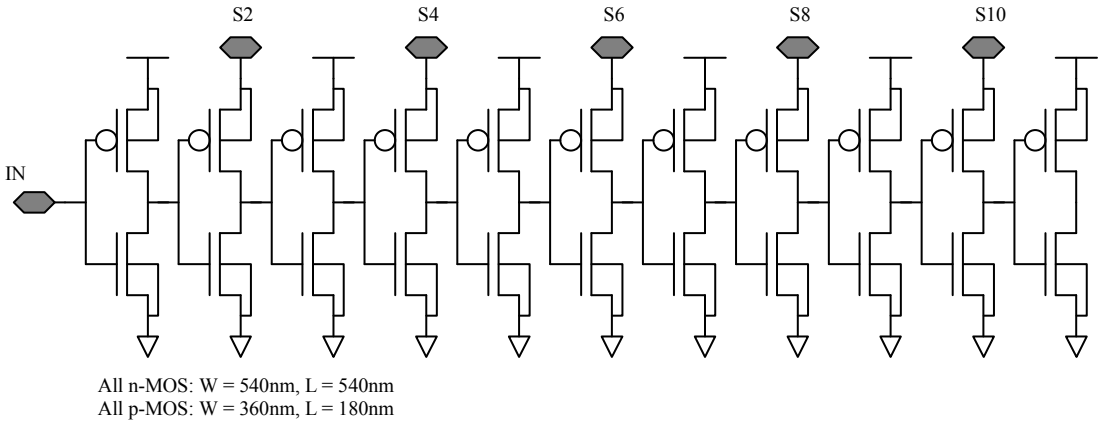


Figure 51: Schematic of Logic Inverter Chain Used for Projecting Power-Related Effects Via Acquired Experimental Data

Simulation data obtained via the above Cadence schematic was then input into the MATLAB script to project the power dissipated versus interface capacitance. Since the interface capacitance values corresponded to a given irradiation level, the power curves were plotted versus the irradiation level rather than capacitance. Note that equation 8 tends to underestimate the sub-threshold swing for p-MOS devices, which as a result will lead to an underestimation of the interface state capacitance; as portrayed in Figure 32(b). Due of this fact, the values for the projected power dissipation may be slightly lower than would be physically observed. Figure 52 below shows the projected sub-threshold power dissipation versus radiation exposure level for the inverter chain above. Figure 53(a) and (b), further below, illustrate the total projected power dissipation for the individual stages and full circuit against radiation. The input signal used to obtain both of these plots was a square wave input as was described in the previous subsection. It is clear from the graphs that the sub-threshold and total power dissipated increase for larger radiation exposures, which again is to be expected. Similar to before, the stage 2 total power tends to decrease

for increased irradiation, which is due in part to the fact that the transition is not as quick as the later stages. In general, the total power summation of the individual stages increases for larger radiation levels, which has significant impact of power dissipation of full-scale systems. It is clear from the simulations in section 4.2 above and the projected power dissipation in this section that the power related issues associated with increases in irradiation cannot be overlooked for accurate modeling and designing of systems with the potential for radiation exposure.

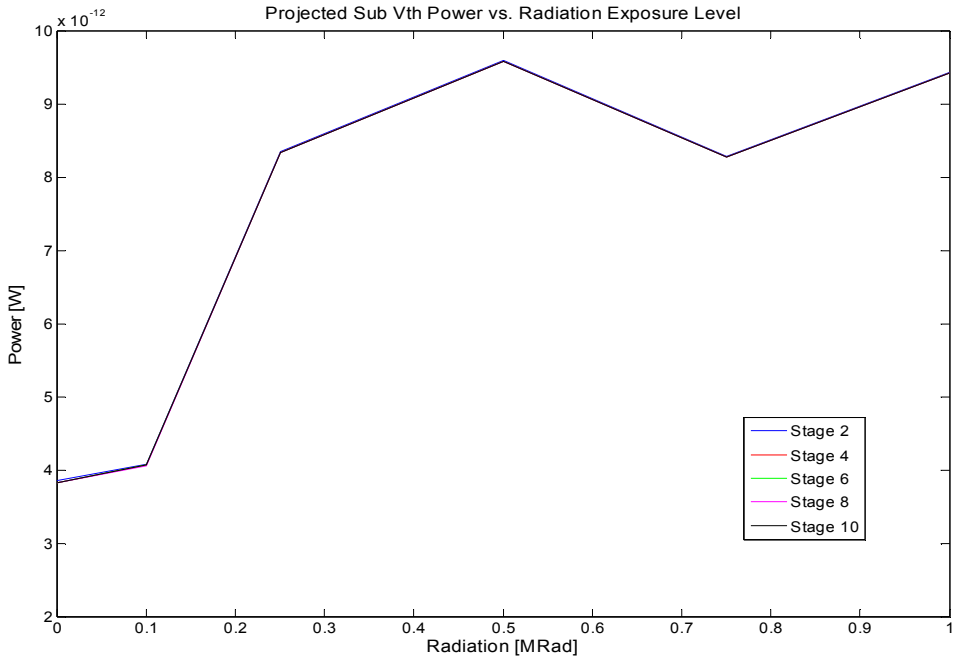
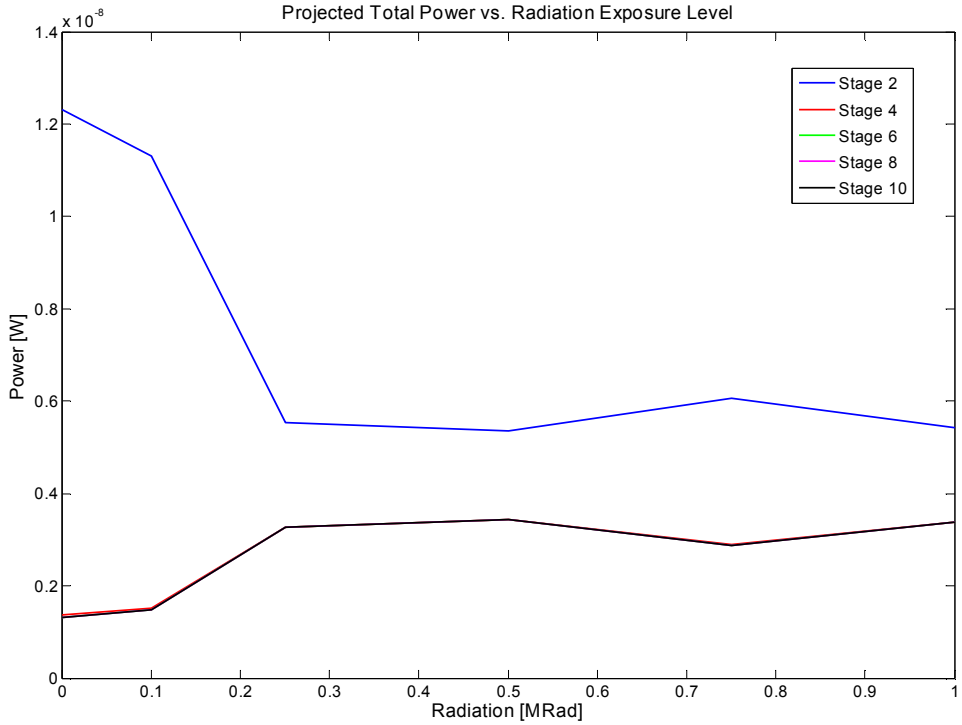
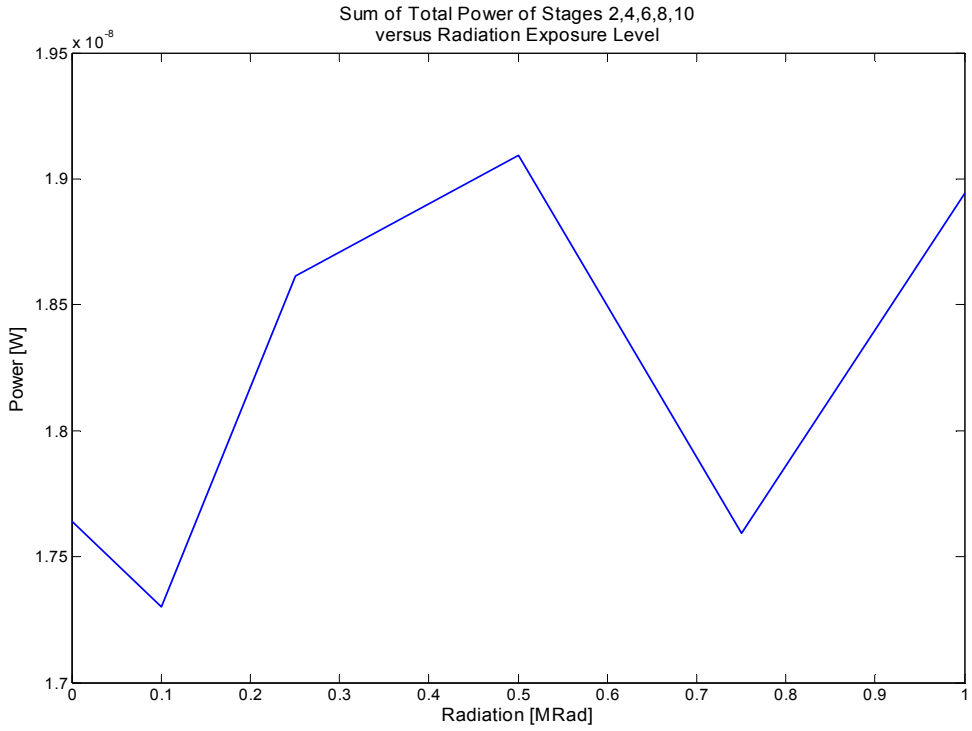


Figure 52: Projected Sub-threshold Power Dissipated versus Total Dose Irradiation Level



(a)



(b)

Figure 53: Projected Total Power Dissipated versus Total Dose Irradiation Level of (a) Individual Stages, and (b) Summation of Stages

4.4 An 11-Stage Ring Oscillator Experiment

A circuit very similar to the logic inverter chains presented above is the ring oscillator circuit. In fact, this circuit is identical to the inverter chain with the only modification coming between the input and output nodes. The output node of the final stage is connected to the input of the first stage, and the circuit is self-sustaining so long as an initial condition is placed on the feedback (FB) line to begin the oscillating. Similarly, the main focus of this simulation was to observe the power related effects of increased irradiations. Osborn et al. have reported the effects of irradiation on ring oscillator circuits, but the gate delay was the sole parameter of interest in these studies[49]. It was reported that power decreased for the larger irradiations, but no explanation or graphical representation was given [49]. The goal here will be to provide a physical model of this phenomenon.

An 11-stage ring oscillator was chosen for simulation because it was the same number of stages as the logic inverter chains simulated previously, and an odd number is needed for proper operation. The sizes of the transistors were also the same, and the Cadence schematic representation is shown below in Figure 54. As mentioned in the previous paragraph, an initial condition is needed to begin the oscillations. For purposes of this simulation, 0.1V was picked as the initial voltage on the FB line. Similar modeling techniques were used to represent the increase in radiation exposure where the interface capacitance term of the model files was varied. Rather than use all ten values as before, only the following capacitances were simulated: 0, 10^{-4}, $5*10^{-4}$, 10^{-3}, $5*10^{-3}$, 10^{-2}. The reason for choosing fewer values was for easier illustration of the resulting effects. The voltage and current of the

individual stages were monitored for the various capacitances to conclude on the observations.

All n-MOS: W = 360nm, L = 180nm
All p-MOS: W = 900nm, L = 180nm

Initial Condition on FB = 0.1V

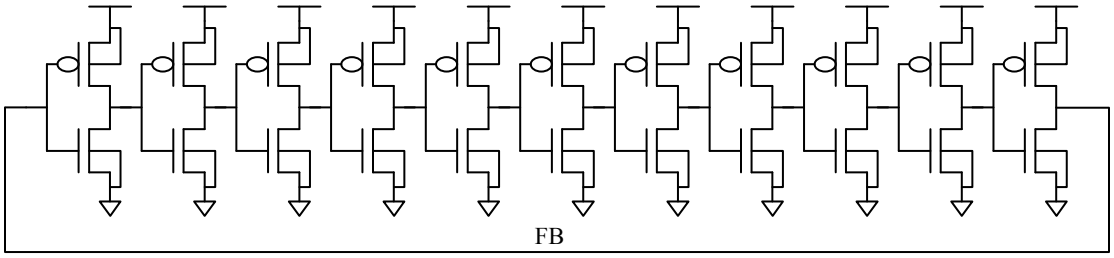


Figure 54: Cadence Schematic of an 11 Stage Ring Oscillator

The output voltage of all the stages is not going to be shown here because the graph is difficult to observe for all of the capacitances used, however these plots allow for calculation of the gate delay versus irradiation. This plot is shown below in Figure 55, and agrees very well with the results of Osborn et al. where the delay increases for increasing radiation levels [49]. The delay shown here was measured between the first and last stage of the 11-stage ring oscillator.

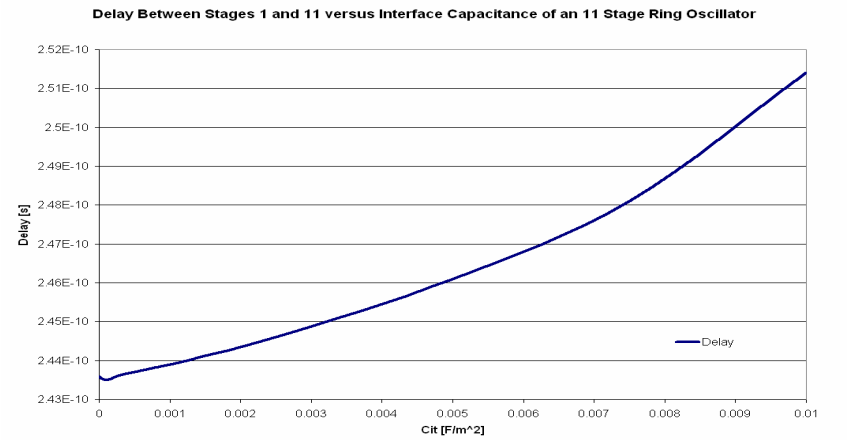
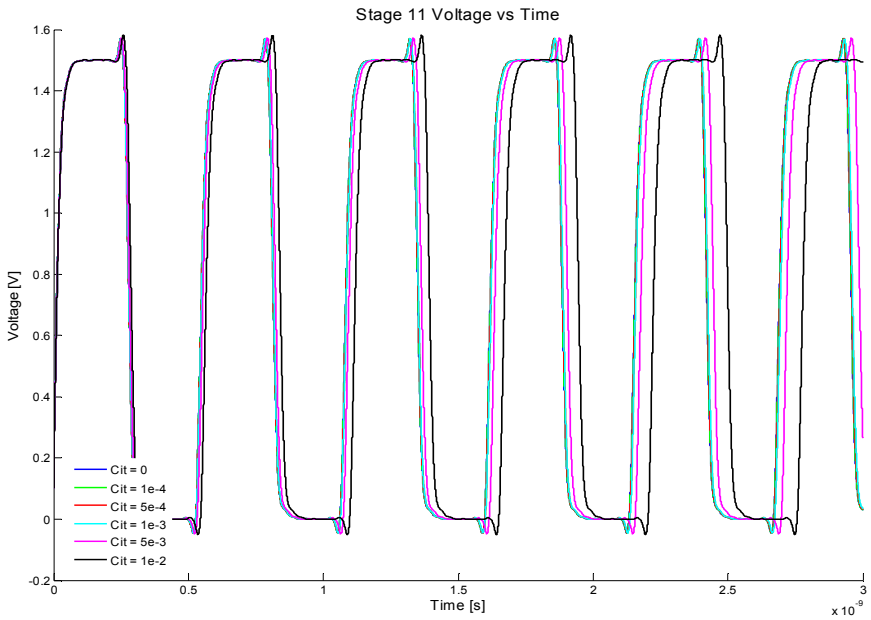
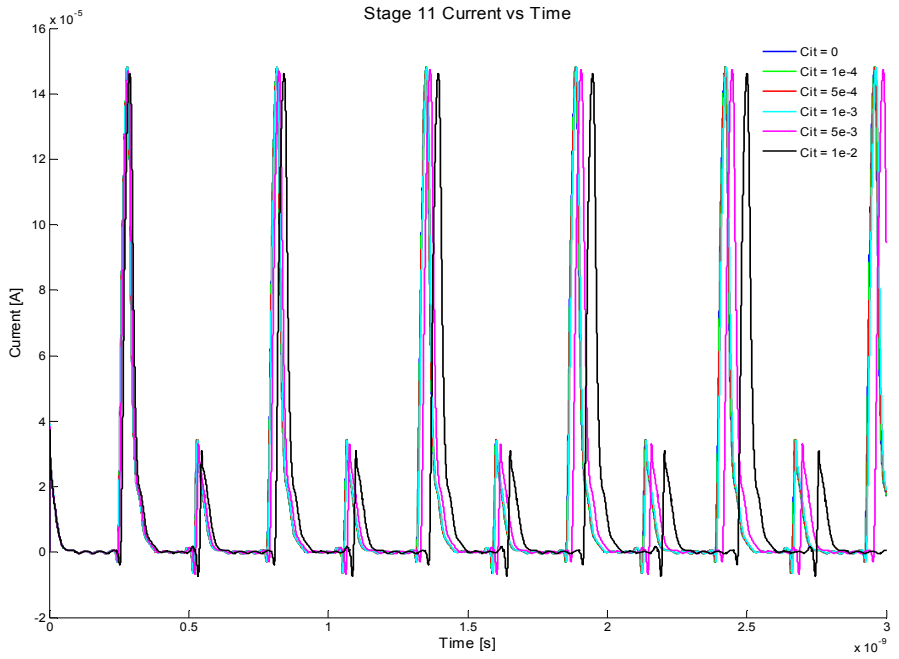


Figure 55: Gate Delay versus Interface Capacitance for an 11 Stage Ring Oscillator

Of more importance for this work is the power dissipated throughout the full oscillator versus interface capacitance; this was stated, and not shown, to decrease in the work by Osborn et al. [49]. The voltage and current of the output stage are important for discussing the reason the power does in fact decrease; these plots are shown below in Figure 56(a) and (b). As employed for the inverter logic chains, the power for the ring oscillator was calculated by integrating the current through the devices over one full cycle. Then, considering that the voltages and currents through each individual stage to be identical, and/or with negligible differences, the total power was found by multiplying the individual stage power by the number of stages, or eleven; the plot is shown further below in Figure 57. As seen in Figure 56(a), one result of the increase in interface capacitance is an increase in the period of oscillation. The interval of integration used for calculating the power dissipation took this period increase into account, as well as a general shift in plots that also occurred in the graphs.



(a)



(b)

Figure 56: Ring Oscillator Output (a) Voltage and (b) Current of Final Stage at Various Interface Capacitances

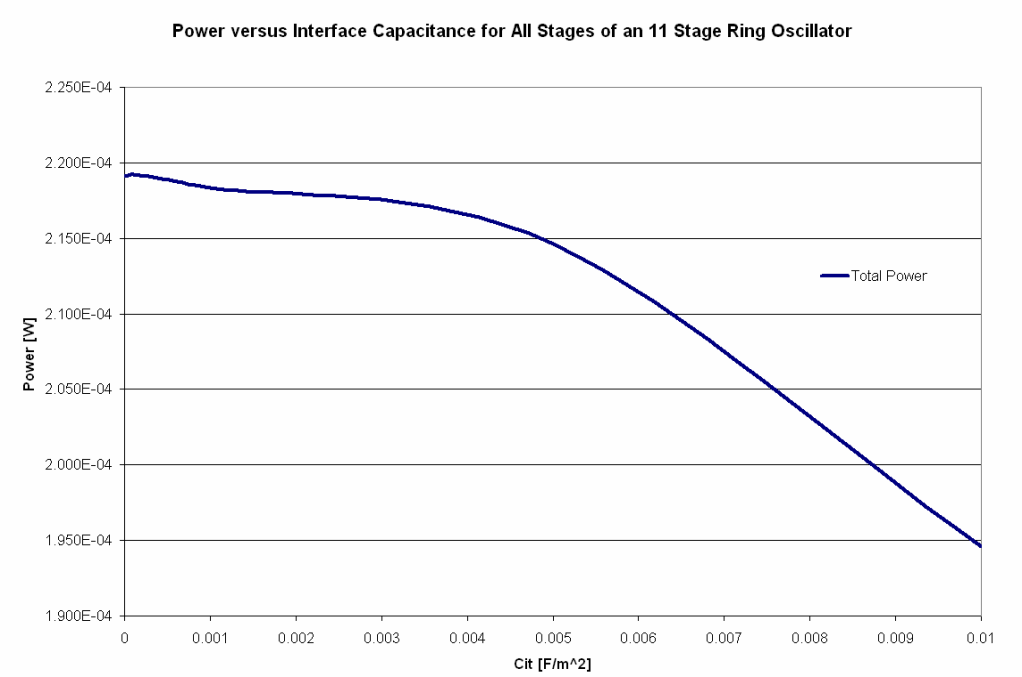


Figure 57: Total Power of Ring Oscillator for Various Interface Capacitances

Again, the power of the ring oscillator is decreasing for increased radiation exposure, modeled by interface capacitance. This result is different than that observed for the logic inverter chains, and the main reason is due to the feedback from the output to the input, which is not present in the logic inverter chains. Mobility degradation, which is observed in Figure 56(b) above, decreases the maximum current and results in a longer time necessary for a given stage to drive the subsequent stage. This further leads to the increase in period that is observed in the voltage, and current, plots. Thus, because of the feedback, the ring oscillator is compensating for the decrease in mobility by increasing the time period of one oscillation cycle. Furthermore, a decrease in the frequency occurs as a result of the larger period. This is the reason for the power decreasing at larger capacitances since a lower frequency directly relates to a decrease in power by $P = CV^2 f$. The capacitance term, C, represents the output node capacitance of the stage and remains relatively constant despite the increase in interface capacitance, which is part of this value. Finally, the amount of decrease in power for the oscillator is comparable to the amount of increase in gate delay [49]. Therefore, the power-delay product remains relatively constant over the interface capacitance range, which supports the observations already made in [49].

4.5 Summary of Circuit Performance Results

Refer to Table 5 below for a summary and comparison of the power related results following the modeled irradiations via simulation. The power dissipation is broken down into the following regions: sneak path, sub-threshold, linear and crowbar together, and total power over one cycle. The numbers represent the

summation of power from the even numbered stages of the logic chains, and were obtained using the MATLAB script provided in Appendix C. Furthermore, the single stage and total power, as well as gate delay and power-delay product results for the ring oscillator are also given in the table.

Logic Inverter Chain *Ramp Input*	Total Sneak Path Region Power [W]	Total Sub-Threshold Region Power [W]	Total Linear & Crowbar Power [W]	Total Power Over One Cycle [W]
Cit = 0 F/m^2	4.002e-10 *(0.031%)*	4.009e-10 *(0.032%)*	1.284e-6 *(99.9%)*	1.285e-6 *(100%)*
Cit = 1e-2 F/m^2	4.298e-9 *(0.68%)*	4.304e-9 *(0.69%)*	6.224e-7 *(98.6%)*	6.311e-7 *(100%)*
Logic Inverter Chain *Square Wave Input*				
Cit = 0 F/m^2	2.161e-9 *(7.68%)*	8.163e-12 *(0.029%)*	2.597e-8 *(92.3%)*	2.814e-8 *(100%)*
Cit = 1e-2 F/m^2	1.972e-8 *(60.7%)*	8.388e-11 *(0.258%)*	1.267e-8 *(39.1%)*	3.247e-8 *(100%)*
Projected Inverter Chain *Square Wave Input*				
Pre-Rad	6.422e-9 *(36.4%)*	1.916e-11 *(0.109%)*	1.120e-8 *(63.5%)*	1.764e-8 *(100%)*
1MRad	1.657e-8 *(87.4%)*	4.713e-11 *(0.249%)*	2.330e-9 *(12.3%)*	1.894e-8 *(100%)*

11-Stage Ring Oscillator	Single Stage Total Power [W]	Oscillator Total Power [W]	Gate Delay [s]	Power-Delay Product [W*s]
Cit = 0 F/m^2	2.0071E-05	2.2080E-04	2.4360E-10	5.3780E-14
Cit = 1e-2 F/m^2	1.9038E-05	2.0940E-04	2.5140E-10	5.2650E-14

Table 5: Summary of Power Dissipation Performance for the Various Logic Circuits Tested

The table clearly indicates that the region where both transistors are on, both the linear and "crowbar" region, are dissipating less power for larger interface state levels. Furthermore, the significance of these regions, which has been considered most important since maximum current flows, is decreasing in terms of percentage. The reason for this has to do with an increase in the amount of time spent in sneak path and sub-threshold, which subtracts from the available time in either linear or "crowbar". Moreover, the leakage currents increase as a result of interface states and further compounds the issue. Although the sub-threshold does increase for larger levels, the initial region of interest should be extended to include the sneak path or

part of the linear region since it is believed the interface states are contributing to longer times in these regions as well. It should be noted that the slow-varying ramp input signal is the reason the corresponding values are so low and the power decreases; this has to do with reasons explained in previous sections above.

The table also shows the decrease in power as a result of interface states for the 11-stage ring oscillator. The total power was calculated by simply multiplying the single stage power by the number of stages. Thus, the data shows that the decrease in power is proportional to the increase in gate delay, as reported by Osborn et al. [49]. Finally, this is more clearly indicated by the power-delay product which remains relatively constant for the varying interface levels, where the percent change was only about 2.1%.

Chapter 5: Conclusion

The research presented in this thesis focused on the radiation-induced damage to electronic components, including a simulation and testing effort to characterize standard silicon MOSFET devices fabricated using the 0.13μm CMOS technology. The primary objective of this work was to observe the effects of irradiations on device parameters and the corresponding damage to circuit performance. More specifically, the parameters of interest included the sub-threshold swing, threshold voltage, and leakage current of the individual transistors. These characteristics exhibited significant increases following simulations and 1MRad total dose irradiation from a Co^{60} gamma-ray source. A testing setup and procedure was created in order for measurements to also be taken at the 0.1, 0.25, 0.5, and 0.75MRad levels within the total 1MRad dose, which were compared with the pre-irradiation values. Such increases in individual device parameters result in substantial increases in the power dissipation of circuits employing such components. Furthermore, the circuits used to analyze the power related effects were logic inverter chains consisting of the transistor sizes tested. The current through the inverters were simulated using two 1ms periodic input voltage sources: a ramp signal and square wave signal. Simulated sub-threshold and total power dissipation over one cycle of the input was found to increase for larger interface state capacitances via simulations; the interface state capacitance was used to model the radiation exposure. Projected sub-threshold and total power dissipation also exhibited increases for the physical irradiation levels used

in testing; the projections were simulated using the interface capacitance associated with the 0.1 through 1MRad experimental levels.

A secondary observation from these experiments was to determine how the power dissipation effects depended on the length of the logic chains. While the sub-threshold power increased, it also became a bigger percentage of the total power dissipated at higher radiation levels. Moreover, this percentage also becomes more significant for the later stages of the inverter chains. An 11-stage ring oscillator was also simulated under similar conditions; this work was previously reported upon with no detailed explanation regarding the power related effects. The total power of the ring oscillator was found to decrease for larger interface capacitances, rather than increase as the inverter chains. The reason for this was due to the feedback of the output to the input, where the circuit compensated for decreasing mobility by increasing the oscillation period, subsequently decreasing the frequency and power. In conclusion, these power dissipation issues must be properly accounted for to best model, design, and analyze systems with potential for exposure to large amounts of radiation, such as space systems.

5.1 Contributions of this Research

The most important contribution of this research provided the researcher a better understanding with regards to the radiation environment and operation of standard MOSFET devices and circuits in such surroundings. Furthermore, this general contribution is a collection of smaller, individual contributions, and these will be described in the subsections to follow.

5.1.1 Irradiation Characteristics of Modern 0.13μm MOSFET Devices

Although much work had previously been completed in the area of radiation damage, much of the device research was completed a few decades ago. The devices and fabrication technologies used during those experiments were not as advanced as today's technologies, where the device dimensions were much larger than the currently used processes. In comparison, the MOSFETs used throughout this work, of the 0.13μm PDK technology, were fabricated using the state-of-the-art advancements in processing techniques. The devices were simulated, designed and fabricated using the Cadence software package and the IBM 8RF process. Even more, some of the additional devices tested were commercially available components whose characterization is important when considering these circuits are used within a larger system. Following the irradiations, the sub-threshold swing, threshold voltage, and leakage current parameters showed substantial increases as a result, which have further implications on operating conditions when used in larger systems.

5.1.2 Impact of Device Characteristics on Power Dissipation in CMOS Logic Circuits

The devices used for testing the radiation-induced damage were then configured into logic structures to observe irradiation effects on power dissipation. The logic structures were chains of inverters comprised of the transistor sizing previously tested, and were simulated using the Cadence software package and IBM 8RF process design kit; similar to the fabricated devices. Larger amounts of sub-threshold power were dissipated following an increase in the interface state capacitances because the threshold voltage, and consequently the sub-threshold region, increased, as well as the leakage current. Furthermore, the total power was

also found to increase for larger capacitance values, corresponding to higher irradiation levels. Projected power dissipation of these logic structures, which were obtained via the interface state capacitances extracted from the experimental data of the individual devices, followed these same trends at higher levels. The sub-threshold region also became a more significant percentage of the power for higher irradiation levels and for stages further down the inverter chains. All of these results support the fact that the power dissipation increase must be properly accounted for to best model, design and construct systems exposed to these radiation environments.

5.1.3 Comparison of Differently Sized, Irradiated Components

While both sets of individual devices, the 0.13μm and commercial, are smaller in size than components of previous decades, the commercial components are assumed to be larger than the 0.13μm counterparts; again, this is based on the allowable voltage rails and measured currents for the devices. These tests have provided experimental data comparing the effects of the larger devices with those of the smaller devices. Based on the extracted device parameters following total dose irradiations, the differently sized components exhibited slightly varied results. More specifically, the larger devices showed more significant impact on the sub-threshold swing, threshold voltage and leakage current because of the thicker oxide layer. This makes characterization crucial in exactly understanding the effects of COTS parts since they're typically larger dimensions and more readily available components, where the fluctuations will result in even more significant power dissipation problems.

5.1.4 Power of an 11-Stage Ring Oscillator

The power dissipation of an 11-stage ring oscillator, which is very similar to the logic inverter chain, was simulated over a range of interface capacitance values modeling radiation damage. While a similar circuit was irradiated, tested and reported in the literature, the main focus was on gate delay and the power was simply stated to decrease [49]; no full explanation was given as to why. The results of this work provided the reason behind the decrease in power for larger levels; the results agreed with those reported by Osborn et al. [49]. Increased irradiation levels increased the oscillation period, which decreased the frequency, and subsequently decreased the power since it's a product of capacitance, voltage squared, and frequency. Thus, the ring oscillator feedback, which is not existent in the logic chains, compensates for the mobility degradation by increasing the oscillation period.

5.1.5 Testing Setup and Procedure for Radiation Exposure

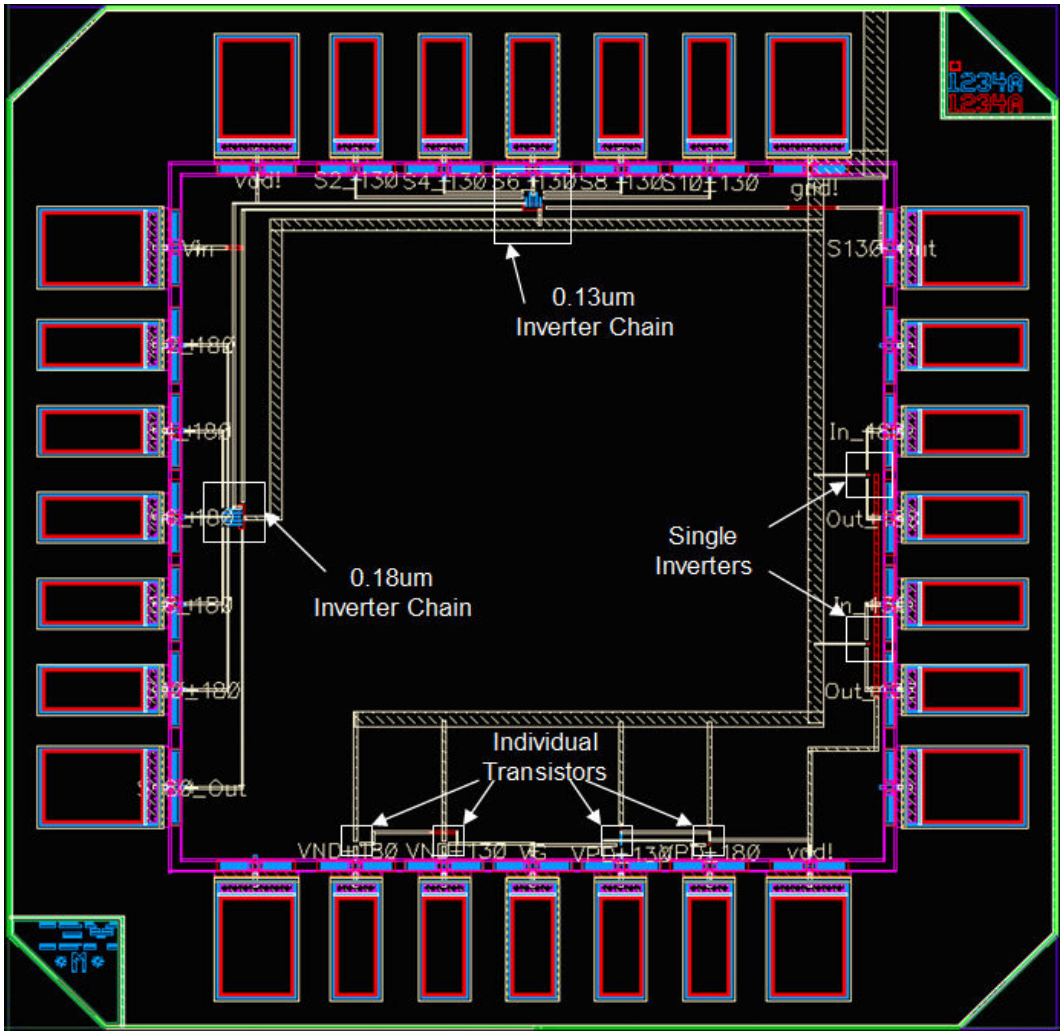
An irradiation procedure for a Gammacell 220 Excel Irradiatior source was provided for setting up the experiments and testing the individual devices, based on similar procedures previously reported in the open literature. This process includes techniques for extracting the necessary device parameters, as well as describing some of the necessary considerations when completing radiation exposures. Furthermore, two testing boards were designed and constructed for acquiring the necessary data of interest when used in conjunction with an HP4156B Semiconductor Parameter Analyzer and HP16058A Personality Board. A transistor array integrated circuit design was also provided and contained a variety of sizes for such irradiation characterization. While this chip design and these boards are specific to the 0.13μm

and commercial components, similar chips and boards for testing other devices can be designed using similar approaches.

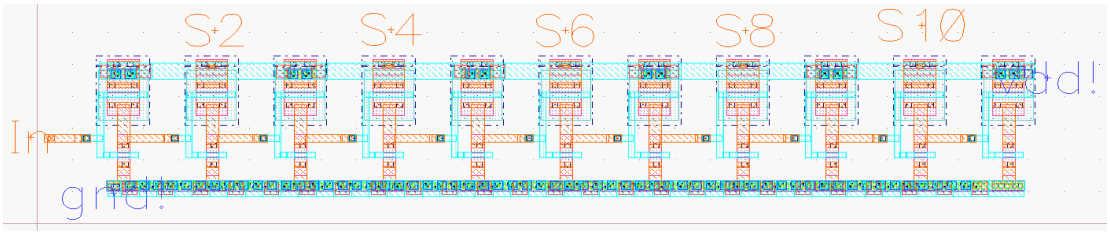
5.2 Recommendations for Future Work

5.2.1 Proposed Testing Setup for Fabricated Logic Chains

Based on the simulation schematic for the logic inverter chains, an integrated circuit was designed for fabrication and testing; although not received as of this writing. Cadence Virtuoso and the IBM 8RF PDK were used to layout two logic inverter chains, two single inverters, and four individual transistors; two each of n-MOS and p-MOS type; see Figure 58 below. Each logic chain utilized either the 0.13μm or the 0.18μm devices, and the same hold true for the individual inverters and transistors. Figure 58(b) shows a close up of a logic chain because the devices are so small that it is difficult to distinguish the chains in the large picture. Notice that the bond pads for this chip are surrounding the outside with no pads towards the middle of the chip. This makes packaging much more straightforward because overlapping bond wires should not become an issue, allowing all of the bonds to be connected with the package.



(a)



(b)

Figure 58: **Integrated Circuit Layout of (a) Full Logic Chain Chip and (b) Inverter Chain Close Up**

Having packaged the devices, they should be exposed to the same range of irradiations as the individual transistor chips. The single transistors on the chip should be biased appropriately during the irradiations, as described before, but

biasing is going to be more difficult for the inverters and the logic chains. Since the gates and drains of the n-MOS and p-MOS devices of an individual inverter are tied together, the biasing scheme above will not work. Thus, the intension for the biasing scheme used with the logic structures would be to have the devices 'on' and operating during irradiations. The same testing setup can be used to acquire data where the parameter analyzer and personality board are connected to the packaged chip. In this configuration, one of the SMUs will supply the ground while a second supplies the V_{DD}, and a third connection will supply a drain voltage equal to V_{DD} and monitor the current through the individual stages of interest: stages 2, 4, 6, 8, and 10. Finally, the acquired data will be compared against one another and analyzed via a similar MATLAB script that will calculate and plot the power related effects of ionizing radiation on circuit characteristics.

5.2.2 Alternative Radiation Sources

Many other topics related to radiation exposure can be studied and coupled with this work to better understand, model and design circuits for use in such environments. Since the space environment cannot be exactly replicated, any strides taken to further represent such surroundings will be extremely beneficial. The most significant combination of environments for study of space related damage includes irradiation tests run under low temperatures. This would result in one of the best representations of space surroundings and allow great observation related to the relationship between radiation and temperature. Low temperatures bring many additional and different considerations that must not be overlooked. Therefore, a test plan for this type of measurement would require similar, but slightly altered,

procedures to those discussed in this work to ensure that the setup does not drastically affect the data acquired. Similarly, and as was briefly touched upon in the introduction, gamma rays are not the only source of irradiation present in space. To this end, these same structures could be exposed to the different individual sources for comparison, and, if possible, to all of the sources in a single environment; this may not be possible, but again would well represent true surroundings. Taking this even one step further would be to test these components while under continuous exposure to the radiation rather than only following total dose.

With regards to the circuit components, inverters are not the only logic gates used in circuits, so other logic components should be tested to verify their individual functionality. Following these experiments, the components could be used to construct a more complex component or system for characterization on a larger scale. Furthermore, since radiation techniques have been studied to lessen the impact of irradiation on circuit performance, these same techniques could be employed to the logic circuits to observe how the methods help with power management. Moreover, the different, and even more exotic, process technologies could be utilized. Generally speaking, and as the case with many research avenues, the possibilities to better represent space environments are theoretically endless considering the vast range of phenomena. The realizations may prevent such representations, but strides towards this end become even more beneficial and significant.

Appendix A: Interesting Result of Gamma Irradiations

Just as an interesting note and something not anticipated prior to irradiations, the irradiation board had a drastic change in color as a result of the radiation exposure. The irradiation board and testing board, which was not exposed to any radiation, were constructed using two of the exact same prototype circuit boards. Thus, the testing board shows the color prior to irradiations, while the irradiation board shows the transformation in color after about 4MRad total dose of gamma irradiations; shown below in Figure A1.

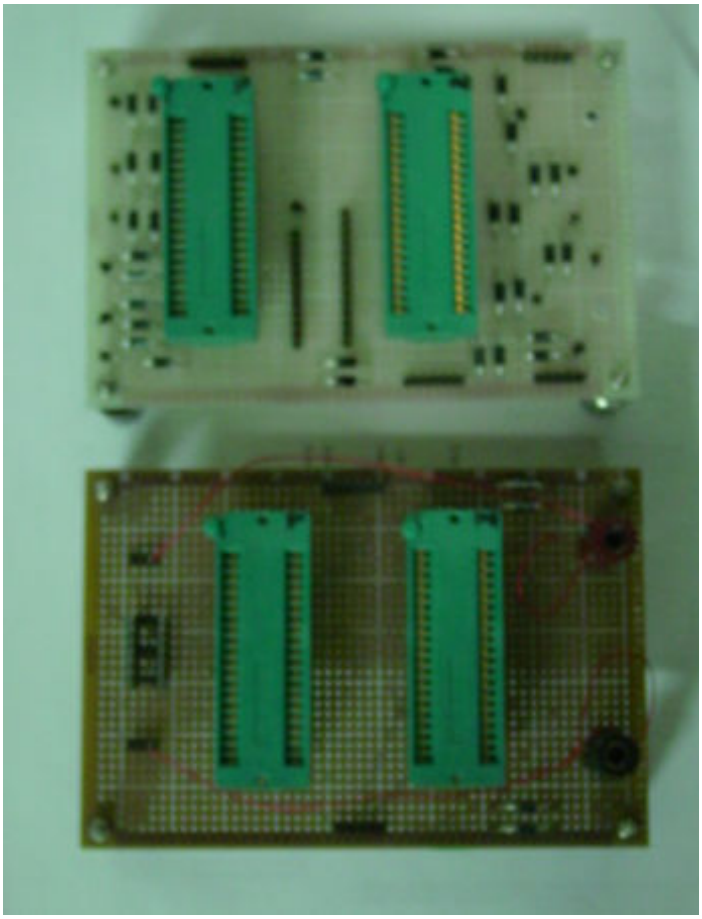


Figure A1: Comparison of Board Colors Before (Top) and After (Bottom) About 4MRad Total Dose Gamma-Ray Irradiation

Appendix B: MATLAB Script for Computing Power Values of Logic Inverter Chains

As was described in section 4.1.2, the MATLAB script below was created to carry out the necessary numerical power calculations and plots for the inverter chains.

MATLAB File:

```
% The purpose of this MATLAB script is to input inverter chain data
% obtained from simulations (or measurements), then run numerical integrations
% on the data to obtain the total power, and total subthreshold power, over
% one cycle of the input ramp dc voltage signal.  The percentage of the
% total power associated with subthreshold power is then calculated to
% observe the effects as they relate to the increase in interface state
% density, represented by Cit [F/m^2].

close all
%clear all
clc

%Read in the data from file
% fid = fopen('chaintestdata1.m','r');
% [A, count] = fscanf(fid,'%g %g %g %g %g %g %g',[7 inf]);
% A = transpose(A);
% fclose(fid);

phin = input('Input NMOS PhiB (or 0.5VTH) [V] = ');
Vn_lower = phin;
Vn_upper = 2*phin;
phip = input('Input PMOS PhiB (or 0.5VTH) [V] = ');
Vp_lower = 1.5-2*phip;
Vp_upper = 1.5-phip;

A = importdata('C:\Documents and Settings\jpwienke.ASDL-3\My
Documents\Thesis\Testing\Simulation Data - Inverter Chains\SC 180 - 1k Sin Input\Chain_Cit_1e-
2',','); %imports data, comma delimiter

% file = input('Input file name = ');
% A = importdata(file,',');

%Create vectors for variables and integration - Preallocation
[m,n] = size(A);
Time = zeros(m,1); Time_sum = zeros(m-1,1);
Vin = zeros(m,1); Vin_sum = zeros(m-1,1);
Stage2 = zeros(m,1); Stage2_sum = zeros(m-1,1);
Stage4 = zeros(m,1); Stage4_sum = zeros(m-1,1);
Stage6 = zeros(m,1); Stage6_sum = zeros(m-1,1);
Stage8 = zeros(m,1); Stage8_sum = zeros(m-1,1);
```

```
Stage10 = zeros(m,1); Stage10_sum = zeros(m-1,1);

%Assign values to variables
for j = 1:1:m
   Time(j) = A(j,1);
   Vin(j) = A(j,2);
   Stage2(j) = A(j,12);
   Stage4(j) = A(j,10);
   Stage6(j) = A(j,8);
   Stage8(j) = A(j,6);
   Stage10(j) = A(j,4);
end

%Plotting
subplot(1,2,1)
plot(Time,Vin)
title('Ramp Input Voltage Signal vs. Time')
xlabel('Time (s)')
ylabel('Vin (V)')

subplot(1,2,2)
plot(Time,-1*Stage2,'b')
hold on
plot(Time,-1*Stage4,'k')
plot(Time,-1*Stage6,'g')
plot(Time,-1*Stage8,'m')
plot(Time,-1*Stage10,'r')
title('Stage Currents vs. Time')
xlabel('Time (s)')
ylabel('Current (A)')
hold off

%Create vectors used for integration --> summing product of time step and
%current step
for j=2:1:m
   Time_sum(j-1) = abs(Time(j)-Time(j-1));
   Vin_sum(j-1) = Vin(j)-Vin(j-1);
   Stage2_sum(j-1) = (Stage2(j)+Stage2(j-1))/2;
   Stage4_sum(j-1) = (Stage4(j)+Stage4(j-1))/2;
   Stage6_sum(j-1) = (Stage6(j)+Stage6(j-1))/2;
   Stage8_sum(j-1) = (Stage8(j)+Stage8(j-1))/2;
   Stage10_sum(j-1) = (Stage10(j)+Stage10(j-1))/2;
end

%Using summation of products, integrate over one cycle and multiply by
%applied voltage to obtain power calculation
[p,q] = size(Time_sum);
SubVT2 = zeros(p,1);
SubVT4 = zeros(p,1);
SubVT6 = zeros(p,1);
SubVT8 = zeros(p,1);
SubVT10 = zeros(p,1);
for k = 1:1:p

   if Vin(k) > Vn_lower && Vin(k) < Vn_upper || Vin(k) > Vp_lower && Vin(k) < Vp_upper
%These values were obtained from making simulation measurements of Vth, and
```

```
%extracting back to find phib
      SubVT2(k) = 1.5*Stage2_sum(k);
      SubVT4(k) = 1.5*Stage4_sum(k);
      SubVT6(k) = 1.5*Stage6_sum(k);
      SubVT8(k) = 1.5*Stage8_sum(k);
      SubVT10(k) = 1.5*Stage10_sum(k);
   else
      SubVT2(k) = 0;
      SubVT4(k) = 0;
      SubVT6(k) = 0;
      SubVT8(k) = 0;
      SubVT10(k) = 0;
   end
end

%Calculate the percentage of the power associated with sub-threshold power
Period = Time(m)-Time(1);

disp('Total SubVT Stage 2 Power')
TSS2P = abs(sum(Time_sum.*SubVT2))/Period;disp(TSS2P)
disp(' ')
disp('Total Stage 2 Power')
TS2P = abs(sum(Stage2_sum.*Time_sum))*1.5/Period;disp(TS2P)
disp(' ')
disp('Percentage of Total Stage 2 Power as Sub Threshold')
PS2 = TSS2P/TS2P*100;disp(PS2)
% pause
% clc
disp('-----------------------------------------------------')
disp('Total SubVT Stage 4 Power')
TSS4P = abs(sum(Time_sum.*SubVT4))/Period;disp(TSS4P)
disp(' ')
disp('Total Stage 4 Power')
TS4P = abs(sum(Stage4_sum.*Time_sum))*1.5/Period;disp(TS4P)
disp(' ')
disp('Percentage of Total Stage 4 Power as Sub Threshold')
PS4 = TSS4P/TS4P*100;disp(PS4)
% pause
% clc
disp('-----------------------------------------------------')
disp('Total SubVT Stage 6 Power')
TSS6P = abs(sum(Time_sum.*SubVT6))/Period;disp(TSS6P)
disp(' ')
disp('Total Stage 6 Power')
TS6P = abs(sum(Stage6_sum.*Time_sum))*1.5/Period;disp(TS6P)
disp(' ')
disp('Percentage of Total Stage 6 Power as Sub Threshold')
PS6 = TSS6P/TS6P*100;disp(PS6)
% pause
% clc
disp('-----------------------------------------------------')
disp('Total SubVT Stage 8 Power')
TSS8P = abs(sum(Time_sum.*SubVT8))/Period;disp(TSS8P)
disp(' ')
disp('Total Stage 8 Power')
TS8P = abs(sum(Stage8_sum.*Time_sum))*1.5/Period;disp(TS8P)
```

```
disp(' ')
disp('Percentage of Total Stage 8 Power as Sub Threshold')
PS8 = TSS8P/TS8P*100;disp(PS8)
% pause
% clc
disp('-----------------------------------------------------')
disp('Total SubVT Stage 10 Power')
TSS10P = abs(sum(Time_sum.*SubVT10))/Period;disp(TSS10P)
disp(' ')
disp('Total Stage 10 Power')
TS10P = abs(sum(Stage10_sum.*Time_sum))*1.5/Period;disp(TS10P)
disp(' ')
disp('Percentage of Total Stage 10 Power as Sub Threshold')
PS10 = TSS10P/TS10P*100;disp(PS10)

%Create vectors to plot final calculations versus one another.  This
%process requires running the code over again with different Cit values.
%Copy the following five lines into the MATLAB work space in order to add
%information to the created vectors.

j = input('Input row number = ');
SUB_POWER(j,1) = TSS2P;
SUB_POWER(j,2) = TSS4P;
SUB_POWER(j,3) = TSS6P;
SUB_POWER(j,4) = TSS8P;
SUB_POWER(j,5) = TSS10P;
TOTAL_POWER(j,1) = TS2P;
TOTAL_POWER(j,2) = TS4P;
TOTAL_POWER(j,3) = TS6P;
TOTAL_POWER(j,4) = TS8P;
TOTAL_POWER(j,5) = TS10P;
PERCENTAGE(j,1) = PS2;
PERCENTAGE(j,2) = PS4;
PERCENTAGE(j,3) = PS6;
PERCENTAGE(j,4) = PS8;
PERCENTAGE(j,5) = PS10;
```

Appendix C: MATLAB Script Used to Breakdown Power Dissipation to Separate Regions

The MATLAB script shown here, similar to that in Appendix B, was used to calculate the power dissipation of the different regions of operation. Numerical integration techniques were again used to find the power specifically associated with the sneak path, sub-threshold, linear, and "crowbar" regions.

MATLAB Script:

```
% The purpose of this MATLAB script is to input inverter chain data
% obtained from simulations (or measurements), then run numerical integrations
% on the data to obtain the total power, and total subthreshold power, over
% one cycle of the input ramp dc voltage signal.  The percentage of the
% total power associated with subthreshold power is then calculated to
% observe the effects as they relate to the increase in interface state
% density, represented by Cit [F/m^2].


close all
%clear all
clc

%Read in the data from file
% fid = fopen('chaintestdata1.m','r');
% [A, count] = fscanf(fid,'%g %g %g %g %g %g %g',[7 inf]);
% A = transpose(A);
% fclose(fid);

phin = input('Input NMOS PhiB (or 0.5VTH) [V] = ');
Vn_lower = phin;
Vn_upper = 2*phin;
phip = input('Input PMOS PhiB (or 0.5VTH) [V] = ');
Vp_lower = 1.5-2*phip;
Vp_upper = 1.5-phip;

A = importdata('C:\Documents and Settings\jpwienke.ASDL-3\My
Documents\Thesis\Testing\Simulation Data - Inverter Projections\Inverter 2 - Square Wave
Input\Rad_Level_1MRad',','); %imports data, comma delimiter

% file = input('Input file name = ');
% A = importdata(file,',');

%Create vectors for variables and integration - Preallocation
[m,n] = size(A);
Time = zeros(m,1); Time_sum = zeros(m-1,1);
Vin = zeros(m,1); Vin_sum = zeros(m-1,1);
```

```
Stage2 = zeros(m,1); Stage2_sum = zeros(m-1,1);
Stage4 = zeros(m,1); Stage4_sum = zeros(m-1,1);
Stage6 = zeros(m,1); Stage6_sum = zeros(m-1,1);
Stage8 = zeros(m,1); Stage8_sum = zeros(m-1,1);
Stage10 = zeros(m,1); Stage10_sum = zeros(m-1,1);

%Assign values to variables
for j = 1:1:m
   Time(j) = A(j,1);
   Vin(j) = A(j,2);
   Stage2(j) = A(j,12);
   Stage4(j) = A(j,10);
   Stage6(j) = A(j,8);
   Stage8(j) = A(j,6);
   Stage10(j) = A(j,4);
end

%Create vectors used for integration --> summing product of time step and
%current step
for j=2:1:m
   Time_sum(j-1) = abs(Time(j)-Time(j-1));
   Vin_sum(j-1) = Vin(j)-Vin(j-1);
   Stage2_sum(j-1) = (Stage2(j)+Stage2(j-1))/2;
   Stage4_sum(j-1) = (Stage4(j)+Stage4(j-1))/2;
   Stage6_sum(j-1) = (Stage6(j)+Stage6(j-1))/2;
   Stage8_sum(j-1) = (Stage8(j)+Stage8(j-1))/2;
   Stage10_sum(j-1) = (Stage10(j)+Stage10(j-1))/2;
end

%Using summation of products, integrate over one cycle and multiply by
%applied voltage to obtain power calculation
[p,q] = size(Time_sum);
SubVT2 = zeros(p,1);
SubVT4 = zeros(p,1);
SubVT6 = zeros(p,1);
SubVT8 = zeros(p,1);
SubVT10 = zeros(p,1);
Sneak2 = zeros(p,1);
Sneak4 = zeros(p,1);
Sneak6 = zeros(p,1);
Sneak8 = zeros(p,1);
Sneak10 = zeros(p,1);
LinSat2 = zeros(p,1);
LinSat4 = zeros(p,1);
LinSat6 = zeros(p,1);
LinSat8 = zeros(p,1);
LinSat10 = zeros(p,1);
for k = 1:1:p

   if Vin(k) > Vn_lower && Vin(k) < Vn_upper || Vin(k) > Vp_lower && Vin(k) < Vp_upper
%These values were obtained from making simulation measurements of Vth, and
%extracting back to find phib
      SubVT2(k) = 1.5*Stage2_sum(k);
      SubVT4(k) = 1.5*Stage4_sum(k);
      SubVT6(k) = 1.5*Stage6_sum(k);
      SubVT8(k) = 1.5*Stage8_sum(k);
```

```
        SubVT10(k) = 1.5*Stage10_sum(k);
    else
        SubVT2(k) = 0;
        SubVT4(k) = 0;
        SubVT6(k) = 0;
        SubVT8(k) = 0;
        SubVT10(k) = 0;
    end
    if Vin(k) < Vn_lower || Vin(k) > Vp_upper
        %Sneak path region
        Sneak2(k) = 1.5*Stage2_sum(k);
        Sneak4(k) = 1.5*Stage4_sum(k);
        Sneak6(k) = 1.5*Stage6_sum(k);
        Sneak8(k) = 1.5*Stage8_sum(k);
        Sneak10(k) = 1.5*Stage10_sum(k);
    else
        Sneak2(k) = 0;
        Sneak4(k) = 0;
        Sneak6(k) = 0;
        Sneak8(k) = 0;
        Sneak10(k) = 0;
    end
    if Vin(k) > Vn_upper && Vin(k) < Vp_lower
        %Region where both transistors are out of sub-threshold
        LinSat2(k) = 1.5*Stage2_sum(k);
        LinSat4(k) = 1.5*Stage4_sum(k);
        LinSat6(k) = 1.5*Stage6_sum(k);
        LinSat8(k) = 1.5*Stage8_sum(k);
        LinSat10(k) = 1.5*Stage10_sum(k);
    else
        LinSat2(k) = 0;
        LinSat4(k) = 0;
        LinSat6(k) = 0;
        LinSat8(k) = 0;
        LinSat10(k) = 0;
    end
end

%Calculate the percentage of the power associated with sub-threshold power
Period = Time(m)-Time(1);

% disp('Total SubVT Stage 2 Power')
TSS2P = abs(sum(Time_sum.*SubVT2))/Period;disp(TSS2P);
% disp(' ')
TSnS2P = abs(sum(Time_sum.*Sneak2))/Period;
TLS2P = abs(sum(Time_sum.*LinSat2))/Period;
% disp('Total Stage 2 Power')
TS2P = abs(sum(Stage2_sum.*Time_sum))*1.5/Period;disp(TS2P);
% disp(' ')
% disp('Percentage of Total Stage 2 Power as Sub Threshold')
PS2 = TSS2P/TS2P*100;disp(PS2);
% pause
% clc
% disp('------------------------------------------------------')
% disp('Total SubVT Stage 4 Power')
TSS4P = abs(sum(Time_sum.*SubVT4))/Period;disp(TSS4P);
```

```
% disp(' ')
TSnS4P = abs(sum(Time_sum.*Sneak4))/Period;
TLS4P = abs(sum(Time_sum.*LinSat4))/Period;
% disp('Total Stage 4 Power')
TS4P = abs(sum(Stage4_sum.*Time_sum))*1.5/Period;disp(TS4P);
% disp(' ')
% disp('Percentage of Total Stage 4 Power as Sub Threshold')
PS4 = TSS4P/TS4P*100;disp(PS4);
% pause
% clc
% disp('-----------------------------------------------------')
% disp('Total SubVT Stage 6 Power')
TSS6P = abs(sum(Time_sum.*SubVT6))/Period;disp(TSS6P);
% disp(' ')
TSnS6P = abs(sum(Time_sum.*Sneak6))/Period;
TLS6P = abs(sum(Time_sum.*LinSat6))/Period;
% disp('Total Stage 6 Power')
TS6P = abs(sum(Stage6_sum.*Time_sum))*1.5/Period;disp(TS6P);
% disp(' ')
% disp('Percentage of Total Stage 6 Power as Sub Threshold')
PS6 = TSS6P/TS6P*100;disp(PS6);
% pause
% clc
% disp('-----------------------------------------------------')
% disp('Total SubVT Stage 8 Power')
TSS8P = abs(sum(Time_sum.*SubVT8))/Period;disp(TSS8P);
% disp(' ')
TSnS8P = abs(sum(Time_sum.*Sneak8))/Period;
TLS8P = abs(sum(Time_sum.*LinSat8))/Period;
% disp('Total Stage 8 Power')
TS8P = abs(sum(Stage8_sum.*Time_sum))*1.5/Period;disp(TS8P);
% disp(' ')
% disp('Percentage of Total Stage 8 Power as Sub Threshold')
PS8 = TSS8P/TS8P*100;disp(PS8);
% pause
% clc
% disp('-----------------------------------------------------')
% disp('Total SubVT Stage 10 Power')
TSS10P = abs(sum(Time_sum.*SubVT10))/Period;disp(TSS10P);
% disp(' ')
TSnS10P = abs(sum(Time_sum.*Sneak10))/Period;
TLS10P = abs(sum(Time_sum.*LinSat10))/Period;
% disp('Total Stage 10 Power')
TS10P = abs(sum(Stage10_sum.*Time_sum))*1.5/Period;disp(TS10P);
% disp(' ')
% disp('Percentage of Total Stage 10 Power as Sub Threshold')
PS10 = TSS10P/TS10P*100;disp(PS10);

TOTAL_SUB = TSS2P+TSS4P+TSS6P+TSS8P+TSS10P
TOTAL_SNEAK = TSnS2P+TSnS4P+TSnS6P+TSnS8P+TSnS10P
TOTAL_LINSAT = TLS2P+TLS4P+TLS6P+TLS8P+TLS10P
TOTAL_POWER = TS2P+TS4P+TS6P+TS8P+TS10P
```

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