# Hybrid Multilevel Converters with Internal Cascaded/Paralleled Structures for MV Electric Aircraft Applications 

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# Hybrid Multilevel Converters with Internal Cascaded/Paralleled Structures for MV Electric 

 Aircraft ApplicationsA dissertation submitted in partial fulfillment
of the requirements for the degree of Doctor of Philosophy in Engineering with a concentration in Electrical Engineering
by

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#### Abstract

Using on-board medium voltage (MV) dc distribution system has been a megatrend for nextgeneration electric aircraft systems due to its ability to enable a significant system mass reduction. In addition, it makes electric propulsion more feasible using MV power electronic converters. To develop high-performance high-density MV power converters, the emerging silicon carbide (SiC) devices are more attractive than their silicon $(\mathrm{Si})$ counterparts, since the fast switch frequency brought by the SiC can effectively reduce the volume and weight of the filter components and thus increase the converter power density. From the converter topology perspective, with the MV dc distribution, the state-of-the-art two-level converters are no longer suitable for next-generation electric aircraft system due to the excessive $\mathrm{dv} / \mathrm{dt}$ and high voltage stress across the power devices.

To address these issues while still maintaining cost-effectiveness, this work demonstrates a megawatt-scale MV seven-level (7-L) $\mathrm{Si} / \mathrm{SiC}$ hybrid converter prototype implemented by active-neutral-point-clamped (ANPC) converter and H-bridges which is called ANPC-H converter in this work, and a MV five-level (5-L) $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter prototype, which are hybrid multilevel converters with internal cascaded and paralleled structures, respectively. Using multilevel circuit topology, the voltage stress across the devices and converter output voltage $\mathrm{dv} / \mathrm{dt}$ are reduced. The tradeoff between the system cost and efficiency was addressed by the adoption of the $\mathrm{Si} / \mathrm{SiC}$ hybrid configuration with optimized modulation strategies. Comprehensive design and evaluation of the full-scale prototypes are elaborated, including the low-inductance busbar designs, power converter architecture optimization and system integration.


To control the 7-L Si/SiC hybrid ANPC-H converter prototype, a low computational burden space-vector-modulation (SVM) with common-mode voltage reduction feature is proposed to fully exploit the benefits of 7-L Si/SiC hybrid ANPC-H converter. To further reduce the converter losses
and simplify control algorithm, an active hybrid modulation is proposed in this work by applying low frequency modulation in Si cells and high frequency modulation in SiC cells, thus the control framework is simplified from the 7-L SVM to a three-level SVM. To control the 5-L Si/SiC hybrid ANPC converter prototype to overall loss minimization, the low frequency modulation and high frequency modulation are also adopted for Si cells and SiC cells respectively in $5-\mathrm{L} \mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter prototype. Compared to the SVM-based hybrid modulation in 7-L ANPC-H converter, the hybrid modulation for 5-L hybrid ANPC adopts a simpler carrier-phase-shifted pulse width modulation for its inner-paralleled high frequency SiC cells, which extensively suppresses harmonics caused by high frequency switching. With the proposed modulation strategies, extensive simulation and experimental results are provided to evaluate the performance of each power stage and the full converter assembly in both the steady-state operation and variable frequency operations of the demonstrated hybrid converters.
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## DEDICATION

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## LIST OF PUBLICATIONS

[1] F. Diao, Y. Li, Z. Wang, Y. Wu and Y. Zhao, "A Computational Efficient Space-Vector Modulation Scheme for A Hybrid Seven-Level Converter for Medium Voltage Grid-Tied Applications," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 1786-1790. Published.
[2] F. Diao, X. Du, Z. Ma, Y. Wu, F. Guo, Y. Li, Z. Zhao and Y. Zhao, "A Megawatt-Scale Si/SiC Hybrid Multilevel Inverter for Electric Aircraft Propulsion Applications," IEEE Journal of Emerging and Selected Topics in Power Electronics. Submitted and under review.
[3] F. Diao, Y. Li, X. Du and Y. Zhao, "An Active Hybrid Modulation Strategy for a Si/SiC Hybrid Multilevel Converter," IEEE Open Journal of Power Electronics, vol. 2, pp. 401413, 2021. Published.
[4] F. Diao, P. Lai, F. Guo, P. Sun, Y. Zhao and Z. Chen, "A Medium-Voltage Multilevel Hybrid Converter using 3.3 kV Silicon Carbide MOSFETs and Silicon IGBT Modules," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC). Submitted and accepted.

Chapter 2 of this dissertation is reused from the contents of [1] and [2] in list of publication.
Chapter 3 of this dissertation is reused from the contents of [3] in list of publication. Chapter 4 of this dissertation is reused from the contents of [4] in list of publication.

## CHAPTER 1

## INTRODUCTION AND THEORETICAL BACKGROUND

### 1.1 Background: The opportunity and challenge of electric aircraft

### 1.1.1 The demand of electrification in electric aircraft

Nowadays, climate change concerns have raised worldwide awareness, and more innovative solutions and technologies have been cultivated in transportation applications to satisfy emissions reduction requirements. According to International Air Transportation Association (IATA), aviation industry alone accounts for $3 \%$ of global total greenhouse gases emissions and is expected to grow by average of $4 \%-5 \%$ annually [1.1]. It is expected by the International Civil Aviation Organization (ICAO) that aviation would account for up to $25 \%$ of global carbon emissions by the year 2050 if no actions are taken to limit traditional fossil fuel consumption [1.2]. To lower the carbon footprint, achieve higher fuel efficiency and better flight experience, more-electric aircraft (MEA) and all-electric aircraft (AEA) technologies [1.3]-[1.6] have caught more and more attention in the aviation industry.

When entering the $21^{\text {st }}$ century, various manufacturers and research institutes worldwide have reached tremendous achievement in electric aircraft prototyping, validating, and commercializing, especially the short-term electric aircrafts for regional transportation. Table 1-1 lists some typical electric aircrafts demonstrated worldwide which have been reported to be validated by ground tests or flight tests in recent years. With continuous research and development effort devoted to breakthrough technology challenges, more electric aircrafts would be manufactured, demonstrated, and commercialized in near future and contribute to build promising green energy market to help protect environment.

Table 1-1 Electric aircraft demonstrated in recent years [1.3].

| Prototype name | Year \& Country | Remarks | Reference |
| :---: | :---: | :---: | :---: |
| Lange Antares 20E | 2003, <br> Germany | Equipped with a $42-\mathrm{kW}$ electric motor and SAFT VL 41M lithiumion batteries | [1.7] |
| Pipistrel Taurus Electro G4 | 2011, Slovenia | World's $1^{\text {st }} 4$-seat full electric and won NASA 2011 green flight challenge | [1.8] |
| Airbus E-Fan | 2014, <br> France | $1^{\text {st }}$ electric aircraft to cross the English Channel. Production cancelled in 2017 | [1.9] |
| Solar Impulse 2 | $2015$ <br> Switzerland | $1^{\text {st }}$ piloted aircraft to circumnavigate of the earth by solar power | [1.10] |
| Siemens Extra EA 330LE | $2017,$ <br> Germany | Top speed above $340 \mathrm{~km} / \mathrm{h}$, world's $1^{\text {st }}$ aerotow with an electric plane | [1.11] |
| Bye Aerospace eFlyer 2 | 2018, USA | With a Siemens SP70D motor powered by lithium-ion batteries | [1.12] |
| White Lightning | 2019, UK | A racing aircraft at flight speed of around $482 \mathrm{~km} / \mathrm{h}$ | [1.13] |
| Lilium | $2019,$ <br> Germany | 186 miles range, top speed of 300 km/h | [1.14] |
| Eviation Alice | 2020, Israel | $2 \times 260 \mathrm{~kW}$ electric motors equipped for propulsion | $\begin{aligned} & {[1.15]} \\ & {[1.16]} \end{aligned}$ |
| XTI TriFan 600 | 2020, USA | Vertical takeoff and landing, 750 miles range | $\begin{aligned} & {[1.17]} \\ & {[1.18]} \end{aligned}$ |
| Rolls Royce ACCEL | 2021, UK | Racing aircraft with world record all-electric flight of 345 mph | [1.19] |
| E-Fan X by Airbus and Rolls-Royce | $2021,$ <br> France/UK | One of the four jet engines replaced by a 2MW electric motor | [1.20] |
| NASA X-57 Maxwell | 2022, USA | NASA $1^{\text {st }}$ electric aircraft to validate distributed propulsion | [1.21] |
| Ampaire Tailwind | 2022, USA | Targeting regional air travel of less than 350 miles | $\begin{aligned} & {[1.22]} \\ & {[1.23]} \end{aligned}$ |

### 1.1.2 The medium voltage trends for electric aircraft

Stepping from the traditional fossil fuel-oriented propulsion system towards the electrical counterpart is still a challenging task since it could involve tremendous modifications to the system architecture and re-designs of the airborne electric power generation, storage, distribution, and
conversion [1.24]. In commercial airliners, the low voltage distribution is a mature candidate at the present time. For instance, the Boeing 787 with approximately 1 MW onboard electric power generation capability adopts $115-235 \mathrm{VAC}, \pm 270 \mathrm{VDC}$ to distribute power for auxiliary onboard electrical power systems, such as HVAC, actuators, avionics, air conditioner and de-icing [1.4], [1.5]. Due to the use of low voltage distribution for such a large amount of power, the high amount of current is inevitable results in more copper for wiring cores, connectors, and resultant power losses, thereby increasing the weight of the aircraft and degrading the overall efficiency.

In contrast, the use of medium-voltage (MV) dc distribution is a long-term solution for the next-generation electric aircraft, which can leverage lightweight and high efficiency for new aircraft design. According to investigation conducted by Advance Research Project Agency Energy (ARPA-E), Figure 1-1 shows that increasing voltage could effectively reduce the conducting core $(\mathrm{Cu})$ wiring weight and increase gravimetric power density, based on estimation assumptions of $8 \times 45 \mathrm{~m}$ cables copper wires on a notional Boeing 787 aircraft with two generators. As shown in Figure 1-1, when dc voltage distribution adopts 540 V, copper wiring weight is estimated approximately more than $1 \times 10^{5} \mathrm{~kg}$, which is almost half of the maximum takeoff weight allowance of Boring 787. In comparison, when dc voltage increases to 2 kV , copper wiring weight is estimated approximately as $3 \times 10^{4} \mathrm{~kg}$, which is reduced to only one-third of 540 V case. Also, MV scale of dc voltage distribution allows the conducting current lowering at the same power level, in turns, conduction loss can be tremendously reduced in both copper wires and power electronics circuit and devices. Thus, power management and driving system on-board could have less weight and high-power density under MV dc distribution, which contributes to substantial improvement for lightweight, reduced volume and fuel-saving of electric aircraft.


Figure 1-1 Voltage versus copper wiring weight (no insulation) and power density investigated by ARPA-E.

Recently, the MV dc voltage distribution for electric aircraft applications has been demonstrated and validated by manufacturers and research institutes. Specifically, a 3 kV MV dc distribution was selected for Airbus's E-Fan X and was tested in 2021 [1.20], whose one of the four jet engines was replaced by a 2 MW electric fan powered by a 2.5 MW Rolls-Royce AE 2100 Engine. In 2030, NASA will launch a new design with 1 kV MV dc distribution, named STARCABL, in which an electric-propulsion motor is installed at the rear of the aircraft. By 2050, N3-X turbo-electric aircraft with the cutting-edge superconducting technologies, also developed by NASA, will be equipped with $\pm 2 \mathrm{kV}$ dc distribution system. Therefore, the evolutions of the onboard MV dc electric power system are expected to gain momentum in the development of future aircraft and bring foreseeable advancements for transportation electrifications.

### 1.2 Background: Two-level and three-level converter for electric aircraft propulsion

### 1.2.1 Opportunity and challenges of conventional two-level VSC applications

Power electronics circuit provides the essential linkage to enable power conversion between dc voltage distribution and ac propulsion of electric aircraft. It also provides the ability for aircraft


Figure 1-2 Topology of conventional two-level converter.
flight control system to control voltage, current, and/or frequency of electrical energy of electric machine, hence, the on-board fans' speed and/or torque could be controlled to regulate aircraft flight status. The electric aircraft state-of-the-art on-board power electronics circuit is implemented by power converters with semiconductors and passive components. The most basic topology configuration of power converter used for electric aircraft propulsion is the conventional two-level converter circuit [1.8], [1.25] shown as Figure 1-2. Its circuit consists of a dc bus capacitor and six semiconductor switch positions. In application, the conventional converter transforms dc power to three-phase ac power to drive ac motor machine, and each ac phase exists two voltage level outputs. With simple structure, low construction and maintenance cost, and high reliability, the conventional converter has been widely applied in various industrial applications.

The semiconductor switch positions in this topology could be implemented by silicon $(\mathrm{Si})$ insulated-gate-bipolar-transistors (IGBT), which have been mature technology for years of development. Nowadays, wide-bandgap (WBG) devices especially silicon carbide (SiC) metal-oxide-semiconductor-field-effect-transistors (MOSFET) have attracted much attention for constructing power electronics converters to improve system-level benefits. Compared to Si IGBTs, SiC MOSFETs have the faster switching speed, lower loss, and high temperature tolerance, which could allow converter operates with the higher switching frequency to lower filtering circuit
requirements and avoid heavy passive filtering components. Hence, on-board power electronics could be more weightless and power-dense by the careful system integration with SiC technology [1.25].

By adopting SiC technology, the conventional two-level converter is the best practice for power conversion with low de voltage distribution, however, it may lose its advantage and compatibility under MV dc voltage distribution. Because the marketplace still lacks commercial affordable SiC MOSFETs which can withstand MV voltages, such as $3.3 \mathrm{kV}, 6.5 \mathrm{kV}$, and 10 kV . Also, even if by adopting expensive high withstand-voltage SiC devices, it requires the careful filtering circuit design to relieve electromagnetic interference (EMI) issue caused by high dv/dt and/or di/dt generated by SiC devices when switching fast with MV dc bus.

### 1.2.2 Opportunity and challenges of state-of-the-art three-level VSC applications

To make it compatible with the MV dc bus and increase system efficiency and power density while still retaining cost-effectiveness, the MV inverters should be comprehensively investigated for the high power-density electric propulsion systems in the MEA or AEA. Compared with the conventional two-level counterpart, the multilevel power converters [1.26], [1.27] have lower harmonics in the ac output voltage, lower device voltage stress, dv/dt, EMI emissions and the potential to reduce the common-mode voltage (CMV) [1.28], [1.29] which causes motor shaft current and put bearing insulation at risk, thereby threatening electric motor lifetime.

In the light of these advantages, three-level (3-L) topologies have already been demonstrated for aerospace applications, such as T-type [1.30], [1.31] converters, neutral point clamped (NPC) [1.32]-[1.34] converters, and active neutral point clamped (ANPC) converters [1.35]-[1.37]. Among the 3-L converters for propulsion applications in literatures, dc bus voltage was up to 2.4
kV [1.35]-[1.37] with improved converter power density and efficiency. Although the power converter performance is improved, system cost could be high especially if all switch positions adopt all-SiC MOSFETs.

Recently, the hybrid $\mathrm{Si} / \mathrm{SiC}$ converter design has become a popular topic, which enables flexible adoption of the off-the-shelf Si and SiC switches to further improve cost-effectiveness and performance. For instance, the $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converters are reported in [1.38] and [1.39], where each ANPC phase leg consists of two SiC switches and four Si switches, such that the converter cost can be much lower than that of an all-SiC ANPC converter. In addition, modulation methods using specific redundant switching states are presented in [1.38] and [1.39] to properly assign the switching actions among Si and SiC devices to achieve high efficiency. Similarly, an ANPC converter using four SiC switches and two Si switches per phase leg is reported in [1.36] and [1.40]. A $\mathrm{Si} / \mathrm{SiC}$ hybrid T-type converter is reported in [1.41], where the efficiency improvement and the thermal stress reduction are highlighted. A 1-MW 3-L ANPC in a novel twostage structure is proposed in [1.42], which uses Si IGBTs at high-voltage (HV) stage and SiC MOSFETs at LV stage, such that the converter can achieve both low cost and low power losses. Compared with literature [1.42] using Si IGBTs in the high-voltage stage, authors in [1.43] use Si diodes in the high-voltage stage and SiC MOSFETs in the LV stage of the 3-L converter, such that the overall cost is lower. A hybrid modulation method combining a 3-L space vector modulation (SVM) and a phase-shifted pulse width modulation (PS-PWM) [1.44] is proposed in [1.45] for a modified ANPC converter, where the four high voltage power devices operate at fundamental frequency, while the other LV power devices operate at high switching frequency. In [1.46], a single-phase $\mathrm{Si} / \mathrm{SiC}$ hybrid converter with auxiliary half-bridges is proposed to benefit costeffectiveness for NPC converter, where a specific modulation method is proposed to switch the
two SiC devices at high frequency and operate the other six Si devices at fundamental frequency. As can be seen from the above literature review, to fully exploit the benefits of the hybrid $\mathrm{Si} / \mathrm{SiC}$ hybrid multilevel converter, sophisticated modulation strategies still need to be developed accordingly.

### 1.3 Background: Hybrid multilevel converters with internal cascaded/parallel structures

Compared to conventional 2-L converter, 3-L converter provides more compatibility for MV applications with the lower voltage stress for switch positions and lower $\mathrm{dv} / \mathrm{dt}$. There is still room to further lower $\mathrm{dv} / \mathrm{dt}$ and relieve EMI issue from operating with higher dc bus voltage, otherwise additional dv/dt filter and/or EMI filter should be still required. For instance, the megawatt-scale 3-L converter design in [1.36], [1.37] still require the carefully filtering design for system noise immunity and performance. To address these issues, the hybrid topologies with internal cascaded and parallel structure which could generate five-level (5-L) [1.47], [1.48] and seven-level (7-L) [1.49]-[1.52] become a trend [1.53]. Note that multilevel converters with more output voltage levels could provide more possibilities for lowering dv/dt, however, their cost-effectiveness, ease-of-implementation, and reliability might be weakened.

### 1.3.1 Hybrid multilevel converter with internal cascaded structure

The hybrid multilevel converter with internal cascaded structure is implemented by cascading the 3-L converter with floating H-bridges [1.51], [1.52], [1.54]-[1.66], such as 7-L T ${ }^{2}$-H converter, i.e., T-type converter cascaded with H-bridges [1.51], [1.58], [1.59] and 7-L ANPC-H converter, i.e., ANPC converter with cascaded H-bridges [1.52], [1.54]-[1.57], [1.60]-[1.66]. Among them, 7-L ANPC-H converter has the advantage of lower voltage stress across power devices and
capability of balancing loss distributions among power switches, which is promising among state-of-the-art 7-L converter topologies.

Control and modulation strategies are significant to cultivate advanced performance of 7-L ANPC-H converter. For instance, in [1.51] and [1.58], authors reported the space-vector modulation and a computational efficient space-vector modulation respectively for general 7-L converters, which can also be used as modulation for 7-L ANPC-H converter. In [1.52], an active hybrid modulation is proposed for 7-L ANPC-H converter with $\mathrm{Si} / \mathrm{SiC}$ hybrid configuration, where high frequency modulation is used for Si cells and low frequency is used for SiC cells. By the hybrid $\mathrm{Si} / \mathrm{SiC}$ configuration and hybrid modulation, the converter overall losses are optimized. In [1.56], [1.60], [1.62], [1.65], [1.66] the model predictive control with multiple improvement objectives considered are proposed and reported for 7-L ANPC-H converter, where in [1.66] switching positions are also operated with high frequency and low frequency switching actions for overall losses optimization.

### 1.3.2 Hybrid multilevel converter with internal parallel structure

To achieve 5-L or 7-L output voltage, the hybrid multilevel converter with internal parallel structure is implemented by doubling or tripling certain internal structures of ANPC converter and configuring by interleaving structures. With the internal parallel structure, the implemented multilevel converter can have lower current stress for devices and enhanced modularity. Also, internal parallel structure configurations are promising for converters to attain higher equivalent switching frequency and higher system power efficiency.

For instance, multiple ANPC modular building blocks are interleaved as one phase-leg for megawatt power conversion application reported in [1.67], such that the overall application
equivalent switching frequency is up to 1 MHz and harmonics is moved to high frequency region for easy filtering circuit design. Also, the parallel structure effectively reduces current stress for each ANPC building block which could be constructed by low-current power devices with lower cost, and overall application power efficiency is improved due to less current stress per power switches. Paralleling multiple ANPC building blocks is straightforward and easy-ofimplementation to fulfill high-power, high-frequency, and high-power efficiency applications. However, it requires excessive power switches and might not be the most cost-effective solution.

Recently, the configuration by only paralleling certain inner circuits within one ANPC has attracted much attention because it requires less power switches than paralleling the entire ANPC building blocks. With the inner hybrid configuration, both superior power performance existing in [1.67] and cost-effectiveness could be guaranteed. In [1.68], the multilevel converter with internal parallel structure concept is summarized, where several paralleled-connected modules are with high switching frequency and the remaining part is with low switching frequency. With this inner interleaved structure, the hybrid converter has increased the number of voltage levels and avoid using excessive power switches which could contribute to cost-effective and reliability. In [1.69] and [1.70], a multilevel internal parallel converter is implemented based on modification of ANPC, and functionality is also validated by its proposed control strategies. In [1.70], a nine-level innerinterleaved hybrid multilevel converter is reported and invalidated by experiments with model predictive control, where paralleled parts are with high frequency and the remaining is with low frequency.

The internal parallel structure is effective to achieve flexibility and modularity, however, circulating current due to inevitable circuit parameter mismatch, common-mode voltage and common-mode current could be issues existing in multi-paralleled converter configuration.

According to literature, these issues could be mitigated or limited by dedicated modulation and control strategies. For example, a centralized carrier-based model predictive control is proposed in [1.71] to eliminate circulating current in the interleaving converters configuration. In [1.72], an interleaved carrier phase-shift pulse width modulation is proposed to reduce circulating current and is general for arbitrary number of interleaved converters. In [1.73], common-mode voltage of interleaved voltage source converters is comprehensively studied and investigated under different modulation strategies. A multilevel space-vector-modulation is proposed in [1.74] for the parallel converter configuration to suppress the circulating current, common-mode voltage, and commonmode current.

### 1.4 Outline

Chapter 2 describes a MW-scale 7-L hybrid ANPC-H converter prototype, which consists of a Si IGBT based ANPC and SiC H-bridges substages with internal cascaded structure, is developed with a feasibility demonstration for MV aerospace motor drive applications. The conventional space-vector-modulation and a proposed computational efficient space-vector-modulation are both illustrated and validated by simulations and experiments conducted on the MW-scale 7-L hybrid ANPC-H converter prototype.

Chapter 3 introduces an active hybrid modulation for the 7-L hybrid ANPC-H converter prototype to further optimize switching actions distributed among switch positions and improve converter power efficiency. In this chapter, the principle, stability, implementation will be illustrated and discussed. Also, both simulation and experimental results are provided to validate the proposed active hybrid modulation method in terms of power conversion performance, converter power loss and efficiency.

Chapter 4 introduces the design and implementation of a hybrid 5-L MV ANPC converter with inner-interleaved configuration using the commercial 3.3 kV Si IGBT half-bridge modules and the custom designed 3.3 kV SiC MOSFETs H-bridge modules. With interleaved configuration and low/high switching frequency allocated among $\mathrm{Si} / \mathrm{SiC}$ devices, the implemented hybrid multilevel converter could be very efficient while achieving 100 kHz equivalent switching frequency in the output voltage. In this chapter, both simulation and experimental results conducted on the MV prototype are given to validate this converter solution for electric aircraft applications.

Chapter 5 conducts a comparison study of the two multilevel converter prototyping solutions, i.e., multilevel converters with internal cascaded structure and with internal parallel structure. The comparison study focuses on circuitry equivalence, prototyping implementation, estimated cost, power conversion performance, dc voltage source utilization, floating capacitor balancing region, common mode voltage, and converter power efficiency.

Chapter 6 concludes the dissertation and discusses future work to improve design, modeling, validating.

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## CHAPTER 2

## MULTILEVEL CONVERTER WITH INTERNAL CASCADED STRUCTURE

### 2.1 Topology and the implemented prototype

### 2.1.1 Basic topology configuration

Figure 2-1 shows the circuit configuration of the 7-L ANPC-H converter, which consists of two cascaded power stages, i.e., three-level (3-L) ANPC stage and H-bridge stage. Table 2-1 lists the overall parameter specification. Assuming the ANPC has a balanced dc link with a total dc link voltage as $U_{d c}$, the voltage across the two series connected capacitors $C_{d c 1}$ and $C_{d c 2}$, which are also called floating capacitors, are both $U_{d c} / 2$.

The ANPC phase-leg can generate three voltage levels, i.e., $-U_{d c} / 2,0$ and $U_{d c} / 2$, with respect to the neutral point $O$. In each H -bridge converter, the dc voltage across its floating capacitor is regulated as $U_{d c} / 4$, which leads to three possible output voltage levels for the H -bridge converter, i.e., $-U_{d c} / 4,0, U_{d c} / 4$. Due to the cascaded structure, there are 7 possible output voltage levels,


Figure 2-1 Topology of the 7-L ANPC-H converter.
which are corresponding to 7 switching states, at the ac output terminal of each phase-leg in the hybrid 7-L converter. The switching states of phase A, B and C are defined as $S_{A}, S_{B}, S_{C}=0,1, \ldots$, 6, and the corresponding output line to neutral, i.e., $V_{A O}$, voltage levels are $-3 U_{d c} / 4,-U_{d c} / 2,-U_{d c} / 4$, $0, U_{d c} / 4, U_{d c} / 2,3 U_{d c} / 4$, respectively.

### 2.1.2 A 1-MVA 7-L ANPC-H converter prototype

### 2.1.2.1 Prototyping implementation

To fully investigate and study of the 7-L ANPC-H converter, a full-scale 1-MVA 7-L ANPC-H converter prototype built as shown in


Figure 2-2. The prototype is installed within a custom 4-ft tall rack, where 3-phase MV ANPC stage is mounted on the top and three single-phase H-bridge PEBBs are placed on the bottom. The prototype is fed with a 3 kV input dc power supply and can generate up to 3.18 kV rms line-toline ac voltage. To achieve sufficient insulation strength for the prototype, fiberglass boards are placed between the phase legs of the 7-L ANPC-H converter. The


Figure 2-2 1-MV 7-L ANPC-H converter prototype.


Figure 2-3 The 3-D view of the designed 3-L 3-phase MV ANPC stage.

1-MVA prototype is implemented by power electronics building block (PEBB) concept due to its modularity, cost effective and fast prototyping merits.

Figure 2-3 shows the 3-D picture of the designed 3-L 3-phase MV ANPC stage. On dc link of ANPC stage, twelve $1.5 \mathrm{kV} 195 \mu \mathrm{~F}$ film capacitors DCP6S06195E000 from WIMA are adopted to form the dc link capacitor bank. The total capacitance for $C_{d c 1}$ and $C_{d c 1}$ are both $293 \mu \mathrm{~F}$ and each capacitor withstand 750 V at rated condition for the proposed hybrid 7-L converter. By adopting multilayer laminated layout, busbars with low parasitic inductance are designed to form linkage between dc link and power modules.

In this work, the 3-phase MV ANPC stage is assembled by three single-phase MV ANPC PEBBs. There are three ANPC PEBBs investigated and prototyped in this work, which are: all-Si switch positions shown in Figure 2-4 (a), all-SiC switch positions shown in Figure 2-4 (b), and hybrid "Si+SiC" switch positions shown in Figure 2-4 (c). In the hybrid PEBB, switch positions $\mathrm{S}_{5}$ and $\mathrm{S}_{6}$ are implemented by SiC MOSFETs, the other switch positions are Si IGBTs. The Si switch positions are implemented by Infineon 3.3 kV half bridge IGBT modules in XHP-3 package,


Figure 2-4 Three implemented single-phase ANPC PEBBs.
and SiC switch positions are implemented by Cree XHV-7 3.3 kV half bridge SiC MOSFET modules. The adopted 3.3 kV Si and SiC modules have the same power terminal dimensions, which provides ease-of-prototyping with strong modularity. In the prototypes, customized dual-
channel gate drivers with under/over voltage lockout, reverse polarity, and overcurrent lockout protection are designed and installed for half-bridge IGBT and MOSFET modules.

The single-phase H-bridge PEBB design is summarized in [2.1]. In each single-phase H-bridge


Figure 2-2, two $1.5 \mathrm{kV} 195 \mu \mathrm{~F}$ film capacitors DCP6S06195E000 from WIMA are used as dc capacitors. The SiC power modules in H-bridge PEBB are the 1.7 kV half-bridge HT-3234-R-VB from Wolfspeed with 7 nH stray inductance and 681 A continuous drain current capability at $25^{\circ} \mathrm{C}$. The commercial off-the-shelf dual-channel differential gate driver boards are used to drive the SiC modules. The gate driver has roughly the same footprint as the power module and has all the essential protections such as under/over voltage lockout, reverse polarity, and overcurrent lockout protection with indicator. Similar with ANPC stage, H-bridge PEBB adopts the planar laminated busbar to form linkage between dc link and SiC power modules. The fan/forced cooled heatsink LA7/100 12 V with $0.1 \mathrm{C} / \mathrm{W}$ thermal resistance from Fischer Elektronik is used for power module cooling.

Table 2-1 7-L ANPC-H converter parameter specification.

| Parameter | Description |
| :---: | :---: |
| dc link voltage | 3 kV |
| H-bridge capacitor voltage | 750 V |
| 3.3 kV IGBT Module | FF450R33T3E3 |
| 3.3 kV SiC MOSFET Module | Cree 3.3kV XHV-7 |
| 1.2 kV SiC MOSFET Module | CAS325M12HM2 |
| Voltage stress of switches in ANPC | 1.5 kV |
| Voltage stress of switches in HB | 750 V |
| Rated designed power | 1 MVA |
| Operating fundamental frequency | Up to 1 kHz |
| Switching frequency | 20 kHz |
| ANPC floating capacitor | $293 \mu \mathrm{~F}$ |

Based on the above-mentioned design illustrations, some typical parameters specification of the implemented 7-L ANPC-H converter prototype is summarized as Table 2-1.

### 2.1.2.2 Submodules experimental testing

The 3-L 3-phase MV ANPC stage was tested as a three-phase inverter with 3 kV dc link voltage and 2 kHz switching frequency to generate a voltage with 60 Hz fundamental frequency. The SPWM with modulation index 0.61 was adopted and converter ac terminals were connected to the


Figure 2-5 ANPC output line voltage at 60 Hz fundamental frequency.

Y-connection load. The load for each phase consists of a series-connected 10 mH inductor and 106 $\mu \mathrm{F}$ capacitor, whose equivalent impedance is $21.25 \Omega$ at 60 Hz . Figure $2-5$ shows the experimental waveforms of ANPC output line voltages and phase currents.

The power testing experimental result of the single-phase H -bridge PEBB was included in [2.1], so it is not respectively illustrated here.

### 2.2 Conventional SVM

SVM strategy is commonly adopted for three-phase converter modulation especially ac propulsion applications. In this subsection, the principle, implementation, and challenges of SVM for multilevel converters are illustrated based on the presented 7-L ANPC-H converter in this work.

### 2.2.1 $\quad$ Switching states definition

The conduction paths of the 7-L ANPC-H converter under all the switching states are shown in Figure 2-6. As shown in Figure 2-6 (a), there is only one conduction path for switching state 6, where phase current flows through the $C_{F C}$, such that $C_{F C}$ is in charging or discharging state, depending on the phase current polarity. And there is no current flowing out from the middle point $M$, so that the voltage across the two dc-bus floating capacitors does not change during this switching state. There is also only one conduction path for the switching state 0 shown in Figure 2-6 (g). In this case, the voltage across the two dc-bus floating capacitors does not change and $C_{F C}$ is in charging or discharging state. Similarly, conduction paths of the other five switching states are shown in Figure 2-6 (c) to (f). In contrast to the switching states 0 and 6, there are redundant conduction paths for each of the switching states 1 to 5 . The redundant conduction paths with different charging or discharging effects to dc floating capacitors provide flexibility for the dc floating capacitors voltage balancing.


Figure 2-6 Conduction paths of a hybrid 7-L ANPC-H converter bridge-leg with output voltage levels: (a) voltage level 6; (b) voltage level 5; (c) voltage level 4; (d) voltage level 3; (e) voltage level $2 ;(\mathrm{f})$ voltage level $1 ;(\mathrm{g})$ voltage level 0 .

The gate signals and the dc floating capacitors charge/discharge state of the 7-L ANPC-H converter, using phase A as an example, during all the switching states with different phase current polarities are summarized in Table 2-2, where " + " stands for the instantaneous ac current flows out from phase-leg to the load, and vice versa; " $\uparrow ", " \downarrow "$, and "*" stand for the floating capacitor charging, discharging and bypass, respectively. There are 16 conduction paths, i.e., $i-x v i$, for the seven switching states, where switching states 1 to 5 have redundant conduction paths.

### 2.2.2 Space-vector diagram of 7-L converter

For the hybrid 7-L converter, $\left[S_{A}, S_{B}, S_{C}\right]$ is defined as the switching state of the converter. $S_{A}$, $S_{B}$, and $S_{C}$ represent the switching states of phase A, B, and C, respectively, where, $S_{A}, S_{B}, S_{C}=0$,

Table 2-2 7-L ANPC-H converter parameter specification.

| Path | State | $\boldsymbol{u}_{\boldsymbol{a}}$ | $\boldsymbol{i}_{a}$ | $\boldsymbol{u}_{\text {FC }}$ | $\boldsymbol{u}_{\boldsymbol{d} \boldsymbol{c} 1}$ | $u_{d c 2}$ | $\begin{gathered} S_{1} S_{3} S_{5} S_{7} S_{9} \\ \left(\bar{S}_{2} \bar{S}_{4} \bar{S}_{6} \bar{S}_{8} \bar{S}_{10}\right) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| i | 6 | $3 U_{d c} / 4$ | + | $\downarrow$ | * | * | 11101 |
|  |  |  | - | $\uparrow$ | * | * |  |
| ii | 5 | $U_{\text {dc }} / 2$ | + | * | * | * | 11111 |
|  |  |  | - | * | * | * |  |
| iii | 5 | $U_{d c} / 2$ | + | * | * | * | 11100 |
|  |  |  | - | * | * | * |  |
| iv | 4 | $U_{\text {dc }} / 4$ | + | $\uparrow$ | * | * | 11110 |
|  |  |  | - | $\downarrow$ | * | * |  |
| v | 4 | $U_{d c} / 4$ | + | $\downarrow$ | $\uparrow$ | $\downarrow$ | 00101 |
|  |  |  | - | $\uparrow$ | $\downarrow$ | $\uparrow$ |  |
| vi | 4 | $U_{d c} / 4$ | + | $\downarrow$ | $\uparrow$ | $\downarrow$ | 11001 |
|  |  |  | - | $\uparrow$ | $\downarrow$ | $\uparrow$ |  |
| vii | 3 | 0 | + | * | $\uparrow$ | $\downarrow$ | 00111 |
|  |  |  | - | * | $\downarrow$ | $\uparrow$ |  |
| viii | 3 | 0 | + | * | $\uparrow$ | $\downarrow$ | 11011 |
|  |  |  | - | * | $\downarrow$ | $\uparrow$ |  |
| ix | 3 | 0 | + | * | $\uparrow$ | $\downarrow$ | 00100 |
|  |  |  | - | * | $\downarrow$ | $\uparrow$ |  |
| x | 3 | 0 | + | * | $\uparrow$ | $\downarrow$ | 11000 |
|  |  |  | - | * | $\downarrow$ | $\uparrow$ |  |
| xi | 2 | $-U_{d c} / 4$ | + | $\uparrow$ | $\uparrow$ | $\downarrow$ | 00110 |
|  |  |  | - | $\downarrow$ | $\downarrow$ | $\uparrow$ |  |
| xii | 2 | $-U_{d c} / 4$ | + | $\uparrow$ | $\uparrow$ | $\downarrow$ | 11010 |
|  |  |  | - | $\downarrow$ | $\downarrow$ | $\uparrow$ |  |
| xiii | 2 | $-U_{d c} / 4$ | + | $\downarrow$ | * | * | 00001 |
|  |  |  | - | $\uparrow$ | * | * |  |
| xiv | 1 | $-U_{d c} / 2$ | + | * | * | * | 00000 |
|  |  |  | - | * | * | * |  |
| xV | 1 | $-U_{d c} / 2$ | + | * | * | * | 00011 |
|  |  |  | - | * | * | * |  |
| xvi | 0 | $-3 U_{d c} / 4$ | + | $\uparrow$ | * | * | 00010 |

$1, \ldots, 6$. When a switching state of the converter is selected, the output voltage vector of the converter can be calculated as

$$
\begin{equation*}
V_{\text {out }}=\left(S_{A}+S_{B} e^{j \frac{2}{3} \pi}+S_{C} e^{j \frac{4}{3} \pi}\right) U_{d c} \tag{2-1}
\end{equation*}
$$

The space-vector (SV) diagram [2.2] of the 7-L converter in sector 1 is shown in Figure 2-7, including all the output voltage vectors and corresponding switching states of the converter. The numbers at each vertex represent the switching states of the converter. For instance, $[6,4,2]$ at the vertex $P_{1}$ represents a switching state of the converter, i.e., $S_{A}=6, S_{B}=4$, and $S_{C}=2$. It should be noted that multiple switching states, also called redundant switching states, can generate the same output voltage vector. For instance, $[6,4,2],[5,3,1]$ and $[4,2,0]$ are the redundant switching states of the output vector at the vertex $P_{1}$.

In Figure 2-7, $\boldsymbol{V}_{1}, \boldsymbol{V}_{2}$ and $\boldsymbol{V}_{3}$, enclosing a reference vector $\boldsymbol{V}_{\text {ref }}$ at vertexes $P_{1}, P_{2}$ and $P_{3}$, respectively, are the nearest three vectors. The triangle with the three vertexes $P_{1}, P_{2}$, and $P_{3}$ is defined as a modulation triangle. The basic concept of SVM is to use the nearest three vectors to synthesize the reference vector as

$$
\begin{equation*}
\boldsymbol{V}_{\text {ref }} T_{s}=\boldsymbol{V}_{1} d_{1} T_{s}+\boldsymbol{V}_{2} d_{2} T_{s}+\boldsymbol{V}_{3} d_{3} T_{s} \tag{2-2}
\end{equation*}
$$



Figure 2-7 Space-vector diagram of a 7-L converter in sector 1 .

Where $T_{s}$ is the switching (sampling) period of the SVM scheme; $d_{1}, d_{2}$, and $d_{3}$, are the duty cycles of the nearest three vectors $V_{1}, V_{2}$ and $V_{3}$, respectively.

In the proposed SVM, the modulation triangle enclosing the reference vector is firstly determined, and the duty cycles of the nearest three vectors are calculated. Then, the switching sequence is formed to synthesize the reference vector.

### 2.2.3 Implementation workflow and complexity challenge

The implementation workflow [2.2] of multilevel SVM strategy is summarized as: step1: determine modulation triangle, step2: calculate vectors duration and generate switching sequence, step3: determine and execute switching sequence based on certain objectives such as floating capacitor balancing.

In the workflow, step1 is implemented based on calculations mentioned in previous subsection. In step2, duration of vectors in all modulation triangles are calculated and stored in lookup tables based on reference vector location within the space-vector diagram. A typical duration of vectors lookup table for some portion of space-vector diagram is given in [2.2]. Also, there are multiple switching sequences that could be formed by the redundant switching states within one modulation triangle. Then, step3 is to select a certain switching sequence and execute it with corresponding vectors duration time. The multiple switching sequences provide flexibility to achieve some control objectives, such as floating capacitor balancing, circulating current reduction, and common-mode voltage reduction.

As can be seen from [2.2], the conventional SVM for multilevel converter requires excessive vectors duration and switching sequences calculation and requires lookup tables embedded in controller to providing those vector duration and switching sequences for execution. Thus, the
conventional multilevel SVM is complex for both design and digital implementation, requiring large memory from controllers. The case is even worse for multilevel converters with higher numbers of voltage level output.

### 2.3 Computational efficient SVM

The conventional SVM applied for multilevel converter is complex and requires lookup tables. To lower design complexity and computational burden, a computational efficient SVM is proposed, and its detailed workflow is illustrated in this section for the 7-L ANPC-H converter prototype established in this work.

### 2.3.1 Determine modulation triangle

According to Figure 2-7, the reference vector locates in one of the modulation triangles in the SV diagram. Assume the reference voltage vector $V_{\text {ref }}$ has a phase angle $\theta$, i.e., the angle between $V_{\text {ref }}$ and A-axis. For instance, $V_{\text {ref }}$ is located in Sector 1, if the angle meets the following requirement.

$$
\begin{equation*}
0 \leq \theta \leq \frac{\pi}{3} \tag{2-3}
\end{equation*}
$$

As an illustrative example, the SV diagram of Sector 1 in a $120^{\circ}$ coordinate frame, which is also called the $x-y$ coordinate frame in this paper, is shown in Figure 2-8. In the $x-y$ coordinate frame, $x$-axis is aligned with phase A , while $y$-axis is aligned with phase B . The coordinate of the original vertex $\boldsymbol{O}$ is defined as $(0,0)$, and the length of the edges of each switching triangle is normalized to be 1 . Based on this assumption, the coordinates of all the vertices in the $x-y$ coordinate frame are shown in Figure 2-8 (a). Since edges of the modulation triangles are all in parallel with either the $x$ - or $y$-axis, the coordinates are all integers in this $x-y$ coordinate frame.


Figure 2-8 The SV diagram of Sector 1 in $120^{\circ}$ coordinate frame: (a) coordinates of each output voltage vector; (b) type I modulation triangle; and (c) type II modulation triangle.

The parallelogram selected in Figure 2-8 (a) is defined as a modulation parallelogram, which is composed of two adjacent modulation triangles, i.e., type I and type II modulation triangles, as shown in Figure 2-8 (b) and (c), respectively. As shown in Figure 2-8 (a), there are two vertices, i.e., $(4,2)$ and $(5,3)$, located at the tips of the edge shared by both modulation triangles in the selected parallelogram, where the vertex with the smaller coordinate is defined as the original vertex of the modulation parallelogram, e.g., $(4,2)$ in the selected parallelogram. The corresponding voltage vector at the original vertex is called the original vector. Suppose the coordinates of the original vertex is $\left(L_{1}, L_{2}\right)$, then coordinates of the other two vertices in type I modulation triangle are $\left(L_{1}+1, L_{2}\right)$ and $\left(L_{1}+1, L_{2}+1\right)$, while the coordinates of the other two vertices in type II modulation triangle are $\left(L_{1}, L_{2}+1\right)$ and $\left(L_{1}+1, L_{2}+1\right)$, as shown in Figure 2-8 (b) and (c), respectively. The original vertex $\left(L_{1}, L_{2}\right)$ and vertex $\left(L_{1}+1, L_{2}+1\right)$ are the two common vertices
shared by the two modulation triangles. For any reference vector in this modulation parallelogram, suppose the coordinate of the reference vector is $(x, y)$, which should meet the relationship:

$$
\begin{align*}
& L_{1}=\operatorname{int}(x)  \tag{2-4}\\
& L_{2}=\operatorname{int}(y) \tag{2-5}
\end{align*}
$$

where $\operatorname{int}()$ is a rounding-down function to the nearest rounding-down integer; $L_{1}$ and $L_{2}$ are the $x$ and $y$-axis coordinates of the original vertex, respectively. If the coordinates of reference vector and original vertex meet the relationship in Eq. (2-6), the reference vector located in a type I modulation triangle. Otherwise, the reference vector is located in a type II modulation triangle.

$$
\begin{equation*}
\bmod \left(x, L_{1}\right) \geq \bmod \left(y, L_{2}\right) \tag{2-6}
\end{equation*}
$$

where $\bmod (m, n)$ is the function to calculate the remainder of the $m$ divided by $n$. For instance, if the coordinate of a reference voltage vector is (4.8, 1.5), i.e., $x=4.8, y=1.5$, then $L_{1}=4, L_{2}=1$, it locates in the type I modulation triangle.

As shown in Figure 2-8 (b), there are nearest three vectors in the type I modulation triangle, i.e., $\boldsymbol{V}_{1}, \boldsymbol{V}_{2}$ and $\boldsymbol{V}_{3}$. According to the volt-second balancing principle given in Eq. (2-2), for a generic reference voltage vector $(x, y)$, following relationship can be derived.

$$
\begin{gather*}
x=L_{1} d_{1}+\left(L_{1}+1\right) d_{2}+\left(L_{1}+1\right) d_{3}  \tag{2-7}\\
y=L_{2} d_{1}+L_{2} d_{2}+\left(L_{2}+1\right) d_{3} \tag{2-8}
\end{gather*}
$$

where $d_{1}, d_{2}$ and $d_{3}$ are the duty cycles of $\boldsymbol{V}_{1}, \boldsymbol{V}_{2}$ and $\boldsymbol{V}_{3}$, respectively. Also, the duty cycles of the nearest three vectors should meet the requirement in Eq. (2-9).

$$
\begin{equation*}
d_{1}+d_{2}+d_{3}=1 \tag{2-9}
\end{equation*}
$$

Then, the duty cycles of the nearest three vectors are calculated as Eq. (2-10) - Eq. (2-12).

$$
\begin{gather*}
d_{1}=1-x+L_{1}  \tag{2-10}\\
d_{2}=x-y+L_{2}-L_{1}  \tag{2-11}\\
d_{3}=1-d_{1}-d_{2} \tag{2-12}
\end{gather*}
$$

Similarly, in type II modulation triangle, the duty cycles for $\boldsymbol{V}_{1}, \boldsymbol{V}_{2}$ and $\boldsymbol{V}_{3}$ are calculated as Eq. (2-13) - Eq. (2-15).

$$
\begin{gather*}
d_{1}=1-y+L_{2}  \tag{2-13}\\
d_{2}=y-x+L_{1}-L_{2}  \tag{2-14}\\
d_{3}=1-d_{1}-d_{2} \tag{2-15}
\end{gather*}
$$

Eq. (2-10)-Eq. (2-15) are generic for duty cycles calculation in any type I or type II modulation triangles. Meanwhile, the duty cycles of the nearest three vectors are simple for digital signal processors, since the calculation only contains the coordinates of the reference vector and nearest three vectors, which are rational numbers.

### 2.3.2 Switching sequence generation

Once the duty cycles of the nearest three vectors in a modulation triangle are determined, an appropriate switching sequence should be generated to synthesis the reference vector. To reduce switching losses and increase the possibility to balance the voltage of floating capacitors, a fivesegment approach is proposed to form the switching sequences instead of other methods using


Figure 2-9 Diagram of a five-segment switching sequence.


Figure 2-10 Switching sequences in: (a) type I modulation triangle; (b) type II modulation triangle.
higher number of segments, e.g., the commonly used seven-segment approach. The diagram of a five-segment switching sequence is shown in Figure 2-9.

All six kinds of available switching sequences in one modulation parallelogram using fivesegment approach are shown in Figure 2-10. Sequences (1), (2), and (3) shown in Figure 2-10 (a) are for type I modulation triangles, and sequences (4), (5), and (6) shown in Figure 2-10 (b) are for type II modulation triangles.

Each voltage vector in a certain switching sequence shown in Figure 2-10 may map to a couple of redundant switching states. When applying a voltage vector, the optimal switching state should be selected from all the available redundant switching states. In this work, the optimal switching
state is determined by following the rule of minimum switching operation to reduce switching losses. For instance, in the switching triangle for the case shown in Figure 2-7, one of the optimal switching sequences is $[4,2,0]\left(\boldsymbol{V}_{1}\right) \rightarrow[5,2,0]\left(\boldsymbol{V}_{2}\right) \rightarrow[5,3,0]\left(\boldsymbol{V}_{3}\right) \rightarrow[5,2,0]\left(\boldsymbol{V}_{2}\right) \rightarrow[4,2,0]\left(\boldsymbol{V}_{1}\right)$, since there is only one phase changing its switching state during voltage vectors transient. In one switching triangle, there are usually more than one optimal switching sequence based on this rule, which are also called redundant switching sequences in one switching triangle.

To illustrate the generic way to generate the switching sequence, Sector 1 is used as an example. As shown in Figure 2-7, the switching state at the bottom of list of the redundant switching states for each output vector is defined as the base switching state for that output vector. For an output vector at $\left(L_{1}, L_{2}\right)$, its base switching state is $\left[L_{1}, L_{2}, 0\right]$. On one hand, according to Figure 2-7, the coordinates of nearest three vectors in both type I and type II modulation triangles can be all derived if the coordinate of the reference vertex is known. Specifically, the base switching state is $\left[L_{1}+1, L_{2}, 0\right]$ for $\left(L_{1}+1, L_{2}\right),\left[L_{1}, L_{2}+1,0\right]$ for $\left(L_{1}, L_{2}+1\right)$, and $\left[L_{1}+1, L 2+1,0\right]$ for $\left(L_{1}+1, L_{2}\right)$. On the other hand, except the base switching state $\left[L_{1}, L_{2}, 0\right]$, all available switching states for the vertex $\left(L_{1}, L_{2}\right)$ are $\left[L_{1}+1, L_{2}+1,1\right],\left[L_{1}+2, L_{2}+2,2\right], \ldots,\left[6, L_{2}+6-L_{1}, 6-L_{1}\right]$, respectively. For instance, at vertex $(4,2)$, all available switching states are $[4,2,0],[5,3,1]$ and $[6,4,2]$, where $[4,2,0]$ is the base switching state.

As a summary, all the available redundant switching sequences classified by sequences (1), (2), (3) for type I modulation triangles and (4), (5), (6)for type II modulation triangles are listed in Table 2-3 and Table 2-4, respectively. Also, in Table 2-3 and Table 2-4, the dwell time of each switching state is also summarized based on the above-mentioned duty cycles calculation.

Table 2-3 All of the available redundant switching sequence classified by three kinds of sequences in type I switching triangles.

| Sequences for (1) | Sequences for (2) | Sequences for (3) |
| :---: | :---: | :---: |
| $\left[L_{1}+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ |
| $t_{1}=T_{s} d_{1} / 2$ | $t_{1}=T_{s} d_{2} / 2$ | $t_{1}=T_{s} d_{3} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+1+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ |
| $t_{2}=T_{s} d_{2} / 2$ | $t_{2}=T_{s} d_{3} / 2$ | $t_{2}=T_{s} d_{1} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ | $\left[L_{1}+2+i, L_{2}+1+i, i+1\right]$ |
| $t_{3}=T_{s} d_{3}$ | $t_{3}=T_{s} d_{1}$ | $t_{3}=T_{s} d_{2}$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+1+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ |
| $t_{4}=T_{s} d_{2} / 2$ | $t_{4}=T_{s} d_{3} / 2$ | $t_{4}=T_{s} d_{1} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ |
| $t_{5}=T_{s} d_{1} / 2$ | $t_{5}=T_{s} d_{2} / 2$ | $t_{5}=T_{s} d_{3} / 2$ |
| $\left(i=0,1, \ldots, 5-L_{1}\right)$ | $\left(i=0,1, \ldots, 5-L_{1}\right)$ | $\left(i=0,1, \ldots, 4-L_{1}\right)$ |

Table 2-4 All of the available redundant switching sequence classified by three kinds of sequences in type II switching triangles.

| Sequences for (4) | Sequences for (5) | Sequences for (6) |
| :---: | :---: | :---: |
| $\left[L_{1}+i, L_{2}+i, i\right]$ | $\left[L_{1}+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ |
| $t_{1}=T_{s} d_{1} / 2$ | $t_{1}=T_{s} d_{3} / 2$ | $t_{1}=T_{s} d_{2} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ |
| $t_{2}=T_{s} d_{2} / 2$ | $t_{2}=T_{s} d_{2} / 2$ | $t_{2}=T_{s} d_{1} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ | $\left[L_{1}+1+i, L_{2}+2+i, i+1\right]$ |
| $t_{3}=T_{s} d_{3}$ | $t_{3}=T_{s} d_{1}$ | $t_{3}=T_{s} d_{3}$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i+1\right]$ |
| $t_{4}=T_{s} d_{2} / 2$ | $t_{4}=T_{s} d_{2} / 2$ | $t_{4}=T_{s} d_{1} / 2$ |
| $\downarrow$ | $\downarrow$ | $\downarrow$ |
| $\left[L_{1}+i, L_{2}+i, i\right]$ | $\left[L_{1}+i, L_{2}+1+i, i\right]$ | $\left[L_{1}+1+i, L_{2}+1+i, i\right]$ |
| $t_{5}=T_{s} d_{1} / 2$ | $t_{5}=T_{s} d_{3} / 2$ | $t_{5}=T_{s} d_{2} / 2$ |
| $\left(i=0,1, \ldots, 5-L_{1}\right)$ | $\left(i=0,1, \ldots, 5-L_{1}\right)$ | $\left(i=0,1, \ldots, 5-L_{1}\right)$ |

Table 2-5 Transforming the switching state in sector 1 to other five sectors.

| Sector | Transformed switching states |
| :---: | :---: |
| 1 | $\left[S_{a}, S_{b}, S_{c}\right]$ |
| 2 | $\left[S_{a}-L_{2}, S_{b}+L_{1}-L_{2}, S_{c}\right]$ |
| 3 | $\left[S_{a}-L_{1}, S_{b}+L_{1}-L_{2}, S_{c}+L_{2}\right]$ |
| 4 | $\left[S_{a}-L_{1}, S_{b}+L_{1}-2 L_{2}, S_{c}+L_{1}\right]$ |
| 5 | $\left[S_{a}-L_{1}+L_{2}, S_{b}-L_{2}, S_{c}+L_{1}\right]$ |
| 6 | $\left[S_{a}, S_{b}-L_{2}, S_{c}+L_{1}-L_{2}\right]$ |

As can be seen, all the available redundant switching sequences can be derived from the coordinate of the original vertex in the modulation parallelogram. This derivation is very straightforward for digital signal processes because it does not require any look-up tables. Thus, complexity for implementation is significantly reduced and computational efficiency is enhanced. These available redundant switching sequences could then provide increased flexibility for floating capacitor voltage balancing because the dc floating capacitors charge/discharge effect is usually different under various switching sequences.

Furthermore, to simplify the analysis and calculation in other five sectors, the reference vector and all the output vectors at the vertices in any of the five sectors can be derived from a virtual vector located in sector 1 via Eq. (2-16).

$$
\begin{equation*}
\boldsymbol{V}=\boldsymbol{V}_{(1)} e^{j \frac{\pi}{3}(s-1)} \tag{2-16}
\end{equation*}
$$

where $\boldsymbol{V}$ is a vector in any of the six sectors; $\boldsymbol{V}_{(1)}$ is the virtual vector in Sector $1 ; s$ is the sector number where the reference vector is. Table 2-5 lists the mapping from the switching state in Sector 1 to those in the other five sectors. For instance, if the reference vector is in one of the other five sectors, its virtual vector in Sector 1 will be firstly derived using Eq. (2-16), such that its
modulation triangle determination and switching sequence generation can be performed using virtual vector in Sector 1.

### 2.3.3 Floating capacitors voltage balancing and CMV reduction

To synthesize a reference vector, there are multiple available switching sequences, as listed in Table 2-3 and Table 2-4. The optimal switching sequence is selected based on a finite-control-set (FCS) method [2.2], [2.3]. At the $j^{\text {th }}(j=1, \ldots, 5)$ switching state in a five-segment switching sequence shown in Figure 2-9, a function $E_{j}$ is designed to assess the dc floating capacitors voltage drifting in the converter as

$$
\begin{equation*}
E_{j}=\frac{1}{2} \sum_{x=A, B, C}\left(C_{F C} \Delta v_{F C x}\right)^{2}+\frac{1}{2} \sum_{y=1,2}\left(C_{d c} \Delta v_{d c y}\right)^{2} \tag{2-17}
\end{equation*}
$$

where the voltage differences are given as,

$$
\begin{align*}
\Delta v_{F C x} & =v_{F C x}-\frac{1}{4} U_{d c}  \tag{2-18}\\
\Delta v_{d c y} & =v_{d c y}-\frac{1}{2} U_{d c} \tag{2-19}
\end{align*}
$$

where $v_{F C x}(x=A, B, C)$ is the H -bridge dc floating capacitor voltage in phase $A, B, C$ respectively. $v_{d c y}(y=1,2)$ is the voltage across the positive arm capacitor and negative arm capacitor in dc link, respectively.

All the dc floating capacitors approach an overall balancing state when the cost function Eq. (2-17) is minimized. The derivative of the cost function can be represented as,

$$
\begin{equation*}
\frac{d E_{j}}{d t}=\sum_{x=A, B, C} \Delta v_{F C x} i_{c x}+\sum_{y=1,2} \Delta v_{d c y} i_{c y} \tag{2-20}
\end{equation*}
$$

where $i_{c x}(x=A, B, C)$ is the current through the H-bridge capacitors in phase $A, B, C$ respectively. $\mathrm{i}_{\text {cy }}(y=1,2)$ is the current through the positive arm capacitor and negative arm capacitor in the dc link, respectively.

The dc link of the hybrid 7-L converter can be modeled as

$$
\begin{gather*}
\Delta v_{d c 1}=-\Delta v_{d c 2}  \tag{2-21}\\
i_{O}=i_{c 1}-i_{c 2}  \tag{2-22}\\
i_{O}=i_{O A}+i_{O B}+i_{O C} \tag{2-23}
\end{gather*}
$$

where $i_{O}$ is current flowing out of the middle point $O$, and $i_{O A}, i_{O B}, i_{O C}$ are current from $O$ to phase$\operatorname{leg} A, B, C$ respectively.

Substituting Eq. (2-21) to Eq. (2-23) into Eq. (2-20) yields

$$
\begin{equation*}
\frac{d E_{j}}{d t}=\left(v_{F C x}-\frac{U_{d c}}{4}\right)\left(i_{c A}+i_{c B}+i_{c C}\right)+\left(v_{d c 1}-\frac{U_{d c}}{2}\right)\left(i_{O A}+i_{O B}+i_{O C}\right) \tag{2-24}
\end{equation*}
$$

where the terms $i_{C A}, i_{C B}, i_{C C}, i_{O A}, i_{O B}, i_{O C}$ all can be determined based on the switching state as illustrated in Table 2-2. For instance, $i_{C A}=-i_{A}, i_{C B}=0, i_{C C}=i_{C}, i_{O A}=0, i_{O B}=0, i_{O C}=i_{C}$, when the switching state of the hybrid 7 -L converter is $[6,5,2]$, where switching state 5 follows the conduction path ii and the switching state 2 follows the conduction path xi.

CM voltage at the $j^{\text {th }}(j=1, \ldots, 5)$ switching state is derived based on converter phase voltages $u_{A O}, u_{B O}$ and $u_{C O}$ [2.4], where,

$$
\begin{equation*}
u_{C M j}=\frac{1}{3}\left(u_{A O}+u_{B O}+u_{C O}\right)=\frac{U_{d c}}{4}\left(S_{A}+S_{B}+S_{C}-9\right) \tag{2-25}
\end{equation*}
$$

To reduce CM voltage, a cost function is given by Eq. (2-26) to minimize the error between desired value and the predicted one.

$$
\begin{equation*}
J_{C M}=\sum_{j=1}^{5}\left|u_{C M j}\right| \tag{2-26}
\end{equation*}
$$

For the switching sequence over one sampling period, a total cost function $J$ is defined as Eq. (2-27) to balance floating capacitors voltage and simultaneously reduce CM voltage, where $t_{j}$ is the dwell time of the $j^{t h}$ switching state in the switching sequence, and $\lambda(0 \leq \lambda \leq 1)$ is the weighting factor for CM voltage. Hence, multiple values of cost function Eq. (2-27) are calculated using all the available switching sequences listed in Table 2-3 and Table 2-4. With this FCS method, the optimal switching sequence can be determined by the one that's minimizes the cost function Eq. (2-27).

$$
\begin{equation*}
J=\sum_{j=1}^{5} t_{j} \frac{d E_{j}}{d t}+\lambda J_{C M} \tag{2-27}
\end{equation*}
$$

### 2.3.4 Scheme flowchart comparison

To demonstrate the efficiency and simplicity of the proposed SVM scheme in implementation, the flowcharts of the proposed scheme and the conventional 7-L SVM [2.2] are both given in Figure 2-11. By adopting the two schemes, the same groups of switching sequences and the dwell time are achieved, if the reference vector has the same coordinates in SV diagram. However, in the conventional scheme, duty cycles and all available switching sequences should be prestored in complex LUTs, which consumes much effort and controller resources. Also, the LUTs require the re-design for multilevel converters with different voltage levels. Instead, the proposed SVM scheme only requires some generic and fast calculation in Figure 2-11, getting rid of complex LUTs. In addition, this scheme is generalized for multilevel converters with different voltage levels.

### 2.3.5 Simulation studies

To simulate the variable frequency operation for electric population, this paper tested the hybrid 7-L ANPC-H converter operated with the variable output frequency from 60 Hz to 1000


Figure 2-11 The implementation flowcharts of scheme 1 (the proposed scheme) and scheme 2
(the conventional scheme in [2.2]).

Hz with a modulation index of 1.3. The modulation index $m$ of this hybrid 7-L converter is defined as Eq. (2-28), where full modulation index for linear modulation region in SVM is 1.5 when phase voltage amplitude $V_{\text {ref }}$ equals to $\sqrt{3} U_{d c} / 2$. The load used in the dynamic test was a three-phase resistor-inductor (RL) load with power factor 0.2 . The weighing factor $\lambda$ is set to be $6.7 \times 10^{-5}$.

$$
\begin{equation*}
m=\sqrt{3}\left|V_{r e f}\right| / U_{d c} \tag{2-28}
\end{equation*}
$$

### 2.3.5.1 Variable frequency operation

Figure 2-12 shows the simulation results including waveforms of the hybrid converter ac output line voltage, phase currents, dc voltage across floating capacitors in both dc link and $\mathrm{H}-$ bridges, and the CM voltage. The fundamental frequency increases from 60 Hz to 1000 Hz within 0.3 s with an averaged ramp rate of $3133 \mathrm{~Hz} / \mathrm{s}$. According to simulated results, the capacitors voltages are all controlled at their rated value over the entire frequency range. The phase currents


Figure 2-12 Variable frequency operation from 60 Hz to 1000 Hz .
are gradually reduced during the transition from low frequency to high frequency range, since the load impedance increases with the increase of the fundamental frequency of the output. Thus, the proposed SVM strategy can be effectively applied for the 7-L ANPC-H converter prototype over the full-frequency operation.

The detailed waveforms of ac output line voltage at $60 \mathrm{~Hz}, 400 \mathrm{~Hz}$ and 1000 Hz are presented in Figure 2-13 (a), (b), (c), respectively. With the modulation index 1.3, the hybrid converter generates 13 levels in the ac line voltage under different fundamental frequencies with the peak-to-peak value of ac line voltage is 9 kV . The harmonic spectrums of the three ac line voltage waveforms are given in Figure 2-14 (a), (b), (c), and their corresponding total harmonics distortion


Figure 2-13 Waveforms of line voltage at the fundamental frequency (a) 60 Hz , (b) 400 Hz and (c) 1 kHz .


Figure 2-14 Harmonics spectrum analysis at the fundamental frequency (a) 60 Hz , (b) 400 Hz and (c) 1 kHz .
(THD) values are $10.95 \%, 11.78 \%, 13.01 \%$, respectively. Noted that the harmonics are mainly concentrated on the multiple times of the SVM switching frequency, which is 20 kHz . Although there are fewer switching actions over one fundamental cycle for high-frequency operations such as 400 Hz and 1000 Hz than low-frequency conditions such as 60 Hz , the THD in the highfrequency scenarios only slightly increased.

### 2.3.5.2 Averaged switching frequency

The switching actions of all devices in both ANPC and H-bridges are counted such that the averaged switching frequency of devices in ANPC and H-bridge is derived under different conditions. Figure 2-15 (a) shows the averaged switching frequency of ANPC devices and Hbridge devices under different operated fundamental frequency when applying modulation index 1.3 for the hybrid 7-L converter. The average switching frequency curve is flat versus the ac output fundamental frequency. The ANPC devices have much lower switching frequency, which are implemented using IGBTs. Figure 2-15 (b) shows the averaged switching frequency under different modulation indexes when operate with 60 Hz fundamental frequency. With the increasing of modulation index, the switching actions in both ANPC and H-bridge decrease.

### 2.3.5.3 Capacitor voltage balancing and CMV reduction

To validate the proposed scheme for capacitors voltage balancing with simultaneous CM voltage reduction, the Figure 2-16 shows waveforms when modulation index step changed from


Figure 2-15 The averaged switching frequency of devices in ANPC and H-bridge when applying (a) modulation index 1.3 and different fundamental frequency, (b) 60 Hz fundamental frequency and different modulation indexes.


Figure 2-16 Modulation index transition from 1.3 to 0.61 with and without applying CM reduction scheme.
1.3 to 0.61 , meanwhile, the CM voltage reduction scheme $\left(\lambda=6.7 \times 10^{-5}\right)$ is applied and then switched off to show the impact. According to results under modulation index $0.61, \mathrm{CM}$ voltage peak-to-peak is reduced from 3500 V to 1040 V when CM voltage reduction scheme is applied. In case of modulation index 0.61 with CM voltage reduction scheme applied, there are only voltage transitions between adjacent voltage levels in phase voltages, however inducing more voltage fluctuation across the dc floating capacitors. Also, dc floating capacitors voltage is stable in the


Figure 2-17 7-L ANPC-H output line voltage at 60 Hz frequency.


Figure 2-18 7-L ANPC-H output line voltage at 400 Hz frequency.
modulation index transient from 1.3 to 0.61 , which demonstrates the proposed SVM can balance capacitors voltage can operate simultaneously with the CM voltage reduction scheme.

### 2.3.6 Experimental studies

### 2.3.6.1 Full-scale 7-L ANPC-H converter test

The assembled 7-L ANPC-H converter was tested in the three-phase inverter mode under 3kV dc link and full modulation index. Figure 2-17 shows the experimental result in the lowfrequency mode, e.g., 60 Hz , while Figure 2-18 and Figure 2-19 illustrate the high-frequency


Figure 2-19 7-L ANPC-H output line voltage at 1 kHz frequency.


Figure 2-20 7-L ANPC-H output line voltage when frequency transiting from 60 Hz to 400 Hz .
operation, i.e., 400 Hz and 1 kHz . Figure 2-20 demonstrates the established 7-L ANPC-H converter prototype can smoothly operate from low-frequency to high-frequency range, e.g., transiting from 60 Hz to 400 Hz , which represents a typical speed ramp in propulsion drive applications.

### 2.3.6.2 Converter efficiency estimation

To compare the power efficiency of 7-L ANPC-H converter when its inner 3.3 kV ANPC stage adopts different structures i.e., all- SiC , all-Si and hybrid $\mathrm{Si}+\mathrm{SiC}$, the converter switching losses and conduction loss are estimated by converter loss model based on SiC and Si devices loss data, under different converter power ratings. Figure 2-21 (a) shows converter efficiency comparison


Figure 2-21 7-L ANPC-H converter with different structure in 3.3 kV ANPC stage (a) efficiency curve under different power ratings and (b) loss distribution at full power.
under the three cases, where the all-SiC case has the highest efficiency. Figure 2-21 (b) shows the switching loss and conduction loss break down both in 3.3 kV ANPC and 1.2 kV HB stages, when 7-L converter operates at 1 MVA rated load. The three cases have the same switching and conduction losses in 1.2 kV HB stage. Because SiC devices consume much smaller energy loss both in switching and conducting, the all-SiC case has the minimum switching/conduction losses in 3.3 kV ANPC stage, the hybrid $\mathrm{Si}+\mathrm{SiC}$ case has the medium values, and the all-Si case has the largest losses.

### 2.3.6.3 Modulation computational efficiency evaluation

To further demonstrate the computational efficiency of the proposed SVM for 7-L ANPC-H converter, both the conventional SVM [2.2] and the proposed SVM are implemented. The control algorithms in block of scheme 1 and block of scheme 2 shown in Figure 2-11 were both implemented in dSPACE and their execution times are also measured in the real-time mode. The implemented discrete control frequency in dSPACE is 20 kHz , namely, the execution time of the strategies in every control iteration cannot exceed $50 \mu \mathrm{~s}$. Figure 2-22 exhibits the real-time mode


Figure 2-22 Execution time comparison of the conventional and proposed SVM strategies. execution times of the two strategies for the specific case when the modulation index is set to be 1.05. As it can be seen, the execution time in conventional SVM strategy is $25.6 \mu \mathrm{~s}$, while the turnaround time is $16.1 \mu \mathrm{~s}$ in the proposed SVM, which demonstrated over $1 / 3$ turnaround time reduction when using the proposed SVM.

### 2.4 Conclusions

In this chapter, the hybrid 7-L ANPC-H converter which adopts the internal cascaded structure is investigated and a 1 MVA prototype with 3 kV de link and $\mathrm{Si} / \mathrm{SiC}$ hybrid configuration is implemented for the next-generation aircraft electric propulsion applications. To lower the complexity of the conventional SVM, a fast and computationally efficiency SVM without using any pre-stored look-up table is proposed for the 7-L hybrid converter. The generalized switching sequences and duty cycle calculation of this scheme is suitable for any modulation triangles in the 7-L space vector diagram. The proposed SVM scheme is generic and can be applied to other multilevel converter topologies. Under the proposed computational efficient SVM, all floating capacitors voltage is balanced, and CM voltage could also be reduced. Validated by the simulation and experiments, the established prototype can successfully operate at MV conditions under typical frequency range of electric aircraft propulsion by using the proposed SVM scheme. Therefore, with the proven excellent simulation and testing performance, the established 7-L

ANPC-H converter with internal cascaded structure can significantly advance the next-generation medium-voltage electric aircraft propulsion based on the up-to-date Si and SiC based devices.

### 2.5 Reference

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## CHAPTER 3

## ACTIVE HYBRID MODULATION FOR MULTILEVEL CONVERTER WITH INTERNAL CASCADED STRUCTURE

### 3.1 Objectives

As mentioned in last chapter, when building 7-L hybrid ANPC-H converter prototype, there are three ANPC PEBBs investigated and prototyped in this work, which are: all-Si switch positions shown in Figure 2-4 (a), all-SiC switch positions shown in Figure 2-4 (b), and hybrid "Si+SiC" switch positions shown in Figure 2-4 (c). When adopting the proposed SVM strategy presented in last chapter, the efficiency curve and loss distribution under the three setups are shown in Figure 2-21. Based on these results, all-Si solution has the lowest cost but generates the largest loss, and all-SiC solution generates the lowest loss but has the highest cost. Comparatively, hybrid " $\mathrm{Si}+\mathrm{SiC}$ " solution is an optimized solution based on trade-off of cost and performance. According to loss distribution of this hybrid solution shown in Figure 2-21, the most loss under hybrid "Si+SiC" solution are from switching losses of Si IGBT devices. It is because the Si IGBT devices in ANPC building blocks run high switching frequency under SVM strategy, and Si IGBT devices are more lossy than SiC MOSFETs.

To further reduce the converter power loss to improve power efficiency, an active hybrid modulation strategy is presented in this chapter. In this proposed modulation strategy, the Si IGBT devices operate with low frequency, and all high frequency switching actions are moved to SiC MOSFET devices in 7-L ANPC-H hybrid converter. With this hybrid modulation, the 7-L converter overall output still has similar performance with SVM, but overall switching losses are optimized with the switching action redistribution. In this way, the 7-L ANPC-H hybrid converter could reach optimized benefits with both cost-effective and high-power efficiency.

### 3.2 Principle of active hybrid modulation

### 3.2.1 $\quad$ Switching states definition

Figure 2-1 shows the topology of the hybrid 7-L converter. Each phase of the hybrid 7-L converter consists of two power stages, i.e., a 3-L ANPC power stage in series with an H-bridge stage. As shown in Figure 2-1, in phase A, the 3-L ANPC power stage has six switch positions, i.e., $S_{1} \sim S_{6}$, which are seen as Si IGBTs in this chapter. To operate the 3-L ANPC power stage, the ON/OFF gate signals of $S_{1}-S_{5}, S_{2}-S_{3}$, and $S_{6}-S_{4}$ are complimentary to each other. The 3-L ANPC converter has three possible switching states. More specifically, 1) $\mathbf{P}$ state, Node A' is connected to the positive tail of the DC link, i.e., $\left.u_{A^{\prime}} O=U_{d c} / 2 ; 2\right) \mathbf{O}$ state, Node A' is connected to the NP of the DC link, i.e., $\left.u_{A^{\prime}} O=0 ; 3\right) \mathbf{N}$ state, Node $\mathrm{A}^{\prime}$ is connected to the negative tail of the dc link, i.e., $u_{A^{\prime} O}=-U_{d c} / 2$. There are two configurations that can lead to the $\mathbf{O}$ state, i.e., $\mathbf{O}+$, where $S_{2}$ and $S_{5}$ are ON, and $\mathbf{O}-$, where $S_{3}$ and $S_{6}$ are ON. Accordingly, the 3-L ANPC converter line-to-neutral output voltage can be represented as $u_{k^{\prime}} o=s_{k^{\prime}} o U_{d c} / 2$, where $s_{k^{\prime}} O \in\{-1,0,+1\}$ and $k \in\{\mathrm{~A}, \mathrm{~B}, \mathrm{C}\}$. The voltage stresses of all switches in the 3-L ANPC power stage are $U_{d c} / 2$, and the voltage stresses of all switches in the H -bridge power stage are $U_{d c} / 4$, therefore, the 3-L ANPC in this hybrid topology is called HV power stage, and the H-bridge is called LV power stage. Table 3-1 lists all the switching states of phase A and their corresponding NP current and the current flowing through H-bridge capacitor.

For a hybrid 7-L converter phase-leg, the output voltage $u_{A O}$ has 7 possible voltage levels. i.e., $+3 U_{d c} / 4,+U_{d c} / 2,+U_{d c} / 4,0,-U_{d c} / 4,-U_{d c} / 2$, and $-3 U_{d c} / 4$, which are defined as voltage level $+3,+2$, $+1,0,-1,-2$, and -3 , respectively. As shown in Table 3-1, there is only one switching state, i.e., $\mathbf{P 3}(1)$, that can generate voltage level +3 ; there are 2 switching states, i.e., $\mathbf{P 2}$ (1) and $\mathbf{P 2}$ (2), that can generate voltage level +2 ; there are 3 switching states, i.e., $\mathbf{P 1 ( 1 ) , ~ P 1 ( 2 ) , ~ a n d ~ P 1 ( 3 ) , ~ t h a t ~ c a n ~}$
 can generate voltage level 0 ; there are 3 switching states, i.e., $\mathbf{N 1 ( 1 ) , ~} \mathbf{N 1 ( 2 )}$, and $\mathbf{N 1 ( 3 )}$, that can generate voltage level -1 ; there are 2 switching states, i.e., $\mathbf{N} 2(\mathbf{1})$ and $\mathbf{N} 2(2)$, that can generate voltage level -2 ; there is only 1 switching state, i.e., $\mathbf{N 3}(1)$, that can generate voltage level -3 . Due to the cascaded structure, the line-to-neutral output voltage of a hybrid 7-L converter phase-leg can be represented as

$$
\begin{equation*}
V_{\text {out }}=\left(S_{A}+S_{B} e^{j \frac{2}{3} \pi}+S_{C} e^{j \frac{4}{3} \pi}\right) U_{d c} \tag{3-1}
\end{equation*}
$$

where $u_{A O}$ is the hybrid 7-L converter phase-to-neutral voltage in phase A.

Table 3-1 Switching states of one phase of the 7-L HMC with the corresponding switching states of ANPC and HB stage.

| Switching States | Voltage Levels | $u_{A O}$ | ANPC Switching States | $\begin{aligned} & S_{1} S_{2} S_{4} \\ & \left(\bar{S}_{5} \overline{S_{3}} \overline{S_{6}}\right) \end{aligned}$ | $i_{O A}$ | HB <br> Switching States | $\begin{gathered} S_{7} S_{9} \\ \left(\overline{S_{8}} \overline{S_{10}}\right) \end{gathered}$ | $i_{F C A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P3 | +3 | $3 U_{d c} / 4$ | P | 110 | 0 | P | 01 | $-i_{A}$ |
| P2 | +2 | $U_{d c} / 2$ | P | 110 | 0 | O+ | 11 | 0 |
|  |  |  |  | 110 |  | O- | 00 |  |
| P1 | +1 | $U_{d c} / 4$ | P | 110 | 0 | N | 10 | $i_{A}$ |
|  |  |  | O+ | 011 | $i_{A}$ | P | 01 | $-i_{A}$ |
|  |  |  | O- | 100 | $i_{A}$ | P | 01 | $-i_{A}$ |
| O0 | 0 | 0 | O+ | 011 | $i_{A}$ | O+ | 11 | 0 |
|  |  |  | O- | 100 |  |  | 11 |  |
|  |  |  | O+ | 011 |  | O- | 00 |  |
|  |  |  | O- | 100 |  |  | 00 |  |
| N1 | -1 | $-U_{d c} / 4$ | O+ | 011 | $i_{A}$ | N | 10 | $i_{A}$ |
|  |  |  | O- | 100 | $i_{A}$ | N | 10 | $i_{A}$ |
|  |  |  | N | 001 | 0 | P | 01 | $-i_{A}$ |
| N2 | -2 | $-U_{d c} / 2$ | N | 001 | 0 | O- | 00 | 0 |
|  |  |  |  | 001 |  | O+ | 11 |  |
| N3 | -3 | $\begin{gathered} - \\ 3 U_{d c} / 4 \end{gathered}$ | N | 001 | 0 | N | 10 | $i_{A}$ |

### 3.2.2 Basic idea of active hybrid modulation

According to Eq. (3-1), the line-to-neutral voltage of the hybrid 7-L converter is the summation of the line-to-neutral voltage of the ANPC converter and AC output voltage of the H -bridge converter. Therefore, it is feasible to decompose the modulation of the entire three-phase hybrid 7-L converter into the modulations of the two power stages. Compared to other popular modulation methods for 7-L converters, e.g., 7-L carrier-based pulse width modulation, or 7-L SVM, this decomposition can effectively reduce the modulation complexity. A single H -bridge has three possible switching states, as listed in Table 3-1. According to [3.1], the H-bridges in the same position of three phase-legs in a cascaded H -bridge (CHB) converter is equivalent to a three-phase three-level converter configuration, which is also true for the three H -bridges in the hybrid 7-L converter in this work. Specifically, Figure 3-1 (a) shows a single H-bridge structure used in the hybrid 7-L converter,

Figure 3-1 (b) exhibits one phase-leg of a three-phase three-level converter. The two structures have the same AC output voltage, as shown in Figure 3-1 (c), if the same PWM signals are applied


Figure 3-1 The equivalence of an H -bridge and a three-level converter phase-leg.


Figure 3-2 Diagram of the basic idea of the hybrid modulation.
to the four power switches both in Figure 3-1 (a) and (b). Hence, the three H-bridges in the hybrid 7-L converter can be switched by a 3-L SVM, since they are equivalent to a three-phase threelevel converter.

The basic idea of the proposed method is illustrated in Figure 3-2. The hybrid modulation consists of two paralleled processes, i.e., the low-frequency (LF) modulation applied to the ANPC converter and a high-frequency (HF) 3-L SVM applied to the H -bridge converters.

As shown in Figure 3-2, for the LF modulation, the reference $u_{A O}^{*}$ for phase A of the hybrid 7L converter is supposed to be within the range from $-V_{m}$ to $+V_{m}$, which is related to the maximum linear modulation boundary, where

$$
\begin{gather*}
V_{m}=\frac{\sqrt{3}}{2} U_{d c}  \tag{3-2}\\
V_{c}=\frac{1}{3} V_{m} \tag{3-3}
\end{gather*}
$$

There are three cases in the LF modulation: 1) When $u_{A O}^{*}$ is higher than the threshold value $V_{c}$, given by Eq. (3-3), the switching state $\mathbf{P}$ is applied to the ANPC converter phase-leg. Thus, the line-to-neutral voltage of the ANPC phase-leg is $\left.u_{A O}=U_{d c} / 2.2\right)$ When $u_{A O}^{*}$ is between $-V_{c}$ and $V_{c}$, the switching state $\mathbf{O}+$ or $\mathbf{O}$ - is applied to the ANPC phase-leg, thus $u_{A^{\prime} O}=0$.3) When $u_{A O}^{*}$ is lower than the threshold value $-V_{c}$, the switching state $\mathbf{N}$ is applied to 3-L ANPC converter phase-leg, thus $u_{A^{\prime} O}=-U_{d c} / 2$.

As shown in Figure 3-2, subtracting the line-to-neutral voltage of the ANPC phase-leg value of $u_{A^{\prime}} O$ from the reference value of the $u_{A O}^{*}$, the reference voltage for the H -bridge converter in phase A, i.e., $u_{A A^{*}}^{*}$, can be obtained. In this work, a three-phase 3-L SVM is used to control the three H-bridges in phase A, B, C. To convey the concept more explicitly, a flowchart of the hybrid modulation for the hybrid 7-L converter is illustrated in Figure 3-3. The space-vector diagram for the 3-L SVM under $\alpha \beta$-frame (converted to the $60^{\circ} \alpha \beta$-frame) [3.2], [3.3] for the three H -bridges in phase A, B, and C is given in Figure 3-4, which basically resembles to a three-level space-vector diagram for a three-phase 3-L converter. As shown, the space-vector diagram of this equivalent 3L converter consists of six sectors, and each sector consists of four modulation triangle regions, e.g., $r_{1}, r_{2}, r_{3}, r_{4}$ are the four modulation triangle regions in sector 1 . In the 3 -L SVM, the three nearest vectors surrounding the modulation triangle region are operated in a switching sequence pattern to synthesize the reference vector $V_{\text {ref }}$ for H -bridges, within one switching cycle $T_{s}$.


Figure 3-3 Flowchart of the hybrid modulation for three-phase hybrid 7-L converter.


Sector 5

Figure 3-4 Space-vector diagram of 3-L SVM for three floating H-bridges.

There are three steps to implement the 3-L SVM, i.e., 1) determining the sector and modulation triangle region according to the reference vector location, 2) calculating duration time of the nearest three vectors, and 3) generating switching sequences. The first step is straightforward under

Table 3-2 Dwell time of the nearest three vectors in sector 1.

| Region | $\boldsymbol{t}_{\boldsymbol{a}}$ | $\boldsymbol{t}_{\boldsymbol{b}}$ | $\boldsymbol{t}_{\boldsymbol{c}}$ |
| :---: | :---: | :---: | :---: |
| $r_{1}$ | $\left(1-t_{b}-t_{c}\right) T_{s}$ | $u_{\alpha}^{*} T_{s}$ | $u_{\beta}^{*} T_{s}$ |
| $r_{2}$ | $\left(1-t_{b}-t_{c}\right) T_{s}$ | $\left(u_{\alpha}^{u}-1\right) T_{s}$ | $u_{\beta}^{*} T_{s}$ |
| $r_{3}$ | $\left(1-u_{\alpha}^{*}\right) T_{s}$ | $\left(1-t_{a}-t_{c}\right) T_{s}$ | $\left(1-u_{\beta}^{*}\right) T_{s}$ |
| $r_{4}$ | $\left(1-t_{b}-t_{c}\right) T_{s}$ | $u_{\alpha}^{*} T_{s}$ | $\left(u_{\beta}^{*}-1\right) T_{s}$ |

Table 3-3 The switching sequences with associated dwell time for each switching state in sector 1 .

| Region | Switching sequences |
| :---: | :---: |
| $r_{1}$ |  |
| $r_{2}$ | $\begin{aligned} & \text { ONN }\left(t_{a} / 2\right) \text {-PNN }\left(t_{b} / 2\right)-\text { PON }\left(t_{c}\right) \text {-PNN }\left(t_{b} / 2\right) \text {-ONN }\left(t_{a} / 2\right) \\ & \text { PNN }\left(t_{b} / 2\right)-\text {-PON }\left(t_{c} / 2\right)-\text {-POO }\left(t_{a}\right) \text {-PON }\left(t_{c} / 2\right) \text {-PNN }\left(t_{b} / 2\right) \end{aligned}$ |
| $r_{3}$ | ONN $\left(t_{c} / 2\right)-$ OON $\left(t_{a} / 2\right)-\mathbf{P O N}\left(t_{b}\right)-$ OON $\left(t_{a} / 2\right)-$ ONN $\left(t_{c} / 2\right)$ OON $\left(t_{a} / 2\right)-\mathbf{P O N}\left(t_{b} / 2\right)-\mathbf{P O O}\left(t_{c}\right)-\mathbf{P O N}\left(t_{b} / 2\right)-$ OON $\left(t_{a} / 2\right)$ PON $\left(t_{b} / 2\right)-\mathbf{P O O}\left(t_{c} / 2\right)-\mathbf{P P O}\left(t_{a}\right)-\mathbf{P O O}\left(t_{c} / 2\right)-\mathbf{P O N}\left(t_{b} / 2\right)$ |
| $r 4$ | $\begin{aligned} & \text { OON }\left(t_{a} / 2\right) \text {-PON }\left(t_{b} / 2\right)-\mathbf{P P N}\left(t_{c}\right) \text {-PON }\left(t_{b} / 2\right)-\text { OON }\left(t_{a} / 2\right) \\ & \text { PON }\left(t_{b} / 2\right) \text {-PPN }\left(t_{c} / 2\right)-\operatorname{PPO}\left(t_{a}\right) \text {-PPN }\left(t_{c} / 2\right)-\operatorname{PON}\left(t_{b} / 2\right) \end{aligned}$ |

the adopted $60^{\circ}$ reference frame, since the sector and modulation triangle region number can be achieved by simple geometric calculation without rational numbers. Defining the dwell time of the three nearest vectors $\boldsymbol{V}_{1}, \boldsymbol{V}_{2}, \boldsymbol{V}_{3}$ as $t_{a}, t_{b}, t_{c}$, respectively, according to the volt-second balancing principle, the dwell time of the three nearest vectors can be calculated using Eq. (3-4).

$$
\begin{equation*}
\boldsymbol{V}_{r e f} T_{s}=\boldsymbol{V}_{1} t_{a}+\boldsymbol{V}_{2} t_{b}+\boldsymbol{V}_{3} t_{c} \tag{3-4}
\end{equation*}
$$

Table 3-2 exhibits the calculated dwell time of the three nearest vectors in four regions in sector 1 shown in Figure 3-4, where $u_{\alpha}^{*}$ and $u_{\beta}^{*}$ are defined as the transformed $\alpha \beta$ references for H -bridges
in Figure 3-4. Table 3-3 gives all the switching sequences together with the assigned duration time of each switching state in the four regions in sector 1 . In this work, the five-segment approach [3.2], [3.3] is used to form the switching sequence, since it is easier to balance dc floating capacitors voltages in three H -bridges with plenty of redundant switching sequences in the fivesegment approach.

### 3.2.3 Capacitor voltage balancing scheme

The details of three H-bridges in hybrid 7-L converter are shown in Figure 2-1, where the currents flowing through $C_{F C A}, C_{F C B}$, and $C_{F C C}$ are $i_{F C A}, i_{F C B}$, and $i_{F C C}$, respectively and the voltages across $C_{F C A}, C_{F C B}$, and $C_{F C C}$ are $v_{F C A}, v_{F C B}$, and $v_{F C C}$, respectively. When the $i^{\text {th }}$ vector of the fivesegment switching sequence is applied, where $i=1,2, \ldots, 5$, there are unavoidable voltage fluctuations though $v_{F C A}, v_{F C B}$, and $v_{F C C}$. The three voltages are all supposed to be constant at $U_{d c} / 4$. The reason for these voltage fluctuations is that $C_{F C A}, C_{F C B}$, and $C_{F C C}$ are charged/discharged by $i_{F C A}, i_{F C B}$, and $i_{F C C}$, as

$$
\begin{align*}
& i_{F C A}=-s_{A A^{\prime}-i} i_{A}  \tag{3-5}\\
& i_{F C B}=-s_{B B^{\prime}-i} i_{B}  \tag{3-6}\\
& i_{F C C}=-s_{C C^{\prime}-i} i_{C} \tag{3-7}
\end{align*}
$$

where the symbols $s_{A A^{\prime}-i}, s_{B B^{\prime}-i}, s_{C C^{\prime}-i}(i=1,2, \ldots, 5)$ represent the switching function of H -bridge
 three possible values: $1,0,-1$, i.e., the switching states $\mathbf{P}, \mathbf{O}, \mathbf{N}$, in the H -bridge.

According to Table 3-3, there are several possible switching sequences in each modulation triangle region which have different charge/discharge effects on H -bridge capacitors. In this work,
a finite-control-set (FCS) method [3.2], [3.3], [3.4] is adopted to select the optimal switching sequence to minimize the voltage fluctuations of the three capacitors over one switching cycle $T_{s}$. At a certain switching state, an energy function $E$ is designed to assess derivations between the actual dc floating capacitors voltages and their references as

$$
\begin{equation*}
E=\frac{1}{2} C_{F C A}\left(\Delta v_{F C A}\right)^{2}+\frac{1}{2} C_{F C B}\left(\Delta v_{F C B}\right)^{2}+\frac{1}{2} C_{F C C}\left(\Delta v_{F C C}\right)^{2} \tag{3-8}
\end{equation*}
$$

where the voltage differences are given by

$$
\begin{align*}
& \Delta v_{F C A}=v_{F C A}-\frac{1}{4} U_{d c}  \tag{3-9}\\
& \Delta v_{F C B}=v_{F C B}-\frac{1}{4} U_{d c}  \tag{3-10}\\
& \Delta v_{F C C}=v_{F C C}-\frac{1}{4} U_{d c} \tag{3-11}
\end{align*}
$$

All the dc floating capacitors achieve overall balancing states when the cost function in Eq. $(3-8)$ is minimized [3.2]. The derivative of the cost function can be represented as

$$
\begin{equation*}
\frac{d E}{d t}=\Delta v_{F C A} i_{F C A}+\Delta v_{F C B} i_{F C B}+\Delta v_{F C C} i_{F C C} \tag{3-12}
\end{equation*}
$$

Which can also be rewritten as

$$
\begin{equation*}
\frac{d E}{d t}=\Delta v_{F C A} i_{A} s_{A A^{\prime}-i}+\Delta v_{F C B} i_{B} s_{B B^{\prime}-i}+\Delta v_{F C C} i_{C} s_{C C^{\prime}-i} \tag{3-13}
\end{equation*}
$$

Over one switching cycle $T_{s}$, according to Table 3-3, when using the five-segment switching sequence, there are five vectors, and their dwell times are represented by $t_{1}$ to $t_{5}$. Then the cost function $J$ for the entire switching cycle can be derived using Eq. (3-13) as

$$
\begin{equation*}
J=\sum_{i=1}^{5} t_{i}\left(\Delta v_{F C A} i_{A} S_{A A^{\prime}-i}+\Delta v_{F C B} i_{B} S_{B B^{\prime}-i}+\Delta v_{F C C} i_{C} S_{C C^{\prime}-i}\right) \tag{3-14}
\end{equation*}
$$

It is noteworthy that $v_{F C A}, v_{F C B}, v_{F C C}, i_{A}, i_{B}, i_{C}$ in Eq. (3-14) can all be sampled once per
 be derived by each switching sequence according to Table 3-1 and Table 3-3. As listed in Table 3-3, there are more than one switching sequences in a certain modulation triangle region where the reference vector locates in. Using Eq. (3-14), the optimal switching sequence that leads to the minimum $J$ can be identified and applied to the next switching period.

### 3.3 Overall control architecture

The overall control framework of the proposed hybrid modulation is depicted in Figure 3-5. The overall closed-loop control consists of the LF modulation, i.e., Block B4, for the 3-L ANPC converter and the 3-L SVM, i.e., Block B6, for three floating H-bridge converters. The references for 3-L ANPC converter, i.e., $u_{A O}^{*}, u_{B O}^{*}$, and $u_{C O}^{*}$ are generated by the coordination of the H-bridge DC voltage control block, i.e., Block B1, the ZSV injection block, i.e., Block B2, and the neutral point (NP) voltage balancing control block, i.e., Block B3.

In Block B2, the ZSV $u_{c m}$ is selected between the $3^{\text {rd }}$ order ZSV signal $u_{c m 3}$ and the $9^{\text {th }}$ order ZSV signal $u_{c m 9}$. According to [3.5], the $3^{\text {rd }}$ order ZSV signal injection is preferable when high modulation index is applied, whereas the $9^{\text {th }}$ order ZSV signal is preferable with lower modulation index is applied, since the $3^{\text {rd }}$ order ZSV injection can lead to wider stable operating region while the $9^{\text {th }}$ order ZSV injection can achieve lower THD. The phases of $u_{c m 3}$ and $u_{c m 9}$ are aligned to three-phase sinusoidal references $u_{A O}^{* *}, u_{B O}^{* *}$, and $u_{C O}^{* *}$, where the initial phase of $u_{c m 3}$ is $-\pi / 2$ and the initial phase of $u_{c m 9}$ is $\pi$ when the initial phase of $u_{A O}^{* \prime}$ is 0 . The amplitudes of both $u_{c m 3}$ and $u_{c m 9}$ are


Figure 3-5 The block diagram of the closed-loop hybrid modulation strategy for the hybrid 7-L converter.
calculated by a proportional integral (PI) controller in Block B1, which aims to control the total voltage across three H -bridge capacitors to track the reference, i.e., $3 \times U_{d c} / 4=3 U_{d c} / 4$. Also, a piecewise selection function is used to determine the ZSV to be injected based on the modulation index $m$. In Block B6, the three H-bridge capacitors voltages are balanced by the proposed 3-L SVM, such that each H-bridge capacitor voltage sticks to the reference, i.e., $U_{d c} / 4$.

As listed in Table 3-1, the current flowing out of neutral-point in each phase leg always equals to the phase current when the switching states $\mathbf{O}+$ or $\mathbf{O}$ - are applied, whereas it equals to 0 when $\mathbf{P}$ or $\mathbf{N}$ are applied. Because of the symmetry of the phase current polarity over one fundamental cycle, the neutral-point capacitors could be self-balanced theoretically. However, there is an unavoidable mismatch of capacitance, hence, the closed-loop neutral-point voltage balancing is still needed. The PI controller in Block 3 generates a $\Delta v^{*}$ to adjust the threshold $V_{c}$ based on the feedback $\Delta v$, which is the derivation between the voltages of the top and bottom capacitors in the dc link. As shown in Figure 3-2, the positive part of the line-to-neutral voltage of the ANPC phaseleg is re-shaped if the $\Delta v^{*}$ is not zero. In other words, the duration of switching states $\mathbf{O}+$ or $\mathbf{O}$ applied in the positive part of each 3-L ANPC converter phase-leg can be adjusted, whereas those in the negative part remain the same, such that the overall charge/discharge of the two NP capacitors can be adjusted over one fundamental cycle. In this way, the NP voltage balancing can be achieved.

As shown in Figure 3-5, with the LF modulation, the ON/OFF state signals of the 3-L ANPC converter and references $u_{A A}^{*}, u_{B B}^{*}$, and $u_{C C}^{*}$ for 3-L SVM of three H-bridges are generated. After the $a b c$-frame to $\alpha \beta$-frame ( $60^{\circ}$ frame) transformation, $u_{\alpha}^{*}$ and $u_{\beta}^{*}$ are derived to switch H-bridges in phase A, B, and C with the 3-L SVM. By selecting the optimal redundant switching sequence from Eq. (3-4), aiming to minimize the voltage fluctuation in all three H -bridges capacitors, the voltages among three H -bridges capacitors can be balanced based on the real-time sampled H bridge capacitors voltages $v_{F C A}, v_{F C B}, v_{F C C}$ and converter AC output phase currents $i_{A}, i_{B}, i_{C}$.

### 3.4 Floating capacitors balancing region

### 3.4.1 Modulation index definition

To compare the proposed hybrid modulation with the conventional 7-L modulation strategy [3.2], the definition of the modulation index of the proposed hybrid modulation is the same as that of the 7-L SVM. A space vector diagram for a generic 7-L multilevel converter is shown in Figure 3-6. If the trajectory of the rotating reference vector is smaller than the inscribed circle of the outer hexagon in space vector diagram, i.e., the $\boldsymbol{V}_{\text {refl }}$ shown in Figure 3-6, the hybrid 7-L converter operates in the linear modulation region. The modulation index $(m)$ of the hybrid 7-L converter is defined as

$$
\begin{equation*}
m=\sqrt{3} \frac{\left|\boldsymbol{V}_{r e f}\right|}{U_{d c}} \tag{3-15}
\end{equation*}
$$

According to Figure 3-6 and Eq. (3-15), $\boldsymbol{V}_{\text {refl }}$ represents the maximum modulation index, which is 1.5 , for the hybrid $7-\mathrm{L}$ converter. The space vector diagram of a 3-L ANPC can be represented inside the dashed hexagon in (3-6), if the dc bus of the 3-L ANPC is also $U_{d c}$. Similarly, $\boldsymbol{V}_{\text {ref2 }}$ represents the maximum modulation index, i.e., $m=1$, for 3-L ANPC.


Figure 3-6 Generic space vector diagram of the 7-L converter.

### 3.4.2 Balancing region summary

The hybrid 7-L converter may have various stable operating ranges, i.e., whether the voltage balancing can be achieved across the floating capacitors, when using different modulation methods. For instance, the stable operating boundary of the hybrid 7-L converter under the conventional 7L SVM [3.2], i.e., the Boundary 1, is illustrated in Figure 3-7.

The floating capacitors voltages can be balanced in the region enclosed by the boundary and vice versa. However, when only using the hybrid modulation method, the 7-L converter can only operate with limited operating points, as shown by Points 2A in Figure 3-7. To extend the stable operating region, an active zero-sequence voltage (ZSV) [3.5] is injected into the original sinusoidal references in this work. With the injected ZSV, e.g., the $3^{\text {rd }}$ order signal, the Boundary 2B can be achieved, which as shown in Figure 3-7, is even wider than that of the conventional 7L SVM.


Figure 3-7 The comparison of the stable operating region using different modulation methods.

### 3.5 Simulation and scale-down experimental studies

To validate the effectiveness of the proposed hybrid modulation strategy, simulation studies in the MATLAB/Simulink and experimental studies on a hybrid 7-L converter prototype are performed. A three-phase resistive-inductive (RL) load, i.e., $R_{L}=10 \Omega$, and $L_{L}=4 \mathrm{mH}$ per phase,

Table 3-4 Parameters in the simulation and experiment studies.

| Parameters | Symbols | Values |
| :---: | :---: | :---: |
| dc-link voltage | $U_{d c}$ | 100 V |
| Neutral point capacitance | $C_{d c 1} / C_{d c 2}$ | $200 \mu \mathrm{~F}$ |
| dc floating capacitance in H-bridges | $C_{F C A} / C_{F C B} / C_{F C C}$ | $2200 \mu \mathrm{~F}$ |
| ac fundamental frequency | $f_{0}$ | 60 Hz |
| Switching frequency in 3-L SVM | $f_{s}$ | 20 kHz |
| Load PF | PF | 0.9888 |



Figure 3-8 Picture of the 7-L converter prototype.


Figure 3-9 The stable modulation boundaries.
with a power factor $(\mathrm{PF})$ of 0.9888 , is connected to the three AC output terminals of the hybrid converter. The system parameters are given in Table 3-4. Figure 3-8 shows the experimental setup of the hybrid 7-L converter. In the experiments, the main algorithm of the hybrid modulation is conducted in the dSPACE MicroLabBox, which is followed by an Intel Max-10 FPGA aiming to generate gating signals and dead time.

### 3.5.1 Comparison of $3^{\text {rd }}$ and 9 $^{\text {th }}$ injection methods

To investigate the switching point of the modulation index $(m)$ in the "Piecewise Selection" in Figure 3-5, the hybrid modulation strategy by separately adopting either the $3^{\text {rd }}$ or $9^{\text {th }}$ ZSV injection is simulated over the entire PF range, i.e., $0 \sim 1.0$. Figure 3-9 shows the stable operating boundaries of the hybrid 7-L converter under the conventional 7-L SVM [3.2] (Boundary 1), the proposed hybrid modulation with $3^{\text {rd }} \mathrm{ZSV}$ injection (Boundary 2 B ) and the proposed hybrid modulation with $9^{\text {th }}$ ZSV injection (Boundary 2C), respectively. It is obvious to observe that the proposed hybrid


Figure 3-10 THD of phase current when $3^{\text {rd }}$ and $9^{\text {th }}$ order ZSV are injected using the proposed hybrid modulation and the $7 \mathrm{~L}-\mathrm{SVM}$.
modulation with $3^{\text {rd }}$ order ZSV injection has the widest stable operating region, while the approach with $9^{\text {th }}$ order ZSV injection can only operate at a modulation index close to 1.0 .

Figure 3-10 shows the THD of phase current when $3^{\text {rd }}$ and $9^{\text {th }}$ order ZSV are injected in the experimental study by comparing with the conventional 7-L SVM. The phase current under $9^{\text {th }}$ order ZSV injection has smaller THD compared to that under $3{ }^{\text {rd }}$ order ZSV injection. Hence, to achieve the higher phase current quality and the larger balancing region, the $9^{\text {th }}$ order ZSV injection method is adopted in the region within Boundary 2C, and then $3^{\text {rd }}$ order ZSV injection method is adopted in the region between Boundary 2C and Boundary 2B in Figure 3-9.

### 3.5.2 Evaluated dynamic and steady performance

Figure 3-11 shows experimental steady-state performance of the hybrid 7-L converter when $m$ $=1.05$. As it can be seen, voltages across the NP capacitors $C_{d c 1}$ and $C_{d c 2}$ are both regulated at 50 V , and voltage across the three H -bridge floating capacitors are all regulated at 25 V , which are at their reference values. The converter line-to-neutral voltage and line-to-line voltage have 7 and 11


Figure 3-11 Steady-state performance when $m=1.05$; (a) converter AC output line-to-line voltage together with voltage across two neutral point capacitors and three H -bridge capacitors, as well as phase current; (b) converter AC output line-to-neutral voltage, ANPC AC output, H-bridge AC output, and hybrid converter common-mode voltage.
voltage levels, respectively. For Phase A, the converter line-to-neutral voltage, AC output voltage generated by ANPC, and AC output voltage generated by H-bridge are presented in Figure 3-11 (b). Since the LF modulation is applied to ANPC and 3-L SVM is applied in H-bridges, the ANPC switches at the fundamental frequency while the switching frequency of the H -bridge is much higher. A $3^{\text {rd }}$ order ZSV is injected in the hybrid modulation when $m=1.05$, as shown in the


Figure 3-12 Harmonics spectrum analysis of converter AC output (a) line-to-line voltage and (b) phase current when $m=1.05$.
common mode (CM) voltage waveform in Figure 3-11 (b). CM voltage is measured between neutral-point $(O)$ and the neutral point of star-connected three-phase load.

Figure 3-12 (a) and (b) show the harmonic spectra of the converter AC output line-to-line voltage and phase current, respectively. The harmonics caused by the switching in the hybrid converter are mainly concentrated around integral multiples of the switching frequency of the 3-L SVM.

Figure 3-13 shows the experimental waveforms of the transient-state performance of the hybrid converter when $m$ changes between 1.05 and 0.3 . Apparently, the voltages across all the dc floating capacitors during the transitions are always balanced, although there is a small voltage overshoot in the dc bus of the hybrid converter, which is caused by the response of dc power supply. In addition, the dynamic response of the ac output voltage and phase current is fast and without


Figure 3-13 Harmonics spectrum analysis of converter AC output (a) line-to-line voltage and (b) phase current when $m=1.05$.
undesired overshoot. In Figure 3-13, when the modulation index $m$ is 0.3 in the proposed hybrid modulation strategy, the converter AC output line-to-line voltage $u_{A B}$ is a stair-case waveform with 5-levels. Voltages across $C_{d c 1}$ and $C_{d c 2}$ are both regulated at 50 V , and voltages across the three $\mathrm{H}-$ bridge floating capacitors are all regulated at 25 V , which are at their corresponding references. When the $9^{\text {th }}$ order ZSV is injected ( $m=0.3$ ), the ANPC has the higher-frequency switching actions; when the $3^{\text {rd }}$ order ZSV is injected ( $m=1.05$ ), the ANPC has the lower-frequency switching actions; As a result, there is $9^{\text {th }}$ order component in the CM voltage.

Figure 3-14 presents the average switching frequency of the power switches in ANPC and Hbridges in the experiment, when the proposed hybrid modulation and conventional 7L SVM strategies are applied under various modulation indices. The average switching frequency is calculated by averaging the switching frequency of every power switch in ANPC and H-bridges, respectively. It can be concluded that the HF switching actions of the hybrid 7-L converter are


Figure 3-14 Average switching frequency of the devices in ANPC and H-bridges by using the proposed hybrid modulation and the conventional 7L SVM.


Figure 3-15 The maximum voltage fluctuation in DC floating capacitors by using the proposed hybrid modulation and the conventional 7L SVM.
completely transferred to H-bridges in the proposed method. Instead, ANPC devices switch at several kilohertz in the 7L SVM, which could induce high switching losses. Also, the average switching frequency in H -bridges when adopting the proposed method is slightly lower than when adopting the 7L SVM.

With the same circuit parameters shown in Table 3-4, Figure 3-15 shows comparison of the maximum voltage fluctuation across the floating capacitors $C_{d c 1}$ and $C_{F C A}$ when applying the proposed hybrid modulation and conventional 7-L SVM, as shown in Figure 3-15. The measurement is conducted when the converter reaches steady states under different modulation indices. The maximum voltage fluctuation $\Delta u_{\max }$ is defined as

$$
\begin{equation*}
\Delta u_{\max }=\left|u-u_{r e f}\right|_{\max } \tag{3-16}
\end{equation*}
$$

where $u$ is instantaneous capacitor voltage, $u_{r e f}$ is 50 V for $C_{d c 1}$ and 25 V for $C_{F C A}$.


Figure 3-16 Turnaround time comparison of the 7-L SVM [3.2] and the proposed hybrid modulation.

Figure 3-15 shows that the conventional 7L SVM has smaller voltage fluctuation in floating capacitors due to its more frequent switching actions as illustrated in Figure 3-14. Although there is a larger voltage fluctuation across DC-bus capacitors caused by the LF modulation when applying the proposed hybrid modulation, the converter still operates well according to the experimental results.

### 3.5.3 Computational efficiency analysis

To demonstrate the computational burden reduction of the proposed hybrid modulation, both the conventional 7-L SVM [3.2] and the proposed hybrid modulation are implemented at 20 kHz , which means the execution time of the strategies in every control iteration cannot exceed $50 \mu \mathrm{~s}$. The turnaround time of the two methods is measured in the dSpace real-time mode. Figure 3-16 exhibits the turnaround time of the two methods when the modulation index is 1.02 . As can be seen, the turnaround time of the conventional 7-L SVM strategy presented in [3.2] and the proposed hybrid modulation strategy are $25.6 \mu \mathrm{~s}$ and $16.9 \mu \mathrm{~s}$, respectively. There is over $30 \%$ turnaround time reduction when applying the proposed hybrid modulation strategy.

### 3.6 Case study on 1-MVA MV prototype

To further highlight advantages of the proposed hybrid modulation in terms of loss reduction and current quality improvement, various case studies are performed on an MV prototype as shown


Figure 3-17 Experimental waveform of the prototype when operated at dc 3 kV with the proposed hybrid modulation.


Figure 3-18 Experimental waveform of the IGBT-based ANPC when operated at dc 3 kV with SPWM at 2 kHz switching frequency.


Figure 2-2, where the three-phase ANPC converter is constructed using 3.3 kV half bridge modules from Infineon, i.e., FF450R33T3E3, and HB converters are built using 1.7 kV SiC module samples from Wolfspeed, i.e., HT-3234-R-VB. Figure 3-17 shows the typical experimental converter line-to-line output voltage and ANPC converter output voltage waveform,

(a)

(b)

Figure 3-19 Harmonics spectrum analysis of ac output line-to-line voltage of (a) the hybrid converter and (b) ANPC converter with 2 kHz switching frequency.
when dc bus is 3 kV and modulation index 0.85 is applied in the prototype test. As comparison, Figure 3-18 shows the typical experimental waveforms of the ANPC using 3.3kV IGBT, where the line-to-line output voltage and three phase currents are presented. The test is also performed when the dc bus is 3 kV and carrier frequency of the sinusoidal pulse width modulation (SPWM) is 2 kHz .

The harmonics spectra of line-to-line voltage shown in Figure 3-17 and Figure 3-18 are provided in Figure 3-19 (a) and (b), respectively. Due to the use of hybrid Si/SiC topology and the proposed hybrid modulation approach, the harmonics are shifted to HF range in the hybrid converter compared to all-Si ANPC converter.

(b)

Figure 3-20 Overall flowcharts of loss model for (a) MOSFET and (b) IGBT.

In addition, the following three scenarios were considered to compare the performance of the hybrid converter with that of the ANPC converter in terms of system efficiency and THD, which includes 1) the 3.3 kV IGBT-based ANPC converter switching with the SPWM at 1 kHz switching frequency, 2) the 3.3 kV IGBT-based ANPC converter switching at 2 kHz switching frequency, and 3) the $\mathrm{Si} / \mathrm{SiC}$ hybrid 7 -L converter using the proposed hybrid modulation.

In all the case studies, 0.99 load PF is used with modulation index, defined in Eq. (3-15), equaling to 1 for cases 1) and 2) and 1.05 for case 3 ). The loss model is developed based on the method proposed in [3.6] and is implemented in MATLAB/Simulink. The flowcharts of the average loss calculation over one fundamental cycle for the MOSFET and IGBT are shown in Figure 3-20 (a) and (b), respectively. By extracting switching energy information from the datasheet of the modules, pre-defined look-up tables are used in the loss model to determine the switching losses. When calculating the IGBT conduction loss, a lookup table is also used to determine the collector-emitter voltage.

### 3.7 Conclusions

This chapter presents a hybrid modulation strategy with reduced complexity and fixed switching frequency for a hybrid 7-L ANPC-H converter, which adopts a simple 3-L SVM for the LV H-bridge stage and a simple LF modulation for the HV ANPC stage. By adopting a ZSV injection method, regulating the threshold of the LF modulation for ANPC stage and selecting the optimal switching sequence in 3-L SVM for H-bridges, all floating dc capacitors are well balanced not only in steady-state but also in transient-state. Thanks to the fact that most of the switching actions in the proposed hybrid modulation strategy are distributed to the LV H-bridge stage rather than the high-voltage ANPC stage, the power losses are significantly reduced. Comprehensive
simulation and experimental studies on both the scale-down and full-scale hybrid 7-L converter prototypes are presented to validate the effectiveness of the proposed hybrid modulation.

### 3.8 Reference

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## CHAPTER 4

## MULTILEVEL CONVERTER WITH INTERNAL PARALLELED STRUCTURE

### 4.1 Topology and the implemented prototype

### 4.1.1 Basic topology configuration

The topology of hybrid 5-L ANPC converter with internal paralleled structure is shown in Figure 4-1, which has two dc floating capacitors in series connection to form dc bus $U_{d c}$. There are eight switch positions $S_{1} \sim S_{8}$ in each phase of the hybrid 5-L ANPC converter, and $S_{5}$ half-bridge and $S_{7}$ half-bridge are interleaved by high frequency inductors to generate the ac terminal of each phase.

The converter can generate five output voltage levels when dc voltages across two floating capacitors are equal to $U_{d c} / 2$. The five output voltage levels are $U_{d c} / 2, U_{d c} / 4,0,-U_{d c} / 4,-U_{d c} / 2$, respectively, when the five switching states are applied in the 5-L hybrid ANPC converter based on Table 4-1. According to switching states summary, $S_{1}$ half-bridge and $S_{3}$ half-bridge can work with fundamental frequency to reduce switching losses, where $S_{5}$ half-bridge and $S_{7}$ half-bridge


Figure 4-1 The five-level hybrid ANPC converter topology.

Table 4-1 Switching states of the hybrid 5-L ANPC converter.

| Switching <br> states | $\boldsymbol{S}_{\mathbf{1}}$ <br> $\left(\overline{\boldsymbol{S}_{\mathbf{2}}}\right)$ | $\boldsymbol{S}_{\mathbf{3}}$ <br> $\left(\overline{\boldsymbol{S}_{\mathbf{4}}}\right)$ | $\boldsymbol{S}_{\mathbf{5}}$ <br> $\left(\overline{\mathbf{S}_{\mathbf{6}}}\right)$ | $\boldsymbol{S}_{\mathbf{7}}$ <br> $\left(\overline{\boldsymbol{S}_{\mathbf{8}}}\right)$ | $\boldsymbol{U}_{\boldsymbol{A 1 O}}$ | $\boldsymbol{U}_{\boldsymbol{A 2} \boldsymbol{O}}$ | $\boldsymbol{i}_{\boldsymbol{O} \boldsymbol{A}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 1 | 1 | 1 | $U_{d c} / 2$ | $U_{d c} 2$ | 0 |
| $3\left(U_{d c} / 4\right)$ | 1 | 1 | 1 | 0 | $U_{d c} / 2$ | 0 | $i_{A 2}$ |
|  | 1 | 1 | 0 | 1 | 0 | $U_{d c} / 2$ | $i_{A 1}$ |
| $2(0)$ | 1 | 1 | 0 | 0 | 0 | 0 | $i_{A 1}+i_{A 2}$ |
|  | 0 | 0 | 1 | 1 | 0 | 0 | $i_{A 1}+i_{A 2}$ |
| $1\left(-U_{d c} / 4\right)$ | 0 | 0 | 1 | 0 | 0 | $-U_{d c} / 2$ | $i_{A 1}$ |
|  | 0 | 0 | 0 | 1 | $-U_{d c} / 2$ | 0 | $i_{A 2}$ |
| $0\left(-U_{d c} / 2\right)$ | 0 | 0 | 0 | 0 | $-U_{d c} / 2$ | $-U_{d c} / 2$ | 0 |

work with high frequency to allow 5-L hybrid ANPC converter ac terminal outputs high performance ac generated voltage. Hence, $\mathrm{S}_{1} \sim \mathrm{~S}_{4}$ in the converter are low-frequency (LF) switches implemented using Si IGBTs, and $\mathrm{S}_{5} \sim \mathrm{~S}_{8}$ are high-frequency (HF) switches implemented by SiC MOSFETs. With this hybrid "Si+SiC" assembly, system overall losses could be optimized while maintaining cost-effectiveness.

### 4.1.2 The developed MV 5-L hybrid ANPC converter prototype

With above-mentioned hybrid "Si+SiC" assembly solution, half-bridge Si IGBT power modules and H-bridge (full-bridge) SiC MOSFET power modules are used to construct a MV 5L hybrid $\mathrm{Si} / \mathrm{SiC}$ ANPC converter protype with topology shown in Figure 4-1. The half-bridge Si IGBT power module is Infineon's 3.3 kV half-bridge IGBT power module FF450R33T3E3 [4.1], as shown in Figure 4-2, which is used as the low frequency Si half-bridge module in topology. The compact custom 3.3 kV SiC MOSFET H-bridge power module shown in Figure 4-3 is used as the high frequency H -bridge cell in topology. The length, width, and height of the custom 3.3 kV SiC MOSFET H-bridge power module are 95 mm , 55 mm , and 18 mm , respectively. In sum, two Si


Figure 4-2 Infineon Si IGBT half-bridge module.


Figure 4-3 Customized SiC MOSFET H-bridge module.

IGBT modules and one SiC MOSFET module are required in each phase of the $5-\mathrm{L}$ hybrid $\mathrm{Si} / \mathrm{SiC}$ ANPC converter prototype.

Figure $4-4$ shows the layout of the custom 3.3 kV SiC MOSFET H-bridge power module. There are four switch positions to form H -bridge circuit inside the customized SiCH H -bridge module, and each switch position is implemented by using the 3.3 kV 50 A bare die (PM3-3300-0040) from CREE. In the layout design, symmetrical layout is adopted between half bridges with the purposes of identical thermal distribution and parasitic. In the fabrication process, 3.3 kV Isolation is reinforced by enough clearance and creepage distances ( 11 mm ) between power terminals.

The fabrication process is illustrated as Figure 4-5. In the the custom 3.3 kV SiC MOSFET Hbridge power module, aluminum nitride (AIN) based direct bonding coppers (DBCs) are utilized


Figure 4-4 Layout of the 3.3 kV H -bridge SiC MOSFET power module.


Figure 4-5 Fabrication process of the customized 3.3 kV H -bridge SiC MOSFET power module.
as substrates. An aluminum silicon carbide (AlSiC) base plate is used as heatsink. Dies are first attached on DBC substrates by SST 3130 Vacuum furnace. Al wires are then bonded for dies and copper traces connection, and copper terminals are attached by SIKAMA Falcon 5 reflow oven. Housing is finally attached to module. Passivation is formed by encapsulating in silicone gel Sylgard 184.

With the above-mentioned half-bridge Si IGBT power module and H -bridge (full-bridge) SiC MOSFET power module, a MV 5-L hybrid $\mathrm{Si} / \mathrm{SiC}$ ANPC converter protype is constructed. Figure 4-6 shows the picture of the established MV 5-L hybrid $\mathrm{Si} / \mathrm{SiC}$ ANPC converter protype, consisting of above-mentioned power modules, customized gate drivers, busbars, and commercial


Figure 4-6 The prototype of an MV 5-L Si/SiC hybrid ANPC converter with internal paralleled structure.
high frequency inductors. To enhance EMI immunity, fiber optics are integrated on all gate drivers for receiving switching, enabling/disenabling signals and sending false protection feedback signals to digital controllers. It is noted that Si IGBTs and its de busing including busbars and dc capacitors are the reuse of 7-L ANPC-H hybrid converter prototype mentioned in previous chapters, for the purpose of fast prototyping and validating. Because low stray-inductance and high-current baring dc bussing design has been illustrated in chapter 2, it is not repeated here. As shown in Figure 4-6, the ac bussing is designed to connect two half-bridge Si IGBT modules and one customized H bridge SiC MOSFET power module in each phase of the 5-L hybrid ANPC converter. For fast prototyping and validating, the ac bussing is implemented by laminated heavy copper printed circuit board (PCB). As shown in Figure 4-6, six high frequency inductors are within the MV 5-L


Figure 4-7 DPT testing circuit setup.
hybrid $\mathrm{Si} / \mathrm{SiC}$ ANPC converter protype. In prototype, two inductors are in interleaved connection in each phase as shown in Figure 4-1.

### 4.1.3 Loss data extraction of customized SiC module

In the customized H -bridge SiC MOSFET power module, short power- and gate-loops are designed for lower parasitic. According to ANSYS Q3D extraction, power-loop stray inductance is only 11.9 nH , high and low side gate-loops parasitic inductances are 8.65 nH and 8.73 nH , respectively. To validate the low parasitic loop design and extract loss data of the customized SiC power module, double pulse test (DPT) is performance for the custom 3.3 kV SiC MOSFET module at 1.5 kV dc and $5 \Omega$ external gate resistance, with setup shown in Figure 4-7.

In DPT testing, the dc link connected to the SiC power module is 1.5 kV . By applying different pulse widths, the switching performance is logged when SiC switching position is turn-on and turn-off at different device drain-to-source currents. Figure 4-8 shows a typical waveform for SiC


Figure 4-8 Typical DPT testing waveform.


Figure 4-9 Switching energy versus switch position drain-to-source current.
device turning-off at 1.5 kV dc link and 40 A drain-to-source current. At 40 A turn-off, device voltage overshoot is 171 V , ringing frequency is 43.6 MHz and $\mathrm{dv} / \mathrm{dt}$ is $52.3 \mathrm{~V} / \mathrm{ns}$.

With logged data from multiple DPTs, Figure 4-9 summarizes the extracted switching energy for turn-on/off, i.e., $\mathrm{E}_{\text {on }}$ and $\mathrm{E}_{\text {off, }}$, versus different drain-to-source current of each switch position within the customized SiC power module.

### 4.2 MV prototype proof-of-concept validation

### 4.2.1 Modulation scheme

Figure 4-12 illustrates the working principle of carrier-based modulation for the $5-\mathrm{L} \mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter. Due to interleaving configuration, the converter phase-leg outputs five voltage levels and doubles the high frequency cell's switching frequency in the converter output voltage.

### 4.2.2 $\quad$ Simulation studies

Using the loss information from the Si IGBT module datasheet [4.1] and loss data of SiC module shown in Figure 4-9, converter system efficiency can be estimated by simulation model with loss data extrapolation. When SiC MOSFETs switch at 50 kHz , i.e., with 100 kHz equivalent switching frequency in the output voltage, Figure 4-11 shows the estimated converter efficiency curve under 2 kV dc-link, where peak efficiency is $98.7 \%$ at 50 kW . Please note, the maximum


Figure 4-10 Working principle of the basic modulation scheme.


Figure 4-11 Efficiency estimation of the 5-L hybrid converter prototype.


Figure 4-12 Converter losses distribution.
power is limited by the SiC module, since it has only one die per switching position. Figure 4-12 provides converter loss distribution among Si and SiC devices.

### 4.2.3 Experimental studies

Figure 4-13 and Figure 4-14 show typical experimental waveforms of converter phase-leg voltage output and current output, when dc bus voltage is 2 kV , HF SiC devices switch at 50 kHz , LF Si IGBTs switch at 60 Hz . Each SiC half-bridge ac terminal outputs 3-L voltage, and phase-


Figure 4-13 Converter voltage waveforms under overall switching frequency 100 kHz .


Figure 4-14 Converter current waveforms under overall switching frequency 100 kHz .
leg equivalent ac output voltage is $5-\mathrm{L}$ because of the inner-interleaved configuration. Due to the interleaving configuration within one phase-leg with the phase-shifted PWM modulation, switching ripples in two HF inductors cancel mutually, such that phase-leg output current $i_{A}$ is almost ripple-free.


Figure 4-15 Harmonics spectrum of $u_{A 1 O}$ under overall switching frequency 100 kHz .


Figure 4-16 Harmonics spectrum of $u_{A O}$ under overall switching frequency 100 kHz .

Figure 4-15 and Figure $4-16$ show harmonics spectrum of $u_{A 1 O}$ and $u_{A O}$, respectively. According to harmonics spectrum of converter ac output voltage $u_{A O}$, converter switching frequency is concentrated to 100 kHz .

### 4.3 Conclusions

This work presents a hybrid 5-L ANPC converter design and implementation with low frequency Si-IGBTs and high frequency SiC MOSFETs, where inner-interleave is configurated for high frequency cells. To the best of authors' knowledge, this is the first reported MV prototype for the present topology. Simulation and experimental validate converter performance, and converter is power efficient at 100 kHz converter switching frequency.

### 4.4 Reference

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## CHAPTER 5

## HYBRID MULTILEVEL CONVERTER ADVANTAGES SUMMARY

In this chapter, the protypes of multilevel converter with internal cascaded structure, i.e., 7-L $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC-H converter, multilevel converter with internal parallel structure, i.e., $5-\mathrm{L}$ $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter, and the conventional 3-L ANPC converter are discussed and compared. By discussing their ease-of-implementation, cost, dc voltage utilization, floating capacitors balancing region, converter power efficiency, and common-mode voltage, both the advantages and disadvantages of the established multilevel converter prototypes are demonstrated and summarized.

### 5.1 Ease-of-implementation and cost

The prototyping of the 3-L ANPC, 7-L Si/SiC hybrid ANPC-H converter and 5-L Si/SiC hybrid ANPC converter are illustrated in previous chapters. Prototyping is implemented by applying PEBB concept, because PEBB concept has merits of fast prototyping, modularity, ease-of-implementation/maintenance which could provide essential cost-effectiveness merits. Hence, all the three prototypes are easy-to-implement.

When compared to 3-L ANPC, the 7-L hybrid ANPC-H converter requires one more H -bridge PEBB in each phase. If 3-L ANPC and ANPC stage in 7-L hybrid converter adopt the same devices, 7-L hybrid converter consumes more cost in construction/maintenance. However, when all-Si switches are adopted in ANPC stage of 7-L hybrid converter, the construction/maintenance cost for 7-L hybrid converter might not be expensive than an all-SiC 3-L ANPC, if the two converters are designed with the same MV dc bus voltage requirements. It is because the MV scale SiC power module is still more expensive than the MV Si power modules.

When compared to 3-L all-Si ANPC, 5-L Si/SiC hybrid ANPC converter could be seen as replacing a 3.3 kV Si half-bridge to a 3.3 kV SiC H -bridge in each phase. The 3.3 kV SiC H -bridge module reported in this work is fabricated within the laboratory, so it is difficult to foresee its marketing cost. Based on SiC marketplace, the MV scale SiC module is still more expensive than Si module, such that $5-\mathrm{L} \mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter is predicted to cost more than all- Si ANPC. However, when comparing to all-SiC 3-L ANPC adopting, it is still promising for the $5-\mathrm{L}$ $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter to have the lower cost.

### 5.2 DC voltage utilization

By considering the same modulation index definition as Eq. (2-28), the dc voltage utilization of 3-L ANPC, 7-L ANPC-H and 5-L hybrid ANPC converter are discussed when they have the same de bus voltage. When modulation index reaches 1, both 3-L ANPC and 5-L hybrid ANPC converter achieve their maximum dc voltage utilization, defined as $100 \%$ of dc bus voltage. Note, only linear modulation region is considered in this work and overmodulation region is not discussed. Compared to 3-L ANPC and 5-L hybrid ANPC converter, the 7-L ANPC-H converter has three more H-bridge PEBBs with dc floating capacitors. Attributed to dc volage charged in those dc floating capacitors, 7-L ANPC-H converter ac output voltage could be larger than dc bus voltage. With this advantage, 7-L ANPC-H converter has 1.5 times larger dc voltage utilization than 3-L ANPC and 5-L hybrid ANPC converter, according to discussions in previous chapters.

### 5.3 Floating capacitors balancing region

By applying different modulation strategies, the floating capacitors balancing region for 7-L ANPC-H converter is given as Figure 3-9. According to it, the dc floating capacitors can balance when modulation index is within 1 for full power factor region. Similarly, the dc floating capacitors in conventional 3-L ANPC and 5-L hybrid ANPC converter can also balance when modulation
index is within 1 for full power factor region. Because 7-L ANPC-H converter have higher dc bus voltage utilization, the dc floating capacitors balancing region is investigated as shown in Figure 3-9. As can be seen, dc floating capacitors in 7-L ANPC-H converter can balance in certain region regarding of the modulation index and power factor. Hence, 7-L ANPC-H converter has the advantage of high dc bus voltage utilization, but it is limited to certain floating capacitor balancing region when modulation index exceeds 1 .

### 5.4 Power conversion performance

To demonstrate the advantage of hybrid multilevel converter, the 7-L hybrid ANPC-H converter is taken as an example for comparison with 3-L ANPC.

### 5.4.1 Voltage output evaluation and CMV

To reveal the advantage of the 7-L hybrid ANPC-H converter regarding output power quality including THD and common-mode voltage, the 3-L ANPC is simulated for comparison with 3 kV dc link as well. The modulation index used in the simulation is 0.61 , which can theoretically generate approximately 1.8 kV ac line voltage. For ensure a fair comparison, the ac output line voltage and common-mode voltage of 7-L hybrid converter under the same modulation index is given as Figure 5-1(a) with its harmonic spectrum exhibited. Figure 5-1 (b) shows ANPC ac line voltage and common-mode voltage waveforms and line voltage spectrum when applying 2 kHz switching frequency. Figure 5-1(c) shows the corresponding results when ANPC applying 6 kHz switching frequency, since ANPC devices average switching frequency is also around 6 kHz in $7-$ L ANPC-H converter shown in Figure 5-1(b). The THD values of the three cases are $25.3 \%$, $44.87 \%, 44.91 \%$, respectively. According to the comparison results with 3-L ANPC, the hybrid 7L converter generates far less harmonics and lower common-mode voltage when they both output the same ac line voltage fundamental peak. Furthermore, the voltage differences between adjacent


Figure 5-1 Line voltage, CMV and line voltage harmonics spectrum of (a) 7-L ANPC-H without CMV reduction scheme, (b) 7-L ANPC-H with CMV reduction scheme applied, (c) 3-L ANPC with 2 kHz switching frequency and (d) 3-L ANPC with 6 kHz switching frequency.
voltage levels in Figure 5-1(a) and (b) are 750 V and 1500 V , respectively, demonstrating 7-L hybrid converter has smaller $d v / d t$ caused by the ac output line voltage. It should be noted that the


Figure 5-2 Comparison of the three studied cases: (a) converter efficiency vs. load power; (b) THD of converter phase output current vs. load power; (c) losses breakdown of the 0.5 MW converter power case.
smaller $d v / d t$ induces less electromagnetic interface (EMI) issues especially for some harsh conditions.

### 5.4.2 Power efficiency

The comparison of the converter efficiency among the three cases is presented in Figure 5-2(a), where hybrid 7-L converter has the highest efficiency. It should be noted that factors such as the deadtime and body diode loss are not considered in the loss model in this work, because the switching loss and conduction loss are dominant in the medium to heavy load region. However, this may lead to overestimated efficiency in the light load region.

The THD of the converter phase output current in the three cases are presented in Figure 5-2(b), where the 7-L hybrid converter has much lower THD than the other two cases. Note that there is trade-off between losses and power efficiency for Si-IGBT based ANPC, hence in practice, Si based converter output current quality is limited by low switching frequency. Figure 5-2(c) presents the switching loss and conduction loss break down of the three cases, when the converters operate at 0.5 MW . With the hybrid modulation adopted in the $\mathrm{Si} / \mathrm{SiC} 7-\mathrm{L}$ hybrid converter, the HF switching actions are mostly assigned to the SiC MOSFETs, such that the 7-L hybrid converter has the lowest switching losses. The 7-L hybrid converter operates with slightly higher modulation index than the ANPC, accordingly, its converter phase current is smaller when the same power rating is applied. Therefore, the 7-L hybrid converter in Figure 5-2(c) has the lowest conduction losses. In summary, the 7-L hybrid converter has superior efficiency and current quality.

### 5.5 Summary

Figure 5-3 compares the figure of merit of the 7-L ANPC-H converter and the conventional 3L ANPC converter implemented by 3.3 kV Si-IGBTs. The dc voltage utilization of 3-L ANPC and 7-L ANPC-H converter is 1 and 1.5 , respectively, such that the present 7-L converter has much higher dc voltage utilization. To achieve the same converter ac output voltage THD, 7-L converter could generate less loss than 3-L converter because its switching actions are largely distributed to 1.2 kV low-voltage SiC H -bridge stages. Hence, 7-L converter could achieve higher power efficiency than 3-L IGBT implemented ANPC. Attributed to 7-level voltage output, 7-L converter has much smaller $\mathrm{dv} / \mathrm{dt}$ in converter voltage output than 3-L converter, hence 7-L converter could have the less EMI issue and better output voltage quality than 3-L converter. The 7-L converter can have less CMV compared with the 3-L converter. Although the IGBT based 3-L ANPC has


Figure 5-3 Comparison of 7-L ANPC-H converter and 3-L ANPC converter.
lower cost than the presented 7-L converters with three kinds of ANPC PEBBs, the ac passive filtering and/or EMI filtering can be much simplified when using the proposed 7-L converter solution leading to higher power density and cost reduction at system level.

Based on above illustrations, Table 5-1 describes the general comparison among the discussed multiple topologies, including 3-L ANPC converter, 7-L hybrid ANPC-H converter, and 5-L hybrid ANPC converter. In each topology, both all-Si, all-SiC and/or $\mathrm{Si} / \mathrm{SiC}$ hybrid configurations are discussed. The discussed performance aspects include ease to implement, cost savings, dc voltage utilization, FC capacitor balancing region, dv/dt reduction, power efficiency, CMV reduction, and output voltage quality. Generally, the 7-L ANPC-H and 5-L ANPC converters with both $\mathrm{Si} / \mathrm{SiC}$ device-level and topology-level hybrid configuration, have superior overall performance than 3-L ANPC especially regarding cost-effectiveness and improved power output performance.

Table 5-1 General comparison among multiple topologies.

| Performance <br> aspects | 3-L ANPC |  | 7-L hybrid ANPC-H |  | 5-L hybrid <br> ANPC |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | All-Si <br> 3.3 kV | All-SiC <br> 3.3 kV | ANPC- Si 3.3 kV <br> $\mathrm{HB}-\mathrm{SiC} 1.2 \mathrm{kV}$ | ANPC-SiC3.3kV <br> HB- SiC 1.2 kV | All-SiC <br> 3.3 kV | $\mathrm{Si}+\mathrm{SiC}$ <br> 3.3 kV |
| Ease to <br> implement | good | good | good | good | good | good |
| Cost saving | good | poor | fair | poor | poor | fair |
| DC voltage <br> utilization | fair | fair | good | good | fair | fair |
| FC capacitor <br> balance region | full | full | specific | specific | full | full |
| dv/dt reduction | poor | poor | good | good | fair | fair |
| Power <br> efficiency | poor | fair | fair | good | good | fair |
| CMV reduction | poor | poor | good | good | - | - |
| Output voltage <br> quality | poor | poor | good | good | fair | fair |

### 5.6 Conclusions

In this chapter, the 7-L Si/SiC hybrid ANPC-H converter, $5-\mathrm{L} \mathrm{Si} / \mathrm{SiC}$ hybrid converter and the conventional 3-L ANPC converter are compared and discussed, in terms of their ease-ofimplementation, cost, dc voltage utilization, floating capacitors balancing region, converter power efficiency, and common-mode voltage. Basically, 3-L ANPC has the best cost-effective due to lowest number of switching positions, however, 7-L Si/SiC hybrid ANPC-H converter and 5-L $\mathrm{Si} / \mathrm{SiC}$ hybrid converter could achieve high performance such as lower $\mathrm{dv} / \mathrm{dt}$, reduced CMV, better power efficiency profile, and improved output harmonics spectrum under MV scale applications.

## CHAPTER 6

## CONCLUSIONS AND FUTURE WORK

### 6.1 Conclusion

MV-scale dc distribution is a promising trend for the next-generation MV electric aircraft propulsion applications, and power converter compatible with MV operations is one of the key technologies for implement high-performance and lightweight electric aircraft. This work investigates hybrid multilevel converters with internal cascaded and internal paralleled structures, i.e., a hybrid 7-L ANPC-H converter and a 5-L Si/SiC hybrid converter, for MV electric aircraft propulsion applications.

Firstly, to demonstrate hybrid multilevel converter with internal cascaded structure, a hybrid 7-L ANPC-H converter prototype system with 3 kV dc bus is implemented by ANPC PEBBs with 3.3 kV Si and/or SiC devices and H -bridge PEBBs with 1.2 kV SiC devices, the established 7-L ANPC-H converter demonstrates the MW-scale prototyping feasibility with hybrid converter concepts. Both the conventional SVM and a computational efficient SVM are implemented to modulate the hybrid 7-L ANPC-H converter prototype, where the computational efficient SVM can effectively lower the design and calculation complexity. Also, an active hybrid modulation strategy with reduced complexity and fixed switching frequency is proposed for a hybrid 7-L converter, which adopts a simple 3-L SVM for the low-voltage H -bridge stage and a simple lowfrequency modulation for the high-voltage ANPC stage. Simulation and experimental validate converter performance and converter efficiency improvement.

Secondly, to demonstrate hybrid multilevel converter with internal paralleled structure, an MV hybrid 5-L ANPC converter is designed and implementation with low frequency Si IGBTs and high frequency customized SiC MOSFETs, where inner-interleave is configurated for high
frequency cells. To the best of authors' knowledge, this is the first reported MV prototype for this present topology. Simulation and experimental validate converter performance, and converter is power efficient at 100 kHz converter switching frequency.

Finally, the general comparison study is conducted in this work to demonstrate the advantages and disadvantages of the hybrid multilevel converters with internal cascaded and internal paralleled structures. Both two solutions have advantages of modularity, ease-of-implementation, high power efficiency, high performance in ac output harmonics and $\mathrm{dv} / \mathrm{dt}$, and common-mode voltage reduction capability. The major defect of hybrid multilevel converters with internal cascaded structure might include the limited dc floating capacitor balancing region when modulation index is above 1. And the major defect of hybrid multilevel converters with internal paralleled structure might include the requirement of external high frequency inductors, however, it is still promising that the wiring between power converter and electric machine could provide inductance and external high frequency inductors could be avoided to save cost.

### 6.2 Future work

The dissertation has conducted some proof-of-concept investigation of the hybrid multilevel converters with internal cascaded and paralleled structures, demonstrated for next-generation ac propulsion with MV dc distribution system. Both the MV prototypes for the two topologies, i.e., hybrid 7-L ANPC-H converter and a 5-L Si/SiC hybrid ANPC converter, have been established and validated by experimental tests. The functionalities of the two prototypes are validated with some typical testing scenarios to mimic the real applications, however, some future work could be conducted to fully validate converters' performance and improve both hardware and control design to improve performance. Several plans for future work are listed below.

Firstly, in 5-L Si/SiC hybrid ANPC converter, the external HF inductors are considered as ideal inductance, their mutual coupling inductance has not been considered in the control loop. Also, the two external inductors could have non-negligible inductance mismatch, which could cause current not evenly distributed between two paralleled loops. One of the merits of this converter is the high frequency harmonics caused by switching can be mutually mitigated within two paralleled loops per phase. The future work for it could be modeling and proposing control methods to optimize harmonics cancelling under parameters mismatch.

Secondly, hybrid 7-L ANPC-H converter and a 5-L Si/SiC hybrid ANPC converter are only validated by resistive-inductor load to fundamentally mimic ac propulsion applications. However, there are still differences between ideal resistive-inductor load and real ac electric machine. The future work related to this topic is to validate the converters loaded with ac electric machines under high-fidelity simulation environment for fully validation.

Thirdly, because the demonstrated converters design is proposed for electric aircraft, the high reliability and altitude-based dielectric strength are essential topics for industrial applications. The future work for these topics could be investigating redundancy plans for power converter backup and some typical estimation of dielectric strength within prototypes under different altitudes.

Except for the above-mentioned research and testing plans, there are also some expectations of these two converters to seek for more broad applications portfolios. For instance, hybrid 7-L ANPC-H is also promising in scenarios with high voltage electric machines but with low-voltage dc source, because ac output voltage in this topology could be boosted compared to dc voltage. Also, 5-L $\mathrm{Si} / \mathrm{SiC}$ hybrid ANPC converter is promising for ac propulsion of multi-segment generators or motors whose ac windings are usually isolated.

```
APPENDIX
This appendix shows the MATLAB code used for plotting some typical curves in figures of this dissertation. These codes allow readers to input data into MATLAB and redraw the curves or use the data for other calculations and deductions purposes.
Plotting of Figure 4-11:
```

```
P=1000*[5 10 15 20 25 30 3540 45 50];%kW
```

P=1000*[5 10 15 20 25 30 3540 45 50];%kW
ANPCLoss=12*[2.6 3.25 4 4.9 5.75 6.6 7.55 8.5 9.5 10.6];
ANPCLoss=12*[2.6 3.25 4 4.9 5.75 6.6 7.55 8.5 9.5 10.6];
HLoss=12*[38 39 39 39 39.540 41 43 45 47];
HLoss=12*[38 39 39 39 39.540 41 43 45 47];
TotalLoss=[490 504 515 524 532545 567595 625 657];
TotalLoss=[490 504 515 524 532545 567595 625 657];
ConvEfficiency=(P-TotalLoss)./P;
ConvEfficiency=(P-TotalLoss)./P;
plot(P,ConvEfficiency,'o-');
plot(P,ConvEfficiency,'o-');
grid on
grid on
xlabel('power rating (W)')
xlabel('power rating (W)')
ylabel('Efficiency (%)')
ylabel('Efficiency (%)')
title('Converter Efficiency Curve')
title('Converter Efficiency Curve')
Plotting of Figure 4-12:

```
```

P=1000*[5 10 15 20 25 30 3540 45 50];%kW

```
P=1000*[5 10 15 20 25 30 3540 45 50];%kW
ANPCLoss=12*[2.6 3.25 4 4.9 5.75 6.6 7.55 8.5 9.5 10.6];
ANPCLoss=12*[2.6 3.25 4 4.9 5.75 6.6 7.55 8.5 9.5 10.6];
HLoss=12*[38 39 39 39 39.540 41 43 45 47];
HLoss=12*[38 39 39 39 39.540 41 43 45 47];
TotalLoss=[490 504 515 524 532545 567595 625 657];
TotalLoss=[490 504 515 524 532545 567595 625 657];
ConvEfficiency=(P-TotalLoss)./P;
ConvEfficiency=(P-TotalLoss)./P;
subplot(122)
subplot(122)
plot(P,ANPCLoss,'o-');hold on
plot(P,ANPCLoss,'o-');hold on
plot(P,HLoss,'s-');hold on
plot(P,HLoss,'s-');hold on
plot(P,TotalLoss,'d-');
plot(P,TotalLoss,'d-');
grid on
grid on
xlabel('power rating (W)')
xlabel('power rating (W)')
ylabel('Loss (W)')
ylabel('Loss (W)')
title('Loss Distribution')
```

title('Loss Distribution')

```
```

