ABSTRACT

Title of Dissertation: SURFACE INSULATION RESISTANCE DEGRADATION AND ELECTROCHEMICAL MIGRATION ON PRINTED CIRCUIT BOARDS

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Widespread adoption of lead-free materials and processing for printed circuit board (PCB) assembly has raised reliability concerns regarding surface insulation resistance (SIR) degradation and electrochemical migration (ECM). As PCB conductor spacings decrease, electronic products become more susceptible to these failures mechanisms, especially in the presence of surface contamination and flux residues which might remain after no-clean processing. Moreover, the probability of failure due to SIR degradation and ECM is affected by the interaction between physical factors (such as temperature, relative humidity, electric field) and chemical factors (such as solder alloy, substrate material, no-clean processing).

Current industry standards for assessing SIR reliability are designed to serve as short-term qualification tests, typically lasting 72 to 168 hours, and do not provide a prediction of reliability in long-term applications. The risk of electrochemical migration with lead-free assemblies has not been adequately investigated. Furthermore, the mechanism of electrochemical migration is not completely

understood. For example, the role of path formation has not been discussed in previous studies. Another issue is that there are very few studies on development of rapid assessment methodologies for characterizing materials such as solder flux with respect to their potential for promoting ECM.

In this dissertation, the following research accomplishments are described: 1). Long-term temp-humidity-bias (THB) testing over 8,000 hours assessing the reliability of printed circuit boards processed with a variety of lead-free solder pastes, solder pad finishes, and substrates. 2). Identification of silver migration from Sn3.5Ag and Sn3.0Ag0.5Cu lead-free solder, which is a completely new finding compared with previous research. 3). Established the role of path formation as a step in the ECM process, and provided clarification of the sequence of individual steps in the mechanism of ECM: path formation, electrodeposition, ion transport, electrodeposition, and filament formation. 4). Developed appropriate accelerated testing conditions for assessing the no-clean processed PCBs' susceptibility to ECM: a). Conductor spacings in test structures should be reduced in order to reflect the trend of higher density electronics and the effect of path formation, independent of electric field, on the time-to-failure. b). THB testing temperatures should be modified according to the material present on the PCB, since testing at 85°C can cause the evaporation of weak organic acids (WOAs) in the flux residues, leading one to underestimate the risk of ECM. 5). Correlated temp-humidity-bias testing with ion chromatography analysis and potentiostat measurement to develop an efficient and effective assessment methodology to characterize the effect of no-clean processing on ECM.

SURFACE INSULATION RESISTANCE DEGRADATION AND ELECTROCHEMICAL MIGRATION ON PRINTED CIRCUIT BOARDS

By

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Dissertation submitted to the Faculty of the Graduate School of the
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CHAPTER 1: RESEARCH BACKGROUND

1.1 Electrochemical Migration and Surface Insulation Resistance

A failure mode of concern to the electronics industry involves current leakage [1] which results in intermittent or permanent failures on the surface of printed circuit boards (PCBs). Current leakage can occur due to a reduction in surface insulation resistance (SIR) between adjacent conductors. This is typically caused by electrochemical migration (ECM), which is the growth of conductive metal filaments (dendrites) on a PCB through an electrolyte solution under the influence of a DC voltage bias [2].

The electrochemical migration process occurs by a sequence of steps consisting of path formation, electrodissolution, ion transport, electrodeposition, and filament growth. Path formation is dependent on PCB materials, such as plating and laminate compositions, and PCB surface conditions, as well as the environment. Relevant PCB surface conditions include composition, concentration, and distribution of contaminants such as residues of fluxes used in the solder assembly process, and the topography of the board surface between adjacent conductors. The most relevant environmental conditions are temperature, humidity, and airborne contaminant composition and concentration.

The typical electrochemical migration path on a PCB develops from layers of moisture adsorbed on the surface. If the surface were ideally smooth and clean then a uniform adsorbed layer of moisture would combine with anions from atmospheric pollutants to form an electrolyte solution capable of transporting metal ions. In the presence of surface roughness and inhomogeneities, the thickness of an adsorbed moisture layer will be greater in areas with higher surface energy or curvature,

including pores and scratches. Condensed-phase contaminants, such as particles, fibers, or flux residues, will generally have higher moisture adsorption capacity than PCB laminates, further raising adsorbed moisture levels and providing a preferential path for ion transport. Surface defects and contaminants thus accelerate the initial, path formation step in the ECM process, reducing the overall time to failure.

Electrodissolution is the generation of solvated metal ions, typically through oxidation at the anode (positive electrode). These ions tend to migrate through the electrolyte under the influence of electromotive forces, typically towards the cathode (negative electrode). Electrodeposition occurs as the metal cations are reduced at the cathode. Filament growth occurs as more metal is deposited on the nuclei, eventually resulting in a dendritic structure.

Once a metal filament has spanned the distance between adjacent conductors, the leakage current between these conductors will increase. Intermittent failures are experienced when a dendrite grows, causes an electrical short, and then burns out due to the high current density. Permanent failures occur when a dendrite is capable of handling the current density, thus causing a complete and permanent short. ECM failures have a direct impact on the functionality of electronic systems, and are especially prevalent within high humidity and high temperature environments.

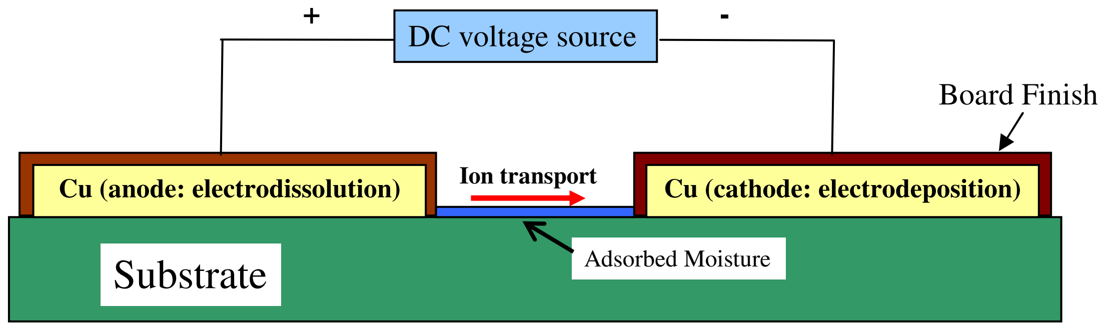

Figure 1.1 Three steps of electrochemical migration initiation

1.2 Electrochemical Migration vs. Conductive Anodic Filament

There are two distinct electrochemical migration phenomena that could occur in PWBs. In the first case, surface dendrites have been observed to form from the cathode to the anode under an applied voltage when surface contaminants and moisture are present (see Figure 1.2). If the voltage bias is sufficiently high, the dendrites bridging the gap between the anode and the cathode may "blow-out" (similar to a fuse), leaving sludge-like debris on the surface. These filaments are fragile and may be destroyed by oxidation, changes in surface tension during moisture absorption, drying, cooling or heating, or burned out if the current is sufficient. Short circuits therefore tend to be intermittent, but filaments can reform.

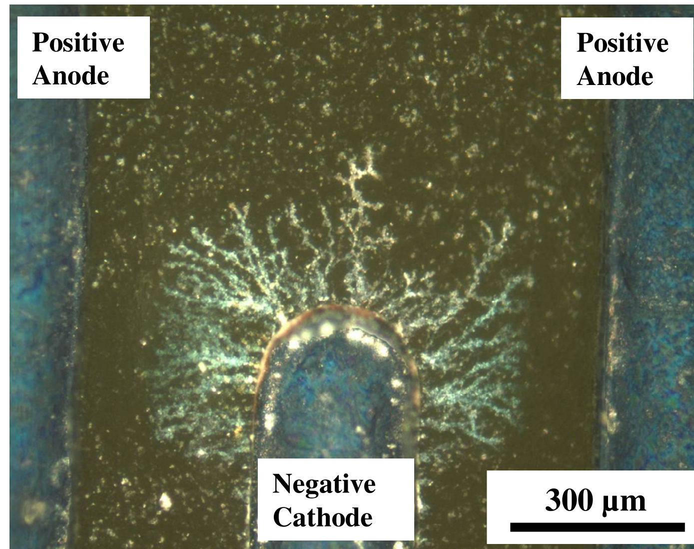

Figure 1.2 Dendritic growth is shown branching from an anodic finger of a comb structure on the surface of a PWB.

The second form of electrochemical migration and the focus of this dissertation is conductive filament formation (CFF), also referred to as conductive anodic filament (CAF) formation (see Figure 1.3). CFF differs from the surface dendritic growth in a number of ways:

- The direction of the filament growth (in the case of copper conductors) is from the anode to the cathode, not from the cathode to the anode.
- The filament is composed of a metallic salt, not neutral metal atoms.
- The phenomenon occurs in the substrate, not on the surface.

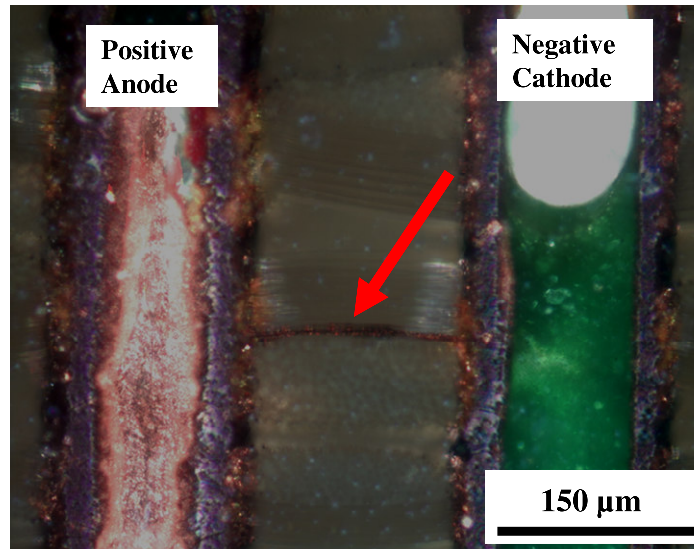

Figure 1.3 Optical image of a conductive filament bridging two plated through holes in a PWB (see arrow)

Electrochemical migration should not be confused with whisker growth, which is induced by mechanical stress, and is not electrically driven (see Figure 1.4).

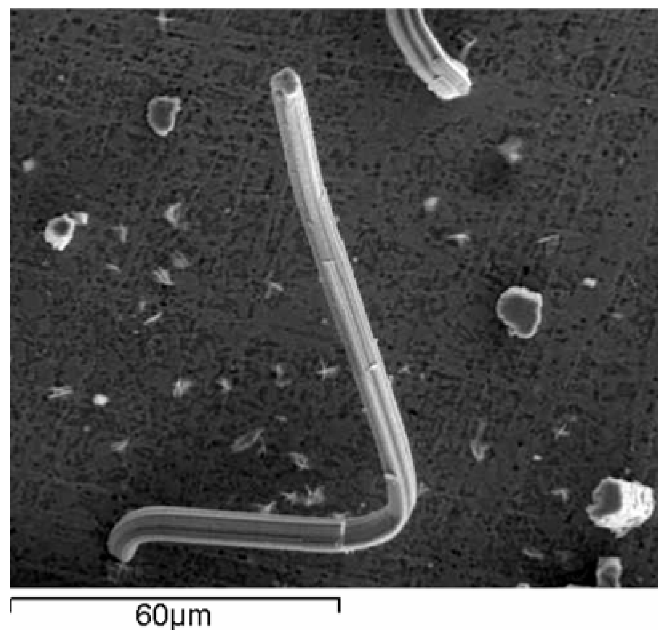

Figure 1.4 E-SEM micrograph of tin whisker growth, due to mechanical stress

1.3 Introduction of Flux

1.3.1 Flux Action

Once the flux is applied to the metal surface, it will first displace the adsorbed gas from the surface. After it has wetted the tarnished metal, it serves to restore the metallic surface, either by reduction of oxides or removal of the oxides from the surface [9].

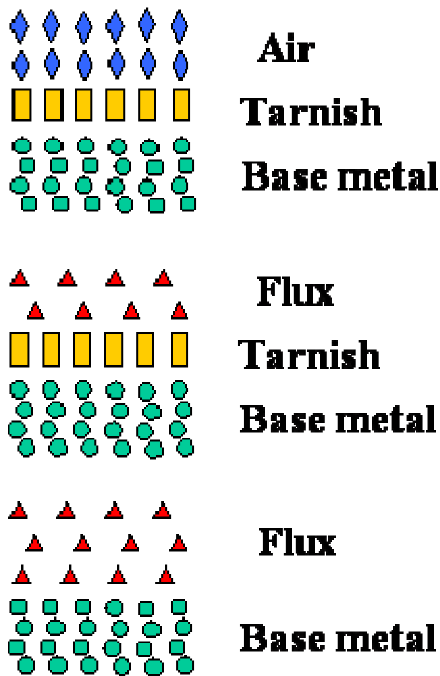

Figure 1.5 The schematic of flux action

1.3.2 No-clean Flux

No-clean flux (NCF) is a flux that requires no post-solder cleaning for defluxing purposes [9]. The no-clean category could be divided into two subsections, according to their composition, as follows.

No-clean rosin fluxes. This category is primarily composed of natural rosin, extracted from the oleoresin of pine trees and refined [5]. Consists of one or more of

the following types of rosin: gum rosin, wood rosin, tall oil rosin, modified or natural rosin.

VOC low no-clean flux. There is a new generation of fluxes that must fulfill some Environmental Protection Agency (EPA) concerns with the emission of volatile organic compounds (VOCs) with an as yet undetermined effect on humans, animals, vegetation, and global warming. The proposed legislation already exists and is pending approval by each state. And, industry has undertaken to address these issues with a new flux grouping labeled VOC-low flux. These fluxes use water, a non-VOC solvent, instead of the alcohol blends used in traditional fluxes as thinner. This has several implications.

1. The evaporation rate of these fluxes is slower, and more preheat is needed to avoid spattering during soldering.
2. The activators dissolved in the water can ionize before soldering, which makes these fluxes stronger than the identical activators in organic solvents.
3. Since the fluxing agents are water soluble, judicious selection can make sure the heated residues are also washable in water.
4. There is no flammability danger with this flux, making its storage much simpler.

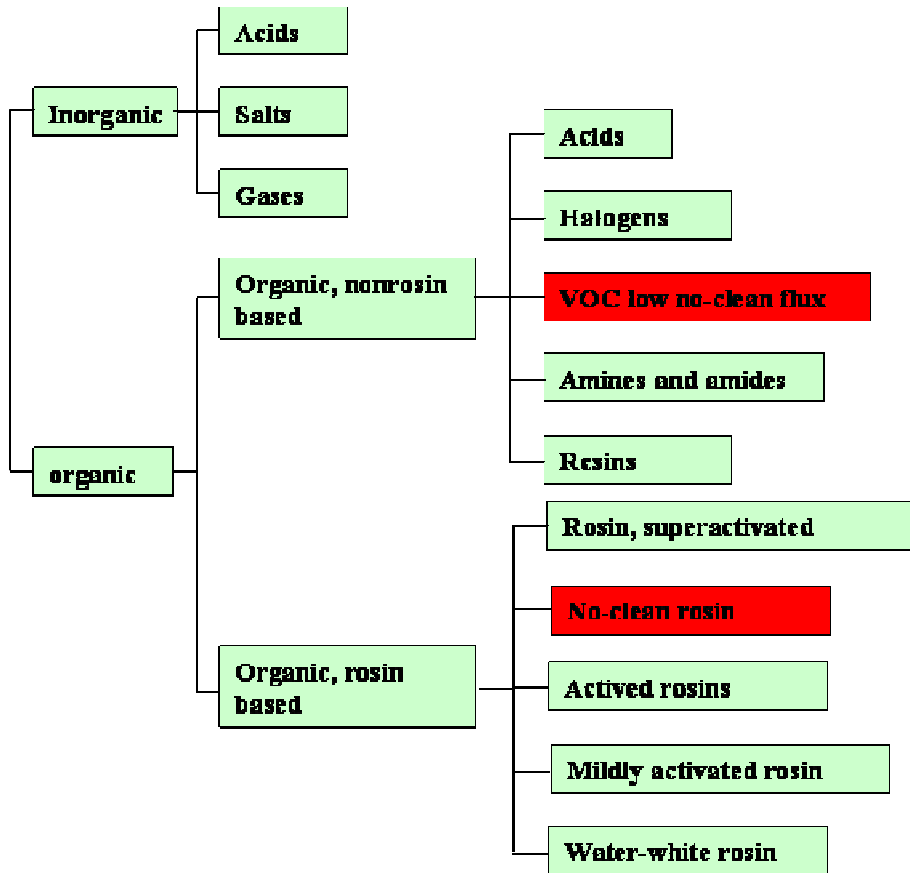

Figure 1.6 Category of flux based on the composition

1.4 Strong Movement to No-clean Processing

The use of traditional flux requires a cleaner to get rid of the residues that are left on the surface of PCBs. However, some of these flux cleaners, such as freon and other chlorofluorocarbons (CFCs), could deplete the ozone layers. Driven by environmental legislation [36], these kinds of cleaner should be prohibited. Moreover, the amount of volatile organic compounds (VOCs) existing in some clean type fluxes is high, which has the potential to harm people's health. And, the Environmental Protection Agency has already supposed legislation, which is pending approval, to restrict the uses of liquid that contains VOC-high content.

With the industry move into high density assemblies with fine-pitch and low-profile components, the difficulty do cleaning the flux residues becomes a nightmare

for manufacturers. pointing addition, the cost of cleaning has also increased. However, if using no-clean processing, the above question could be solved, since the clean process could be eliminated, which could save much time and cost. And also, the chemistry of some types of no-clean flux is VOC-low content, which could meet the requirements of coming legislation.

CHAPTER 2: RESEARCH MOTIVATION AND OBJECTIVES

2.1 Research Motivation

Widespread adoption of lead-free materials and processes for printed circuit board assembly has raised reliability concerns regarding surface insulation resistance (SIR) degradation and electrochemical migration (ECM).

As PCB conductor spacings decrease, electronic products become more susceptible to these failures, especially in the presence of surface contamination and flux residues, which might remain after no-clean processing.

Current industry standards on testing for susceptibility to ECM need to be updated to accommodate the materials used for no-clean processing, for lead-free applications, and for higher density PCB structures.

The traditional means for assessing ECM risk, temperature-humidity-bias testing, requires considerable time, human labor, and specialized equipment, which must be repeated if test samples change. More efficient testing methodologies are needed for assessing ECM risk.

Understanding how the mechanism of ECM is stimulated by lead-free applications and no-clean processing should allow identification of effective approaches for reducing ECM.

2.2 Noteworthy Studies

- D.Q. Yu, W. Jillek, E. Schmitt, *J Materials Science* (2006), made the statement that Ag has no migration due the formation of intermetallic compounds in the solder alloys. So, lead free solder alloys such as Sn-Ag, Sn-Ag-Cu are more reliable than than Pb containing solders [52].
- S. Lee, et al, "*Thin Solid Films* (2006), discussed that Pb was more susceptible to CAF failure than Sn in the eutectic SnPb alloy [50].
- M. Pasquale, et al, *J. Electrochemical Society* (2005), found that controlling the concentration ratio of 3-mercapto-1-propane sulfonic acid (MPSA) and poly ethylene glycol (PEG) could affect the growth velocity and morphology of copper dendrite [29].
- S. Bodea, R. Ballou, P. Molho, *Physical Review* (2004), observed that magnetic field could affect the morphology of the dendrit, which is composed of iron ion [28].
- P. Kinner, *IEEE Conference on Business of Electronic Product Reliability and Liability* (2004), observed that current test methods are outdated due to inappropriate settings for temperature, coupon design, and frequency of measurement [38].
- J. Sprovieri, *Assembly* (2003), discussed the importance of cleaning processes applied to PCBs after no-clean processing and failures caused by no-clean flux residues [27].

- S. Stock and L. Turbini, *Science* (2002), discussed how dendritic growth differs from CAF formation. In dendritic growth, the metal ions go into solution at the anode but plate out at the cathode, forming needles or tree-like formations [26].
- D. Pauls, *Circuit World* (2000), performed tests to examine a series of residues which come from conventional and no-clean fluxes, on printed circuit boards and assemblies [25].
- D. Rocak, et al, *Microelectronics Journal* (1999), evaluated four different no-clean rosin-based fluxes and found that two of them can lower SIR under condition of 40C and 93%RH with 50 VDC [65].
- C. Hunt and L. Zhou, *Soldering & Surface Mount Technology* (1999), investigated how SIR is affected by different fluxes, flux surface concentration, temperature, humidity and soldering process [24].
- L. Turbini, et al, *J. Electron. Mater* (1999), applied SIR tests to study the corrosive behavior of three weak organic acids and suggested that the industry standard tests at 85°C may be inappropriate for these materials. Accelerated testing at high temperature may return inaccurate predictions of long term reliability [23].
- T. Takemoto, et al, *Corrosion Science* (1997), observed that, in the Sn-Pb alloy system, pure lead showed the highest susceptibility to electrochemical migration. Alloys with 5-60%Sn showed similar high susceptibility. Further addition of tin lowered the susceptibility and pure tin had the lowest susceptibility [22].

- L. Turbini, *International SAMPE Technical Conference* (1996), made the statement that in general 85°C/85%RH provides the best accelerating conditions for assessing the electrochemical migration susceptibility of most fluxes [20].
- Cavallotti, et. al, *J. Electron. Mater* (1995), conducted a potentiostat experiment to evaluate the corrosivity of no-clean solder paste with respect to solder joints [21].
- L. Turbini, et. al, *Thirteenth IEEE/CHMT International* (1992), discussed that aqueous-based flux is more corrosive than rosin-based flux [3]and that there are several factors which affect the rate of growth of dendrites: (a) voltage gradient (b) critical humidity (c) contamination and (d) temperature [8].
- J. Brous, *National Electronic Packaging and Production Conference* (1992), found that flux and flux residues contain compounds such as glycol or polyglycol, which could enhance the water absorption of the PCB laminate [19].

2.3 Problems Remaining

Surface insulation resistance (SIR) degradation and electrochemical migration (ECM) do not result from independent factors. The interaction between physical factors (temperature, relative humidity, electric field, etc.) and chemical factors (solder alloy, substrate material, no-clean processing, etc.) needs to be understood.

Current industry standards are designed to serve as short-term qualification tests, typically lasting 72 to 168 hours, and do not provide a prediction of reliability in long-term applications. The failure mechanism for ECM in reliability of lead-free assemblies is not clear.

There are very few studies on development of rapid assessment methodologies for detecting the risk of ECM.

The mechanism of electrochemical migration is not completely understood. For example, the role of path formation has not been discussed in previous studies.

2.4 Research Objectives

Evaluate the effect of the following experimental factors on time-to-failure due to electrochemical migration:

- physical factors: temperature, relative humidity, electric field (combination of applied voltage and conductor spacing);
- chemical factors: lead-free solder, substrate (laminate) material, surface contamination, plating material and no-clean chemistry.

Demonstrate how the mechanism of electrochemical migration is stimulated by lead-free application with no-clean processing.

Investigate the role of path formation in the mechanism of electrochemical migration.

Develop recommendations to update the current industry testing standard for ECM.

Develop efficient and effective methodologies for assessing the possibility of electrochemical migration on printed circuit boards.

2.5 Research Approaches

To assess reliability concerns associated with surface insulation resistance degradation with electrochemical migration on printed circuit boards, and the effects of no-clean processing, there are five main points that need to be investigated. These are: revising current accelerated testing standards, assessing the risks caused by the new combination of lead-free systems, developing new assessment methodologies, applying protective coatings and evaluating the effect of contaminations. Each of them has been studied and is discussed in the following chapters.

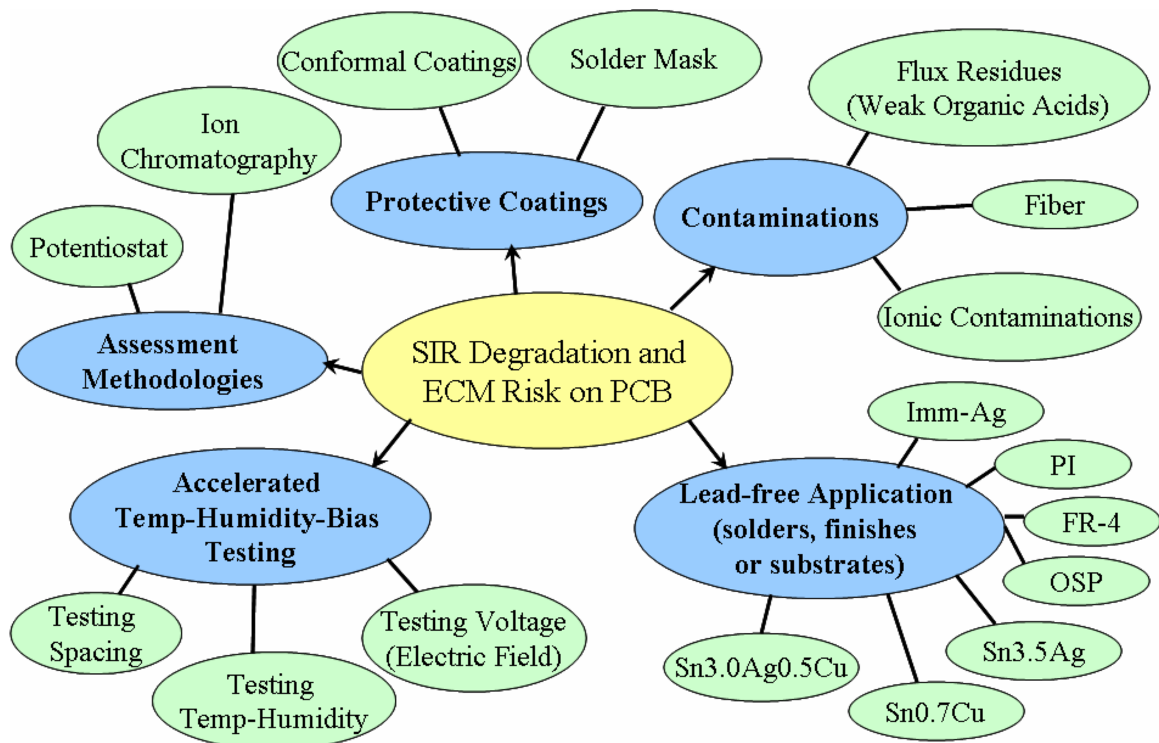

Figure 2.1 Research approaches to electrochemical migration

CHAPTER 3: SURFACE INSULATION RESISTANCE OF CONFORMALLY COATED PRINTED CIRCUIT BOARDS PROCESSED WITH NO-CLEAN FLUX

3.1 Abstract of Testing Findings

Printed circuit board (PCB) specimens containing three different IPC-B-25 test structures were exposed to temperature/humidity/bias conditions in order to evaluate the effects of conformal coating, conductor spacing, voltage bias, flux chemistry and test environment on surface insulation resistance (SIR). Results indicate that conformal coatings improve reliability, provided that sources of contamination on the PCB and within the coating are minimized. The presence of fibrous contaminants within the coating represents a preferential medium for moisture adsorption and ion transport, leading to accelerated reduction of SIR. In the absence of contamination, PCBs with conformal coatings were found to be less susceptible to SIR degradation than uncoated PCBs, with silicone providing better protection than urethane, and acrylic providing the least protection of the three coating materials evaluated. Conductor spacing was observed to represent a factor in the electrochemical migration (ECM) process independent of electric field, indicating that updated test structures are required to predict reliability of today's high density assemblies. The SIR failure rate with rosin-based no-clean flux was observed to be greater than that with aqueous-based no-clean flux. A higher failure rate was also observed for tests conducted at 40°C/93% RH than for 85°C/85% RH. Due to the more rapid evaporation of weak organic acids in the flux residues at higher temperatures, test

results obtained at 85°C/85% RH will not accurately predict reliability at lower temperatures for PCBs processed using no-clean flux.

3.2 Reliability Concerns of Conformal Coated Printed Circuit Boards

Conformal coatings are thin layers of synthetic resins or plastics that are applied to PCBs and conform to the contours of the assembly [11]. The primary functions of the coating are to protect the PCB from condensation of moisture and to provide a diffusion barrier for vapor phase moisture, ion transport, and filament growth, thereby reducing the risk of electrochemical migration. The process for conformally coating an electronic assembly has the potential to introduce reliability risks specifically associated with the coating. Such risks arise from contamination trapped under or within the coating or from voids between the PCB and the coating into which moisture can diffuse.

One concern with conformal coating arises when it is applied over a non-clean surface. This concern has increased because, in an effort to reduce costs and facilitate processing of high density assemblies with fine-pitch and low-profile components, the electronics industry has been adopting no-clean flux technology. The advantage of no-clean flux is that there is no stated requirement to clean the PCB after soldering. This is because the flux residues are not believed to adversely impact the performance or reliability of the electronic system. Nevertheless, residues left on the PCB surface are capable of absorbing moisture from the environment. The combination of adsorbed moisture and ionic contaminants associated with flux residues or the environment leads to formation of an electrolyte that can provide a medium for electrochemical migration [30]. When applied over a clean PCB surface, a conformal

Table 3.1 Experimental design for assessment of SIR degradation using no-clean fluxes on conformally coated PCBs

Conformal Coating	Urethane	Urethane	Acrylic	Acrylic	Silicone	Silicone
Type	VOC	VOC	VOC Free	VOC	VOC	VOC
Flux Type	Aqueous	Rosin	Rosin	Rosin	Aqueous	Rosin
Deactivated (Exposed to Reflow Profile)	Yes	Yes	Yes	Yes	Yes	Yes
Voltages (VDC)	6, 12, 24, 42	6, 12, 24, 42	6, 12, 24, 42	6, 12, 24, 42	6, 12, 24, 42	6, 12, 24, 42
Environments (^{o}C/ %RH)	40/93, 85/85	40/93, 85/85	40/93, 85/85	40/93, 85/85	40/93, 85/85	40/93, 85/85

coating can retard moisture absorption and decrease electrochemical migration failure rate.

3.3 Design of Experiments

A set of experiments was performed to assess susceptibility to SIR degradation and electrochemical migration of PCBs processed with no-clean fluxes. Two types of flux and four conformal coatings were tested under various accelerated conditions. Each test lasted 168 hours. The types of flux and conformal coating and the corresponding conditions are provided in Table 3.1.

The no-clean fluxes used in this study, consisting of a rosin and an aqueous-based flux, are representative of those used in manufacturing and rework processes. Following the IPC-J-004 standard, the rosin-based flux and aqueous-based flux are “ROM0” and “ORL0” respectively. The no-clean designation means the residues can be left on the board. The conformal coatings assessed in this study were acrylic, urethane, and silicone, which are low in cost and widely used in industry. Environmental conditions were selected based upon recommendations in industry

standards for accelerating SIR degradation and ECM [6][15]. The voltages selected were those commonly used in the automotive electronics industry. For instance, the common car battery operates at 12V, and 24V is commonly used in large diesel engine vehicles. Testing was performed at 42V because the automotive industry will be transitioning to higher power batteries (approximately 5 kilowatts) in order to run more systems on battery power. A 6 volt bias level was included to expand the experimental design range to lower voltages.

3.3.1 Test Vehicle

The test vehicles used in this study were IPC-B-25 test boards [3], as illustrated in Figure 3.1. These boards each consisted of three comb structures, with 6.25, 12.5 and 25 mil spacing (equivalent to 0.16, 0.32 and 0.64 mm). These spacings span the range of current lead spacings in fine-pitched plastic packages. In order to investigate current leakage and dendritic growth between solder joints, the comb structures were coated with a eutectic (63Sn/37Pb) solder applied by hot air solder leveling (HASL).

3.3.2 Surface Insulation Resistance Test System

Surface insulation resistance (SIR) test systems are commonly used to detect leakage current on a PCB. Sources of leakage current include surface dendritic growth, conductive filament formation [40] [41][42] (similar to dendritic growth but beneath the PCB surface), and other surface anomalies, such as flux residues, that create a conductive path [30]. On typical FR-4 PCBs, the SIR measurement is 99.9% confined to the surface of the PCB even though SIR measures both surface and bulk conduction [40]. One of the objectives of this research was to evaluate the effect of test environment and bias voltage on SIR and dendritic growth. Therefore, our tests were conducted under a variety of temperature, humidity, and bias conditions, some

of which corresponded to those cited in commonly used standards for SIR testing. According to IPC-TM-650 [3] and J-STD-004A [5], the PCB is considered to have failed when the resistance drops below 100 megohms. To meet these requirements in the present study, SIR readings were taken at less than one minute intervals on a test system designed to measure current in the picoampere range. Since SIR will be affected by the test conditions, our failure criteria combined an SIR threshold level of 100 megohms with verification of the presence of an abnormal physical feature. The SIR test system used for these tests included a one-megohm resistor in series with each SIR test structure, which served to limit the current to prevent fusing of dendrites due to high current density.

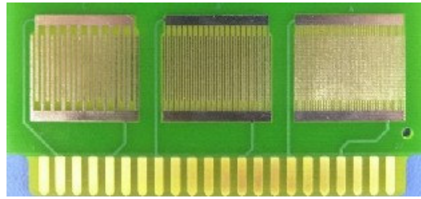

Figure 3.1 IPC-B-25 test coupon showing conductor spacings from left to right of 25 mil (0.64 mm), 12.5 mil (0.32 mm), and 6.25 mil (0.16 mm).

3.3.3 Processing of Test Coupons

Each of the IPC-B-25 test coupons was inscribed with sample identification information on the unbiased side of the PCB. All test coupons were cleaned after processing and identification, and prior to application of no-clean flux, to remove contaminants present from the board manufacturing process. Cleaning was performed by soaking the boards for one hour at 80°C in a solution of isopropyl alcohol and deionized water. The average measured surface insulation resistance (SIR) of the boards after cleaning was 2×10^{12} Ohms. The flux was applied by an airbrush technique with a fine mist evenly distributed over the entire PCB surface.

Boards were allowed to dry for 24 hours before reflow processing. Reflow was performed by Capital Electro-circuits in Gaithersburg, MD using their standard eutectic Sn-Pb reflow profile. After reflow the boards were conformally coated to a uniform thickness of between 25 and 75 µm using professional spraying equipment in commercial processing facilities. The acrylic coatings were Humiseal 1R32A-2 (VOC-containing, applied in a single coating operation) and 1H2OAR1 (VOC-free, applied in two coating operations). The urethane coating was Cytec Conathane® CE-1135-35, applied as a single coating. The silicone coating was Dow Corning 3-1753, applied in one coating operation.

3.4 **Results and discussion**

Temperature/humidity/bias tests of fixed, 168 hour duration were performed to assess the effects of conformal coatings, contamination, electric field, conductor spacing, flux chemistry, and temperature/humidity conditions on stability of surface insulation resistance. Analysis of the SIR data, combined with physical analysis of the test specimens, provided insight into the causes of observed SIR degradation and the experimental conditions which were more conducive to electrochemical migration. The SIR of control boards, containing HASL finish without no-clean flux or conformal coating, varied during the course of the 85°C/85% RH test in the 10^9 to 10^{10} Ohm range with no values below 2 x 10^9 Ohms. SIR values for boards with 6.25 mil (0.16 mm), 12.5 mil (0.32 mm), and 25 mil (0.64 mm) spacings were similar.

3.4.1 Effect of Conformal Coatings and Contamination

Conformal coatings are meant to retard moisture diffusion to the PCB surface, prolonging the formation of electrolyte on the surface of the PCB and increasing the time-to-failure of the system. The PCB test structures that exhibited SIR drops below

Table 3.2 Results of the temperature/humidity/bias tests of conformally coated PCBs. For each individual comb structure for which an SIR failure was detected, the following symbols are used to report results of observations from failure analysis: "D": dendritic growth; "N": nodules; "F": fiber contamination.

			Urethane		Acrylic		Silicone	
Environment (^{o}C/%RH)	**Voltage (VDC)**	**Spacing (mil)**	**Aqueous-based flux**	**Rosin-based flux**	**VOC**	**VOC-free**	**Aqueous-based flux**	**Rosin-based flux**
					Rosin-based flux			
40/93	**6**	6.25		F				
		12.5		F				
		25						
	42	6.25	F	F, F, N	F	F, F, N	F	F, F, F
		12.5			F	F,D		
		25						
85/85	**6**	6.25			N			
		12.5						
		25						
	42	6.25		F, F	N, N,D	F, F	F, F	
		12.5			N			
		25						

the failure threshold of 10^8 Ohms were examined using optical microscopy to identify surface features associated with the failures. As presented in Table 3.2, the failed comb structures were put into three categories: those showing clear evidence of dendritic growth (labeled "D" in the table), those containing nodular growth along the conductors (labeled "N" in the table), and those containing fiber contamination (labeled "F" in the table).

Figure 3.2 shows the growth of dendritic structures between adjacent conductors. These delicate branched structures can produce a continuous conduction path between electrodes, but are easily fused open due to high current densities arising from their small cross-sections. This can lead to intermittent shorts followed by periods of higher SIR.

A number of failed comb structures were found to possess nodular growths without fully developed dendrites, as shown in Figure 3.3. These nodules may have

been present prior to SIR testing, or the specimens may be examples of intermittent failure in which the conduction path was destroyed by high current density. Alternatively, they may have experienced reduced SIR due to a combination of metallic conduction due to ECM and adsorbed moisture at the PCB surface. Elevated levels of adsorbed moisture can be promoted by voids within the conformal coating, such as those which are visible in Figure 3.3.

With the adoption of no-clean fluxes by the electronics industry the cleaning step after reflow is increasingly being eliminated. Flux residues and other surface contamination such as fibers, introduced during assembly, handling, or testing, may remain on the surface of PCBs. Fibers provide a medium for adsorption of moisture, allowing it to combine with no-clean flux residues such as weak organic acids (WOAs) to form an electrolyte. Figure 3.4 shows a section of a failed comb structure with a fiber bridging two adjacent conductors.

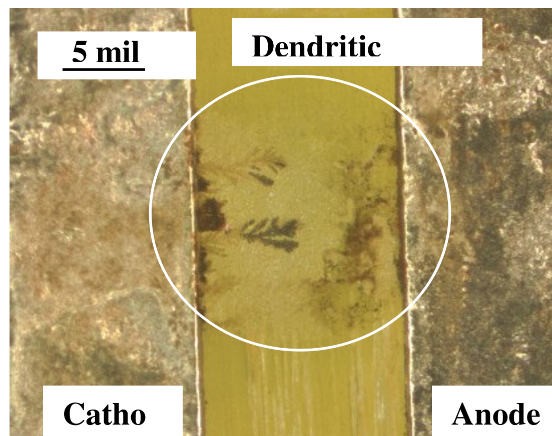

Figure 3.2 Comb structure with dendritic growth: optical micrograph of deactivated rosin-based flux, 12.5 mil (0.32 mm) conductor spacing, with acrylic-VOC-free conformal coating exposed to a 40°C/93% RH environment with an applied 42V bias.

The IPC-B-25 test structure consists of three comb structures with 6.25 mil (0.16 mm), 12.5 mil (0.32 mm) and 25 mil (0.64 mm) spacings. With regard to the effect of

conductor spacing, larger spacings should lead to longer time-to-failure and thus fewer SIR drops observed in a fixed duration test. However, as illustrated in Figure 3.5, on one test PCB the SIR dropped to below the failure criterion only on the 12.5 mil (0.32 mm) comb structure. This raises the question of why the 6.25 mil (0.16 mm) structures did not fail. Failure analysis of the PCB surface showed that only the 12.5 mil (0.32 mm) comb structure had fiber contamination, similar to that shown inFigure 3.4. These organic fibers were introduced prior to conformal coating either during or after application of the flux. Since the no-clean flux residues were a focus of the experiment, no cleaning was performed prior to conformal coating, to avoid removing any residues. The presence of a fiber could provide an interface for diffusion and accumulation of moisture or a preferential medium for moisture adsorption, accelerating the formation of a continuous path of electrolyte between anode and cathode. In the absence of fiber contamination, it would take much longer for electrolyte to collect at the interface between the PCB and the coating. This electrolyte reduces the SIR and can also serve as a path for electrochemical migration.

As discussed in the introduction, the first step in the ECM mechanism is path formation. If this step can be delayed, the overall rate of dendrite formation, which is required for ECM failure, will be decreased. The fiber can thus provide a path for the next three steps of ECM, electrodissolution, ion transport, electrodeposition, which significantly shortens the time-to-failure of ECM. Furthermore, as will be discussed in Section 3.2, the path formation step can exhibit a dependence on spacing which is independent of electric field.

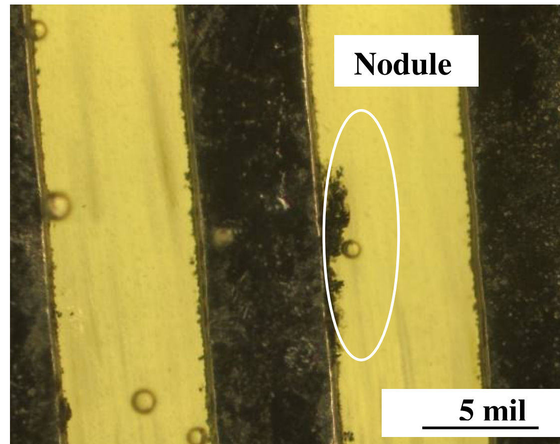

Figure 3.3 Comb structure with nodules: optical micrograph of deactivated rosin-based flux, 6.25 mil (0.16 mm) conductor spacing, with acrylic-VOC-free conformal coating exposed to a 40°C/93% RH environment with an applied 42V bias.

Table 3.2 shows that the majority of failures in this study have been traced to fiber contamination. Nevertheless, a significant finding from this work, which applies equally well to all failures, is that silicone is more effective at preventing SIR reduction than urethane, which is in turn better than acrylic.

Table 3.3 Results of the temperature/humidity/bias tests of PCBs without conformal coatings. For each individual comb structure for which an SIR failure was detected, the symbol "D" is used to indicate that failure analysis revealed the presence of dendritic growth.

Environment (^{o}C/%RH)	Voltage (VDC)	Spacing (mils)	Aqueous-based flux	Rosin-based flux
40/93	6	6.25	D	DDD
		12.5		
		25		
	12	6.25	DDD	
		12.5		
		25		
	24	6.25		D
		12.5		
		25		
	42	6.25		
		12.5		
		25		
85/85	6	6.25		
		12.5		
		25		
	12	6.25		
		12.5		
		25		
	24	6.25		D
		12.5		
		25		
	42	6.25		D
		12.5		
		25		

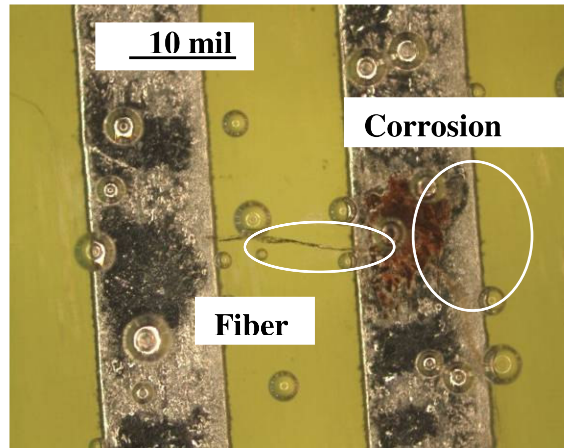

Figure 3.4 Comb structure with fiber contamination: optical micrograph of deactivated rosin-based flux, 12.5 mil (0.32 mm) conductor spacing, with urethane conformal coating exposed to a 40°C/93% RH environment with an applied 6V bias.

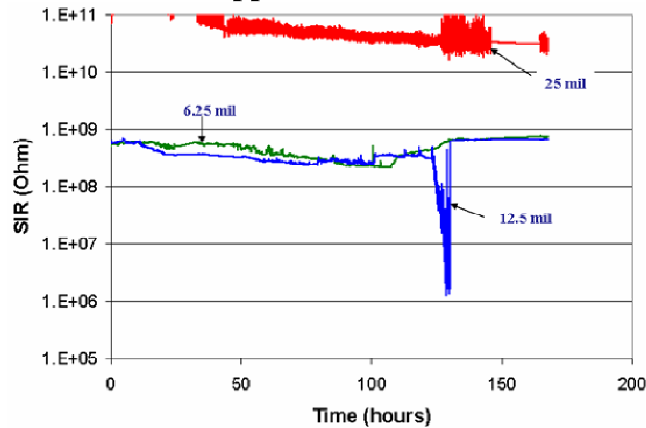

Figure 3.5 SIR trends for deactivated rosin-based flux with urethane conformal coating exposed to a 40°C/93% RH environment with an applied 6V bias.

As shown in Table 3.3, higher failure rates were observed for uncoated PCBs compared with those from coated PCBs for which failure was not caused by fibers. Thus, when processing conditions are properly controlled to prevent surface contamination, conformal coatings retard dendritic growth on the surface of PCBs.

3.4.2 Electric Field and Conductor Spacing Effect

Since each IPC-B-25 test coupon contained 3 different comb structures, the total number of combs in this study was 216. Table 3.2 shows that 28 out of 216 comb

structures experienced failures during the temperature/humidity/bias testing. None of these failures occurred at the 25 mil (0.64 mm) spacing, indicating a relatively low risk of SIR degradation for PCBs with widely spaced conductors. The remaining comb structures, with either 6.25 mil (0.16 mm) or 12.5 mil (0.32 mm) conductor spacing, experienced a 20% failure rate. Considering only the 42V test on 6.25 mil (0.16 mm) comb structures, 21 out of 36 specimens experienced failures or almost 60%. These trends apply also if failures due to fiber contamination are ignored. These observations show that as PCB designs migrate to higher densities, the risk of ECM failure increases. This risk increases dramatically as high density designs are coupled with high bias voltages.

The voltage bias is directly proportional to the force applied to charged particles (e.g., metallic ions) within the electric field. The force applied to a charged particle will affect the time it takes an ion to move through the electrolyte solution. The electric field can be calculated from the applied voltage and the geometry of the structure under consideration. For parallel conductors, $E=V/d$, where E is the average electric field, V is applied voltage, and d is the distance separating two oppositely biased conductors [46]. Therefore, as the voltage bias is increased or the spacing is reduced, the higher electric field may accelerate electrochemical migration. For a comb structure with 6.25 mil (0.16 mm) spacing under a 6V bias, the electric field is 1V/mil, and for a 42 V bias, it is 7V/mil. From Table 3.2, no failures were found at 25 mil (0.64 mm), although the electric field of 42V/25 mil (1.7V/mil) is higher than that for 6 V/6.25 mil. This suggests that the spacing plays a role in ECM independent of the electric field. The longer time required for continuous path formation at longer

spacings may manifest itself as a larger incubation period prior to dendrite nucleation, lengthening the time to ECM failure even when the electric field driving ion transport is the same or greater than at smaller spacings. This observation is particularly significant in view of the ongoing trend in the electronics industry toward reduced spacings on PCBs. The absence of observed electrochemical migration or drops in SIR for 25 mil (0.64 mm) conductor spacing also suggests that industrial and military specifications [1][2][5][47] based on older PCB designs need to be updated to correctly assess reliability of higher density PCB designs.

3.4.3 Effect of Flux Chemistry

Test results shown in Table 3.2 and Table 3.3 indicate somewhat higher failure rates for PCBs processed with rosin-based flux as compared with aqueous-based flux. This suggested that the flux residues from rosin-based flux have a higher degree of reactivity than those from aqueous-based flux. To measure the relative reactivity of the two types of flux residue, potentiostat measurements were performed on extracts from deactivated (reflowed) flux. Flux residues were extracted by soaking in a warm solution of deionized water and isopropyl alcohol. From the corrosion current measured at the corrosion potential for each sample, the potentiostat allowed calculation of corrosion rates as shown in Table 3.4, which provide a relative measure of reactivity. These results confirm that residues from the rosin-based flux have higher reactivity than those from aqueous-based flux.

Table 3.4 Corrosion rate and weak organic acid composition of flux residues after solder reflow

	Aqueous-based Flux	Rosin-based Flux
Corrosion rate (µm /year)	2±0.3	14±7
Weak Organic Acid		
Glutaric (ppm)	7500	22500
Adipic (ppm)	13000	6500
Succinic (ppm)	Not Detected	4500
Total Amount (ppm)	20500	33500
Concentration (µg/in^2)	113	185

Since weak organic acids (WOAs) have been identified as a component of flux residues that can contribute to reduction in SIR [48], an analysis of the WOA content of the flux residues was undertaken to establish whether this would explain the differing reactivity of the two types of flux. Extracts were analyzed by ion chromatography (IC) in order to determine the composition and amount of weak organic acids contained in the flux residues remaining on PCB surfaces after reflow. As shown in Table 3.4, residues from the rosin-based flux contained about 50% higher concentration of WOA than those from the aqueous-based flux, which helps to explain the higher reactivity observed for the rosin-based flux.

3.4.4 Effect of Temperature and Humidity

Current industry standards recommend either 40°C/93% RH or 85°C/85% RH as test conditions. Table 3.2 and Table 3.3 show that the 40°C/93% RH environment is more likely to induce drops in surface insulation resistance when testing PCBs processed using no-clean flux. Moreover, 85°C/85% RH may not be an appropriate test condition because it causes the dissolution of HASL plating as seen in Figure 3.6, Figure 3.7 and Figure 3.8. The dissolution of the plating material would make more metal ions available within the electrolyte and thus increase the risk of dendrite

formation. Most importantly, an 85°C environment will increase the evaporation rate of WOAs [48], which are one of the crucial drivers for ECM of PCBs processed using no-clean fluxes. The results of this study therefore lend further support to the view that temperatures less than 85°C should be used to accelerate testing for SIR degradation of PCBs processed with no-clean flux.

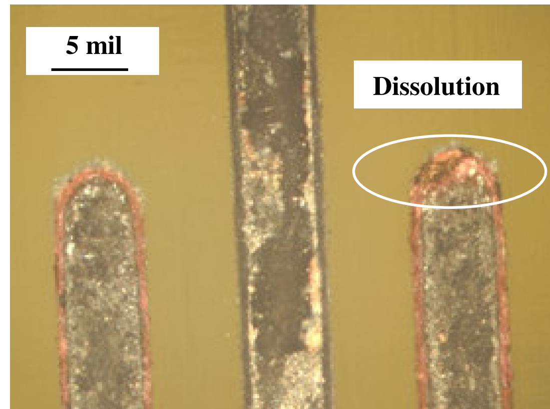

Figure 3.6 Optical micrograph of deactivated rosin-based flux, 6.25 mil (0.16 mm) conductor spacing, with acrylic-VOC conformal coating exposed to a 85°C/85% RH environment with an applied 6V bias.

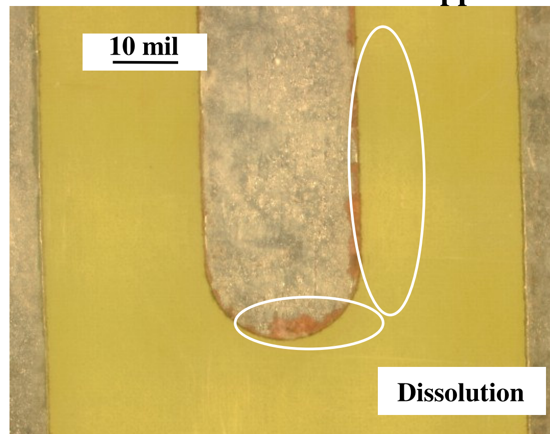

Figure 3.7 Optical micrograph of deactivated aqueous-based flux, 25 mil (0.64 mm) conductor spacing, with silicone conformal coating exposed to a 85°C/85% RH environment with an applied 42V bias.

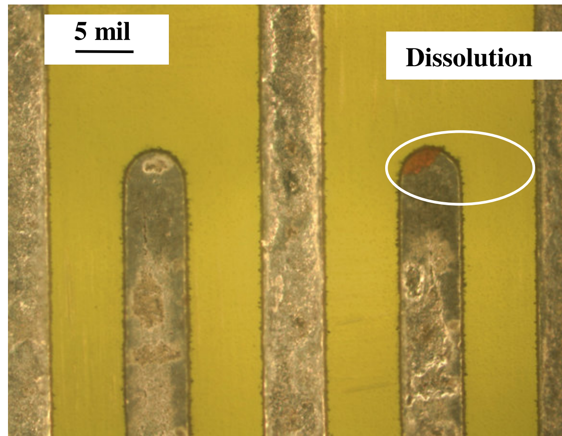

Figure 3.8 Optical micrograph of deactivated rosin-based flux, 6.25 mil (0.16 mm) conductor spacing, with silicone conformal coating exposed to a 85°C/85% RH environment with an applied 42V bias.

3.5 Conclusions

PCB specimens containing three different IPC-B-25 test structures were exposed to temperature/humidity/bias conditions in order to evaluate the effects of conformal coating, conductor spacing, voltage bias, flux chemistry and test environment on reduction of surface insulation resistance. Some of the PCBs which were conformally coated were found to possess fiber contamination embedded in the coating. The fibers provided a medium for adsorption of moisture, allowing it to combine with flux residues to form an electrolyte. This constituted a preferential path for ion transport which increased the susceptibility of these specimens to failure by SIR degradation. Thus, proper quality and contamination control is required in all steps of the PCB assembly process in order to avoid introduction of contaminants which can lead to early failure.

In the absence of fiber contamination, conformal coatings were found to reduce the risk of electrochemical migration since PCBs with conformal coatings were less susceptible to SIR degradation than uncoated PCBs. Of the three coating materials

studied, silicone was found to be most effective in retarding SIR degradation, followed by urethane and then acrylic.

Conductor spacing was found to be a factor in the ECM process independent of electric field. Current industry standards recommend a spacing of 25 mil (0.64 mm) in specimens used for ECM testing. Nevertheless, smaller spacings are already present in electronic products in use today. The observation that electric field alone was not sufficient to accelerate all the steps in the ECM process suggests that industry and military specifications and test standards based on older PCB designs are not suitable for assessing the reliability risk associated with ECM in higher density products. Successful prediction of susceptibility to ECM requires test structures with comparable spacings, produced using the same production materials and processes as the electronic products whose reliability is to be evaluated through accelerated testing.

From the SIR test results on uncoated PCBs, it is clear that the risk of ECM with rosin-based no-clean flux is at least as great as that with aqueous-based no-clean flux. Residues of rosin-based flux were found to contain about 50% higher concentration of weak organic acids after reflow. This led to higher activity and promoted moisture adsorption, further reducing the time-to-failure due to SIR reduction.

It is noteworthy that the tests performed at 85°C/85% RH produced fewer failures than tests at 40°C/93% RH, rather than accelerating the ECM process. This result is explained by the volatile nature of the weak organic acids which are responsible for the reactivity of the flux residues. The more rapid evaporation of these WOAs in the higher temperature test environment resulted in a lower failure rate. This makes the 85°C/85% RH environment less effective than 40°C/93% RH at

reproducing and accelerating degradation processes expected to lead to SIR failure under typical application conditions for PCBs assembled using no-clean processing. Although a number of industry standards recommend the use of $85^{o}C$/85% RH as a test environment for assessing the risk of SIR degradation, it is evident that this is no longer appropriate with the introduction of solder assembly processes using no-clean flux chemistries.

CHAPTER 4: LONG-TERM RELIABILITY OF LEAD-FREE PRINTED CIRCUIT BOARDS IN TEMPERATURE-HUMIDITY-BIAS CONDITIONS

4.1 Abstract of Testing Findings

This chapter reports on the results of long-term temperature-humidity-bias testing on FR4 and polyimide printed circuit boards processed with three different types of solder (Sn-3.0Ag-0.5Cu, Sn-37Pb, and Sn-3.5Ag) and a variety of board finishes**.** The purpose was to evaluate the relative susceptibility to reduction in surface insulation resistance and electrochemical migration. The results from these reliability tests, which lasted over 8,000 hours, provide design guidance for electronic assemblies expected to survive many years under operating conditions involving high relative humidity. For assemblies consisting of polyimide substrates processed with silver-containing lead-free solder, recommendations are to use greater conductor spacings whenever possible, to minimize ionic contamination, and to consider use of a protective coating.

4.2 Reliability Concerns of Lead-free Printed Circuit Boards

The recent widespread adoption of lead-free materials and processes for printed circuit board assembly has introduced uncertainties regarding the long-term reliability of lead-free electronic products. Current industry standards, such as IPC-TM-650 and IEC 61189-5, recommend the use of temperature-humidity-bias (THB) testing to assess the stability of surface insulation resistance (SIR) and risk of electrochemical migration (ECM) of electronic assemblies. These tests typically last 72 to 168 hours and do not provide a prediction of reliability in long-term applications because

acceleration factors for ECM of lead-free assemblies have not yet been available. Thus, test times used in procedures described in industry standards cannot be translated to equivalent field life. The present study was intended to provide reliability data of lead-free electronic assemblies subject to long-term (over 8,000 hours) THB condition.

4.3 Design of Experiments

A design of experiments was performed to assess susceptibility to SIR degradation and electrochemical migration of PCBs processed with lead-free or eutectic Sn-37Pb solder alloy, using several different fluxes and plating types, as shown in Table 4.1.

Table 4.1 Description of printed circuit boards used for ECM testing

Board No.	Plating Type	Substrate Type	Flux Type	Solder Alloy
1	HASL	FR4	No-clean-rosin	SnPb (Sn-37Pb)
2	ImAg	FR4	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
3	ENIG	PI	Rosin	SnAg (Sn-3.5Ag)
4	ImAg	PI	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
5	ImAg	PI	Rosin	SnAg (Sn-3.5Ag)
6	ENIG	FR4	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
7	ENIG	PI	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
8	ImSn	FR4	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
9	ImSn	PI	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
10	OSP	FR4	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
11	Sn	PI	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
12	Sn	PI	Rosin	SnAg (Sn-3.5Ag)
13	ImSn	PI	Rosin	SnAg (Sn-3.5Ag)
14	HASL	FR4	No-clean-rosin	SnPb (Sn-37Pb)
15	ImAg	FR4	No-clean-resin	SAC (Sn-3.0Ag-0.5Cu)
16	ENIG	PI	Rosin	SnAg (Sn-3.5Ag)

Key to abbreviations: HASL: Hot air solder leveling, Sn-37Pb; ImAg: immersion silver; ENIG: electroless nickel/immersion gold; ImSn: immersion tin; OSP: organic solderability preservative; Sn: property Sn.

4.3.1 Samples and Sample Preparation

SIR testing was performed using a test structure designed to simulate a practical PCB assembly. The test structure consisted of 11 pairs of solder pads in parallel, which is marked with position 1 to position 11, shown in Figure 4.1, with edge-to-edge pad separations of 0.25 mm (10 mils). In order to compare the effect of the substrate on susceptibility to electrochemical migration, two different PCB substrates, FR-4 and polyimide (PI), were tested. The solder pads were plated with a wide variety of common plating materials in order to assess the role of the plating in ECM. A no-clean Kester R905 SAC (Sn3Ag0.5Cu) paste containing resin-based flux was used for lead-free SAC PCBs. A no-clean Kester 256 paste (Sn-37Pb) containing rosin-based flux was used for the eutectic Sn-37Pb PCBs. The Sn-3.5Ag solder paste was Alphametals RMA-390DH3 containing a rosin-based flux designed for washability of flux residue after reflow. A laser-cut stencil with 5 mils nominal thickness was used for printing. The 16 board configurations used in the present study are described in Table 4.1. In keeping with the objective of simulating practical implementations of high-density PCB designs, pads were stencil printed with solder and subjected to convective reflow.

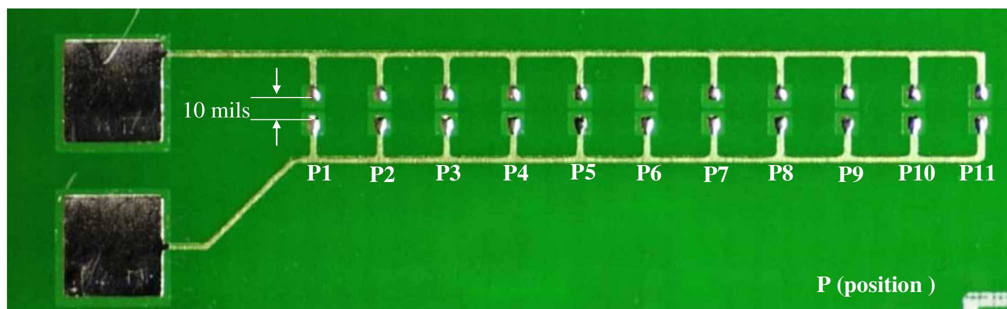

Figure 4.1 Test structure used in ECM study

For the SAC and Sn-Pb boards, reflow was conducted in a 10 zone convection oven with nitrogen ambient. The maximum peak temperature measured on the board surface was 245ºC for Pb-free reflow while the corresponding peak temperature for Sn-Pb reflow was 215ºC. Thus there is a 30ºC increase in the peak temperature for the Pb-free reflow process compared to Sn-Pb reflow. The Sn-Ag boards were processed using a vapor phase reflow, with a vapor temperature of 260ºC. All the boards were subjected to two reflow passes in order to simulate actual top and bottom assembly processes. The Sn-Ag boards were washed in an aqueous bath after reflow processing.

4.3.2 Environmental Testing Conditions

The test structures were exposed to a series of temperature/humidity/bias (THB) conditions, as shown in Table 4.2, in order to evaluate relative susceptibility to electrochemical migration. The first set THB conditions selected for study were 40°C, 93% relative humidity (RH), and 5V bias. These temperature and humidity conditions are consistent with the requirements of IPC-TM-650, Section 2.6.14.1 [3] and IEC 61189-5 [6]. Furthermore, since many of the samples in this study were processed with no-clean flux, this was an appropriate starting condition to ensure that volatile organic acids which may have remained as residues on the PCB after processing were not lost to evaporation prior to significant THB exposure. The initial bias voltage was maintained at 5V in order to typical conditions experienced with high density PCB assemblies in low-power applications such as consumer electronics.

Table 4.2 Sequence of environmental test conditions (total time: 8170 hours)

Test Sequence Description	Testing Time (Hours)	Testing Condition (Temperature/Relative Humidity/Bias Voltage)
Fixed THB Condition 1	672	40°C93RH5V
Fixed THB Condition 2	168	65°C88RH5V
THB cycling	552	Temperature varied between 40 and 65°C Relative humidity varied between 65 and 93 % Bias voltage varied between 5 and 10 V
Fixed THB Condition 3	294	65°C88RH10V
Fixed THB Condition 4	168	65°C88RH20V
Fixed THB Condition 5	168	65°C88RH30V
Fixed THB Condition 6	6148	65°C88RH40V

After four weeks of exposure at the starting THB condition, there were no observations of failure. The THB conditions were then adjusted to 65°C, 88% RH, and 5V. These temperature and humidity conditions represent an alternate recommended condition provided in IPC-TM-650, Section 2.6.14.1 [3]. Following one week at these conditions, a sequence of THB conditions was applied, temperature varied between 40 and 65°C, relative humidity varied between 65 and 93 % and bias voltage varied between 5V and 10V. The final portion of the investigation consisted of the application of successively increasing bias voltages, starting at 10V and

increasing to 40V, during 65°C, 88% RH exposure. The total THB exposure time for the test samples was 8170 hours.

4.3.3 Surface Insulation Resistance Test System

According to the standards listed in IPC-TM-650, Section 2.6.3.3 [3]and J-STD-004 [5], a PCB is considered failed when the resistance drops below 100 megohms. An SIR system capable of detecting ECM failures according to these requirements must be designed to measure the level of surface insulation resistance no less than 10^{10} Ohms. The system used in the present study had a detection limit of 10^{11} Ohms and included a one-megohm resistor in series with each SIR test structure, which served to limit the current to prevent fusing of dendrites due to high current density [44]. The SIR value of each test board was recorded once every 55 seconds.

4.4 Results and Discussion

The failure criterion for SIR is less than 1×10^8 ohms. One of the recognized failure mechanisms associated with SIR reduction is ECM, which is characterized by an SIR failure accompanied by detection of a dendrite. Thus, all instances of failure due to ECM entail an SIR failure, but not all observed SIR failures are necessarily caused by ECM.

Exposure to a series of temperature/humidity/bias conditions of increasing severity up to 65°C, 88% RH at 40V produced SIR failures in six out of sixteen samples over a total of 8170 hours of testing. All failures occurred between 2000 and 4000 hours of testing. After 4000 hours of testing no significant SIR degradation was observed. Four samples showed a persistent sequence of SIR drops. Three of these samples, board 5, board 13 and board 16, were processed using Sn-3.5Ag solder on

polyimide substrate, and the fourth, board 10, was processed with Sn-3.0Ag-0.5Cu solder on FR-4 substrate. Metallic migration was detected for all of these boards. Energy dispersive x-ray spectroscopy mapping of migrations showed that the dendrite are composed of silver. Two samples, board 4 and board 7, failed intermittently and then recovered, between 2000 and 2600 hours of testing. Both of these samples were processed using Sn-3.0Ag-0.5Cu solder on polyimide substrates. A summary of the test results is shown in Table 4.3.

Illustrated in the Table 4.3, there are two categories of SIR failure. One category is intermittent SIR failure, which refers to an SIR drop below the failure criteria lasting less than 5 hours followed by recovery. The second is permanent SIR failure, which means that the SIR dropped below the failure criteria for more than 5 hours. The samples exhibiting intermittent failure were kept in the chamber until the testing was completed, while the samples showing permanent failure were taken out during testing without being returned back to the chamber.

As depicted in Figure 4.1, the test structure has 11 contact pairs across which ECM can occur. All the test samples were analyzed through optical analysis, ESEM (Environmental Scanning Electron Microcopy), and EDS (energy dispersive spectroscopy) analysis. Several different characteristic features were observed in contact pairs associated with SIR failures. One failure mode is exemplified by board 5, which experienced a permanent SIR drop, for which dendrites were observed on 9 pairs out of the total 11 pairs. A second failure mode, such as that found for board 4 which experienced intermittent SIR drops, consisted of surface contamination rather

than dendrites. A third failure mode was that of board 11 which displayed no SIR drops, in which dendrites were observed on 2 pairs out of the total 11 pairs.

Table 4.3 Test summary and SIR failures

Sample No.	Plating	Substrate	Solder	Flux	SIR Failure Time (hours)	Contact Pairs with Dendrites
1	HASL	FR4	SnPb	No-clean-rosin	N/A	0/11
2	Imm Ag	FR4	SAC	No-clean-resin	N/A	0/11
3	ENIG	PI	SnAg	Rosin	N/A	0/11
4	Imm Ag	PI	SAC	No-clean-resin	2096 (intermittent) 2512 (intermittent)	0/11 (Surface contamination)
5	Imm Ag	PI	SnAg	Rosin	2430 (permanent)	9/11
6	ENIG	FR4	SAC	No-clean-resin	N/A	0/11
7	ENIG	PI	SAC	No-clean-resin	2098 (intermittent)	1/11
8	Imm Sn	FR4	SAC	No-clean-resin	N/A	0/11
9	Imm Sn	PI	SAC	No-clean-resin	N/A	0/11
10	OSP	FR4	SAC	No-clean-resin	3961 (permanent)	1/11
11	Sn	PI	SAC	No-clean-resin	N/A	2/11
12	Sn	PI	SnAg	Rosin	N/A	0/11
13	Imm Sn	PI	SnAg	Rosin	3820 (permanent)	2/11
14	HASL	FR4	SnPb	No-clean-rosin	N/A	0/11
15	Imm Ag	FR4	SAC	No-clean-resin	N/A	0/11
16	ENIG	PI	SnAg	Rosin	3610 (permanent)	3/11

4.4.1 Causes of SIR Intermittent Failures

During the 8,170 hours THB testing, there were two PCBs exhibiting surface insulation resistance (SIR) intermittent failures. One is board 4, which experienced SIR drops below the failure criteria twice. The first time was at 2096 hours, and the second time was at 2512 hours. Then, the SIR recovers to the level of 10^{10} Ohms, which can be seen from Figure 4.2. Another one is board 7, which experienced one SIR drop below the failure criteria around 2098 hours. The SIR graph of this board 7 is shown in the Figure 4.3**.**

Although both of the failures exhibited intermittent SIR drops at the appearance level, the root causes of the failure for each PCB are different and needed to be investigated at a the deeper level. With optical inspection, there are fiber contaminations detected on position 4 of board 7, which can be seen from Figure 4.4**.** The fiber, bridging the electrodes of the test structure, builds a path for conductive ions to migrate when the electrolyte medium forms. Under the humidity testing environment, the moisture molecules accumulated along the fiber and desolved the flux residues to form the conductive electrolyte. The fiber is composed of organic material but not of any metallic elements. The ESEM and EDS map of the fiber contamination is shown in Figure 4. 5**.**

The root cause of intermittent SIR drops for board 7 is the metallic dendrite bridging the two electrodes of the testing specimens. The solder alloy used on board 7 is SAC lead-free solder, which contains 96.5%Sn, 3%Ag and 0.5Cu. Based on the ESEM and EDS analysis, which is shown in Figure 4.6**,** the metallic dendrite is composed solely of Sn. The reaction at the anode side is: (1) $Sn \rightarrow Sn^{2+} + 2e^-$ (2)

$H_2O \rightarrow \frac{1}{2}O^2$+2$H^+$+2$e^-$ (3) Sn + H_2O → SnO+2H^++2 e^-. The reaction between two electrodes: (1) Sn^{2+} +2OH^- → SnO + H_2O (2) Sn^{2+}+ 2OH^- → $Sn(OH)_2$. The reaction at the cathode side: (1) Sn^{2+} + 2 e^- → Sn (2) O_2 + 2 H_2O + 4e^- → 4OH^- (3) 2H_2O+ 2e^- → H_2 + 2OH^- (4) Sn^{2+} +2OH^- → SnO + H_2O (5) Sn^{2+}+ 2OH^- → $Sn(OH)_2$

At the anode, the Sn dissolves into the electrolyte to form Sn^{2+} ions. Then, the Sn^{2+} combine with OH^- to form $Sn(OH)_2$. Because the solubility of $Sn(OH)_2$ is low, the Sn^{2+} ions escapes and moves toward the cathode after an incubation period. When the Sn^{2+} ions reach the cathode, the electrodeposition occurs, in which the Sn deposited on the cathode and then the Sn filaments grows and metallic dendrite are formed.

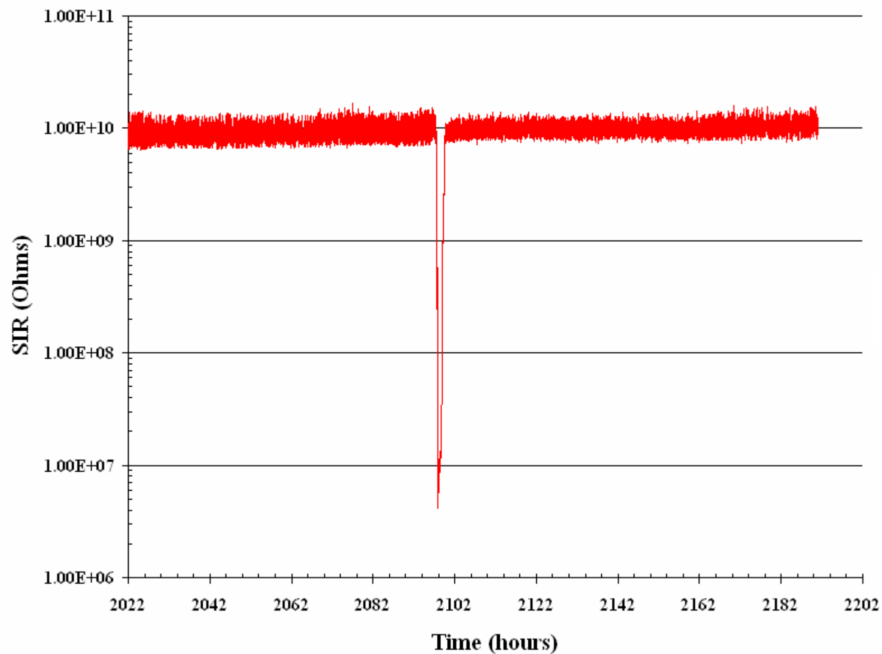

Figure 4.2 Graph of SIR for board 4 processed with resin based flux and SAC lead-free solder under fixed THB condition 6

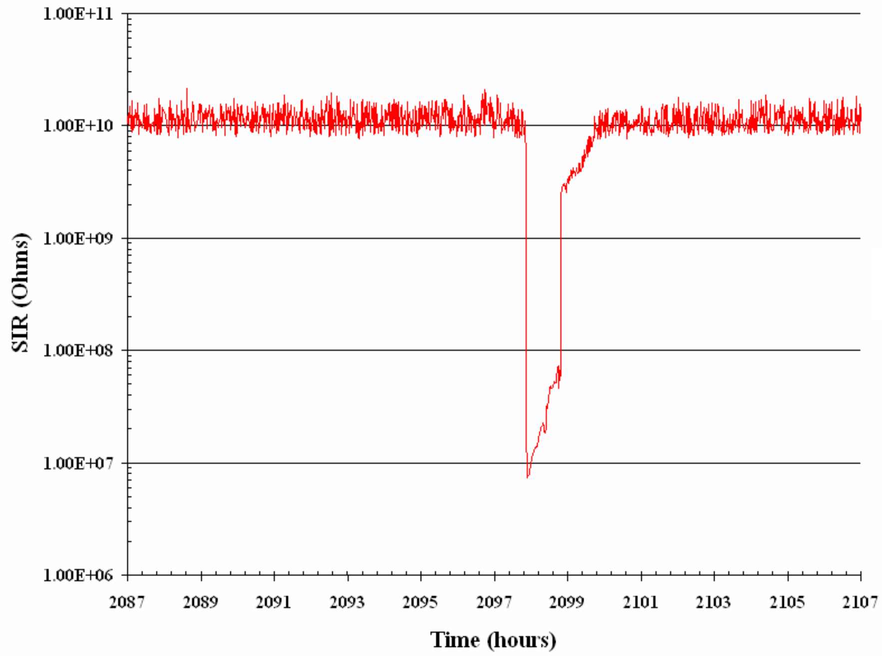

Figure 4.3 Graph of SIR for board 7 processed with resin based flux and SAC lead-free solder under fixed THB condition 6

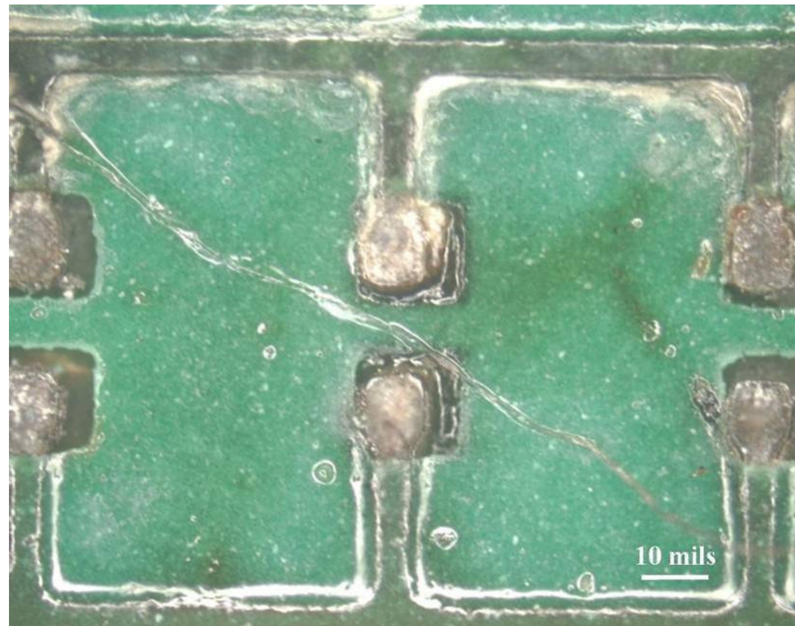

Figure 4.4 Optical micrographs of SIR for board 7 processed with resin based flux and SAC lead-free solder after 8170 hours of THB exposure

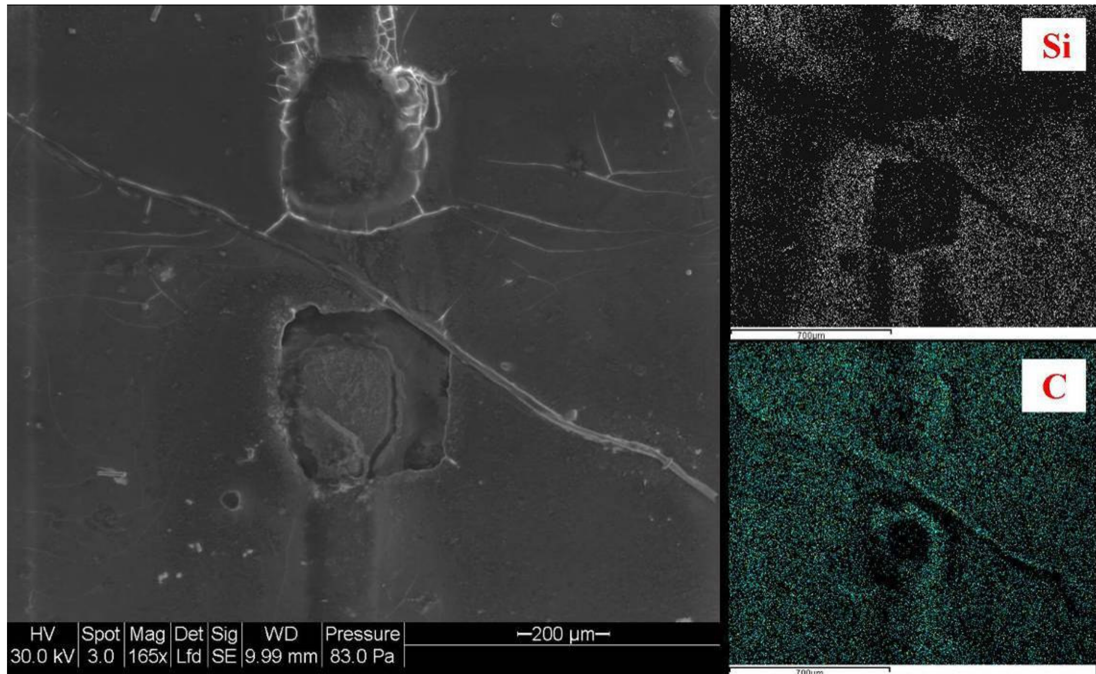

Figure 4. 5 ESEM (left) and EDS map (right) of board 7 processed with resin based flux and SAC lead-free solder after 8170 hours of THB exposure

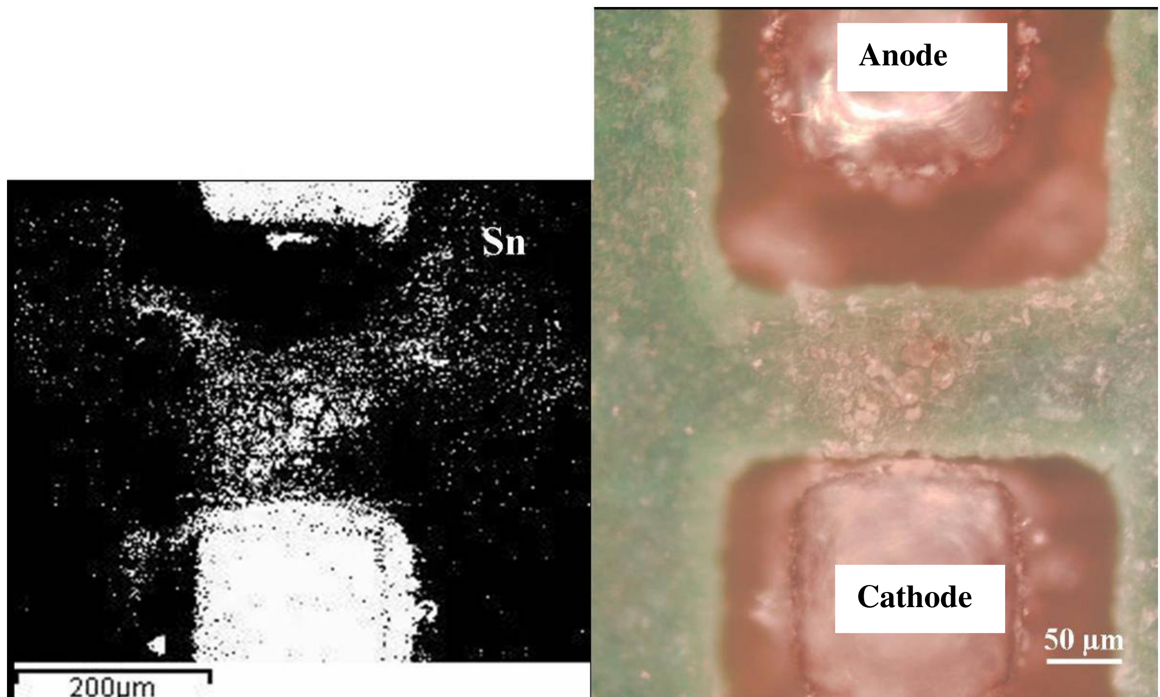

Figure 4.6 EDS map (left) and optical micrograph (right) of board 7 processed with resin based flux and SAC lead-free solder after 8170 hours of THB exposure

4.4.2 Metallic Migration Occurring with Solder Mask and Exposed Substrate Area

The application of solder mask on the surface of a PCB is to secure the solder alloys to be only applied on the solder pad instead of everywhere. The interesting phenomena that has been found in this study is that the surface of the solder mask plays an important role in path formation for the whole electrochemical migration process. Board 13 experienced SIR drops from 3820 hours, shown in Figure 4.7. After being monitored for another 48 hours, board 13 was taken out from the THB chamber for further analysis. Through optical inspection, in Figure 4.8, it was found that there was a dendrite bridging the electrodes, which causes the SIR drops. The point needs to be stressed is that the route that the dendrite chooses to grow along with is not the shortest path between the two electrodes. However, the dendrite choose the path which is along the edge of the solder mask, instead of crossing over the surface of the exposed substrate. The availability of medium is the answer to this phenomenon. Within a humid environment, water molecules prefer to stay at the edge of the solder mask to form the electrolyte making the path for the metal ions migrating. Through the ESEM and EDS analysis, in Figure 4.9, the dendrite is solely composed of Ag. Since the immersion Sn is the plating for this board, the only source for Ag, constituting the dendrite, is coming from the SnAg lead-free solder.

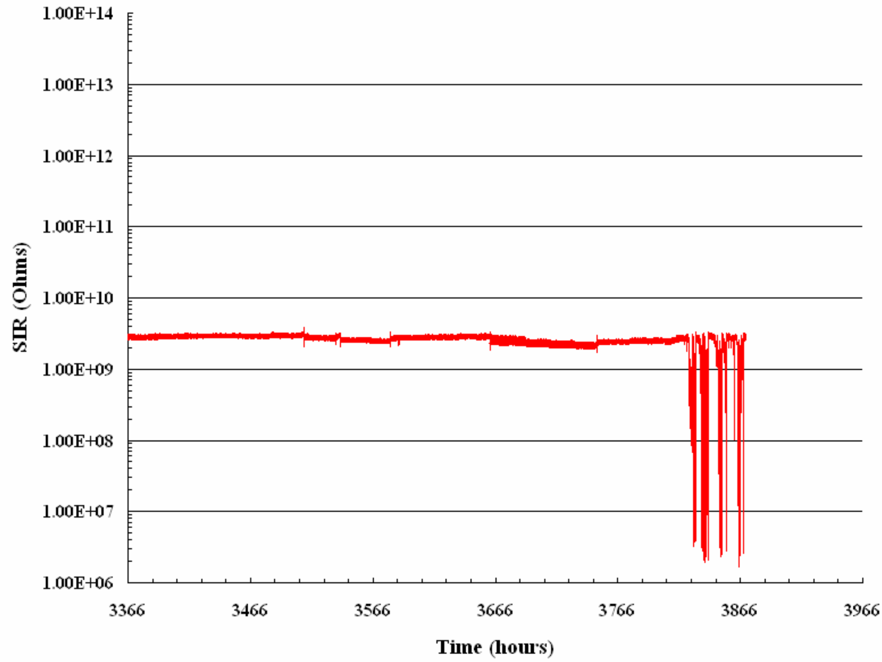

Figure 4.7 Graphs of SIR for board 13 processed with rosin based flux and SnAg lead-free solder under fixed THB condition 6

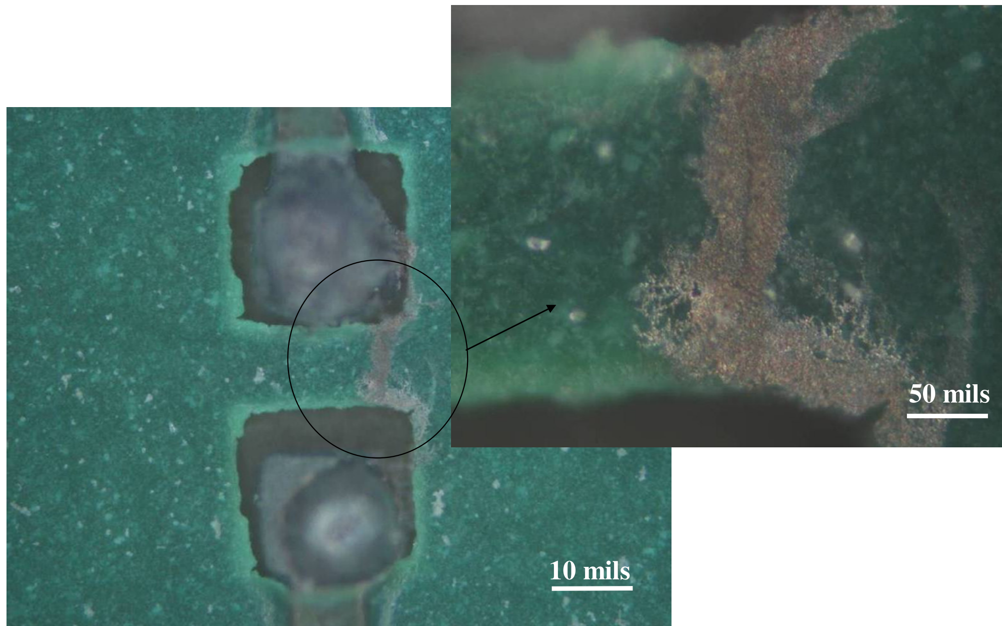

Figure 4.8 Optical Micrographs of SIR for board 13 processed with rosin based flux and SnAg lead-free solder after 3870 hours of THB exposure

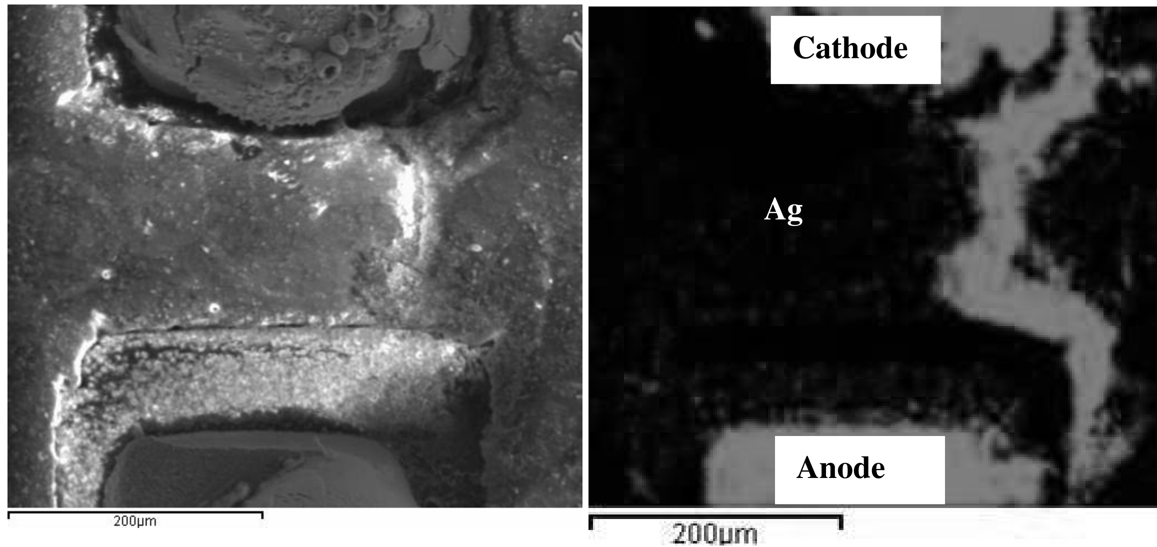

Figure 4.9 ESEM (left) and EDS (right) map of board 7 processed with resin based flux and SAC lead-free solder after 3870 hours of THB exposure

Another metallic migration was detected on position 3 of board 10, which is processed with resin based flux, OSP plating and SAC lead-free solder. The morphology of this migration is abnormal compared with the common structures of other dendrites. In fact, this migration is not a real dendrite according to the view of the morphology. The formation of this migration is determined by the path formation step of the ECM. From the ESEM analysis, in Figure 4.11, there are several cracks detected within the substrate. The crack, crossing over the area between two electrodes, plays the role as the path for migration to occur. Water molecules accumulate on this specific path to form the electrolyte. Then, metallic ions follow this existing path to migrate from anode to cathode. Through the EDS analysis, Ag is the only element migrating in this crack, while the SAC lead-free solder is the only responsible source for this Ag migration.

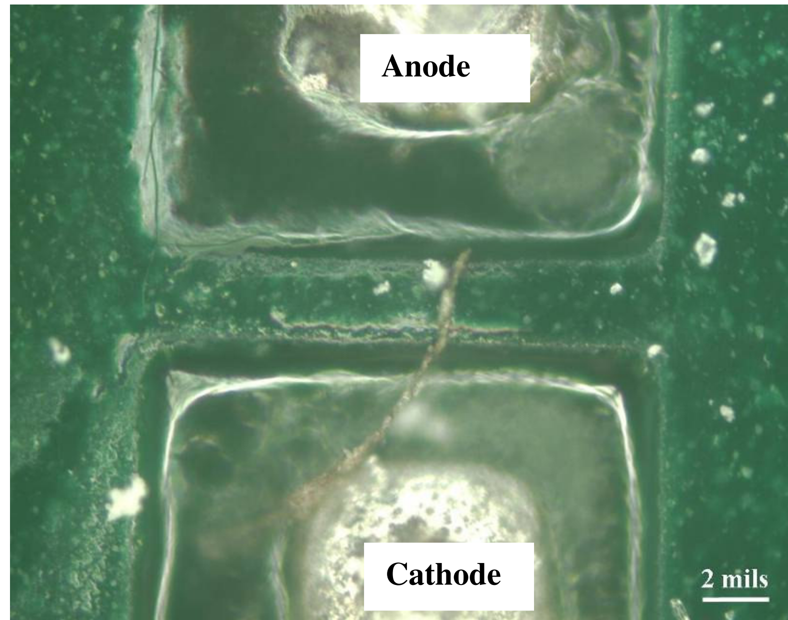

Figure 4.10 Optical Micrographs of SIR for board 10 processed with resin based flux and SAC lead-free solder after 3983 hours of THB exposure

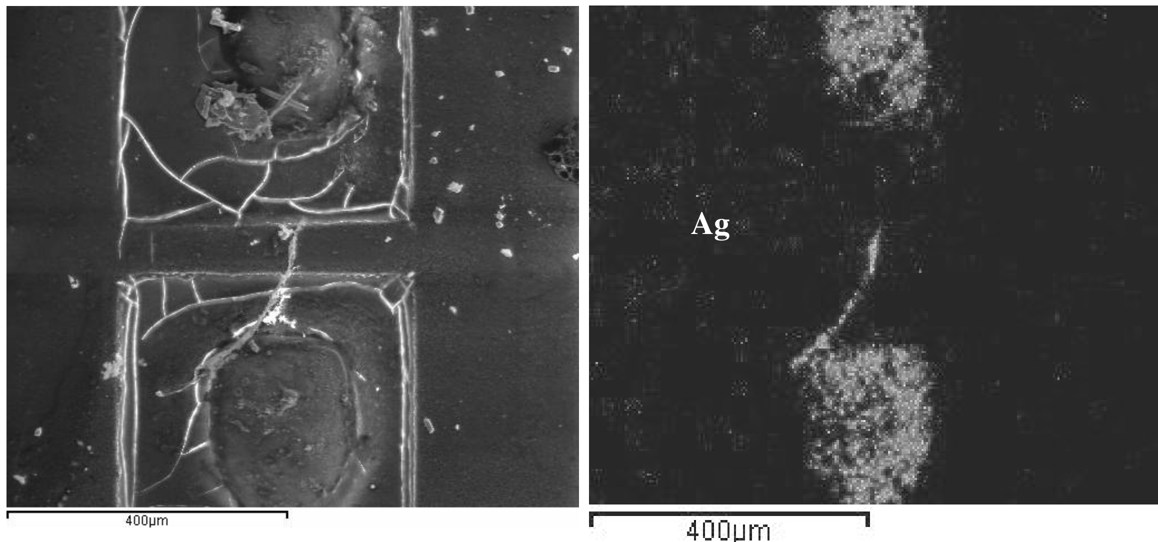

Figure 4.11 ESEM (left) and EDS map (right) of board 10 processed with resin based flux and SAC lead-free solder after 3983 hours of THB exposure

4.4.3 Effect of Substrate Material

Polyimide (PI) is the second most common resin in use today for printed circuit board laminates. Its advantage lies in its high glass transition temperature (Tg) of 260 °C, which stems from the addition of methylene dianiline and maleic anhydride. This property is beyond the peak temperature of most soldering profiles, and helps in high-

performance/high-temperature applications where operational environments exceed the Tg of both FR-4 and HTFR-4.

The resin's chief disadvantage is its tendency to absorb relatively higher levels of moisture and its higher cost. Therefore, in the same relative humidity and temperature environment, the weight gain of moisture absorption for PI substrate is almost 34% higher than that of FR-4 substrate, which was measured in this study. This could help to explain the observation that there are six boards with the dendrites detecgted, and five of these six are PI substrate, which are shown in Table 4.3. Therefore, for electronics assemblies that are expected to survive operating conditions with high temperature and relative humidity, polyimide substrates processed with silver-containing solder may not be suitable or may require a protective coating.

4.4.4 Effect of Temperature and Humidity

Raising the temperature while holding humidity constant was observed to cause a reversible decrease in the SIR. This is explained by the fact that materials have higher moisture absorption capacity at higher temperature for the same relative humidity. Raising the temperature from 40°C to 65°C while keeping the relative humidity at 65% causes a drop in SIR, which is evident in the data between 1260 hours and 1280 hours shown in Figure 4.12. Furthermore, keeping temperature constant while increasing the relative humidity level results a similar reversible decrease in SIR, which may be observed between 1280 hours and 1310 hours in Figure 4.12.

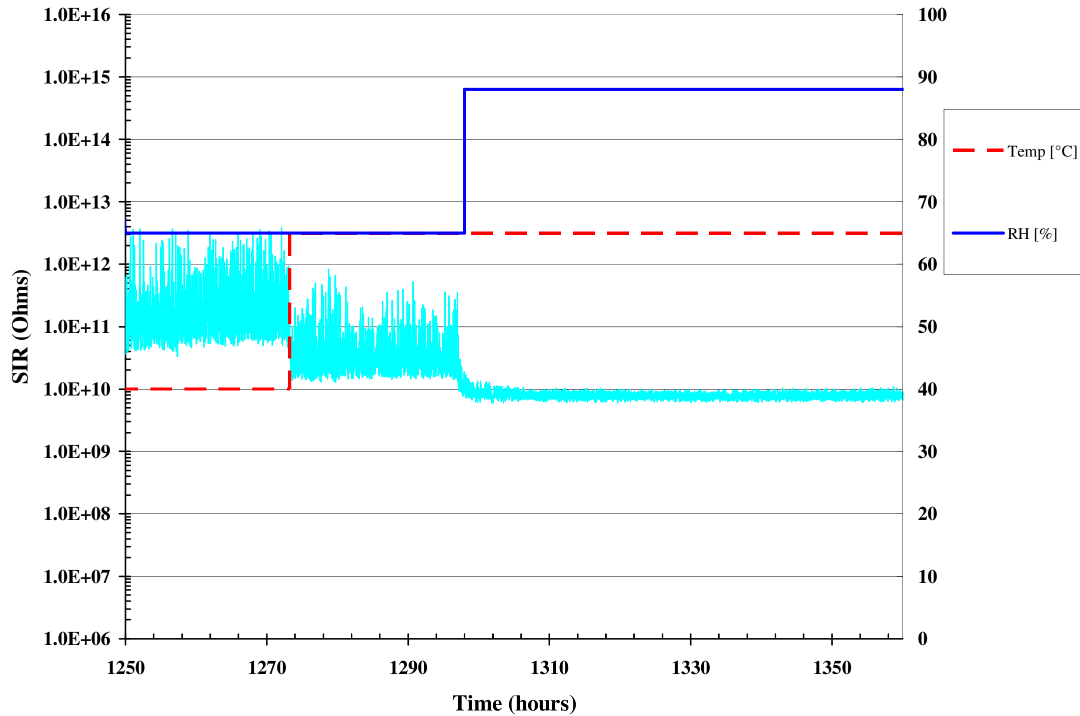

Figure 4.12 SIR graph from THB cycling test

4.5 Conclusions

This study employed temperature-humidity-bias testing to assess the reliability of FR-4 and PI printed circuit boards processed with a variety of solder pastes and solder pad finishes. Exposure to a series of temperature-humidity-bias conditions of increasing severity up to 65°C, 88% RH at 40V produced failures in six samples over a total of 8170 hours of testing. All failures occurred between 2000 and 4000 hours of testing. After 4000 hours of testing no further significant SIR degradation was observed.

Four failed samples showed a persistent sequence of SIR drops. Three of these samples were processed using Sn-3.5Ag solder on polyimide substrate, and the fourth was processed with Sn-3.0Ag-0.5Cu solder on FR-4 substrate. Dendritic growth was detected on all of these boards. Energy dispersive x-ray spectroscopy mapping of

dendrites showed that they were all composed of silver. The only FR-4 board to experience failure was found to have cracks in the substrate. The accumulation of flux residues and moisture in these cracks is believed to have created a preferential path for silver migration. The remaining three of these four boards contained polyimide substrates which absorb relatively higher levels of moisture than FR-4. For a same relative humidity and temperature environment, a PI substrate will typically absorb about 34% more moisture compared with an FR-4 substrate. This increases the risk of ECM for PI substrates processed with silver-containing solder.

Two of boards failed intermittently and then recovered. These boards, processed using Sn-3.0Ag-0.5Cu solder on polyimide substrate, were both found to have surface contamination.

The risk of ECM with lead-free solders, such as silver containing solder, was found to be higher than that for tin-lead solders. For electronic assemblies expected to survive operating conditions involving high temperature and relative humidity, polyimide substrates processed with silver-containing solder may require a protective coating. It may also be advisable in such cases to use larger conductor spacings whenever possible to increase lifetime. It is clear from the results of this study that intermetallic compounds in Sn-Ag and Sn-Ag-Cu alloys do not prevent silver migration on boards assembled with these solders. Thus, susceptibility of lead-free PCBs to SIR reduction and dendritic growth should be thoroughly characterized by manufacturers of products which may operate at high temperature and relative humidity.

CHAPTER 5: RELIABILITY OF EUTECTIC TIN-LEAD HASL FINISH PRINTED CIRCUIT BOARDS PROCESSED USING NO-CLEAN FLUX TECHNOLOGY IN TEMPERATURE-HUMIDITY-BIAS CONDITIONS

5.1 Abstract of Testing Findings

Printed circuit board (PCB) specimens containing three different IPC-B-25 test structures were exposed to temperature-humidity-bias conditions in order to evaluate the effects of no-clean flux chemistry, conductor spacing, voltage bias and test environment on surface insulation resistance (SIR). Results indicate that the SIR failure rate with rosin-based no-clean flux was observed to be greater than that with aqueous-based no-clean flux. This is explained by the higher activity of the flux residues, and the higher concentration of the weak organic acid (WOA) in the rosin based flux residues. Flux residues combined with adsorbed moisture from the environment to form an acidic medium, occasionally breaking through the passivation layer on the electrodes. Then, the resistance level is decreased caused by conductive flux residues bridging the electrodes. The repeated penetration and rehealing of the passivation layer resulted in intermittent SIR drops, which could severely affect the reliability of electronics assemblies. Conductor spacing was observed to represent a factor in the electrochemical migration (ECM) process independent of electric field, indicating that updated test structures are required to predict the reliability of today's high density assemblies.

Temperature-humidity-bias (THB) testing is a widely accepted accelerated test method for assessing PCB materials for their susceptibility to degradation of surface

insulation resistance (SIR) and electrochemical migration. The present study reports the effects of no-clean flux chemistries on SIR of hot air solder level (HASL) plated parallel conductors when subjected to various THB conditions. Moreover, this study provides recommendations for accelerated testing and updates that are needed to current industry standards to ensure relevance of test results to field reliability.

5.2 Reliability Concerns

The electronics industry is continuing the transition to no-clean halide-free fluxes. Yet, such industries as automotive, telecommunication, medical, and others that experience harsh environments with uncoated no-clean PCBs remain concerned about electrochemical migration.

Currently the electronics industry uses qualification tests such as temperature-humidity-bias in an attempt to assess the likelihood of ECM induced failures. Such tests are described in various standards, including IPC-TM-650 section 2.6.3.3, "Surface Insulation Resistance, Fluxes" [3], IPC-TM-650 section 2.6.14.1, "Electrochemical Migration Resistance Test" [3], G-78-CORE section 13.1.5, "Electrochemical Migration" [4], J-STD-004, "Surface Insulation Resistance" [5], and IEC 61189-5, "Surface Insulation Resistance" [6]. Table 5.1 illustrates the differences seen within the electronics industry on how to conduct surface insulation resistance testing. For instance, the applied voltage bias ranges from 5V in the IEC 61189-5 standard [6] to 50V in IPC-TM-650 section 2.6.3.3 [3]. Variations in specified test duration are equally dramatic, ranging from 72 hours to 500 hours. There are also significant differences in test voltage, failure criteria, and environmental conditions, leaving it to the board manufacturer, assembler to decide

which standard to use. It may require a considerable amount of time and resources to qualify PCBs to one or more of these standards.

Since temperature-humidity-bias testing with SIR monitoring requires considerable time, human labor, and specialized equipment, choosing an inappropriate comb spacing to accelerate ECM testing can delay product development by inaccurately predicting the reliability of electronics assemblies. Therefore, updating current industry standards to conform to current product design and material systems is necessary.

Table 5.1 Electrochemical migration qualification tests

Standard	Environment	Bias Voltage	Test Voltage	Test Duration	Failure Criteria
IPC-TM-650 2.6.3.3[3]	**85°C/85% RH**	**50 V**	**100 V**	**168 hours**	**SIR<1 x 10^9 ohms**
IPC-TM-650 2.6.14.1[3]	**40°C/93% RH 65°C/88% RH 85 °C/85% RH**	**10 V**	**100 V**	**500 hours**	**No Dendrites**
J-STD-004[5]	**85°C/85% RH**	**48 V**	**100 V**	**168 hours**	**SIR<1 x 10^8 ohms**
GR-78-CORE Section 13.1.5[4]	**65°C/85% RH**	**10 V**	**45-100 V**	**500 hours**	**No Dendrites**
IEC 61189-5 (in draft)[6]	**40°C/93% RH**	**5 V**	**5 V**	**72 hours**	**----**

5.3 Experiments

To determine the most effective conditions for assessing no-clean fluxes with respect to electrochemical migration, three types of flux were tested under various accelerated conditions. The types of flux and the corresponding test conditions are summarized in Table 5.2. This table shows the three temperatures and relative humidity environments which were used for each flux sample. In this study, three boards were tested for each bias voltage at each temperature-humidity testing condition.

Table 5.2 Experimental design for qualification of PCBs processed with no-clean flux

Flux	A	B	C
Type	Aqueous	Rosin	Aqueous
Form	Liquid	Liquid	Solder Paste
Thickness (microns)	120	120	150
Voltage (VDC)	6, 12, 24	6, 24	6, 12, 24
Environment (^{o}C/%RH)	40/93 65/95 85/85	40/93 65/95 85/85	40/93 65/95 85/85

The two liquid fluxes and solder paste selected for qualification testing are commonly used in PCB assembly and rework processes. The no-clean fluxes used in this study, consisting of a rosin and an aqueous-based flux, are representative of those used in manufacturing and rework processes. Following the IPC J-STD-004 standard [5], the rosin-based flux and aqueous-based flux are "ROM0" and "ORL0" respectively. The no-clean designation means the residues can be left on the board.

The test vehicles used in this study were IPC-B-25 test boards, as seen in Figure 5.1. These boards each consisted three comb patterns, with 6.25, 12.5 and 25 mil spacing (equivalent to 0.16, 0.32 and 0.64 mm). This spacing is in agreement with

current lead spacings in fine-pitched plastic packages. In order to investigate current leakage and dendritic growth between solder joints, the comb patterns were coated with a eutectic (63Sn/37Pb) solder applied by hot air solder leveling (HASL).

Each of the IPC-B-25 test coupons was inscribed with sample identification information on the unbiased side of the PCB. All test coupons were cleaned after processing and identification, and prior to application of no-clean flux, to remove contaminants present from the board manufacturing process. Cleaning was performed by soaking the boards for one hour at 80°C in a solution of isopropyl alcohol and deionized water. The average measured surface insulation resistance (SIR) of the boards after cleaning was 2 x 10^{12} Ohms. The flux was applied by an airbrush technique with a fine mist evenly distributed over the entire PCB surface. Boards were allowed to dry for 24 hours before reflow processing. Reflow was performed by Capital Electro-circuits in Gaithersburg, MD using their standard eutectic Sn-Pb reflow profile.

The environmental conditions were selected on the basis of recommendations in industry standards for accelerating ECM as shown in Table 5.1. Bias voltage of 6V and 24V were selected for all three flux types in order to cover a wide range of practical application conditions for electronic products. Two flux types were also tested at 12V bias to provide additional insight into voltage effects. For instance, 12V is the voltage of a common car battery, and 24V is commonly used in large diesel engine vehicles because of the larger power requirements for the starter.

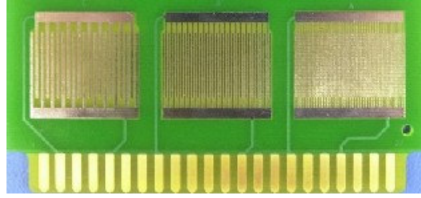

Figure 5.1 IPC-B-25 test coupon (conductor spacing are 25 mil (0.64 mm), 12.5 mil (0.32 mm), and 6.25 mil (0.16 mm), from left to right)

Surface insulation resistance (SIR) test systems are commonly used in detecting leakage current on a PCB. In the absence of condensation, sources of leakage current include ECM [40], conductive filament formation (CFF) [41][42] (similar to ECM but beneath the board surface), and other surface anomalies, such as flux residues, that create a conductive path. In cases where CFF is not a factor, 99.9% of the current leakage on an FR4 PCB will occur on the surface of the board even though SIR reflects both surface and bulk conduction paths [37]. Once a dendrite bridges two conductors, a sharp drop in surface insulation resistance is experienced between the conductors. According to the standards listed in Table 5.1, a PCB is considered failed when the resistance drops below approximately 100 megohms. An SIR system capable of detecting ECM failures according to these requirements must be designed to measure a level of surface insulation resistance no less than 10^{10} Ohms. The system used in the present study had a detection limit of 10^{11} Ohms and included a one-megohm resistor in series with each SIR test structure, which served to limit the current to prevent fusing of dendrites due to high current density [44]. The SIR value of each test board was recorded once every 55 seconds.

5.4 Experiments Results and Discussion

Temperature-humidity-bias tests of fixed, 168 hour duration were performed to assess the effects of conductor spacing, voltage bias, flux chemistry, and temperature-

humidity conditions on stability of surface insulation resistance. Analysis of the SIR data, combined with physical analysis of the test specimens, provided insight into the causes of observed SIR degradation and the experimental conditions which were more conducive to electrochemical migration.

5.4.1 Effect of Flux Selection and Flux Residues

Based solely on SIR measurements, the deactivated rosin-based flux (B) was the most active flux at all the temperature-humidity testing conditions. This is illustrated for the 40°C/93% RH environment with an applied 6V bias as seen in Figure 5.2, Figure 5.3 and Figure 5.4. This activity may have been caused by moisture absorbed into conductive residues left by the flux that created a path for conduction causing the sharp drops in resistance seen in Figure 5.3.

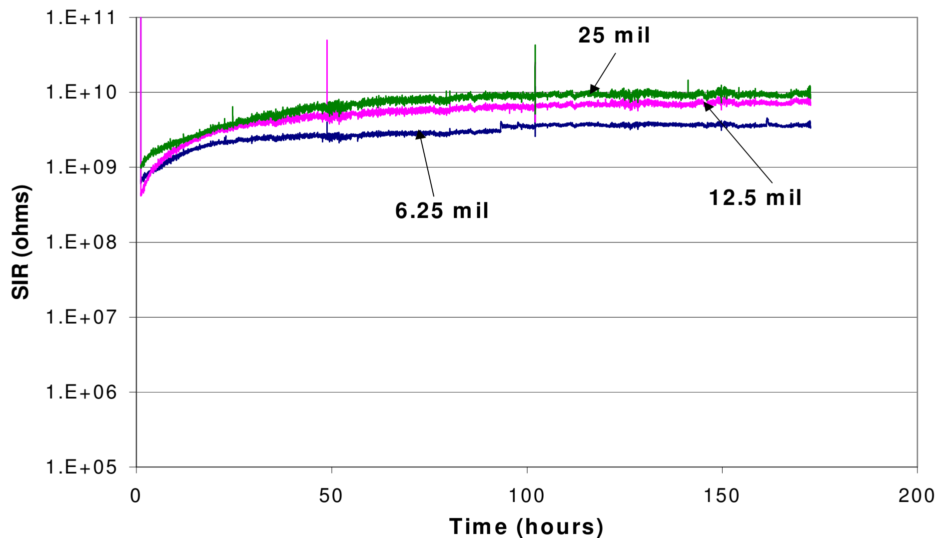

Figure 5.2 SIR graph of PCB processed with deactivated aqueous-based flux (A) exposed to a 40°C/93% RH environment with an applied 6V bias.

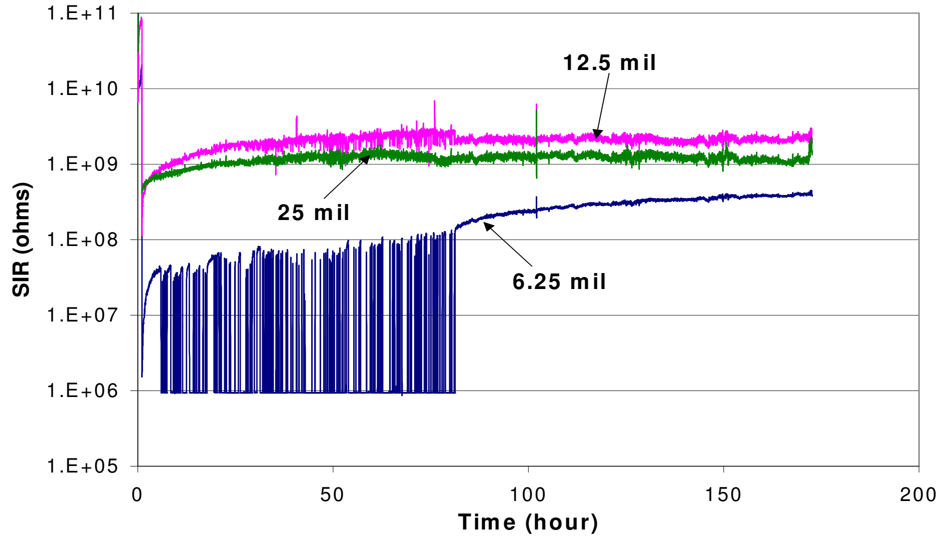

Figure 5.3 SIR graph of PCB processed with deactivated rosin-based flux (B) exposed to a 40°C/93% RH environment with an applied 6 V bias.

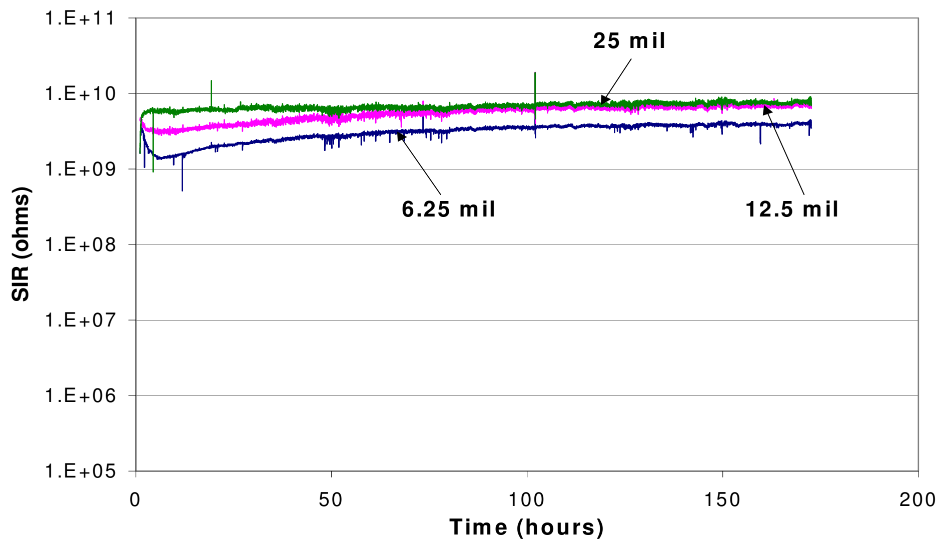

Figure 5.4 SIR graph of PCB processed with deactivated aqueous-based solder paste (C) exposed to a 40°C/93% RH environment with an applied 6V bias.

The deactivated aqueous-based flux (A) did not exhibit a noticeable variation in SIR as voltage increased at the 40°C/93% RH condition. No dendrites were observed optically, so several locations on the 6.25 mil (0.16 mm) comb structure were inspected with an environmental scanning electron microscope (ESEM) to eliminate the possibility of dendritic growth. Analysis by energy dispersive spectroscopy

(EDS) did not reveal any significant concentrations of copper, tin, or lead on the laminate as seen in Figure 5.5.

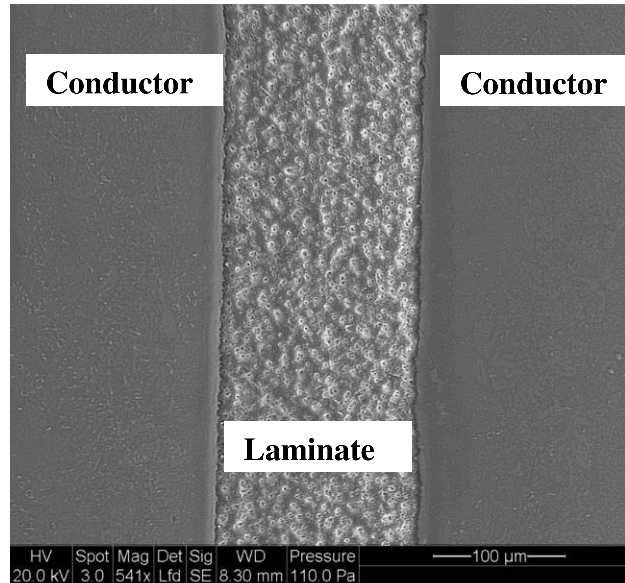

Figure 5.5 ESEM picture of deactivated aqueous-based flux (A) exposed to a 40°C/93% RH environment with an applied 6V bias.

Rosin-based flux (B), at 6 V and 6.25 mil (0.16 mm) conductor spacing, experienced frequent sharp drops in resistance for the first 75 hours of SIR testing as seen in Figure 5.3, which was consistent with the two replicate flux (B) boards tested at these conditions. Microscopic analysis revealed no indication of dendrites bridging the conductors for the any of these samples. Furthermore, the SIR exhibits an overall trend of increasing time, which may be seen in Figure 5.3.

The behavior described above can be explained through the theory of passive corrosion, which is the most common form of corrosion, in combination with conductive flux residues bridging the narrow conductor spacing. A passive corrosion process generates reaction products that severely retard the rate of corrosion. The reaction products, usually oxides, coat the metal surface, thus passivating it from further corrosion. The comb patterns contained a eutectic (63Sn/37Pb) HASL coating,

which is highly corrosion resistant [49]. After the formation of the passivation layer, the rate of corrosion is dependent upon either the rate of diffusion through the passivation layer or upon the removal of that layer. If the corrosion mechanism is dependent upon diffusion, the rate of corrosion will slowly retard as the passivation layer thickens. This describes the observed trend for the base level of SIR, which rose rapidly at the beginning of the test and then more gradually as the test progressed. Breaching of the passivation layer will cause the rate of corrosion to fluctuate as the layer is penetrated and then reforms. This explains the series of intermittent SIR drops observed during the first 75 hours of testing. Flux residues combined with absorbed moisture from the environment to form an acidic medium. Lead oxide does not form a stable passivation layer and tin is known to undergo corrosion in acidic environments. Thus the oxide layer was attacked, periodically exposing the electrode metal to the conductive flux residues. This led to a drop in SIR until the breach was healed by reformation of oxide.

For the aqueous-based solder paste (C) boards exposed to a $40^{o}C$/93% RH environment at 6V and 12V, the SIR was stable throughout the test for all three spacings and never dropped below 10^{8} ohms, which is the failure criterion. This is in contrast to the behavior of SIR at 24V. As seen in Figure 5.6, drops in SIR occur on the 25 mil (0.64 mm) and the 6.25 mil (0.16 mm) conductor spacing and are representative of what would occur when dendrites grow and bridge the conductor. No dendrites were observed optically, but the solidified flux from the solder paste did bridge the gap between conductors at several locations on the 6.25 mil (0.16 mm) comb structure as seen in Figure 5.7.

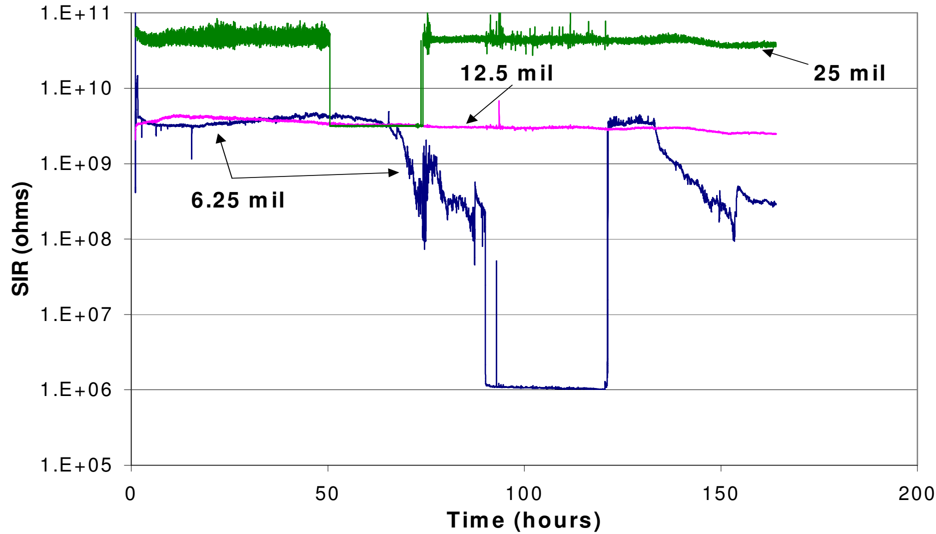

Figure 5.6 SIR trends for PCB processed with deactivated aqueous-based solder paste (C) exposed to a 40°C/93% RH environment with an applied 24V bias.

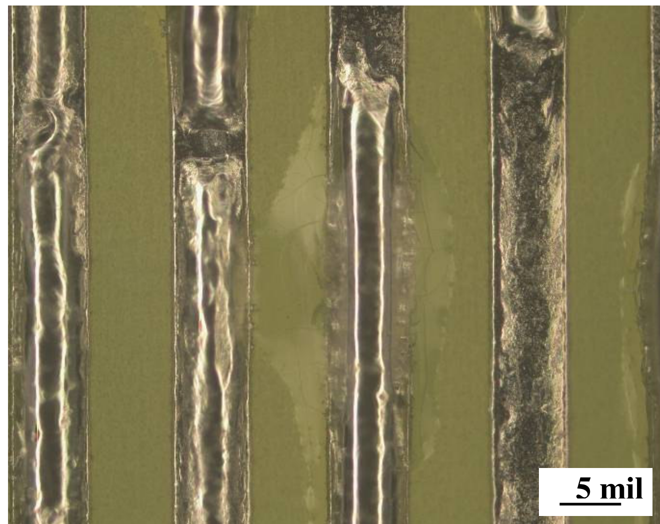

Figure 5.7 Flux residue from aqueous-based solder paste (C), 6.25 mil (0.16 mm) conductor spacing, bridging conductors on board exposed to a 40°C/93% RH environment with an applied 24V bias.

Higher failure rates were observed for PCBs processed with rosin-based flux as compared with the PCBs processed with aqueous-based flux. This suggested that the flux residues from rosin-based flux have a higher degree of reactivity than those from aqueous-based flux. To measure the relative reactivity of the two types of flux residue,

potentiostat measurements were performed on extracts from deactivated (reflowed) flux.

Flux residues were extracted by soaking in a warm solution of deionized water and isopropyl alcohol. From the corrosion current measured at the corrosion potential for each sample, the potentiostat allowed calculation of corrosion rates, which provide a relative measure of reactivity. For deactivated aqueous-based flux (A), the corrosion rate is 2±0.3 µm /year; for deactivated rosin-based flux (B), the corrosion rate is 14±7 µm /year. These results confirm that residues from the rosin-based flux have higher reactivity than those from aqueous-based flux. Since weak organic acids (WOAs) have been identified as a component of flux residues that can contribute to reduction in SIR [48], an analysis of the WOA content of the flux residues was undertaken to establish whether this would explain the differing reactivity of the two types of flux. Extracts were analyzed by ion chromatography (IC) in order to determine the composition and amount of weak organic acids contained in the flux residues remaining on PCB surfaces after reflow. The test results show that the total amount of weak organic acid was 20500 ppm for deactivated aqueous-based flux (A) and 33500 ppm for deactivated rosin-based flux (B). According to the size of the PCB area, the concentration levels were 113µg/in^2 for aqueous-based flux and 185µg/in^2 for rosin-based flux. Therefore, residues from the rosin-based flux contained about 50% higher concentration of WOA than those from the aqueous-based flux. Together with the potentiostat results, this helps to explain the higher reactivity observed experimentally for the rosin-based flux.

5.4.2 Effect of Electric Field

The voltage bias is directly proportional to the force applied to a charged particle (e.g., a metallic ion) within an electric field, which exists on the surface of PCBs. The force applied to a charged particle will determine the time it takes an ion to move through the electrolyte solution [38].

The electric field can be calculated from the applied voltage and the geometry of the structure under consideration. For parallel conductors, E=V/d, where E is the average electric field, V is applied voltage, and d is the distance separating two oppositely biased conductors [38]. Therefore, as the voltage bias is increased or the spacing is reduced, the higher electric field may accelerate electrochemical migration. For a comb structure with 6.25 mil (0.16 mm) spacing under a 6V bias, the electric field is approximately 1V/mil, and for a 24V bias, it is 4 V/mil. From the test results, no failures were found at any voltage level for 12.5 mil (0.32 mm) and 25 mil (0.64 mm), even though the electric field of 24V/12.5 mil (2 V/mil) was higher than that for 6V/6.25 mil (1V/mil). This suggests that the spacing plays a role in ECM independent of the electric field. The longer time required for continuous path formation at longer spacings may manifest itself as a larger incubation period prior to dendrite nucleation, lengthening the time to ECM failure even when the electric field driving ion transport is the same or greater than at smaller spacings. This observation is particularly significant in view of the ongoing trend in the electronics industry toward reduced spacings on PCBs. The absence of observed electrochemical migration or SIR failures for 12.5 mil (0.32 mm) and 25 mil (0.64 mm) conductor spacings also suggests that industrial and military specifications [2][3][5][6][47] based on older PCB designs need to be updated to correctly assess reliability of higher density PCB designs. The

resources expended on THB testing would be more effectively used by replacing 25 mil (0.64 mm) comb structures with those having lower spacings that accurately reflect their higher risk for SIR drops.

5.4.3 Effect of Temperature and Humidity

Keeping humidity constant, boards with deactivated aqueous-based flux (A) biased at 6V displayed approximately half an order of magnitude decrease in SIR between 40°C and 65°C, and no difference between 65°C and 85°C for all conductor spacings. At the higher voltages of 12V and 24V, for all conductor spacings, there was a decrease of approximately one order of magnitude in SIR as the temperature increased from 40°C to 85°C. For boards processed with deactivated aqueous-based flux (A) exposed to a 65°C/95% RH environment, SIR graphs for tests at 12V and 24V bias showed frequent singularities representative of moisture condensation as seen in Figure 5.3. ESEM analysis confirmed that dendrites did not cause these intermittent drops.

Deactivated rosin-based flux (B), with an applied 6V bias, exhibited no significant difference for all conductor spacings in the overall SIR trend between the 40°C/93% RH, 65°C/95% RH and 85°C/85% RH conditions. There were two dendrites detected on the rosin-based flux (B), 6.25 mil (0.16 mm) conductor spacing, exposed to a 65°C/95% RH environment with an applied 6 volt bias as shown in Figure 5.8, but no dendrites were detected at the 6V 40°C/93% RH and 6V 85°C/85% RH conditions on the rosin-based flux (B) boards. No distinguishable SIR trend was found for the deactivated rosin-based flux (B) at 24V when looking at the effect of increasing temperature.

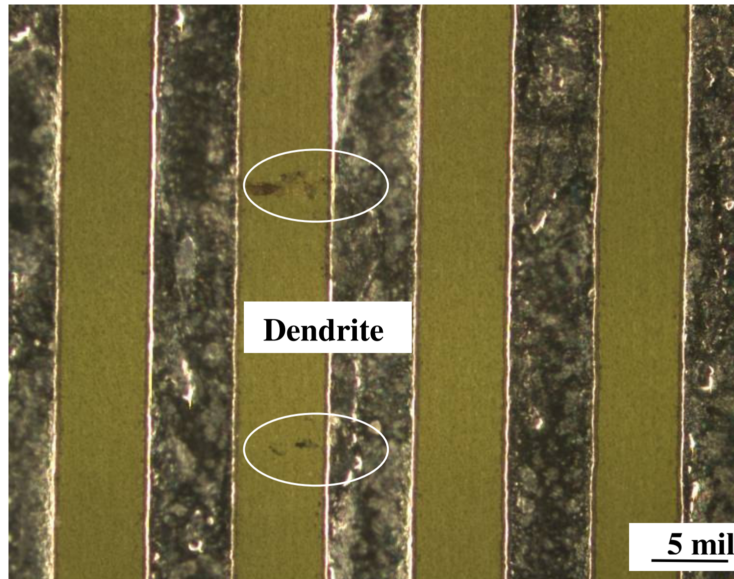

Figure 5.8 Deactivated rosin-based flux (B), 6.25 mil (0.16 mm) conductor spacing, exposed to a 65°C/95% RH environment with an applied 6V bias. Two dendrites were observed on this board without affecting the SIR graph.

The aqueous-based solder paste (C), at applied bias of 6V, 12V, and 24V, showed on average a one order of magnitude decrease in SIR values between 40°C/93% RH and 85°C/85% RH, as shown in Figure 5.9 and Figure 5.10. The brief gaps exhibited in Figure 5.10 were caused by power outages. In the 65°C/95% RH environment, a few copper dendrites were observed as shown optically in Figure 5.11. Dried flux residues adjacent to the conductor on the right side of the image promoted dendritic growth. One of these dendrites extended to the adjacent conductor and created a short. EDS mapping (shown in Figure 5.12) revealed that the dendrite was composed primarily of copper, which indicates that copper migrates more readily than tin or lead in the present test conditions.

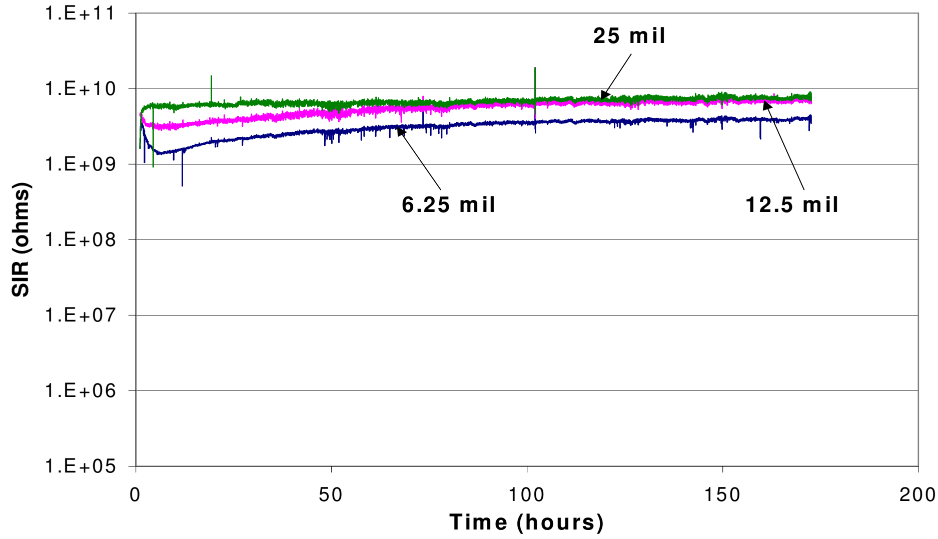

Figure 5.9 SIR graph for PCB processed with deactivated aqueous-based solder paste (C) exposed to a 40°C/93% RH environment with an applied 6 V bias.

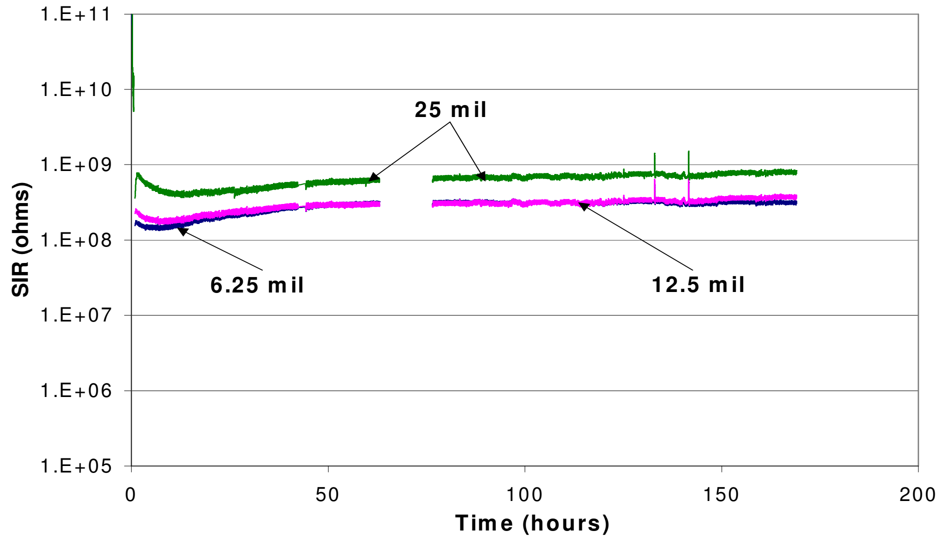

Figure 5.10 SIR graph for PCB processed with deactivated aqueous-based solder paste (C) exposed to an 85°C/85% RH environment with an applied 6 V bias.

Figure 5.11 Aqueous-based solder paste (C), 6.25 mil (0.16 mm) conductor spacing, exposed to a 65°C/95% RH environment with an applied 6V bias.

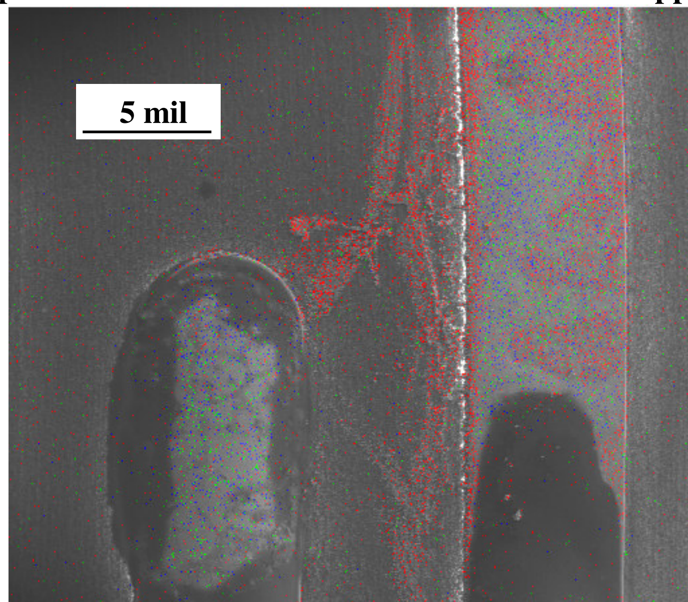

Figure 5.12 EDS overlay on an ESEM picture of aqueous-based solder paste (C), 6.25 mil (0.16 mm) conductor spacing, exposed to a 65°C/95% RH environment with an applied 6V bias. EDS mapping indicates that the material bridging the conductors is mostly copper (shown in red). Tin (in green) and lead (in blue) are restricted largely to the conductor surfaces.

5.5 Conclusions

It was found that aqueous-based no-clean fluxes are more resistant to ECM and drops in SIR than rosin-based no-clean fluxes. Thus, extrapolating the behavior of

conventional aqueous-based fluxes and rosin-based fluxes to no-clean flux chemistries could lead to erroneous expectations. From the SIR test results, it is clear that the risk of ECM with rosin-based no-clean flux is at least as great as that with aqueous-based no-clean flux. Residues of rosin-based flux were found to contain about 50% larger concentration of weak organic acids after reflow. This increased their reactivity and promoted moisture adsorption, further reducing the time-to-failure due to SIR reduction.

For aqueous-based flux at 12 volts and 24 volts bias, the SIR at 85^oC and 85% RH was approximately one order of magnitude less than SIR at 40^oC and 93% RH. At 6 volts bias the difference in SIR level was smaller, approximately half an order of magnitude between 40^oC and the higher temperatures. The aqueous-based solder paste, across all bias levels, showed a one order of magnitude decrease in average SIR between 40^oC/93% RH and 85^oC/85% RH.

In contrast to the aqueous-based fluxes, no overall trends in SIR were found for the rosin-based flux at 6 or 24 volts between the three temperature-humidity conditions which were examined. In some cases, the background level of SIR increased by half an order of magnitude for the first 75 hours, but this was accompanied by intermittent drops. A plausible explanation was offered for this behavior based on passive corrosion with repeated penetration and rehealing of the passivation layer on the electrodes.

Conductor spacing was found to be a factor in the ECM process independent of electric field. Current industry standards recommend a spacing of 25 mil (0.64 mm) in specimens used for ECM testing. Nevertheless, smaller spacings of less than 12.5

mil (0.32 mm) are already widely used in electronic products today. The observation that electric field alone was not sufficient to accelerate all the steps in the ECM process suggests that industry and military specifications and test standards based on older PCB designs are not suitable for assessing the reliability risk associated with ECM in higher density products. Successful prediction of susceptibility to ECM requires test structures with comparable spacings, which are produced using the same production materials and processes as the electronic products whose reliability is to be evaluated through accelerated testing.

CHAPTER 6: ELECTROCHEMICAL MIGRATION ON LEAD-FREE PRINTED CIRCUIT BOARDS WITH PROTECTIVE COATING-SOLDER MASK

6.1 Abstract of Research Findings

Printed circuit board (PCB) specimens containing three different IPC-B-25 test structures, 4 mil, 6 mil and 12 mil (equivalent to 0.10, 0.15 and 0.30 mm), were exposed to temperature/humidity/bias conditions in order to evaluate the effects of lead-free finished (Sn-0.7Cu and Immersion Ag), conventional finishes (Sn-37Pb and OSP), conductor spacing, voltage bias, flux chemistry, solder mask coating and test environment on surface insulation resistance (SIR). Results indicate that, among these four finishes without solder mask coating protection, Sn-0.7Cu has the highest potential for inducing electrochemical migration to occur. There are few SIR drops occurring on the PCBs that had fibrous contamination within the solder mask coating. The presence of fibrous contaminants within the coating represented a preferential medium for moisture adsorption and ion transport, leading to accelerated reduction of SIR. In the absence of contamination, PCBs with solder mask coatings were found to be less susceptible to SIR degradation than uncoated PCBs.

Table 6.1 Experimental design for assessment of SIR degradation using no-clean fluxes on conformally coated PCBs

<table>
<tr><td>Substrate</td><td colspan="4">FR-4</td></tr>
<tr><td rowspan="2">Board Finish</td><td colspan="2">Lead-free Finishes</td><td colspan="2">Conventional Finishes</td></tr>
<tr><td>Immersion Silver (Imm Ag)</td><td>Sn-0.7Cu HASL</td><td>Eutectic (Sn-37Pb) HASL</td><td>Organic Solderability Preservative (OSP)</td></tr>
<tr><td>IPC Structure Spacing</td><td colspan="4">4 mils, 6 mils, 12 mils</td></tr>
<tr><td>Circular Structure Spacing</td><td colspan="2">4 mils, 6 mils, 12 mils without solder mask stripe</td><td colspan="2">6 mil with solder mask stripe</td></tr>
<tr><td>Flux</td><td colspan="4">Rosin-based no-clean flux</td></tr>
<tr><td>Deactivated</td><td colspan="4">Yes (exposed to reflow profile)</td></tr>
<tr><td>Voltage</td><td colspan="4">3 VDC, 6 VDC, 24 VDC</td></tr>
<tr><td>Replicates</td><td colspan="4">3 boards with each finish were tested at each voltage condition</td></tr>
<tr><td>Environment</td><td colspan="4">65° C/ 88% RH</td></tr>
<tr><td>Test Time</td><td colspan="2">Test to failure or up to 504 hours for boards with exposed traces</td><td colspan="2">168 hours for boards coated with solder mask</td></tr>
<tr><td>Coating</td><td colspan="2">Uncoated solder mask (exposed traces)</td><td colspan="2">Coated with solder mask</td></tr>
</table>

6.2 Abstract of Research Findings Design of Experiments

A set of experiments was performed to assess susceptibility to SIR degradation and electrochemical migration of PCBs processed with no-clean fluxes. Two types of lead-free finishes (Sn-0.7Cu and Immersion silver) and two types of conventional finishes (Sn-37Pb and OSP) were tested under various accelerated conditions, 3V, 6V and 24V with 65°C/ 88% RH environment. For PCBs coated with solder mask, each test lasted 168 hours to check the possibility of early failures due to board manufacturing defects, especially with test structures having critical dimension of 4 mils. For the PCBs with exposed traces, the specimens were tested to failure or up to

504 hours. The types of finished, conductor spacing, voltage bias, flux chemistry, solder mask coating and the corresponding environmental conditions are provided in Table 6.1.

The no-clean flux used in this study, a rosin-based flux, is representative of those used in manufacturing and rework processes. Following the IPC-J-004 standard [5], the rosin-based flux is marked as “ROM0”. The no-clean designation means the residues can be left on the board.

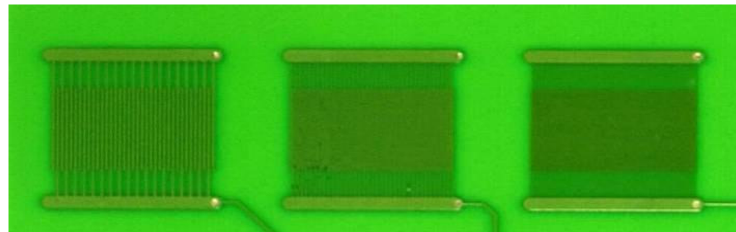

Figure 6.1 IPC-B-25 test coupon coated with solder mask showing conductor spacings from left to right of 12 mil (0.30 mm), 6 mil (0.15 mm), and 4 mil (0.1 mm).

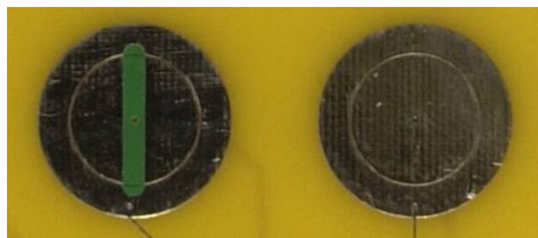

Figure 6.2. Circular test structures with and without solder mask stripe, 6mil (0.15 mm).

6.2.1 Test Vehicle

The test vehicles used in this study were fine-revised version of IPC-B-25 test boards [2], as illustrated in Figure 6.1. These boards each consisted of three comb structures, with 4, 6 and 12 mil spacing (equivalent to 0.10, 0.15 and 0.30 mm), original spacings of IPC-B-25 are 6.25, 12.5 and 25 mil spacing (equivalent to 0.16, 0.32 and 0.64 mm) . These spacings span the range of current lead spacings in fine-

pitched plastic packages. In order to investigate current leakage and dendritic growth between solder joints, the comb structures were coated with Sn-0.7Cu and eutectic (63Sn/37Pb) finishes applied by hot air solder leveling (HASL), along with immersion silver finish and organic solderability preservative finish. Another structure we designed and used in this study is the circular structure with 4, 6 and 12 mil spacing (equivalent to 0.10, 0.15 and 0.30 mm) and with or without solder mask stripe on the surface to evaluate the possibility of the preferential path built by the solder mask, shown as Figure 6.2. All the circular structures were processed with the same kinds of finishes applied for the IPC structures.

6.2.2 Surface Insulation Resistance Test System

Surface insulation resistance (SIR) test systems are commonly used to detect leakage current on a PCB. Sources of leakage current include surface dendritic growth, conductive filament formation [42] (similar to dendritic growth but beneath the PCB surface), and other surface anomalies, such as flux residues, that create a conductive path [44]. On typical FR-4 PCBs, the SIR measurement is 99.9% confined to the surface of the PCB even though SIR measures both surface and bulk conduction [40]. One of the objectives of this research was to evaluate the effect of test environment and bias voltage on SIR and dendritic growth. Therefore, our tests were conducted at a variety of temperature, humidity, and bias conditions, some of which corresponded to those cited in commonly used standards for SIR testing. According to IPC-TM-650 [3] and J-STD-004A [5], the PCB is considered to have failed when the resistance drops below 100 megohms. To meet these requirements in the present study, SIR readings were taken at less than one minute intervals on a test system designed to measure current in the picoampere range. Since SIR will be

affected by the test conditions, our failure criteria combined an SIR threshold level of 100 megohms with verification of the presence of an abnormal physical feature. The SIR test system used for these tests included a one-megohm resistor in series with each SIR test structure, which served to limit the current to prevent fusing of dendrites due to high current density.

6.2.3 Processing of Test Coupons

Each of the fine-revised IPC-B-25 test structures and circular test structures was inscribed with sample identification information on the unbiased side of the PCB. All test coupons were cleaned after processing and identification, and prior to application of no-clean flux, to remove contaminants present from the board manufacturing process. Cleaning was performed by soaking the boards for one hour at 80°C in a solution of isopropyl alcohol and deionized water. The average measured surface insulation resistance (SIR) of the boards after cleaning was 2×10^{12} Ohms. The flux was applied over the entire PCB surface after the solder bath were applied for Sn-0.7Cu and Sn-37Pb HASL finishes. Boards were allowed to dry for 24 hours before reflow processing. Reflow was performed using standard eutectic Sn-Pb reflow profile and Pb-free reflow profile.

6.3 Results and Discussion

Temperature/humidity/bias tests of fixed, 168 hour duration were performed to assess the effects of lead-free finished (Sn-0.7Cu and Immersion Ag), conventional finishes (Sn-37Pb and OSP), conductor spacing, voltage bias, flux chemistry, solder mask coating and temperature/humidity conditions on stability of surface insulation resistance. Analysis of the SIR data, combined with physical analysis of the test specimens, provided insight into the causes of observed SIR degradation and the

Table 6.2 Results of the temperature-humidity-bias tests of PCBs not Coated with Solder Mask Tested at 24V. For each individual comb structure for which an SIR failure was detected, the following symbols are used to report results of observations from failure analysis: "D": dendritic growth; "C": contamination.

Structure	Spacing (mils)	Sn-0.7Cu	Imm Ag	Sn-37Pb	OSP
IPC structures	4	D D D			
	6	C C D			
	12	D			
Circular, no solder mask stripe	4	D			
	6				
	12	C			
Circular, with solder mask stripe	6	D			

experimental conditions that were more conducive to electrochemical migration. The SIR of control boards, containing Sn-0.7Cu and Sn-37Pb HASL finish, immersion silver finish and OSP finish without no-clean flux, varied during the course of the 65°C/88% RH test in the 6×10^{8} to 1.1×10^{10} Ohm range.

6.3.1 Effect of Lead-free Finishes and Conventional Finishes

The specimens discussed in this section are the group of PCBs uncoated with solder mask with exposed traces. The PCB test structures that exhibited SIR drops below the failure threshold of 10^8 Ohms were examined using optical microscopy to identify surface features associated with the failures. As presented in Table 6.2, the failed structures were put into two categories: those showing clear evidence of dendritic growth (labeled "D" in the table), and those containing contamination (labeled "C" in the table).

The only failures observed in this study were on Sn-0.7Cu boards exposed to 24V and were associated with dendritic growth (7 out of 21), or contamination (3 out of 21). All the IPC structures, 4 mil (0.10 mm), 6 mil (0.15 mm) and 12 mil (0.30 mm), experienced the electrochemical migration failure: all the 4 mil (0.30 mm) spacing has been observed with the dendritic growth. For the circular structure with and without solder mask stripe, the electrochemical migration failure has been found with the detection of tin and copper migration. Compared with the IPC structures, the number of failed case of circular structure is lower. The reason is that the IPC structure is comb style, which has multiple electrodes to increase the possibility for electrochemical migration to occur. The purpose of designing circular structure is to generate a uniform electrical field at the cathode, where the dendrite begins to grow.

Eutectic tin-lead, immersion-silver and OSP finishes survived under the accelerated stress test conditions for 504 hours. The risk of electrochemical migration with Sn-0.7Cu lead-free finishes is highest among the tested four different finishes. As illustrated in the Figure 6.3, there are SIR degradations below the failure criteria 10^8Ohms for all these three spacings of IPC structures. Through the optical analysis

on 12 mil (0.30 mm) spacing structure, shown in Figure 6.4, there is a dendrite being detected between the two electrodes, which is compose of copper analyzed through X-ray mapping. For the 4 mil (0.10 mm) spacing structure, the dendrite was also observed and found to be composed of tin and copper, illustrated in Figure 6.5 and Figure 6.6. The sulfur ion has been detected associated with the dendrite, which could induce the corrosion on the Sn-0.7Cu finish and result in the Sn and Cu ions migration. Besides the dendrite between the two electrodes being detected, fibrous contamination was found to bridge the electrodes, illustrated in Figure 6.7.

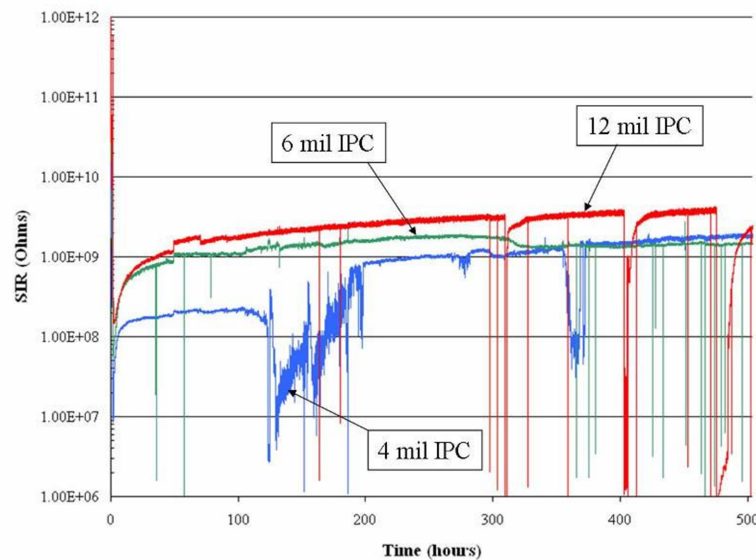

Figure 6.3 SIR trends for the failed 4mil (0.10 mm), 6 mil (0.15 mm) and 12 mil (0.30 mm) IPC structures processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

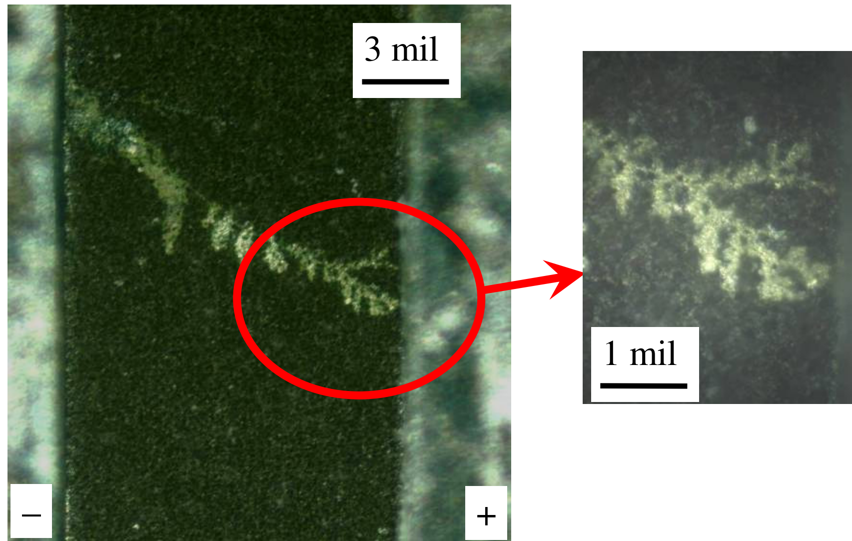

Figure 6.4 Optical micrograph of dendritic growth on the failed 12 mil IPC structure processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

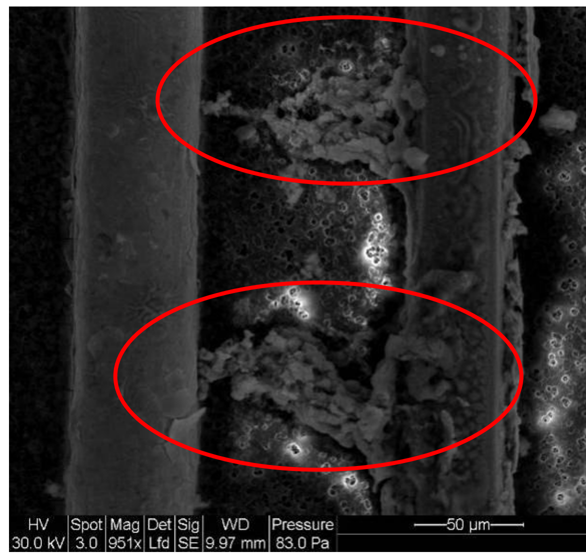

Figure 6.5 Electron micrograph of dendritic growth on the failed 4 mil IPC structure processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

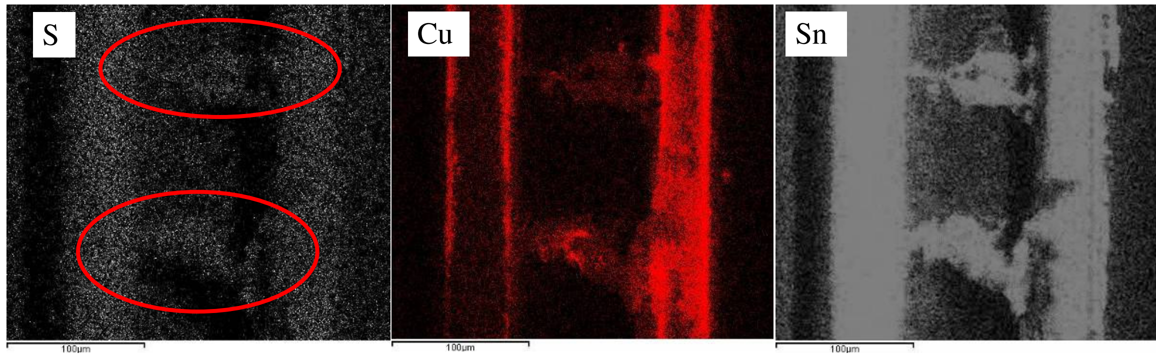

Figure 6.6 X-ray mapping of dendritic growth on the failed 4 mil IPC structure processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias. The dendrite has been identified with sulfur, copper and tin ions.

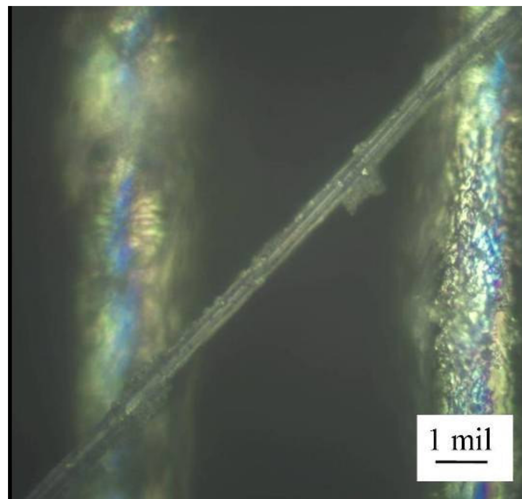

Figure 6.7 Optical micrograph of fiber contamination on the failed 4 mil IPC structure processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

6.3.2 Effect of Solder Mask Coating

The main function of a solder mask is to prevent solder bridges between component pads. In this study, the solder mask is evaluated as a protective coating to retard the susceptibility of electrochemical migration on the PCB surface. As illustrated in the Table 6.1, the THB testing of the PCBs coating with the solder mask were performed at 65°C/88% RH with 3V, 6V, and 24V DC Bias for 168 hours to

check for the possibility of early failures due to board manufacturing defects and check for the possibility of ECM failures in structures coated with solder mask.

The test results show that no dendritic growth was observed on any of the PCBs coated with solder mask. The only failures observed were on Sn-0.7Cu HASL boards biased at 24V, and were associated with fibrous contamination, as shown in Figure 6.8. The fibrous contamination provides a preferential path for water molecules to accumulate along the edge of the fiber, allowing it to combine with no-clean flux residues and ionic contamination from the industry atmosphere, such as halide elements and SO_2, to form an electrolyte. This kind of phenomenon could accelerate the process of electrochemical migration and result in SIR degradation due to ionic migration occurring between two electrodes. Therefore, to increase the reliability performance of the PCBs, the board manufacturers should improve cleaning and inspection of boards prior to manufacturing of uncoated boards.

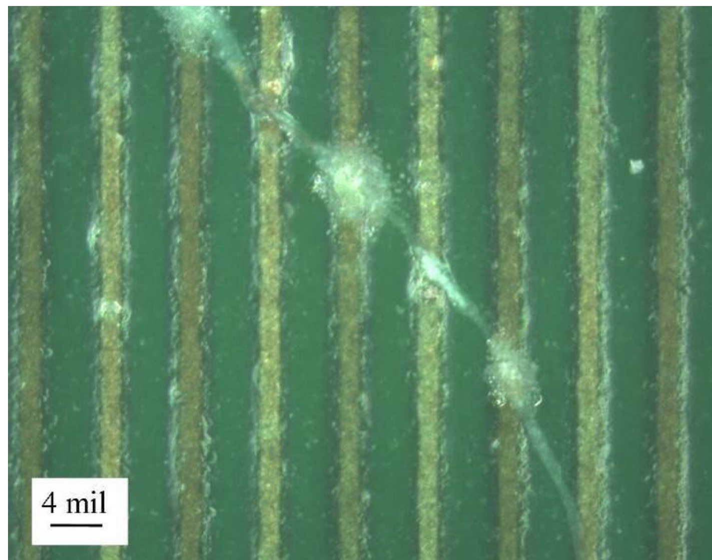

Figure 6.8 Optical micrograph of dendritic growth on the failed 4 mil IPC structure processed with Sn-0.7Cu lead-free finish and solder mask coating exposed to a 65°C/88% RH environment with an applied 24V bias.

As illustrated in Figure 6.2, the circular structure has been designed as an exposed board surface coating with and without solder mask strip to evaluate the possibility of the preferential path built by the solder mask. From the testing results, as presented in Table 6.2, the solder mask strip does not play a role as a preferential path for electrochemical migration to occur. Actually, one failed case of the circular structure coated with solder mask stripe has dendritic growth in the area without any solder mask strip coating, as shown in Figure 6.9. The x-ray mapping, illustrated in Figure 6.10, on the dendrite between two electrodes identifies the composition as tin and copper, which has migrated from the Sn-0.7Cu lead-free finish. The SIR behavior of this failed structure compared with the structure without solder mask stripe is shown in Figure 6.11.

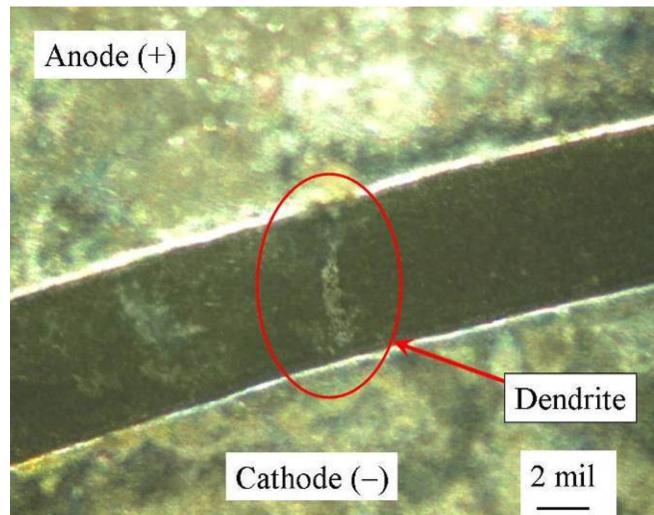

Figure 6.9 Optical micrograph of dendritic growth on the failed 6 mil circular structure with solder mask stripe processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

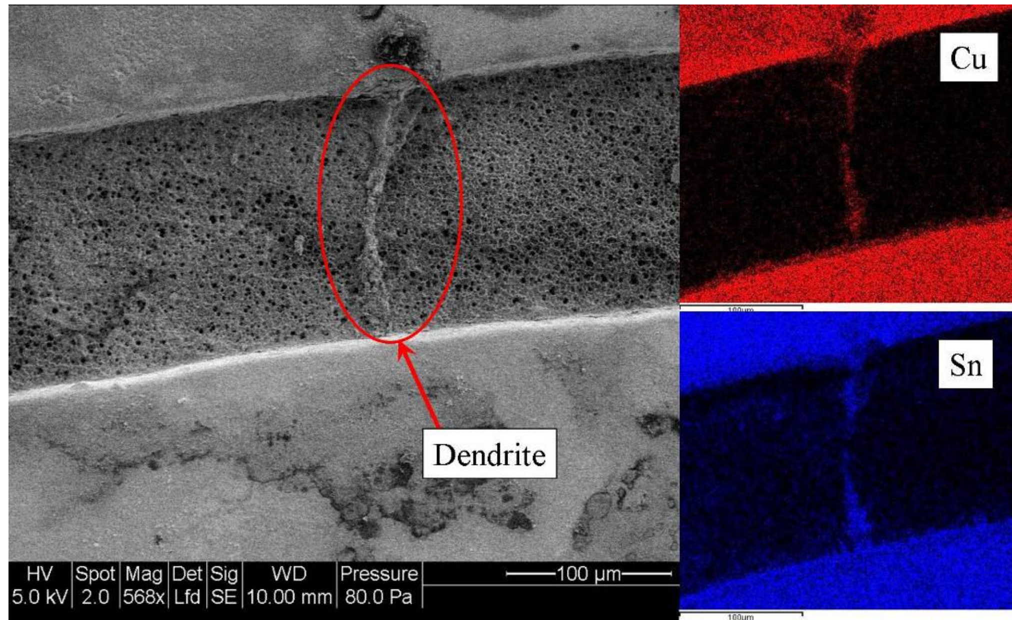

Figure 6.10 Electron micrograph and X-ray mapping of dendritic growth on the failed 6 mil circular structure with solder mask stripe processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

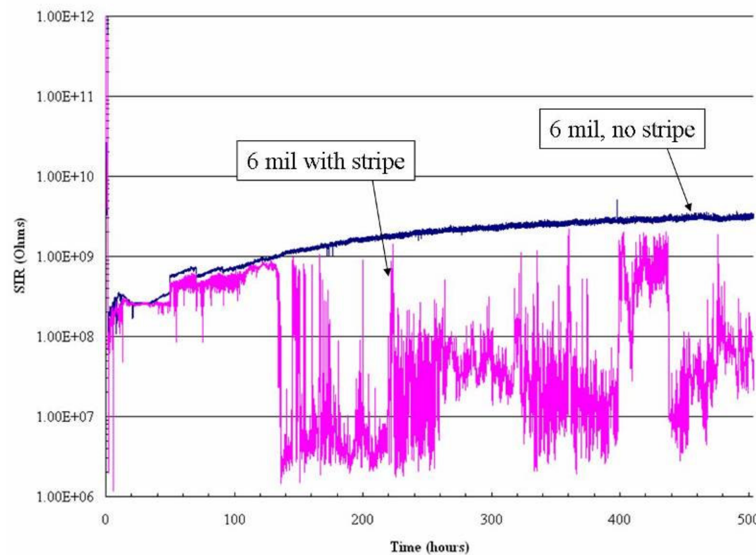

Figure 6.11 SIR trends for the failed 6 mil circular structure with and without solder mask stripe processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

6.3.3 Effect of Conductor Spacing

The conductor spacing with the effect of voltage always plays an important role in the process of electrochemical migration [38]. In this study, all the failed cases occurred at 24V and associated with 4 mil (0.10 mm) to 12 mil (0.30 mm) spacing. So, the conductor spacing become the point needed to be investigated. There are two kinds of structures tested in this study. One is the IPC comb structures, and another one is the circular structure. Both of them had 4 mil (0.10 mm), 6 mil (0.15 mm) and 12 mil (0.30 mm) spacing. From the testing results, illustated in Figure 6.3 and Figure 6.12, the SIR level decreased with reduced spacing for both IPC structures and circular structures.

From Table 6.2, all the 4 mil (0.10 mm) spacing IPC structures were identified with dendritic growth, and some of them also experienced fiborous contamination. This indicates that the smaller spacing may have the tendency to a lower level of SIR or electrochemical migration caused by the ionic contamination or fibrous contamination bridging the electrodes. Therefore, it is advisable in such cases to use larger conductor spacings whenever possible, to minimize ionic contamination.

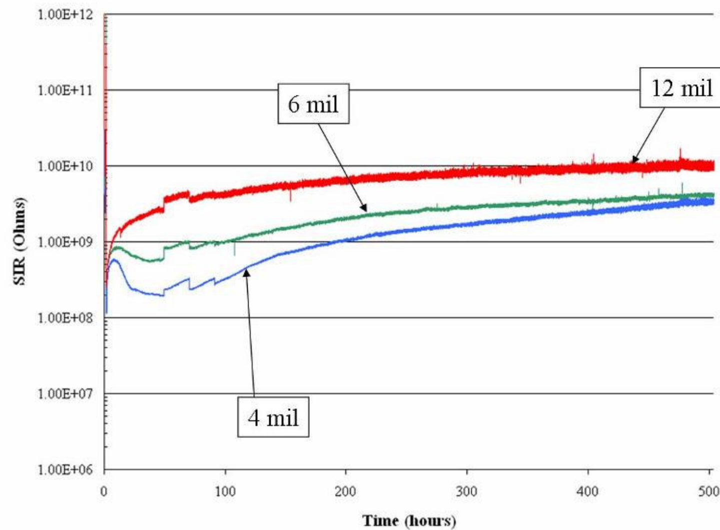

Figure 6.12 SIR trends for the 4 mil (0.10 mm), 6 mil (0.15 mm) and 12 mil (0.30 mm) circular structures without solder mask stripe processed with Sn-0.7Cu lead-free finish exposed to a 65°C/88% RH environment with an applied 24V bias.

6.4 Conclusions

PCB specimens containing fine-revised IPC-B-25 test structures and circular structures were exposed to temperature/humidity/bias conditions in order to evaluate the effects of solder mask coating, conductor spacing, voltage bias, flux chemistry and test environment on reduction of surface insulation resistance. Some of the PCBs that were coated with solder mask were found to possess fiber contamination embedded in the coating. The fibers provided a medium for adsorption of moisture, allowing it to combine with no-clean flux residues and ionic contamination from the industry atmosphere, such as halide elements and SO_2, to form an electrolyte. This constituted a preferential path for ion transport which increased the susceptibility of these specimens to failure by SIR degradation. Thus, proper quality and contamination control is required in all steps of the PCB assembly process in order to avoid introduction of contaminants that can lead to early failure.

In the absence of fiber contamination, a solder mask coating was found to reduce the risk of electrochemical migration since PCBs with solder mask coating were less susceptible to SIR degradation than uncoated PCBs.

Conductor spacing was found to be a factor effecting the SIR level. For both of the IPC structures and circular structures, the SIR level decreased with reduced spacing. This indicates that the smaller spacing may have a lower level of SIR caused by the flux residues or some other ionic contamination bridging the electrodes. Therefore, it is advisable in such cases to use larger conductor spacings whenever possible, to minimize ionic contamination or fibrous contamination.

Through the exposure to 65°C/ 88% RH RH environment with an applied 3V, 6V and 24V bias, the dendritic growth and SIR degradation were only detected for the uncoated PCBs processed with Sn-0.7Cu lead-free finish after 504 hours testing. Both tin and copper migration have been detected in the composition of the dendrite bridging the electrodes. Eutectic tin-lead, immersion-silver and OSP finishes survived under the accelerated stress test conditions for 504 hours. The risk of electrochemical migration with Sn-0.7Cu lead-free finish is the highest among all of these four tested finishes.

CHAPTER 7: NEW ASSESSMENT METHODOLOGIES

The current approach for assessing the potential for fluxes initiating electrochemical migration is through industry specified test protocols. This methodology requires significant capital investment (temperature/humidity/bias chamber, high resistance meter, switch system with low leakage current), consumables and personnel cost, and up to three weeks of actual test time. Since solder joint corrosion and ECM are corrosion-based process, it is possible that using techniques developed in the corrosion science field may provide a lower cost alternative to current practices. This study will identify the potentiostat test as the most applicable to identifying no-clean chemistries that may induce solder joint corrosion and electrochemical migration.

7.1 Introduction

The majority of consumer electronics manufacturers have been using no-clean, rosin-based fluxes in the assembly of electronics since the mid-1980's. This movement to no-clean flux chemistry led some companies to introduce an internal qualifying procedure designed to identify aggressive flux residues that might initiate corrosion and diminish solder joint reliability. And recently, some in the electronics industry have begun to move from rosin-based fluxes to aqueous-based fluxes. Aqueous-based fluxes have several advantages, including better solderability, better process control, cost effectiveness, and environmental-friendliness.

Aqueous-based fluxes have one disadvantage in that they do not form a “protective” coating over the board like the rosin based fluxes. This coating can encase contaminants and prevent possible failure mechanisms such as

electrochemical migration (ECM) and corrosion. Residues of aqueous-based fluxes also are soluble in moisture. Therefore, under the appropriate humidity conditions, they can more readily form an electrolytic solution than residues from rosin-based fluxes.

The increased use of no-clean fluxes may increase the occurrence of solder joint corrosion as a life-limiting failure mechanism, possibly due to the presence of certain wetting agents. Another primary failure mechanism due to the presence of no-clean flux residues on the board has been ECM, also known as dendritic growth. Electrochemical migration progresses through a sequence of three primary stages, consisting of path formation, initiation, and propagation. Path formation is dependent on the board surface conditions and material composition, and perhaps most importantly the environment. Some of the main factors concerning the board surface are residues of fluxes used for soldering, composition of board materials such as the plating and laminate and surface roughness. The typical path (electrolyte) experienced on a PCB is from the build-up of monolayers of water to a bulk solution capable of transporting metal ions. Initiation consists of three steps including electrodissolution, ion transport, and electrodeposition. Electrodissolution is the dissociation of metal ions (oxidation), typically from the anode (ground, positive). These ions tend to migrate because of electromotive forces, typically towards the cathode (power, negative) through the electrolyte. Electrodeposition occurs in the form of reduction once the metal cations arrive at the oppositely charged conductor. Propagation occurs as more metal is deposited and the filament grows.

7.2 Corrosion

This section reviews the basic theory of metallic corrosion and provides specific detail on the corrosion behavior of tin alloys used as interconnects in electronic products.

7.2.1 Corrosion of metals

There are four conditions that must be met in order for electrochemical corrosion to occur. There must be something that corrodes, often called the anode, there must be a cathode, there must an electrolyte, and there must be a conductor to carry the flow of electrons from the anode to the cathode, usually a metal-to-metal contact [78]. Metal corrosion may be divided into two major categories, active corrosion and passive corrosion.

Corrosion of metals that occurs in the absence of reaction products is called active corrosion. This corrosion is caused by the removal of ions of the metal or the metal's oxidation. The rate of ion transfer depends exponentially on the potential difference across the metal-solution interface. At potentials as low as 100mV, the rate of corrosion can be extremely rapid. The active dissolution of alloys is quite peculiar in itself. When the constituent metals of an alloy have dissimilar thermodynamic tendencies, the more reactive metal dissolves and, the less reactive metal stays, and a porous layer of the noble metal, a metal extremely resistant to chemical attack, such as gold, forms on the surface. There have been two explanations proposed for this incidence. One explanation states that both alloyed metals dissolve, but the less reactive one is redeposited. The second explanation claims that the more reactive metal dissolves, leaving vacancies in the alloy. The vacancies move into the metal

and force out more of the reactive metal to the surface, thus creating a porous layer of the less reactive layer.

Passive corrosion is the most common form of corrosion. It indicates the presence of reaction products, which severely retard the rate of corrosion. The reaction products, usually oxides, coat the metal surface thus passivating it from further corrosion. After the formation of the passivation layer, the rate of corrosion is dependent either upon the rate of diffusion through the passivation layer or upon the removal of that layer. If the corrosion mechanism is dependent upon diffusion, the rate of corrosion will slowly retard as the passivation layer thickens. If the occurrence of corrosion is dependent upon breaching the passivation layer, the rate of corrosion will fluctuate as the layer is penetrated and then reforms.

In addition to active and passive, corrosion mechanisms can be further categorized based on the materials, the environment and the architecture necessary for these mechanisms to occur. The types most relevant to flux-induced corrosion on a printed circuit board are displayed below.

Uniform Corrosion: Uniform corrosion is a type of corrosion that generally attacks the entire surface area of a piece of metal. The metal is thinned until failure occurs, though failure is rare because uniform corrosion is easily measured and predicted. If uniform corrosion is left unchecked, other types of corrosion, such as pitting, may follow, which could be more disastrous [79].

Concentration Cell: Concentration cell corrosion is the result of having unequal concentrations of a solution in contact with the surface of a metal. The area of the metal in contact with a low concentration of metal ions will act as a cathode and will

not be corroded, while the area of the metal in contact with a high concentration of metal ions will act as an anode and corrode [78]. Concentration cell corrosion might be a valid form of corrosion of solder from no-clean flux residue because the residue may easily exist on solder joints at various concentrations.

Pitting Corrosion: Pitting is the formation of holes or pits in a metal due to localized corrosion attacks. Pitting is harder to predict and detect than uniform corrosion and is thus more detrimental. Pitting itself comes in many forms including narrow holes, subsurface pits, undercutting pits, and horizontal and vertical grain attacks. A single pit in an electrical system could lead to the failure of the system if the pit is allowed to spread and widen [79].

Galvanic Corrosion: Galvanic corrosion is the result of two metals with different corrosion potentials being brought together in the presence of an electrolyte solution. In such cases, the metal with a nobler configuration becomes the cathode, and the other metal becomes the anode, which is destroyed by anodic dissolution. If the surface area of the anode is small compared to the surface area of the cathode, the galvanic current is concentrated on one small area [79]. Each material in the galvanic series, which details susceptibility to corrosion in seawater, has a range of potentials. In some situations, copper can be more cathodic than tin-lead solder, which can accelerate corrosion of eutectic solder joints. This can also be true for tin-alloys, suggesting the lead-free solders may also be susceptible to galvanic corrosion [80].

Crevice Corrosion: Crevice corrosion is localized corrosion that occurs in constrained areas with stagnant solutions and a deficiency of oxygen. Examples of these areas on electronics include solder joints, especially solder bumps and solder

balls, separable connectors, and regions of delamination. In most cases, the rate of crevice attack is not constant. Initially, there is an incubation period where the attack rate is essentially zero. However, as the corrosivity of the crevice environment increases with exposure time, the rate of attack will increase [81].

Intergranular: Intergranular corrosion is a localized attack along the grain boundaries in the microstructure of metals and alloys. Intergranular corrosion is often caused by specific chemical phases forming on grain boundaries. This precipitation can cause zones of reduced resistance to corrosion in the metal [79].

7.2.2 Corrosion of tin and tin alloys

Tin is generally very corrosion-resistant in non-aqueous conditions. In air, tin passivates, forming a protective oxide (SnO_2) Layer on its surface. This passivation layer protects tin from most types of non-aqueous corrosion. The destruction of the oxide layer will result in the formation of more oxide and continuing corrosion. In aqueous environments tin may corrode in several ways. In acidic solutions, such as aqueous solutions with halides, tin corrodes by the formation of Sn^{2+} and Sn^{4+}, and in acidic solutions with high potential tin forms a gaseous hydride. The initial tin corrosion in a solution containing chloride ions is accelerated by lowering the pH below 4 and contact with a noble metal such as copper [82]. In basic solutions tin corrodes by the formation of SnO_3^{2-}.

Oxygen, readily reducible organic depolarizers, and contact with metals that have a low hydrogen overvoltage are other factors besides pH that can increase the rate of corrosion [82]. Depolarizers are substances that prevent the deposition of gases liberated by the action of the current in an electrolytic reaction [83]. Hydrogen overvoltage is the difference between the actual electrode potential when appreciable

electrolysis begins that causes the liberation of hydrogen gas [81]. In acids the corrosion of tin is largely dependent upon the oxygen concentration and the presence of metallic impurities in the tin or the acid that can concentrate on the surface [82].

Eutectic solder (63Pb/37Sn) is considered to be the most corrosion resistant solder [82]. Lead's oxide is unstable and reacts readily, but tin's oxide does not. The passivation layer formed on the tin in the solder spreads over the entire surface, thus protecting it from corrosion. Tin is considered resistant to corrosion when the rate is less than 24 mg/(dm^2) per day and is considered unsuitable when the rate is greater [82].

7.3 Flux Corrosion of Solder

Flux is used to enhance wetting of solder on the metal to be joined by deoxidizing the metal surfaces. Solder flux falls into two categories, rosin-based and water-soluble. The active ingredient in rosin-based fluxes is abietic acid (an organic acid) as well as some other activators that aid in deoxidizing the metal to be joined. A solvent with a low boiling point, such as isopropyl alcohol, is used as the vehicle for the flux. Water-soluble, or aqueous, fluxes can be either organic or inorganic in nature. Aqueous fluxes are more active than all rosin-based fluxes, while inorganic aqueous fluxes are the most active of them all. Low solids no-clean fluxes can be either rosin- or water-based and are typically only moderately active; they do not require a post-solder cleaning.

Low-solids fluxes contain a solids content of approximately 2-3 %wt and use weak organic acids (WOA's) such as adipic, glutaric, and succinic acids as active ingredients. These fluxes leave very little residue on the printed circuit boards after

use so cleaning is often not necessary. Water-soluble fluxes, however, seem to be inherently more corrosive than rosin-based flux, possibly due to the presence of wetting agents, or surfactants. Most of the WOA residues that ate left on boards are degraded during reflow and form anhydrous organic compounds, which are considered to be corrosive. There is evidence that wetting agents and other minor chemicals in the flux are actually more corrosive to solder than the flux's active ingredients. Surfactants, or surface-active chemicals, aid in the wetting ability of the flux. Many such surfactants fall into the category of polyglycols, such as polyethylene glycol or polypropylene glycol. Other possible surfactants are alkylenic ethoxylates and fluorinated esters. Polyglycols, though perhaps not corrosive themselves, can trap corrosive halides from the environment. Glycols, which may also be found in flux, have been shown to not cause corrosion of tin [82].

Discussions of flux corrosion of solder, outside of electrochemical migration (ECM), are rare in the published literature. Cavallotti [21] conducted a similar potentiostat experiment. Five types of no-clean pastes, were decomposed by a reflow process and the remaining residues were dissolved in a solution of isopropyl alcohol and distilled water. FR4 coupons were then prepared by reflowing the same set of solder pastes over copper pads. The anodic behavior of the FR-4 coupons in the flux solutions was then measured using an AMEL System 5000 potentiostat. Unfortunately, by only measuring the anodic behavior, the corrosion rate of the solder joints on the FR-4 coupons could not be calculated. However, the paper did discuss that the no-clean flux solutions displayed aggressivity towards the solder joints, as evidenced by an increase in current over time. Three of the flux solutions also

induced increased levels of tin oxidation. The authors stated that electrochemical corrosion may occur because of the trapping of organic compounds by solder during reflow.

7.4 Background on Potentiostat Assessment Technology

A potentiostat test applies a series of voltages to the interface between the test metal and the test solution, which is in an electrochemical cell, and measures the resulting current [13][17]. This test can be conducted at many temperatures so as to simulate many environments. The scan begins at the initial programmed voltage and measures the current flowing, while at the same time plotting the current as a function of time. After a set amount of time the voltage is incremented by a set value and the current is again measured and plotted. The process repeats itself until the potentiostat reaches its programmed final potential.

A common electrochemical test cell, as shown in Figure 7.1, is a glass flask with four tapered holes in the top. Three of the holes are fitted with Teflon tubing adapters. The materials used in the test cell are very chemically inert so many types of materials may be tested. The adapters hold the working electrode in the central hole, and the graphite counter electrode and gas dispersion tube in the other tubes. The remaining hole holds a glass Luggin capillary that houses the reference electrode.

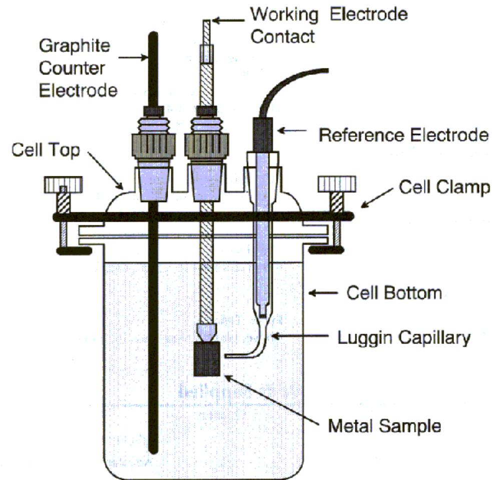

Figure 7.1 Schematic of an electrochemical test cell

Information from which corrosion rates are found comes from the generation of a Tafel Plot [18]. To generate a Tafel Plot, first measure the corrosion rest potential (E_{0-}) with the potentiostat (most potentiostats have this capability). E_0 is the potential at which no current flows and can be determined from a plot of current versus potential if the potentiostat is incapable of determining it. Next, have the potentiostat scan from E_0 - 50mV to E_0 at a scanning rate of about 0.1 mV/sec. to generate the cathodic portion of the plot. Then scan from E_0 to E_0 + 50mV at the same rate to get the anodic portion. For example, an E_0 of 100 mV would require a full scan from 50mV to 150mV. The resulting curves are a plot of applied potential vs. the current on a logarithmic scale. Extrapolate straight lines from the linear portions of the anodic and cathodic curves. The lines should intersect at E_0. The current corresponding to E_0 is the corrosion current, i_{corr}. From the i_{corr} corrosion rate may be calculated using the following formula:

$$rate_{corr} = \frac{0.13(i_{corr})(E.W.)}{A \cdot d}$$

E.W. = equivalent weight (g/eq.)

A = area (cm^2)

d = density (g/cm^3)

0.13 = metric and time conversion factor

The equivalent weight of a metal is found by dividing its atomic mass by the valence of the metal. Valence is defined as the number of electrons that a molecule gives up or accepts when reacting.

There are several advantages to using a potentiostat test, the most important being the generation of an accurate corrosion rate. A potentiostat test is also less time-consuming than the other tests described above; it takes only a few hours for each flux. Once learned, the operation of the potentiostat is relatively easy, especially with a software-driven potentiostat within a personal computer. Another benefit is that knowledge of what the corrosion products are is not necessary as the corrosion rate calculation is independent of corrosion product chemistry. Also note that a potentiostat can merely be a board in a personal computer controlled by special software.

The potentiostat test is also relatively inexpensive, in comparison with the weight-loss and resistance change tests. In addition, the test setup can be exposed to elevated temperatures for examination on how temperature changes affect the corrosion rate.

7.5 Potentiostat Testing and Test Results

After a careful review of the three testing methods previously described, the potentiostat test was determined to be superior in both accuracy and cost in comparison with the weight loss and resistance change tests. A potentiostat test was conducted to both examine the corrosive effects of three no-clean, no-halide fluxes and to test the effectiveness of the test itself. Information on the no-clean flux chemistries is displayed in Table 7.1.

Table 7.1 No-clean flux chemistries

Products	**Aqueous-based**	**Rosin-based**
Manufacturer	Alpha	Henkel
Appearance	Clear colorless liquid	Cloudy, white mobile liquid
Solubility in water	Complete	Complete
Flux Type	Aqueous VOC Free	Rosin VOC Free
Specific gravity	1.006	0.9-1.0

For this project, an electrochemical test cell was developed in-house. The cell was comprised of an acrylic tube with disk-shaped solder electrodes from Metal Samples Co. on both ends. One disk acted as both the working electrode (WE) and a reference electrode (RE2), while the other disk was the counter electrode (CE). A small hole was drilled into the acrylic tubing for filling purposes, and as an opening through which was passed a small platinum wire to act as another reference electrode (RE1). O-rings were required between the solder disks and the acrylic tubing to form a tight seal. Square acrylic pieces mounted to either end of the cell with machine

screws were used to hold the tube and electrodes together. Figure 7.2 shows a drawing of the completed cell.

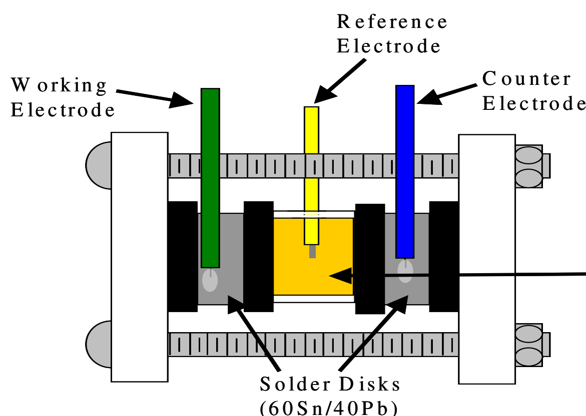

Figure 7.2 Schematic of the corrosion cell

The solder samples used in this investigation were 60/40 Pb-Sn disks, 0.50" in diameter. The solder disks were used with two different surface finishes. Corrosion rate measurements were made using an ECOCHEMIE Autolab PGSTAT 30 Potentiostat, which was driven by GPES software. The E_0 was found by allowing the system within the test cell stabilize until the potential measured between the metal-solution interface changed at a rate of only about 1 mv/minute. Once E_0 was found, according to the circumstances, the potentiostat was programmed to apply voltages from E_0 – 50mV to E_0 + 50mV, E_0 – 100mV to E_0 + 100mV, E_0 – 150mV to E_0 + 150mV or E_0 – 200mV to E_0 + 200mV at a scan rate of 0.1 mV/sec.

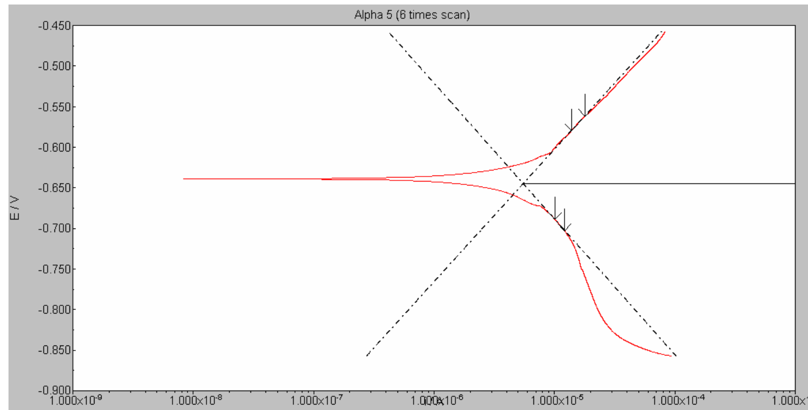

Figure 7.3 Applied current cathodic and anodic polarization curve of a corroding metal showing Tafel extroplation. The X-axis is the log $i_{applied}$, and the Y-axis is the applied potential.

A log i versus E plot is called a Tafel plot. From the Figure 7.3, the region of linearity is referred to as the Tafel region. The total anodic and cathodic polarization curves correspond to hydrogen evolution and metal dissolution. To determine the corrosion rate from such polarization measurements, the Tafel region is extrapolated to the corrosion potential. At the corrosion potential, the rate of hydrogen evolution is equal to the rate of metal dissolution, and this point corresponds to the corrosion rate of the system expressed in terms of current density. The software would process the data and calculate out the corrosion rate in the unit of μm/year.

7.6 Test Results and Discussion

The test results (Tafel plot) are displayed in Table 7.2. The most aggressive flux, based on the corrosion rates determined by the potentiostat tests using solder disks was rosin-based no-clean flux, which had a corrosion rate of 10.9 μm/year. Another kind of no-clean flux, aqueous-based one, had a corrosion rate of 2.7 μm/year.

Table 7.2 Experiment results of potentiostat assessment methodology on no-clean flux chemistries

Corrosion Rate	**Aqueous-based**	**Rosin-based**
(μm /year)	51 $\pm$19	16 $\pm$7
Pre-reflow	2 $\pm$0.3	14 $\pm$7

The rates determined by the potentiostat test, however, may not be truly representative of the actual conditions on printed circuit boards fluxed with no-clean flux. After a normal solder reflow process, the flux would have been degraded to form anhydrous organic compounds, which may be more corrosive. In addition, the coarseness of the surface of the solder disks may have initiated corrosion mechanisms, such as concentration cell, which may not actually be present in the field.

7.7 Correlation of the Assessment Methodologies

The traditional means for assessing electrochemical migration risk, temperature-humidity-bias testing, requires considerable time, human labor, and specialized equipment, which must be repeated if test samples change. Therefore, new assessment methodologies have been developed for assessing the electrochemical migration risk.

Ion-chromatography methodology has been applied for assessing the contamination level for the printed circuit boards. Through this method, the types of the ions and the quantity of the ions could be detected and estimated, which could help to understand the inducing factor ionic contamination brings. But, when performing the analysis, the whole board or part of it needs to be soaked in the solution to obtaining the extraction from the board. That means the information from the extraction includes global information of the board instead of the point which might induce the electrochemical migration or corrosion problem.

Table 7.3 Correlation of the assessment methodologies

Assessment Methodologies		**Flux: Alpha Metals (NR300A2)**	**Flux: Henkel (MF101)**
Ion Chromatography Potentiostat Assessment Methodologies Ion Chromatography	Glutaric (ppm)	7500	22500
	Adipic (ppm)	13000	6500
	Succinic (ppm)	ND	4500
	TOTAL WOA (ppm)	20500	33500
	WOA Contamination Level (mg/in^2)	113	185
Potentiostat	Corrosion rate (mm /year)	2±0.3	14±7
Temp/Humidity/Bias results	Rate of ECM Failures on the PCBs	7.4%	11.1%

The results of Temp-Humidity-Bias testing with the analysis results from ion-chromatography and potentiostat on the flux used for the assembly process have been compared and correlated in the Table 7.3. The detail of the temp-humidity-bias testing of this table has been discussed in the chapter 5.

CHAPTER 8: CONTRIBUTIONS

Conducted long-term temp-humidity-bias testing over 8,000 hours to assess the reliability of printed circuit boards processed with a variety of lead-free solder pastes, solder pad finishes, and substrates.

Identified silver migration from Sn3.5Ag and Sn3.0Ag0.5Cu lead-free solder, which is a complete new finding compared with previous research.

Established the role of path formation as a step in the ECM process, and provided clarification of the sequence of individual steps in the mechanism of ECM: path formation, electrodeposition, ion transport, electrodeposition, and filament formation.

Developed appropriate accelerated testing conditions for assessing the no-clean processed PCBs' susceptibility to ECM:

- Conductor spacings in test structures should be reduced in order to reflect the trend of higher density electronics and the effect of path formation, independent of electric field, on the time-to-failure.
- Temp-humidity-bias testing temperatures should be modified according to the material present on PCB, since testing at 85°C can cause the evaporation of weak organic acids (WOAs) in the flux residues, leading one to underestimate the risk of ECM.

Correlated temp-humidity-bias testing with ion chromatography analysis and potentiostat measurement to develop an efficient and effective assessment methodology to characterize the effect of no-clean processing on ECM.

REFERENCE

[1]. IPC Publication IPC-TR-476A, "*Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies*," Northbrook, IL, May 1997.
[2]. IPC Publication IPC-9201, "*Surface Insulation Resistance Handbook*," Northbrook, IL, July 1996.
[3]. IPC Publication IPC-TM-650, "Test Methods Manual," Northbrook, IL, Sept 2000.
[4]. Telcordia Publication GR-78-CORE, Issue 1, "Generic Requirements for Physical Design and Manufacture of Telecommunications Products and Equipment", Red Bank, NJ, September 1997.
[5]. IPC Publication IPC J-STD-004, "Requirements for Soldering Fluxes," Jan 1995.
[6]. DIN IEC Publication IEC 61189-5-draft, "Draft Document – Test Method for Electrical Materials, Interconnection Structures and Assemblies - Part 5: Test Method for Printed Board Assemblies," Nov 2002.
[7]. IPC, "*Requirements for Soldered Electrical and Electronic Assemblies*," J-STD-001C, Section 8.36.
[8]. L. Turbini, "Water Soluble Fluxes", Proceedings of the Technical Program - National Electronic Packaging and Production Conference, v 3, 1992, p 1687-1695.
[9]. H. Manko, *Solders and soldering: materials, design, production, and analysis for reliable bonding*, 4th ed, McGraw-Hill, New York, 2001.
[10]. Robert G. Kelly, et al, "Electrochemical techniques in corrosion science and engineering," Marcel Dekker, New York, 2003.
[11]. M. Pecht, *Contamination of electronic assemblies*, CRC Press, Boca Raton, FL, 2003.
[12]. F. N. Speller, *Corrosion, causes and prevention; an engineering problem*, McGraw-Hill book company, inc., New York, 1926.
[13]. Uhlig, Herbert Henry, *The corrosion handbook*, sponsored by the Electrochemical Society, inc., New York, J. Wiley, 1948.
[14]. H. H. Manko, *Solders and soldering : materials, design, production, and analysis for reliable bonding*, New York : McGraw-Hill, c2001.
[15]. L. M. Klyatis, *Accelerated quality and reliability solutions*, Amsterdam, Boston, Elsevier, 2006.
[16]. M. Paunovic, *Fundamentals of electrochemical deposition*, New York Wiley, 1998.
[17]. John O'M, *Modern electrochemistry*, Plenum Press, New York, 1998-c2000.
[18]. N. Perez, *Electrochemistry and corrosion science*, Kluwer Academic, Boston, 2004.
[19]. J. Brous, "*Electrochemical Migration and Flux Residues – Causes and Detection*," Alpha Metals.
[20]. L. Turbini, J. Jachim, G. Freeman, and J. Lane, "*Characterizing Water Soluble Fluxes: Surface Insulation Resistance vs Electrochemical*

Migration”, Thirteenth IEEE/CHMT International, September 28-30, 1992, Pp. 80 – 84.

[21]. P. Cavallotti, G. Zangari, V. Sirtori, and A. Manara, "Reactivity of no-clean pastes and fluxes for the surface mount technology process. II. Corrosion rich measurements for printed circuit boards and solder joints," *J. Electron. Mater.*, vol. 24, no. 4, pp. 371-78, April 1995.

[22]. T. Takemoto, R.M. Latanision, T.W. Eagar, A. Matsunawa, "Electrochemical migration tests of solder alloys in pure water", *Corrosion Science*, v 39, n 8, Aug, 1997, p 1415-1430.

[23]. B. Smith and L. Turbini, “Characterizing the Weak Organic Acids Used in Low Solids Fluxes*”*, Journal of Electronic Materials, vol 28, no. 11, p 1999. *Conditions on Surface Insulation Resistance Values for Various Fluxes*,” Soldering & Surface Mount Technology

[24]. C. Hunt., L. Zou., “Impact of temperature and humidity conditions on surface insulation resistance values for various fluxes”, *Soldering & Surface Mount Technology*, v 11, n 1, p 36-43, 1999.

[25]. D. Pauls, “*Residues in Printed Wiring Boards and Assemblies*,” Circuit World, vol. 27, no. 1, pp. 32-41, 2000.

[26]. S. Stock, L. Turbini, “*Atacamite in jaws and printed wiring boards”*, *Science*, v 298, n 5600, Dec 6, 2002, p 1892-1893.

[27]. J. Sprovieri, “*Why Clean No-clean*,” Assembly, v 46, n 12, November, 2003, p 60-63.

[28]. S. Bodea, R. Ballou, P. Molho, "Electrochemical growth of iron and cobalt arborescences under a magnetic field", *Physical Review E*, v 69, n 2 1, February, 2004, p 021605-1-021605-12.

[29]. Pasquale, M.A, and et al, “*Influence of additives on the growth velocity and morphology of branching copper electrodeposits”*, Journal of the Electrochemical Society, v 152, n 3, 2005, p C149-C157.

[30]. S. Zhan, M. H. Azarian and M. Pecht, “Surface Insulation Resistance of Conformally Coated Printed Circuit Boards Processed with No-Clean Flux”, *IEEE Transactions on Electronics Packaging Manufacturing*, vol.29, no.3, p 217-223, July, 2006.

[31]. S.Zhan, M. H. Azarian and M. Pecht, “Reliability Issues of No-Clean Flux Technology for Printed Circuit Boards”, under IEEE TDMR review.

[32]. DiGiacomo, G., “Metal Migration (Ag, Cu, Pb) in Encapsulated Modules and Time to Fail Model as a Function of the Environment and Package Properties,” IEEE Proceedings of the IRPS, 1982. pp. 27 – 33.

[33]. Major Appliances Manufacturer, "Printed circuit board assembly cleanliness specification," Number 700002, Rev. 0, May 2003.

[34]. National Defense Center for Environmental Excellence (NDCEE), “*Joint Test Protocol CC-P-1-1 for Validation of Alternatives to Lead-Containing. Surface Finishes, for Development of Guidelines for Conformal Coating Usage, and for Qualification of Low-VOC Conformal Coatings*,” Contract No. DAAA21-93-C-0046, Johnstown, PA, June 1999.

[35]. IPC, “*Qualification and Performance Specification for Rigid Printed Boards*,” IPC-6012A -AM, Section 3.10.1, Northbrook, IL, July 2000.

[36]. United Nations Environmental Program, "*Montreal Protocol on Substrates that Deplete the Ozone Layer-A protocol to the Vienna Convention for the Protection of the Ozone Layer*", 1987.

[37]. W. Jud Ready and L. Turbini, "A Comparison of Hourly Versus Daily Testing Method for Evaluating the Reliability of Water Soluble Fluxes," *IEEE Transactions on Advanced Packaging*, Vol. 23, No. 2, May 2000.

[38]. Phil Kinner, "A New, More Representative SIR Test Method is Used to Validate the Reliability of a More Environmentally Acceptable PCB Production Process," *International IEEE Conference on the Business of Electronic Product Reliability and Liability,* 2003.

[39]. E. Bumiller, M. Pecht and C. Hillman, "*Electrochemical Migration on HASL Plated FR-4 Printed Circuit Boards*," *Proceedings of 2004 SMTA Pan Pacific Microelectronics Symposium*, Oahu, HI, pp. 201-205, February 11, 2004; *Journal of Surface Mount Technology*, Vol. 17, Issue2, pp.37-41, April-June 2004.

[40]. M. Pecht, K. Rogers and C. Hillman, "Hollow Fibers can Accelerate Conductive Filament Formation," *ASM International Practical Failure Analysis*, pp. 57-60, Vol. 1, Issue 4, Aug. 2001.

[41]. M. Pecht, B. Wu and D. Jennings, "Conductive Filament Formation in Printed Wiring Boards," *13th IEEE Intern. Electronics Manuf. Techn. Symposium*, pp. 74-79, 1992.

[42]. K. Rogers, C. Hillman, M. Pecht and S. Nachbor, "Conductive Filament Formation Failure in a Printed Circuit Board," *Circuit World,* Vol. 25 (3), pp. 6-8, 1999.

[43]. W. Jud Ready and L. Turbini, "A Comparison of Hourly Versus Daily Testing Method for Evaluating the Reliability of Water Soluble Fluxes," *IEEE Trans. Adv. Packag.*, Vol. 23, No. 2, May 2000.

[44]. S. Zhan, M. H. Azarian and M. Pecht, "Reliability Issues of No-Clean Flux Technology with Lead-free Solder Alloy for High Density Printed Circuit Boards," *38th International Symposium on Microelectronics,* pp. 367-375, Philadelphia, PA, September 25-29, 2005.

[45]. Phil Kinner, "A New, More Representative SIR Test Method is Used to Validate the Reliability of a More Environmentally Acceptable PCB Production Process," *International IEEE Conference on the Business of Electronic Product Reliability and Liability,* 2003.

[46]. E. Bumiller, M. Pecht and C. Hillman, "Electrochemical Migration on HASL Plated FR-4 Printed Circuit Boards," *Journal of Surface Mount Technology*, Vol. 17, Issue2, pp.37-41, April-June 2004.

[47]. U.S. Department of Defense, MIL-PRF-31032/1A, *Performance Specification Printed Wiring Board, Rigid, Multilayered, Thermosetting Resin Base Material, With Or Without Blind And Buried Plated Through Holes, For Soldered Part Mounting*, June 1999.

[48]. B. Smith and L. Turbini, "Characterizing the Weak Organic Acids Used in Low Solids Fluxes," *Journal of Electronic Materials*, Vol. 28, No. 11, pp. 1299-1306, Nov. 1999.

[49]. H. Leidheiser, *The Corrosion of Copper, Tin, and Their Alloys*, John Wiley & Sons, New York, NY, 1961.
[50]. S. Lee, Y. Yoo, J. Jung, Y. Park, Y. Kim, Y. Joo, " Electrochemical migration characteristics of eutectic SnPb solder alloy in printed circuit board", *Thin Solid Films*, v 504, n 1-2, May 10, 2006, p 294-297.
[51]. D.Q. Yu, W. Jillek, E. Schmitt, "Electrochemical migration of lead free solder joints," *Journal of Materials Science: Materials in Electronics*, v 17, n 3, March, 2006, p 229-241.
[52]. D.Q. Yu, W. Jillek, E. Schmitt, "Electrochemical migration of Sn-Pb and lead free solder alloys under distilled water," *Journal of Materials Science: Materials in Electronics*, v 17, n 3, March, 2006, p 219-227.
[53]. Shin-Bok Lee, Young-Ran Yoo, Ja-Young Jung, Young-Bae Park, Young-Sik Kim, Young-Chang Joo, " Electrochemical migration characteristics of eutectic SnPb solder alloy in printed circuit board," *Thin Solid Films*, v 504, n 1-2, May 10, 2006, *Proceedings of The International Conference on Materials for Advanced Technologies (ICMAT 2005) Symposium*, p 294-297.
[54]. R. Ciocci, M. Pecht, "Learning from the migration to lead-free solder," *Soldering and Surface Mount Technology*, v 18, n 3, 2006, p 14-18.
[55]. P. Reid, "Demonstrating the lead-free capability of PCBs," *Printed Circuit Design and Manufacture*, v 23, n 4, April, 2006, p 32-35.
[56]. Peck, D. Peck, "Lead-free rework: Are you ready?,"*SMT Surface Mount Technology Magazine*, v 20, n 2, February, 2006, p 42-51.
[57]. J. Zhou, R. Clawson, P. Wittmer, R. Snyder, J. Badgett, "Electrochemical Migration of Immersion Silver Finishes: Test Vehicle and Material Evaluation,"*Proceedings of SPIE - The International Society for Optical Engineering*, v 5288, *2003 International Symposium on Microelectronics*, 2003, p 351-356.
[58]. C. Alexander, "Cleaning flux residue in hand solder rework and the effects on SIR," *Circuits Assembly*, v 17, n 9, September, 2006, p 65-66.
[59]. W. Yin, G. Beckwith, H. Hwang, K. Lee, N. Lee, "Epoxy Flux - An Answer for Reliable No-Clean Flip Chip Assembly," *Proceedings of the IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium*, 2003, p 409-415.
[60]. M. Tidy, L. Turbini, T. North, B. Watson, N. Kester, J. McIntyre, "Soldering fluxes and the repair process," *Global SMT and Packaging*, v 3, n 5, July/August, 2003, p 17-22.
[61]. R. P. Prasad, "Part 2: How clean is clean?," *SMT Surface Mount Technology Magazine*, v 19, n 2, February, 2005, p 14.
[62]. T. Munson, "Can you clean a no-clean assembly?," *Circuits Assembly*, v 14, n 1, January, 2003, p 48.
[63]. J. Fellman, "A study of the lead-free hot air solder levelling process," *Circuit World*, v 31, n 2, 2005, p 3-9.
[64]. S. Yang, J. Wu, M. Pecht, "Electrochemical migration of land grid array sockets under highly accelerated stress conditions," *Electrical Contacts, Proceedings of the Annual Holm Conference on Electrical Contacts*, v 2005,

Electrical Contacts 2005 - Proceedings of the Fifty-First IEEE Holm Conference on Electrical Contacts, 2005, p 238-244.

[65]. D. Rocak, K. Bukat, M. Zupan, J. Fajfar-Plut, V. Tadic, "Comparison of new no-clean fluxes on PCBs and thick film hybrid circuits," *Microelectronics Journal*, v 30, n 9, Sep, 1999, p 887-893.

[66]. W. G. Kenyon, "Controlling the no-clean process," *SMT Surface Mount Technology Magazine*, v 11, n 9, Sep, 1997, p 22, 2.

[67]. C. Ramirez, K. Lei "Evaluation of the reliability and corrosivity of VOC-free, no-clean fluxes using standard, modified and electrochemical methods," *Soldering and Surface Mount Technology*, v 8, n 1, 1996, p 1-9.

[68]. E. Pope, J. Watson, D. Kennish, "Evaluation of no-clean fluxes for high reliability applications," *Materials Research Society Symposium - Proceedings*, v 390, *Electronic Packaging Materials Science VII*, 1995, p 231-243.

[69]. H. A. Chan, "Is the current surface insulation resistance (SIR) methodology appropriate to today's manufacturing technology?," *Proceedings - Electronic Components and Technology Conference*, 1996, p 234-241.

[70]. M. E. Jozefowicz, N. Lee, "Electromigration versus surface insulation resistance test," *International Journal of Microcircuits and Electronic Packaging*, v 17, n 3, Third Quarter, 1994, p 280-292.

[71]. J.E. Sohn, U. Ray, "Weak organic acids and surface insulation resistance ," *Circuit World*, v 21, n 4, Jul, 1995, p 22-26.

[72]. T. Crawford, "Conformal coating adhesion over low residue fluxes," *EMPF (Electronic Manufacturing Productivity Facility) Report*, n PP0014, May, 1995, p 1-7.

[73]. Chemical Society (Great Britain), *Electrochemistry*, Chemical Society, London, 1969.

[74]. E. M. Bumiller, "Electrochemical migration on FR-4 printed circuit board surfaces," 2003, M.S. Thesis.

[75]. *Electrochemical processing*, Plenum Press, New York, 1981.

[76]. M.D. Danford, *Electrochemical studies of corrosion inhibitor,* National Aeronautics and Space Administration, Office of Management, Scientific and Technical Information Division, 1990.

[77]. *Electrochemical technology*, Manchester, N.H., Electrochemical Society, 1963-1968.

[78]. NASA, Corrosion Control and Treatment Manual, TM-584C, November 1,1994

[79]. P. Roberge, *Handbook of Corrosion Engineering*, Washington, D.C.: McGraw-Hill, 2000.

[80]. ASTM G82-98 Standard: Guide for Development and Use of a Galvanic Series for Predicting Galvanic Corrosion Performance, American Society for Testing and Materials, West Conshohocken (PA)

[81]. InterCorr International, *Learning Center: Crevice Corrosion*, Retrieved on November 2, 2001 on the World Wide Web. http://www.corrosionsource.com/learningcenter/crevice.htm

[82]. H. Leidheiser, *The Corrosion of Copper, Tin, and Their Alloys*, John Wiley & Sons, New York, NY, 1961.
[83]. Webster's Revised Unabridged Dictionary, © 1996, 1998 MICRA, Inc.
[84]. NIST, Metallurgy Division, *Phase Diagrams & Computational Thermodynamics*, http://www.metallurgy.nist.gov/phase/solder/solder.html, Nov 2006.
[85]. F. Song and S.W.R. Lee, "Corrosion of Sn-Ag-Cu Lead-free Solders and the Corresponding Effects on Board Level Solder Joint Reliability", Electronic Components and Technology Conference, 2006. Proceedings. 56th 30 May-2 June 2006 Page(s):891 – 898.