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Simulation and Design Optimization of Germanium-on-Silicon Single Photon Avalanche Diodes

Charles Smith^a, Jaroslaw Kirdoda^a, Derek C.S. Dumas^a, Conor Coughlan^a,
Charlie McCarthy^a, Hannah Mowbray^a, Muhammad Mirza^a, Fiona Fleming^b, Xin Yi^b,
Lisa Saalbach^b, Gerald S. Buller^b, Douglas J. Paul^a, and Ross W. Millar^a

^aJames Watt School of Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, United Kingdom

^bInstitute of Photonics and Quantum Sciences, School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh EH14 4AS, UK

ABSTRACT

Single photon avalanche diodes (SPADs) are semiconductor photodiode detectors capable of detecting individual photons, typically with sub-ns precision timing. We have previously demonstrated novel pseudo-planar germanium-on-silicon SPADs with absorption into the short-wave infrared, which promise lower costs and potentially easier CMOS integration compared to III-V SPADs. Here we have simulated the dark count rate of these devices, using a custom solver for McIntyre's avalanche model and a trap assisted tunnelling generation model. Calibration and fitting have been performed using experimental data and the results have highlighted areas in which the technology can be optimised.

Keywords: Single photon avalanche diode, Ge-on-Si, device simulation, Si Photonics

1. INTRODUCTION

Single photon avalanche diodes (SPADs) are semiconductor photodiode devices biased above avalanche breakdown in the so-called Geiger mode, typically with sub-ns timing resolution.¹ There is demand for single-photon detection in the short-wave infrared (SWIR) to enable long range eye-safe LIDAR,² operation in quantum systems at telecommunications wavelengths,³ as well as imaging through obscurants.⁴⁻⁶ Effective SWIR performance is not achievable with silicon SPADs due to limited absorption at wavelengths $> 1 \mu\text{m}$. We have previously demonstrated novel pseudo-planar germanium-on-silicon SPADs with absorption into the SWIR, which offer the prospect of lower costs, and easier CMOS integration compared to III-V SPADs.⁷⁻⁹ There is significant scope to optimize these devices in order to make the technology competitive with InGaAs/InP SPAD devices; this is facilitated using process and device simulation to guide design decisions. Our model uses technology computer aided design (TCAD) for simulating the fabrication and electrical properties of a device, but requires additional custom code to predict device metrics including dark count rate (DCR) and single photon detection efficiency (SPDE). Here, we use experimental data to calibrate these simulations, and investigate the spatial distribution of dark counts to gain an insight into the device dynamics.

Group IV materials have been investigated for SPADs operating in the SWIR for a number of years¹⁰⁻¹² to enable devices that can be mass produced at low cost due to Si foundry compatibility. This typically involves using a (Si)Ge absorber layer, grown epitaxially on top of a Si multiplication region, in a separate absorption charge and multiplication (SACM) geometry. Initially, strain balanced multiple-quantum well devices were demonstrated,¹³ followed by demonstration of Ge-on-Si mesa based devices,¹⁰ and subsequently a waveguide coupled SPAD was demonstrated.¹⁴ Mesa detectors are dry-etched to define the pixel active area, meaning that defective sidewalls are close to regions of high electric field. Electric field hot-spots can also be present leading to preferential edge breakdown. This led to the re-design of the Ge-on-Si SPAD pixel, using a local implanted charge sheet in conjunction with a local p+Ge contact layer to confine the electric field away from etched sidewalls for isolation,⁷ Figure 1. This device had an active area diameter of $100 \mu\text{m}$, it demonstrated SPDEs up to 38 % at 1310 nm wavelength, and facilitated LIDAR measurements in laboratory conditions.^{15,16} A scaled, $26 \mu\text{m}$ diameter pixel

Further author information: (Send correspondence to Prof Douglas J. Paul, Dr Ross W. Millar)
E-mail: Douglas.Paul@glasgow.ac.uk, Ross.Millar@glasgow.ac.uk

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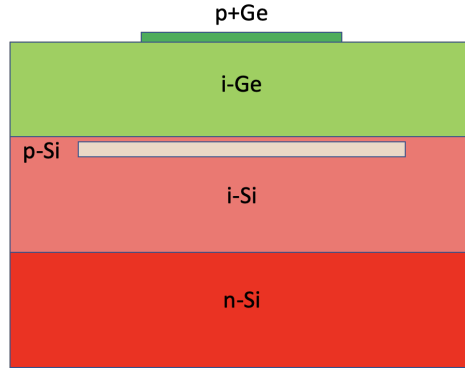


Figure 1. Schematic showing pseudo-planar Ge-on-Si SPAD structure.

was subsequently demonstrated,⁸ which showed a record low noise-equivalent power of $7.7 \times 10^{-17} \text{ W/Hz}^{0.5}$ operating at 1310 nm wavelength; approximately two orders of magnitude lower than an equivalent mesa device. The devices, however, still required operation at temperatures below 175 K, and therefore further optimisation is required to achieve operation temperatures achievable with Peltier-coolers ($\sim 230 \text{ K}$). By reducing dark-count rates by elimination of electric field hot-spots, devices can be operated at higher temperatures for a given DCR. Increasing the operation temperature can also improve detection efficiencies towards 1550 nm wavelength, as the band-gap red-shifts at higher temperatures. This optimisation requires insight through device modelling to understand the dynamics of the pseudo-planar geometry.

2. SIMULATION

In this work, Synopsys Sentaurus is used to simulate Ge-on-Si SPAD devices. Initially, a processing module is used to simulate the fabrication process (described in detail in a previous publication⁷). This includes the ion-implantation of the charge-sheet layer, which is used to mediate the electric field profile in the device such that Si multiplication layer is above breakdown, while the absorber remains at only moderate field, sufficient to sweep out photo-generated carriers. The simulation accounts for high temperature activation and anneal steps, to accurately capture dopant diffusion in the device, which can influence the electric field profile.

The results of the process simulator serve as the input to a Device simulation package, which solves drift-diffusion equations and the continuity equations to calculate the electric field profile in the device. In this work, 2D simulations are run which are later scaled to 3D by exploiting the rotational symmetry of the detector. Simulations are run to calculate the electric field profile beyond the breakdown field, to mimic the state of the device while it is biased above breakdown but before it has triggered. As such, ionisation gain is disabled in the TCAD model. Using the charge-sheet values obtained by secondary ion mass spectroscopy (SIMS), the model gave good agreement with experiment with regard to the observed punch-through and breakdown voltages, which gives confidence in the calculated electric field profile. The TCAD package does not allow for metrics such as dark-count rate to be solved directly. In order to achieve this, custom code was written, which uses the electric field as an input. The dark count rate is calculated using McIntyre's model¹⁷ to translate the device electric field into triggering probabilities, by solving the following coupled differential equation:

$$\begin{aligned} \frac{\delta P_E}{\delta x} &= -(1 - P_E)\alpha_E(P_E + P_H - P_E P_H) \\ \frac{\delta P_H}{\delta x} &= (1 - P_H)\alpha_H(P_E + P_H - P_E P_H) \end{aligned} \quad (1)$$

Here, P_E is the electron triggering probability, P_H is the hole triggering probability and $\alpha_{E,H}$ are the electron/hole impact ionisation coefficients, which are functions of the electric field. Figure 2 shows an example of the electric field from a vertical line-cut through the device, and the corresponding triggering probability for

electrons, holes, and the joint triggering probability, which can be given as $P_J = P_E + P_H - P_E P_H$. It is implicit in this model that carriers generated in the Ge are collected, i.e. the collection efficiency is 1, which may serve to overestimate DCR. To approximate a 2D structure, it is typical to solve along multiple vertical line-cuts through the device. Here, however, we solve this integral along electric field lines, which can more accurately capture edge effects. This allows the creation of a spatial probability map, which shows the probability that the device will generate a self-sustaining current pulse if a electron/hole is generated at a given point.

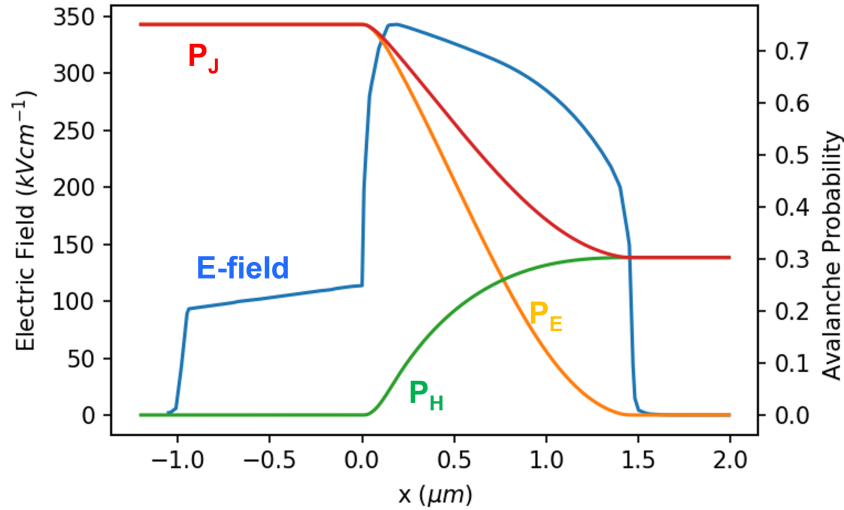


Figure 2. E-field and Electron (P_E), hole (P_H) and joint (P_J) triggering probabilities, solved along a line cut of a Ge-on-Si pseudo-planar SPAD.

Figure 3 shows a 2D simulation of a single Ge-on-Si SPAD biased above breakdown with the E-field shown on the left side of the pixel, and with the triggering probability shown on the right. This highlights that the triggering probability appears to be dominated by the p+Ge layer as opposed to the locally implanted charge sheet. It is evident that there is still a significant electric field towards the edge of the pixel, and this may explain the relatively high dark currents observed in experimental measurements for the corresponding DCR, i.e. it suggests there is an un-multiplied leakage current in the device that may not be detrimental to DCR but will increase power consumption.

In order to calculate the DCR, the generation rate at a given point is multiplied by the triggering probability at that point, and integrated over the full structure. Using y as the radial axis this can be given as:

$$\text{DCR} = 2\pi \int P_j(x, y)G(x, y)y dx dy. \quad (2)$$

Here, G is the generation rate. In order to calculate the generation rate, a modified Shockley-Read-Hall (SRH) generation model is implemented. This model¹⁸ includes a modifier term, Γ , which models the effects of the electric field. As such, the model accounts for both thermal-assisted generation and trap-assisted tunnelling (TAT). Band-to-band tunnelling was calculated¹⁹ and was found to be negligible at the electric fields present in the device. The modified SRH expression including TAT is given below, where $\tau_{n,p}$ are the electron/hole lifetimes, n_i is the intrinsic carrier concentration, and E_T and E_i are the trap energy and the intrinsic Fermi-level respectively

$$G_{\text{TAT}} = \frac{n_i}{\frac{\tau_n}{1+\Gamma} e^{-(E_T-E_i)/k_B T} + \frac{\tau_p}{1+\Gamma} e^{(E_T-E_i)/k_B T}}. \quad (3)$$

The intrinsic carrier concentration is calculated as a function of temperature, and includes the effects of the $\sim 0.18\%$ tensile strain in the Ge epi-layer. Here, the electron and hole lifetimes are unknown and are assumed

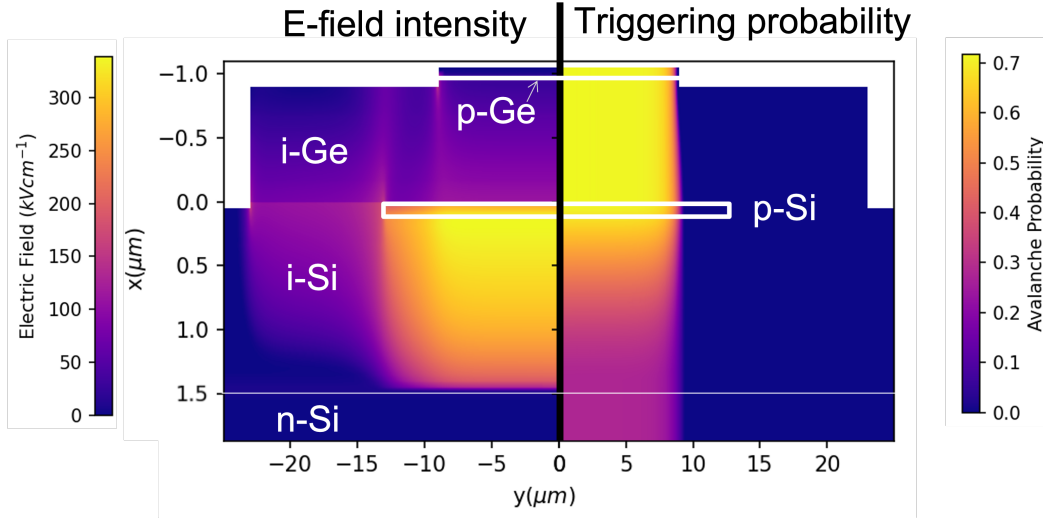


Figure 3. 2D simulation of a Ge-on-Si SPAD pixel. Left side of pixel - E-field intensity. Right side of pixel - triggering probability as calculated using equation (1).

to be equal, and used as a fitting parameter to match experimental results from a 26 μm diameter pixel.⁸ The Γ term captures the effects of the electric field, as defined by Hurkx¹⁸ as:

$$\Gamma = 2\sqrt{3\pi} \frac{|F|}{F_{\Gamma}} \exp\left(\left(\frac{F}{F_{\Gamma}}\right)^2\right) \quad (4)$$

where F_{Γ} defines a temperature dependent scaling factor to the electric field F . This introduces an additional effective tunneling mass m_t^* governing where the electric field becomes dominant by:

$$F_{\Gamma} = \frac{\sqrt{24m_t^*(k_B T)^3}}{q\hbar}. \quad (5)$$

3. RESULTS

Figure 4 shows the total DCR from the simulated device. A reasonable fit to the experimental data is found in the temperature range of 125 K to 175 K. The simulation shows some disagreement with the 100 K experimental data. At low temperatures, theory suggests that TAT begins to dominate, which is highly dependent on the electric field and the temperature. Hot spots in the device are hard to capture accurately through simulation and this is thought to be the cause of the discrepancy. It should be noted that in this work the lifetime is assumed constant, and is not spatially dependent in the device. In reality the etched sidewalls, and Si/Ge interface will have an increased defect density, with the associated increase in recombination-generation.

In order to gain more insight into the device dynamics, the spatial DCR density is shown in a 2D device cross section, alongside the generation rate in the Ge. This is shown in Figure 5, which shows a single Ge-on-Si SPAD pixel with the generation rate and DCR density shown on the left and right side respectively. It is clear that there are regions around the perimeter of the charge-sheet where the generation rate is increased due to the increased electric field. Similarly, there are regions around the p+Ge layer where the carrier generation is increased due to E-field hotspots. Comparing this to the DCR density, however, reveals that carriers originating from these spots are not able to trigger the device, i.e. they contribute to an un-multiplied dark current. The DCR density plot does show some contribution to total DCR from regions of high field extending from the edge of the p+Ge layer. In this model, sloped etches were used for the p+Ge layer to approximate the fabrication process. Vertical etches were found to produce significant hot-spots that prevented the simulation from converging. This suggests

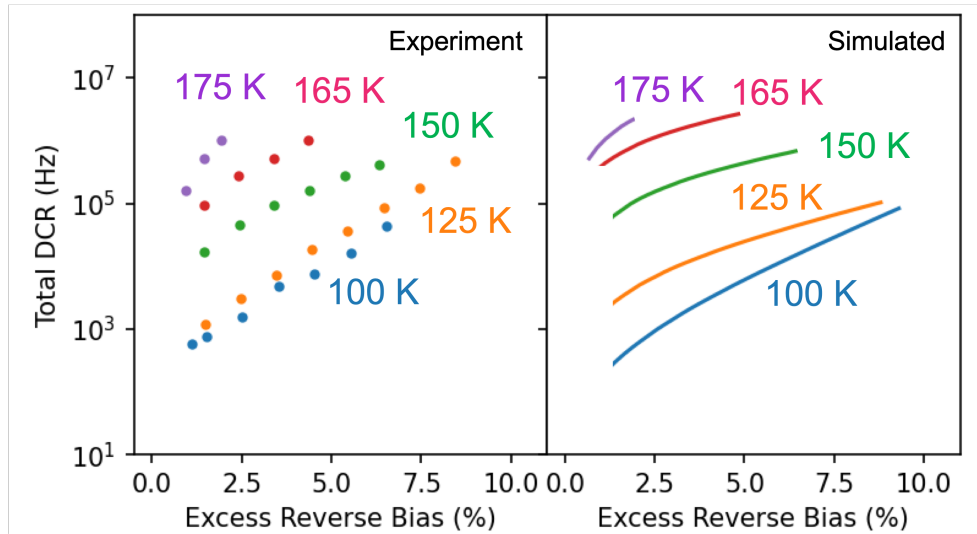


Figure 4. Left - Experimentally measured dark count rate (DCR) from a 26 μm diameter Ge-on-Si SPAD. Right - Simulated total DCR for the same device geometry.

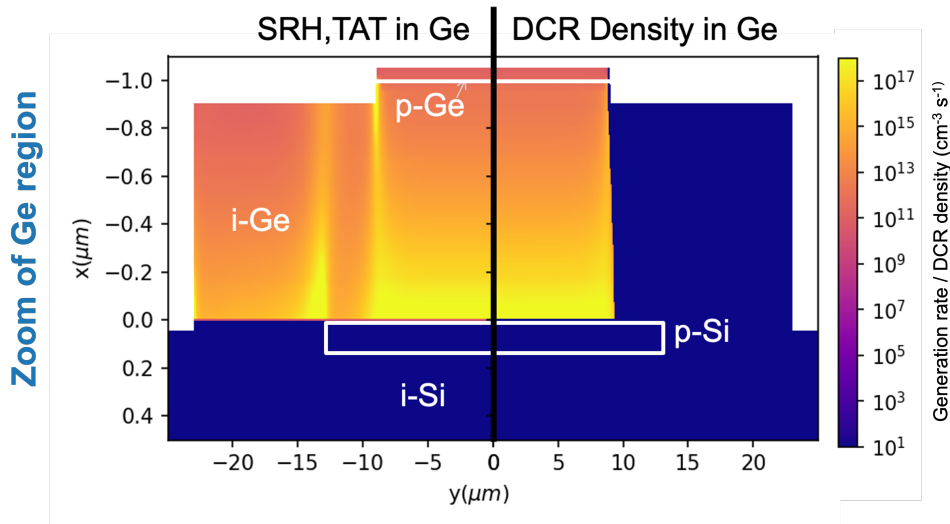


Figure 5. 2D simulation of a Ge-on-Si SPAD pixel. Left side of pixel - Generation in Ge from Shockley-Read-Hall and trap assisted tunnelling. Right side of pixel - Dark count rate per unit area.

that care needs to be taken with this etch layer and that the etch profile could play a significant role in reducing DCR. In future, implanted p+Ge regions will be investigated to determine if this can smooth E-field hot-spots. It should be noted that the relative distance between the p+Ge and the charge-sheet is likely to influence the contribution of the p-Si hot-spots, and this will be a focus of future work. Furthermore, Monte Carlo simulations may be required to fully capture the influence of the lateral device regions.

4. CONCLUSIONS

A model has been implemented to gain an understanding into the dynamics of pseudo-planar Ge-on-Si SPADs. Synopsys Sentaurus TCAD was used to simulate device process steps, including the effects of thermal processing on dopant diffusion. TCAD was also used for simulation of electric field profiles, with custom code then used for calculation of avalanche triggering probabilities and trap assisted tunneling generation rates. This data

was used to estimate DCR for a 26 μm Ge-on-Si SPAD, showing good agreement with previously published experimental measurements. Hot spots in the electric field at the edge of the implanted charge sheet and around the trench etch contribute to a higher dark current. However, these regions do not appear to generate multiplied carriers, and so do not contribute to DCR in this model. Monte Carlo simulations may be required to accurately capture carrier diffusion. In the pseudo-planar architecture the p+Ge layer was shown to largely dominate the active area of a pixel, with some dependence on the reverse bias, which will be explored further in future work. In particular, the relative diameters of the p+Ge and charge sheet layers will be explored experimentally to validate these simulations. It was found that electric field hot spots at the edge of the p+Ge layer can contribute significantly to dark currents and DCR, particularly if vertical etches are used, suggesting there is scope for optimisation to enable higher temperature operation. Further experimental work will be carried out to decouple the recombination-generation rates at interfaces and in the bulk, so that simulations can be used to accurately design novel architectures, and facilitate the optimisation of Ge-on-Si SPAD technology towards operation at Peltier cooler temperatures.

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