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ALAX – A P1355–BASED ARCHITECTURE FOR AN ATM LAN ACCESS SWITCH, WITH APPLICATION TO ATM ONBOARD SWITCHING

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Abstract

We draw attention to the new IEEE P1355 Standard for Heterogeneous InterConnect as a possible platform to support several onboard processing functions, including onboard communications and onboard ATM switching. The main features of IEEE P1355 are illustrated through a discussion of the basic principles and protocol architecture of ALAX, the ATM LAN Access Switch, currently under design in the Laboratory for Advanced Switching Technologies at the University of Maryland, College Park.

BACKGROUND

Military and civilian operations increasingly rely on the availability of efficient, reliable and flexible networking resources that support broadband transmisssion capabilities for multi–media applications. In response to emerging demands for broadband multi–media services, the telecommunications industry has sought to integrate these and future services on a single type of user–network interface. This has lead to a focused effort to define the Broadband Integrated Services Digital Network (B–ISDN). In a nutshell, B–ISDN is a standardized public–switched communication network infrastructure capable of supporting both broadband and narrowband services on a single flexible network platform, and of providing customer access over a single family of interfaces.

A standardized transport, multiplexing and switching technique called the Asynchronous Transfer Mode (ATM) has been recommended as an efficient transmission standard for B–ISDN: ATM combines the advantageous features of both the circuit- and packet–oriented techniques. The former requires only low overhead and processing, and once a circuit–switched connection is established, the delay in transferring information over it is low. The latter is much more flexible in terms of bit rate assigned to individual (virtual) connections. ATM is a circuit–oriented hardware–controlled low overhead concept of virtual channels which have no flow control or error recovery. These virtual channels are implemented by packing the transferred information into relatively short fixed–size packets called cells, and this provides the basis for both switching and multiplexed transmission. The use of short cells in ATM and the high transfer rates involved (up to 150 Mbps for HDTV) result in transfer delays and delay variations which are sufficiently small to afford universal applicability to a wide range of services including real–time services. The capability of ATM in multiplexing and switching at the cell level supports flexible bit rate allocation.

This evolution of the communication scenario has profound implications for the role of communication satellites in the larger context of the communication infrastructure. Indeed, it raises the possibility that the satellite be viewed not merely as a repeater, its traditional role as a bent pipe in the sky, but rather as a network node in its own right in a hopefully integrated space/terrestrial network. For instance, a suitable architecture would use a satellite subnetwork with multiple spotbeams and onboard baseband switching capabilities, thereby providing the required interconnection among the different beams. Several such advanced systems are currently under design, and the recent deployment by NASA of its advanced communication technology satellite (ACTS) represents a key step in demonstrating feasibility.

To achieve this integration, the space subnetwork architecture has to use access and switching methods that are compatible with the ATM solution adopted on the ground segment. In particular, in these advanced satellite systems, a reliable onboard fast packet switch is essential for ensuring that packets are routed from different uplink beams to different downlink beams. Although the onboard and terrestrial (ATM) switches share many similar features and capabilities, the design of an onboard fast–packet switch needs to incorporate additional factors due to the unique satellite communication environment; these factors include size, power, reliability, fault–tolerance, multicasting and congestion control, to name a few.

IEEE P1355

The requirements imposed on onboard switching capabilities call for design approaches which are different from those followed in designing conventional ATM switches for terrestrial networks. In that context, we draw attention to the IEEE P1355 Standard for Heterogeneous InterConnect (HIC) (IEEE 1995, Kim 1995), a new serial bus standard which provides data interconnect between communication modules with scalability, flexibility and simplicity. The P1355 Standard is ideally suited for designing interfaces between legacy LAN's and the ATM world; such an approach has been demonstrated in the ongoing work on ALAX, the ATM LAN Access Switch, under design in the Laboratory for Advanced Switching Technologies at the University of Maryland, College Park (Kim and Ryu 1995, Ryu and Kim 1995). In light of our recent experience with ALAX, we believe that the P1355 Standard would indeed represent a very promising approach for addressing some of the design issues inherent to the onboard environment.

The IEEE P1355 Standard affords low cost, low latency scalable serial interconnect for parallel system construction. This protocol was also submitted to the ISO/IEC JTC1 standard committee, and accepted as standard. IEEE P1355 specifies the physical connectors and cables to be used, the electrical properties of the interconnect, and a cleanly separated set of logical protocols to perform the interconnection in the simplest possible way. The purpose of this standard is to enable high–performance, scalable, modular, parallel systems to be constructed with low cost, where "cost" must include not only the price of components, but also the enginering effort to use them successfully

The purposes of the P1355 Standard are manifold: (i) To enable high–performance parallel systems which are scalable and modular to be constructed with low system integration cost; (ii) to support communication fabric; (iii) to provide a transparent implementation of a wide range of high–level protocols; (iv)

to support communication links between heterogeneous systems. Of great importance is the P1355 serial bus architecture, which provides a solution to the bottleneck problem within the high–speed communication system.

At the heart of the IEEE P1355 standard is the realization that the requirements for performance, scalability and low cost can be met by allowing many instances of a cheap component to operate concurrently. Thus the interconnect should consist of many separate connections operating simultaneously to give a high aggregate performance. Provided each component can be utilized at a reasonable level, its raw performance need not be very high, allowing both component and engineering costs to be kept down. For maximum simplicity, modularity and fault–tolerance, each connection should be point–to–point. The requirement of low cost implies that at the very least, a connection to the interconnect can be implemented with a relatively small ammount of circuitry in a non–exotic technology. Ideally such a connection could be integrated onto a chip with a processor or other device to minimize costs. The requirement of a small amount of circuitry implies that protocols must be simple and require minimal buffering. The first implementations of some of these ideas are already available commercially, e.g., SGS-Thompson's Data–Strobe Link interface device fo high–speed asynchronous communications which support the C104 Asynchrnous Packet Switch.

These features are ideally suited for implementation onboard a spacecraft where communication links are short and system components need to space–hardened against radiations. As an added advantage, the adoption of the IEEE P1355 standard in the design of the onboard switch provides a framework for naturally integrating other onboard communication processes by suitable protocol conversion.

ALAX

As mentionned earlier, we have already used the IEEE P1355 Standard in designing an interface between legacy LAN's and the ATM world; such an interface will give network managers the option of gradually integrating ATM technology into existing networks. A summary of the architectural features of ALAX are available in (Kim and Ryu·1995, Ryu and Kim 1995); an OPNET simulation model, which is in its last stage of development, will provide a tool for assessing end–to–end performance. This project is the result of the collaboration between the Protocol Engineering Center of the Electronics and Telecommunications Research Institute (ETRI), the Institute for Systems Research at the University of Maryland, College Park and Modacom Co. Ltd.

The most important design characteristic of ALAX lies in its adoption of the IEEE P1355 Standard as the data communication paths within the ALAX switching fabric. This makes it possible to design a high–performance switching system with a parallel architecture in conformance with emerging open technologies and related standards. ALAX will have packet conversion capabilities between ATM and legacy LAN's, as well as the ability to route packets from LAN to LAN. Initially, the system will be built in a IBM PC environment with the IEEE P1355 serial bus data communication capability.

This approach provides easy expandability by following the modularity design concept. Many applications can be added to the system by inserting the application modules into the slots of the ALAX. This insertion of new modules can be achieved without changing the entire architecture by taking advantage of the the scalable, modular and parallel structure of the P1355 serial bus. The future applications to be implemented in this system include MPEG2 over ATM, interface to N–ISDN, Multiprotocol over ATM, ATM terminal interface and Circuit emulation, etc. In the first phase of this design effort an ATM hub system will be built with the capability of LAN emulation over ATM for Ethernet LAN. This first version of the ALAX include: (i) ATM to P1355 Interface; (ii) P1355 Virtual Switch Fabric; (iii) Ethernet to P1355 Interface.

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