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IEEE 1355-Based Architecture for an ATM Switch: A Case
for Onboard Switching and Processing

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IEEE 1355-BASED ARCHITECTURE FOR AN ATM SWITCH:
A CASE FOR ONBOARD SWITCHING AND PROCESSING

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Abstract

The recent evolution of the communication scenario has profound implications for the role of communication satellites within the communication infrastructure. Indeed, it raises the possibility that the satellite be viewed not merely as a repeater but rather as a network node in its own right in a hopefully integrated space/terrestrial network. We draw attention to the new IEEE 1355 Standard for Heterogeneous InterConnect as a possible platform to support several onboard processing functions, including onboard communications and onboard ATM switching. The IEEE 1355 is a new serial bus standard which enables high-performance, scalable, modular, parallel systems to be constructed with low system integration cost. This IEEE 1355-based approach can satisfy many of the requirements of onboard communications and onboard ATM switching, e.g., size, flexibility, reliability, fault-tolerance, and high communication processing speeds. This is made possible by using the highly integrated 1355 chipsets and performing protocol processing with multiple transputers in parallel. The IEEE 1355 approach also allows for easy expandability owing to its inherent design modularity.

Introduction

Military and civilian operations increasingly rely on the availability of efficient, reliable and flexible networking resources that support broadband transmission capabilities for multi-media applications. In response to emerging demands for broadband multi-media services, the telecommunications industry has sought to integrate these and future services on a single type of user-network interface. This has lead to a focused effort to define the Broadband Integrated Services Digital Network (B-ISDN). In a nutshell, B-ISDN is a standardized public-switched communication network infrastructure capable of supporting both broadband and narrowband services on a single flexible network platform, and of providing customer access over a single family of interfaces.

A standardized transport, multiplexing and switching technique called the Asynchronous Transfer Mode (ATM)[1, 2, 3] has been recommended as an efficient transmission standard for B-ISDN: ATM combines the advantageous features of both the circuit and packet oriented techniques. The former requires only low overhead and processing, and once a circuit-switched connection is established, the delay in transferring information over it is low. The latter is much more flexible in terms of bit rate assigned to individual (virtual) connections. ATM is a circuit-oriented hardware-controlled low overhead concept of virtual channels which have no flow control or error recovery. These virtual channels are implemented by packing the transferred information into relatively short fixed-size packets called cells, and this provides the basis for both switching and multiplexed transmission.

The use of short cells in ATM and the high transfer rates involved result in transfer delays and delay variations which are sufficiently small to afford universal applicability to a wide range of services including real time services. The capability of ATM in multiplexing and switching at the cell level supports flexible bit rate allocation.

This evolution of the communication scenario has profound implications for the role of communication satellites in the larger context of the communication infrastructure. Indeed, it raises the possibility that the satellite be viewed not merely as a repeater, its traditional role as a bent pipe in the sky, but rather as a network node in its own right in a hopefully integrated space/terrestrial network. For instance, a suitable architecture would use a satellite subnetwork with multiple spot beams and onboard baseband switching capabilities, thereby providing the required interconnection among the different beams. Several such advanced systems are currently under design, and the recent deployment by NASA of its advanced communication technology satellite (ACTS) represents a key step in demonstrating the feasibility of this concept.

To achieve this integration, the space subnetwork architecture has to use access and switching methods that are compatible with the ATM solution adopted on the ground segment. In particular, in these advanced satellite systems, a reliable onboard fast packet switch is essential for ensuring that packets are routed from different uplink beams to different downlink beams. Although the onboard and terrestrial (ATM) switches share many similar features and capabilities, the design of an onboard fast-packet switch needs to account for additional factors which are unique to the satellite communication environment; these factors include size, power, reliability, fault-tolerance, multicasting and congestion control, to name a few.

The requirements imposed on onboard switching capabilities call for design approaches which are different from those followed in designing conventional ATM switches for terrestrial networks. In that context, we draw attention to the IEEE 1355 Standard for Heterogeneous InterConnect (HIC)[4], a new serial bus standard which provides data interconnect between communication modules with scalability, flexibility and simplicity. The IEEE 1355 Standard is ideally suited for designing interfaces between legacy LAN's and the

ATM world; such an approach has been demonstrated in the ongoing work on ALAX, the ATM LAN Access Switch based on IEEE 1355, under design in the Laboratory for Advanced Switching Technologies (LAST) at the University of Maryland, College Park[5, 6, 7]. In light of our recent experience with ALAX, we believe that the 1355 Standard would indeed represent a very promising approach for addressing some of the design issues inherent to the onboard environment.

This paper is organized as follows: In the next section, IEEE 1355 and ALAX are briefly described. We then follow up with a conceptual design of the Satellite Onboard ATM Switch (SOAS) based on IEEE 1355. The design issues covered here include hardware architecture, packet conversion and Packet Mapping Layer (PML).

IEEE 1355 and ATM LAN Access Switch

As mentioned earlier, we have already used the IEEE 1355 Standard in designing an ATM LAN Access Switch to provide the interface between legacy LAN's and the ATM world. In this section, we review the key features of IEEE 1355, and then describe ALAX which was designed in LAST.

IEEE 1355

The IEEE 1355 Standard affords low cost, low latency scalable serial InterConnect for parallel system construction. This protocol was accepted as an IEEE standard in September 1995, and also submitted to the ISO/IEC JTC1 standard committee. IEEE 1355 specifies the physical connectors and cables to be used, the electrical properties of the interconnect, and a cleanly separated set of logical protocols to perform the interconnection in the simplest possible way. The purposes of the 1355 Standard are manifold: (i) To enable high-performance parallel systems which are scalable and modular to be constructed with low system integration cost where "cost" must include not only the price of components, but also the engineering effort to use them successfully; (ii) to support communication fabric; (iii) to provide a transparent implementation of a wide range of high-level protocols; (iv) to support communication links between heterogeneous systems.

Of great importance is the 1355 serial bus architecture, which provides a solution to the bottleneck problem within the high-speed communication system.

ALAX

As mentioned earlier, we have already used the IEEE 1355 Standard in designing an interface between legacy LAN's and the ATM world; such an interface will give network managers the option of gradually integrating ATM technology into existing networks. An OPNET simulation model, which is in its last stage of development, will provide a tool for assessing end-to-end performance.

The main function of the ALAX is to provide interfaces among different legacy communication networks and the ATM world. The design objective of the ALAX system is to achieve an excellent performance/cost ratio while simplifying the overall systems engineering process, rather than to achieve the highest possible speeds. The LAN to ATM interface protocol of the first phase of the ALAX will be the LAN Emulation which is now documented as LAN Emulation Over ATM Specification by the LAN Emulation SWG Drafting Group[8] of the ATM Forum. The system modules which are needed to build the first LAN Emulation version of the ALAX are the ATM Interface module, Switch Matrix module and Ethernet Interface module.

There are several important design characteristics of the ALAX system which differentiate it from existing and emerging systems. The most important design characteristic of the ALAX system is the high level of technology integration inherent in our system by virtue of the adoption of the IEEE 1355 Standard for Heterogeneous Inter Connect (HIC) as the internal data communication paths of the switching system. The ALAX system will be built on the PCI Bus-based IBM PC[9, 10, 11, 12] and will incorporate the IEEE 1355 serial bus data communication capability through existing IEEE 1355 standard related chipsets. The core of this system is the SGS-THOMSON Microelectronics' ST C104 Asynchronous Packet Switch chipset[13] which interconnects 32 high bandwidth (100 Mbps) serial communication links (DS-Link™) via a 32 x 32 non-blocking crossbar switch with a 200 Mpackets/sec processing capability and less than 1 usec packet latency. A second important design characteristic of the

ALAX system is its adoption of the multiprocessor approach using multiple T9000 transputers[14, 15, 16, 17, 18]. This approach can satisfy the high communication processing requirements of the ALAX system by performing protocol processing with multiple transputers in parallel. The third important design characteristic of the ALAX system is its easy expandability owing to the modularity of its design. Many network interfaces can be added to the system by inserting appropriate interface modules into the slots of the ALAX. The new interfaces can be inserted into this system without changing the entire architecture; this is achieved with the help of the scalable, modular and parallel structure of the IEEE 1355 serial bus.

Conceptual Design of the Satellite Onboard ATM Switch Based on IEEE 1355

A Satellite Onboard ATM Switch (SOAS) based on IEEE 1355 is now conceptually designed at LAST as a collaborative project between the Protocol Engineering Center (PEC) of the Electronics and Telecommunications Research Institute (ETRI), the Institute for Systems Research (ISR) at the University of Maryland, College Park and Modacom Co. Ltd. The design issues of the SOAS are now described.
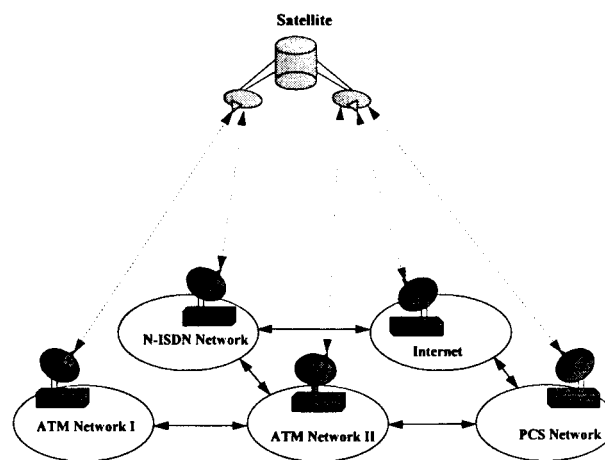

Figure 1. Network Environment of the SOAS.

The communication network environment where SOAS works is shown in Figure 1. As we can see in this Figure, the SOAS should be able to switch multiple spot beams from different ground networks by virtue of the onboard baseband switching capabilities, thereby providing the required interconnection among the different beams from different ground networks.

IEEE 1355 in the SOAS

At the heart of the IEEE 1355 standard is the realization that the requirements for performance, scalability and low cost can be met by allowing many instances of a cheap component to operate concurrently. Thus the interconnect should consist of many separate connections operating simultaneously to give a high aggregate performance. Provided each component can be utilized at a reasonable level, its raw performance need not be very high, allowing both component and engineering costs to be kept down. For maximum simplicity, modularity and fault-tolerance, each connection should be point-to-point. The requirement of low cost implies that at the very least, a connection to the interconnect can be implemented with a relatively small amount of circuitry in a non-exotic technology. Ideally such a connection could be integrated onto a chip with a processor or other device to minimize costs. The requirement of a small amount of circuitry implies that protocols must be simple and require minimal buffering. The first implementations of some of these ideas are already available commercially, e.g., SGS-THOMSON's Data-Strobe Link interface device for high-speed asynchronous communications which support the C104 Asynchronous Packet Switch.

These features are ideally suited for implementation onboard a spacecraft where communication links are short and system components need to space-hardened against radiation. As an added advantage, the adoption of the IEEE 1355 standard in the design of the onboard switch provides a framework for naturally integrating other onboard communication processes by suitable protocol conversion. Therefore, the IEEE 1355-based approach can satisfy the requirements of onboard communications and onboard ATM switching like size, flexibility, reliability, fault-tolerance, and high communication processing speeds.

Hardware Architecture of the SOAS

To satisfy the requirements already mentioned, SOAS hardware should provide high communication processing speeds, a high-speed internal data communication path and the flexibility in handling different packet types. This is possible by adopting the IEEE 1355 into the SOAS. First, high communication processing speeds can be achieved by using multiple Transputers which are equipped with IEEE 1355 DS-Link™. Secondly, the high-speed internal data communication path is possible by using the SGS-THOMSON's C104 Asynchronous Packet Switch fabric chipset as the central switch matrix unit. Therefore, the IEEE 1355 communication path acts as a turbo charger of the bus-based architecture by adding extra internal data communication capabilities to the bus-based system. This is the main reason as to why the system with IEEE 1355 shows much higher internal data communication speeds than the bus-based architecture system. Lastly, flexibility is the most important feature of the IEEE 1355 because it can handle all kinds of packets in the same manner by converting all different packet types into a simple type of 1355 packets and routing them through the C104 Matrix switch.
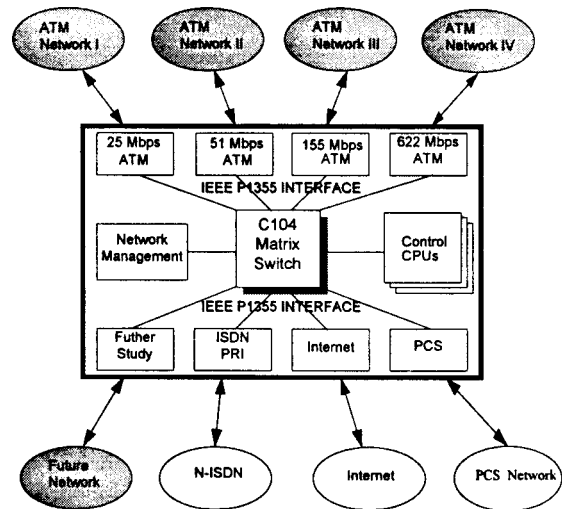

FIGURE 2. System Architecture of SOAS

The hardware architecture of the SOAS will be designed based on the experience of the ALAX architecture design. The block diagram of the SOAS is shown in Figure 2. The C104 Matrix Switch is the core

of this system with many interface modules being provided for the different ground networks. All the packets from different ground networks will be converted into IEEE 1355 packets in order to go through the C104 Matrix Switch. By using this scheme, the different packet formats and different traffic speeds can be exchanged smoothly without consuming the line capacity of the switch.

Transputers will be used as the control CPUs of the system. The required number of the transputers will be decided after an extensive simulation study. All control signals between the interface modules and the control CPU are also exchanged through the C104. The network management functions will be performed onboard by another transputer.

In addition to the different kinds of traffic (25 Mbps, 51 Mbps, 155 Mbps, 622 Mbps) of ATM networks, traffics carried by other networks like N-ISDN, PCS and Internet can be switched directly within the satellite. As future networks evolve, the SOAS can easily add interface boards to this system owing to the modularity of its design concept. Modularity is one of the most important design characteristics of the SOAS system. Many applications can be added to the system by inserting appropriate interface modules into the slots of the SOAS. The new interfaces can be inserted into this system without changing the entire architecture; this is achieved with the help of the scalable, modular and parallel structure of the IEEE 1355 serial bus. The following features are considered for the hardware design of the SOAS:

- Internal data communication paths of the system is DS-Link™ of IEEE 1355;
- ATM and AAL5 protocols are performed by ATMizer™ [19, 20, 21];
- C104 Asynchronous Packet Switch is used as the central switch matrix;
- ATM User Network Interface applies UNI 3.0 specification[22] as defined by the ATM forum;
- ATM Physical Layer applies the specification as defined by the ATM forum;
- Transputer provides the parallel processing capability.

Packet Conversion within the SOAS

All the packets which go through the SOAS should have the 1355 packet format. Therefore, packets which arrive at one of the interface adapter board should be changed into 1355 packets. The 1355 protocol stack consists of 6 levels which are the Physical, Signal, Character, Exchange, Packet and Transaction Levels. The functions of each level are explained in the IEEE 1355 Standard. Most of the protocol layers of the 1355 are executed automatically in the DS-Link™ modules of the C104 Asynchronous Packet Switch, C101 Parallel Interface Adapter and T9000 Transputers. Transaction level and part of the Packet level of the P1355 are executed by the software program execution of the T9000 Transputer.

The routing functions within the 1355 network are handled by the C104 Asynchronous Packet Switch. The C104 uses wormhole routing in which the routing decisions are taken as soon as the header of the packet has been input. If the output link is free, the header is output and the rest of the packet is sent directly from input to output without being stored; if the output link is not free the packet is buffered. The behavior of the packet transmission within the ALAX will be simulated and analyzed, and the optimal architecture of the SOAS system will be designed accordingly.

Packet Mapping Layer of the SOAS

The Packet Mapping Layer (PML) Protocol is the interface protocol between the ground networks and IEEE 1355, and is being developed as a part of this project. The PML protocol is needed within the SOAS because all the packets should be converted to the 1355 packets before passage through the switch fabric of the SOAS. The main functions of the PML are local addressing and conversion to the 1355 packet format. The function of the local addressing is to obtain the local address which comprises the 1355 packet destination port number of the C104 Asynchronous Packet Switch chipset. The term "local" in this usage means that the location of the sending and receiving ports are located within the same product system enclosure. This local address is in one-to-one correspondence with the port number of the C104 chipset. In order to accomplish the local addressing function, we will use the Local Address Look-Up Table (LALUT) which was already used in designing the ALAX system.

In order to go through the C104 Switch Fabric, all

the packets within the ALAX system should be converted to the 1355 packet. The conversion between the ATM packet and the 1355 packet format is performed automatically at the DS-Link™ hardware module of the T9000 Transputer of the ATM interface modules. Each ATM cell should be divided into two 1355 packets and the headers, derived from executing the Local Addressing functions, are attached to each of these two 1355 packets. We can define the size of the 1355 packets by programming the T9000. In this SOAS implementation, 1355 packets are 32 bytes long; this is the maximum packet size the T9000 Transputer can handle. When the maximum size which can be handled by the 1355 chipsets is increased by the new product line of the SGS-THOMSON, the optimal size can be decided by performance analysis.

In the case of the non-ATM packets, the packet conversion is performed in the same way as for the ATM packet described above. However, this time it will be performed automatically at the DS-Link™ hardware module of the T9000 Transputer at each ground interface modules and the number of 1355 packets and the size of each 1355 packet will be decided differently from the ATM packet case. The higher level gateway function among all different networks can be performed at the interface modules of SOAS or at the ground station of each network.

Conclusions

In this paper, we have reviewed the design issues of the Satellite On-board ATM Switch (SOAS) which is under design at the Laboratory for Advanced Switching Technologies (LAST). The design goal of the SOAS is to achieve next generation satellite ATM switching in an environment where the satellite be viewed not merely as a repeater, but rather as a network node in its own right in a hopefully integrated space/terrestrial network. The requirements imposed on onboard switching capabilities call for design approaches which are different from those followed in designing conventional ATM switches for terrestrial networks.

By adopting the IEEE 1355 standard in the design of the onboard switch, we can achieve a framework for naturally integrating other onboard communication processes by suitable protocol conversion. Therefore,

this IEEE 1355-based approach can satisfy the requirements of the onboard communications and onboard ATM switching like size, flexibility, reliability, fault-tolerance, and high communication processing speeds. This is made possible by using the highly integrated 1355 chipsets and performing the protocol processing with multiple transputers in parallel. The IEEE 1355 approach also guarantees easy expandability owing to the modularity of its design.

Acknowledgments

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