# TECHNICAL RESEARCH REPORT

Design of an ATM LAN Access Switch Based on IEEE P1355

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**CSHCN T.R. 95-17**
**(ISR T.R. 95-114)**


*The Center for Satellite and Hybrid Communication Networks is a NASA-sponsored Commercial Space Center also supported by the Department of Defense (DOD), industry, the State of Maryland, the University of Maryland and the Institute for Systems Research. This document is a technical report in the CSHCN series originating at the University of Maryland.*

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# Design of an ATM LAN Access Switch Based on IEEE P1355

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Today, as network speeds increase dramatically and many organizations demand dedicated bandwidth to the desk, the need for communication systems with superior performance is increasing rapidly. Provision of increased bandwidth access to users via high performance ATM switches will soon become increasingly evident. However, this solution is cost-effective only if the users' investment in existing LAN architectures and equipment is protected. In order to meet this requirement, manufacturers are already providing many kinds of ATM LAN Access Switches to the market place.

An ATM LAN Access Switch (ALAX) based on IEEE P1355 is being designed at the Laboratory for Advanced Switching Technologies (LAST) as a collaborative project by a research team which consists of the Protocol Engineering Center (PEC) of Electronics and Telecommunications Research Institute (ETRI) of Korea, Institute for System Research (ISR) of the University of Maryland at College Park (UMCP) and Modacom Co., Ltd of Korea. The main function of the ALAX is to provide interfaces among different legacy communication networks and the ATM world. The design objective of the ALAX system is to achieve an excellent performance/cost ratio while simplifying the overall process of systems engineering, rather than to achieve the highest possible speeds. In this paper, some of the architectural issues involved in the ALAX design are discussed.

There are several important design characteristics of the ALAX system which differentiate it from existing and emerging systems. The most important design characteristics of the ALAX system involve the high level of technology integration inherent in our system by virtue of the adoption of the IEEE P1355 Standard for Heterogeneous Inter Connect (HIC) as the internal data communication paths of the switching system. The IEEE P1355 is a new serial bus standard which enables high-performance, scalable, modular, parallel systems to be constructed with low system integration cost. The ALAX system will be built on the PCI Bus-based IBM PC and will incorporate the IEEE P1355 serial bus data communication capability which can be achieved by using the existing IEEE P1355 standard related chipsets. The core of this system is the SGS-THOMSON Microelectronics' ST C104 Asynchronous Packet Switch chipset which interconnects 32 high bandwidth (100 Mbps) serial communication links (DS-Link™) via a 32 x 32 non-blocking crossbar switch with a 200 Mpackets/sec processing capability and less than 1 usec packet latency. A second important design characteristic of the ALAX system is the adoption of the multiprocessor approach using multiple T9000 transputers. This approach can satisfy the high communication processing requirements of the ALAX system by performing protocol processing with multiple transputers in parallel. The third important design characteristic of the ALAX system is its ability to provide easy expandability owing to the modularity of its

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design. Many applications can be added to the system by inserting appropriate interface modules into the slots of the ALAX. The new interfaces can be inserted into this system without changing the entire architecture; this is achieved with the help of the scalable, modular and parallel structure of the IEEE P1355 serial bus. Future interfaces to be implemented in this system include those for MPEG2 over ATM, NISDN, Multiprotocol over ATM, ATM terminal interface, satellite communication and PCS.

The ALAX is designed to function as an ATM LAN Access Switch which conveys LAN packets to the ATM world as well as ATM cells to the legacy LAN environment. The ALAX will also connect two separate legacy LANs by conveying the LAN packets between them. The LAN to ATM interface protocol of the first phase of the ALAX will be the LAN Emulation which is now documented as LAN Emulation Over ATM Specification by the LAN Emulation SWG Drafting Group of the ATM Forum. The legacy LAN which we are considering in the first phase is the IEEE 802.3 Ethernet LAN. The system modules which are needed to build the first LAN Emulation version of the ALAX are: ATM Interface module, Switch Matrix module and Ethernet Interface module. Currently, the first version of the ALAX has the following features:

- Internal data communication paths of the system is DS-Link™ of IEEE P1355;
- PCI bus is used as the main system bus of the PC-based system as defined in PCI Special Interest Group;
- ATM and AAL5 are performed by ATMizer™;
- LAN interface applies IEEE 802.3 Ethernet;
- ATM User Network Interface applies UNI 3.0 specification as defined by the ATM forum;
- ATM Physical Layer applies TAXI™ for the 100 Mbps multimode fiber;
- Transputer provides the parallel processing capability.

The MAC Mapping Layer (MML) Protocol is the interface protocol between LAN and P1355 and is being developed as a part of this project. The MML protocol is needed within the ALAX because all the packets should be converted to the P1355 packets before passage through the switch fabric of the ALAX. The main functions of the MML are local addressing and conversion to the P1355 packet format. The function of the local addressing is to obtain the local address which comprises the P1355 packet destination port number of the C104 Asynchronous Packet Switch chipset. The term "local" in this usage means that the location of the sending and receiving ports are located within the same product system enclosure. This local address is in one-to-one correspondence with the port number of the C104 chipset.

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**October 30, 1995**

**Laboratory for Advanced Switching Technologies**





## Contents

# Laboratory for Advanced Switching Technologies (LAST)

## 1. Project Team

- **Protocol Engineering Center**
  Electronics and Telecommunications Research Institute, Taejon, Korea
- **Institute for Systems Research**
  University of Maryland, College Park, MD
- **Modacom Co. Ltd.**
  Seoul, Korea

## 2. Project Period

From September 1994





# Design Environment

## 1. ATM LAN Access Switch Based on IEEE P1355

- Existing LAN architectures and equipments
- High -performance communication system
- Excellent performance/cost ratio
- Simplifying the overall systems engineering process
- PC based high-performance system

## 2. IEEE P1355

- Standard for Heterogeneous Inter Connect (HIC)
- Serial bus standard proposed by SGS-THOMSON
- High-performance, scalable, modular, parallel system
- ST C104 Asynchronous Packet Switch chipset

# ATM LAN Access Switch Based on IEEE P1355

## 1. Design Goal

- Utilizing the evolving standard elements and subsystems as building blocks
- Excellent performance / cost ratio
- Simplified overall process of systems engineering
- High level of technology integration inherent in our design

## 2. Why IEEE P1355 ?

- Make it possible to connect different kinds of protocols easily
- Easy to get the standardized chipsets and systems (T9000, C104)
- It solves the bus bottleneck problems of the existing system
- Cost effective PC based system is possible.





# IEEE 1355

## 1. Standard for Heterogeneous Inter Connect (HIC)

- Serial bus standard proposed by SGS-THOMSON
- Became IEEE Standard in September 1995
- Can interconnect the heterogeneous protocols

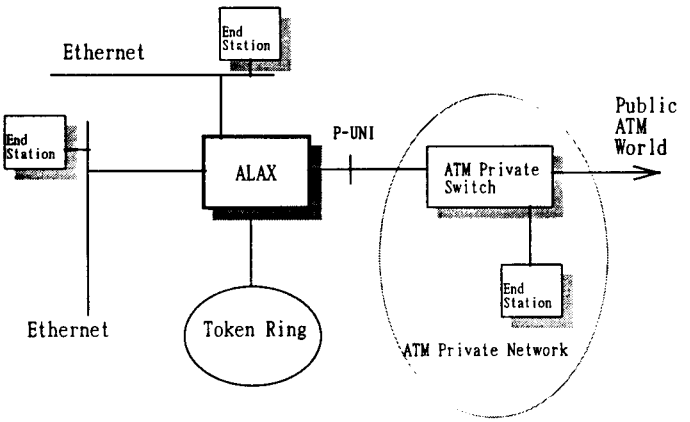
## 2. Purpose of IEEE 1355

- Enable High-performance, scalable, modular, parallel system
- Low cost, low engineering efforts (chipsets)
- Scalable serial interconnect for parallel system construction

## 3. ST C104

- Asynchronous Packet Switch
- 32 by 32 non blocking crossbar switch
- 100 Mbps DS-Link ™

## Network Environment of the ALAX








## Design Characteristics of the ALAX

**1. Adoption of the IEEE P1355**

- IBM PC based system
- Serial internal data communication paths (Solves bus bottleneck problem)
- SGS-THOMSON Microelectronics' ST C104 Asynchronous Packet Switch

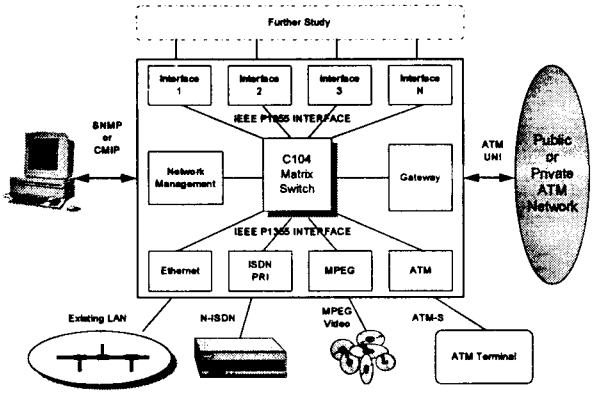
**2. Multiprocessor Approach**

- T9000 Transputers
- Parallel protocol processing
- High-performance architecture

**3. Modular Design**

- Easy Expandability
- Interface modules into the slots

## System Architecture of the ALAX



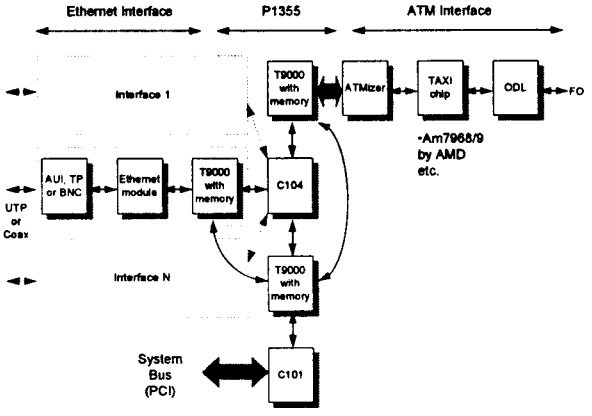





## Hardware Design Specifications of the ALAX

- Internal data communication path is DS-Link™ of the IEEE P1355
- PCI bus based IBM PC is used as the platform of the system
- ATM and AAL5 are performed by ATMizer™
- LAN Interface is for the IEEE 802.3 Ethernet
- ATM User Network Interface applies UNI 3.0 specification of the ATM Forum
- ATM Physical layer applies TAXITM for the 100 Mbps multimode fiber
- Multiple Transputers are used for the processing power of each adapter board

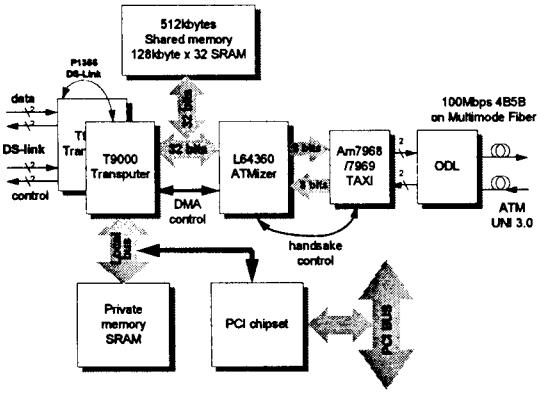
## Block Diagram of the First Version of ALAX



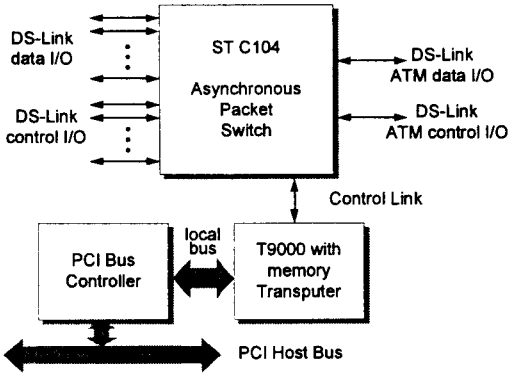





## ATM Interface Module



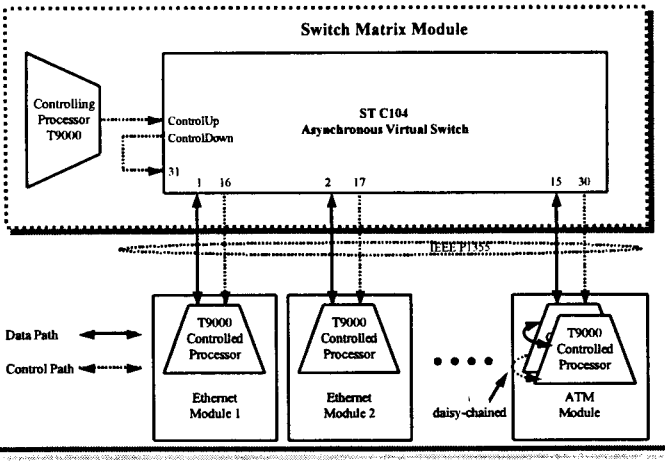
## Switch Matrix Module



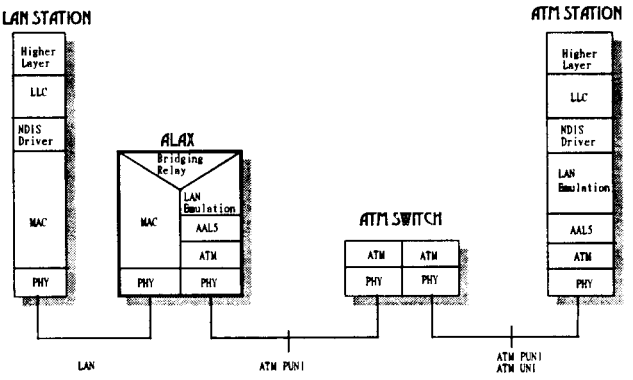





## Control and Data Link Connections via Switch Matrix Module



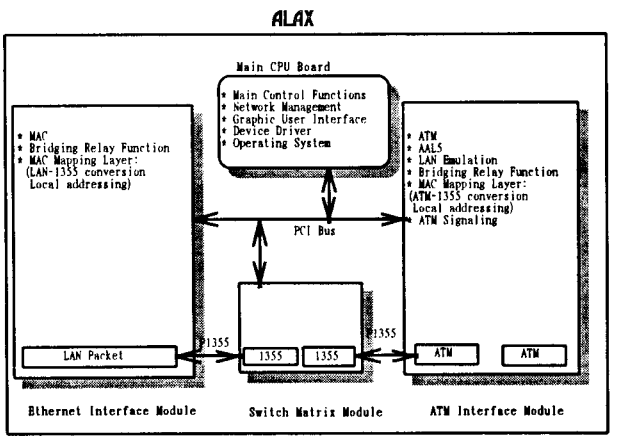
# Network Architecture of the ALAX in LAN Emulation Environment



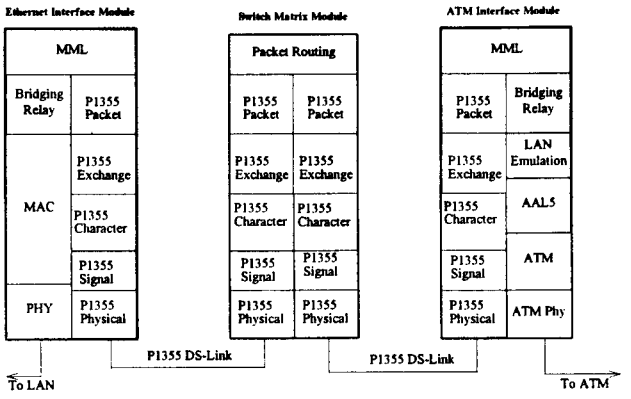





# ALAX Protocols



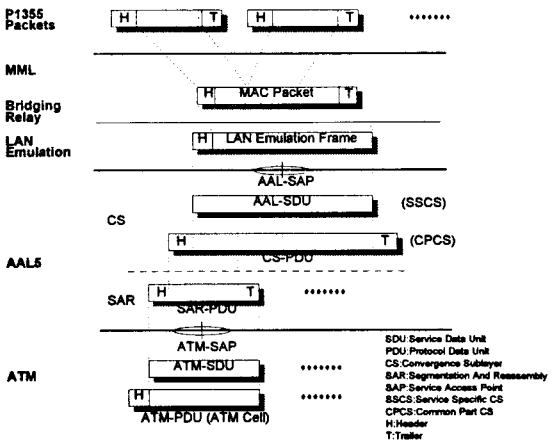
# P1355 Packet Conversion within the ALAX



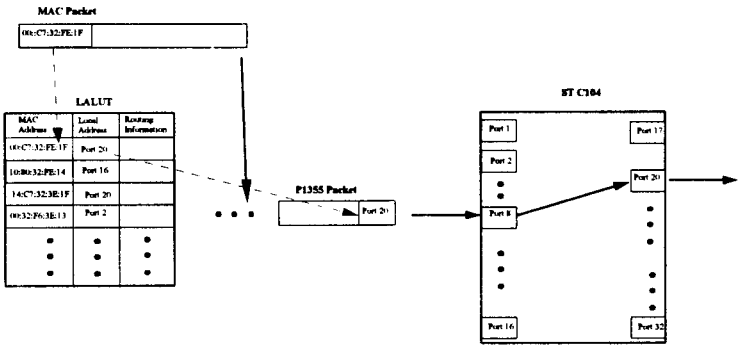





# Packet Conversion within the ATM Interface Module



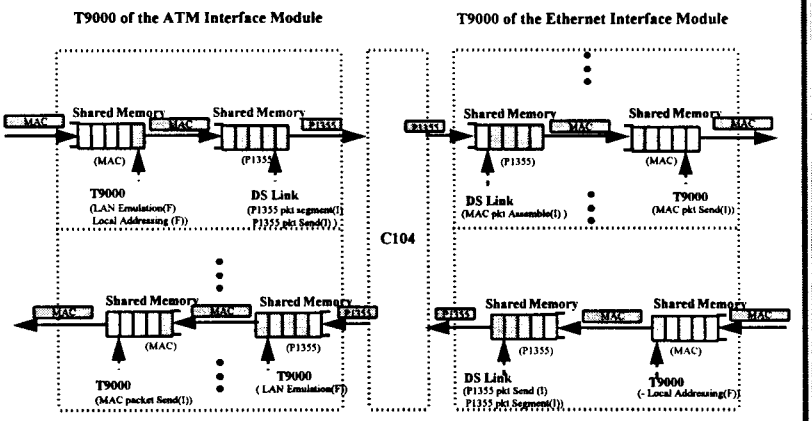
# Local Addressing of the ALAX



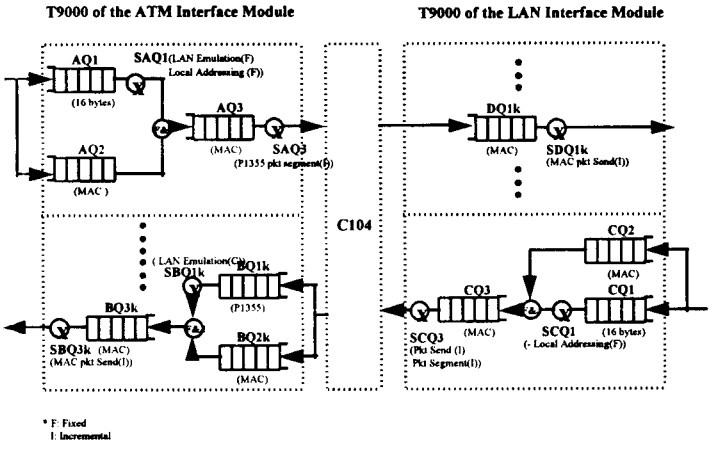





# OPNET Model of the T9000 & C104 of ALAX



# Queueing Model of the T9000 & C104 of ALAX








# Conclusions

- ATM LAN Access Switch on PC
- IEEE P1355 serial internal data communication bus
- Simplifying the overall system engineering process
- Performance analysis by OPNET simulation