ABSTRACT

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                                DIE BGA ASSEMBLIES UNDER

                                MECHANICAL BENDING LOADS

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Directed By: Prof. Michael G. Pecht, Mechanical Engineering

This thesis presents a reliability evaluation of stacked die ball grid array (BGA) assemblies under mechanical bending loads. During assembly and use conditions, it is not uncommon for these products to be subject to dynamic bending loads. It is therefore necessary to understand how stacked die BGA assemblies respond to dynamic loads.

The test specimens used in this investigation were four die stacked BGAs assembled on printed circuit boards (PCBs) with eutectic tin-lead solder and gold over nickel finishes, both as-reflowed and after aging. The failure envelopes of both types of specimen were quantified in terms of PCB flexural strain and strain rate. The experimental data from cyclic bending tests at three strain amplitudes with a constant strain rate have been used to determine the effect of strain amplitudes on cycles to failure. The experimental data from cyclic bending tests were combined with the data from impact tests to determine the effect of strain rate to cycles to failure. For the

aged specimens, the relationship between durability and PCB flexural strain and strain rate was determined using an existing power law model. It shows that durability is strongly dependent on strain and weakly dependent on strain rate within the range of conditions studied. The failure sites associated with each test condition were identified, and failure site transition phenomena are reported and discussed.

RELIABILITY EVALUATION OF STACKED DIE BGA ASSEMBLIES

UNDER MECHANICAL BENDING LOADS

By

Bo Song

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Dedicated to my parents and Zhi.

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1. Chapter one: Introduction

Stacked die ball grid array (BGA) packages have gained popularity in many applications due to the advantages of miniaturization and cost savings. In addition, stacked die configurations provide faster signal propagation than multiple single-die packages, as a result of shorter connections between chips. The technology also enables the flexibility of combining custom chips with off-the-shelf devices to further reduce total system cost and size. Portable electronics products, such as cell phones, digital cameras, personal digital assistants (PDAs), camcorders and wireless consumer systems, can benefit from the combination of multi-chip function and small footprint [1].

Stacked die packages usually are referred to as system-in-package (SIP) or three-dimensional (3-D) packages. The SIP, which incorporates stacked package and stacked die approaches, offers solutions toward faster time-to-market and business impediments that have plagued multi-chip module (MCM) deployment of the past decade. The history of SIP can be traced back to the emergence of system-on-chip (SOC). In SOC, the IC devices integrate logic, SRAM, DRAM and analogue blocks on an individual chip, which can be also called horizontal or two-dimensional (2-D) integration of IC blocks. With system-on-package (SOP), the package can function as a system. SOP includes both active and passive components in thin-film form, and functions in a microminiaturized package or board. SIP can be viewed as a certain kind of SOP. When horizontal SIP-to-SIP wiring and embedded thin film components are included in the substrate, SIP becomes SOP [2].

Stacked die packages used in mobile phones and digital cameras often contain more than two die and function for both data storage and data processing. The most common component in a stack die package includes a NAND/NOR flash memory, a static random access memory (SRAM) and a dynamic random access memory (DRAM). With the increasing requirements on data processing, logic chips are also integrated in the die stacking configuration.

As the primary use environment of stacked die packages is in portable electronic products, mechanical stress is one of the major factors affecting package reliability. Due to the rapid miniaturization of integrated circuit technology, portable electronic products become lighter and smaller by adopting a thin printed circuit board (PCB) and thin plastic housing. During assembly and use conditions, it is not uncommon for these products to be subject to different dynamic bending loads. PCB assembly and handling operations often include a variety of steps that involve monotonic bending of the PCBs, such as, in-circuit testing, depaneling process. In everyday use, the repeated key-press action can cause a large number of repeated bend cycles during the life of the product. Also these products are more prone to experience accidental impacts during their useful life due to their size and weight. These external forces can induce stresses and strains in the PCB within, which will in turn result in loading experienced by IC packages and package-to-board interconnections [3]. It is therefore essential for the products containing stacked die packages to be robust enough to withstand the dynamic loading conditions. We focused on the influence of mechanical stresses on the package reliability.

This work aimed to find out the weak link in the stacked die BGA packages assembled on printed circuit boards and the durability of these PCB assemblies (PCBA) under dynamic loading conditions. We quantified the durability of test specimens (four die stacked BGAs assembled on PCB with eutectic tin-lead solder and gold over nickel finishes) in terms of PCB flexural strain and strain rate, both as-reflowed and after aging. Failure analyses were conducted to identify the critical failure sites of test specimens at the board level, and to verify if there is any failure site associated specifically with stacked die architecture under the selected loading conditions. Failure site transition phenomenon was reported. In addition, we were also interested to find out the quality and reliability issues of stacked die package associated each manufacturing process.

The contributions of this work include several aspects. The dependence of the durability on PCB flexural strain rate in a selected stacked die BGA package was quantified in terms of cycle to failure for both as-reflowed and after aging. The dependence of the durability on PCB flexural strain in a selected stacked die BGA package was quantified in terms of cycles to failure the for both as-reflowed and after aging specimens. Failure sites for all tested conditions were identified. A failure site transition phenomenon for the selected test vehicles was observed with the increasing of PCB flexural strain, changing from solder joint to Cu trace/FR4 laminate.

2. Chapter Two: Background

2.1. *Background Information of Stacked Die Package*

The proliferation of portable consumer electronics created an insatiable and expanding need for small form factor packages in board assembly to reduce the size and weight. First, single chip packages (SCP) such as BGA, chip scale packages (CSP) including fine-pitch BGA (FBGA), and reduced sized lead frame packages such as micro-leadframe (MLF) packages are widely used in many consumer electronics device assembly. In more recent years, stacked die packages are gaining popularity over the SCP. The main reasons and advantages of adopting this new technology include:

1. More functionality per package (stacked die package may carry more functions previously required by several different SCP)

2. More capacity and higher efficiency

3. Easier circuit design and layout, quicker turn around and time to market

4. Higher manufacturing yield, lower cost and faster throughput

5. Better electrical performance in most cases

6. Modular design and more interchangeable parts

There are different die stacking configurations according to the variance of die size. Three basic configurations with wire bond interconnections are illustrated in Figure 1 to Figure 4 [4]. They are pyramid stacking, same size die stacking, and overhang stacking. Figure 1 shows pyramid die stacking, where smaller die are placed on top of larger die. In same size die stacking, a silicon interposer or a filled paste type epoxy is placed between two dies, as illustrated in Figure 2 and Figure 3. Figure 4 demonstrates the overhang

stacking configuration, where rectangular die are placed at 90 degrees on top of each other. The stacked die packages containing more than two die are normally a combination of two or more basic die stacking configurations.
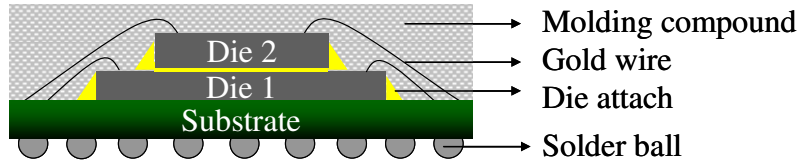
Figure 1: Pyramid stack configuration
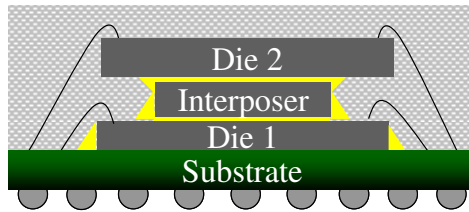
Figure 2: Same size die stack configuration with dummy die interposer
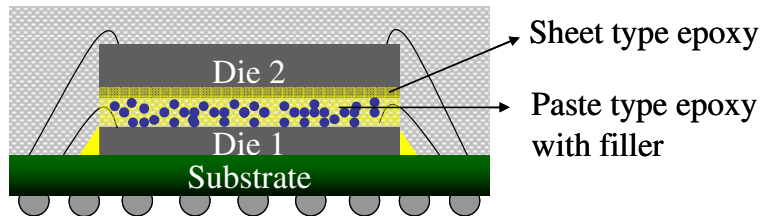
Figure 3: Same size die stack configuration with filled paste type epoxy
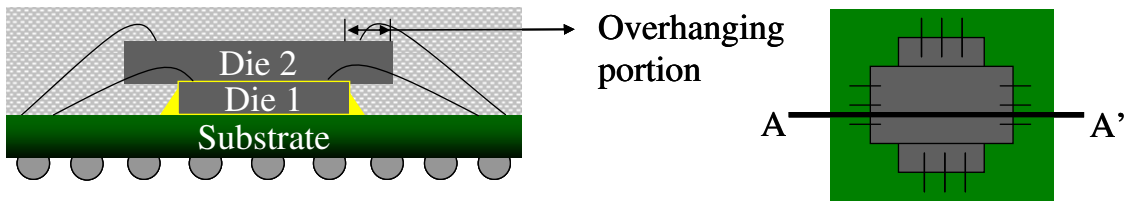
Figure 4: Overhang cross stack configuration: side view along the line AA' (left) and top view (right)

The majority of stacked die packages shipped in the past years contained two memory die, flash and SRAM die. Increasingly stacked die packages with four and five die are

shipping in production. The developments in stacked die package are summarized in Table 1 (source: [5]).

Table 1: Developments in stacked die package

Company	Max. No. of Die	Die Thickness (micron)	Package Height (mm)	Substrate Type	Interconnect
	3+spacer	100, 75	1.4	Laminate	WB
Amkor	2	175-200	1.2	Flex circuit	WB
	4	100	1.4	Laminate	WB
ASE	3	100	1.2	Laminate	WB
ChipPAC	4	100,75	1.4	Flex circuit	WB
Fujitsu	2	50	1.2	Laminate	WB
Intel	5	75,50	1.2	Laminate	WB
Mitsubishi Electric	2	150 (top) 90 (bottom)	1.2	Laminate	WB
Sharp	4	100, 84, 75	1	Flex circuit	WB
Shinko Electric		150, 100			WB
SPIL	3	100	1.4	Laminate	WB
Toshiba	6+3 spacers	85, 70	1.4	Laminate	WB

No doubt stacked die packages are currently used most widely in portable consumer electronic devices where size and weight are premium and hence the main drivers for miniaturization. With their multiple functionalities they are also moving into computing, communications and other applications in medical electronics, space and military electronics. Some practical examples of their applications are in [6].

1. RF and wireless modules such as Bluetooth module and cellular phone RF module

2. Nonvolatile memory storage NAND flash cards such as compact flash, secure digital, and multimedia card (MMC)

3. Code storage and execution package for portable devices, cell phones and PDAs using SRAM

4. High speed and high volume DRAM modules for servers and computers, notebooks

5. Small, odd form medical and specialty applications such as hearing aid, and implantable heart pacers.

Dimensional constraint is a big issue in stacked die package development. The critical dimensions in the package have to be decreased, including die thickness, mold cap clearance, die attach bond line thickness, and wire loop profile, because the number of die inside each package are continuously increased and the package height keeps decreasing. At present, many manufactures have moved from 150 μm to 100 μm thick die towards the die thickness of 50~75 μm. The state-of-the-art stacked die packages can have up to eight die stacked in one package. The challenges of stacked die packages include wafer thinning, known good die (KGD), thin die attachment, low profile wire bonding, wire bonding on overhanging die and low sweep molding, etc [5].

2.2. *Package Level Reliability Concerns*

Two important processes during stacked die fabrication are the backside grinding and wafer sawing because die thickness must be reduced to the range of 50~125 μm in order to make two or more IC chips within the standard package heights. As such, gentle and controlled wafer handling is necessary. The die attach process could be implemented by epoxy paste or tape/film solution for bottom die and top die attaching. For same-size die stacking, the silicon spacer or tape will be used to separate the bottom and top die. As for the different-size die stacking, normal epoxy paste can be applied, which is same as the

single die attaching process. For the wire bonding process, the combination of normal and reversed bonding will be used for solving wire sweeping issues. Wire sweep, coplanarity, and mold voids were found in the molding process due to high filler loading and viscosity of molding compound material. In other aspects, the warpage issues can cause trouble during the die bonding process due to the thin, large die. The selection of die attach paste is critical because the epoxy bleed out can cover the wire bonding pads and cause the wire bond ability issues and large errors of die placement can lead to electrical failure.

From a thermal management point of view, there are multiple heat sources due to the die stacking architecture. As a result, the thermal problem could be a concern in the vertical stacked die package. Thermal characterization can not be easily defined and measured. Temperature of multi-chip package typically needs to be measured at various power level combinations [7].

The main quality and reliability concerns in stacked die applications at the package level include wire bond failure, die cracking, and delamination [8]-[13]. The contributing factors to each concern are categorized and represented by fishbone diagrams shown in Figure 5 to Figure 7. Causes to each failure mode are grouped into four aspects: design, process, material and environment.

The recognized failure sites and failure modes are sensitive to environmental stresses like high humidity combined with elevated temperature. One needs to pay particular attention

to these issues to develop high quality stacked die packages. The main causes for these failures can be ranked in the order of importance. From the environmental aspect, the combination of humidity and thermal stresses (for example, moisture soaking followed by reflow) is one of the drivers of failure. Material selections of die attach and epoxy molding compound (EMC) materials are very important. The materials with improved flow characteristics, and lower saturated moisture absorption capacity are preferred. From the design aspect, structural characteristics, such as die stacking configuration and bond wire layout, should be optimized. In addition, care should be taken to avoid organic contamination on the bond pads and die surfaces due to multiple die attach curing processes or backside grinding. Appropriate measures, such as aqueous or plasma cleaning, should be used to remove organic residues.

Figure 5 shows contribution factors to wire bond failure. Wire bond failures have two failure modes, open and short circuit. The failure sites cover wire to wire short due to wire sweep, leakage between wire to die, die broken wire, detached wire bond. The contributing factor to die cracking failure is summarized in Figure 6. Die cracking can be induced directly by stresses from wafer fabrication during backside grinding or wafer saw. The crack often initiates at the backside or edge of die in those processes. The environmental conditions, such as moisture levels and temperature, can cause die cracking indirectly. Figure 7 shows the contributing factors for the delamination failure. Delamination can take place at different interfaces, for example, between molding compound and die top (between PI coating and die top or molding compound), between die attach and die, and between EMC and package substrate. Delamination can initiate in

some small cracks in the molding compound or die attach material. The recessed area in die stacking architecture or corners of fillet of die attach layer, where the stresses are concentrated, can also be an initial point of delamination.

2.3. *Board Level Reliability Concerns*

With the advent of fine pitch BGA packages, it has become clear that PCB bending is a critical factor in portable electronic product reliability. The failure sites are in area array solder joints and the failure sites changes under the different bending loads. Several previous studies have discussed the reliability of BGA second level interconnect systems in response to dynamic bending loading, using JEDEC-compliant board-level drop testers [16]-[19], pendulum impact machines [20] [21], vibration shakers [22] and bend testing machines [23]-[29]. External loading factors like maximum applied deflection and excitation frequencies have influence on the fatigue life of interconnect system. It was reported that interconnect fatigue life was strongly degraded by the input deflection level under mechanical bend tests [30].

Researchers have also reported failure site transitions during drop testing of PCBA. Heaslip, et al. [28] observed that failure sites and failure mechanisms changed with drop height and solder type. Varghese, et al. [32] showed that the failure site changed from the solder to the copper trace with an increase of drop height for PCBAs with organic solderability preservative (OSP) metal finish and tin-lead interconnects. Wong, et al. [31] showed that the failure sites and failure mechanisms change with solder and plating type. In an earlier paper [33], the authors demonstrated failure site transition phenomena in

interconnects of two types of plastic BGA (PBGA) packages with changes of PCBA flexural strain or strain rate.

Some publications have reported on failure sites and failure mechanisms in tin-lead solder interconnect systems using gold-over-nickel board and component finishes. Chiu, et al., [34] indicated a very strong correlation between board-level drop reliability and Kirkendall voiding at the intermetallic compound (IMC) interface. A study of brittle interfacial fracture in electroless nickel immersion gold (ENIG) metal finishes with tin-lead solder [35] showed that weak adhesion between Ni_3Sn_4 and $AuSn_4$ IMCs resulted in a greater susceptibility to fracture after aging. The coexistence of these two phases was considered responsible for the deterioration of the solder joint. Some investigators [35] reported a detrimental effect of $AuSn_4$ after aging on the bending strength of BGA assemblies, with breakage energies considerably lower after aging. In another study [37], a ternary intermetallic phase, $Au_{0.5}Ni_{0.5}Sn_4$ was observed to grow at the Ni_3Sn_4 and solder interface upon annealing in systems with electrolytic gold over nickel plating and tin-lead solder. The presence of $Au_{0.5}Ni_{0.5}Sn_4$ was found to decrease the fracture toughness of the joint.

Effects of external loading such as applied deflection, vibration frequency, and displacement waveforms also have a significant influence on the positions of failed solder joints on the BGA package. Due to the difference in bending rigidity of package and test board, joints located at the most outer row will suffer the most deformation applied, while the central joint is in a minimum stressed state. As a result, packages under repetitive

three-point bending normally fail at the outer most rings of joints. Similar phenomenon is also reported in [37][38]. But in the four-point bending test, due to the uniform bending moment formed on the board, the package fails at the outer several columns of the solder joints along the loading bars [30].

The benefits of stacked die packages performance, cost, and time to market far outweigh the challenges associated with the packages design and qualification. Stacked die packages offer a good quality, reliable, and cost-effective solution. A recent market survey has shown that every cell phone and digital camera contains at least one stacked die package [1]. In 2005 stacked die CSP accounted for more than 80 percent of the worldwide handset memory market [15]. With such a proliferation of stacked-chip packages, it makes good engineering and business sense to perform a thorough reliability assessment of stacked die packages as part of the overall design and qualification process.
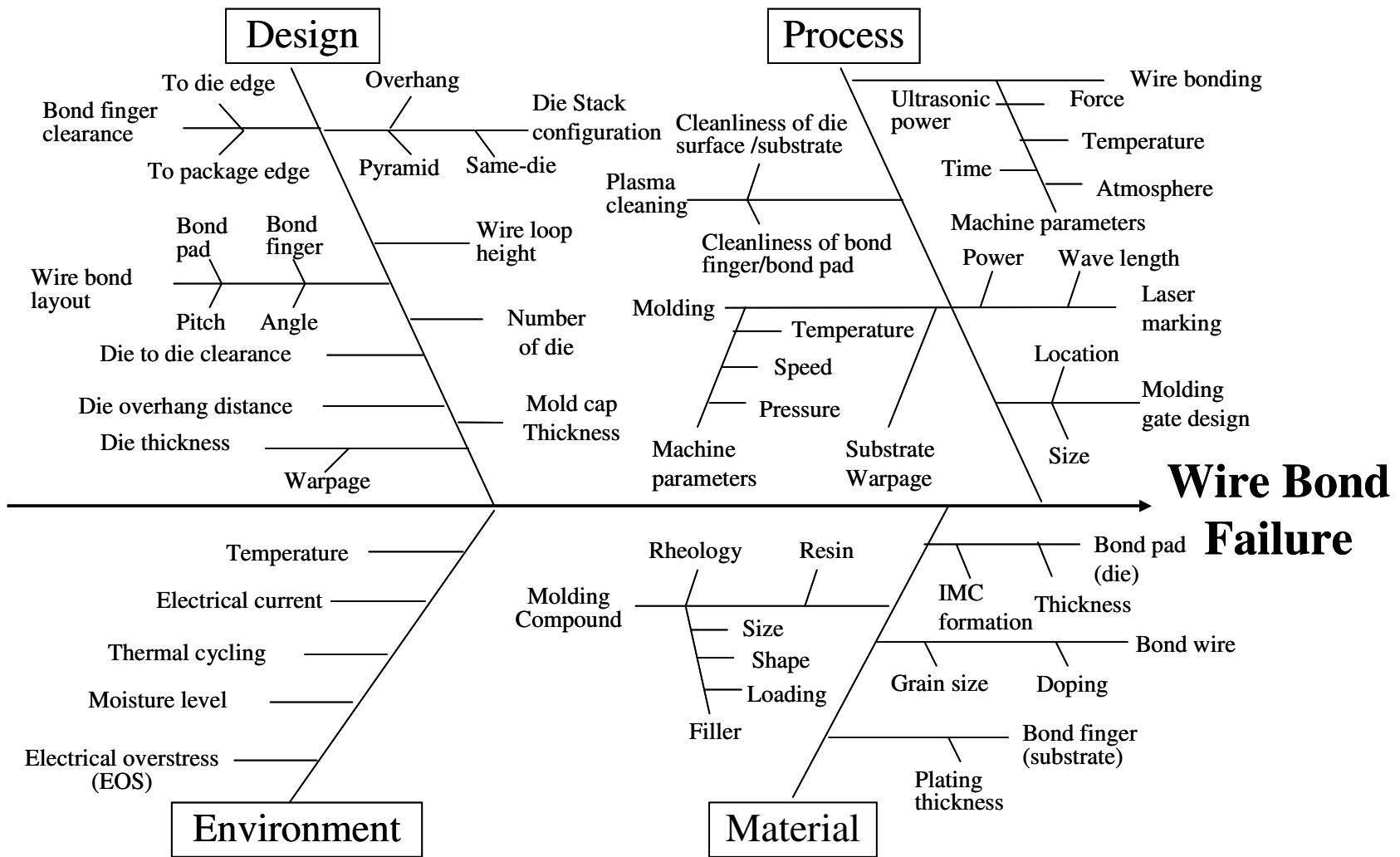
Figure 5: Fishbone diagram showing contributing factors to wire bond open or short
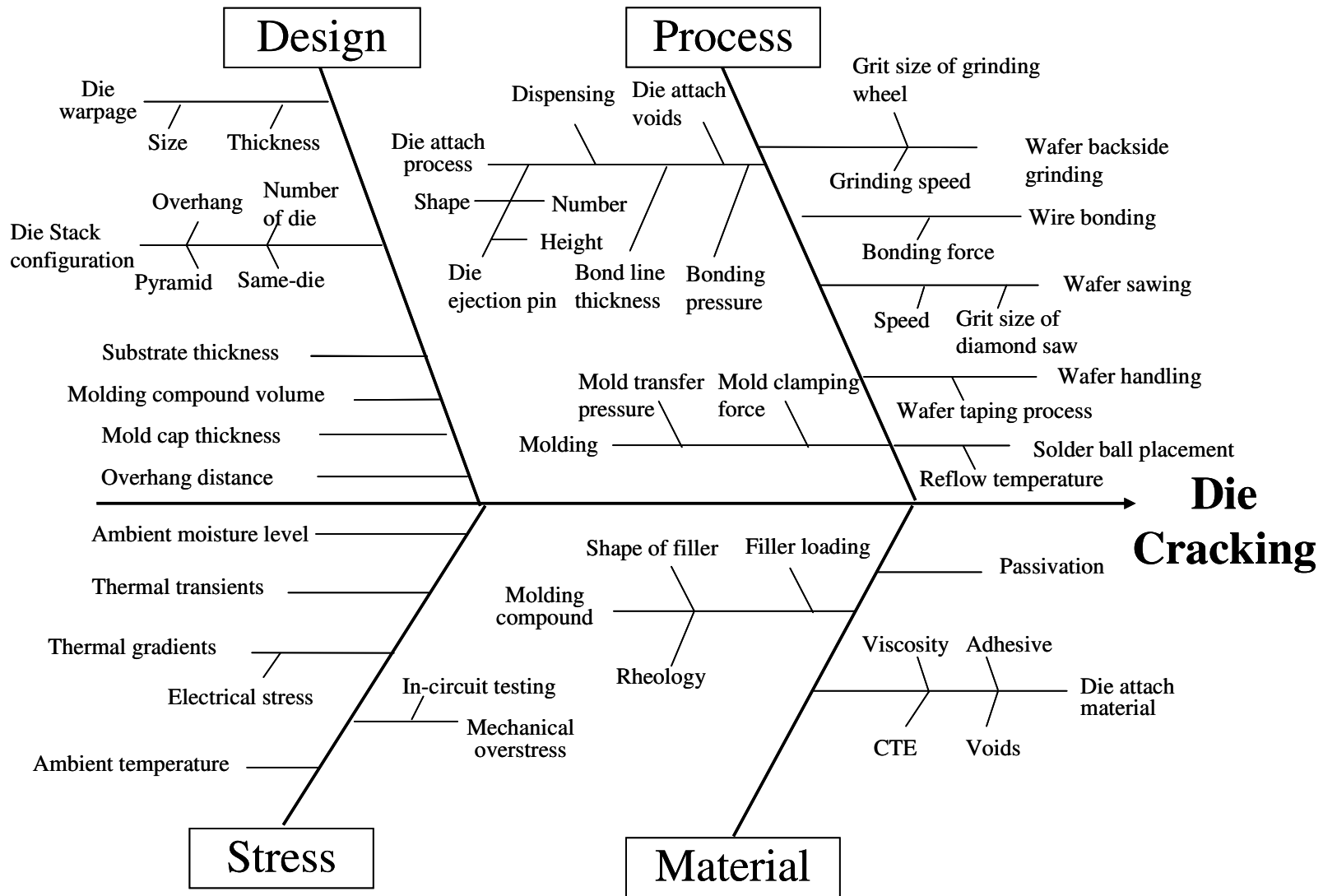
Figure 6: Fishbone diagram showing contributing factors to die cracking
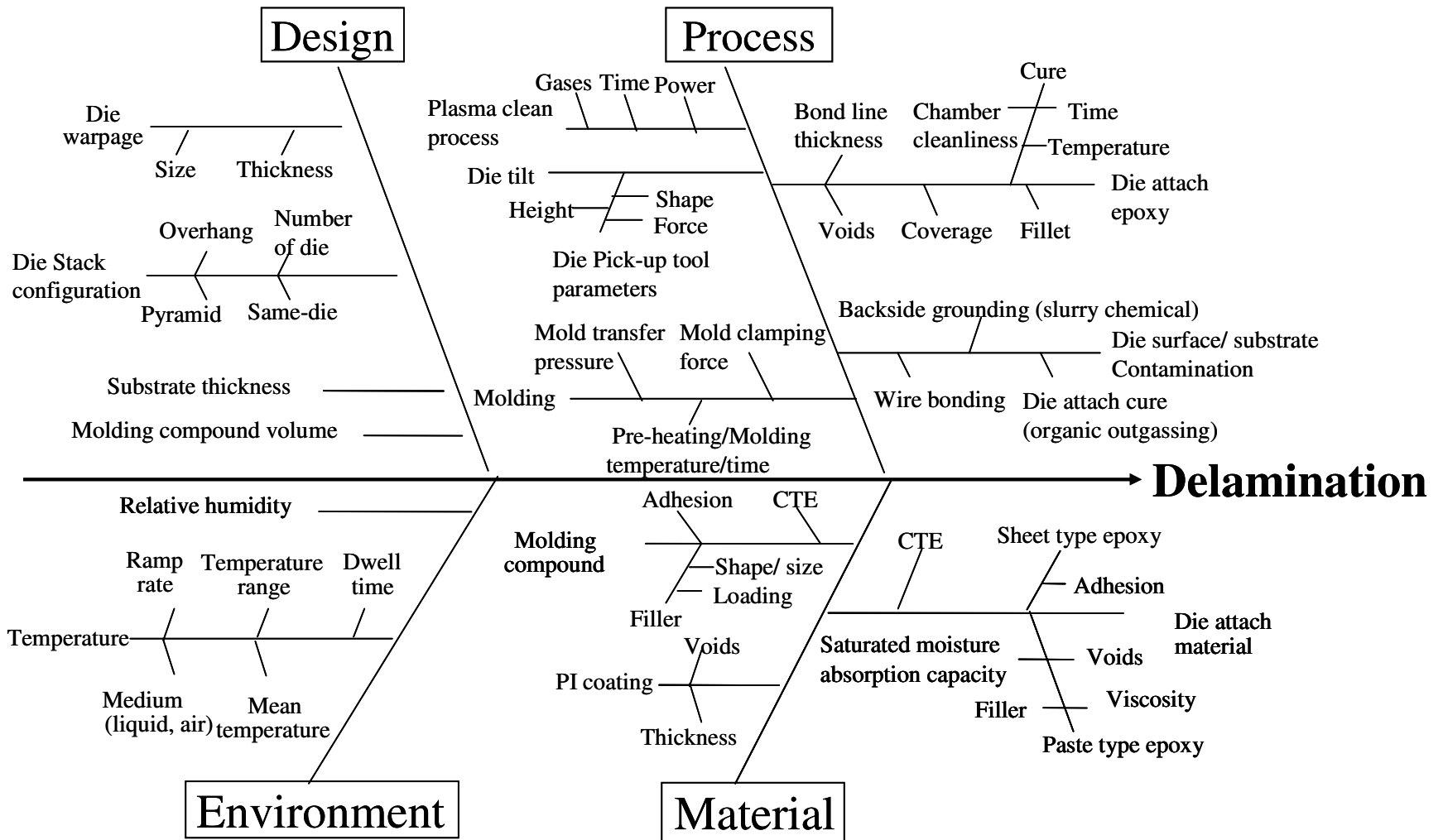
Figure 7: Fishbone diagram showing contributing factors to delamination

3. Chapter Three: Manufacturing Processes

Stacked die package provides more integration flexibility, faster time to market, lower research and development cost, and lower product cost for some application compared with SOC (system on chip).

Low cost higher density substrates and improved materials for encapsulation are needed for stacked die application. High speed simulation tools for electrical & mechanical analysis are highly desired. Lower cost assembly equipment need to be developed.

Because there are many different forms and used for stacked die package, this thesis focuses on various flash memory die as an example to describe the stacked die BGA package manufacturing process.

3.1. *Manufacturing Processes of Stacked Die BGA Packages*

If the size of top die is the same as or larger than the bottom die, an interposer layer can be used to provide enough space for wire bonding. If a dummy silicon die or polymer film is used as an interposer between the dies, delamination, voiding, and die cracking can be induced by the thermal and mechanical stresses concentration in the recessed area [40]. Recently, the stack configuration using filled epoxy die attach adhesive as the interposer has been applied in the mass production. This new approach has two advantages over dummy die interposer: one is the reduction of assembly process because the steps such as dummy die attachment, die attach curing and plasma cleaning are skipped; the other is the reduction of stress concentration due to its configuration.

The flowcharts of two different manufacturing processes of two die stacked BGA package are shown in Figure 8 and Figure 9. Figure 8 illustrates a process flow of stacked die BGA package with dummy die interposer. In this process, the plasma cleaning is involved in the builds of stacked die packages three times. Plasma cleaning can effectively remove organic contaminants to prepare the bonding surfaces. The first two plasma cleaning processes are before the wire bonding to create a clean bond pad for wire bonding. The last one is followed by the molding process. It is used to remove the contamination on the die surface and package substrate, and thus mitigates or eliminates interfacial delamination. The manufacturing process of stack die BGA package with filled paste type epoxy is shown in the Figure 9. The process flow is simpler compared with dummy die interposer configuration because the additional dummy die attachment and curing steps are skipped. The sheet type epoxy die attach can be applied on the backside of the wafer to reduce die warpage.
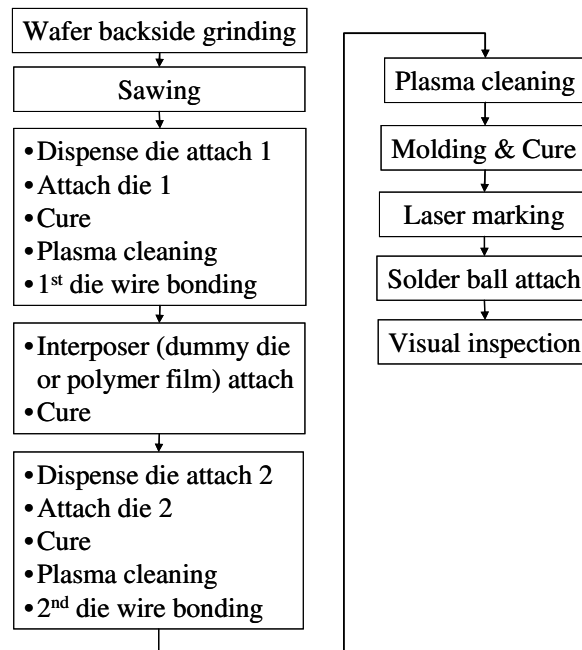
Figure 8: Manufacturing process of stack die BGA package with dummy die interposer
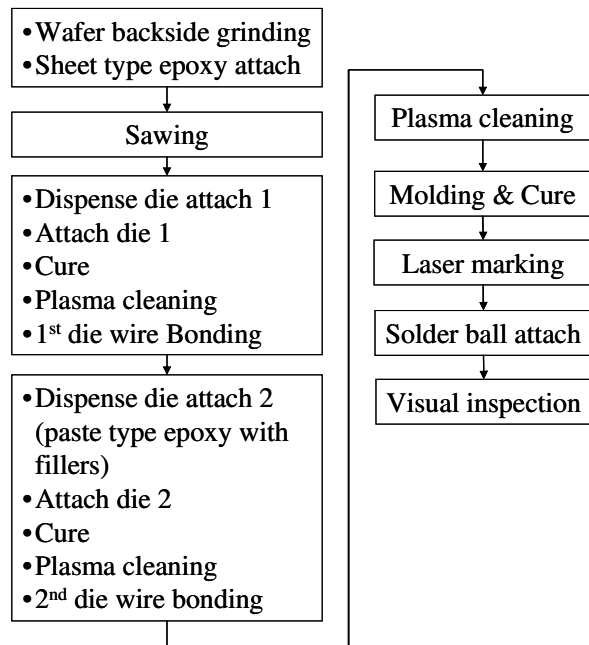
Figure 9: Manufacturing process of stack die BGA package with filled paste type epoxy

The flowcharts show the two die stacked BGA manufacturing processes. Currently, the four die stacked die BGA package are the mainstream in the handheld electronic products. The internal configurations of four die stacked package are shown in Figure 10 and Figure 11 with two different processes.
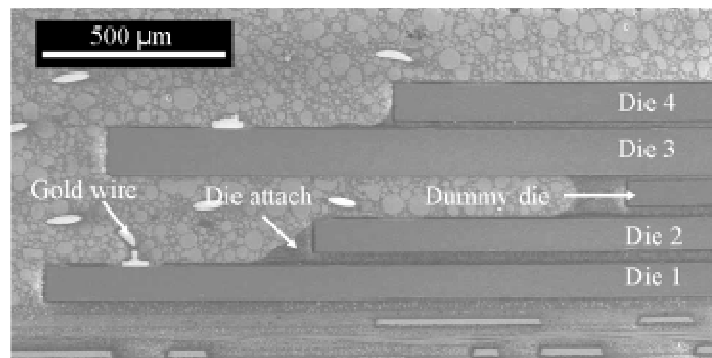
Figure 10: Four die stacked package with dummy die interposer between die 2 and die 3
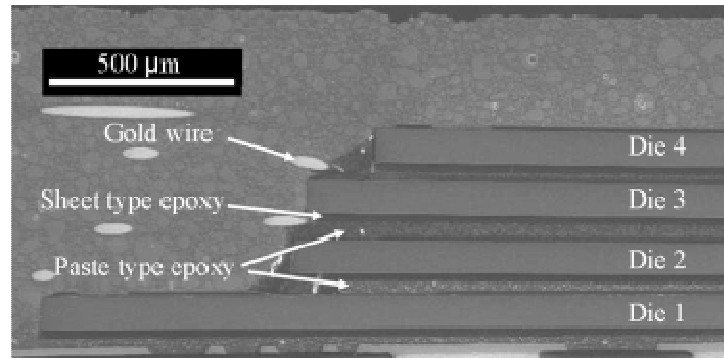
Figure 11: Four die stacked package with filled pasted type epoxy

Failure analysis has shown that the recessed area in the dummy die interposer is the most susceptible area for delamination initiation. In the filled paste type epoxy configuration, the spherical filler particles in the die attach material are able to generate a uniform die attach bonding line due to the consistency in the filler size. By using the spherical particles with the die of standoff between top and bottom die, spacer filled die attach can be used to replace dummy die. For instance, in the same die stack configuration, 10 or 20 μm spherical filler particles can be loaded with 50 to 60 wt% to ensure bond line thickness and minimize die tilt.

The finite element analysis (FEA) results in [10] shows that in dummy die interposer design stresses on molding compound and die attach are very sensitive to die attach coverage in recessed area. The stress increases sharply as die attach coverage increases. With filled paste type epoxy replacing dummy die, FEA showed no effect of die attach coverage on stress in die attach, and assembly steps will be reduced and process tolerances will also be greatly improved.

3.2. *Quality and Reliability Issues Associated with Each Process Step*

3.2.1. Wafer Thinning

A typical wafer is around 850 μm think and can be mounted in a lead frame or on a substrate at that thickness. The driver for wafer thinning, which is sometimes referred to as "backside grinding", is to add more die without increasing the overall package height. The methods of wafer thinning are mechanical grinding, chemical etching, or the new technology-Atmospheric Downstream Plasma (ADP) [9]. Backside grinding is a traditional method of thinning a wafer and has high throughput. Today it has been utilized to work down to a thickness less than 100 μm without etch or plasma.

For the stacked die application, it requires significant thinning of wafer. Normally in a BGA package with the overall height of 1.2 or even 1.0 mm, each die thickness is around 150~175 μm for 2 or 3 die stack, while the die thickness should be further reduced to 75~100 μm for 4 to 7 die stacking application. Today the primary formats are 3 and 4 wire bonded stacks although stacks of 6, 7, and more are in development or low volume production.

The main quality issue in wafer thinning is the deep wheel mark from mechanical backside grinding with diamond wheel. The wheel mark can vary from 0.1 to 2 μm in depth according to the different grinding condition and diamond wheel quality. Especially, if die is as thin as 75 μm with the deep wheel mark on backside surface, it tends to break or crack in the following die attachment, wire bonding and molding processes. To prevent the wheel mark, a fine polishing step can be used in wafer backside

grinding process by using slurry-chemical typical with a maximum roughness under 50 nm.

3.2.2. Die Attaching

The manufacturing process in Figure 9 reveals that the cure step has to be repeated after each die attachment including the dummy die. Recent years, in order to reduce the process steps and reliability issues induced by dummy space die, direct die attach with paste type epoxy method has been introduced to provide space for wire bonding. By adapting this new technique, more die can be added in a stacked die package [10].

Die attachment using paste type epoxy is a traditional method for die-to-die or die-to-substrate bonding. However, for multi-die stack application, either the die or the package substrate is inclined to have a warpage due to the thin thickness. So, epoxy voids and incomplete coverage can occur during die attachment. The selection of die attach material becomes a critical issue to ensure a good quality and reliability. Most recently, wafer with adhesive tape on the backside using direct attaching method has been developed and applied. The sheet type die attach adhesive incorporates the function of wafer dicing tape. Wafers with the adhesive tape on the back are diced, picked and attached to a substrate or on the top of the another die with the paste type die attach epoxy.

Bond line thickness voids and coverage of paste type epoxy should be strictly controlled to prevent delamination in the interfaces and voiding in the die attach layer. Stacked die package is weaker than the single die package in moisture resistance because the reduction of the volume of molding compound. For instance, in a four die stacked

package the volume of the molding compound is about 50 percent of that of the mold, while in a single die package, the percentage is 75%.

Figure 12 shows some failure sites after preconditioning test in a four die stacked package with filled paste type epoxy die attach. Delamination and voids in the die attach material can propagate to induce die cracking and swelling of the epoxy, which can become sources of electrical function failure like open or short circuit during reliability tests such as preconditioning, temperature cycle, and autoclave test. To prevent moisture absorption from environment, die attach and EMC material with high filler content and lower moisture absorption capacity should be developed. The crack of die in Figure 12 starts from the backside of the die close to the corner of die attach fillet. If the crack reaches the metallization, electric failure can be induced. Figure 12 emphasis the importance of material selection of die attach and EMC.
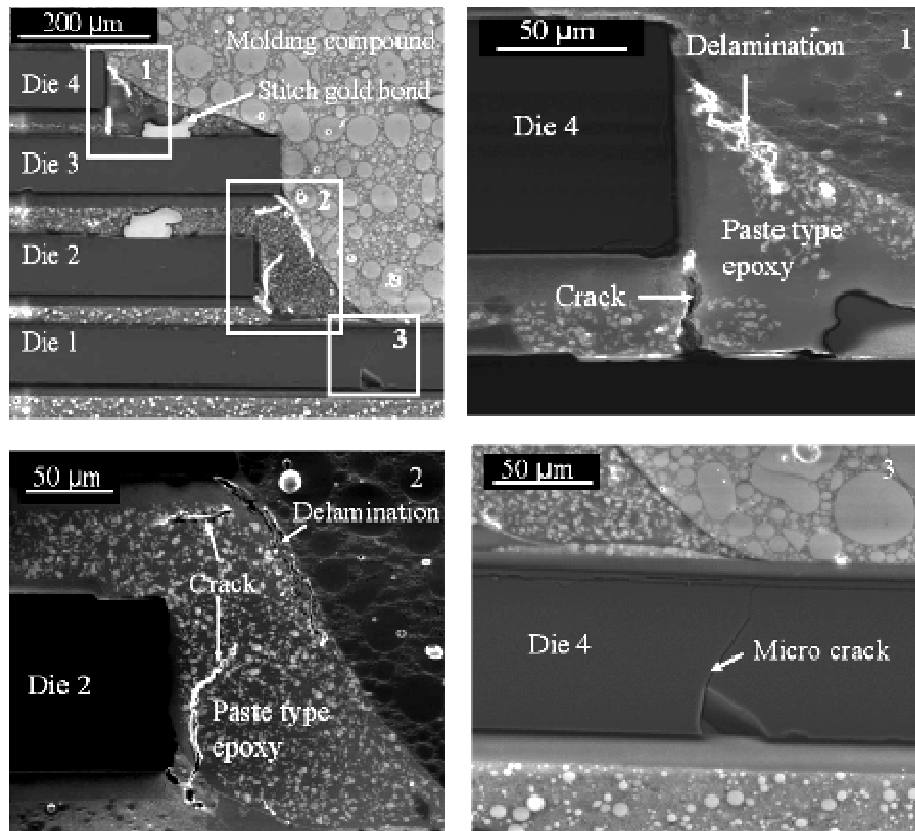
Figure 12: Failure sites in a four die stacked package after preconditioning test at 30 °C/60 RH for 168 hrs (SEM micrographs)

3.2.3. Wire Bonding

The challenges in the bonding technologies include low loop requirements, clearance considerations between the layers of the wire loops to avoid shorting and cross talk, and straightness requirements to avoid wire sweep to ensure good yield. Several wire bonding methods with low loop profile have been in development to meet the above requirements. Low loop requirement is one of the most critical challenges to ensure the high quality and reliability. The looped wire of the top die can be exposed outside the epoxy molding compound (EMC) without decreasing the loop height due to the small clearance between die top and mold. A short between the wire loop and the adjacent dies can also be induced by a high loop height.

The height requirement of low profile looping is to be less than 70 μm, which has propelled the growth of ultra low loop normal bonding and reverse ball bonding [11]. An ultra low loop forward (normal) ball bonding process places a ball bond on the die first, performs the looping motions to the substrate and places a stitch bond on the bond finger of the substrate (see Figure 13). The loop height can be obtained to be less than 70 μm using this technique. A reverse (bump) ball bonding process places a bump on the die pad first. After the bump is formed, a ball bond is placed on the substrate and the stitch bond is placed on the bump (see Figure 14). This bonding process can form a bonding height to be less than 50 μm.
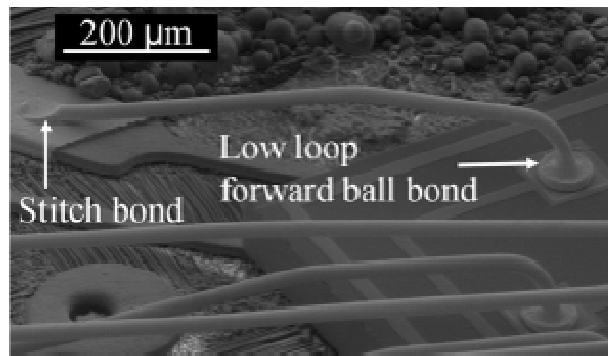
Figure 13: Low loop forward ball bonding (decapsulated package)
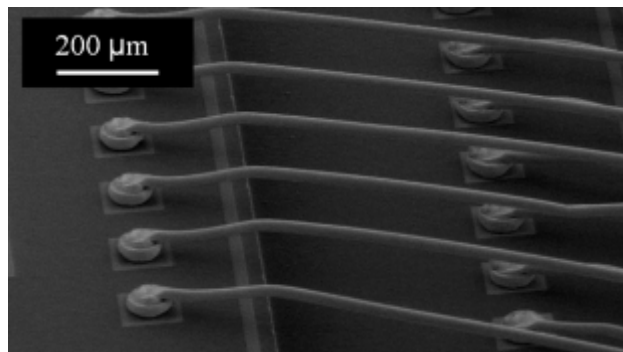
Figure 14: Reverse ball bonding (decapsulated package)

Normally, productivity of the normal bonding is 1.2~1.5 times of that of reverse bonding. Low profile normal bonding is more capable of fine pitch application than reverse

bonding. However, it has a loop height constraint due to the neck area above the ball. Excessive bending above the ball for a lower loop can cause broken neck or cracks due to the larger Au grain size formed during electronic flame off (EFO) heating. To prevent the wire sweep, some dopant as Pd, Si, Cu are added in Au wire to increase the hardness of the wire, but the Au wire with higher hardness has the potential to break. Reverse wire bonding can form lower loop height, but it tends to have the wire sweep issue during the molding process.
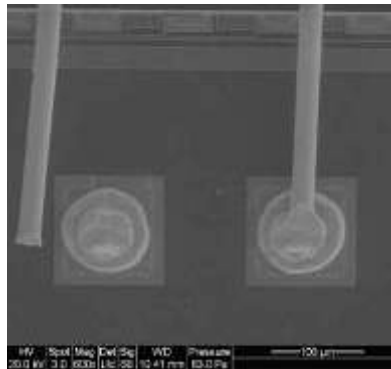
Figure 15: Fractured wire at the neck of reverse bond

One of the important quality issues during the reverse bonding for a low loop profile is the poor adhesion between Au bump and bond figure on the substrate. When a ball bond is placed on the bond figure of the substrate, good adhesion is needed between Au bump and 0.5~1 μm thick Au plating on bond finger. The key factors for a good adhesion include bonding force by capillary, substrate heating temperature and cleanness of bond pad. In stack die packages, the substrate should be heated up to 150~180°C. Plasma cleaning before wire bonding process is required to remove the organic contaminations deposited on the bonding finger during the die attach cure process. Figure 16 shows the

delamination between Au bump and Au plating after unbiased autoclave test at 121℃/100% RH, 2 atm for 96 hrs.
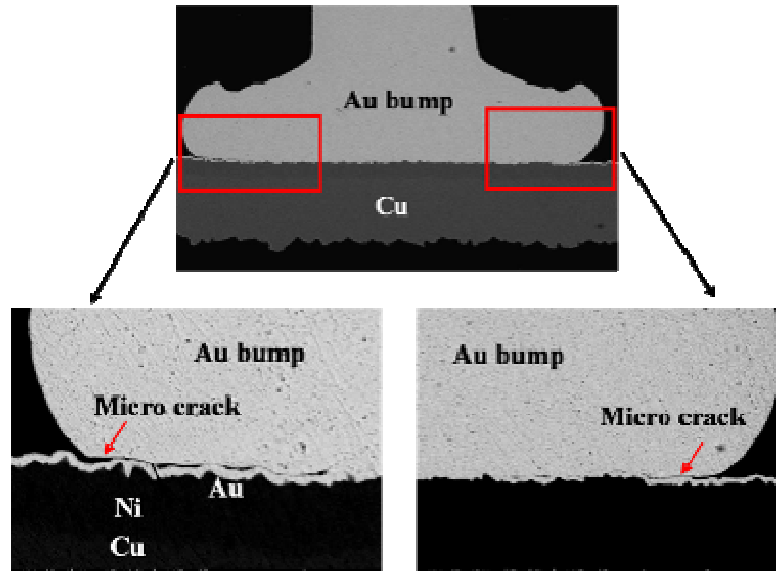
Figure 16: Delamination between Au bump and Au plating after unbiased autoclave test at 121℃/100% RH, 205kPa for 96 hours

3.2.4. Molding

The molding process in stacked die package is more difficult than a single die package due to the increase of die quantity, wire loop density and wire length. The complexity of the configuration decreases the flow ability and molding ability of EMC, and thus increases possibility of wire sweep. Empirically, an ultra low loop normal bonding can reduce wire sweep due to the lower flow resistance compared with the reverse bonding.
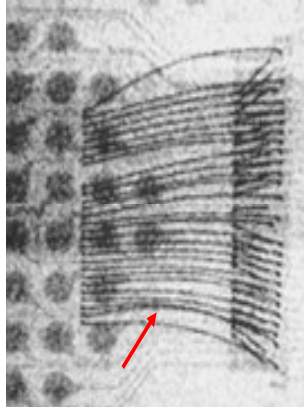
Figure 17: X-ray image of wire sweeping during molding in a stacked die package

Incomplete molding and micro–voids are the main quality issues due to the unbalanced flow of EMC. If four dies of 100 μm thick are stacked, the stacking height should be around 0.6~0.7 mm including bondline thickness. There is not enough space for the wire loop on the top die, and the clearance will be less than 0.2 mm in 0.8 mm thick mold body. So, the wire of the top die can be damaged by top cavity of molding cap easily. In the case that the substrate has a warpage due to the thin thickness and the molding compound does not have good flow ability, Au wire exposure or EMC voids on the top of molding cap may occur by incomplete molding. To achieve high quality and reliability in stacked die application, high flow ability molding compound with fine filler development is required. In addition, the parameters of molding machine and bond wire layout should be optimized to reduce the wire short issue.

4. Chapter Four: Mechanical Bending Tests

Four die stacked BGA package with a dummy die spacer assembled on the PCB was selected as the test specimen. The specimen response under dynamic loading conditions has been quantified in terms of the PCB flexural strain and strain rate. For both as-reflowed and aged specimens, experimental data from cyclic bending tests has been combined with the data from impact tests to obtain the relationship between cycles to failure and strain rate over nearly four orders of magnitude in the strain rate. For both as-reflowed and aged specimens, experimental data from cyclic bending tests at three strain amplitudes with a constant strain rate ($1x10^{-3}$ sec^{-1}) has been used to obtain the relationship between cycles to failure and strain amplitude. In addition, the failure sites associated with each test condition are identified and a failure site transition phenomenon is reported in this work.

4.1. *Test Specimens*

The stacked die BGA package in this study was a stack of four dies with a dummy die spacer in the center to provide more space for wirebonding, as shown in Figure 18. The thickness of each die was approximately 100 microns. Each package had 167 I/Os, using a full grid of twelve by fourteen solder balls, with the exception of one corner solder ball. After reflow, solder balls were 0.44 mm in diameter, and the ball pitch was 0.8 mm. The pad finish on the package side of the eutectic tin-lead solder balls was electrolytic gold over nickel plating, and the PCB metal pad finish system was ENIG plating. The land pattern on the package side was solder mask defined (SMD), while on the FR-4 board

side it was non-solder mask defined (NSMD). For the SMD land pattern, the solder mask openings were smaller than the metal pads.
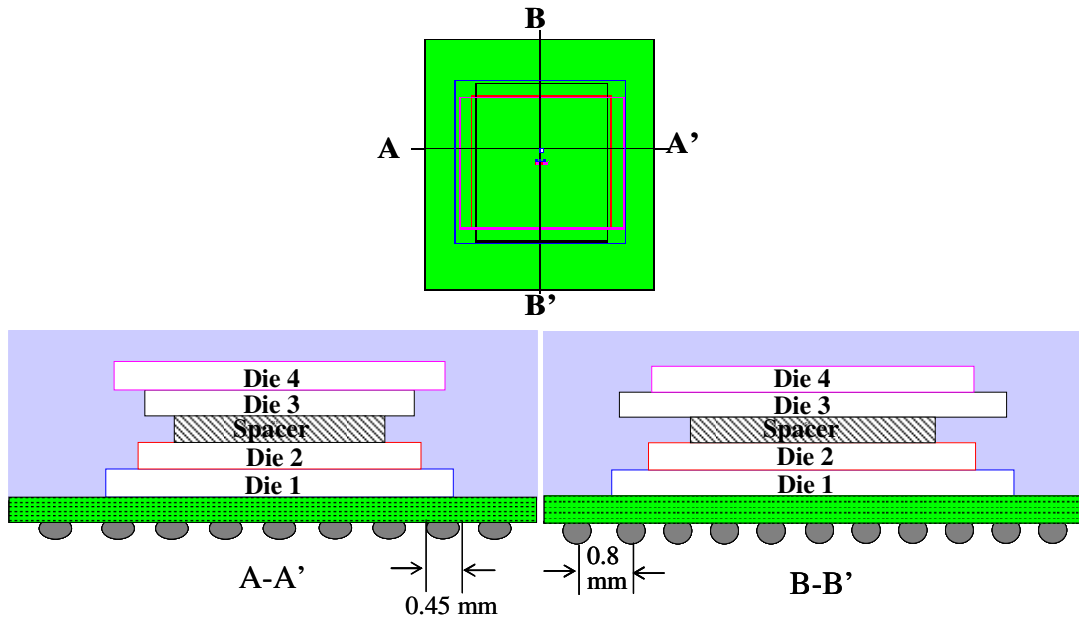
Figure 18: Schematic drawing of internal configuration of test specimens

There were two types of test boards used in this study, one for low strain rate cyclic bending tests and the other for impact tests. The cyclic bending test board, shown in Figure 19, was a 200 x 55 x 1.5 mm FR-4 board assembled with four daisy-chained stacked die BGA packages on one side. The impact test board was a 75 x 40 x 1.5mm FR-4 board with one package in the center. On both types of board, each package had two daisy chains: one was primarily between the die and the substrate (including some solder joints), and the other was between the substrate and the solder balls. Test specimens were either used without aging ("as-reflowed specimens") or subjected to aging at 135ºC for between 168 hours and 200 hours ("aged specimens").
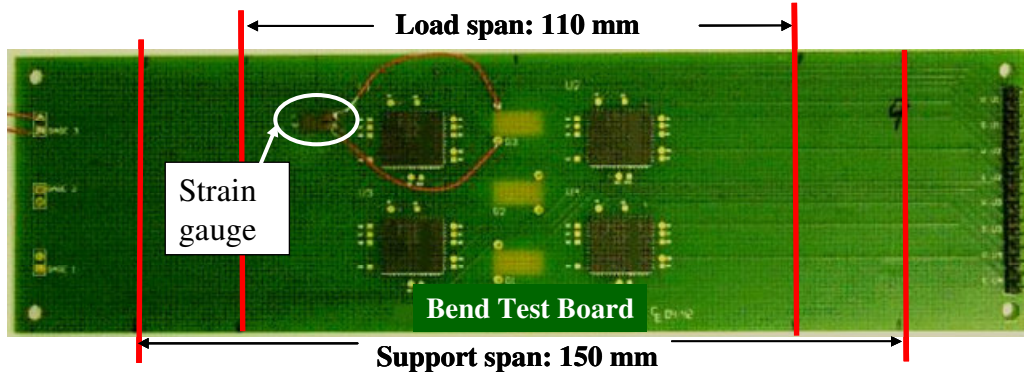
Figure 19: Cyclic bending test board with four packages on one side
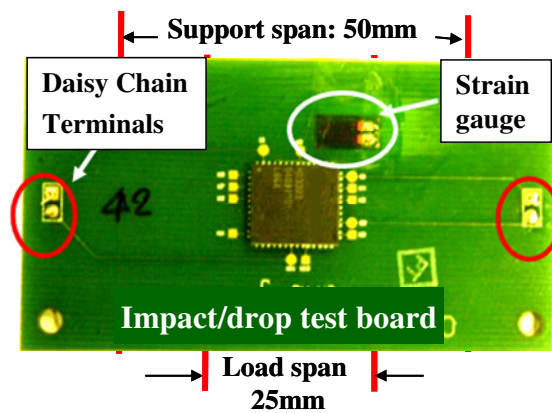
Figure 20: Impact test board with one package at center

4.2. *Construction Analysis of Test Specimens*

Construction analysis was conducted on both as-reflowed and aged specimens in order to obtain the critical dimensions of test specimen before testing. Figure 21 and Figure 22 show cross-sectioning images of the die stacking configuration and solder joint (second level interconnect) of an as-reflowed test specimen using scanning electronic microscopy (SEM). The critical dimensions of the tested stacked die package are listed in Table 2.
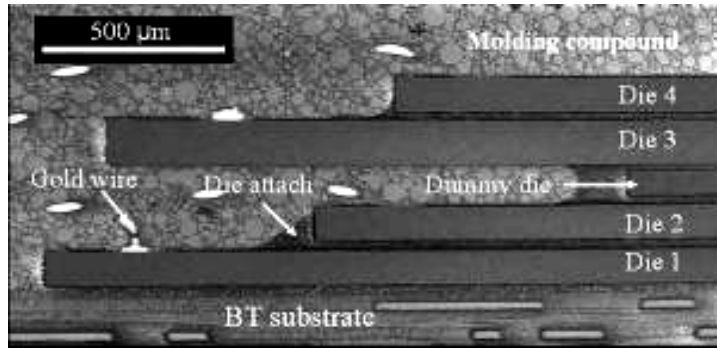
Figure 21: Four die stacked BGA package with a dummy die as spacer (SEM micrograph)
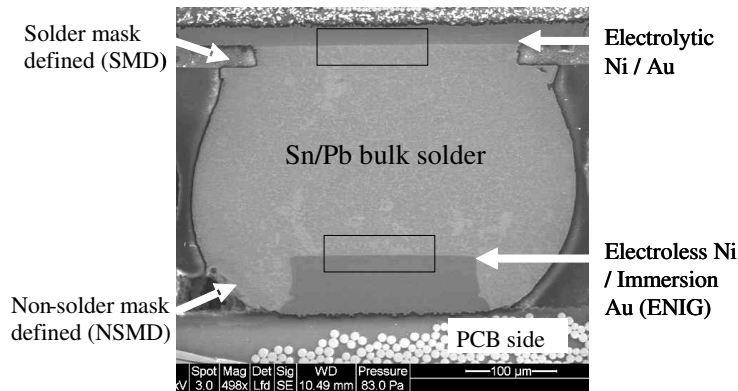
Figure 22: Solder joint configuration (Details in the boxes will be shown in the figure 21)

Table 2: Critical dimensions of the test specimen

Package	Dimensions (mm) Thickness x Length x Width
Substrate (4-layer BT)	0.36 x 10.80 x 12.07
Aspect ratio	1.0 : 1.1
Die 1 die attach	0.038
Die 1	0.095 x 8.13 x 8.13
Die 2 die attach	0.031
Die 2	0.090 x 6.60 x 6.60
Dummy die attach	0.031
Dummy die	0.065 x 5.38 x 5.38
Die 3 die attach	0.031
Die 3	0.115 x 6.27 x 7.95
Die 4 die attach	0.031
Die 4	0.090 x 8.13 x 6.30
Die overhang	1.285
Mold cap	0.86
Au wire diameter	0.025
Wire bond pad pitch	0.100 and 0.203
Ball pitch	0.8
Overall height	<1.6

After isothermal aging, there was a significant IMC layer growth on the solder/pad interface in the aged specimens on both component and PCB sides. The IMC growth between the metal pad and the bulk solder on both the PCB and the package sides of the solder joints is illustrated in Figure 23. As shown in Table 3, the thickness of the IMC layer was in the range of 2 to 3 microns for the aged specimens, but less than 0.3 micron for the as-reflowed specimens.
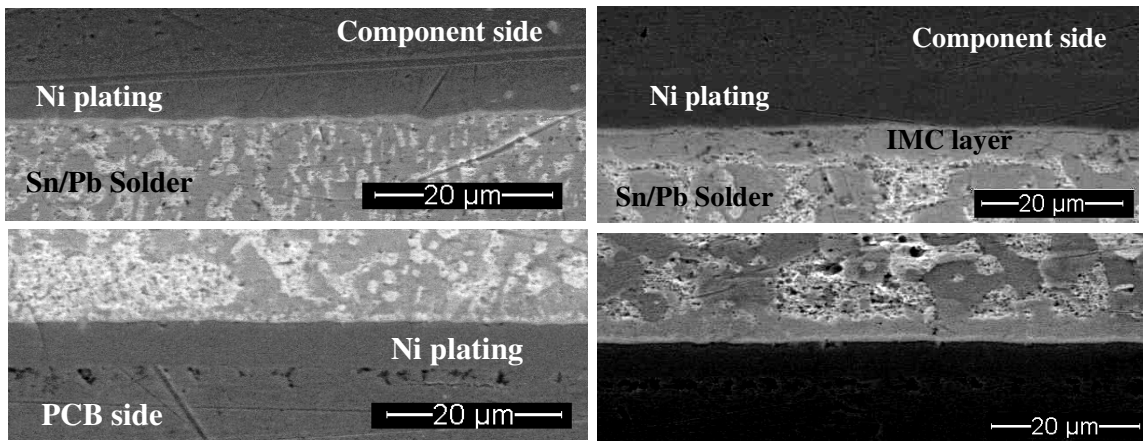
Figure 23: Construction analysis at interfaces in the eutectic Sn/Pb solder joints with gold over nickel plating: as-reflowed specimen (on the left) and aged specimen (on the right)

Table 3: IMC layer thickness

Specimen		IMC (micron)
As-reflowed	Package side	<0.3
	Board side	Not detectable
Aged	Package side	3.0
	Board side	2.8

Some defects were found on the as-received aged specimen, including voids in the solder joint, delamination between eutectic Sn/Pb solder and copper pad. The voids might take place during the reflow of the solder joint placement. Since the size of the voids is less than 25% of cross-sectioning area, thus it should not have big influence on the fatigue life of test specimen during the mechanical testing. The delamination in the solder joint was

due to the poor adhesion between solder and Ni plating, which might be caused by the contamination on the surface of Ni plating. This defect might appear before the isothermal aging process due to the pick-up force. The delamination can initiate the crack and reduce the fatigue life of test board under mechanical loading conditions. These defects can not be examined during electrical testing; however, it can lead to a big deviation of the fatigue life of test boards.
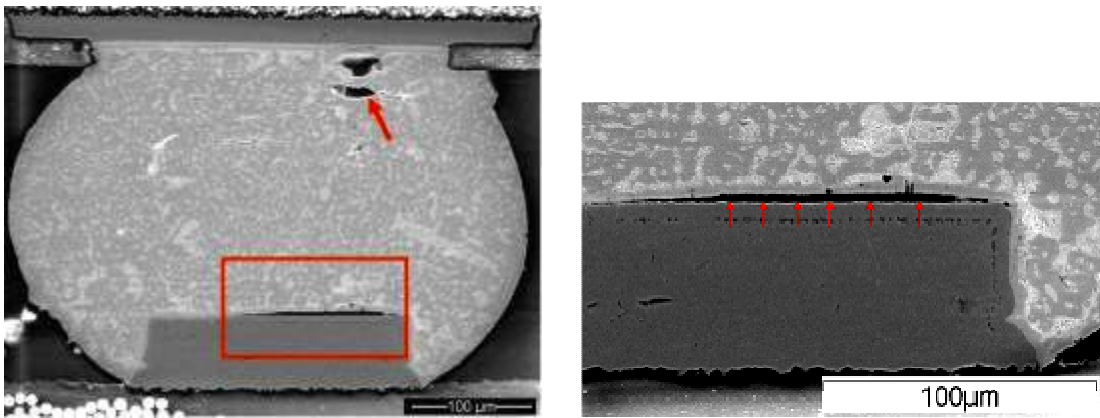
Figure 24: Defects in the solder joint of an as-received aged specimen and the close-up image in the box (SEM micrograph)

4.3. *Instrumentation*

4.3.1.   PCB Flexural Stain Monitoring

The strain gauges used in this project is uniaxial gauges with a resistance of 350 ohm, manufactured by Vishay. Figure 25 illustrates the schematic diagram of the strain gauge used in this work. The strain gauges were attached on the package side of the PCB near the corner of package to measure the uniform PCB strain. The resistance change of the strain gauge was inputted to a strain gauge signal conditioner, which provides a conditioned, amplified analog voltage output for strain gauge based sensors. A data logger with a sampling rate of 200~300 data/sec per channel was used to collect the data

from the strain gauge conditions. The data was recorded and post-processed by LabVIEW (short for Laboratory Virtual Instrumentation Engineering Workbench) which is a platform and commonly used for data acquisition. The average PCB strain rate is calculated based on the change in strain divided by the time interval during which this change is measured.
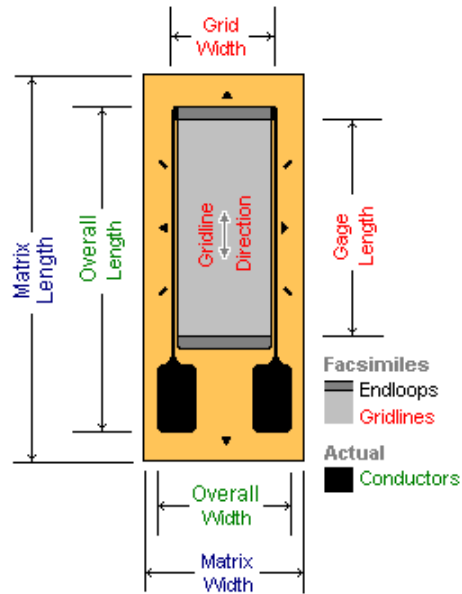
Figure 25: Schematic diagram of strain gauge

4.3.2. Daisy Chain Resistance Monitoring

There are two daisy chains on each package: one including die, substrate, and solder balls, and the other only between substrate and solder balls. The top view of the daisy chain configuration on the board side is shown in Figure 26. Failure of a test package was defined as an increase of 1000 ohms in the resistance of either of the two daisy chains. Under the dynamic bending loads, even though the test specimens had failed, as the curvature test board of decreased, the daisy chain recovered itself, which was followed by a decrease of resistance. Due to the transient nature of the test, a high-speed data acquisition system was used for in-situ resistance monitoring. The sampling rate during

the testing varies from 100 to 2500 data/sec per channel based on time per cycle in the four-point cyclic bend test. Shorter cycle time, higher sampling rate is needed to get good resolution of the daisy chain resistance change.
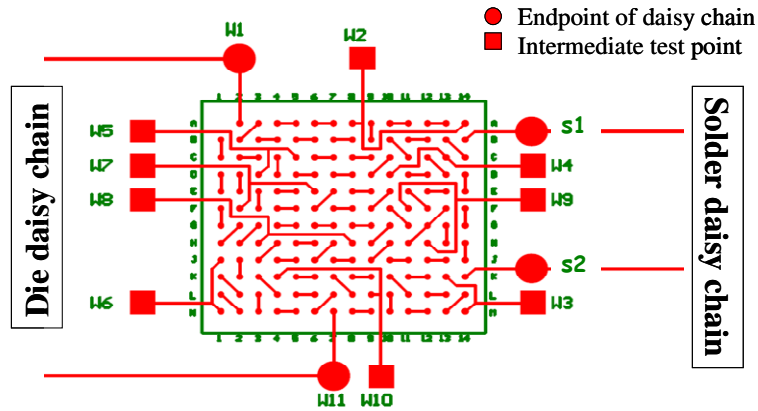
Figure 26: Top view of the daisy chain configuration on the board side

The resistance monitoring system consisted of a Wheatstone bridge, with the daisy chain resistance forming a quarter of the bridge circuit (see Figure 27). The bridge was balanced in the unloaded state and its sensitivity was determined by the values of the resistance of the other three bridges.

E: Input voltage
e_0: Output voltage
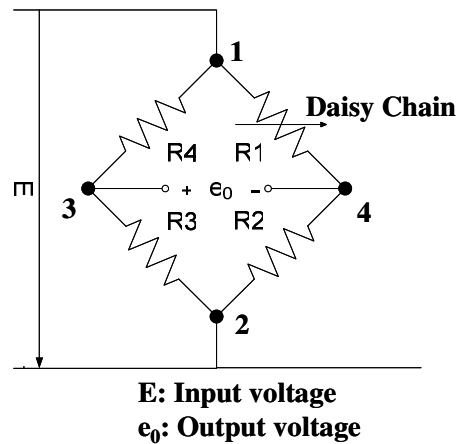
Figure 27: Wheatstone bridge with the daisy chain forming a quarter of the bridge circuit

The instrumentation used for this test is represented by the flowchart shown in Figure 28. In Figure 28, it shows two loops: one is for strain monitoring indicated by the dashed lines, and the other is for resistance monitoring indicated by solid lines.
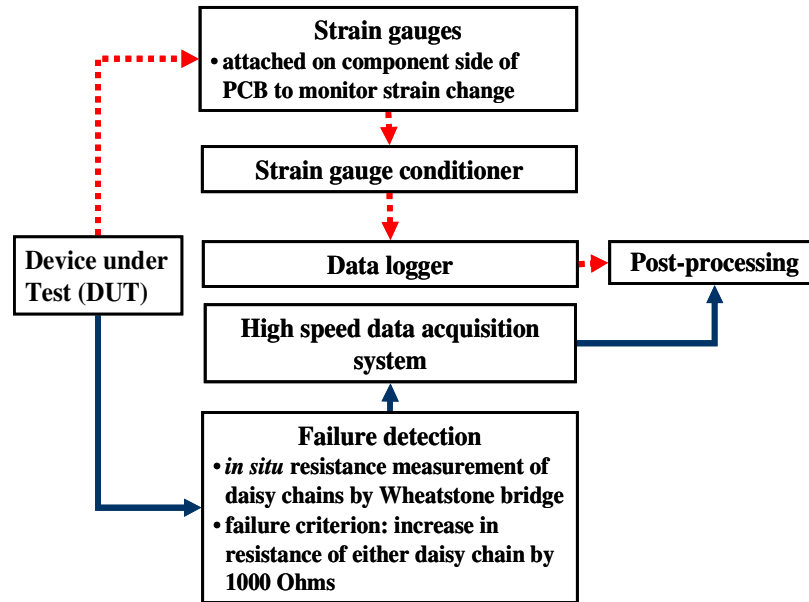
Figure 28: Instrumentation

4.3.3. Apparatus

Four-point bending tests were conducted on the specimens to induce a uniform bending moment across the load span. A commercially available servo-hydraulic bending test machine (see Figure 29) was used for the low strain rate cyclic bending tests (below 0.1 sec^{-1}). For specimens tested with this apparatus, the support span was fixed at 150 mm and the load span was 110 mm. The crosshead travel distance can be varied from 0 mm to 100 mm and crosshead speed can be varied from 0 mm per second to 12.5 mm/second.
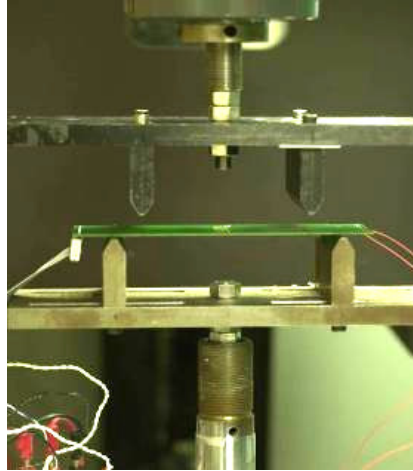
Figure 29: Four-point bend test fixture on servo-hydraulic mechanical tester

The crosshead travel distance and crosshead speed of a universal tester are approximately proportional to the test board assembly strain and strain-rate, respectively. The relationship between these variables can be determined empirically by testing a mechanically representative package/board assembly (set-up test board); however, these relationships may prove non-constant or non-determinant, depending on universal tester capability and board/ package configuration. In this work, the PCB response was recorded by the in situ strain gauge monitoring.

In this test, simplified analytical relationships for 4-point bending shown in (a) and (b) have been used for estimating the global PCB strain and strain rate, as suggested in IPC-9702 [43]. These equations are derived from classic beam theory and ignore any effects due to the package, or to the Poisson's ratio effect of a plate in bending.

$$\delta = \frac{\varepsilon(L_s - L_L)(L_s + 2L_L)}{6t} \tag{a}$$

$$\dot{\delta} = \frac{\dot{\varepsilon}(L_s - L_L)(L_s + 2L_L)}{6t}$$
(b)

where,

- ε is the global strain along the length of the board,

- δ is the relative displacement between the load bars and the support bars,

- t is the PCB thickness,

- L_L is the load span,

- L_S is the support span.

The deviations between the calculated value and measured value (from strain gage measurement) are within 40% for strain and within 10% for strain rate. It indicates that the stiffness of the package can not be ignored in our test specimens. However, these equations are helpful in the initial selection settings of tester.

The drop tower is used to drop steel balls on the fixture holding the specimen to conduct higher speed four-point bending tests compared with cyclic bend tests (see Figure 30). For specimens used for these impact tests, the support span was 50 mm, and load span was 25 mm and the BGA package was located on the underside of the PCB.

The mass of the ball can be varied from 65 grams to 450 grams and the impact velocity can be varied from 0 to 6 m/sec by changing the ball drop height. The drop tower is six feet tall, which is designed and fabricated in-house. The specimen is supported in a 4-point bend configuration. The rigid base and the crossbar are made of aluminum. The guide rods, made of hardened steel, are aligned parallel to each other and perpendicular to

the base. Both guide rods are torqued to increase its natural frequency and thus decrease vibration during testing. A four point bend is achieved without any contact damage to the specimen. The flexural mass is kept light by using aluminum linear bushings to reduce the quasi-static load on the specimen. The flexural masses are made of delrin to damp out the high frequency ringing during impact. Details of the test setup and instrumentation can be found in [32] and [33].
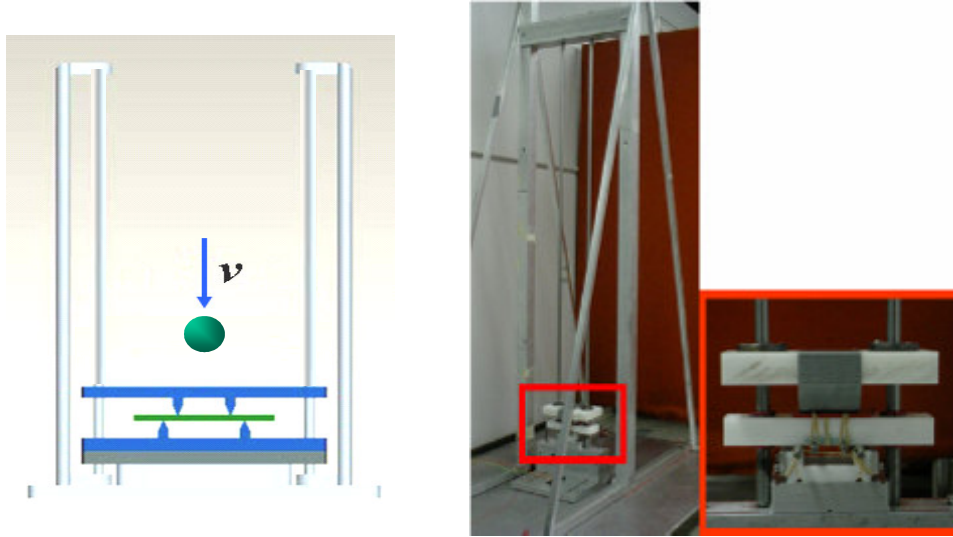
Figure 30: Schematic diagram of drop tower: (left), picture of drop tower with mass (right)

4.4. *Experimental Procedure*

In this study, both the strain and strain rate effects were examined. The experimental work was conducted in three steps. In a preliminary step, overstress tests were conducted to determine the failure strain ($\varepsilon_{failure}$) of the stacked die packages. The average failure strain obtained from this step was used to determine the peak strain for the cyclic four-point bending tests. In the cyclic bending tests, the effects of strain on the fatigue life (number of cycles to failure) were examined using different peak strain levels (25%, 50% and 75% of $\varepsilon_{failure}$) for a strain rate of 1.0×10^{-3} sec^{-1}. The effects of strain rate were also

examined from 3×10^{-4} to 2 sec^{-1} at a peak strain amplitude of 50% of $\varepsilon_{failure}$. There were four BGA packages assembled onto each board, with two daisy chains for each package. The cyclic bending tests were continued until all eight daisy chains failed. For each package, the failure strain was recorded as the strain at which the first of the two daisy chains failed. In the last step, a high-speed bending test (impact test) was conducted to span the strain rate from quasi-static to intermediate magnitudes. The parameters measured in each step are listed in Table 4.

Table 4: Parameters measured in each step

Overstress Test	• To determine the overstress strain limit ($\varepsilon_{failure}$) for as-reflowed and aged specimens • To select the peak strains for the cyclic bend tests
Cyclic Bend Test	• To examine the strain effect on the durability (cycles to failure) using different strain levels (25%, 50% and 75% of $\varepsilon_{failure}$) at the same strain rate • To examine the strain rate ($d\varepsilon/dt$) effect on the durability by changing the strain rate under the same peak strain
Impact Test	• To examine the durability of the specimens under strain rates ($d\varepsilon/dt$) higher than cyclic bend tests.

All specimens were monitored in real-time for continuity, while the test was being conducted, using a high-speed data acquisition system. Failure of a test package was defined as an increase of 1000 ohms in the resistance of either of the two daisy chains. In addition, each test board was instrumented with a strain gauge, to monitor the severity of the PWB flexural strain and strain rate.

4.5. *Test Results*

The overstress limits of the test specimens were obtained for four point bend tests conducted using a monotonically increasing strain. During the tests all daisy chains on

the test specimens failed as the strain was ramped up. Figure 31 is a sample plot of the overstress test on an aged specimen. In this figure, the heavy solid line represents PCB strain, and the horizontal dashed line is the failure threshold. The overstress limit was calculated as the average failure strain of all four packages on a bend test board. At the fixed strain rate of $1x10^{-3}$ sec^{-1}, the overstress limit of the aged specimens was approximately 3.6 millistrain. The overstress limit of the as-reflowed specimens was nearly twice that of the aged specimens, or about 6.8 millistrain.
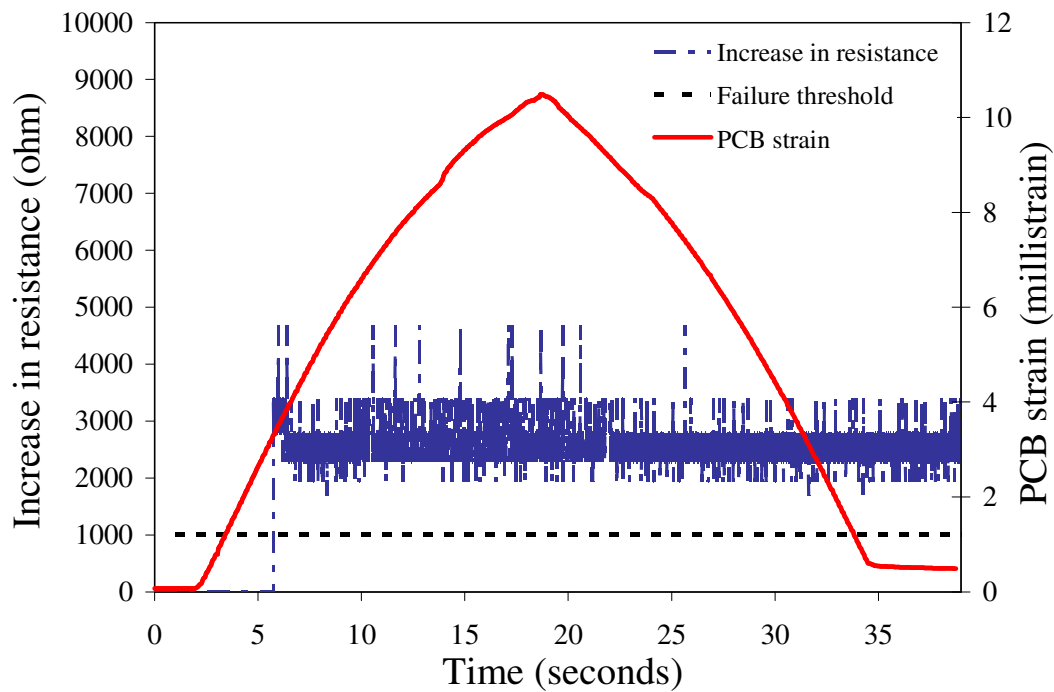
Figure 31: Sample plot of PCB strain and increase in resistance of solder daisy chain during an overstress test on an aged specimen (at a strain rate of $1x10^{-3}$ sec^{-1})

Figure 32 is a sample plot of the solder daisy chain resistance during a portion of a cyclic bend test on an aged specimen at a strain rate of $1x10^{-3}$ sec^{-1}. The resistance of the daisy chain (dashed line) changed following the periodicity of the cyclic strain curve (solid line), and this has been expressed in terms of the number of cycles. For the specimen shown in the figure, we can see it failed during cycle 177.
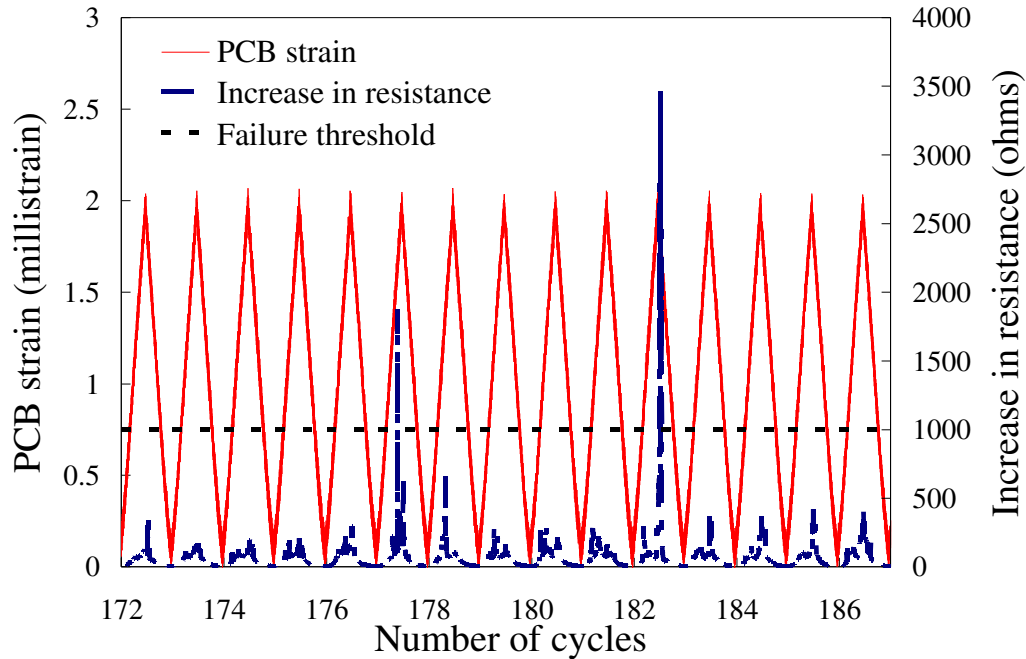
Figure 32: Sample plot of number of cycle to failure in the cyclic bending test on the aged specimen (at a strain rate of 1x10^{-3} sec^{-1})

Fifty percentage of the overstress limit was set as the target peak strain in the high strain rate impact tests. The test conditions in the impact tests were more difficult to control due to the transient nature of the test, but they were very consistent for each individual specimen. For the as-reflowed specimens, the peak strains were maintained within 23 percent of the target strain of 3.4 millistrain. The strain rates were more than 1 sec^{-1}, which were 2 or 3 orders of magnitude higher than the highest strain rate achieved in the cyclic bend tests. For the aged specimens, the peak strains were kept within 11 percent of the target value of 1.8 millistrain, while the strain rates averaged around 0.6 sec^{-1}.

A sample plot of the solder daisy chain resistance and strain in the impact test on an aged specimen at a strain rate of 0.6 sec^{-1} is shown in Figure 33. The heavy solid line represents the strain curve. This impact event generated a failure of the solder daisy chain, which can be observed as an increase in daisy chain resistance at the peak strain.

Subsequent to the impact event the solder daisy chain voltage returned to its original value. This observation underscores the importance of real-time daisy chain monitoring, since the failure would not be evident in the unloaded state.
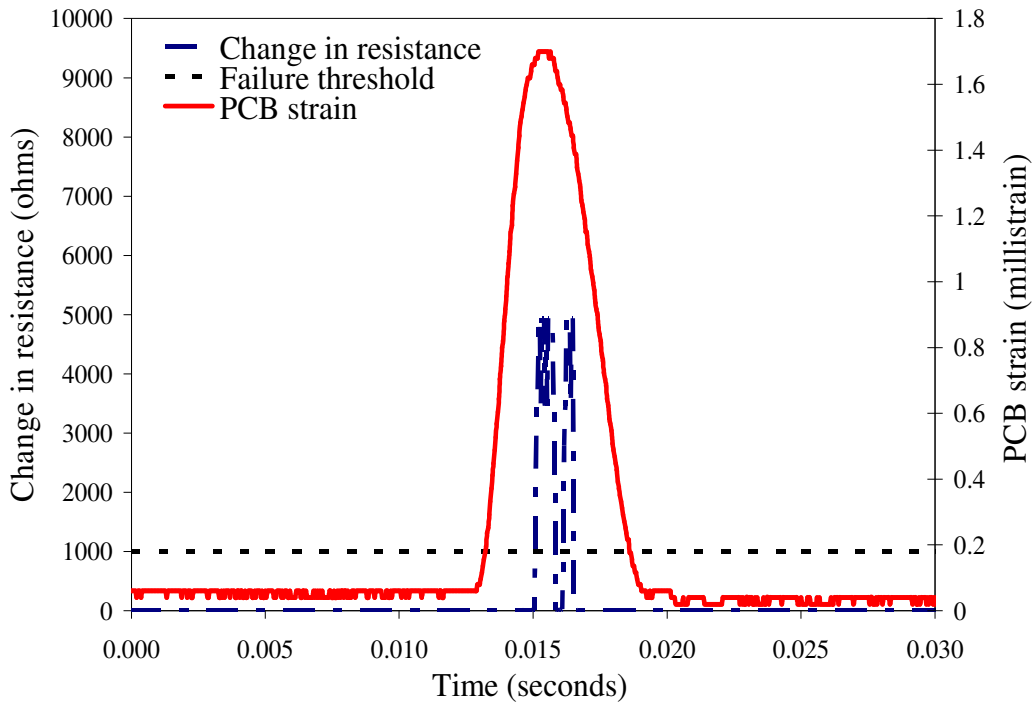
Figure 33: Sample plot of PCB strain and increase in resistance of solder daisy chain during an impact test on an aged specimen at a strain rate of 0.6 sec^{-1}

The number of cycles to failure of test specimens in the cyclic bending tests has been summarized in Table 5. Four as-reflowed and seven aged test boards were subjected to the cyclic bending. The second and third columns of Table 5 list the test conditions of peak strain and strain rate. For the two daisy chains in each package, the cycles to failure for the daisy chain which failed first has been reported as the cycles to failure for that package. The last column of the table is the number of cycles to failure of each board, which is the average number for the four packages on each test board.

Table 5: Summary of number of cycles to failure on the bend test boards in the cyclic bend test

As-reflowed Specimens

Board No.	Peak Strain (millistrain)	Strain Rate (millistrain/sec)	Number of Cycles to Failure				
			Package1	Package2	Package 3	Package 4	**Average**
1	5.70	0.87	5	5	8	5	**6**
2	4.14	0.94	18	23	33	17	**23**
3	4.40	9.78	23	28	41	17	**27**
4	2.40	1.07	810	825	885	835	**839**

Aged Specimens

Board No.	Peak Strain (millistrain)	Strain Rate (millistrain/sec)	Number of Cycles to Failure				
			Package1	Package2	Package 3	Package 4	**Average**
5	3.04	1.00	7	32	9	15	**16**
6	2.06	1.02	177	199	26	130	**133**
7	2.01	0.99	112	176	197	332	**204**
8	2.00	10.00	125	161	47	75	**102**
9	1.06	1.06	1312	2500	628	2500	**1735**
10	0.33	40.75	2926	2530	460	3777	**2423**
11	2.06	0.34	273	294	277	233	**269**

The number of impacts to failure in the high speed tests has been summarized in Table 6. Fifty percent of the overstress limit was set as the target peak strain in the tests. On each specimen, the peak strains (shown in the second column of Table 6) are the average value from multiple impacts. For the as-reflowed specimens, the peak strains were maintained within 23 percent of the target strain of 3.4 millistrain. The strain rates were more than 1 sec^{-1}, which was 2 or 3 orders of magnitude higher than the highest strain rate achieved in the cyclic bending tests. The number of impacts to failure varied a lot, as shown in the last column of Table 6. For the aged specimens, peak strains were kept within 11 percent of the target value of 1.8 millistrain, while strain rates averaged about 0.7 sec^{-1}. The number of impacts to failure was very close each other.

Table 6: Summary of number of drops to failure in the impact test

As-reflowed specimens

Board No.	Peak strain (millistrain)	Strain rate (1/sec)	Number of Drops to Failure
1	4.2	2.1	6
2	3.7	1.9	80

Aged specimens

Board No.	Peak strain (millistrain)	Strain rate (1/sec)	Number of Drops to Failure
4	1.8	0.7	6
5	1.8	0.6	5

5. Chapter Five: Failure Analysis

Failure analysis was systematically conducted on failed specimens to determine the critical failure site, the location where the failure first occurred. The process begins with the most non-destructive techniques and then proceeds to the more destructive techniques, allowing the gathering of unique data from each technique throughout the process. The recommended sequence of procedures is: visual inspection, electrical testing, non-destructive evaluation and destructive evaluation.

There were two daisy chains in each package. One was the die daisy chain. The other was the solder daisy chain. The mechanical testing was continued until all packages on the each board failed. Failure analysis was performed on the failed specimens to identify the critical failure sites under each test conditions.

In this chapter, different failure analysis techniques that are useful of stacked die BGA packages investigation are briefly described. Critical failure sites of test specimens under all test conditions are identified. Critical failure sites were limited to the interconnect system between the package and PCB under tested dynamic loading conditions. During the tests, most packages failed first in the solder daisy chain, but a small fraction of them failed first in the die daisy chain. The packages which failed first in the die daisy chain also failed in interconnects without internal failure sites associated die stacking architecture verified by different failure analysis techniques.

5.1. Failure Analysis Techniques

Based on the potential failure sites in the stacked die BGA assemblies, some failure analysis techniques were selected to investigate the failed test specimens. Scanning acoustic microscopy (SAM) and X-ray were very powerful non-destructive tools for pinpointing internal failure sites in the package. Many destructive failure analysis techniques were also adopted. Decapsulation was employed to observe the failures in wire bond and die surface directly. It can also verify the results obtained from indirectly non-destructive analysis. Dye-and-pry test can reveal failure sites in solder joints and allow correlation of failure site within each solder joint to position of solder joints on BGA package. Cross-Sectioning of solder joint followed by Scanning Electron Microscopy (SEM) / Energy Dispersive X-ray Spectroscopy (EDS) can perform morphologic and compositional analysis, can also provide information on the dimensions of die, interconnects, die attach materials, and other internal features.

5.1.1. SAM

SAM is a non-destructive failure analysis technique, which uses acoustic impedance to produce high resolution images of a specimen's interior structure to detect defects, such as interfacial delamination, die attach voiding, die tilt, etc.

Based on acoustic microscope principles, density changes at interfaces reflect sound back in varying amount. If air is present at an interface, all of the ultrasound is reflected back since air has an acoustic impedance of zero. However, there are some limitations of this technique if it is applied to stacked die package.

- The signals between different interfaces are not separated well enough if the thickness of each layer is too thin.
- Signal propagation is weakened progressively through multi-layers structure and epoxy molding compound with high filler loading.

There is always a tradeoff between using high frequency and low frequency transducers. High frequency transducer can provide better signal separation, but it has smaller depths of penetration than the low frequency transducer since it attenuates more. Materials like epoxy molding compound attenuate the signal greatly compared with materials like silicon, which are mostly homogenous. Low frequency transducer is needed for the encapsulated packages because the filler in the molding compound attenuates the signal greatly, but it is usually not sufficient for signal separation.

5.1.2.   X-ray Microscopy

X-ray microscopy permits nondestructive assessment of internal damage, defects, and degradation in microelectronic packages. Illuminating a sample with X-ray energy provides images based on material density that allows characterization of solder voiding, wire sweep, and wire bond breakage in packages. Used in conjunction with SAM, X-ray is a powerful non-destructive tool for pinpointing internal failure sites in electronic packages.

Manufacturing of stacked die package is faced with the task of creating bond wire profile with insufficient clearance due to dimensional constraints. X-ray inspection is a fast and easy way to examine the wire bonding issues like wire sweep. Typical 2-D X-ray

inspection systems are not able to distinguish elevations or 3-D features, and are not viable inspection systems for stacked die package [44].

5.1.3. Decapsulation

An optimum decapsulation procedure must be fast, clean, and leave the exposed device electrically unaltered [45]. This technique is a very useful tool to identify the internal failure sites within the stacked die package, such as broken wire, fractured bonding, and die cracking.

Chemical decapsulation must be carried out in an exhaust hood and the necessary equipment consists of rubber gloves, smock, small milling machine, hot plate, some clamping material and a dropper. The red fuming nitride acid and sulfuric acid are commonly used solvents to remove the epoxy molding compound. The procedure is described briefly as below:

- The package is X-rayed in a side view to determine the height of the bond wire loops within the package.

- A cavity is milled in the top of the package above the die to within 25 to 75 micron of the tip of the bonding wires (Care should be taken since the clearance is very small in stacked die package.)

- After milling, the device is placed on a hot plate set at approximately $140{\sim}200^{o}C$ according to different epoxy molding compound material. (In this work, the molding compound material is Sumitomo EME7730L. Hot plate is set to $200^{o}C$).

- The machined cavity is then filled with a few drops of acid. These drops are allowed to work until foaming action slows down (30 seconds). They are then followed by a replenishment of a few drops.

- Between these drops of acid it is advisable to clean the package which may be done by submerging it in acetone.

- Final cleaning may be done ultrasonically in acetone too.

Plasma etching is an other decapsulation techniques, which is very slow compare to chemical etching, but it is clean, and works on all types of epoxy materials. It needs mechanical thinning by grinding parallel to the chip surface, which destroys the bond wires or by milling a cavity above the chip surface which leaves the wire intact but makes etch times much longer (typically 8 hours).

5.1.4. Dye-and-Pry Test

Dye-and-pry test was used to reveal failure sites in solder joints and allow correlation of failure site within each solder joint to position of solder joints on a BGA package. The test procedure is listed as below.

- Ultrasonic clean test specimen with IPA for 3-5 minutes, and then dry it

- Apply red dye using dropper around the package with one-side or two-side application

- Apply vacuum 2-3 times to help dye penetration, and dry it at room temperature or a little bit higher temperature

- Take off the package from PCB

- Identify fractured area from red dye residue.

5.1.5. Cross Sectioning Analysis

Once the failure is identified, usually through electrical testing and visual inspection, cross sectioning is often necessary to identify the exact failure sites or failure mechanisms. Cross sectioning is a failure analysis technique for mechanically exposing the plane of interest for examining the internal construction, microstructure, characterizing degradation and quality assessment. Analysis of the polished cross sectioned surface can be performed using a variety of techniques, such as optical and electron microscopy and EDS.

Cross sectioning is very useful failure analysis technique for stacked die components, which can be used to inspect intermetallic compound growth, solder joint fracture, interfacial delamination and die cracking issues. As mentioned above, non-destructive failure analysis, SAM might be a useful technique for interfacial delamination. Cross sectioning analysis can be used to further verify the results obtained from SAM inspection.

To examine the internal failure sites of stacked die package, it is very easy to damage the die during cross-sectioning due to the thin thickness of each die. During grinding step, avoid using sandpaper which is coarser than 240 grit. There is a very high probability that 60 and 120 grit can harm the specimen or crack the die. It is important that sand paper coarser than 600 grits can not be used to grind the die.

Interconnection integrity of stacked die package can be inspected by performing cross-sectioning analysis. To examine the first level wire bonding interconnection, care must be exercised in the grinding steps since to avoid accidentally grounding the desired location. Complicated bond wire layout in the stacked die package makes it more difficult. Knowledge regarding the structure of the package is very helpful, which can be obtained from X-ray microscopy inspection.

5.1.6. SEM/EDS

The SEM combined with EDS is a powerful and versatile failure analysis tool to provide both compositional and morphologic information of the surface of interest qualitatively or quantitatively. SEM/EDS can be used to identify the fractured solder joint, intermetallic growth, grain size of solder, etc.

When the electrons strike the sample, a variety of signals are generated, and it is the detection of specific signals which produces an image or a sample's elemental composition. The three signals which provide the greatest amount of information in SEM are the secondary electrons (SE), backscattered electrons (BSE), and X-rays.

The main principle of SEM is when a beam of electrons is focused and hits its target, elastic and inelastic scattering events follow. Usually there are two detectors for SEM. One is used to measure BSE; the other is for SE. While the majority of the incident electrons eventually deposit all their energy in the target, a significant fraction undergo sufficient multiple elastic scattering that they exit the specimen back through the target surface as BSE. The amount of energy possessed by the BSE depends on the atomic

number of the specimen and the angle of the incidence on the target, which makes BSE a convolution of both composition and surface topology. Typically, separation of material by backscattering is observed when the difference in atomic number is at least two or three. Inelastic scattering transfers energy from the incident electrons energy to the atoms of the specimen, thus causing a number of secondary effects. SE are formed by the specimen's valence band or conduction band electrons, which obtain enough energy from the beam electrons to escape the specimen with low energies (0-50eV). They contribute significantly to the topographic contrast but are rather insensitive to the atomic number of the specimen material.

Interaction of the primary beam with atoms in the sample causes shell transitions which result in the emission of an X-ray. The emitted X-ray has an energy characteristic of the parent element. Detection and measurement of the energy permits elemental analysis EDS can provide rapid qualitative, or with adequate standards, quantitative analysis of elemental composition with a sampling depth of 1-2 microns. X-rays may also be used to form maps or line profiles, showing the elemental distribution in a sample surface.

5.2. _Critical Failure Site Identification_

In this work, no failure sites were detected that were associated specifically with the stacked die architecture for the range of dynamic loading conditions evaluated. Failure sites were confined to the interconnect system (second level interconnection) in all cases.

5.2.1. Solder Joint Failure

Since cyclic bend testing was continued until all four packages on each board failed the initial failure sites for three of the packages on each cyclic bending test board could not be determined directly by observation. Instead, these were inferred from the geometry of the board and the location of the die shadow area and verified by failure analysis on the last package to fail.

The die shadow area covered the outermost two or three columns of the solder joints. In a stacked die package the total package thickness occupied by dies is normally higher than for a single-die package. In this study, the total thickness of the die stack of the test specimen was 0.67 mm, whereas the die thickness in a single die BGA package normally ranges from 0.3 to 0.5 mm. Due to the stiffening effect of the package and the die shadow area, the critical solder joint failures should be within the three outermost columns along the two edges parallel to the loading bar. Dye-and-pry testing was used to obtain the spatial distribution of failure sites on the last failed package on the board which confirmed this judgment regarding the location of the critical failed solder joints.
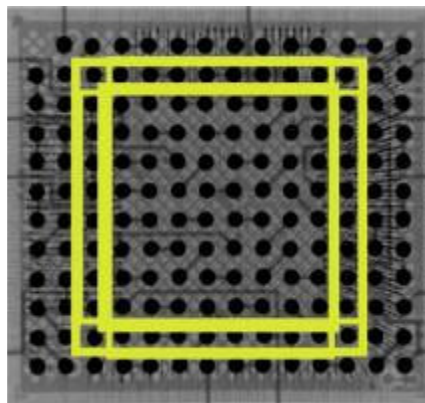
Figure 34: Die shadow area (each box indicates one die, picture is drawn to scale)
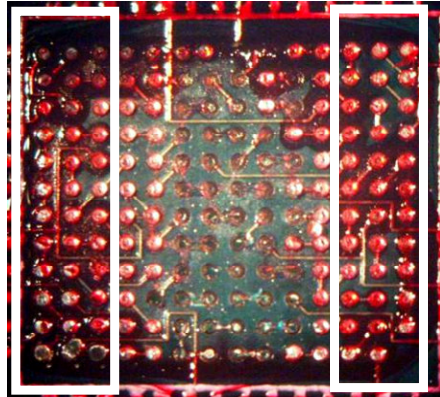
Figure 35: Dye-and-pry test result on the PCB side showing failure distribution

Based on dye-and-pry testing combined with cross-sectional analysis, for peak strain amplitudes above 3 to 4 millistrain the dominant failure sites of as-reflowed specimens were in the FR4 laminate and copper trace, as represented by Figure 36. Below the peak strain amplitude of 3 to 4 millistrain, the failure site changed to the bulk solder as shown in Figure 37. Aged samples, with a thicker intermetallic layer than as-reflowed specimens, failed in the intermetallic layer between the pad and the bulk solder for all tested values of PCB flexural strain and strain rate. Figure 38 indicates a brittle facture, which was dominant in the aged specimens. The crack was observed to penetrate the IMC layer on the package bond pad.
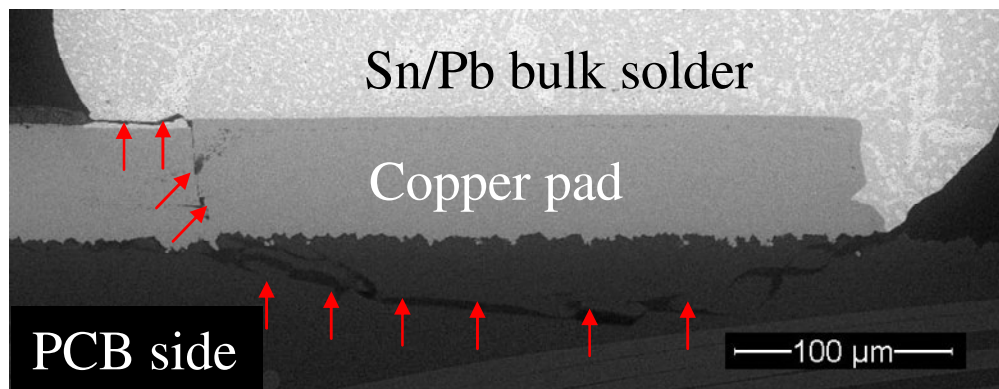
Figure 36: Fracture in the PCB substrate and copper trace on the PCB side of an as-reflowed specimen
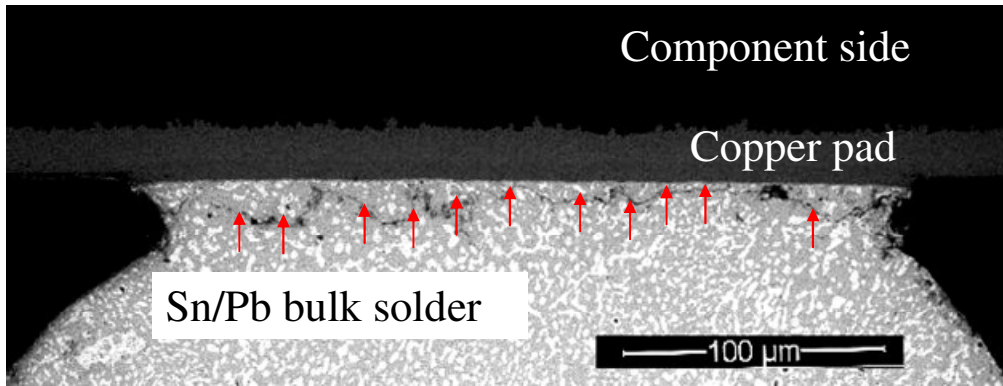
Figure 37: Fracture in the bulk solder on the package side of an as-reflowed specimen
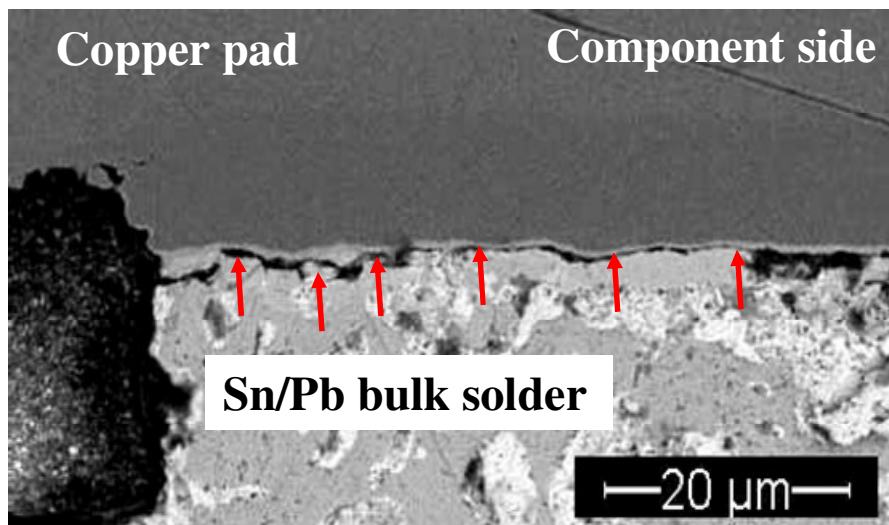
Figure 38: Fracture in the IMC layer on the package side of an aged specimen

Compositional analysis using SEM/EDS was applied to localize the failure site in the aged specimens. Compositional analysis on the fracture surface along the crack is shown in Figure 39. The ratio of atomic percentages indicates that the composition on the fracture surface of the package side is Ni_3Sn_4 and on the bulk solder side is $AuNi_{0.5}Sn_4$. The determination of the stoichiometry of these two phases is consistent with [41].
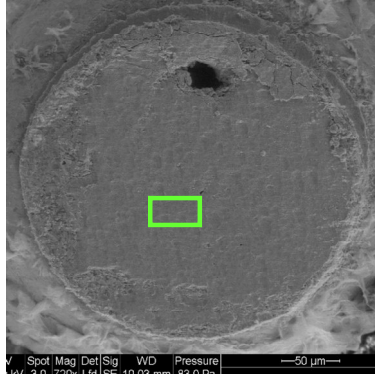
Figure 28 (a): SEM micrograph of
fractured surface, PCB side
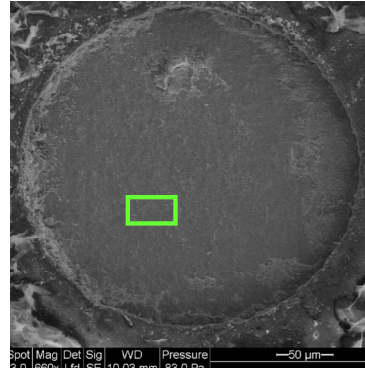
Figure 28 (b): SEM micrograph of
fractured surface, component side

Element	Weight%	Atomic%
Ni	4.3 ± 0.4	8.9
Sn	78.4 ± 1.0	80.4
Au	17.3 ± 1.0	10.7
Totals	100.0	100.0

Figure 8 (c): EDS compostional analysis on
fractured surface, PCB side

Element	Weight%	Atomic%
Ni	38.4 ± 0.7	55.4
Cu	1.7 ± 0.4	2.3
Sn	58.6 ± 0.8	41.8
Au	1.2 ± 0.8	0.5
Totals	100.0	100.0

Figure 8 (d): EDS compositional analysis on
fractured surface, component side

Figure 39: Compositional analysis of the fracture surfaces of an aged specimen

5.2.2.   Wire Bond and Silicon Die Failure

It is valuable to understand whether the resistance change in the die daisy chain was due to failures inside the package. Non-destructive analyses, SAM and X-ray inspection, were performed first, and was followed by decapsulation analysis on the failed specimens in which the die daisy chain failed first. Decapsulation analysis was used to verify the results from non-destructive analysis. Based on the analysis, no internal failure sites were identified in these stacked die package.

X-ray microscopy was used to investigate the first level interconnection integrity. Figure 40 and Figure 41 show the 2D and 3D x-ray images of the same failed stacked die package. By comparing these two figures, the 3D X-ray image can provide higher

resolution than the 2D X-ray. No wire bond failure was observed in this specimen. The result was further verified by the decapsulation analysis.
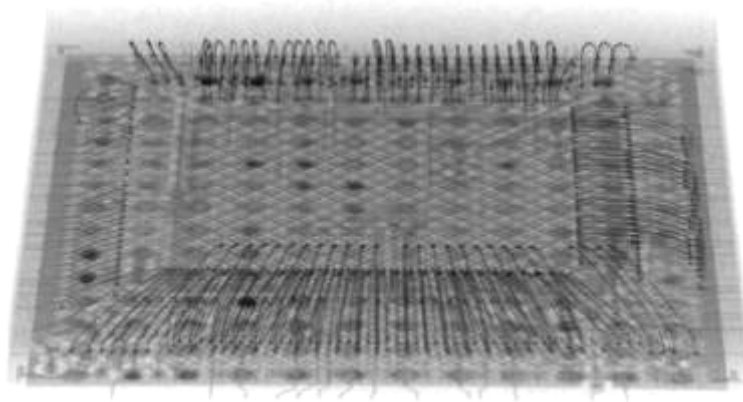
Figure 40: Wire bond profile of a failed stacked die package (2D X-ray image)
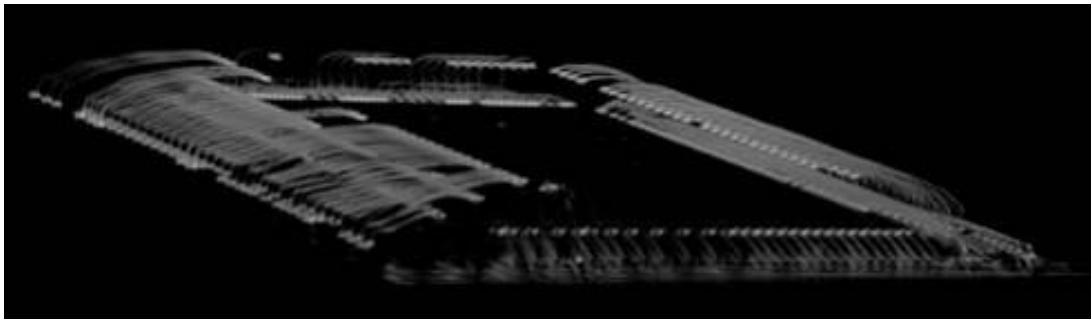
Figure 41: Wire bond profile of a failed stacked die package (3D X-ray image)

SAM with 35 MHz transducer was selected to analyze the test specimens since it can provide the best resolution of the SAM images. 15 MHz transducer could not provide the signal separation required to separate the different layers of the stacked die architecture. The transducers with frequencies greater than 110 MHz provide the resolution necessary for bare die structure, but attenuation from epoxy molding compound does not allow use of those high frequency transducers.
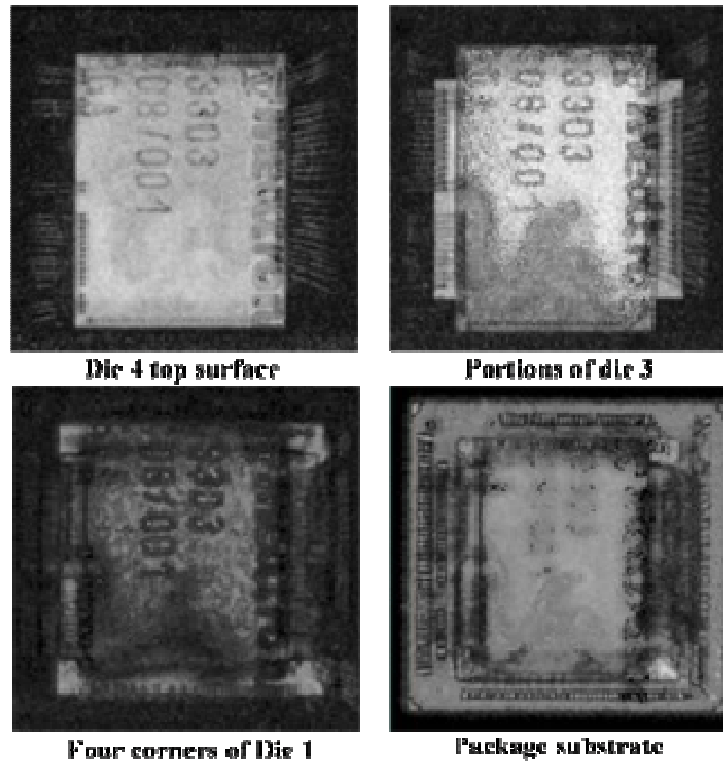
Figure 42: Scanning acoustic micrographs of a failed specimen using 35MHz transducer with focal length of 12mm

No delamination or void was found on these specimens. Figure 42 shows the scanning acoustic micrographs at the interfaces of a failed specimen. Die 4 surface, die 3 overhang portions, corners of die 1 and bond fingers on the substrate were identified. The center areas of die 1, die 2 and die 4 could not be identified due to the interference of echoes from different layers. Cross-sectional analysis was used to verify the test results, which is in good agreement with SAM images.

Decapsulation analysis was conducted on the failed specimens, in which the die daisy chain failed first. However, no wire bond breakage, wire sweep, wire bond detached or die cracking phenomena were observed. The decapsulation results of test specimens are shown in Figure 43 and Figure 44
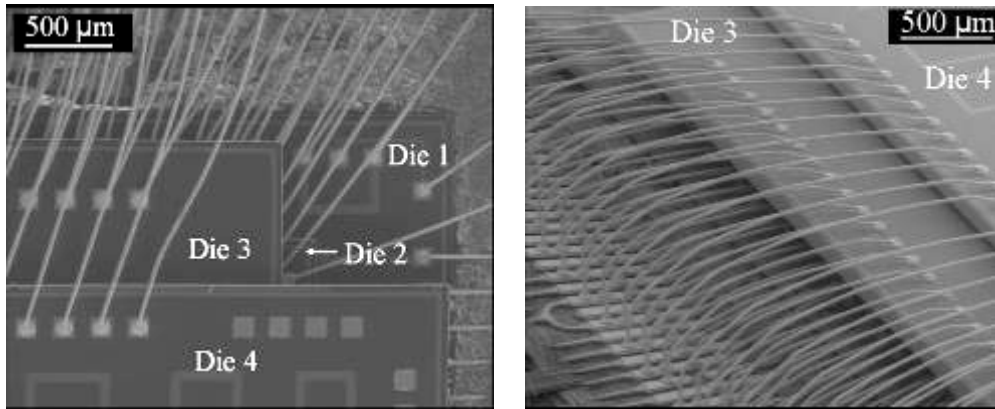
Figure 43: Decapsulation of a failed specimen: top view (left) and side view (right)
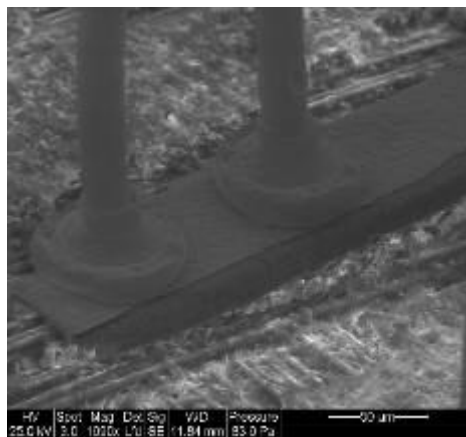
Figure 44: Decapsulation of a failed specimen: ball bonding

Cross-sectional analysis was performed, followed by SEM observation on these suspicious specimens. Some small die attach voids were found on one specimen in the die attach material as shown in Figure 45, which should be formed during die attachment process. These voids did not become the initial point for delamination or die cracking issues under the tested bending loads. Some small interfacial delamination was observed between the die attach material and epoxy molding compound as shown in Figure 46. These observations can not induce the electrical failure in the die daisy chain, so they are not the failure of interest.
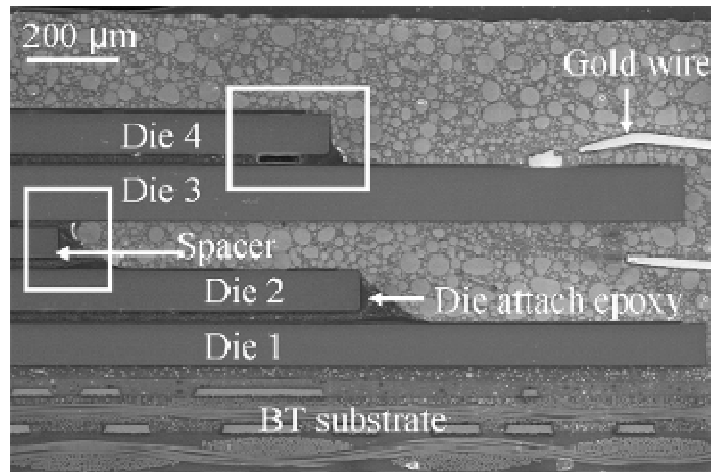
Figure 45: Cross sectioning of a failed specimen showing delamination and die attach voiding
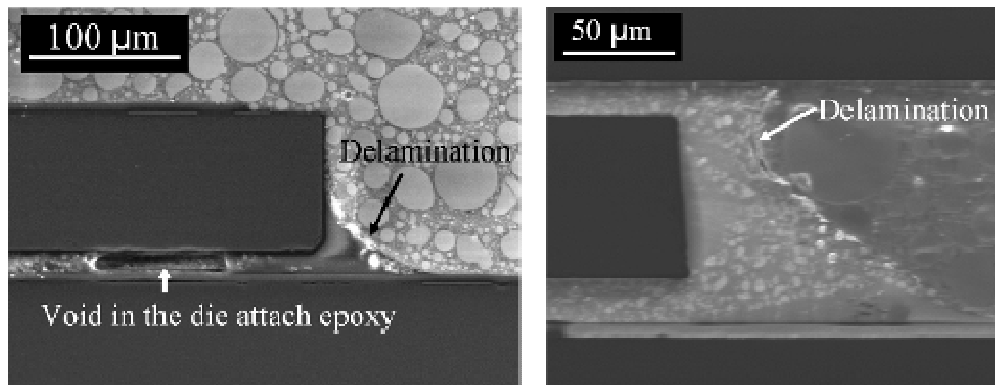
Figure 46: Close-up of the figure 45

6. Chapter Six: Discussion

The specimen response under dynamic loading conditions has been quantified in terms of the PCB flexural strain and strain rate. For both as-reflowed and aged specimens, experimental data from cyclic bending tests at three strain amplitudes with a constant strain rate ($1x10^{-3}$ sec^{-1}) has been used to obtain the relationship between cycles to failure and strain amplitude. The durability of specimens, both as-reflowed and aged, decreased monotonically with increasing PCB flexural peak strain. The aged specimens had lower durability than as-reflowed specimens. For both as-reflowed and aged specimens, experimental data from cyclic bending tests has been combined with the data from impact tests to obtain the relationship between cycles to failure and strain rate over nearly four orders of magnitude in the strain rate ($3x10^{-4}$ to 2 sec^{-1}). The durability of aged specimens decreased monotonically with increasing printed circuit board (PCB) flexural strain rate, while the durability of as-reflowed specimens increased slightly with increasing strain rate.

In this chapter, the PCB flexural strain and strain rate effects on the durability of stacked die BGA assemblies are discussed in detail [46] [47]. The failure sites associated with each test condition are identified and a failure site transition phenomenon is reported in this chapter.

6.1. *PCB Strain Dependent Effects*

The durability of specimens, both as-reflowed and aged, decreased monotonically with increasing PCB flexural peak strain at a fixed strain rate ($1x10^{-3}$sec^{-1}). The aged

specimens had lower durability than as-reflowed specimens. The as-reflowed specimens showed a transition in the failure site from the bulk solder to the FR4 laminate and copper trace with increasing PCB strain. The aged samples failed in the intermetallic layers for all values of tested PCB flexural strain. These test results are represented in Figure 47. Data points represent mean values and error bars indicate maximum and minimum values of each test condition.

Figure 47: Durability and failure site transition in terms of PCB peak strain

Figure 47 shows that there is a transition region, which is approximately 3 to 4 millistrain. Above this transition region, failure sites are limited to the copper trace and FR-4 laminate. Below this region, the failure site is at the solder joint, but for the as-reflowed specimens the failure site is in the bulk solder, whereas for the aged specimens the failure site is in the IMC layer.

The fatigue life of each material in an electronic assembly may be characterized by a relationship between cycles to failure (N) and strain range ($\Delta\varepsilon$). The materials with the lowest cycles to failure in the loading conditions represent potential failure sites of the whole assembly. The strain energy of deformation is divided among the potential failure sites. Under a specific loading condition the material with the lowest life will be the first material to fail, representing the dominant failure site.

The variation of cycles to failure with strain range will typically differ among the materials in an assembly, as a result of variations in characteristics such as fracture toughness, yield stress, elastic modulus, and work hardening behavior. As a consequence, the N-$\Delta\varepsilon$ curves may intersect as strain range varies (see Figure 48). This leads to transitions in the dominant failure site, such as those observed in the present investigation.
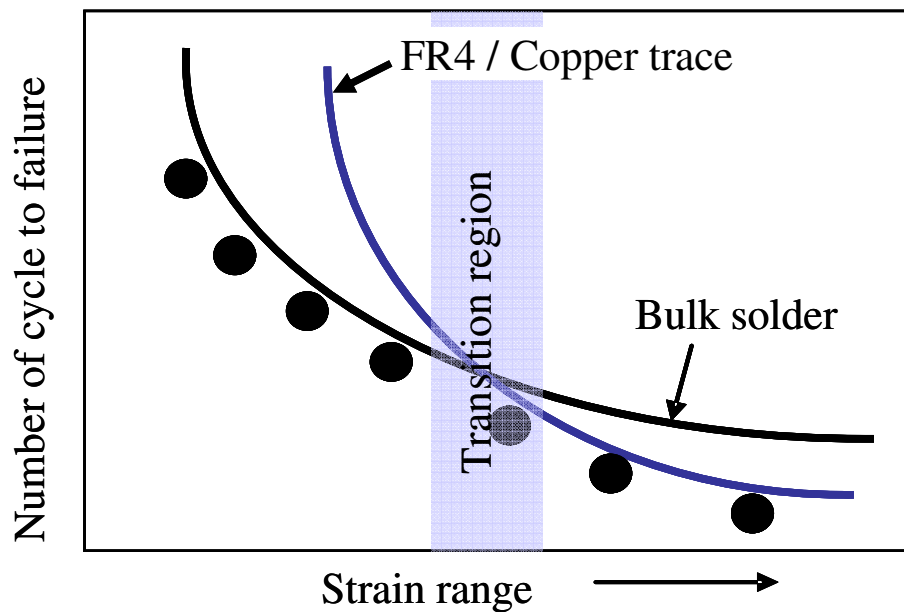
Figure 48: Schematic representation of competing fatigue curves of as-reflowed specimen

6.2. *PCB Strain Rate Dependent Effects*

The durability of test specimens has been quantified in terms of cycles to failure. Strain rate has a stronger effect on the aged specimens than on the as-reflowed specimens. Durability of the aged specimens decreased monotonically with increasing PCB flexural strain rate at a peak strain around 2 millistrain (50% of overstress limit). Durability of the as-reflowed specimens is not sensitive to PCB flexural strain rate at a peak strain around 4 millistrain (50% of overstress limit), and it shows a slightly increased trend with increasing strain rate. For the aged specimens, the failure sites were in the solder joint. Eutectic Sn/Pb Solder, being a rate dependent ductile material, shows increased elastic modulus. This implies that, at a constant strain amplitude, the stress built up in the IMC region increases with increasing strain rate. Therefore, for the aged specimens, the durability is dependent on the strain rate.

The dependence of the durability of test specimens on the PCB flexural strain rate is represented in Figure 49 using a log–log scale. Data points represent mean values and error bars indicate maximum and minimum values of each test condition.
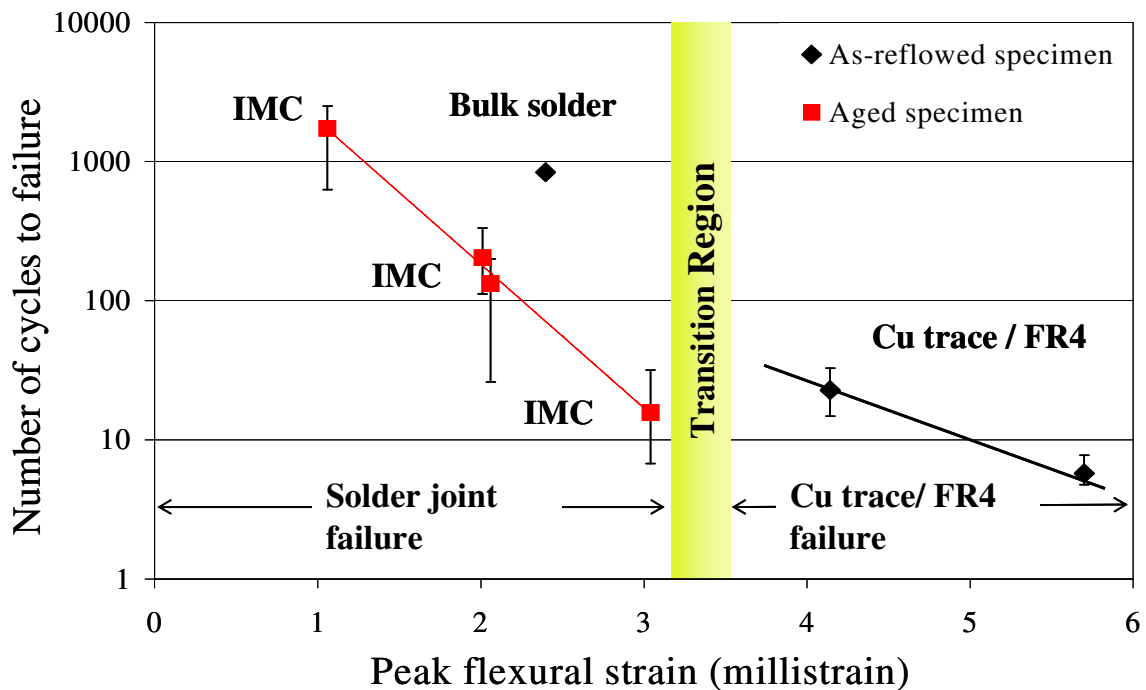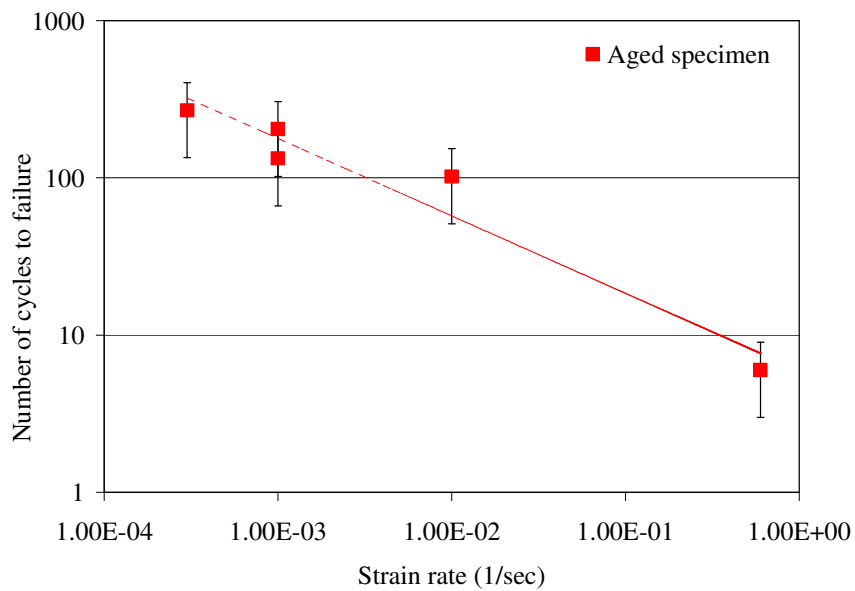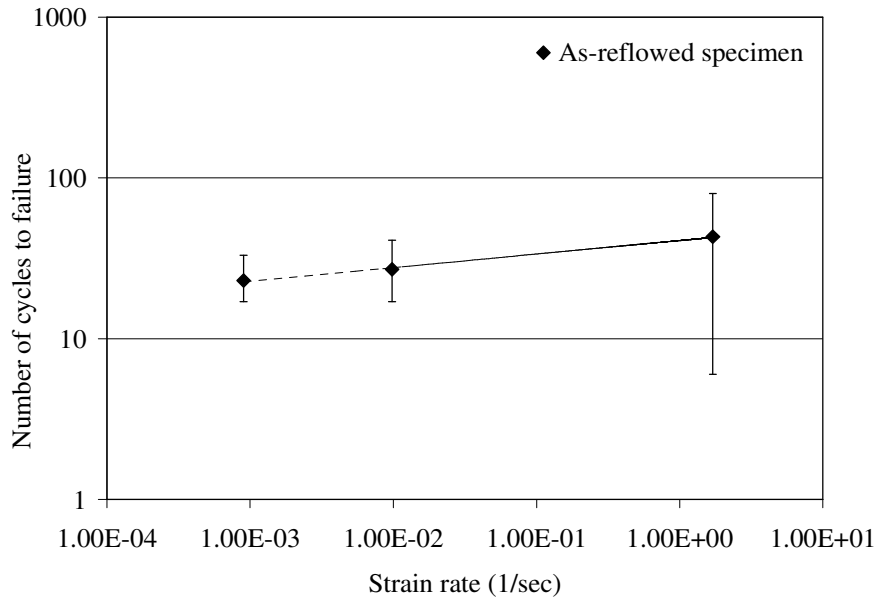
Figure 49: Durability in terms of PCB strain rate (50% of overstress strain limit)

For the as-reflowed specimens, over the entire range of tested strain rates the failure sites were in the FR4 laminate and copper trace. All of the aged specimens failed in the IMC layer by brittle fracture due to significant IMC layer formation after isothermal aging. In the constructional analysis, the results show that a 3 μm thickness IMC layer had grown

from the interface into the bulk. As the IMC thickness grows, the IMC grains get smaller and the individual IMC layers begin to have a continuous interface. The continuous layer of IMC is more brittle than the solder or copper trace, and thus the fracture toughness of the IMC layer decreases dramatically. In the as-reflowed specimen, a very thin IMC layer was detected, which is less than 1 μm. The presence of thin thickness of IMC indicates that a good bond has formed. The competing failure sites in the as-reflowed specimens are in the bulk solder and in FR4 laminate/Cu trace. The different weak points in as-reflowed and aged specimens lead to their different dominated failure sites in test conditions.

In the aged specimens, the crack was observed to penetrate within the IMC layer close to the package bond pad. The land pattern on the package side was SMD, thus that area constituted the bottleneck of the solder joint due to the small diameter. The pad finish on the package side was electrolytic gold over nickel plating. The two layer construction of the IMC can lead to failure sites within the IMC region. Previous studies with respect to electrolytic gold over nickel plating [37] [41] indicated that during thermal aging the Ni_3Sn_4 layer would thicken. Gold migrated from the bulk solder to the solder interface adjacent to the Ni_3Sn_4 intermetallic, and a ternary intermetallic phase, $(Au_{0.5}Ni_{0.5})Sn_4$, grew at the Ni_3Sn_4 and bulk solder interface (Figure 50). In the present study, there are several reasons that might be responsible for the observed brittle facture in the IMC. The presence of $(Au_{0.5}Ni_{0.5})Sn_4$ could decrease the fracture toughness of the joint during the bending test. The coexistence of these two phases ($(Au_{0.5}Ni_{0.5}) Sn_4$ and Ni_3Sn_4), with poor adhesion properties to each other might be responsible for the brittle fracture of the solder

joint. It has been reported [34] that there is a strong correlation between board bending reliability and Kirkendall voiding at the intermetallic compound (IMC) interface. Cross-sectional analysis was conducted on the as-received aged specimen. Some micro-voids were found within the IMC layer, which might degrade the mechanical reliability of the aged specimens.
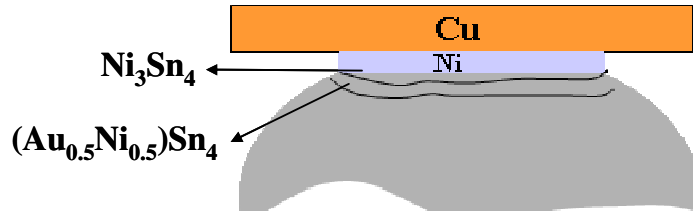
Figure 50: Schematic drawing of two-layer IMC structure on aged specimen on the package side

6.3. *Strain Effect vs. Strain Rate Effect in the Aged Specimens*

Failure analysis revealed that failure occurred by brittle fracture in the IMC region for all aged specimens under the tested conditions. An empirical durability estimation model developed in [49] was used to relate the fatigue life to the strain and strain rate.

Where the stress is less than the yield stress in the solder, the Basquin equation can be used to characterize the fatigue life of the solder joint interconnect.

$$N = a(\sigma)^{-b} \tag{1}$$

where

- σ is the stress amplitude

- a and b are empirical constants, which are structure and material-specific

- N is the number of cycles to failure

For overstress failure, N =1, $\sigma = \sigma_f$ (failure stress). Thus, $1 = a(\sigma_f)^{-b}$. By comparing this

equation with equation (1), the new equation takes the form,

$$\frac{N}{1} = \frac{a(\sigma)^{-b}}{a(\sigma_f)^{-b}} \tag{2}$$

Where, σ_f is the overstress limit in the monotonic bend test. The fatigue life of solder

joints in the aged specimens is dependent on the stress that the solder joint experiences.

Eutectic Sn/Pb Solder, being a rate dependent ductile material, shows increased elastic

modulus and decreased plastic deformation with increasing strain rate [48]. This implies

that, at a constant strain amplitude, the stress that the solder experiences increases with

increasing strain rate. The stress level built up in the IMC is dependent upon the strain

rate. For a given PCB assembly, the stress level in the solder joint changes with PCB

strain amplitude and strain rate following a power law or linear relationship in a small

range. The following derivation process is parallel to that in [49]. Therefore,

$$\sigma = f\left(\dot{\varepsilon}_{PWA}, \varepsilon_{PWA}\right) = k_1\left(\varepsilon_{PWA}\right)^{b_1}$$

$$where \qquad k_1 = c\left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-c_1} \tag{3}$$

Similarly,

$$\sigma_f = f\left(\dot{\varepsilon}_{PWA}, \varepsilon_{PWA}^{failure}\right) = k_s \varepsilon_{PWA}^{failure}$$

$$where \qquad k_2 = d\left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0}\right)^{-d_1} \tag{4}$$

where

- $A, B, C, k_1, k_2, c, c_1, d, d_1$: Damage model constants

- ε_f : Failure strain of the solder (-)

- ε_{PWA} : PWA flexural strain (-)

- $\varepsilon_{PWA}^{failure}$: PWA strain for overstress failure at quasi-static loading conditions (-)

- $\dot{\varepsilon}_{PWA}$: PWA flexural strain rate (sec^{-1})

- $\dot{\varepsilon}_0$: Quasi-static PWA strain rate (sec^{-1})

After substituting (3) and (4) into (2) and combining the constants, the equation takes the form

$$N = A \left(\frac{\varepsilon_{PWA}}{\varepsilon_{PWA_0}^{failure}} \right)^{-B} \left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0} \right)^{-C} \tag{5}$$

Let $B = bb_1$, $C = b(d_1 - c_1)$

The model was applied to the durability data of aged specimens. The model constants are architecture dependent and are empirically determined from dynamic testing. We applied the data from Table 5 of the aged specimens in (5) to obtain the model constants. The values of $\varepsilon_{PWA}^{failure}$ and $\dot{\varepsilon}_0$ are 3.6x10^{-3} and 1x10^{-3}sec^{-1} respectively, which were obtained from the overstress test. The damage constants, listed in Table 7, are valid only for the tested specimen because the damage metrics are structure-specific. A least squares fitting method was used to calculate the three unknowns from seven data ponits.

Table 7: Damage constants for the aged specimen during cyclic bend tests

Specimen	A	B	C
Aged specimen	29.84	2.85	0.53

After substituting the damage constants in the (5), we obtained equation (6). It indicates that the durability of aged specimen varied strongly with PWA strain and weakly with PWA strain rate.

$$N = 29.84 \left(\frac{\varepsilon_{PWA}}{\varepsilon_{PWA_0}^{failure}} \right)^{-2.85} \left(\frac{\dot{\varepsilon}_{PWA}}{\dot{\varepsilon}_0} \right)^{-0.53} \tag{6}$$

The data from Table 6 were used to obtain equation (6), allowing prediction of the durability under the high strain rate test condition. For instance, when $\varepsilon_{PWA} = 1.8$ millistrain and $\dot{\varepsilon}_{PWA} = 0.7$ sec^{-1}, the calculated N (number of drops to failure) is 7, which is very close to the experimental result of 6 drops. This indicates that equation (6) can be used to accurately predict bend test results over a wide range of strain rates, under the assumption that the failure sites remain constant in the solder joint.

7. Chapter Seven: Screening and Accelerated Testing

There are some recognized failures associated with stacked die packages, which are sensitive to the life cycle loads of products. Improper design or manufacturing processes can cause quality and reliability issues. Industry standard test methods like JEDEC, IPC, EIAJ are designed to access the quality and reliability of IC components, but may not be applicable for stacked die packages. Specialized qualification tests need to be designed to identify these risks.

Due to the increases of silicon volume percentage in the mold body, the risk for the moisture absorption has increased in the stacked die packages. One of the important acceleration factors for the failure of stacked die package is the combination of high humidity and high temperature conditions.

At the board level, PCB assembly and handling operation often include a number of steps involving monotonic bending and cyclic bending. Stacked die package response under bending loadings needs to be evaluated and compared against single die package to understand the effect of die stacking configuration. Multiple die stacking configurations can also lead to higher package stiffness, which might degrade the package reliability or reduce fatigue life under bending conditions. During assembly the number of repeated bend cycles is small, like in-circuit testing, but the magnitude of flexure can be significant. On the other hand, the actual use conditions such as repeated key-presses in mobile phone or MP3 players can result in a large number of repeated bend cycles during the life of the product, albeit at a low magnitude. Handheld electronic products containing stacked die packages are more prone to being dropped during their useful

service life because of the size and weight of product. The dropping can not only cause mechanical failures in the housing of the device but also create electrical failures in the printed circuit board assemblies mounted inside the housing due to transfer of energy through PCB supports.

Table 8 summarizes the JEDEC standards that can be applied to stacked die packages. These test methods focus on the temperature and humidity life cycle loads. The unbiased autoclave test (JESD22A102-C) can not be applied on laminated or tape based packages, including FR4 material, polyimide tape or equivalent. Therefore, it is not suitable for stacked die BGA packages. Unbiased HAST (JESD22A118) is an alternative to the unbiased autoclave using non-condensing conditions. For both methods, the combination of high humidity and high temperature (higher than glass transition temperature) may produce unrealistic material failures, because absorbed moisture typically decreases glass transition temperature for most polymeric materials. Thus, caution is needed. The temperature cycling test (JESD22A104-C) can be applied to both package and board level. Test conditions that exceed 125°C for sample temperature (max) are not recommended to Sn/Pb solder compositions.

Table 8: Quality and reliability tests at the package level

Number	Standard Name	Scope
JESD22A113-E	Preconditioning of Non-hermetic Surface Mount Device prior to Reliability Testing	It is a representative of a typical industry multiple solder reflow operation.
JESD22A102-C	Accelerated Moisture Resistance - Unbiased Autoclave	Saturated pressure; Not applied on laminate package
JESD22A118	Accelerated Moisture Resistance - Unbiased HAST	An alternative to unbiased autoclave; Under no-condensing conditions
JESD22A110-B	Highly-Accelerated Temperature and Humidity Stress Test (HAST)	It employs severe conditions of temperature, humidity, and bias.
JESD22A104-C	Temperature cycling	It can determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes.

The commonly used screening methods for stacked die packages include thermal cycling (2~5 cycles), moisture soaking/stream aging followed by reflow. Sometimes screening tests are applied to the products upon the requirement of customers. Thus manufacturers can increase the quality of products which are shipped. However, it is still desirable to eliminate the screening test since it usually can reduce useful life and increases the cost of production.

For the board level testing, the important life cycle loads focus on the flexural loadings, which come from assembly, shipping and use applications. Table 9 lists the tests listed in the JEDEC standards that can be applied to stacked die components at the board level. Correlations between these tests and field conditions are not fully established yet. Consequently, the test procedure is presently more appropriate for relative component performance than for use as a pass/fail criterion.

Table 9: Quality and reliability tests at the board level

Number	Standard Name	Scope
IPC/JEDEC-9702	Monotonic Bend Characterization of Board-Level Interconnects	It specifies a common method of establishing the fracture resistance of board-level device interconnects to flexural loading during non-cyclic board assembly and test operations
JESD22B113	Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products	It is intended to evaluate and compare the performance of surface mount electronic components in an accelerated test environment for handheld electronic products applications.
JESD22B111	Board Level Drop Test Method of Components for Handheld Electronic Products	It is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product application in an accelerated test environment, where excessive flexure of a circuit board causes produce failure.

To reduce defects in the packages, screening should be applied when necessary and accelerated testing should be designed to stress recognized causes of failures. Accelerated tests like HAST, unbiased autoclave and thermal cycling are most relevant to evaluate reliability of these products. It is important to make full use of available end-of-design experimental and modeling methods like environmental testing, mechanical testing, and simulation tools to optimize the design of stacked die packages.

8. Chapter Eight: Conclusions

Dynamic loading condition is an important feature of the usage environment of stacked die BGA packages. The durability of stacked die PBGA assemblies with tin-lead solder was evaluated by four-point bending tests and quantified in terms of number of cycles to failure or impacts to failure. For the range of dynamic loading conditions evaluated in this study, no failure sites were detected that were associated specifically with the stacked die architecture. This work reveals that the primary failure sites of stacked die BGA packages are in the interconnect system and not internal to the package under the test conditions.

Strain effects on durability were demonstrated and quantified at a fixed strain rate. The durability of specimens, both as-reflowed and aged, decreased monotonically with increasing PCB flexural strain. Aged samples, with a thicker intermetallic layer than as-reflowed specimens, had lower durability and failed in the intermetallic layer between the package pad and the bulk solder for all tested values of PCB flexural strain. These results demonstrate the importance of aging history to board-level reliability in dynamic loading conditions.

Strain rate effects on durability were demonstrated and quantified at a fixed peak strain. The durability of aged specimens decreased monotonically with increasing PCB flexural strain rate. The durability of as-reflowed specimens increased slightly with increasing PCB flexural strain rate. Over the range of tested PCB strain rates, 3×10^{-4} to 2 sec^{-1}, at a

fixed peak strain, as-reflowed specimens failed in the FR4 board laminate and copper trace, while aged specimens failed in the IMC layer.

A failure site transition was observed for the test vehicle. As the PCB flexural peak strain increased above the range of 3 to 4 millistrain, the failure site changed from solder joints to the FR-4 board and copper trace. Above this transition region, failure sites were limited to the copper trace and FR-4 laminate. Below this region, the failure site for all specimens was within the solder joint. For the as-reflowed specimens the failure site was in the bulk solder, while for the aged specimens the failure site was in the IMC layer. This phenomenon can be explained by the competing fatigue curves of different materials in a material set. The fatigue curves of different materials may cross each other in a certain strain range. This leads to transitions in the dominant failure site as strain range varies.

There are different failure sites for as-reflowed and aged specimens due to significant IMC layer formation after isothermal aging. For the as-reflowed specimens, over the entire range of tested PCB flexural strain and strain rates the failure sites were in the bulk solder or FR4 laminate and copper trace. All of the aged specimens failed in the IMC layer by brittle fracture. In the constructional analysis, the results show that a 3 μm thickness IMC layer had grown from the interface into the bulk. As the IMC thickness grows, the IMC grains get smaller and the individual IMC layers begin to have a continuous interface. The continuous layer of IMC is more brittle than the solder or copper trace, and thus the fracture toughness of the IMC layer decreases dramatically. In

the as-reflowed specimen, a very thin IMC layer was present at the interface, which indicates that a good bond had formed without compromising the solder joint reliability. The competing failure sites in the as-reflowed specimens are in bulk solder and in FR4 laminate/Cu trace. The different weak links between as-reflowed and aged specimens lead to their different primary failure sites under the range of test conditions.

For both as-reflowed and aged specimens, the dominated failure sites were close to the package bond pads. This could be explained by the different land pattern on the package and PCB side, and which were SMD and NSMD, respectively. The solder joint near the package side has a smaller diameter due to the size of solder mask opening therefore that area has the highest stress.

A durability estimation model developed by Dasgupta, et al. in [47] was applied to compare the strain dependent and strain rate dependent effects in durability of the aged specimen. Failure analysis revealed that the failure sites were consistent for all aged specimens under tested conditions. The analytical model indicated that the durability of aged specimens varied strongly with PWA strain and weakly with PWA strain rate. This model successfully predicted the durability of the test specimen under impact test with a high strain rate.

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